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Novel Nonvolatile Memories With Engineered Nanocrystal Floating Gate

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Bei Li

June 2010

Dissertation Committee:
Dr. Jianlin Liu, Chairperson
Dr. Cengiz Ozkan
Dr. Roger Lake

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Bei Li
2010

The Dissertation of Bei Li is approved:

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Committee Chairperson

University of California, Riverside

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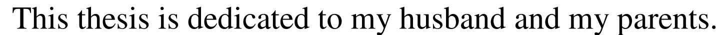
I would like to thank my parents for upporting me and encouraging me with their best wishes. Special thank to my husband, Dr. Qinghui Shao. He was always there cheering me up and stood by me through the good times and bad.


This thesis is dedicated to my husband and my parents.

ABSTRACT OF THE DISSERTATION

Novel Nonvolatile Memories With Engineered Nanocrystal Floating Gate

by

Bei Li

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, June 2010
Dr. Jianlin Liu, Chairperson

Tunnel oxide thickness scaling is encountering problem for next generation flash memory device. With tunnel oxide shrinking down, the stress-induced leakage current becomes more serious leading to degraded retention. To overcome this, flash memory with discrete-traps as floating gate was proposed, including nitride charging and nanocrystal storage. The first report on nanocrystal memory is Si nanocrystal memory. After that, tremendous efforts have been put on using semiconductor or metal nanocrystals for memory application. However, for Si, although long retention time has been demonstrated, the long retention is believed to be related to charge storage on defect levels. Those levels are distributed throughout the whole band gap of Si and are not thermally stable, resulting in compromised device reliability. For metals, on the other hand, the band gap is negligible, therefore the issue of defect

level charging is effectively avoided. However, the problem with metal nanocrystal memory lies in the reaction or inter-diffusion between metal and tunnel oxide underneath at high-temperature process step, such as source/drain dopant activation annealing for MOSFET. The reaction or diffusion of metal atoms generates weak points in the tunnel oxide, which degrades the device retention.

To solve the dilemma between long retention and scaled tunnel oxide, in this work, engineered floating gate, such as hybrid-nanocrystal and new materials nanocrystals that are compatible with current Si technology, was proposed and good memory performance was demonstrated. Chapter 1 introduces the conventional flash memory, including the operation principle, architectures, challenge in next generation flash memory and some new technologies to address this issue in conventional flash. Chapter 2 describes the methodologies used in this thesis work, including nanocrystal growth methods, nanocrystal characterization techniques, and nanocrystal memory fabrication and device characterization. Chapter 3 discusses the flash memory with Ge/Si hetero-nanocrystals as floating gate. Type-II band alignment between Ge and Si makes Ge/Si hetero-nanocrystal good for long time hole storage than Si nanocrystal memory. In addition to p-MOS, we also developed n-MOS memory with $CoSi_2$-coated Si nanocrystals as floating gate in the Chapter 4. The Fermi-level of $CoSi_2$ locates around the midgap of Si so that the device is good for both electrons and holes trapping. Furthermore, the quantum well formed between $CoSi_2$ and SiO_2 is deeper than that of Si and SiO_2, leading to an elongated retention time. The Si nanocrystal underneath the $CoSi_2$ effectively prevents the charges stored in $CoSi_2$ from leaking back to the channel. In order to lower the thermal budget to make silicide nanocrystals, vapor-solid-solid (VSS) growth mode was employed and $NiSi_2$ nanocrystsals were

synthesized as presented in Chapter 5. The long retention of $NiSi_2$ nanocrystal memory is also benefited from the deep quantum well between $NiSi_2$ and SiO_2. For next generation flash memory, more uniform nanocrystals with higher dot density, $10^{12}cm^{-2}$, is necessary to meet the requirement of 22nm technology and beyond. In Chapter 6, we developed PtSi nanocrystals using the similar synthesis technique as $NiSi_2$. The nanocrystal density is enhanced from $3\times10^{11}cm^{-2}$ to $1.5\times10^{12}cm^{-2}$.

In short, engineering the nano-floating gate by replacing Si nanocrystals with hybrid nanocrystals and silicide nanocrystals benefits the device retention time. These new memories also exhibit faster programming and erasing speeds. The enhanced memory performance makes the devices fit for next generation memory with further scaled tunnel oxide.

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Chapter 1: Introduction

1.1 Flash memory introduction

Flash memory, both NOR and NAND type, was invented by Dr. Fujio Masuoka at Toshiba in 1980. The name of "Flash" was suggested because the erasure process of the memory contents takes place in a large block. NOR type Flash was first commercialized by Intel Corporation in 1988. It has long erase and write times, but provides full address and data buses, allowing random access to any memory location. This makes it suitable for replacement of older Read-only memory (ROM) chips, which are used to store program code that rarely needs to be refreshed, such as computers' BIOS. Its endurance is up to 10^6 times of operation cycles. NOR-based flash was the basis of early flash-based removable media. CompactFlash was originally based on it, while later cards moved to less expensive NAND flash. NAND flash was first announced at 1987 IEDM. It shows faster erase and write times, and requires a smaller chip area per cell, allowing greater storage densities and lower costs per bit than NOR flash. It also has 10 times the endurance of NOR flash. However, the I/O interface of NAND flash does not allow a random access external address bus. Rather, data must be read on a block-wise basis, with typical block sizes of hundreds to thousands of bits. This means NAND flash is not suitable for a replacement for program ROM sicne most microprocessors and microcontrollers requires byte-level random access. Therefore, NAND flash is similar to other secondary storage devices, such as hard disk drives (HDD) for the use in mass-storage devices, such as memory cards.

Flash memory has been the dominant technology and has extremely wide applications in modern electronic systems, such as PDA (personal digital assistants), cellular phones, digital cameras, laptop computers, and global positioning systems. It has also gained popularity in console video game hardware, where it is often used instead of EEPROMs or battery-powered static RAM (SRAM) for game save data. In addition to the nonvolatility, flash memory offers fast read access times and better kinetic shock resistance than hard disks, which has mechanical moving parts to write/read the data. Another merit of flash memory is its extremely durable package, being able to withstand intense pressure, temperature and humidity.

Flash memory is a nonvolatile memory, with information stored in an array of memory cell in the form of floating gate transistors. Figure 1-1 shows the schematic device structure of conventional flash memory.

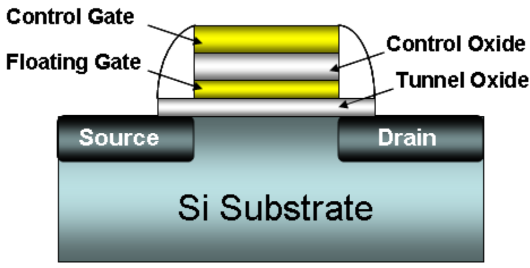


Figure 1-1 Schematic of conventional floating gate memory with a continuous poly-silicon layer as the charging node.

In traditional single-level cell (SLC) devices, each cell stores one bit of information. For multi-level cell, each device can store more than one bit. In conventional flash memory, the floating gate is a conductive layer of poly-silicon, embedded between two dielectric layers, such as SiO_2. Because the floating gate is electrically isolated by top and bottom dielectric layers, any electrons/holes stored on it are trapped and therefore under normal conditions, will not discharge for a very

long time. Flash memory works by sensing the MOSFET threshold voltage (V_T) shift to as programming and erasing the devices to define the logic status, “1” or “0”. When the floating gate is charged with carriers (electrons or holes), it will screen the electric field from the control gate, thus modifying the V_T of the cell. To read the cell, an intermediate voltage is applied to the control gate and the MOSFET channel becomes conducting or insulating, depending on the V_T of the cell, which is controlled by the charge on the floating gate. The best and fastest way to do this is by reading the current driven by the cell at a fixed gate bias. In fact, in the current-voltage plane two cells, respectively, logic “1” and “0” exhibit the same transconductance curve but are shifted by quantity, as shown in the I_D-V_G curves in Figure 1-2. The V_T shift is proportional to the stored electron charge. Figure 1-2 shows the memory cell energy diagrams and corresponding transfer characteristics under charged and discharged states.

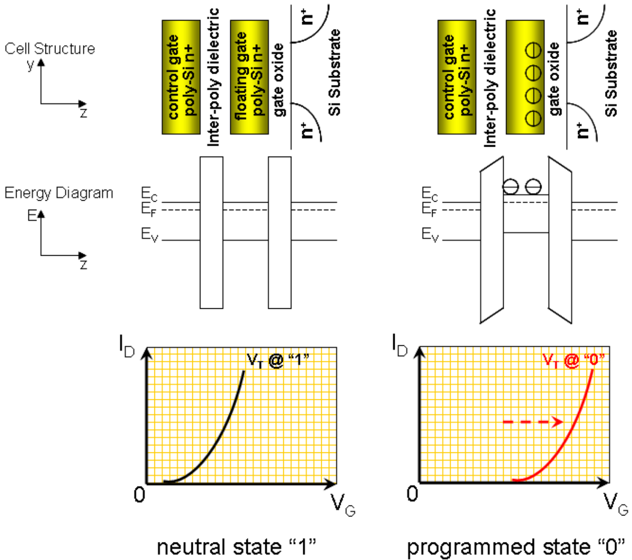


Figure 1-2 Schematic cell structures, energy band diagrams and their corresponding I_D-V_G characteristics of flash memory under neutral (un-charged) state “1” and programmed (charged) state “0”. With electrons charged on the floating gate, the V_T shifts to a larger value compared to the initial state.

1.2 NOR flash memory

The NOR flash name is related to the way the cells are arranged in an array, through rows and columns in a NOR-like structure. Flash cells sharing the same gate constitute the so-called wordline (WL), while those sharing the same drain electrode (one contact common to two cells) constitute the bitline (BL). In the internal circuit configuration of NOR flash, as shown in Figure 1-3, the individual memory cells are connected in parallel, which enables the device to achieve random access. This configuration enables the short read times required for the random access of microprocessor instructions. NOR flash is good for lower-density, high speed read applications, which are mostly read only, often referred to code-storage applications.

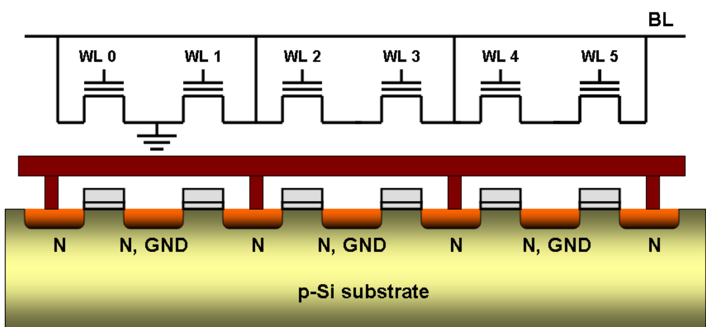
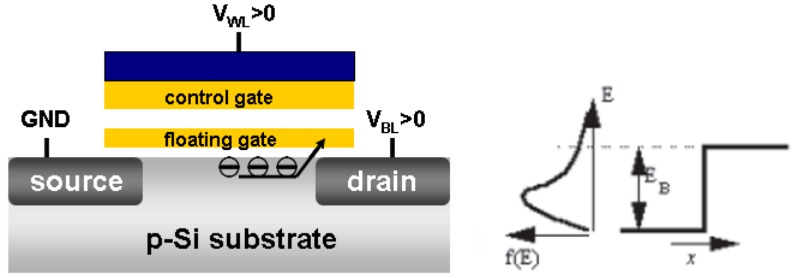


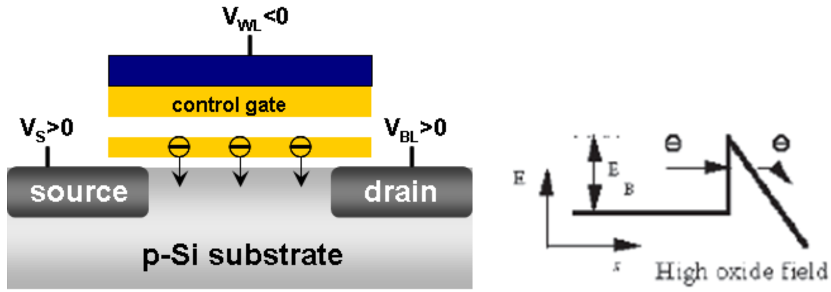
Figure 1-3 Architecture of NOR flash memory

Single-level NOR flash memory in its default state is logically equivalent to binary "1" state because current flows through the channel under application of an appropriate voltage to the control gate. The program procedure for NOR flash is first, biasing the control gate with an elevated on-voltage to turn on the channel with electrons flowing from the source to drain; then the source-drain current is sufficiently high to cause high energy electrons to jump over the barrier between floating gate and tunnel oxide via the process called hot carrier injection (HCI).

A NOR Flash memory cell is programmed by HCI in the floating gate at the drain side and it is erased by means of the Fowler-Nordheim (FN) electron tunneling through the tunnel oxide from the floating gate to the silicon surface. Figure 1-3 shows the scheme of NOR programming and erasing.



Device and energy diagram schematic of HCI programming



Device and energy diagram schematic of FN erasing

Figure 1-4 Device schematic showing the HCI programming and FN erasing for NOR flash memory. The energy band diagrams on the right shows the mechanism of electrons tunneling into and back from floating gate.

1.3 NAND flash memory

NAND Flash was developed as an alternative optimized for high-density data storage, giving up random access capability in a tradeoff to achieve a smaller cell size, which translates to a smaller chip size and lower cost-per-bit. This was achieved by creating an array of eight memory transistors connected in a series. Utilizing the NAND Flash architecture’s high storage density and smaller cell size, NAND Flash

systems enable faster write and erase by programming blocks of data. NAND Flash is ideal for low-cost, high-density, high-speed program/erase applications, often referred to as data-storage applications.

NAND flash also uses floating-gate transistors, but they are connected in a way that resembles a NAND gate: several transistors are connected in series, and only if all word lines are pulled high (above the transistors' V_T) is the bit line pulled low. These groups are then connected via some additional transistors to a NOR-style bit line array.

To read, most of the word lines are pulled up above the V_T of a programmed bit, while one of them is pulled up to just over the V_T of an erased bit. The series group will conduct (and pull the bit line low) if the selected bit has not been programmed. Figure 1-5 shows the NAND flash memory architecture.

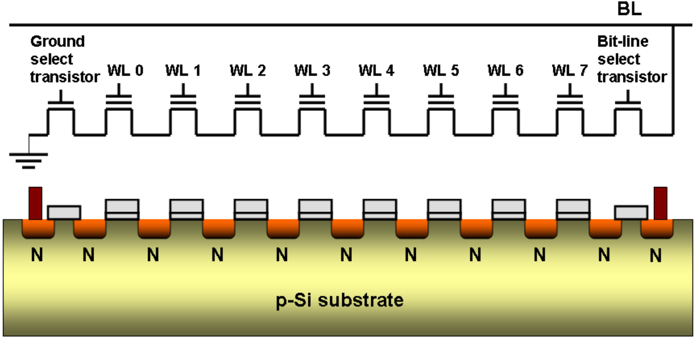
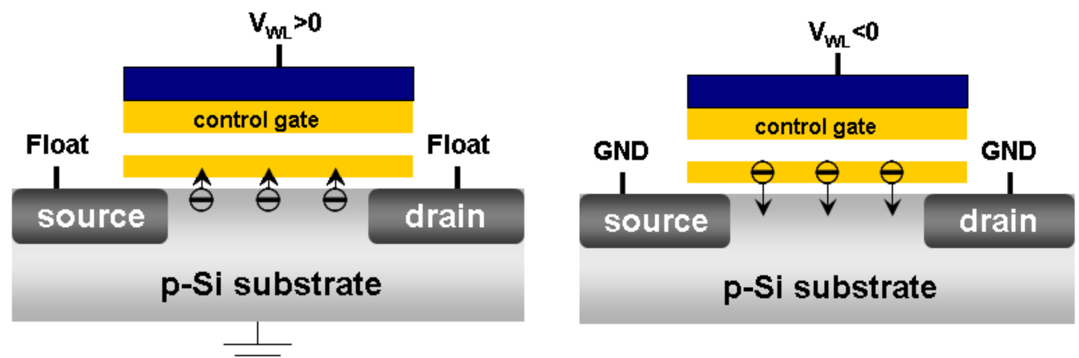


Figure 1-5 Architecture of NAND flash memory

Despite the additional transistors, the reduction in ground wires and bit lines allows a denser layout and greater storage capacity per chip. In addition, NAND flash is typically permitted to contain a certain number of faults (NOR flash, as is used for a BIOS ROM, is expected to be fault-free). NAND flash uses tunnel injection for writing and tunnel release for erasing. The operation schemes are shown in Figure 1-6.

NAND flash memory forms the core of the removable USB storage devices known as USB flash drives and most memory card formats available today.



NAND programming with FN tunneling NAND erasing with FN tunneling

Figure 1-6 Device schematic showing the FN programming and erasing for NAND flash memory.

1.4 Discrete trap flash memory

1.4.1 Comparison between nanocrystal and SONOS

An ideal memory would require high density, high speed for programming and erasing, low power consumption and nonvolatility. Flash memories are the most frequently used devices with nonvolatile properties. Since 1990s, flash memories are scaling following Moore's law. However, beyond 30nm technology node, this scaling is becoming more and more difficult because the reliability concerns have limited the bottom or tunnel oxide to a thickness of about 10nm. This in turn makes it difficult to lower the voltage necessary to operate the memory module.

As an alternative the replacement of the conductive floating gate node by not electrically communicating floating nodes has been investigated. The two main thrusts in this area are silicon nitride storage known as SONOS and nanocrystal storage. Because of the isolated nature of the floating gate, these approaches allow for thinner tunnel oxide and consequently more aggressive scaling of the flash memory.

In nanocrystal memory, a localized single leakage path due to a defect in the tunnel oxide can only drive a small portion of the charges stored on floating gate to the channel.

The most successful device in this category nowadays is the SONOS type (Semiconductor-oxide-nitride-oxide-semiconductor) structure, in which the insulator consists of a silicon nitride layer surrounded by silicon oxide layer, as shown in Figure 1-7. A significant advantage of SONOS type memories is the much smaller process complexity compared to forming nanocrystals of correct size and density and preserving them during subsequent processing.

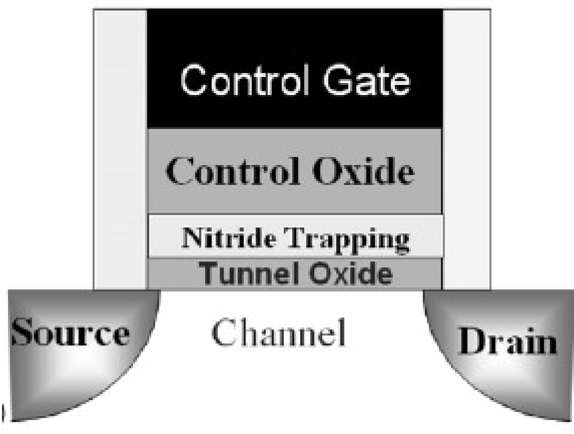


Figure 1-7 Device structure of SONOS memory

Another type of charge-trapping memory was proposed by S. Tiwari in 1996, where Si nanocrystals were employed as floating gate. Compared to SONOS cell, the NC cell exhibits several potential advantages: First deeper electron storage traps (~3eV) than nitride traps (1-2eV) improves electron retention within the nanocrystals. Second, the ability to physically observe the trap centers and obtain their number density and size somewhat mitigates the process complexity. Third, local field effects as well as Coulomb blockade are central to superior FN erase characteristics

compared to SONOS that enables standard HCI-FN NOR architecture. In SONOS, as the gate bias is increased, the FN erase proceeds faster but saturates at a higher erased threshold voltage [1]. This erase saturation arises from a balance between the current through the bottom oxide and competing electron injection from the gate. In contrast, FN erase in a nanocrystal memory leads to a saturation threshold voltage that is independent of the gate bias. Figure 1-8 compares the band diagrams for SONOS and the nanocrystal memory under FN erase [2].

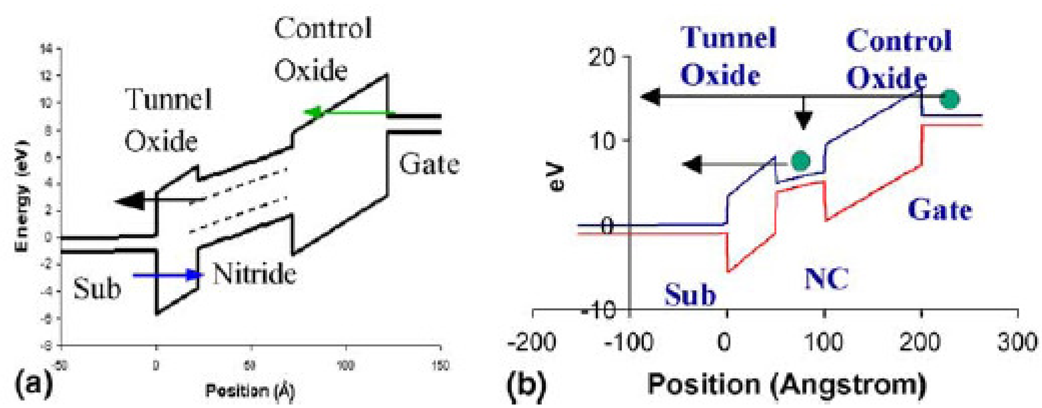


Figure 1-8 Band diagram of SONOS (a) and nanocrystal memory (b) under negative gate bias for FN erase.

In SONOS, the erase current through the bottom oxide is less responsive to the field, while attenuates more rapidly with increasing tunnel oxide thickness than the competing back injected current through the top oxide. Therefore, it is not practical to erase a SONOS bit cell with a tunnel oxide thickness larger than 5nm with tunneling. For nanocrystal memory, the erase current through the bottom oxide and the competing back injection have identical dependence on the field and experience similar barriers. As long as nanocrystals are charged with electrons the field in the bottom oxide is higher than the field in the top oxide, which facilitates the electrons to

be removed from the nanocrystals to the substrate. After removal, the field across the top oxide increases while the one across the bottom oxide decreases until a steady state is reached when both fields and hence both FN currents are equal. This steady state implies that there is no effective transfer of charge to and from the nanocrystals. Figure 1-9 compares the erase simulations for SONOS [3] and nanocrystal memory using a WKB tunneling based model [4] with gate injection and Coulomb blockade effects considered. It is found that the deeper electron traps in nanocrystals makes data retention substantially less temperature sensitive compared to SONOS where charge transport within the nitride layer is Frenkel-Poole emission that is temperature-dependent.

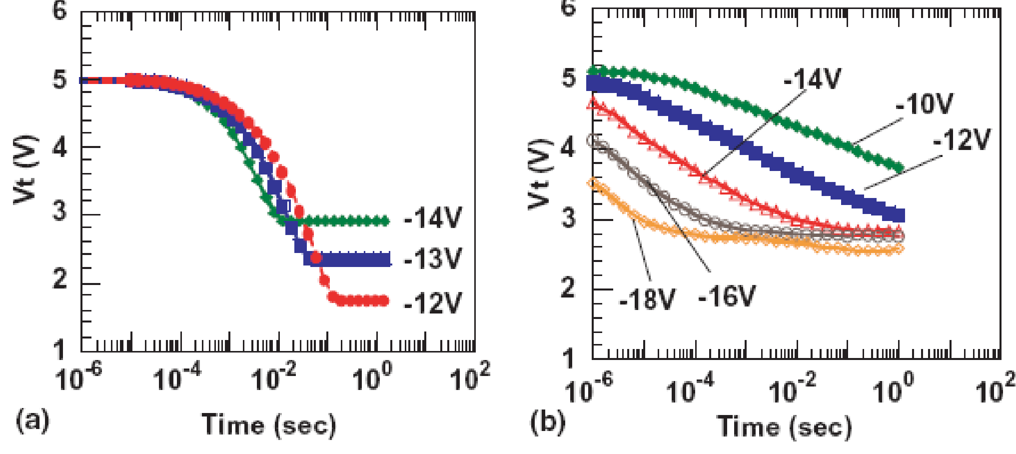


Figure 1-9 Simulation results showing gate bias dependence of FN erase for SONOS with 25A/120A/50A bottom oxide/nitride/top oxide thickness and nanocrystal memory with 50A tunnel oxide and 100A control oxide. After references [3] and [4].

Nanocrystal memory also shows advantage of the feasibility to control the ordering of trap sites than SONOS, where the charge traps originates from the silicon dangling bonds, which makes it difficult to have well-ordered traps. However, it seems to be possible to have regularly ordered quantum dots by self-assembled

technique. For example, the colloidal method can be used to produce mono-dispersed nanocrystals, including semiconductors, such as CdSe [5], CdTe [6], InP [7] and PbS [8], and metals, such as Ag [9], Pt [10], Au [11], Pd [12], Co [13], Fe [14]. It could enable the further scaling-down of cell size by depressing the dot number fluctuation, especially for next generation cells, such as 65 nm and 45 nm technology nodes.

Due to the strong Coulomb blockade effect in nanocrystals with small size [15], nanocrystal memory have potential to achieve multi-level cell application. The electron charge will raise the nanocrystal's potential and reduce the electric field across the tunnel oxide, leading to the reduction of programming current. For a nanocrystal of 3 nm diameter, 2.5 nm thick tunnel oxide and 5 nm control oxide, the electrostatic charge energy will be ~ 95 mV if there exists one electron in the nanocrystal. This energy will increase to 380 mV after the second electron is injected to the dot [16]. The charging energy separates more clearly different memory charge statues and favors the application for multi-level cell for the nanocrystal memory cells. Accordingly, the data density in the memory chip can be double or triple of the one for a binary-level cell. Once the retention issue with a thinner tunnel oxide is solved by splitting the floating gate into isolated nodes, the thickness of tunnel oxide can shrink further. As has been well known that the tunneling current almost exponentially depends on the reciprocal of tunnel oxide thickness, thinner tunnel oxide enables much faster programming and erasing speeds. Also due to the thinner tunnel oxide the defect generation during programming/erasing stress will be significantly depressed and the device endurance performance can be greatly improved [17], which means much higher reliability or in other words, much longer device life time.

1.4.2 Semiconductor nanocrystals

Memory-cell with nanocrystals as the charging storage media have received much attendtion as the promising candidates to replace conventional dynamic random array memory for future high speed and low power consumer memory devices [18-20]. Most studies were focusd on Si and Ge nanocrystal MOS memories [21-29] due to their material compatibility with Si VLSI technology. Various methods can be implemented to synthesize Si nanocrystals, such as chemical vapor deposition (CVD), ion-implantation, sputtering [18,30-33]. Direct CVD is preferred over ion implantation and recrystallization anneal due to the difficulty in obtaining the required amount of Si in the stack. Further nucleation and growth by CVD provides appropriate simpler processing controls to manipulate the size and density of nanocrystals. Tremendous efforts have focused on obtaining nanocrystals with density around $10^{12}cm^{-2}$ and size around 5nm. Si nanocrystals with number density between 10^{11} and $10^{12}cm^{-2}$ have been demonstrated on various dielectrics such as SiO_2, Si_3N_4, Al_3O_4 using CVD technique [34-36]. Si island growth during CVD on amorphous substrate is believed to proceed by atomistic nucleation, with a critical size of between 1 and 4 atoms [37]. Figure 1-10 [38] shows a typical nucleation and growth curve of Si nanocrystal formation during CVD along with SEM images of the surface during various phases of the nucleation and growth curve. During the initial incubation phase, there are not enough adatoms on the surface for nucleation to occur. With increasing of the growth time, this adatom concertation increases until reaching a point where adatoms start to diffusely encounter each other to form small clusters. In this region, the nanocrystal density increases rapidly with time. Once a certain saturation density is obtained, fresh nucleation stops as all incoming adatoms are captured by the

existing nanocrystals. The nanocrystal density insignificantly changes while the nanocrystal size increases. Eventually the growing nanocrystals coalesce with adjacent ones and the nanocrystal density starts to decrease.

High-density Si nanocrystal memory has been reported and long retention time was observed. However, it is believed that the role of traps and defects inside or at the surface of nanocrystals can explain the experimental observation of the long time retention [39], which makes their operation similar to trap-assisted storage [40]. The control of trap levels and density is thus critical for consistency in long retention time while is difficult because of the high sensitivity of trap formation and annihilation during the annealing process.

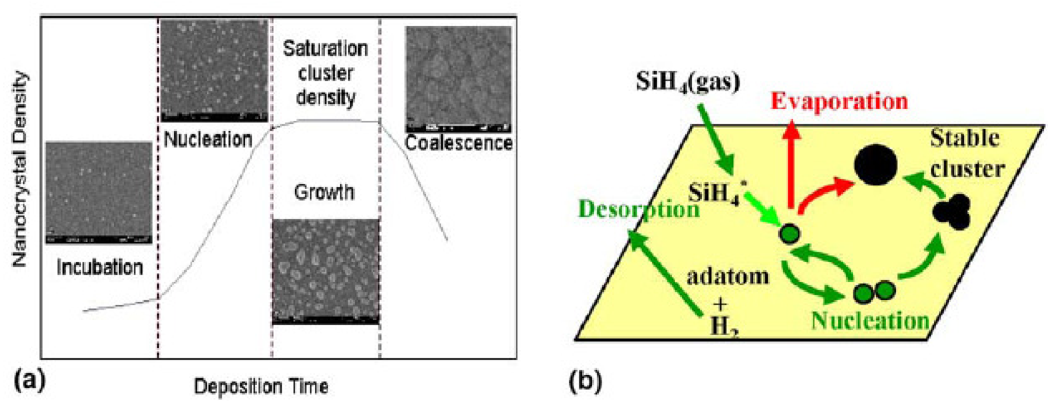


Figure 1-10 (a) Typical Si CVD nucleation curve along with SEM images showing the evolution of the nanocrystals formation on SiO_2, (b) atomistic nucleation of Si nanocrystals on a dielectric surface showing surface processes including SiH_4 adsorption, adatom re-evaporation and diffusion as well as H_2 desorption.

1.4.3 Metal nanocrystals

Memory effects of the various metals, such as Ag, Au, Pt, W, Co, Ni and et al. were investigated [41-56]. Generally metal nanocrystal memories possesses several advantages compared with semiconductor nanocrystal memories, such as stronger

coupling with the conduction channel, a wide range of available work functions, higher density of states around the Fermi level and smaller energy perturbation due to carrier confinement [41]. For metal nanocrystal memories, the work function engineering makes it possible to improve the storage capacity as well as the retention time. The larger work function in selected metal nanocrystals creates a deeper quantum well for long electron storage without affecting the efficiency of the electron injection. Figure 1-11 shows the energy band diagrams comparison between Si nanocrystal and metal nanocrystal memories. Selecting the right metal, whose workfunction is larger than that of Si nanocrystal, is possible to create a deeper quantum well for long time electron storage. Table 1-1 lists the work functions of various metals [57].

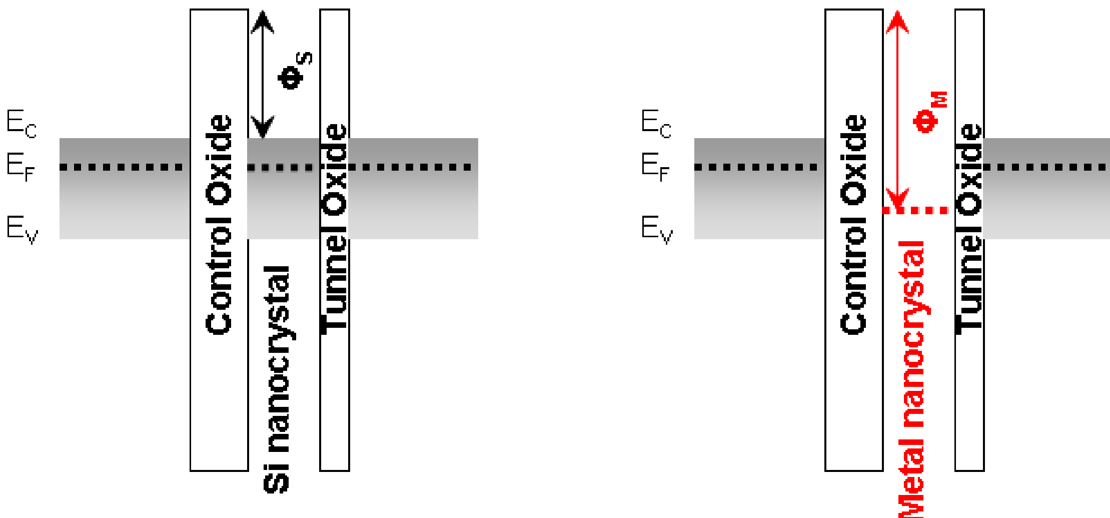
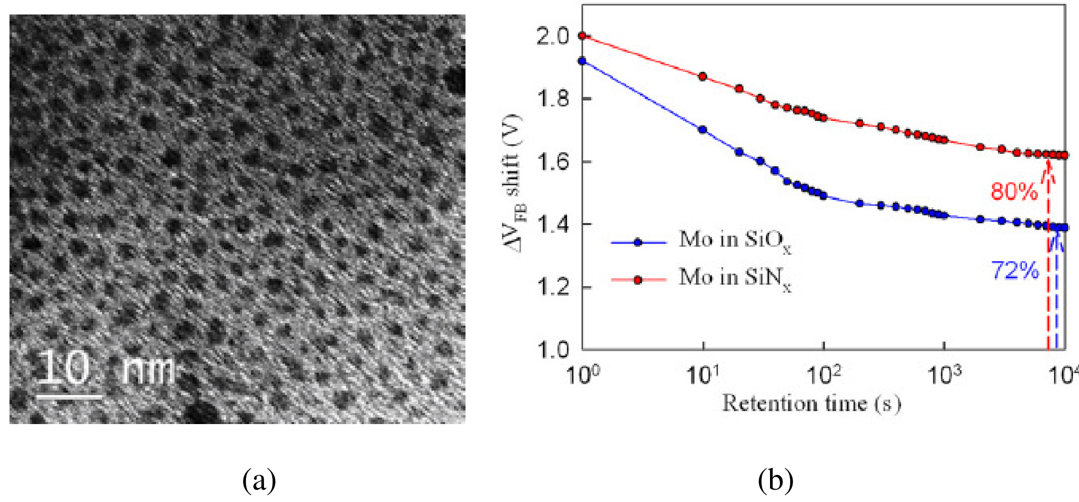


Figure 1-11 Energy band diagrams of Si nanocrystal memory and metal with higher work function than Si, nanocrystal memory. Metal has higher work function.

Element	Work function, Φ (eV)
Au	5.10 ± 0.1
Ag	4.33 ± 0.15
Pt	5.32 ± 0.1
W	4.55 ± 0.1
Ni	4.96 ± 0.1
$NiSi_2$	4.71 ± 0.1
$CoSi_2$	4.70 ± 0.1
Al	4.24 ± 0.1
TiN	2.92 ± 0.1

Table 1-1 Work function of various metal materials.

Metal nanocrystals can be formed by various methods including colloidal suspension, aerosol deposition, ion implantation and direct deposit self assembly. Among these methods, direct deposition, which involves the spontaneous formation of nanocrystals to achieve a local minimum energy, is believed as the most suitable one because of its simplicity and compatibility with current Si technology. Figure 1-12 (a) shows the transmission electron microscope (TEM) image of the Mo nanocrystals with very high dot density ($6\times10^{12}cm^{-2}$) synthesized by Mo sputtering plus post thermal annealing [58]. It can be seen from retention characteristics in the Figure 1-12 (b), that 80% charges are remaining in the nanocrystals after 10^4 seconds and 10^6 program/erase cycles. The better retention observed in Mo in SiN_x than SiO_x is attributed to the larger electrical field in the tunnel oxide of Mo embedded in the oxide than in the nitride, resulting in significant oxide degradation of tunnel oxide, which in turn compromises the retention performance.



(a) (b)

Figure 1-12 (a) TEM image of the Mo nanocrystals embedded in the SiN_x matrix and (b) retention performance achieved in this Mo/SiN_x and Mo/SiO_x nanocrystal memory.

The issue with metal nanocrystals on gate oxide is believed to be the reaction/diffusion between metal and gate oxide underneath. Although the metal nanocrystals can be synthesized at room temperature, the following high temperature treatment, such as dopant annealing for source/darin in MOSFET process, will significantly induce the reaction/diffusion between metals and oxide. This problem will become more and more critical for future generation memory as tunnel oxide scales down below 10nm. In this sense, metal only nanocrystals may not be suitable for scaled memory devices. New concepts or device structures are needed to address this problem.

1.5 Other nonvolatile memory technologies

In addition to charge-trap flash memories, some new nonvolatile memory technologies are being investigated, aiming to find the ideal memory that combines fast read, fast write, non-volatility, low-power, unlimited endurance and obviously at

a cost comparable with Flash or DRAM. Two main categories of emerging NVM technologies have been investigated so far, one based on inorganic materials, such as FeRAM, MRAM or PCM, and another based on organic materials, such as ferroelectric or conductance switching polymers.

1.5.1 FeRAM

Ferroelectric RAM, developed in late 1980s, is a random access memory similar to DRAM in terms of construction except that a ferroelectric layer is used to achieve nonvolatility instead of a dielectric layer. Data in a DRAM is stored as the presence or lack of an electrical charge in the capacitor, with the lack of charge generally representing "0". Writing is accomplished by activating the associated control transistor, draining the cell to write a "0", or sending current into it from a supply line if the new value should be "1". While writing in FeRAM is accomplished by applying a field across the ferroelectric layer by charging the plates on either side of it, forcing the atoms inside into the "up" or "down" orientation (depending on the polarity of the charge), thereby storing a "1" or "0". FeRAM offers low power consumption, fast write performance and extremely good endurance (up to 10^{16} cycles for 3.3V devices). Actually, the most used perovskite material for ferroelectric memories is lead zirconate titanate (PZT), while the layered ferroelectric choice for FeRAM memories is a Strontium–Bismuth–Tantalite alloy (SBT).

Although FeRAM has the similar architecture with DRAM (1Transistor/1Capacitor), there still exists the scaling limit because with device size further shrinking, the amount of charge stored in the capacitor might be too small to be detected. An additional limitation on size is that the materials tend to stop being

ferroelectric when they are too small [59-60]. Another concern of FeRAM is that the PZT ferroelectric layer and the noble metals used for electrodes raise CMOS process compatibility and contamination issue although the process is much simpler than current Flash memory. Figure 1-13 shows the typical FeRAM device with stacked capacitor approach [61].

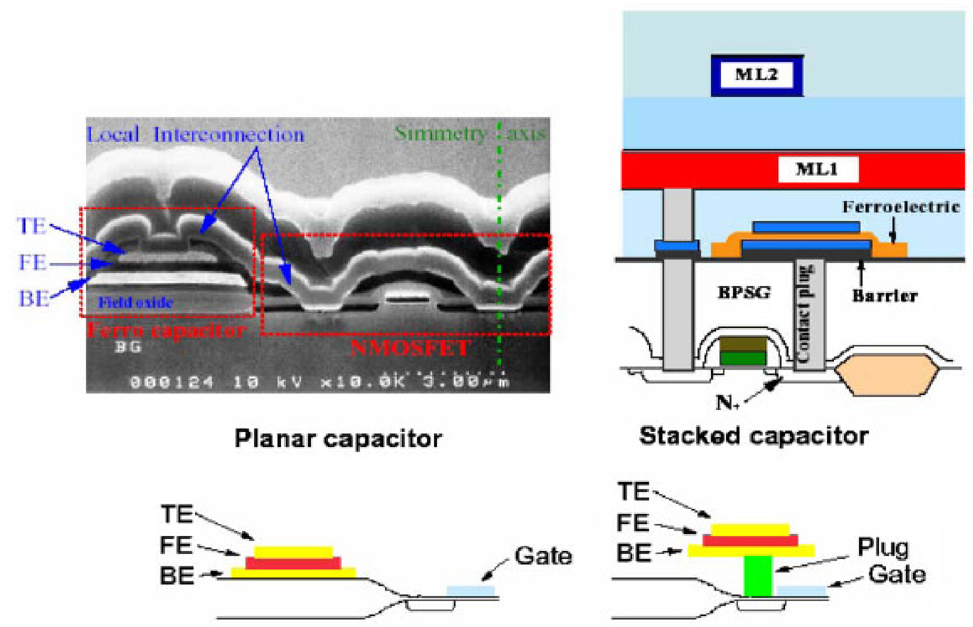


Figure 1-13 Schematic Structure of an FeRAM with the stacked capacitor approach.

1.5.2 MRAM

Magnetoresistive RAM (MRAM) is a nonvolatile memory technology that has been developed since 1990s. Unlike conventional RAM chip technologies, in MRAM data is not stored as electric charge or current flows, but by magnetic storage elements. The elements are formed from two ferromagnetic plates, each of which can hold a magnetic field, separated by a thin insulating layer. One of the two plates is a permanent magnet set to a particular polarity, the other's field will change to match

that of an external field. A memory device is built from a grid of such "cells". Reading is accomplished by measuring the electrical resistance of the cell. Typically if the two plates have the same polarity this is considered to mean "1", while if the two plates are of opposite polarity the resistance will be higher and this means "0". Data is written to the cells using a variety of means. In the simplest, each cell lies between a pair of write lines arranged at right angles to each other, above and below the cell. When current is passed through them, an induced magnetic field is created at the junction, which the writable plate picks up.

The non-destructive read with a very fast access cycle is the premise for high performance, equal-long read and write cycles and for low power operation. Moreover, the structure is radiation hard with an unlimited read/write endurance, which makes MRAMs suitable for write intensive storage applications. The major MRAM disadvantage appears to be the high write current. While this technology has enough read current to guarantee a fast access time, it requires a very large write current (mA range), which increase power consumption. Although FeRAM and MRAM nonvolatile cells are very promising for high performance and low power systems, to date their development has faced many challenges that impact the manufacturability of high-density devices. Additionally, as the device is scaled down in size, there comes a time when the induced field overlaps adjacent cells over a small area, leading to potential false writes. Most of the architecture of MRAM technology takes form of MTJ cell based 1Transistor/1Resistor (1T/1R) structure, as shown in Figure 1-14 [62].

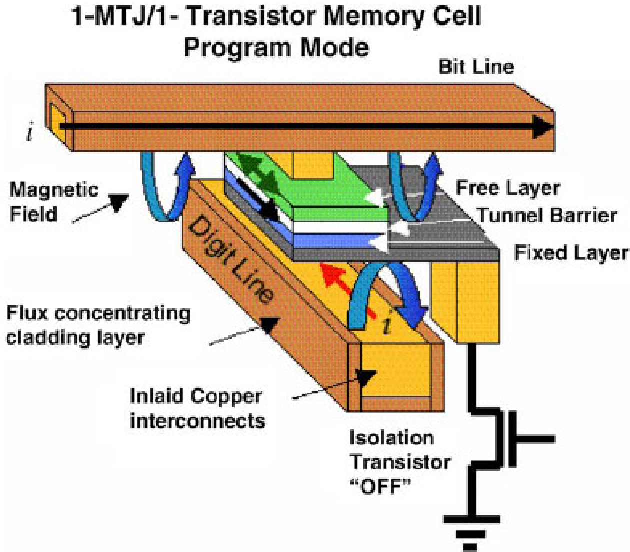
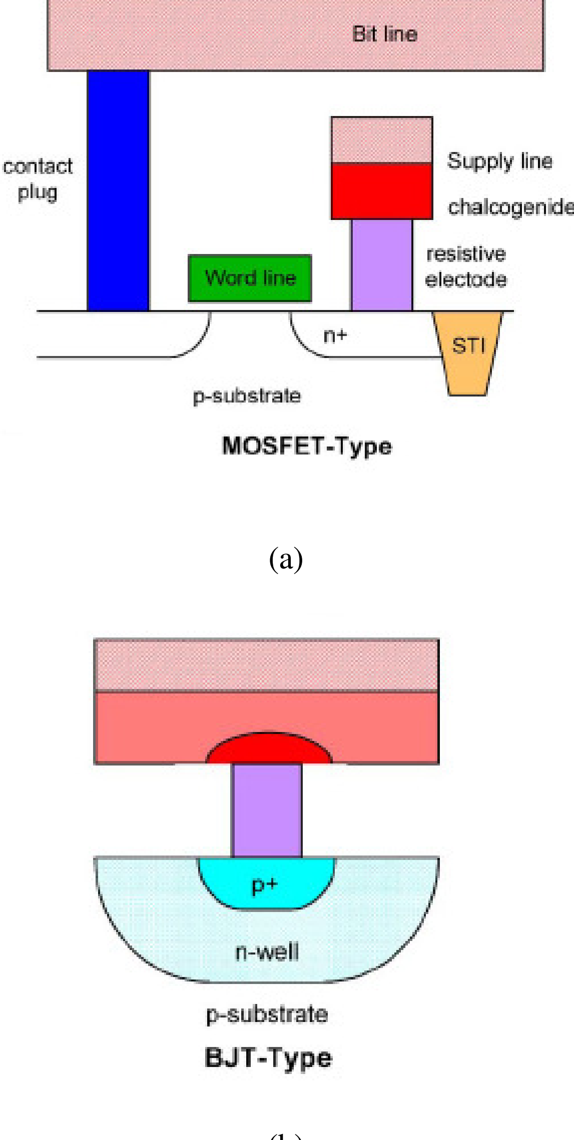


Figure 1-14 Schematic of MRAM cell showing the programming operation mode.

1.5.3 Phase change memory

Phase change memory (PCM) is one of the most promising candidates for next-generation NVM [63-66], having the potential to improve the performance compared to Flash— random access time and read throughput (versus NOR), write throughput (versus NAND), direct write, bit granularity, endurance—as well as to be scalable beyond Flash technology. PCM uses the unique behavior of chalcogenide glass, which switches between crystalline and amorphous states with the application of heat. The phase change property of chalcogenide glasses was first recognized by Stanford R. Ovshinsky in the 1960s and published by Gordon Moore in 1970. Due to the material quality and power consumption issues, this technology has not been commercialized. Recently, interest has returned as flash and DRAM encounter the scaling limit as chip lithography shrinks.

The electrical resistance difference between crystalline and amorphous states of chalgenide glass is the basis by which the data is stored. The amorphous of high resistance represents “0” while crystalline of low resistance state represents “1” state. Figure 1-15 (a) and (b) show the typical PCM architecture in forms of MOSFET and BJT, respectively.



(a)

(b)

Figure 1-15 Schematic cross section of PCM memory cells in (a) MOSFET and (b) BJT architectures.

PCM offers quick writing because of the very quick switching of the memory element and also single bit may be changed to “1” or “0” without pre-erasing of the cells. The endurance of PCM is much better than Flash memory and 10^8 write/erase cycles have been demonstrated. Also PCM possesses superior data retention than Flash due to the stable memory element in PCM. At temperature of 85ºC, it is projected to retain data for 300 years [67]. The challenges of PCM include: high programming current density, dielectric degradation at high temperature, less consistent data retention, amorphous state aging, where the resistance of amorphous state slowly increases with time, high cost and the un-compatibility with current CMOS technology.

1.6 Motivation of this research

The aim of this research is to enhance memory performance of nanocrystal memory. In order to achieve the goal of faster writing/erasing speed and longer retention time, it is necessary to have an asymmetry of charge transport. Three different methods can be used for this purpose: First, by replacing the rectangular barrier with a parabolic or triangular barrier, the barrier height can be modulated by the electrical field in the tunneling oxide [68]. Therefore, a higher barrier is seen during retention while a lower barrier is present during write/erase operations. The second approach is to use double-stacked storage nodes, preferably self-aligned with smaller dots at the lower stack [69]. Fast writing/erasing speed can be achieved if sufficient thin oxide is used below and between the two stacks. And the retention time can be prolonged due to the Coulomb blockade effect at the lower stack, which prevents electrons in the top stack from tunneling back to the substrate. The third way

is to engineer the depth of the potential well at the storage nodes in order to create an asymmetrical barrier between the substrate and the storage nodes, i.e., a small barrier for writing and a large barrier for retention [70-72]. The motivation in this thesis work is to preserve data retention characteristics and to allow voltage scaling simultaneously by engineering the nanocrystal floating gate.

1.6.1 Ge/Si heteronanocrystal memory

As mentioned in the above section, the long retention time observed in Si nanocrystal memory is believed to relate to defect-related trap levels. To address the issue, a new type of nano-structure, Ge/Si heteronanocrystals, was proposed. A quantum well of about 0.47eV deep is artificially created for holes to store in Ge side as a result of type-II band alignment for Ge on Si system. In this case, most of holes are stored in this quantum well after programming (a p-channel memory) rather than in trap levels with broad distribution in Si nanocrystal only case. This enhances endurance and characteristics markedly. In short, the device performance can be controlled by design, better than un-controllable from broad distribution of defect levels in Si nanocrystal memory. The detailed experimental results of Ge/Si heteronanocrystal memory are discussed in Chapter 3.

1.6.2 Sillicide-based nanocrystal memories

Silicide, for example $TiSi_2$, $CoSi_2$, and NiSi, which poses the advantage of lower resistance and a self-aligned feature during silicon process, is widely used for Ohmic contacts in modern CMOS technology. The incorporation of metal silicides in MOS devices has a principal purpose of reducing the parasitic components in the three

terminals of a MOSFET: gate, source and drain, to increase switching speed. A suitable silicide for this purpose should meet the basic requirements for contact metallization: low specific resistivity, low contact resistivity to both p- and n-type silicon, high thermal stability, good processibility, and therefore excellent process compatibility with standard silicon technology. As the silicon integrated circuits continues to scale down, the contact materials have evolved from Al/Ti, to $MoSi_2$, WSi_2, to current $TiSi_2$, onto $CoSi_2$ and NiSi in the deep sub-100 nm CMOS technology.

In this work, we explore silicide nanostructures and exploit another of silicide's salient properties, i.e., work function difference with silicon. Table 1-2 [73] lists the workfunction of various silicide. By selecting the correct silicide materials, it is also possible to engineering the nano-floating gate to create a deeper quantum well for long time electron storage. The deeper quantum well formed in silicide nanocrystal than Si only nanocrystals offers the long retention time for electron storage. Table 1-3 [74] shows the bond dissociation energy of metal-metal bonds and metal-silicon bonds. It is found that generally the dissociation energy of the silicide is higher than metals. Therefore, silicide is believed as a more thermally stable material than metal counterparts, which means the device reliability, retention and endurance, of the memory devices will be improved by replacing metal with silicide nanocrystals.

Silicide	Workfunction (eV)
$TiSi_2$	4.53
$CoSi_2$	4.77
NiSi	4.68
$NiSi_2$	4.71
$MoSi_2$	4.82
WSi_2	4.88
PtSi	4.86

Table 1-2 Summary of various silicide work function for nanocrystal floating gate engineering. By selecting the suitable silicide, the retention time can be effectively improved compared to Si nanocrystal memory.

Chemical Bonds	Bond Dissociation Energy (KJ/mol)		Chemical Bonds	Bond Dissociation Energy (KJ/mol)
Ti-Ti	**117.6**		**Ti-Si**	**249±16**
Ni-Ni	**200.74**		**Ni-Si**	**318±17**
Co-Co	**90.6**		**Co-Si**	**274.4±17**
Pt-Pt	**361±15**		**Pt-Si**	**501±18**
Al-Al	**153**		**Al-Si**	**246.9±12.6**
Cu-Cu	**195.7**		**Cu-Si**	**221.3±6.3**
Pd-Pd	**109±21**		**Pd-Si**	**261±12**
Zn-Zn	**19.9±2.5**		**Zn-Si**	**274.1±9.6**
Fe-Fe	**105±21**		**Fe-Si**	**297±25**
Mn-Mn	**31-54**		**Mn-Si**	**79±26**

Table 1-3 Summary of bond dissociation energy of metal-metal bonds and metal-silicon bonds. Silicide materials show the larger dissociation energy, indicating the better thermal stability of silicides than metals.

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Chapter 2: Fabrication and characterization methodology

2.1 Nanocrystal growth

2.1.1 Chemical vapor deposition

Si nanocrystals have been synthesized through various methods, such as chemical vapor deposition (CVD), ion implantation, rapid thermal oxidation, solution-based synthesis. Among them CVD is the most popular methods because it is a simple process and easy to be integrated into current CMOS process for mass production. In this thesis, the Si nanocrystals, Ge/Si hetero-nanocrystals were grown through CVD process.

Generally CVD is a process used to produce high-purity, high performance thin films in the semiconductor industry. In a CVD process, the wafer is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposits. The volatile by-products are removed by gas flow through the reaction chamber. Typical materials that can be deposited by CVD process include semiconductors, such as silicon, germanium, silicon carbide, zinc oxide, gallium arsenide, and dielectrics, such as silicon oxide, silicon nitride, etc. Based on the operating pressure, CVD can be categorized into atmospheric pressure CVD (APCVD), low-pressure CVD (LPCVD), and ultrahigh vacuum CVD (UHVCVD). In this thesis work, the Si nanocrystals, Ge/Si hetero-nanocrystals, control oxide, poly-silicon gate and silicon nitride layer are all deposited using LPCVD system. Plasma-enhanced CVD is a process utilizing plasma to enhance chemical reaction rates of the precursors. With plasma assistant, the processing allows deposition at lower temperature than LPCVD. In this research, the metal contacts

isolation for metal oxide semiconductor field effect transistor (MOSFET) was PECVD-deposited SiO_2.

The reactions occurred during CVD deposition with SiH_4 as the precursors for Si nanocrystals and poly-silicon gate is: $SiH_4 \rightarrow Si + 2H_2$. Either pure SiH_4 or SiH_4 with H_2 as the carrier gas was used as the precursors. Temperature between 585ºC and 625ºC and pressure between 25mTorr and 400mTorr was used for the Si growth. Hydrogen gas was introduced to reduce the growth rate for uniform nano-scale materials growth. For silicon dioxide in this work, the reaction is simply expressed as: $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$ for LPCVD and $SiCl_2H_2 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2HCl$ for PECVD. The silicon nitride, used for hard mask during local oxidation of silicon isolation was grown through: $3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$.

2.1.2 Physical vapor deposition

In addition to CVD, Physical vapor deposition (PVD) is also a well-established method for nanocrystal synthesis, such as metals and silicides. Basically, PVD is generally used to deposit thin films by the condensation of a vaporized form of the materials into various surfaces. The coating method involves purely physical processes such as high temperature vacuum evaporation or plasma sputter bombardment rather than involving a chemical at the surface to be coated as in chemical vapor deposition. Electron beam (e-beam) physical vapor deposition is a process where the materials to be deposited is heated to a high vapor pressure by electron bombardment in vacuum. Sputtering is a physical vapor deposition process

wherein atoms or molecules are ejected from a target material by high-energy particle bombardment so that the ejected atoms or molecules can condense on a substrate as a thin film. Sputtering is one of the most widely used techniques for depositing various metallic films on wafers, including aluminum, aluminum alloys, platinum, gold, and tungsten.

In this research, we used PVD to deposit metal film on top of Si nanocrystals for silicide formation, to be discussed in Chapter 4. In Chapter 5 and 6, the $NiSi_2$ and PtSi nanocrystals synthesis also involves PVD deposition of metal catalysts first before silicide formation occurs. The advantage of PVD over CVD is that the film thickness is easier to be precisely controlled especially for high density nanocrystals.

2.2 Nanocrystal characterization

2.2.1 Scanning electron microscope

Nanocrystals morphology, including nanocrystal density and average size were measured by scanning electron microscope (SEM). All the SEM images shown in this thesis were measured by electrons.

SEM is a type of microscope that images the sample surface by scanning it with a high-energy beam of electrons in a raster scan pattern. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition and other properties such as electrical conductivity. The types of signals produced by an SEM include secondary electrons, back-scattered electrons (BSE), characteristics X-rays, light, specimen current and transmitted electrons. Secondary electron detectors are used in this research for nanocrystal morphology measurement. The signal results from interactions of the

electron beam with atoms at or near the surface of the sample. In standard detection mode, secondary electron imaging, the SEM can produce very high-resolution images of a sample surface, revealing details about less than 1 to 5nm in size. Due to the very narrow electron beam, SEM micrographs have a large depth of field yielding a characteristic three-dimensional appearance useful for understanding the surface structure of a sample. BSE are beam electrons that are reflected from the sample by elastic scattering. BSE are often used in analytical SEM along with the spectra made from the characteristic X-rays. Because the intensity of the BSE signal is strongly related to the atomic number of the specimen, BSE images can provide information about the distribution of different elements in the sample. For the same reason, BSE imaging can image colloid gold immuno-labels of 5 or 10nm diameter which would otherwise be difficult or impossible to detect in secondary electron images in biological specimens. Characteristic X-rays are emitted when the electron beam removes an inner shell electron from the sample, causing a higher energy electron to fill the shell and release energy. These characteristic X-rays are used to identify the composition and measure the abundance of elements in the sample.

Figure 2-1 shows the schematic diagram of an SEM tool. An electron beam is thermionically emitted from an electron gun fitted with a tungsten filament cathode. Tungsten is normally used in thermionic electron guns because it has the highest melting point and lowest vapor pressure of all metals, thereby allowing it to be heated for electron emission, and because it is low cost. The electron beam, which typically has an energy ranging from a few hundred eV to 40 keV, is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter. The beam passes through pairs of scanning coils or pairs of deflector plates in the electron column, typically in

the final lens, which deflect the beam in the x and y axes so that it scans in a raster fashion over a rectangular area of the sample surface. When the primary electron beam interacts with the sample, the electrons lose energy by repeated random scattering and absorption within a teardrop-shaped volume of the specimen known as the interaction volume, which extends from less than 100 nm to around 5 µm into the surface. The size of the interaction volume depends on the electron's landing energy, the atomic number of the specimen and the specimen's density. The energy exchange between the electron beam and the sample results in the reflection of high-energy electrons by elastic scattering, emission of secondary electrons by inelastic scattering and the emission of electromagnetic radiation, each of which can be detected by specialized detectors. The beam current absorbed by the specimen can also be detected and used to create images of the distribution of specimen current. Electronic amplifiers of various types are used to amplify the signals which are displayed as variations in brightness on a cathode ray tube. The raster scanning of the CRT display is synchronised with that of the beam on the specimen in the microscope, and the resulting image is therefore a distribution map of the intensity of the signal being emitted from the scanned area of the specimen.

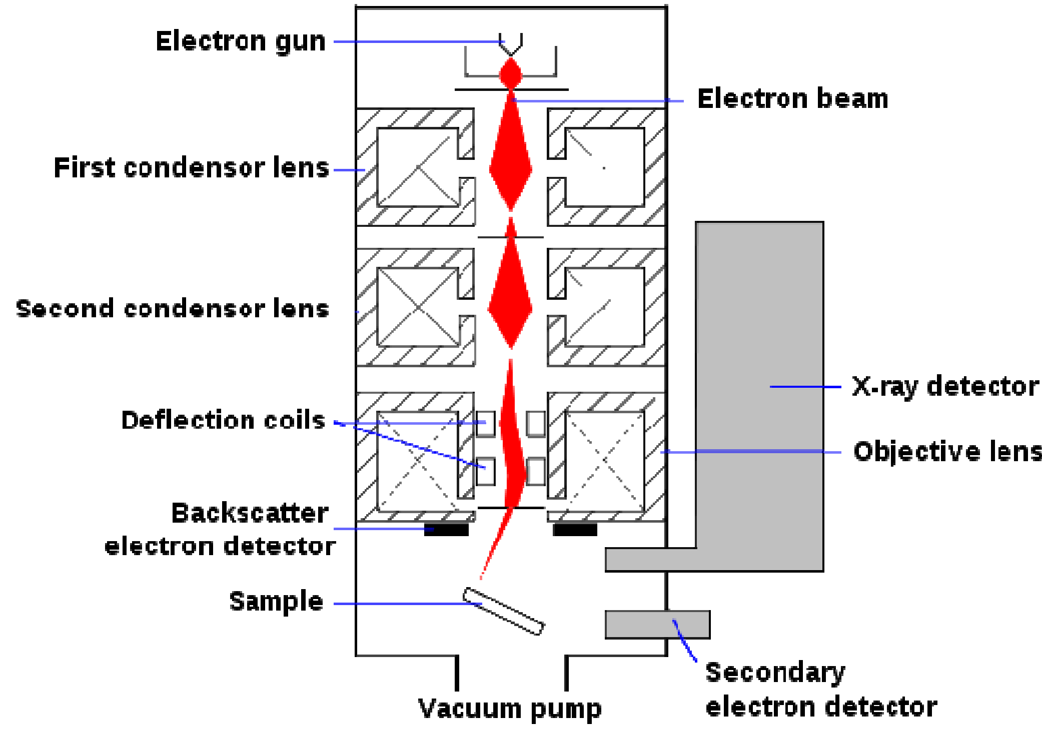


Figure 2-1 Schematic diagram of an SEM tool.

2.2.2 Atomic force microscope

Atomic force microscope (AFM) was used to check the nanocrystal average height. By comparing the average height of Si nanocrystals and Ge/Si heteronanocrystals, the self-alignment between Ge and Si was confirmed by observing the larger height in Ge/Si heteronanocrystals.

AFM is an instrument that can be used to analyze and characterize the sample at microscope level. It operates by allowing an extremely fine sharp tip to either come in contact or in a very close distance to the sample that is being imaged. The AFM consists of a cantilever with a sharp tip (probe) at its end that is used to scan the specimen surface. The cantilever is typically silicon or silicon nitride with a tip radius of curvature on the order of nanometers. When the tip is brought into proximity of a

sample surface, forces between the tip and the sample lead to a deflection of the cantilever according to Hooke's law. Depending on the situation, forces that are measured in AFM include mechanical contact force, van der Waals forces, capillary forces, chemical bonding, electrostatic forces, magnetic forces, Casimir forces, solvation forces, etc. Typically, the deflection is measured using a laser spot reflected from the top surface of the cantilever into an array of photodiodes. Other methods that are used include optical interferometry, capacitive sensing or piezoresistive AFM cantilevers. If the tip was scanned at a constant height, a risk would exist that the tip collides with the surface, causing damage. Hence, in most cases a feedback mechanism is employed to adjust the tip-to-sample distance to maintain a constant force between the tip and the sample. Traditionally, the sample is mounted on a piezoelectric tube, that can move the sample in the z direction for maintaining a constant force, and the x and y directions for scanning the sample. Alternatively a 'tripod' configuration of three piezo crystals may be employed, with each responsible for scanning in the x,y and z directions. This eliminates some of the distortion effects seen with a tube scanner. In newer designs, the tip is mounted on a vertical piezo scanner while the sample is being scanned in X and Y using another piezo block. The resulting map of the area s = f(x,y) represents the topography of the sample.

Tapping mode AFM was used in this research to check the topography of nanocrystals. In tapping mode, the cantilever is driven to oscillate up and down at near its resonance frequency by a small piezoelectric element mounted in the AFM tip holder. The amplitude of this oscillation is greater than 10 nm, typically 100 to 200 nm. Due to the interaction of forces acting on the cantilever when the tip comes close to the surface, Van der Waals force or dipole-dipole interaction, electrostatic forces,

etc cause the amplitude of this oscillation to decrease as the tip gets closer to the sample. An electronic servo uses the piezoelectric actuator to control the height of the cantilever above the sample. The servo adjusts the height to maintain a set cantilever oscillation amplitude as the cantilever is scanned over the sample. A tapping AFM image is therefore produced by imaging the force of the oscillating contacts of the tip with the sample surface. Figure 2-2 shows the schematic of an AFM.

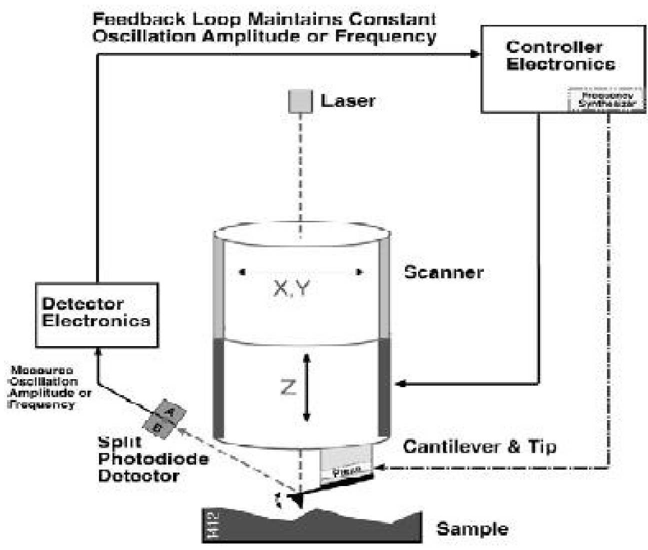


Figure 2-2 Schematic diagram of an AFM.

2.2.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) was used to check the nancorystals chemical nature. XPS is a quantitative technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 to 10 nm of the material being analyzed. XPS requires ultra high vacuum (UHV) conditions. A typical XPS spectrum is a plot of the number of electrons detected (sometimes per unit time) (Y-axis, ordinate) versus the

binding energy of the electrons detected (X-axis, abscissa). Each element produces a characteristic set of XPS peaks at characteristic binding energy values that directly identify each element that exist in or on the surface of the material being analyzed. These characteristic peaks correspond to the electron configuration of the electrons within the atoms, e.g., 1s, 2s, 2p, 3s, etc. The number of detected electrons in each of the characteristic peaks is directly related to the amount of element within the area (volume) irradiated. The photo-emitted electrons that have escaped into the vacuum of the instrument are those that originated from within the top 10 to 12 nm of the material. All of the deeper photo-emitted electrons, which were generated as the X-rays penetrated 1-5 micrometers of the material, are either recaptured or trapped in various excited states within the material. For most applications, it is, in effect, a non-destructive technique that measures the surface chemistry of any material. Figure 2-3 shows the schematic diagram of XPS system.

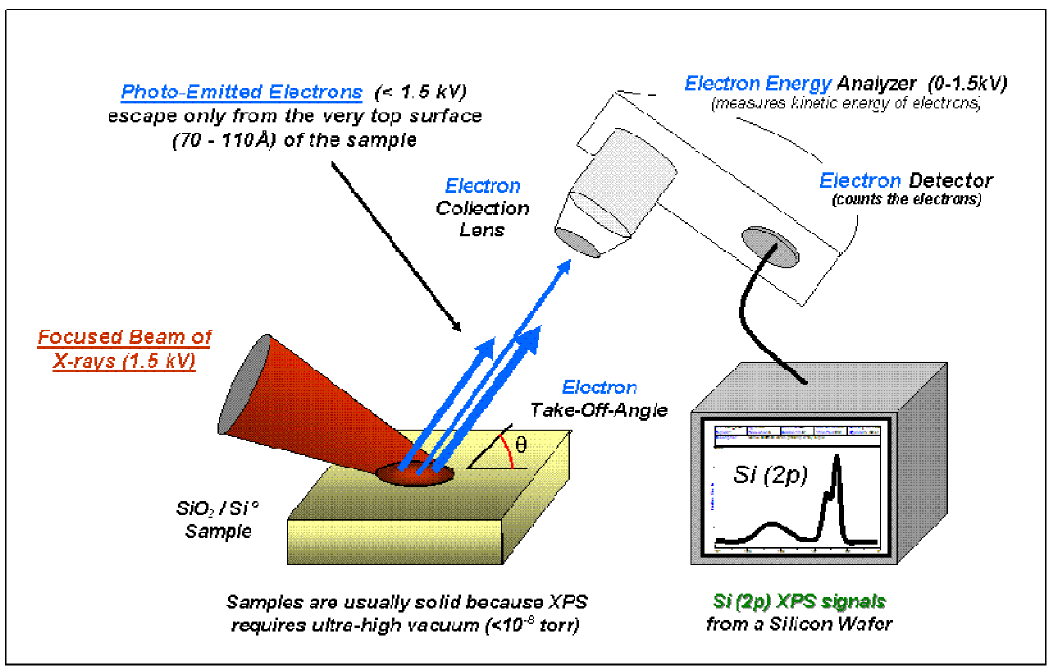


Figure 2-3 Schematic of XPS system.

2.2.4 Transmission electron microscope

Transmission electron microscopy (TEM) was used to check the cross-section of nanocrystals embedded between two layers of oxide, which is the critical region in our nanocrystal memory device. It shows the information on nanocrystal size and distance between adjacent nanocrystals.

TEM is a microscopy technique whereby a beam of electrons is transmitted through an ultra thin specimen, interacting with the specimen as it passes through. An image is formed from the interaction of the electrons transmitted through the specimen; the image is magnified and focused onto an imaging device, such as a fluorescent screen, on a layer of photographic film, or to be detected by a sensor such as a CCD camera. TEMs are capable of imaging at a significantly higher resolution than light microscopes, owing to the small de Broglie wavelength of electrons. This enables the instrument's user to examine fine detail—even as small as a single column of atoms, which is tens of thousands times smaller than the smallest resolvable object in a light microscope. TEM forms a major analysis method in a range of scientific fields, in both physical and biological sciences. TEMs find application in cancer research, virology, materials science as well as pollution and semiconductor research. At smaller magnifications TEM image contrast is due to absorption of electrons in the material, due to the thickness and composition of the material. At higher magnifications complex wave interactions modulate the intensity of the image, requiring expert analysis of observed images. Alternate modes of use allow for the TEM to observe modulations in chemical identity, crystal orientation, electronic structure and sample induced electron phase shift as well as the regular absorption based imaging. Figure 2-4 shows the schematic setup of a TEM.

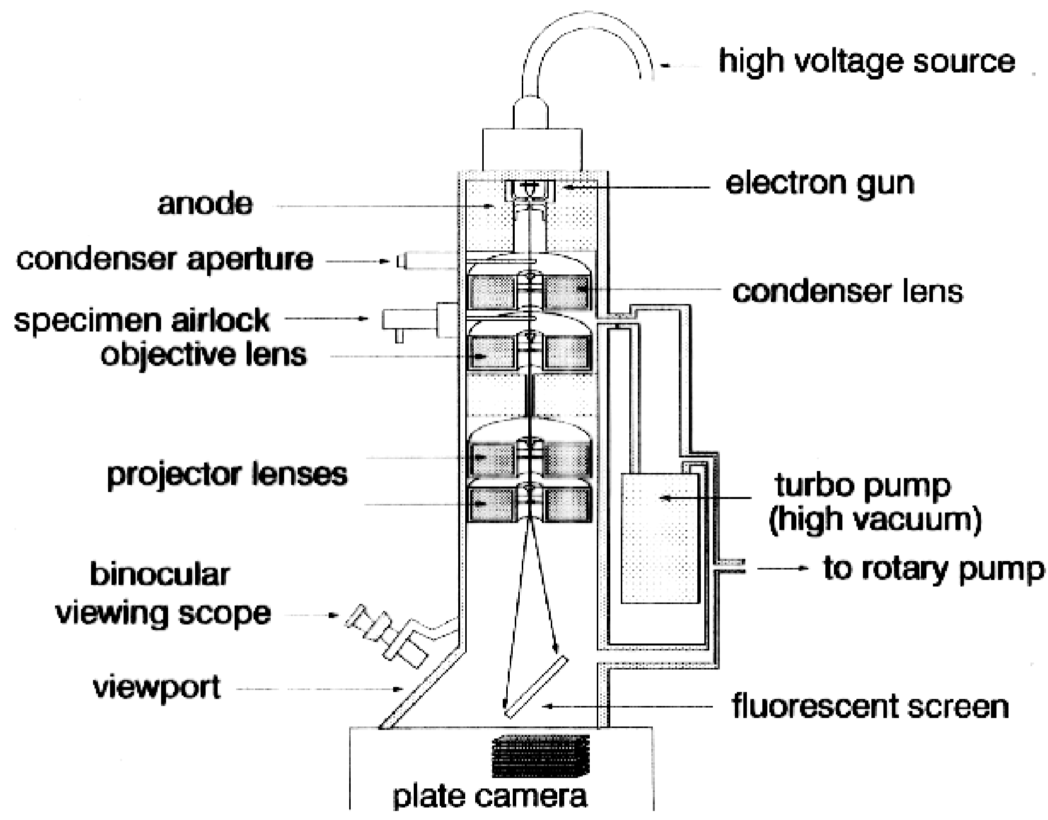


Figure 2-4 Schematic diagram of a TEM.

2.3 Nanocrystal memory fabrication

The device isolation was done with local oxidation of silicon (LOCOS). After the definition of active region by using LOCOS, the nitride hard mask is removed by dry etch. After removing the residual ultra-thin oxide in active region, tunnel oxide is grown. Then the wafer is transferred into LPCVD furnace and Si dots are deposited. Then the silicidation is carried out. The control oxide is deposited in a HTO furnace. These steps are very similar to that descried for MOS memory device.

Poly-Si is then deposited in LPCVD furnace with thickness of ~ 200 nm. Then the whole stack (Poly-Si/control oxide/nanocrystals/tunnel oxide/Si substrate) is patterned with dry etch. This self-aligned step forms the gate pattern. Then the wafer

is sent for source/drain implantation, which forms the heavily doping regions and functional gate. Then the wafer is capped with thick HOT film to passivate the device. The metal contact is realized by opening contacting holes and contact pads are also introduced in this step.

2.4 Nanocrystal memory characterization

2.4.1 Capacitance-voltage measurement

The Capacitance-voltage (C-V) measurement is a simple and effective way to examine the memory effect of metal oxide semiconductor (MOS) memory. This is done by a home-made Labview code with a GPIB card for communication between the computer and an Agilent 4192 Precise LCR meter. The input interface of the Labview code allows one to specify the measuring frequency, (voltage) sweep range, delay time between two voltage points, double-sweep or single-sweep, output file name, etc. By specifying the delay time (during this time the voltage is kept) and using a single voltage point, we can bias a MOS device with a voltage pulse for a certain time. In other words, we can program and erase a MOS nanocrystal memory device with Labview code as well. In order to avoid the deep depletion, during programming, the device was illuminated with light. After each programming or erasing pulse, the C-V curve of the device is measured and the flat-band voltage was recorded. The programming transient then can be obtained by comparing the flat-band voltage shift. Similar measurement was done for retention: flat-band voltage was measured from time to time and its decay indicates the charge loss as time elapses.

2.4.2 MOSFET memory measurement

For a three-terminal MOSFET memory device, the F-N programming/erasing was done with floating the source, drain, grounding the substrate while only biasing the control gate. The programming/erasing pulse was provided by an Agilent 8110A pulse generator. After each voltage pulse, the source-drain current was measured as a function of gate voltage. Defining V_T the gate voltage where I_D=100nA, the programming/erasing performance then was derived from the V_T shift after each pulse. During retention, I_D was frequently measured so that the time-dependent V_T can be tracked. The retention was done at room temperature. The device characterizations under hot carrier injection mode are similar to that in F-N, except that the programming was performed by grounding the source and applying biases on both gate and drain terminals, where the high field generated in the channel create carriers, for example, electrons for n-MOSFET memory, with sufficient energy to overcome the barrier between Si substrate and tunnel oxide and be trapped into nanocrystals.

Chapter 3: Ge/Si heteronanocrystal memory

3.1 Motivation

Flash memory, stand-alone or embedded, takes form of floating gate technology in which charges are stored in a piece of floating gate, polysilicon embedded between two dielectric layers, such as SiO_2 or oxide-nitride-oxide. Charging and discharging the floating gate shifts the threshold voltage of the memory device, which is an n-MOSFET or p-MOSFET with floating poly gate in SiO_2. The inherent wear-out mechanism for floating gate memory is called low-temperature data retention, which causes a small fraction of the bits in a Flash array to lose charge after repeated program/erase cycles. The field failure rate of low-temperature date retention increases with the decrease of tunnel oxide thickness. In order to guarantee chip reliability against certain field failure rate, the tunnel oxide can not be much thinner than 10nm. This remains an issue for next generation memory, which requires shrinking the device size and lowering the power consumption.

In order to simultaneously improve the retention time and shrink the tunnel oxide, which in turns benefits the operation (programming/erasing) speed and power consumption, flash memory using discrete traps as storage nodes were proposed. The device concept of Si nanocrystal memory was first introduced by Tiwari in 1996 [1]. Since then, much progress has been made in the area of nanocrystal deposition [2-8], stack engineering [9-12], process integration [13-17], cell operation and array architecture [18-21]. Basically, the idea behind using Si nanocrystal instead of conventional continuous poly-Si floating gate in MOSFET is to trap the charges into electrically-isolated nodes, so that even there are some defects in the tunnel oxide

forming leakage path, it is impossible for all the charges in nanocrystals to tunnel back to substrate. Only charges in those nanocrystals close enough to the defects in the oxide has a chance to be leaked away. The majority of charges in the nanocrystals remain in there. Therefore, a thinner tunnel oxide can be used in nanocrystal memory, and faster programming speed and lower operation voltage can be expected [22-25].

Memory with metal nanocrystals, silicide nanocrystals, hybrid-nanocrystals, multi-stack nanocrystals and engineered gate stack have been proposed and demonstrated with improved performance over Si nanocrystal only memory. The motivation to conduct such research is that the long retention shown in Si nanocrystal memory is believed to be attributed to charging in the defect levels rather than in the conduction or valence bands in Si nanocrystals [26-27]. These defect charging, on one hand is thermally un-stable, which means thermal processing, such as dopant activation could easily discharge the carriers stored on these levels. On the other hand, these defect levels are hard to control during process, in other words, good consistency in device performance is not easily achieved, especially for devices containing only several or even one nanocrystal storage node.

In this chapter, we report our research on using Ge/Si hetero-nanocrystals, in stead of Si only nanocrystals as the floating gate for memory application. The idea is to elongate the retention time by creating a deeper quantum well between nanocrystal and dielectric layer matrix for longer time charge, in this case, holes storage. Table 3-1 shows the schematic diagrams of Si nanocrystal and Ge/Si hetero-nanocrystal memories and their band diagrams under writing, erasing and retention modes. The devices take structure of MOS capacitor forms with nanocrystals embedded between a 5nm tunnel oxide and 25nm control oxide. The substrates used for device fabrication

is n-type Si because the Ge/Si type-II band alignments only benefit the hole storage, compared to Si nanocrystal memory. During writing, with negative bias applied on the gate, holes accumulated in the inversion region of the substrate tunnel into the nanocrystals through F-N tunneling and stored inside of Ge, where they have lower energy. During erasing, with positive bias on the gate, holes stored in the nanocrystals were pushed back to the substrate. On the other hand, considering the barrier height and lower mass of electrons, tunneling of electrons from the accumulation region of the surface to the nanocrystals to neutralize the holes stored in Ge dominate the whole erasing process. During retention, with no gate bias applied, the stored holes in Ge are expected to stay for longer time compared to the Si nanocrystal memory because there is a double barrier preventing holes from leaking back to the channel, one is Si nanocrystal underneath the Ge and the other one is the tunnel oxide. In other words, the holes have to be thermally activated to overcome the valance barrier between Ge and Si, which is about 0.47eV before tunneling occurs. Therefore, retention can be markedly improved without sacrificing writing/erasing efficiency.

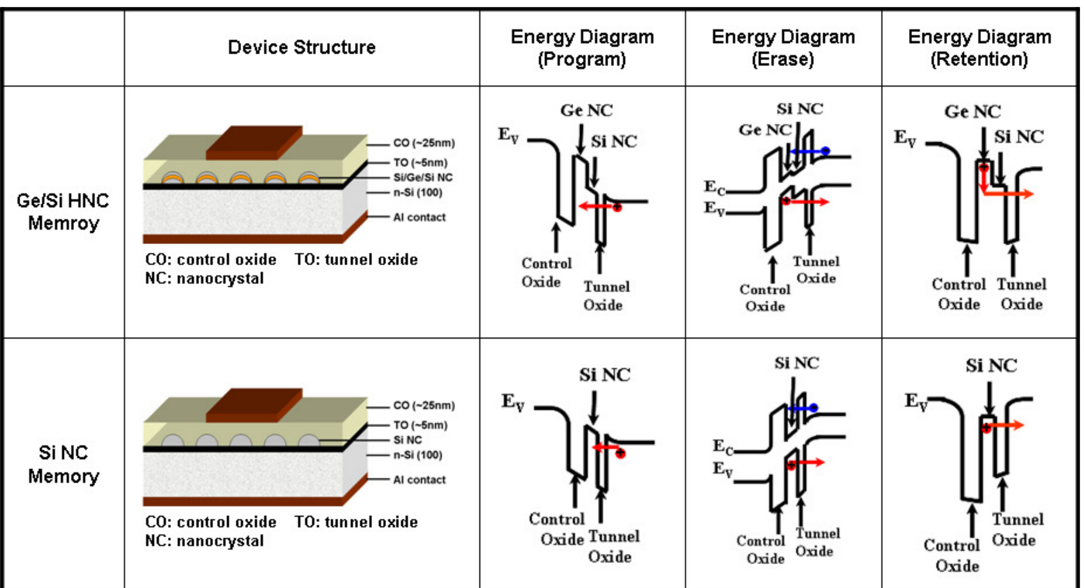


Table 3-1 Device structures of Ge/Si heteronanocrystal and Si nanocrystal memories with band diagrams under program, erase, and retention modes. Programming is realized by holes charging from substrate to Ge nanocrystals. Erasing is carried out through holes discharging from Ge to substrate and electrons tunneling from substrate into the Ge. The double barrier in Ge/Si heteronanocrystal memory elongates the holes storage time during retention.

3.2 Experiment

3.2.1 Si nanocrystal growth

Before growing Ge/Si heteronanocrystals, it is necessary to investigate Si nanocrystals first. There are many ways to synthesize Si nanocrystals, such as chemical vapor deposition, sputtering, Si ion implantation. In this work, we use low pressure chemical vapor deposition to grow Si nanocrystals. Basically to form Si nanocrystals, the growth goes through four steps: incubation, nucleation, growth and coalescence [28]. As deposition time goes, Si precursor, such as SiH_4 or Si_2H_6, adsorbs onto the oxide surface and with hydrogen desorption Si adatoms start to nucleate. The incubation stage has little visible dot formation. During the nucleation

stage, the dot density grows with deposition time. To the growth stage, the dot density remains stable while the size of the dots grows. This is the desirable stage for ease of process control. Finally in the coalescence stage, dots start to merge to a large island while dot density starts to decrease. With further growth, the dots will eventually form a continuous film.

The growth temperature, time, and substrate treatments all affect the growth of sample. Figure 3-1 shows the scanning electron microscope (SEM) images of Si nanocrystal grown at different temperature with other growth parameters fixed, the pressure of 200mTorr and SiH_4 flow rate of 100sccm, respectively. It can be seen that the nucleation sites for Si increases with increasing of the growth temperature from 580ºC ~ 620ºC until reaching a certain point where nanocrystal coalescence occurs, at 650ºC. At 580ºC, the nanocrystal density is estimated as $1.2\times10^{11}cm^{-2}$, where nucleation starts to form dots. For temperature lower than 580ºC, such as 550ºC, there were no visible dots seen. When temperature increases to 600ºC, the dot density increases to $2.5\times10^{11}cm^{-2}$ and this density does not change much when temperature increases to 620ºC. After this saturation point, at 650ºC, the nanocrystals start to coalesce and end up with a large nanocrystal size and compromised dot density, dropping to $1.5\times10^{11}cm^{-2}$, which due to the high-temperature-induced strong surface diffusion. In addition to the nanocrystal density, it is noted that the nanocrystal size insignificantly change with temperature before it is too high resulting in coalescence. For example, the size at temperature of 580ºC, 600ºC and 620ºC is all about 10nm, indicating that the adatom diffusion concentration gradient on the surface leads to a partially self-organized growth. This self-organized growth effectively eliminates the any severe occurrence of charge percolation.

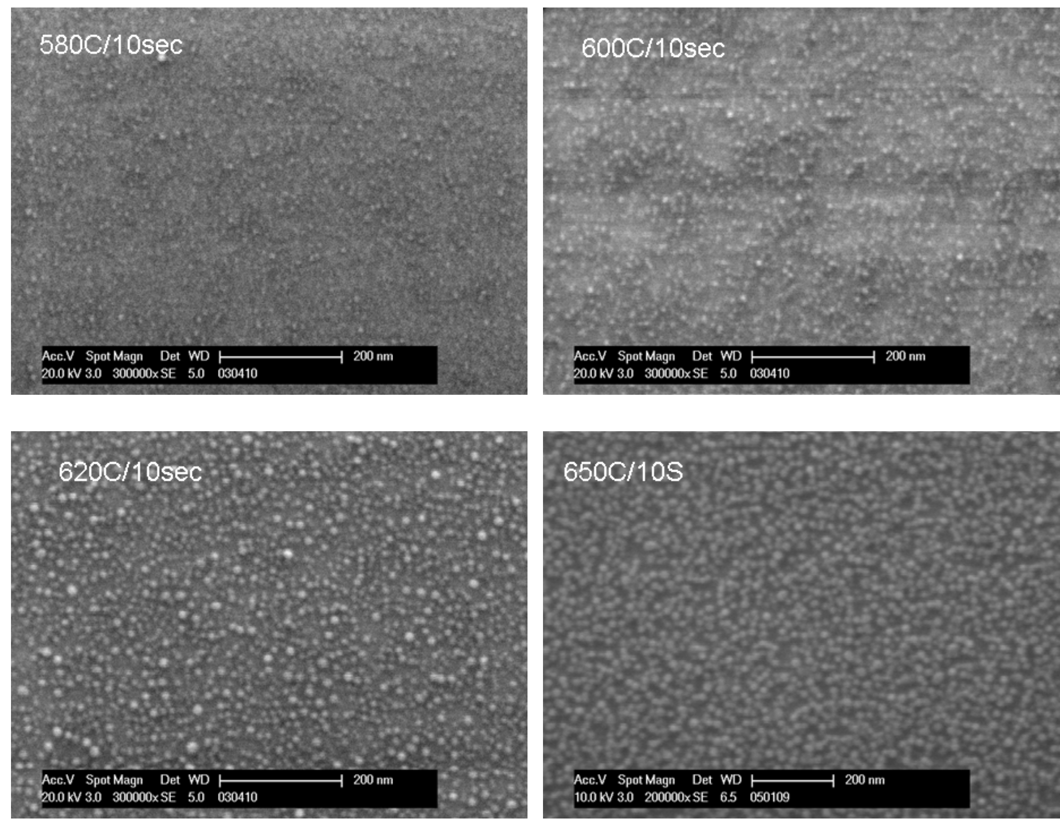


Figure 3-1 Scanning electron microscope (SEM) images of Si nanocrystals grown at temperature 580ºC, 600ºC, 620ºC and 650ºC.

Figure 3-2 shows the SEM images of Si nanocrystals grown at different time with other growth parameters fixed at temperature of 600ºC, pressure of 200mTorr and SiH_4 flow rate of 100sccm. It is seen with 5 seconds growth, Si nucleation is already shown with dot density around $2\times10^{11}cm^{-2}$. As growth time increases to 15 seconds, the dot density reaches $5\times10^{11}cm^{-2}$. With 20 seconds growth, the dot density decreases due to the small dots coalescence and bigger dots consuming smaller ones.

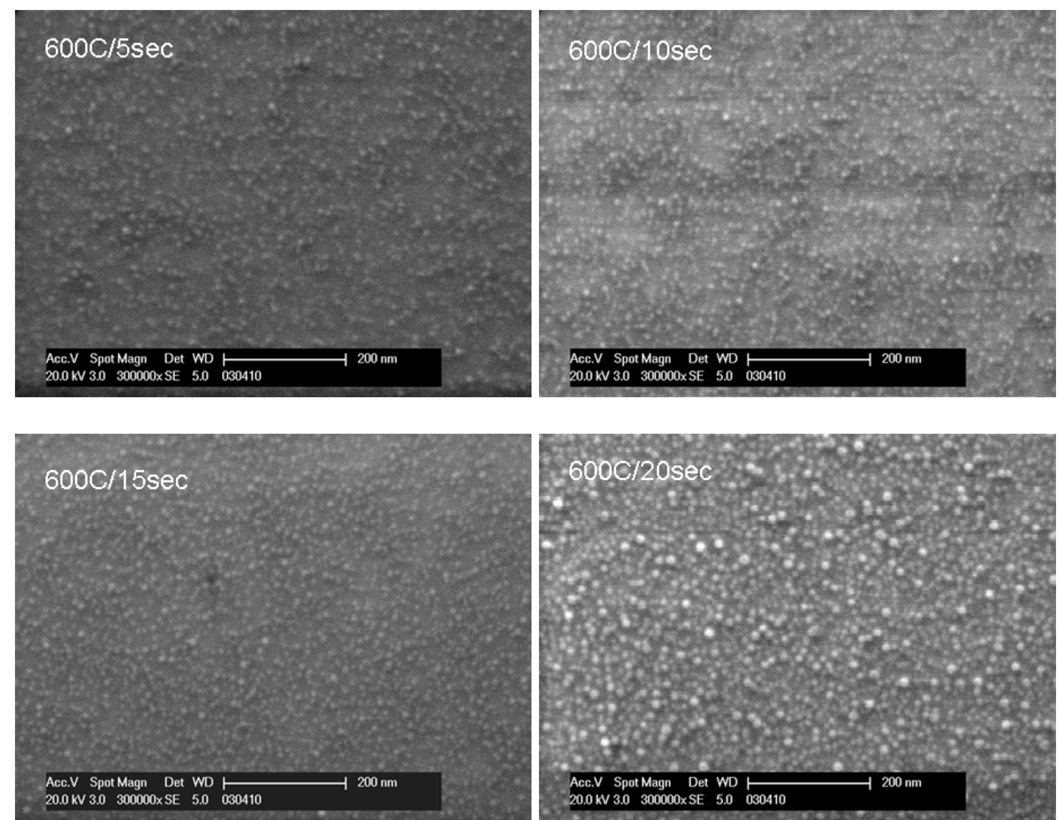


Figure 3-2 SEM images of Si nanocrystal grown for different period of time from 5 seconds to 20 seconds at temperature of 600ºC, pressure of 200mTorr and SiH_4 flow rate of 100sccm. The dot density increases with growth time until coalescence or ripening happens resulting in bigger dots with lower dot density.

By tuning the growth conditions, the highest Si dot density we got is $5\times10^{11}cm^{-2}$, grown at 600ºC for 15 seconds at 200mTorr with SiH_4 flow rate of 100sccm. In addition to tuning and optimizing the LPCVD Si growth condition, the substrate preparation is also essentially important to determine the Si dot density. For example, as reported in [29-30], dipping the as-grown thermal oxide in dilute HF solution followed by an annealing helps increasing the dot density by creating more surface silanol bonds (Si-OH), which serves as Si nanocrystal nucleation site. With this surface treatment, we also improved our Si dot density from $1\times10^{11}cm^{-2}$ to $5\times10^{11}cm^{-2}$ at the optimized growth condition, as shown in Figure 3-3.

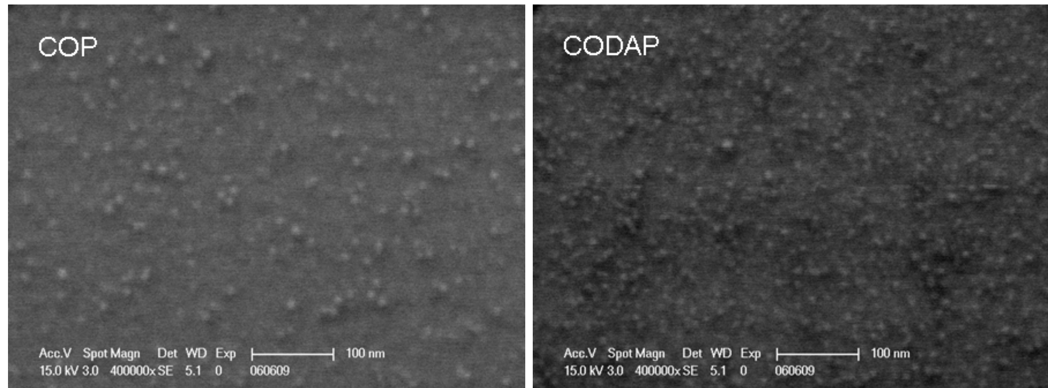


Figure 3-3 SEM images of Si nanocrystals deposited on as-grown thermal oxide (COP) and HF-treated thermal oxide (CODAP). The dot density achieved by dipping into HF solution is 2.5 times higher than that without surface treatment.

3.2.2 Ge/Si heteronanocrystal growth

Ge selective growth on Si has been demonstrated in both one-dimensional (1D) and two-dimensional (2D) array [31-33] through the template windows. Chemical vapor deposition and gas source molecular beam epitaxy (MBE) with Cl and H chemistry are successfully used to achieve selective growth of Ge on patterned Si substrates. Solid source MBE has also been demonstrated for 2D Ge selective growth with threading-dislocation free.

In this section, we report zero dimensional (0D) self-assembly of Ge/Si heteronanocrystals for memory application. Above we have discussed Si nanocrystals deposition by LPCVD and for Ge/Si heteronanocrystals growth we used the same chamber to sequentially flow SiH_4 and GeH_4 to form the nanocrystals stack. Figure 3-4 shows the SEM images taken for Si nanocrystals grown at 600ºC for 10 seconds and Ge growth on Si nanocrystals at a series of growth temperature from 250ºC to 450º. Other growth parameters were fixed at growth time of 3 minutes, pressure of 200mTorr and flow rate of GeH_4 of 5sccm. It is found that at 250ºC, the nanocrystal

density and average size after Ge growth is pretty much similar to the Si nanocrystals, indicating the temperature is not enough to induce the selective Ge growth. At temperature range of 300ºC to 400ºC, the Ge/Si heteronanocrystal shows a similar dot density and larger dot size than Si nanocrystal, indicating that the Ge is actually well-aligned with the Si nanocrystals underneath. However at temperature of 450ºC, the size of the heteronanocrystals are not uniformly increasing, but at certain places nanocrystal ripening occurs. In addition to temperature, growth time was also studied for Ge growth at 400ºC with pressure of 200mTorr and flow rate of 5 sccm. Figure 3-5 shows the SEM images of Ge growth at 400ºC from 1 minute to 5minutes, where we found that 3minutes growth gives the optimized dot density and size. The size distribution of Ge/Si heteronanocrystals grown at 400ºC/3min and Si nanocrystals is shown in Fig. 3-6. The mean size of Si nanocrystals and Ge/Si heteronanocrystals are 5.96nm and 6.96nm, respectively. Since these numbers are obtained from SEM investigation, they represent more or less the “base” diameter of the nanocrystals, suggesting the larger size of the heteronanocrystals. We can speculate that the “height” of these heteronanocrystals is also larger although the accurate value was not determined from the atomic force microscope (AFM) images, which is shown in Fig. 3-7. The presence of Ge was verified by x-ray photoelectron spectroscopy (XPS). Figure 3-8 shows the XPS wide scan spectra collected for Ge/Si heteronanocrystals and Si nanocrystals. The Ge signals are clearly observed in the Ge/Si heteronanocrystals curve. To further verify the Ge/Si heteronanocrystals formation, in the same LPCVD chamber, tunnel oxide without Si nanocrystals on top were subjected to the same Ge growth conditions. In this case, no Ge signals were found in XPS, which suggests that Ge does not nucleate on the tunnel oxide at low temperature.

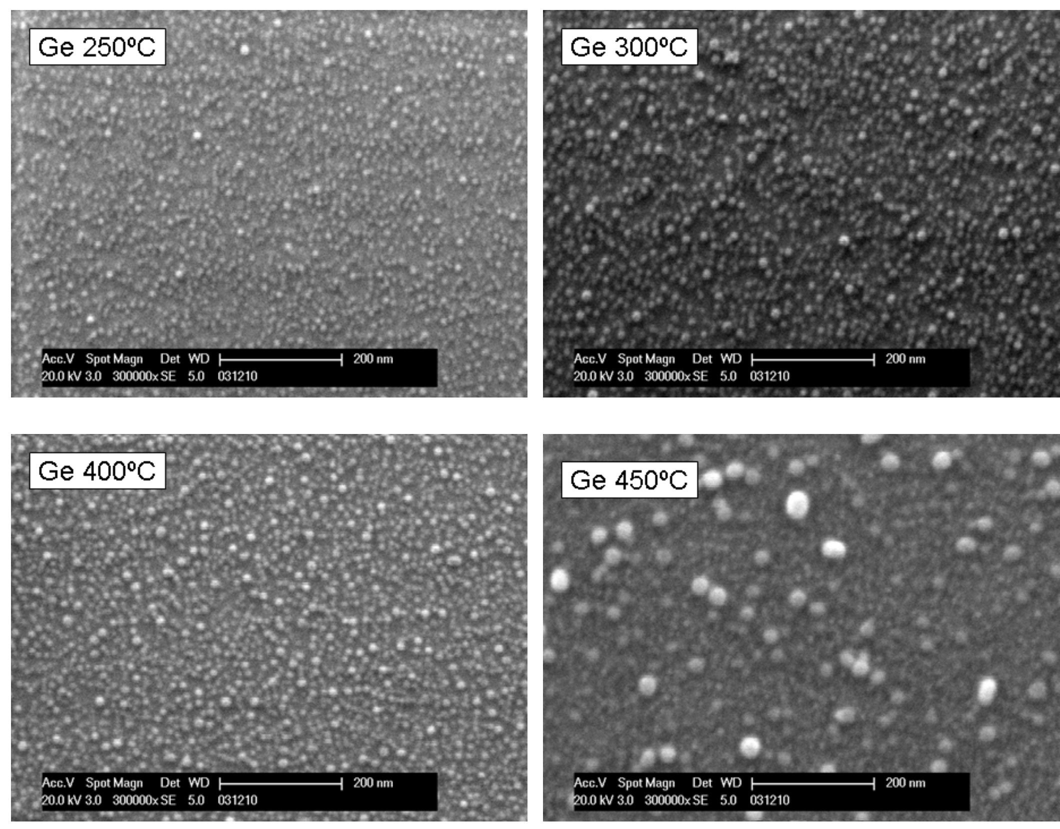
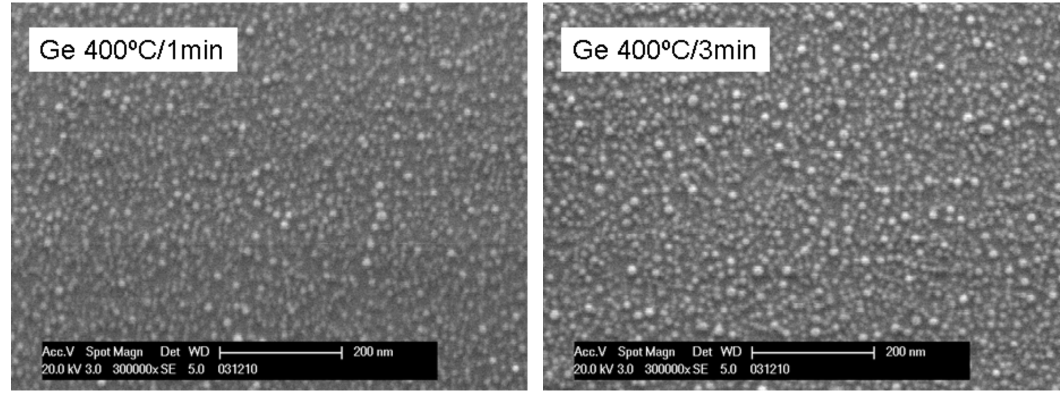


Figure 3-4 SEM images of Ge growth on Si nanocrystals showing temperature effect. The growth time is 3minutes, the pressure is 200mTorr and the GeH_4 flow rate is 5sccm.



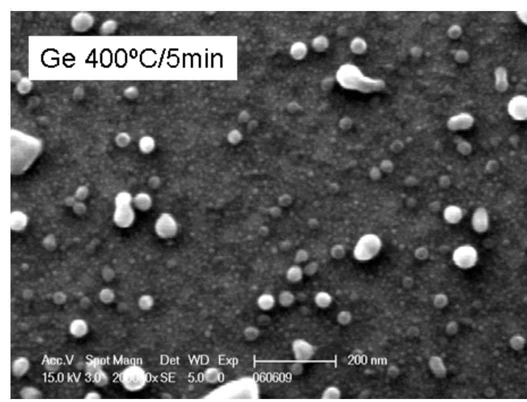


Figure 3-5 SEM images of Ge growth on Si nanocrystals showing growth time effect. The growth temperature is fixed at 400ºC, the pressure at 200mTorr and GeH_4 flow rate at 5sccm.

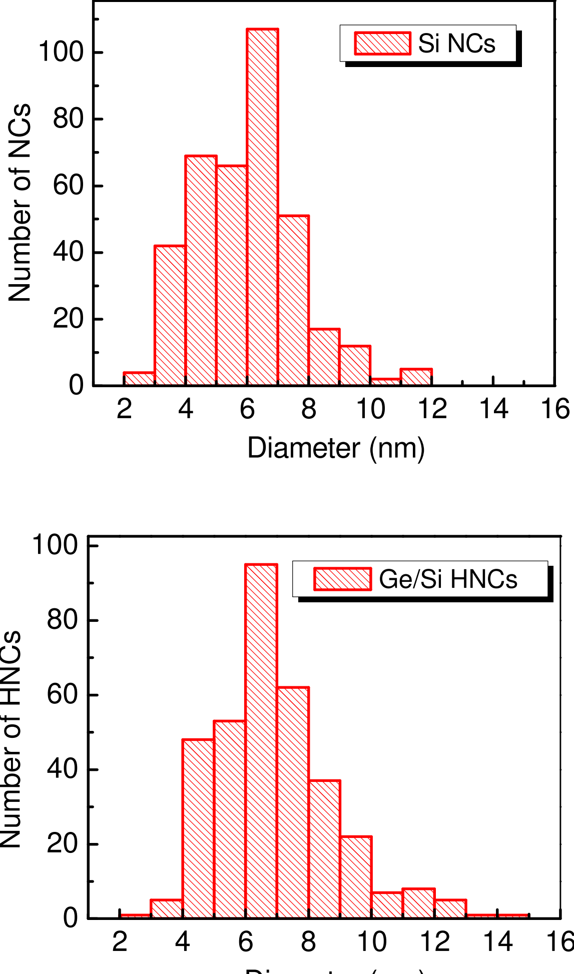


Figure 3-6 Size distribution of Si nanocrystals and Ge/Si heteronanocrystals. The average size is read as 6nm and 7nm for Si and Ge/Si nanocrystals, respectively.

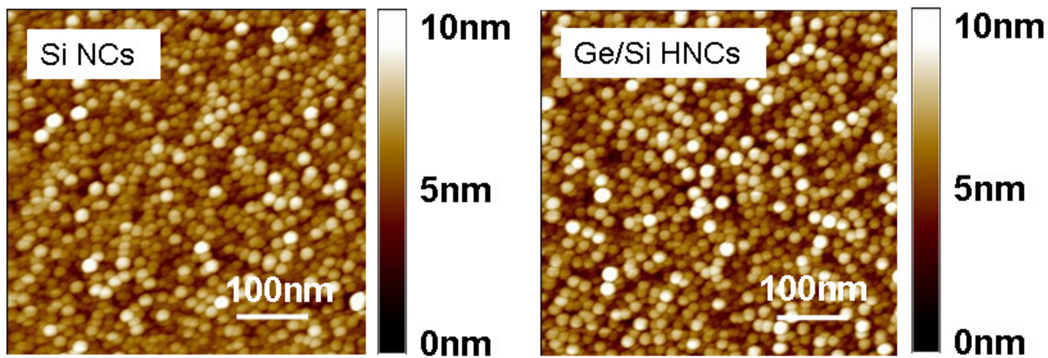


Figure 3-7 AFM images of Si nanocrystals and Ge/Si heteronanocrystals.

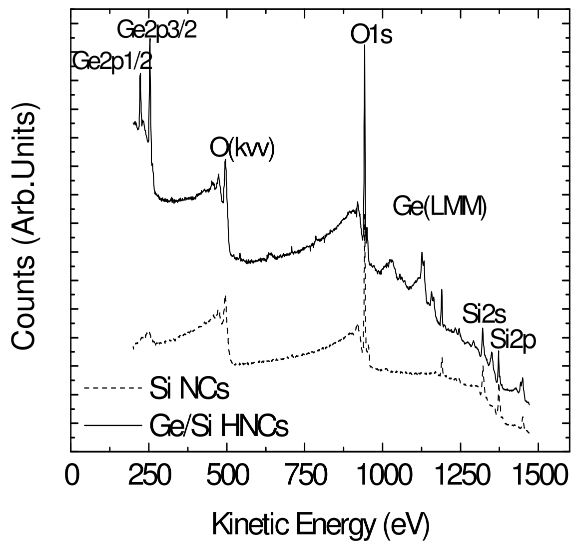


Figure 3-8 XPS elemental analysis for Si nanocrystals (dot) and Ge/Si heteronanocrystals (solid).

To protect the Ge from being oxidized in the following control oxide deposition process, a Si cap layer is necessary to cover the Ge/Si heteronanocrystals. In other words, our Ge/Si nanocrystal is essentially like Ge/Si core/shell structure. Figure 3-9 shows the SEM image of this core/shell nanocrystal. The temperature of 500ºC was used for this cap layer deposition to prevent Si from growing on the area with no

Ge/Si heteronanocrystals. The deposition time is 1 minute, the pressure is 200mTorr and flow rate of SiH_4 is 100sccm.

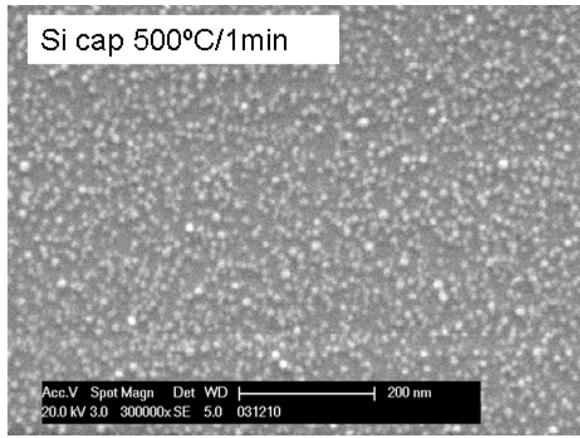


Figure 3-9 SEM image of Ge/Si core/shell nancorystals. Si cap layer was deposited at 500ºC for 1 minute. The pressure is fixed at 200mTorr and the SiH4 flow rate is 100sccm.

3.2.3 MOSFET memory with Ge/Si heteronanocrystal fabrication

P-MOSFET processes were used to fabricate the Ge/Si heteronanocrystal memory. Two reference devices (Si nanocrystal memory device and a MOSFET device without nanocrystal embedded) were fabricated simultaneously using the same processes as Ge/Si heteronanocrystal memory for comparison. The device fabrication began with an n-Si (100). Local oxidation of silicon (LOCOS) process was used to electrically isolate devices. Field oxide and nitride were deposited sequentially followed by photolithography and reactive ion etching (RIE) to define and expose the active region. Pre-diffusion cleaning was carried out followed by a 5nm tunnel oxide growth at 850°C and in-situ annealing in N_2 at 900°C. The thin nitride layer formed on tunnel oxide acts as the protection layer to suppress the leakage paths through the weak points in the SiO_2 layer. Then Si nanocrystals were deposited on the tunnel oxide at 600°C for 15sec in a LPCVD furnace followed by Ge selective growth on top

of Si nanocryals at 400°C and 200mTorr. After Ge/Si heteronanocrystals growth, in the same chamber, a Si cap layer was deposited to cover the Ge/Si heteronanocrystals. By controlling the deposition pressure and temperature, extra Si growth on oxide where no Ge/Si heteronanocrystals are covered can be effectively suppressed. The typical growth temperature and pressure is around 500ºC and 100mTorr, respectively. The fact that there is no extra Si growth was confirmed by the similar nanocrystal density before and after the cap layer deposition, because otherwise the density would become higher after the cap layer deposition. In addition, we used a reference SiO_2 sample, where no Ge/Si heteronanocrystals were pre-grown, to monitor the Si growth under the cap layer deposition conditions. No nanocrystal was found on that sample. The intention to deposit this Si cap layer is to protect the Ge from being oxidized in the following control oxide deposition step. In this step, SiH_4 and O_2 flow onto the sample at 400°C, at which Ge would be easily oxidized without cap layer protection. Control oxide of about 25nm was deposited at 400°C followed by polysilicon gate deposition. Ohmic contacts were formed on source, drain and gate to complete the device fabrication.

3.3 Device characterization

3.3.1 MOS memory Ge/Si heteronanocrystal

MOS capacitors with Ge/Si heteronanocrytals and Si nanocrystals embedded in the SiO_2 were characterized by C-V sweep measurements. The measurement was carried out by sweeping from the inversion to accumulation and then back to inversion again. Figure 3-10(a) shows the high frequency (1MHz), ±15V C-V sweeps of Ge/Si heteronanocrytal memory and Si nanocrytals memory. With the same device

size and sweep range, larger memory window is observed in Ge/Si heteronanocrytal capacitor compared to Si only nanocrytals capacitor, which indicates that Ge/Si heteronanocrytal memory has a larger storage capacity. Figure 3-10(b) shows the dependence of memory window on the sweep voltages of Ge/Si heteronanocrytal memory, further confirming the memory effect of our devices because the memory window increases with the scanning gate voltage. No such hysteresis is found in control device where no nanocrytals were embedded between control oxide and tunnel oxide, as shown in Fig. 3-10(c). This means that the oxide quality is good and the memory effect shown in the Ge/Si heteronanocrytal memory and Si nanocrytals memory is due to the charge stored in the nanocrytals rather than the defect or interface states charging.

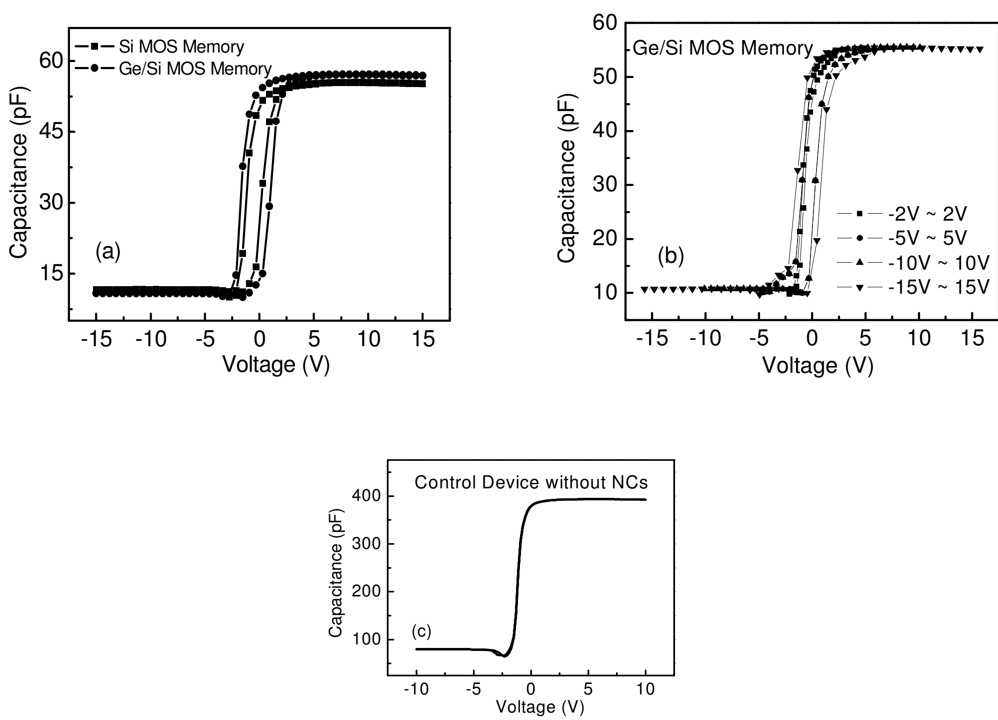


Figure 3-10 C-V sweep of (a) Ge/Si heteronanocrystal MOS memory and Si nanocrystal MOS memory, (b) Ge/Si hetero-nanocrytal MOS memory under different scanning gate voltage, (c) reference MOS capacitor without nanocrystals.

Figure 3-11 shows the retention characteristics of Ge/Si heteronanocrytal and Si nanocrytals MOS memories. After programming of holes onto the floating gate with gate bias of -20V for 2 seconds the transient capacitance (C_t) was recorded every 30ms. Flat band voltage (V_{FB}) shift is deduced by subtracting the voltage at C_t on the fresh C-V curve from the initial V_{FB}, where the capacitance starts to be recorded. It is shown that after 10^4 seconds, the percentage of hole charge loss of Ge/Si heteronanocrytal memory is only half compared with Si nanocrytals memory, which confirms that an additional quantum well exists in Ge side of the heteronanocrystals. The charge decay for Ge/Si heteronanocrystal and Si nanocrystals memories is a bit fast.

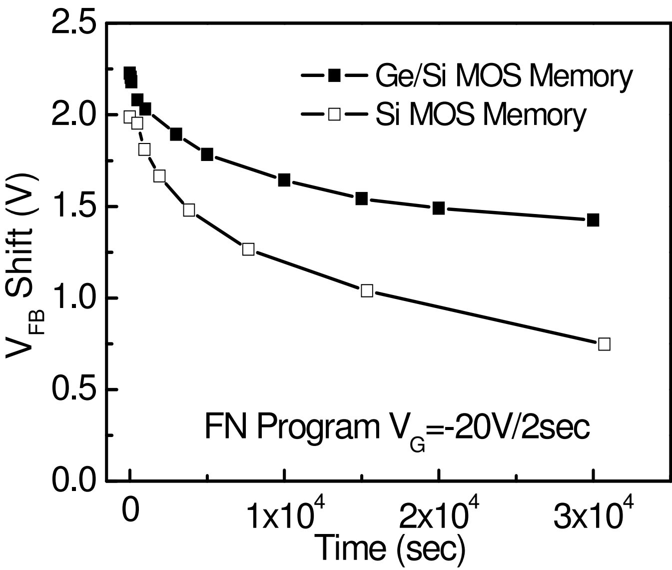


Figure 3-11 Hole charge retention characteristics of Ge/Si HNC and Si NC MOS memories. Slower charge delay was observed in Ge/Si hetero-nanocrystal memory.

3.3.2 MOSFET memories with Ge/Si heteronanocrystal

Fig. 3-12 shows three I_D-V_G curves, from left to right, corresponding to programmed, neutral and erased states of the Ge/Si heteronanocrystal MOSFET memory, respectively. The gate bias conditions for programming and erasing are -15V/4sec and +16V/4sec, respectively. The shift of I_D-V_G curves indicates an evident memory effect. The threshold voltage value (V_T) represents the amount of the electrons/holes charged on the nanocrystals. As shown in Fig. 3-12, V_T increases (absolute value) in programming and decreases in erasing. It is found that V_T at erased state is smaller than neutral state. It is understandable considering that electron injection dominates the erasing process. After neutralizing the charged holes during programming, extra electrons were injected and stored in the nanocrystal to shift the V_T to smaller value than neutral state. The reason that electron injection dominates the erasing process is because of the smaller effective mass of electron and the lower injection energy barrier for electron, compared to hole.

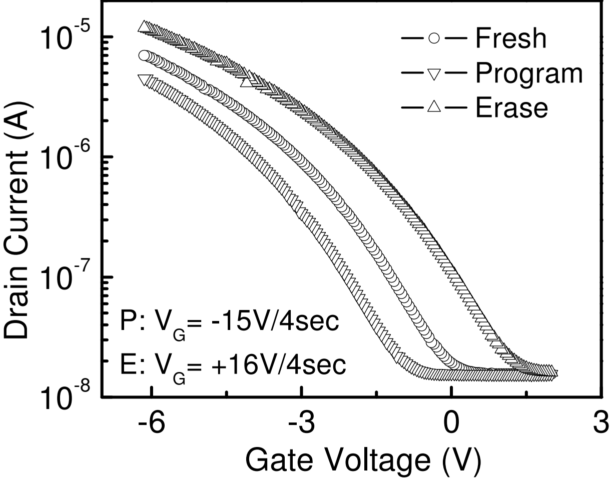


Figure 3-12 Transfer characteristics of Ge/Si heteronanocrystal MOSFET memory under fresh, FN programmed and FN erased conditions.

Figure 3-13 shows programming and erasing characteristics of the Ge/Si heteronanocrystal and Si nanocrystals memory devices. Gate bias of -15V and +15V were used to program and erase the devices. After 2 seconds both programming and erasing get saturated because of the coulomb blockade effect in nanoscale materials. Faster programming and a comparable erasing speed are observed in Ge/Si heteronanoscrytal memory compared with Si nanocrystals memory. Faster programming speed of Ge/Si heteronanocrystals relates to the fact that deeper quantum well in Ge/Si heteronanocrystal creates more energy levels compared to Si nanocrystals and the similar erasing speed is understandable considering that the electrons tunneling from channel to nanocrystals dominates the whole erasing process. Larger memory window in Ge/Si heteronanocrystal memory (the voltage difference between the erased and programmed states) is due to more energy levels in larger Ge/Si well than Si well.

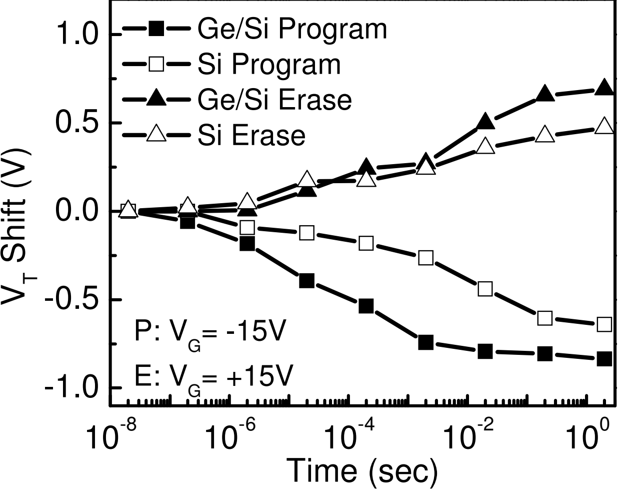


Figure 3-13 Hole charge programming and erasing characteristics of Ge/Si heteronanocrystal and Si nanocrystal MOSFET memories.

Figure 3-14 is the retention performance comparison between Ge/Si HNC memory and Si NC memory, which plots threshold voltage shift as a function of waiting time. Programming condition is gate bias of -15V for 4 seconds to fully charge the device before the threshold voltage is recorded. There was no stress applied in-between measurement points, which explains why the retention time for MOSFET memory appears much longer than that from the MOS capacitor memories, where flat band voltage was recorded with gate bias applied. Slower hole charge decay was found in Ge/Si HNC memory, especially at the early retention stage. This is because, for Ge/Si HNC memory, most of the holes prefer to store inside the Ge NCs. To leak back to the channel, these holes have to be thermally activated to overcome the Si NC barrier first before it can tunnel through the tunnel oxide and back to the channel. While for Si NC memory, charging of the defect levels within Si NCs dominates the programming process. Defect-related charging is not reliable [34].

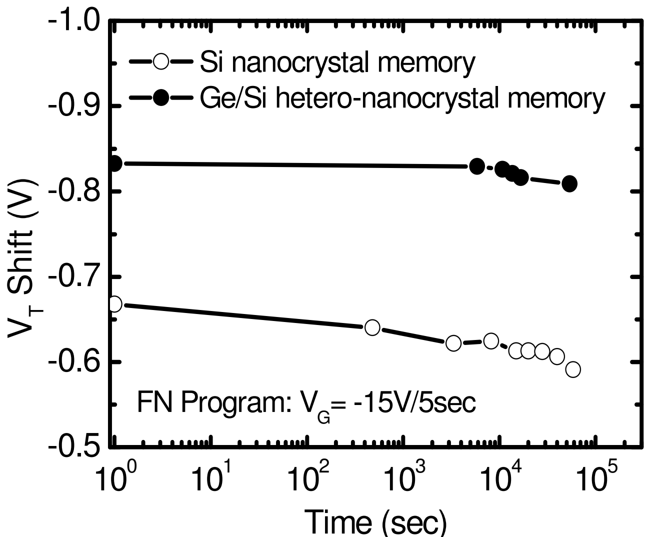


Figure 3-14 Hole charge retention characteristics of MOSFET memory with Ge/Si heteronanocrystals and Si nanocrystals as floating gate after FN programming.

Figure 3-15 shows the endurance characteristics of Ge/Si heteronanocrystal and Si nanocrystal memories. The programming and erasing conditions are -15V/20ms and +15V/20ms, respectively. Both devices exhibit good endurance behavior up to 10^5 cycles of operation.

In addition to FN operation, HCI programming was also used to operate the devices and the device performance was compared between Ge/Si heteronanocrystal memory and Si nanocrystal memory. Figure 3-16 shows HCI programming characteristics of Ge/Si heteronanocrystal and Si nanocrystal memories. Both gate voltage and drain voltage affect the programming speed. A large threshold voltage shift of about 0.913V can be achieved under V_G= -10V and V_D= -7V for 2 seconds in the Ge/Si heteronanocrystal memory. As shown in Fig. 3-16, similar to FN programming characteristics, Ge/Si heteronanocrystal memory exhibits faster programming speed with HCI programming.

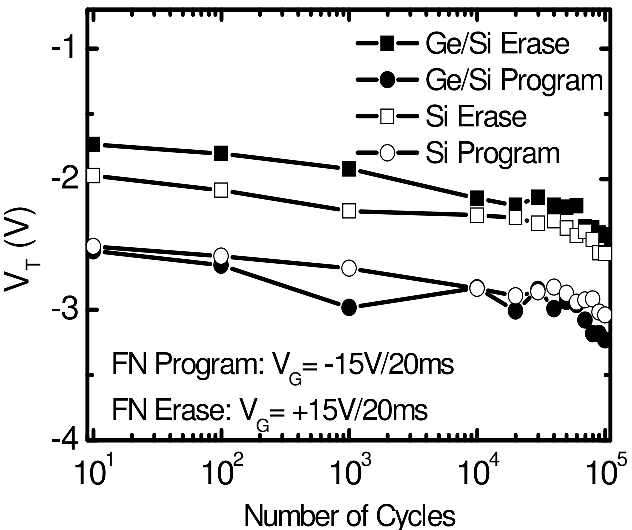


Figure 3-15 Endurance characteristics of Ge/Si heteronanocrystal and Si nanocrystal MOSFET memories. Programming and erasing are through FN operations.

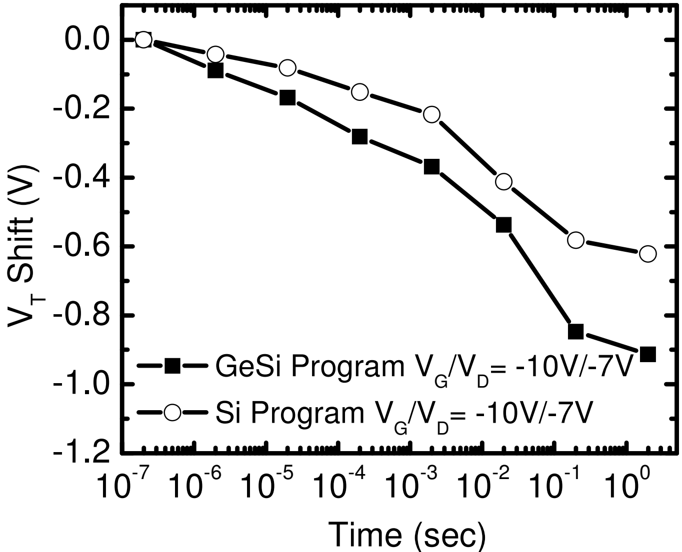
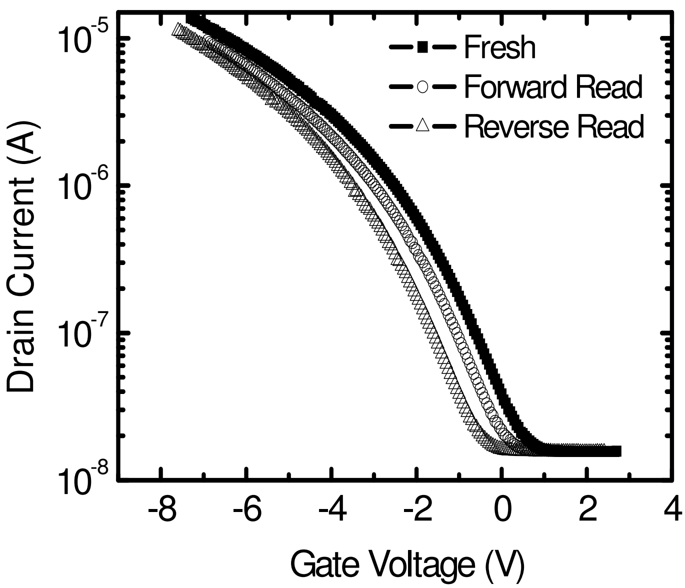


Figure 3-16 Hole HCI programming characteristics of Ge/Si heteronanocrystal and Si nanocrystal memories.

After hot carrier programming, most charges have been written into the heteronanocrystals near the drain side while those nanocrystals near the source side are partially charged or uncharged. Therefore, two threshold voltage states can be obtained when the device is read from drain side (forward read) and source side (reverse read), respectively. Figure 3-17(a) shows I_D-V_G curves at fresh, reverse and forward read conditions, indicating different threshold voltage shift. Figure 3-17(b) shows threshold voltage shift measured in forward and reverse read conditions after HCI programming of the Ge/Si heteronanocrystal memory. Two sets of threshold voltage shift are clearly observed. Different threshold voltage shift with different drain voltage during forward reading is because the bias on drain side effectively changes the barrier height for the channel carriers while during reverse read this barrier height is insignificantly affected by small read voltages, which explains independence of threshold voltage shift on the source side bias.



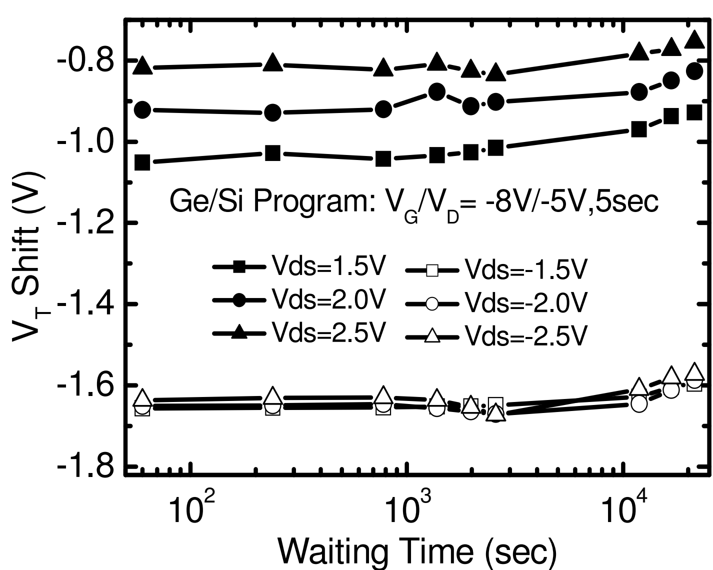


Figure 3-17 (a) I_D-V_G curves at fresh and HCI programmed modes, including reverse and forward read conditions, and (b) threshold voltage shift measured in forward and reverse read conditions after HCI programming of the Ge/Si heteronanocrystal memory.

While p-channel MOSFET Ge/Si heteronanocrystal memory exhibits superior hole storage because of the type-II energy band alignment between Ge and Si, it is

interesting to investigate electron storage due to its small effective mass and less damage during the operation. Other than deeper potential well between valance band of Ge and Si for holes storage, there also exists a potential well between conduction band of Si nanocrystal and SiO_2 for electrons storage as shown in Table 3-1. Basically band to band tunneling was used for hot electron injection. Figure 3-18 shows how this injection occurs. A positive gate voltage and negative drain voltage are applied so that p+-drain/n-channel junction is reversely biased. The electrons generated in this junction via band-to-band tunneling can be re-directed into the floating dots near the drain side under the electrical field between gate and channel. Therefore the threshold voltage sensed from drain and source side is different because of this locally charged floating gate. Similar programming scheme for using electron to program p-channel device was reported by other researchers [33].

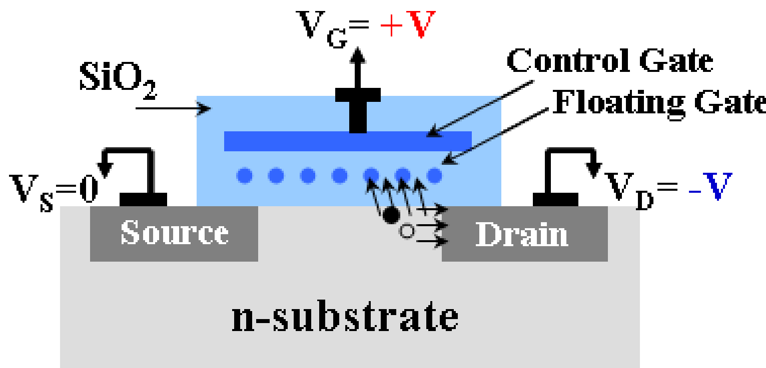


Figure 3-18 Schematic of hot electron injection operation.

Figure 3-19 shows the transient electron charging characteristics of Ge/Si heteronanocrystal memory using HCI to program. The efficiency of the programming is improved with increasing bias combination of control gate and drain, and this phenomenon was also found in holes storage characteristics. Figure 3-20 shows the

programming and erasing characteristics of Ge/Si heteronanocrystal and Si nanocrystal memories using HCI to program and FN to erase the electrons. With HCI programming, memory windows of 0.813V and 0.668V are reached in Ge/Si heteronanocrystal and Si nanocrystal memories, respectively, with control gate and drain bias of 10V/-7V for 2 seconds. The slightly larger memory window in Ge/Si heteronanocrystal memory indicates that, during programming, not only Si nanocrystal is charged, but also Ge nanocrystal and interface level charging play a role to the threshold voltage shift. The programming and erasing speeds do not show much difference between Ge/Si heteronanocrystal memory and Si nanocrystal memory and it is due to the fact that electrons are charged/discharged through the Si nanocrystals in both devices. Figure 3-21 shows the electron retention characteristics of Ge/Si heteronanocrystal memory and Si nanocrystal memory. The devices were programmed with gate and drain bias of 11V and -8V, respectively, for 10 seconds. The charge decay within the 15 hours for Ge/Si heteronanocrystal and Si nanocrystal memories are very similar. The electron retention is worse than hole retention due to the shallower electron barrier in the conduction band edge.

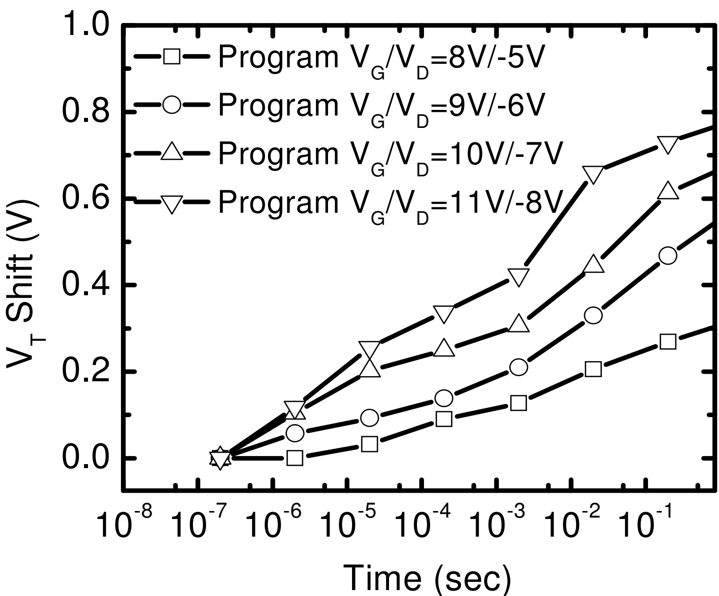


Figure 3-19 Electron charge HCI programming characteristics of Ge/Si heteronanocrystal memory with four sets of control gate and drain bias.

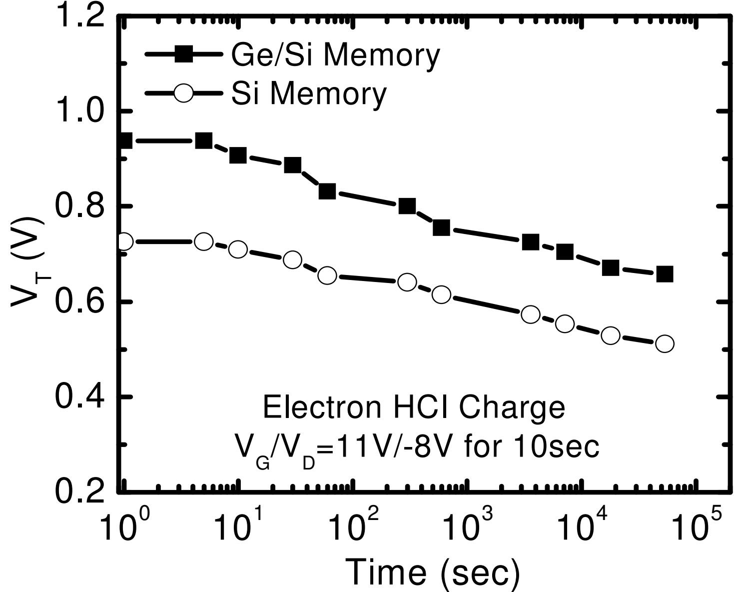


Figure 3-20 Electron charge HCI programming and FN erasing characteristics of Ge/Si heteronanocrystal and Si nanocrystal memories.

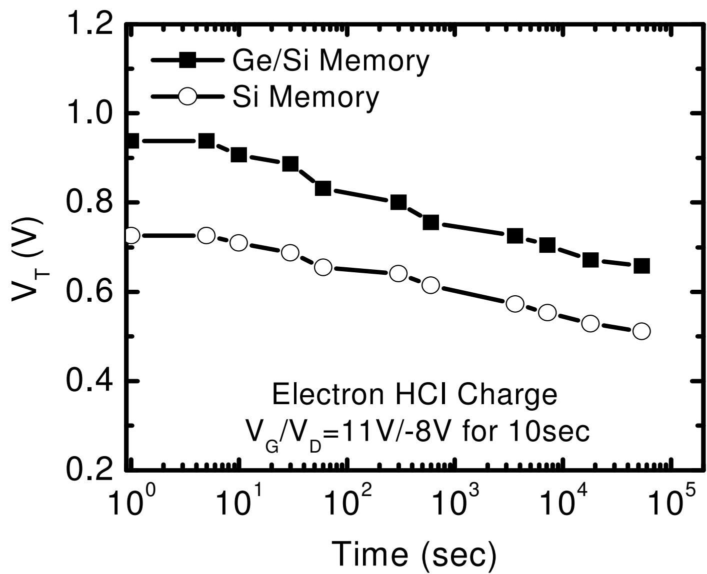


Figure 3-21 Electron charge retention of Ge/Si heteronanocrystal and Si nanocrystal memories after HCI programming. The programming condition is indicated in the figure.

3.4 Summary

Ge/Si self-assembled heteronanocrystals with high density were grown using LPCVD. MOS capacitors and MOSFET memory devices with Ge/Si heteronanocrystals and Si nanocrystals embedded between control and tunnel oxide were fabricated with the same process flow. Both FN and HCI programming were used to operate the devices. Enhanced performance of Ge/Si heteronanocrystal memory is achieved compared to Si nanocrystal memory, including improved retention time, faster programming speed and larger charge storage capability.

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Chapter 4: $CoSi_2$-coated Si nanocrystal memory

4.1 Motivation

Nonvolatile memories with discrete charge traps are extensively investigated as one of the possible solutions to the scaling limit of flash memory devices. The localized charge in electrically discrete nodes guarantees insensitivity to stress-induced oxide defects and therefore allows for thinner tunnel oxide and faster programming/erasing speed. Moreover drain turn-on effect is suppressed by using nanocrystals as floating gate so that the cell length can be further scaled.

Recently much effort has been made to develop nonvolatile memory devices using nanocrystals, such as Si [1], Ge [2], metal [3-5] and dielectric materials [6-7]. Other novel structures such as double stack of nanocrystals [8], engineered dielectric tunneling layers [9-10], and hetero-nanocrystals [11-12] are also reported with good memory performance. Metal nanocrystal memory has the advantage over semiconductor counterparts in terms of higher density of states around Fermi level, which is normally aligned in the forbidden gap of Si, leading to larger memory window and stronger coupling between the nanocrystals and the substrate for faster programming. A wide range of metal nanocrystal materials, such as Au, Ni, and W, have been successfully implemented [13-15]. Silicide-based nanocrystals, which have metallic nature of high density of states and high thermal stability, were proposed to improve memory performance [16]. Shortly after these efforts, other groups followed up with their own efforts on silicide nanocrystal MOS memories [17-23]. For examples, $CoSi_2$ nanocrystals were formed by exposing the Co/Si/HfO2/Si stacks in an external UV laser [17]; Double-layer $CoSi_2$ nanocrystal MOS memory was formed

by evaporating Si/Co/Si tri-layer on tunnel oxide followed by rapid thermal annealing [18].

In this chapter, $CoSi_2$-coated Si nanocrystals are used as the discrete charge traps and MOSFET memories are fabricated and characterized. These $CoSi_2$-coated Si nanocrystals were formed by silicidation of Si nanocrystals on SiO_2 and subsequent selective etching of unreacted metal cobalt over silicide, a process which is similar to the fabrication of $TiSi_2$/Si heteronanocrystals [16]. Nevertheless, there are several advantages of using $CoSi_2$ over $TiSi_2$ in this process. Among all silicides, $CoSi_2$ shows little reactivity with metal/oxide interface [24]. The formation of $TiSi_2$ on Si nanocrystals by annealing is much more difficult and requires much higher temperature due to fine-line effect [25]. Owing to high-density interface states between silicide and Si, the defects induced during original formation of Si nanocrystals may be pinned at the Fermi level of silicide [26-30], leading to uniform programming/erasing among the devices on a chip. This was not recognized in our earlier $TiSi_2$ nanocrystal memory effort [11]. Furthermore, $CoSi_2$ pins the Fermi level deeper than that of $TiSi_2$, leading to better electron retention. Compared with other methods as discussed earlier, $CoSi_2$-coated Si nanocrystals approach presents minimized change in the process of Si nanocrystal memories, which are currently pursued by industry for commercialization.

4.2 Experiment

4.2.1 Device fabrication

A 5nm thermal oxide was grown on the p-Si (100) substrate at 850℃ for 5min followed by a 900℃ in-situ annealing in N_2. Si nanocrystals were deposited on the

tunnel oxide by LPCVD at 600℃ and 200mTorr. After the Si nanocrystals deposition the wafer was immediately transferred to another chamber for cobalt sputtering. The thickness of the deposited cobalt film is about 1~2nm. Two steps of annealing at 600 ℃ and 850℃, respectively, and selective etching of unreacted Co over $CoSi_2$ in the mixture of H_2SO_4 and H_2O_2 were carried out to form $CoSi_2$-coated Si nanocrystals. Then a 20nm control oxide was deposited at 400℃ by LPCVD followed by un-doped poly-Si deposition and patterning. Phosphorous atoms were implanted to form heavily-doped gate/source/drain regions simultaneously. Aluminum was evaporated as the contacts to the three terminals. Reference Si nanocrystals memory and a device without any floating nanocrystals were also fabricated in the same fabrication run for comparison. The process flow is shown in Figure 4-1. Figure 4-2 shows a photography of a device after processing. Soruce, drain, gate pads and active region of the device are clearly shown.

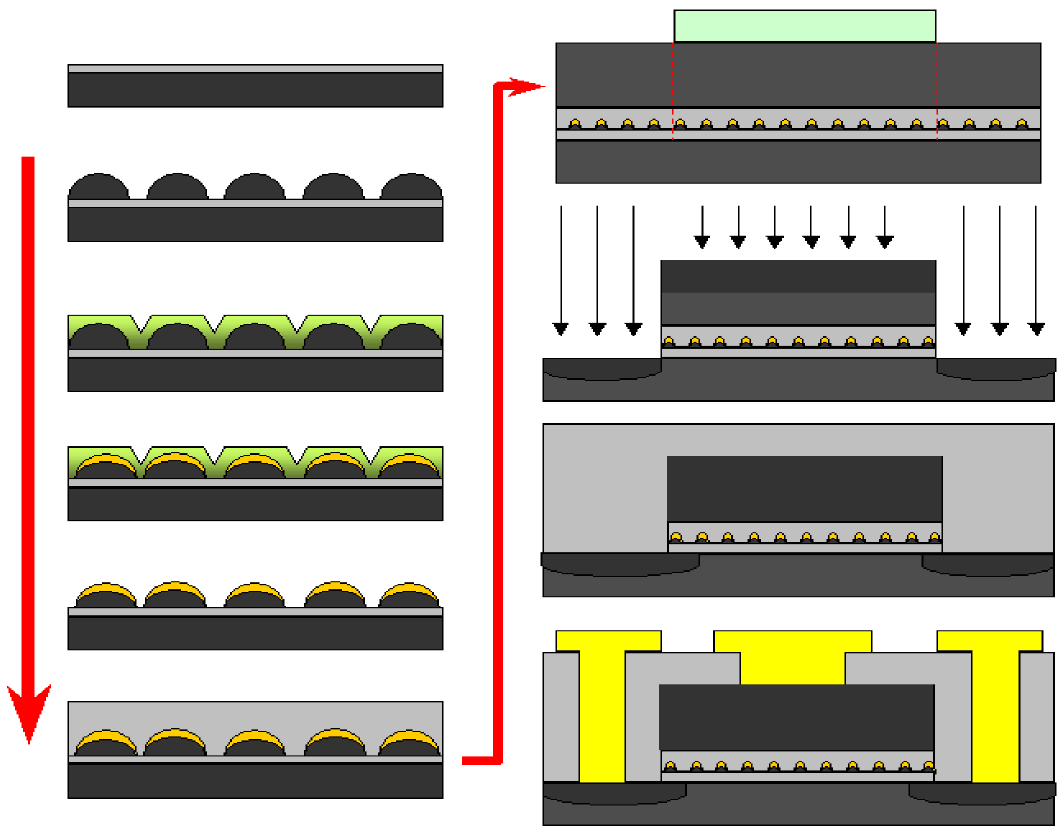


Figure 4-1 Process flow for fabrication of $CoSi_2$-coated Si nanocrystal MOSFET memory device.

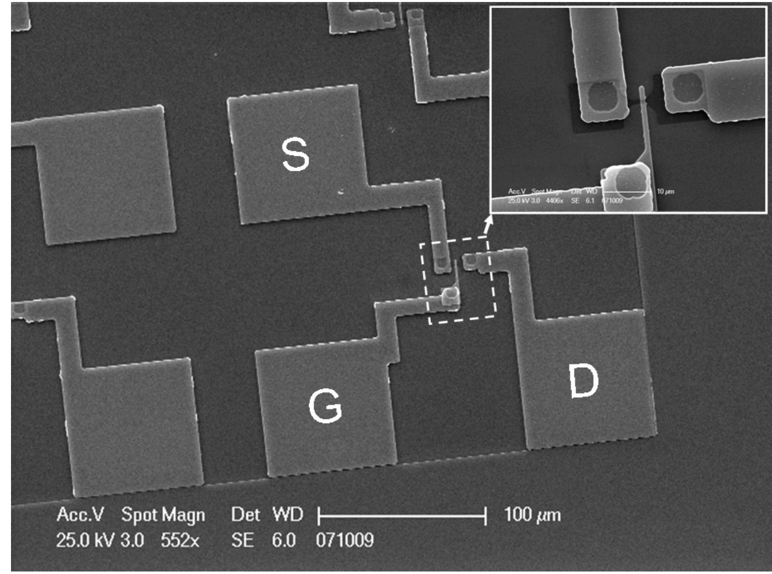
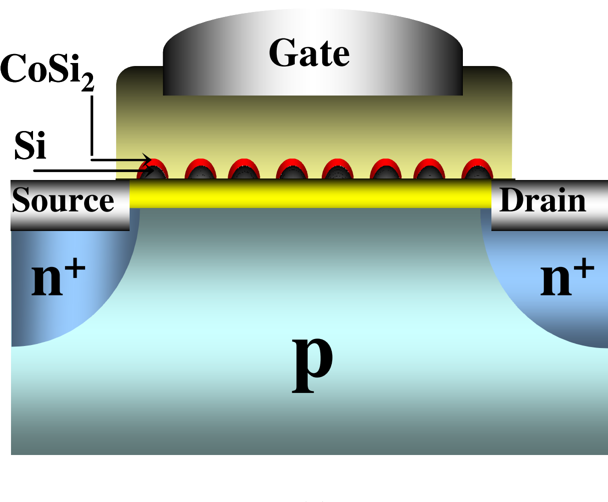
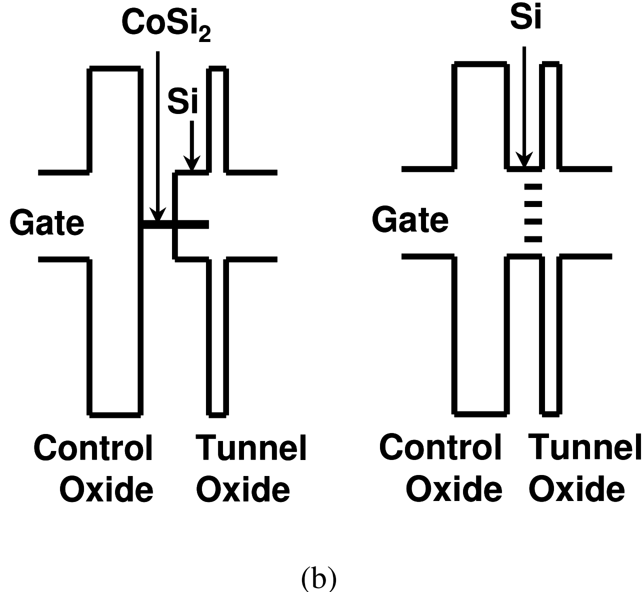


Figure 4-2 $CoSi_2$-coated Si nanocrystal MOSFET memory pattern. Inset is the magnified image showing the active region.

Figure 4-3(a) shows the schematic cross section of $CoSi_2$-coated Si nanocrystal memory. Figure 4-3(b) shows energy band diagrams for both $CoSi_2$-coated Si nanocrystal memory and Si nanocrystal memory. The wide distribution of defect related deep levels are associated with the Si nanocrystal memory [31], as depicted in the schematic of Fig. 3-1(b) in the right. Although the existence of these defects in Si nanocrystals results in relatively long retention performance, this defect-related retention enhancement is not thermally robust [32]. The left one in Fig. 4-3(b) is the diagram of $CoSi_2$-coated Si nanocrystal memory. The reported work function of $CoSi_2$ is 4.55eV [33], namely, the Fermi-level of $CoSi_2$ is within the band gap of Si and close to Si intrinsic Fermi-level. However when $CoSi_2$ connects with Si, the actual Fermi-level of $CoSi_2$ is pinned around Si valance band, together with those interface defect states [26-27]. Owing to the pinning effect and high density of states around the Fermi level, $CoSi_2$-coated Si nanocrystal memory can achieve larger storage capacity, more uniform program/erase and stable retention performance.



(a)



(b)

Figure 4-3 (a) Schematic of $CoSi_2$-coated Si nanocrystal memory device, and (b) energy band diagrams of $CoSi_2$-coated Si nanocrystal and Si only nanocrystal memories. Wide distribution of deep levels arises from embedding of Si nanocrystals in oxide (right schematic). These deep levels may be pinned along the Fermi level of $CoSi_2$ (left schematic).

4.2.2 $CoSi_2$-coated Si nanocrystal characterization

The insets (a) and (b) of Fig. 4-4 show the scanning electron microscope (SEM) images of Si nanocrystals and $CoSi_2$-coated nanocrystals, respectively. The average size of Si nanocrystals and $CoSi_2$-coated Si nanocrystals is 10nm and 12nm, respectively, and the density of dots for both Si and $CoSi_2$-coated Si is about $4x10^{11}cm^{-2}$, indicating that

$CoSi_2$ and Si nanocrystals are well self-aligned. Figure 4-4 is the Energy dispersive x-ray analysis (EDX) spectrum of $CoSi_2$-coated Si nanocrystals. Cobalt signal at 6.9eV is clearly observed. Because we had a selective etching step in between two annealing steps to have unreacted Co removed, Co signal in the spectrum suggests that $CoSi_2$ is formed and covers the Si nanocrystals.

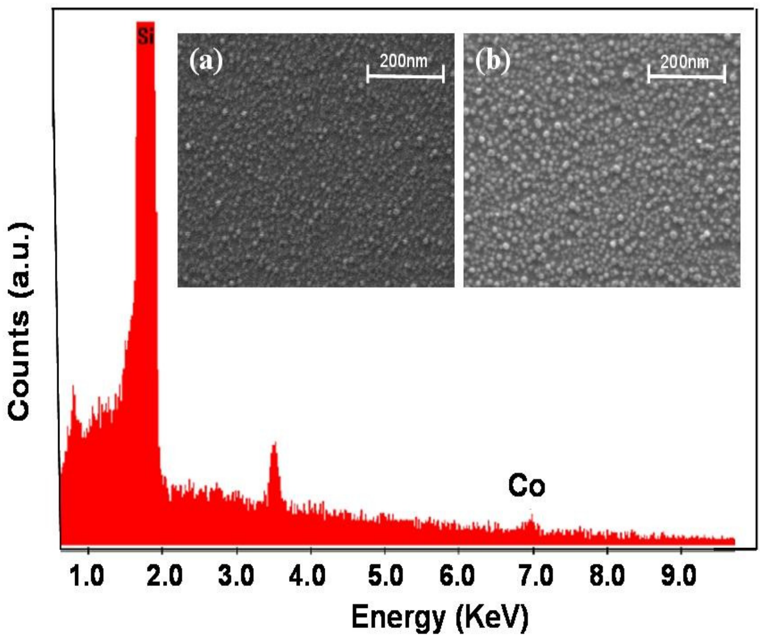
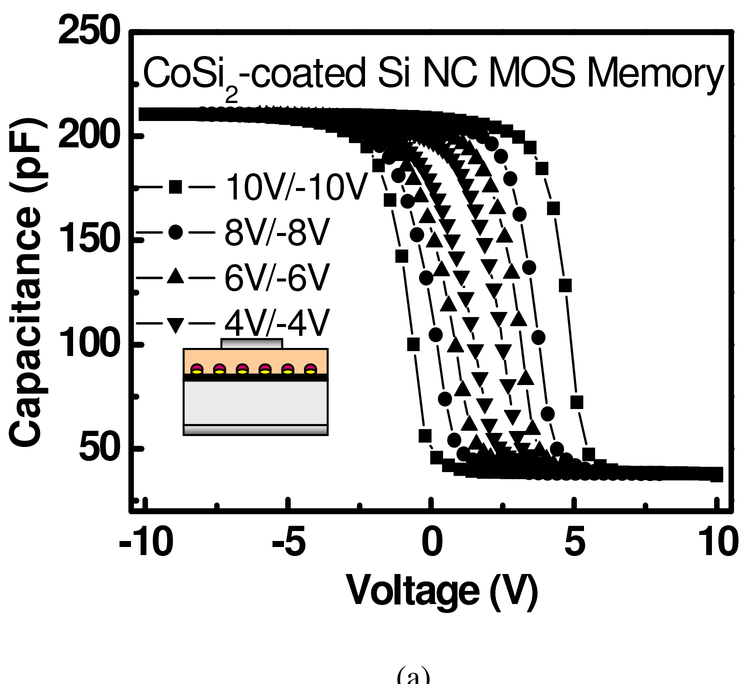


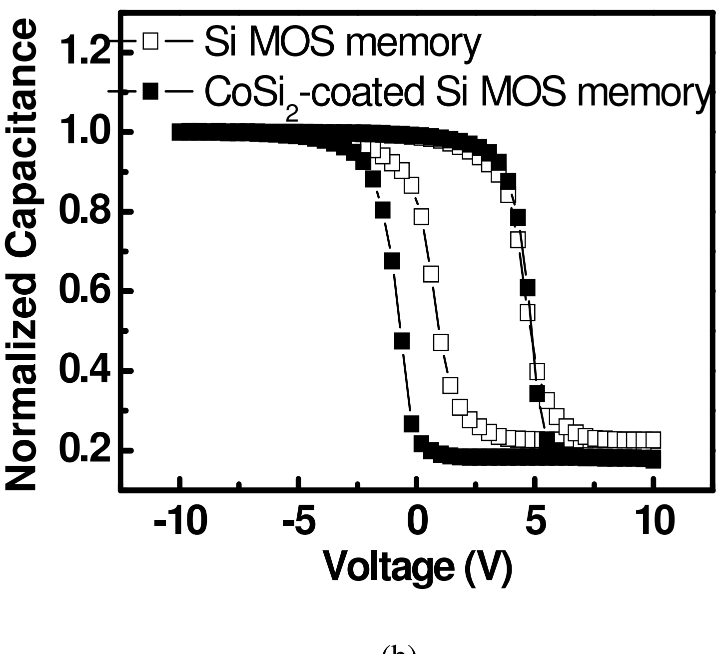
Figure 4-4 EDX spectrum of $CoSi_2$-coated Si nanocrystals. Insets show the SEM images of (a) Si nanocrystals and (b) $CoSi_2$-coated Si nanocrystals.

4.2.3 $CoSi_2$-coated Si nanocrystal MOS memory characterization

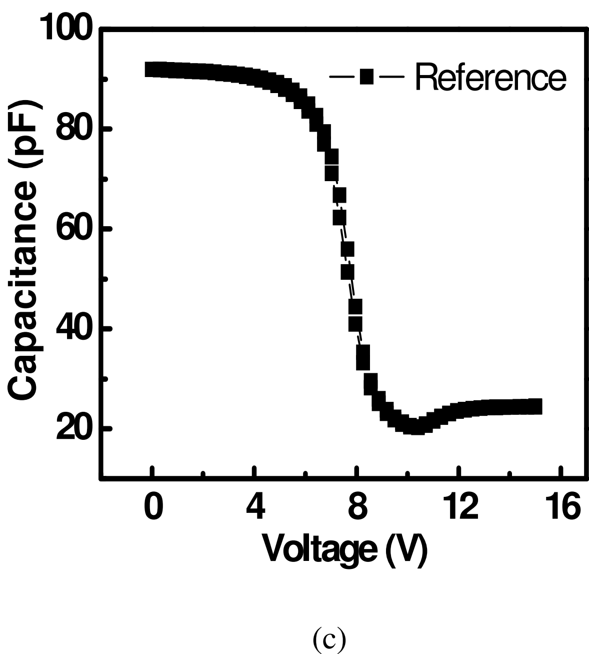
Si nanocrystal and $CoSi_2$-coated Si nanocrystal MOS memories are fabricated and tested. The tunneling oxide and control oxide thickness are 5nm and 20nm, respectively. Figure 4-5(a) shows high frequency (1MHz) capacitance-voltage (C-V) sweep of $CoSi_2$-coated Si nanocrystal MOS memory with different scanning range from ±4V to ±10V. Scanning starts from inversion region to accumulation region and back to inversion region again. Figure 4-5(b) shows the comparison of normalized C-V sweep at ±10V between Si nanocrystal and $CoSi_2$-coated Si nanocrystal MOS memories. A larger memory window is observed from $CoSi_2$-coated Si nanocrystal MOS memory, which is due to the large density of states in the metallic $CoSi_2$. For MOS memory without any nanocrystals, the flat band voltage shift between programming and erasing is negligible, as shown in Figure 4-5 (c).



(a)



(b)

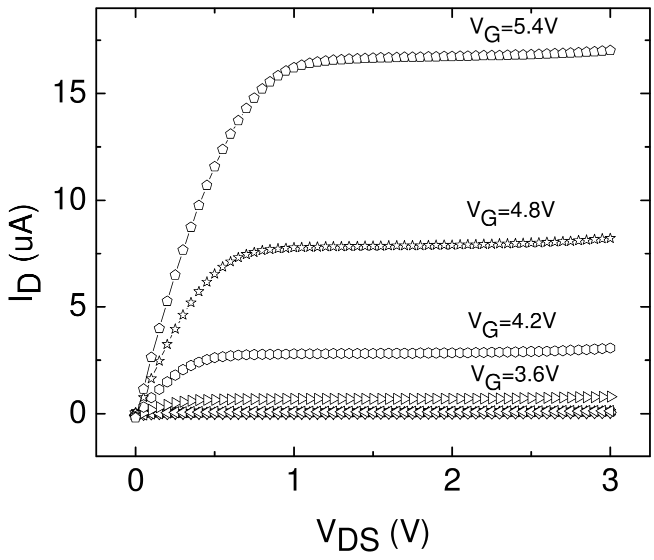


(c)

Figure 4-5 Capacitance-voltage (C-V) sweep of MOS memory with (a) $CoSi_2$-coated Si nanocrystals, (b) C-V comparison between $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories, (c) C-V sweep of MOS reference device, where no nanocrystals were embedded.

4.2.4 $CoSi_2$-coated Si nanocrystal MOSFET memory characterization

Figure 4-6 (a) shows the output characteristics of $CoSi_2$-coated Si nanocrystal MOSFET memory. Typical n-channel MOSFET characteristic is observed. The device tested is of feature size 1μm ×1μm. Figure 4-6 (b) shows the transfer characteristics of $CoSi_2$-coated Si nanocrystal memory. By charging and discharging the device with gate voltage of 12V and -12V for 2 seconds, the device shows a clear threshold voltage shift, which indicates an obvious memory effect.



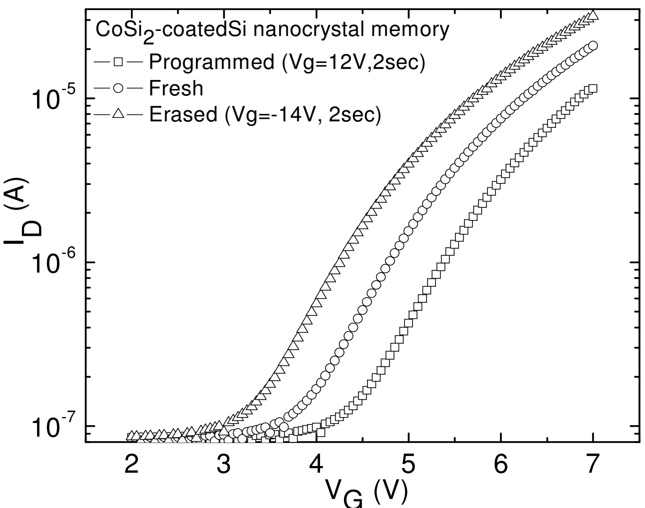


Figure 4-6 Output (a) and transfer (b) characteristics of MOSFET memory with $CoSi_2$-coated Si nanocrystal as floating gate.

Figure 4-7 shows the programming and erasing characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal MOSFET memories. Agilent 81104A Pulse Generator is used to operate the devices and threshold voltage is read from Agilent 4155C Semiconductor Parameter Analyzer. The gate bias of 16V and -16V are used

to program and erase the devices, respectively, and programming and erasing time is accumulated from 2 nano-seconds to 10 seconds. Faster programming/erasing speed is observed in $CoSi_2$-coated Si nanocrystal memory, which can be explained by the stronger coupling between metallic $CoSi_2$ and the channel. $CoSi_2$-coated Si nanocrystal memory also shows a higher level of threshold voltage (V_T) shift saturation, indicating larger storage capability.

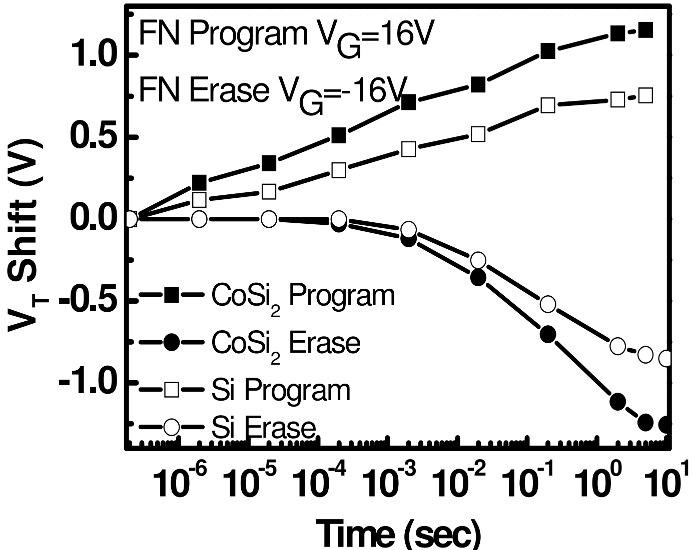


Figure 4-7 Transient programming and erasing characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories.

Figure 4-8 shows the endurance characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories. The programming and erasing conditions are ±16V for 200ms. The memory windows of the two devices stay open up to 10^5 times of operation, although the magnitude shrinks about 25%. The up-shift of the threshold voltage with times of operation is due to the accumulated trapped positive charges in the oxide layer.

Retention characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories are shown in Fig. 4-9. The plot is the remaining charge percentage converted from the V_T shift against waiting time. $CoSi_2$-coated Si nanocrystal memory demonstrates a longer retention time compared to Si nanocrystal memory. This indicates that $CoSi_2$-coated Si nanocrystals indeed re-align their original wide distributed defect-related energy levels around the Fermi-level of the silicide, which is deeper.

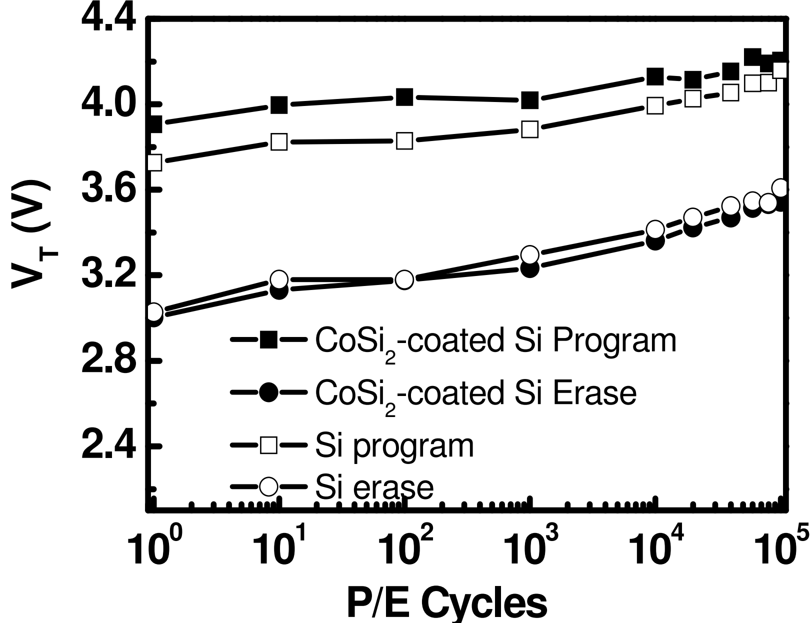


Figure 4-8 Endurance characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories.

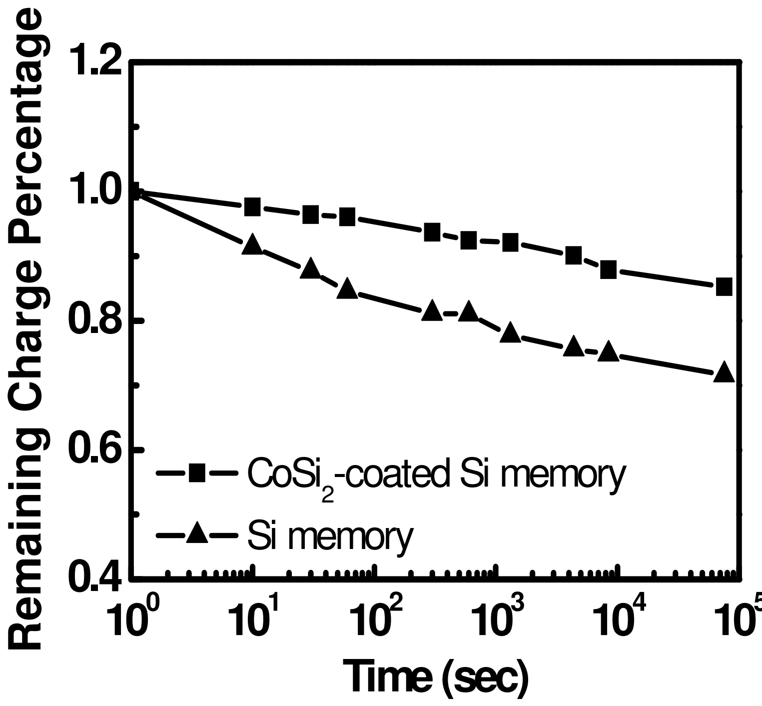


Figure 4-9 Remained charge percentage converted from threshold voltage shift as a function of time.

To prove the discrete nature of $CoSi_2$-coated Si nanocrystals and the capability of local charge storage, hot carrier injection (HCI) was also used to write electrons onto portion of these nanocrystals near the drain side. Programming and erasing characteristics are shown in Figure 4-10. Gate and drain voltage of 7.5V and 5V are used to charge and -10V and 5V are used to discharge the devices. Similar to FN operation, device performance enhancement in $CoSi_2$-coated Si nanocrystal memory is observed in terms of faster programming and larger charge capability. Figure 4-11 shows the retention characteristics comparison between $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories. Longer retention was observed in $CoSi_2$-coated Si nanocrystal memory and the charge loss in $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories are ~20% and ~38%, respectively. The better retention in $CoSi_2$-coated Si nanocrystal memory can be attributed to the primarily charging

around the silicide Fermi-level in stead of the defect levels in Si nanocrystals due to the Fermi-level pinning effect.

Figure 4-12 shows the threshold voltage shift as a function of waiting time after the device was programmed at V_G/V_D=7.5V/5V for 2 seconds. Forward (read from drain) and reverse (read from source) read at different read voltages were used. Because of the local charge storage near the drain side, an additional energy barrier was formed for channel electrons. When the device was read from the drain (forward), this barrier was effectively lowered at larger read drain voltages, leading to different threshold voltage shift. On the other hand, when the device was read from the source (reverse), the source voltage cannot effectively change this barrier, leading to insignificant change of threshold voltage. This result suggests that the device has potential to be used for dual-bit application.

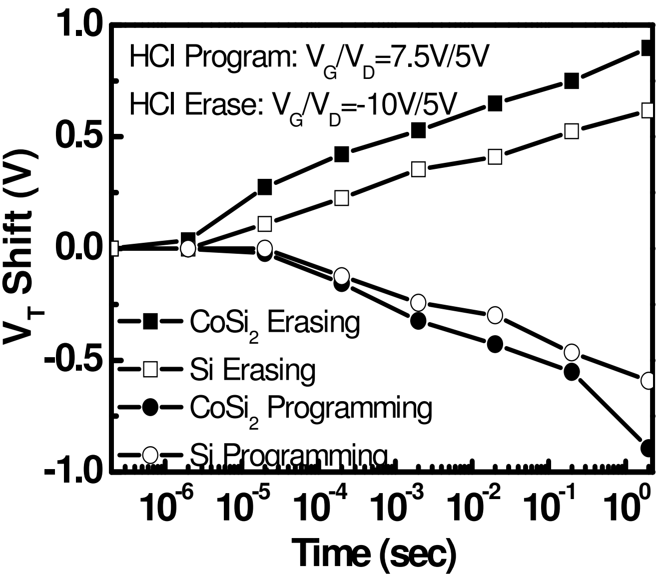


Figure 4-10 Hot-carrier programming and Fowler-Nordheim erasing characteristics of $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories.

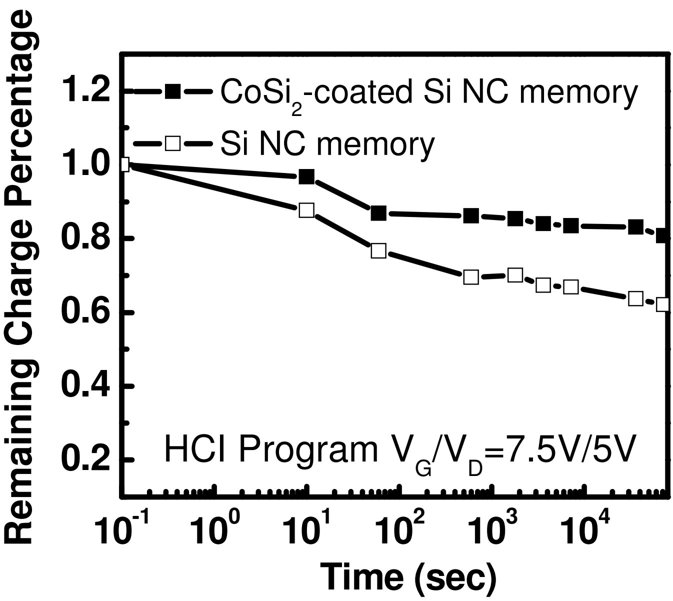


Figure 4-11 Retention characteristics of $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories after HCI programming. The charge loss in $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories are ~20% and ~38%, respectively.

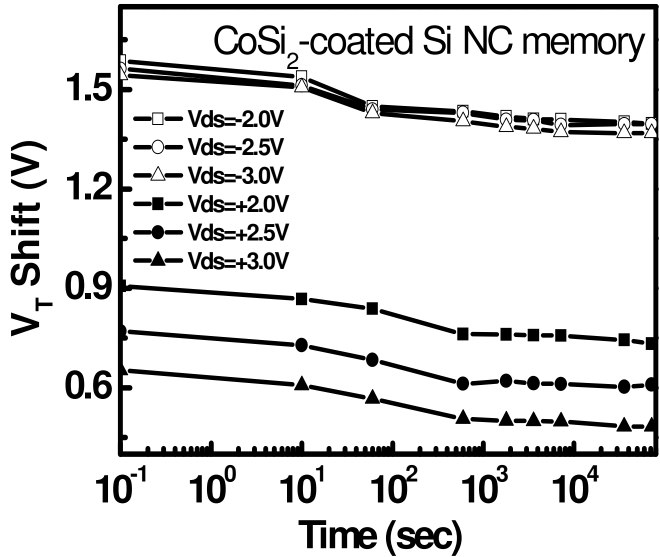


Figure 4-12 Retention characteristics of $CoSi_2$-coated Si nanocrystal memory after HCI programming under forward and reversed read conditions.

4.3 Summary

In summary, MOSFET memory devices with $CoSi_2$-coated Si nanocrystals as floating gates were fabricated and characterized. Memory performances between $CoSi_2$-coated Si nanocrystal memory and Si only nanocrystal memory were compared. Better performance in terms of longer retention time, faster operation speed and larger memory window has been achieved in $CoSi_2$-coated Si nanocrystal memory. The Fermi-level pinning as a result of $CoSi_2$ coating results in the device performance enhancement. The work suggests that the simple silicidation treatment of Si nanocrystals may fundamentally solve non-uniform device operation due to the wide distribution of defect levels in Si nanocrystals and allow Si nanocrystal memory to scale further into next nonvolatile memory generations.

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Chapter 5: VSS $NiSi_2$ nanocrystal memory

5.1 Motivation

In recent years, the growth and device applications of nanowires by vapor-liquid-solid (VLS) method [1-5] and vapor-solid-solid (VSS) method [6-8] attracted extensive attentions. Both methods begin with metal catalyst dots on a substrate in the liquid, and solid form, respectively, depending on different substrate temperature. The introduction of vapor phase precursors changes the nature of these dots from metal to silicide alloy, which acts as effective catalyst. Further introduction of gas molecules results in the growth of nanowires under these catalyst dots. In comparison with these studies on nanowires, little research has been focused on their original stages, i.e., the nucleation catalyst seeds and their potential applications. In this chapter, we report VSS growth of $NiSi_2$ nanocrystals and demonstration of their nonvolatile memories.

The cross section of the device structure and schematic energy diagram of $NiSi_2$ nanocrystal memory are shown in Figure 5-1.

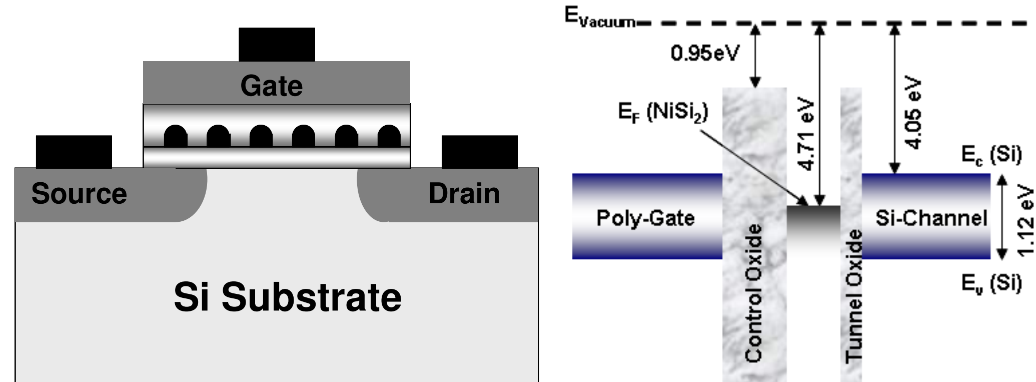


Figure 5-1 Device structure and band diagram of $NiSi_2$ nanocrystal memory.

Memory device operates by sensing the threshold voltage shift under programmed and erased states. Generally, silicide nanocrystals are better than both Si nanocrystals and metal nanocrystals for memory applications. One of the reasons that $NiSi_2$ nanocrystals is better than Si nanocrystals arises from the fact that $NiSi_2$ is metallic material with good thermal stability. The Fermi level of $NiSi_2$ locates ~0.66eV below the conduction band of Si, which means a higher confinement barrier for electrons in comparison with those Si nanocrystals [9]. This is translated into a much longer retention time in the $NiSi_2$ nanocrystal memory. Furthermore, due to metallic nature of $NiSi_2$ nanocrystals, electrical coupling between floating gate and channel is stronger, leading to higher programming/erasing speed. Compared with pure metal nanocrystals for nonvolatile memory applications [10-13], silicide nanocrystals are more thermally stable. $TiSi_2$ [14], $CoSi_2$ [15-16], and NiSi [17] NCs have been synthesized by other methods, which have a common process, i.e., high-temperature annealing. Here, $NiSi_2$ nanocrystals are synthesized by VSS at relatively low temperature of around 600°C for nonvolatile memory applications. Plenty of metals can be used for VSS process to synthesize silicide nanocrystals, therefore work function engineering is possible to optimize memory device performance. The selection of Ni catalyst here is also considered for its full compatibility with Si complementary metal-oxide-semiconductor (CMOS) technology.

5.2. Ni-induced Si growth

Figures 5-2 (a)-(c) show the SEM images of samples grown at 500°C, 600°C and 700°C, respectively. The nominal thickness of the Ni is 0.8nm. The growth time is 10min, and the SiH_4 flow rate is 20sccm at pressure of 500mTorr. At 500°C some

Si NWs grew under the Ni catalysts, but the growth did not take place on each single catalyst, indicating the temperature is not high enough to provide energy for all the Ni nanocrystals to act as the catalyst for Si nanowire growth. At 700°C, nucleation took places on more catalysts, and at some places, nanowires grew rapidly compared to their surrounding nanowires. Also at these places, the nanowires growth was not uni-directional, the side wall growth was clearly seen at the bottom part of the NW. Therefore the temperature window to obtain good $NiSi_2$ nanocrystals falls between 500°C and 700°C. More experiments were done to further narrow and optimize the growth temperature. We found 600°C is the best temperature to balance the density and uniformity. This growth temperature is below $NiSi_2$ eutectic temperature [19], therefore the growth mechanism is VSS.

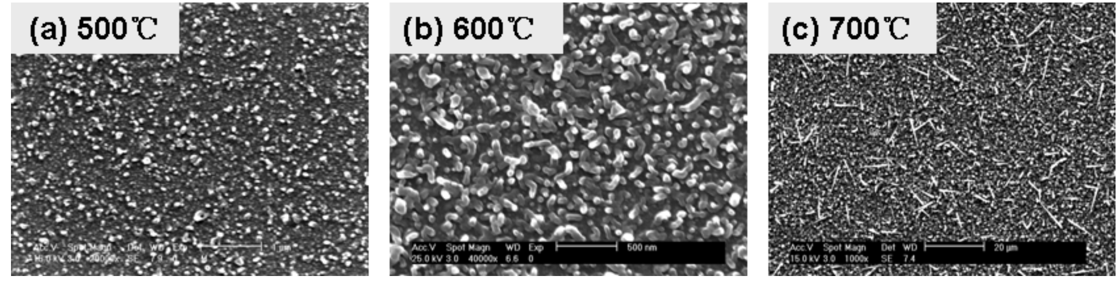


Figure 5-2 SEM images of Ni-catalyzed Si nanowires growth at (a) 500°C, (b) 600°C and (c) 700°C.

Figures 5-3 (a)-(c) show the SEM images of the formation of Si nanowires grown on these substrates covered with different nominal thickness of Ni film. The growth temperature was kept at 600°C with SiH_4 flow rate of 20sccm for 2 minutes. The nanowire density as a result of nominal 0.4nm Ni film as catalysts is relatively low, which is due to insufficient nucleation sites provided by thin Ni film. As the film thickness changes to 0.8nm, not only the nanowire density increases, but also the average size of the nanowires increases. With 1.5nm Ni film, the nanowire size

increases while the nanowire density decreases. As the film thickness is higher than a certain value, the Ni nanocrystal size compromises the nanocrystal density, which is reasonable considering the mass conservation rule. Under these growth conditions, 0.8nm Ni film was found to obtain a good nanocrystal density and size distribution.

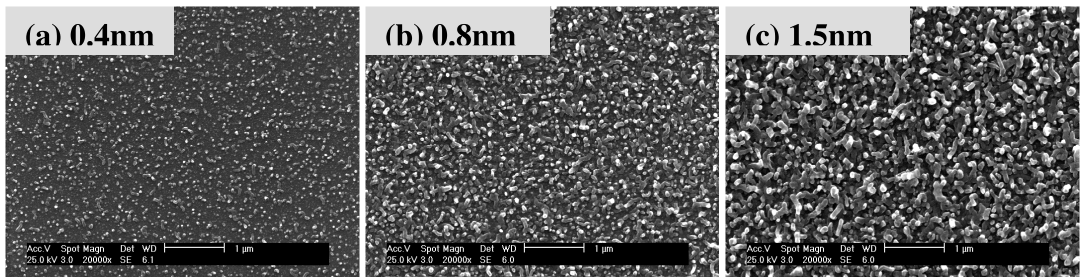


Figure 5-3 SEM images of Ni-catalyzed Si nanowires growth with deposited Ni initial film thickness of (a) 0.4nm, (b) 0.8nm and (c) 1.5nm.

Growth time effect on the formation of $NiSi_2$ nanocrystals and Si nanowires is shown in the SEM images in Fig. 5-4 (a)-(c). Three different durations (5min, 2min, and 15sec) were used to grow Si on 0.8nm Ni film-covered SiO_2 at 600°C. As growth time was shortened from 5 minutes to 2 minutes, the length of the nanowires decreased. As the time decreases further to 15 seconds, there was no nanowire observed in the SEM image, only $NiSi_2$ nanocrystals were found. This time frame of 15 seconds roughly defines the growth time window for the formation of $NiSi_2$ dots before the formation of Si nanowires.

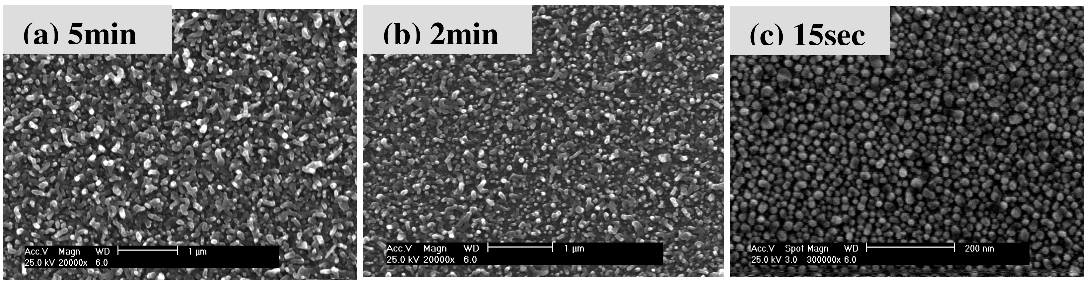


Figure 5-4 SEM images of Ni-catalyzed Si nanowires growth for (a) 5min, (b) 2min, and (c) 15sec.

5.3 $NiSi_2$ nanocrystal and memory device

5.3.1 Device fabrication

The $NiSi_2$ NCs growth and MOSFET memory device fabrication start with a p-Si (100) substrate. Local oxidation of silicon (LOCOS) process was used to electrically isolate devices. Field oxide and nitride were grown sequentially followed by photolithography and reactive ion etching (RIE) to define and expose the active region. A thin oxide of ~5nm was thermally grown at 850℃ for 5min, followed by a brief N_2 in situ annealing at the same temperature to solidify the tunnel oxide. Temescal BJD 1800 ebeam evaporator was used to deposit 1 nm nickel (Ni) film as the catalysts for the formation of silicide dots. After metal deposition, the wafer was immediately transferred to a LPCVD system. The metal film converted to nanoparticles as the furnace heated up to the growth temperature of 600°C, and then SiH_4 gas of 100sccm was introduced and diffused into the nanoparticles, leading to the formation of silicide NCs. The growth temperature is below $NiSi_2$ eutectic temperature [18], therefore the growth mechanism is VSS rather than VLS. The growth time is set to be 15 seconds to avoid nanowire growth. Control oxide of 20nm and polysilicon of 300nm were deposited sequentially followed by source/drain/gate patterning. Phosphorus ion implantation was performed on the poly gate along with the source/drain to obtain the heavily-doped regions. Finally, aluminum was evaporated and patterned as the contact material. The device characterization was carried out by Agilent 4155C semiconductor parameter analyzer to sense the threshold voltage and Agilent 81104A pulse/pattern generator to program/erase the device. The feature size of the device tested in this experiment is 1 μm × 1 μm.

5.3.2 $NiSi_2$ nanocrystal characterization

Figure 5-5 shows a transmission electron microscope (TEM) image of a reference sample under the same process conditions as the metal-oxide-semiconductor field-effect-transistor (MOSFET) memory sample except that the control oxide was adjusted to be slightly thicker, 30 nm, for TEM sampling. The average size of the $NiSi_2$ dots is about 7~10 nm, and they are homogeneous and well separated from each other. The density of the $NiSi_2$ nanocrystals is determined to be ~3×10^{11} cm^{-2}. It should be noted that VSS (VLS) has intrinsic capability to achieve silicide nanocrystals with much higher density > $10^{12}cm^{-2}$, as seen from nanowire research [19], which is critical for future nanvolatile memory applications. We argue that the present study serves as the first try of using VSS method to synthesize silicide nanocrystals for memory applications, therefore the dot density has not been optimized. The effort toward the density optimization is in progress.

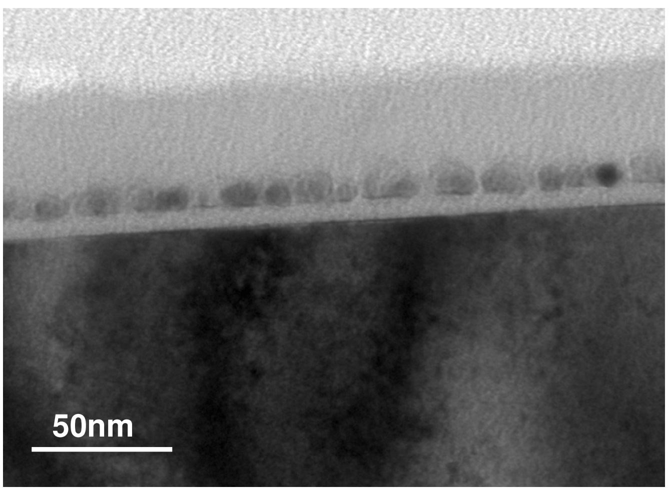
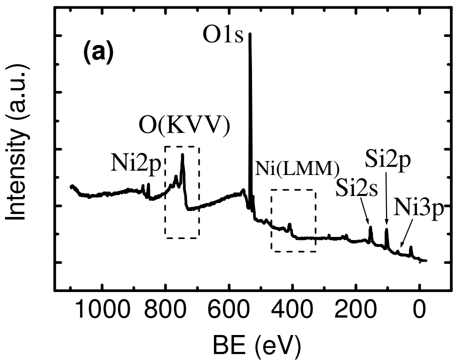


Figure 5-5 TEM image of $NiSi_2$ nanocrystals embedded in a SiO_2 matrix. The size of the nanocrystals is about 7~10 nm.

X-ray photoelectron spectroscopy (XPS) was used to ascertain the chemical composition of the catalyst nanocrystals. Spectra were collected from the nanocrystals

and from a NiSi film (as a standard) using Mg Kα radiation. All spectra were calibrated by assigning the O1s binding energy (BE) to 533.2 eV [20-21]. A survey spectrum collected from the nanocrystals of a reference sample before the control oxide was grown is shown in Fig. 5-6(a) and Fig. 5-6(b) is the high-resolution spectrum of the Ni 2p level. The Ni 2p3/2 and Si 2p3/2 BEs are given in Table I for the nanocrystals, along with values from the literature for Ni metal [22], Ni deposited on Si [23] and two stable silicides, NiSi and $NiSi_2$ [23]. The Ni2p3/2 peak from $NiSi_2$ NCs locates at 855eV, which is slightly higher than that from $NiSi_2$ film (854.3eV) reported in [22]. The binding energy shift in $NiSi_2$ nanocrystals is due to the reduction of screening in excess positive charge being distributed over the nanoparticle surface, increasing the core-level binding energy to a higher value [24-25]. In addition, once the nanocrystal size is very small, the band gap and binding energy increases as the size of the materials decreases [26-28]. Alternatively, selective wet etching experiments using dilute HF as the etchant were carried out. The nickel signal from these samples was very small, confirming the existence of Si in the nanocrystals as metallic Ni is unlikely to be removed by dilute HF.



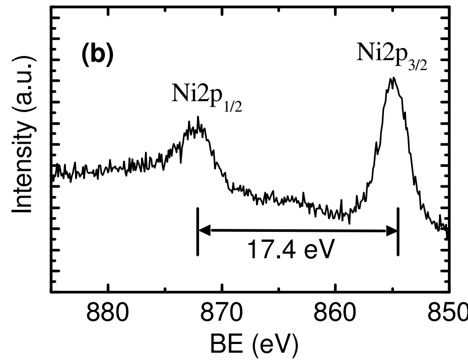


Figure 5-6 (a) XPS survey spectrum of $NiSi_2$ nanocrystals on SiO_2/Si substrate and (b) high-resolution scan of the Ni 2p peaks

5.3.3 $NiSi_2$ nanocrystal MOSFET memory characterization

Figure 5-7 shows the transfer characteristics (I_D-V_G) of the $NiSi_2$ nanocrystal MOSFET memory. FN mechanism, i.e., gate voltages of +18 V for one second and -18 V for one second were applied to program and erase the device, respectively. A threshold voltage shift is clearly observed between programmed and erased states, indicating the charging/discharging effect of the electrons stored on $NiSi_2$ nanocrystals. A memory window of 1.71 V is obtained when using the industry standard of 100 nA drain current to define the threshold voltage. For the control device without nanocrystals embedded, an insignificant threshold voltage shift was found at the same programming voltages for nanocrystal memories, which confirms that the memory effect observed in $NiSi_2$ nanocrystal memory is dominated by the charging effect of the nanocrystals, rather than by defect or interface states.

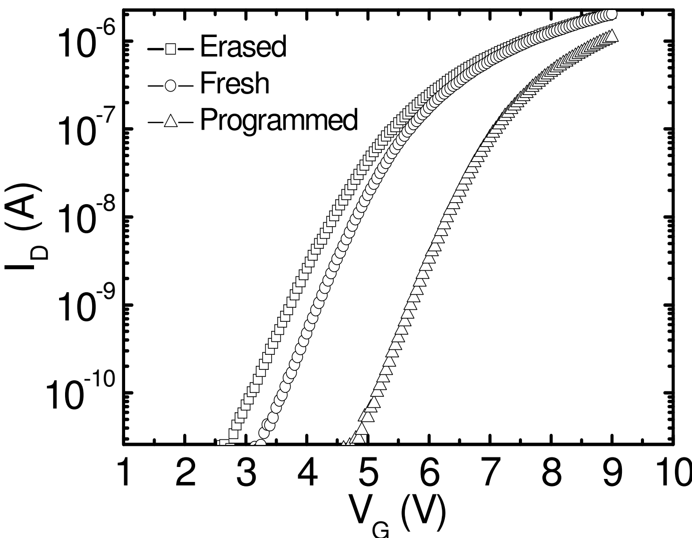


Figure 5-7 Transfer characteristics of $NiSi_2$ nanocrystal MOSFET memory. Three I_D-V_G curves from left to right correspond to programmed, fresh and erased states.

Figure 5-8 shows transient programming and erasing characteristics of $NiSi_2$ nanocrystal memory. The programming and erasing conditions are gate biases of +/- 20 V, respectively. In programming, after one millisecond the threshold voltage shifts 1.68 V from the fresh state, and after one second it shifts 2.2 V and is saturated. In erasing, after one millisecond the threshold voltage shifts 0.56 V towards the fresh state, and after one second it shifts 1.75 V. The erasing process does not shift the threshold voltage back to the initial state because of insufficient erasing of the deeper quantum levels formed with $NiSi_2$.

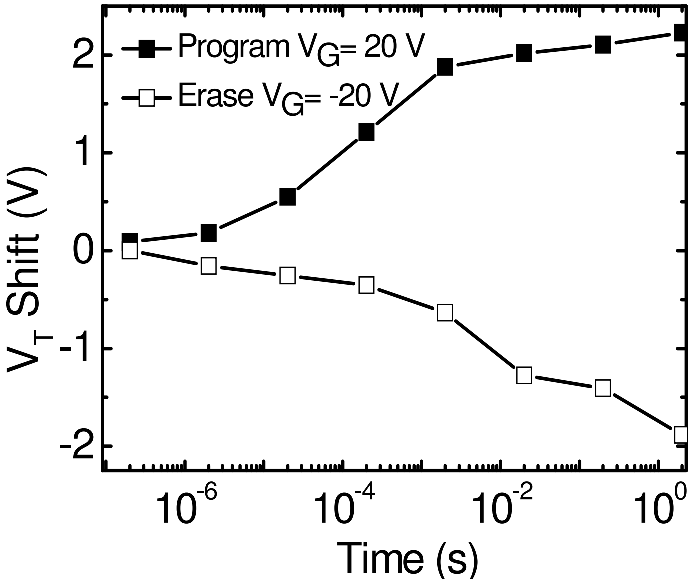


Figure 5-8 Programming and erasing characteristics of $NiSi_2$ nanocrystal memory. Program and erase conditions are V_G=20 V and V_G=-20 V, respectively.

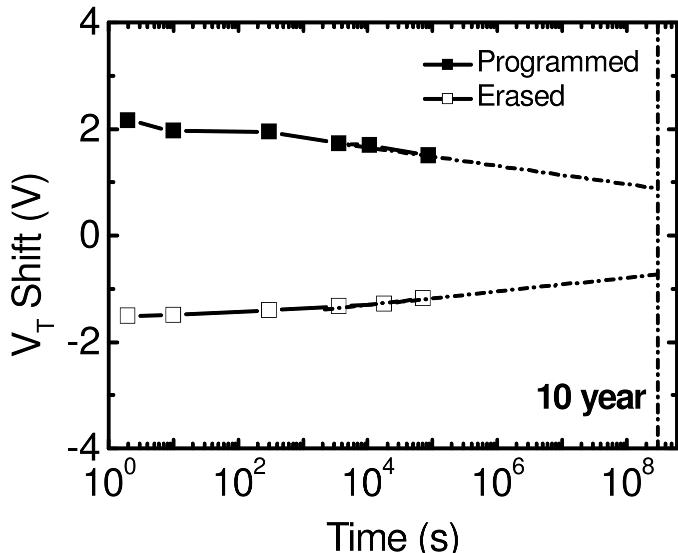


Figure 5-9 Retention characteristics of $NiSi_2$ nanocrystal memory under charged and discharged states. Ten-year retention line is indicated in the figure showing that about 50% of the charge survived after ten years.

Figure 5-9 shows the retention characteristics of $NiSi_2$ nanocrystal memory under programmed and erased states. The device is programmed and erased with gate voltages of +/- 20 V, respectively, for 5 seconds. The data trend is extrapolated, indicating that the memory window of the device still opens fairly widely even after 10 years.

Figure 5-10 shows the transient programming performance of $NiSi_2$ nanocrystal memory under HCI program scheme. HCI was performed by simultaneously biasing the gate and drain, leading to the injection of charges into floating gate around drain side. Through HCI programming, un-even charging of floating gate from source side to drain side is realized, which can be used for two-bit applications. Figure 5-10(a) is the plot with V_D fixed and V_G changed from 8V to 10V and (b) is the plot with V_G

fixed and V_D changed from 3V to 5V. The program time accumulated from nano-seconds to seconds. Both gate and drain biases affect the charging efficiency, i.e., the higher the bias is, the more the charge is injected. This is reasonable as electrons gain higher energy at higher drain voltage and higher gate voltages attract more electrons from channel to the floating gate. Figure 5-10(c) shows the erasing characteristics of an HCI programmed device by biasing a negative gate voltage while keeping source and drain floated. The erasing curve shows similar trend to the one with F-N operation shown in Fig. 5-8 except that the starting point to erase in this case is a partially charged cell while in F-N case, it is a fully and uniformly charged state.

Figure 5-11 shows retention characteristics for HCI programmed and FN erased device. Gate and drain bias of 10V and 4V were used for hot electrons to inject into floating gate around drain side. Gate bias of -20V was used to erase the electrons from the floating gate back to the channel on an HCI charged cell. Programming and erasing time were 5seconds to make sure the fully charged and discharged states. After 15 hours retention, the charges remained at programmed and erased states are 74% and 76%, respectively. Further extrapolation suggests that most of these remaining charges can be still on the floating gate even after 10 years.

Figure 5-12(a) and (b) show the device endurance performance under FN and HCI program scheme, respectively. The memory window stays open at about 77% and 72% of the original window after 10^5 times of programming/erasing operation cycles under FN and HCI program scheme, respectively. This is an indication of good endurance performance. The slight up-shift of the threshold voltage is due to the positive defects charging effect in oxide layer during the operations.

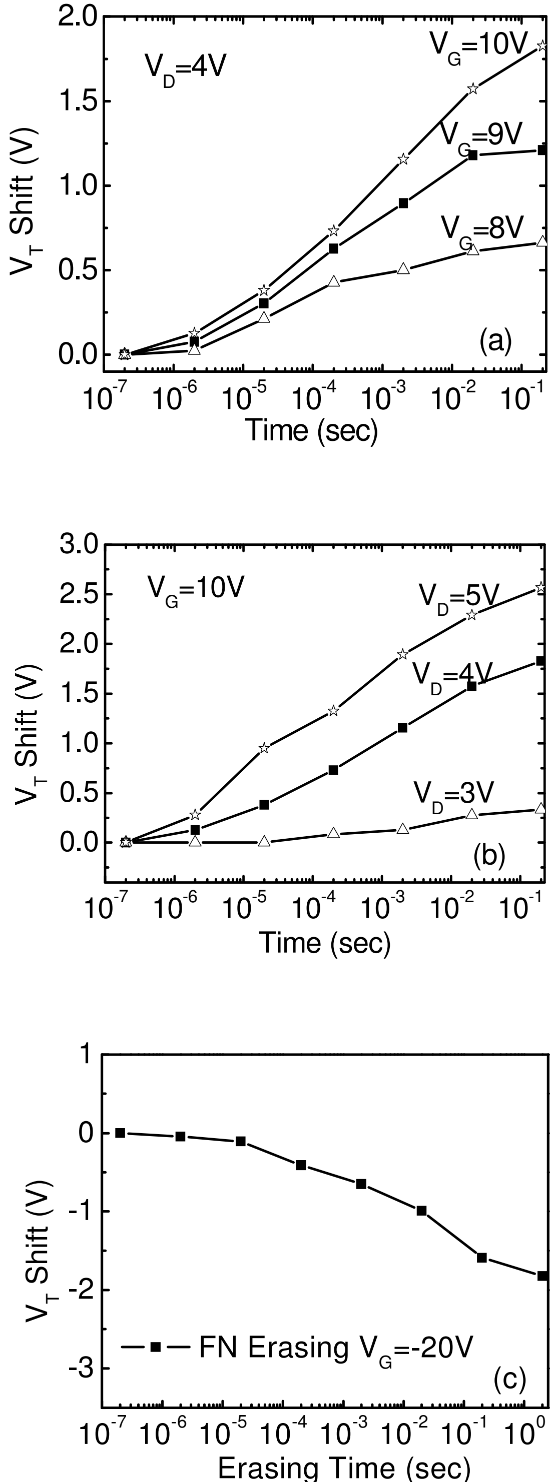


Figure 5-10 (a) HCI transient programming characteristics under fixed drain voltage and various gate voltages, (b) HCI transient programming characteristics under fixed gate voltage and various drain voltages, (c) FN erasing characteristics with V_G=-20V. The cell was programmed through HCI with V_G/V_D=10V/4V.

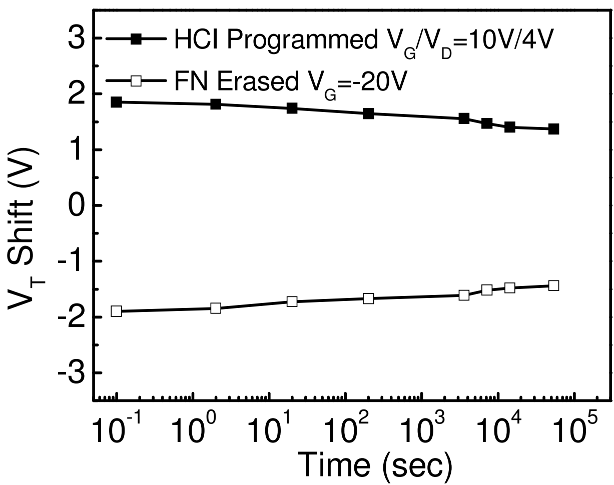


Figure 5-11 Retention performance of $NiSi_2$ nanocrystal memory at HCI programmed and FN erased states.

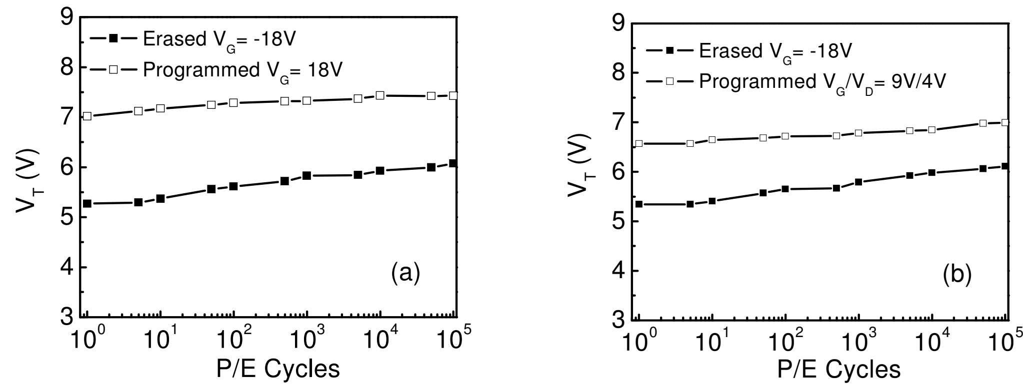


Figure 5-12 (a) Endurance performance of $NiSi_2$ nanocrystal memory under FN operation mode, (b) endurance performance of $NiSi_2$ nanocrystal memory under HCI operation mode.

5.4 Summary

In summary, $NiSi_2$ nanocrystals were synthesized by VSS-growth of Si into Ni catalysts in an LPCVD. MOSFET memory with $NiSi_2$ nanocrystals as the floating gate was fabricated and characterized. Good memory performance, including fast programming/erasing, long retention time, and good endurance was demonstrated. Due to superior thermal stability properties, $NiSi_2$ nanocrystals formed by simple VSS

process may be promising in the future nonvolatile memory technologies. Further optimization of density, size, and uniformity of silicide nanocrystals for nonvolatile memory is in progress.

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Chapter 6: High-density VSS PtSi nanocrystals for memory application

6.1 Motivation

Nonvolatile memory with discrete-trap type storage nodes attracts much attention as a promising candidate for future low power electronics. Si nanocrystal memory, introduced by Tiwari [1], has been investigated tremendously at both academia and industry due to its potential to exceed the performance limits of conventional flash memories in terms of programming/erasing speeds, retention time and endurance. Although superior performance was demonstrated in Si nanocrystal memory, the device reliability remains an issue because of the defect-related charge storage in Si nanocrystals. The traps and defects inside or at the surface of semiconductor nanocrystals play an important role in the experimental observation of long retention times. However, it is difficult to control the trap levels and densities to achieve a consistency in retention because trap formation and annihilation are sensitive to high temperature processes such as source/drain dopant activation annealing. To solve this problem, many other nanocrystals, such as Ge [2], Ge/Si [3], metal [4-6], silicide [7-9], and engineered gate structures [10-12] were proposed and good performance was reported in terms of long retention and proficient programming/erasing.

In this chapter, we report the fabrication and characterization of high-density PtSi nanocrystal MOS memories. PtSi nanocrystals were formed by VSS growth mechanism, where Si precursor was introduced into Pt thin film-covered SiO_2/Si substrate at a sub-eutectic temperature. Traditionally VSS was only used for nanowire research [13-15], however the initial stage of the VSS growth to form silicide dots

before the formation of nanowires can be interesting for memory applications. The advantages of using PtSi nanocrystals as floating gate for memory include easy and simple fabrication procedure, good thermal stability, high storage capability, fast operation, and long retention. These merits play important roles in future scaled memory technologies, for example, long retention time allows thinner tunnel oxide to be used in PtSi nanocrystal memory rather than Si nanocrystal memory to solve the dilemma between retention and operation voltage.

6.2 Device fabrication

The device fabrication starts with a p-Si (100) substrate. Pre-diffusion cleaning was carried out by dipping the wafer sequentially into piranha (H_2SO_4:H_2O_2=4:1), HCl:H_2O_2:H_2O=1:1:4 and diluted HF with intermediate DI water rinse steps. A thin thermal oxide of 3nm was grown on the substrate at 850ºC. A very thin layer of metal catalyst film was deposited by e-beam evaporator on the tunnel oxide at room temperature. Then the wafer was transferred into a LPCVD system for VSS Si growth. Typical growth temperature used in our experiment is 600 ºC, which is much lower than the eutectic temperature of 979 ºC [16] between Pt and Si, indicating that the growth mode is VSS rather than vapor-liquid-solid (VLS). Si growth rate calibration experiments were carried out in order to control the growth time to avoid the growth of Si NWs. After PtSi NCs were formed, control oxide of 20nm was deposited in another LPCVD furnace. Finally Al was evaporated on the front and back of the wafer to be used as contacts of MOS memories.

Figure 6-1 shows energy band diagram of the memory device with Pt nanocrystals as floating gate. The work function of bulk PtSi, 4.9eV [17], is used to

draw the diagram. Therefore, the Fermi level of PtSi is within the band gap of Si and the conduction band offset between PtSi and SiO_2 is 3.95eV, 0.85eV higher than that of Si memory, leading to longer retention time for electron storage.

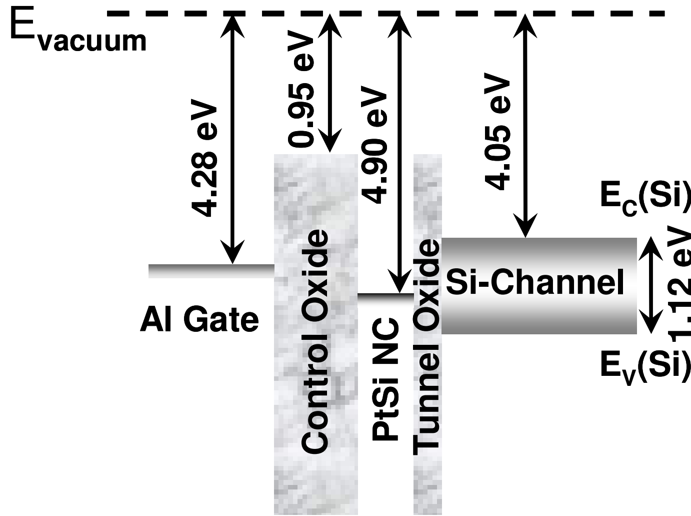

Figure 6-1 Energy band diagram of floating gate memory with PtSi nanocrystals. Deep quantum well of 3.95eV exists between PtSi and SiO_2.

6.3 High-density of PtSi nanocrystals characterization

Figure 6-2 shows the SEM image of PtSi nanocrystals and the inset is the magnified image. The nanocrystal average size and nanocrystals density can be obtained to be 5nm and $1.5\times10^{12}cm^{-2}$, respectively. A reference sample running the same temperature ramping process with the PtSi nanocrystals sample except the introduction of the SiH_4 exhibits Pt nanocrystal average size of about 4nm and the same density as PtSi nanocrystals. The larger size of PtSi nanocrystal confirms the Si growth into Pt catalyst. For VSS growth, temperature, pressure, time, and metal catalyst film thickness all affect the Si growth rate. Figure 6-3 shows the PtSi density and average size dependence on the catalyst film thickness. The growth temperature of 600ºC, SiH_4 pressure of 250mTorr, and growth time of 15seconds were kept the

same for all samples. It can be seen that the nanocrystal average size increases while nanocrystal density decreases with the increase of Pt catalyst thickness. For examples, with Pt thickness of 3nm, the size and density is 37nm and $5.2\times10^{10}cm^{-2}$, respectively; with Pt thickness of 0.2nm, the size and density is 5nm and $1.5\times10^{12}cm^{-2}$, respectively, as shown in Fig. 6-2.

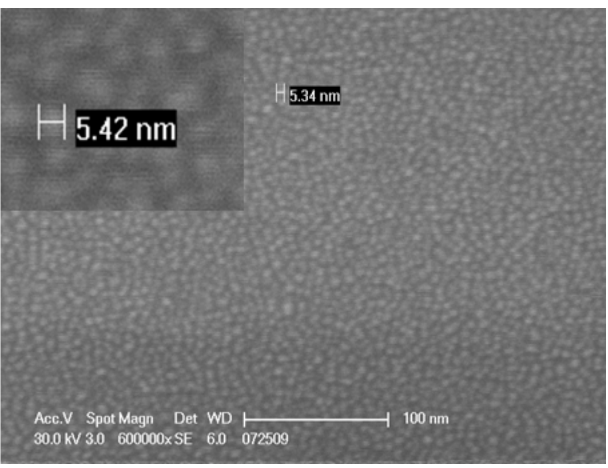

Figure 6-2 SEM image of PtSi nanocrystals on SiO_2/Si substrate and the inset is the magnified image. The density and average size of PtSi nanocrystals is 1.5×10^{12} cm^{-2} and 5nm, respectively.

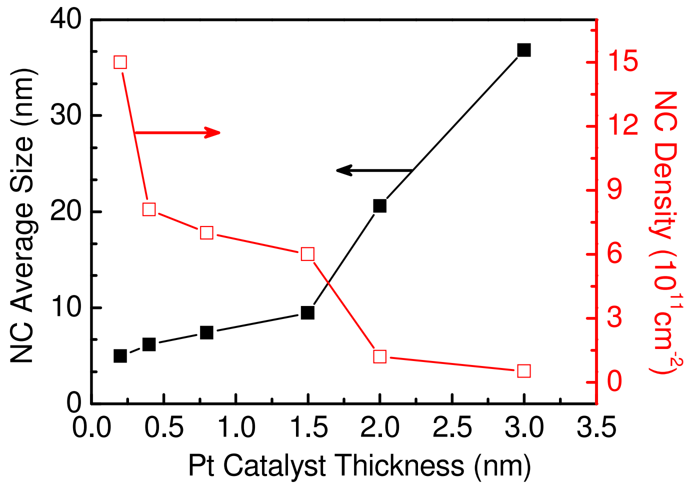

Figure 6-3 PtSi nanocrystal density and average size dependence on the Pt catalyst initial thickness. Nanocrystal density increases while average size decreases with shrinking the Pt thickness.

XPS was used to study the chemical nature of the nanocrystals. Figure 6-4 shows high-resolution XPS data for Pt 4f of the sample with the density of $1.5\times10^{12}cm^{-2}$. The binding energy of Pt 4f was obtained at 73.1eV and 76.4eV [18], indicating the nature of the nanocrystals is PtSi, further confirming the Si diffusion into Pt catalysts to form silicide nanocrystals in addition to the fact of the size increase of PtSi nanocrystals compared to Pt nanocrystals.

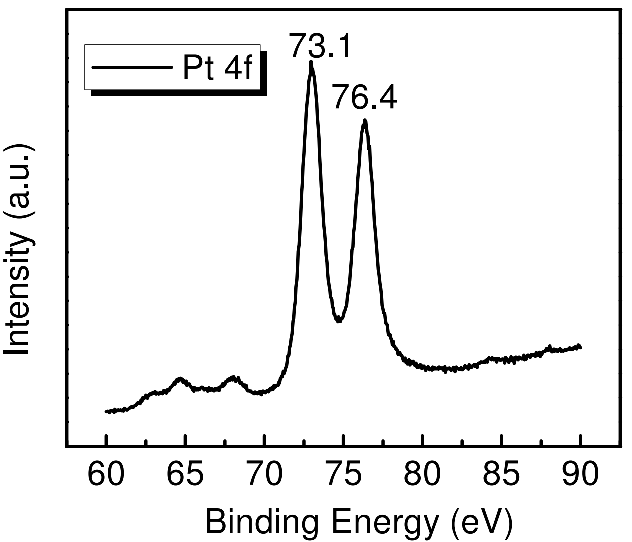

Figure 6-4 XPS result of PtSi nanocrystals on SiO_2/Si substrate and Pt 4f peak position confirms the chemical nature of nanocrystals is PtSi.

6.4 PtSi nanocrystal MOS memory characterization

Figure 6-5 shows the C-V sweep characteristics of PtSi MOS memory sample with the dot density of $1.5\times10^{12}cm^{-2}$. The scanning gate voltage changes from ±2V to ±10V and the observed memory window increases from 0.26V to 8.2V, indicating that the memory effect is due to the nanocrystal storage rather than defect/interface state charging. C-V sweep experiments of a reference sample without nanocrystals between control and tunnel oxide were also carried out and no hysteresis behavior

was found no matter what scanning gate voltage between ±2V and ±10V was used (not shown here). This further confirms the fact that no defect/interface charging contributes to the memory effect, which is observed in PtSi nanocrystal memory.

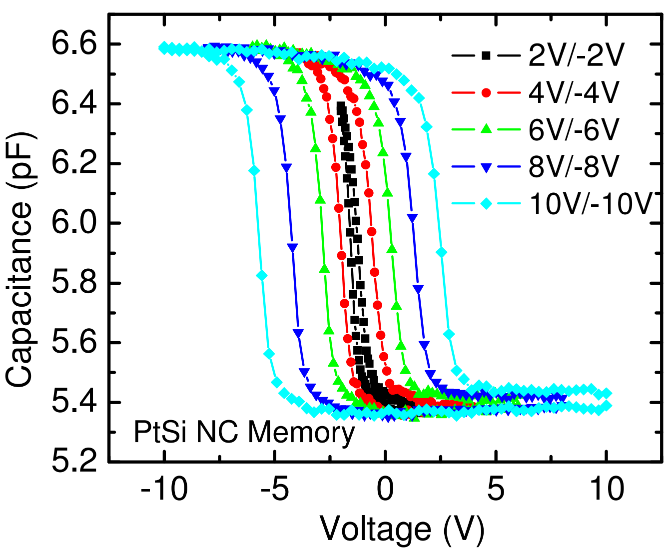

Figure 6-5 C-V sweep of MOS memory device with PtSi nanocrystals under different scanning gate voltage from ±2V to ±10V.

Figure 6-6 shows the dependence of flat band voltage (V_{FB}) shift and number of electrons or holes stored in each nanocrystal on the programming voltage. The writing of electrons was conducted by biasing a positive voltage, while for programming with holes (erasing), a negative bias was applied on the gate. The charges in a single device is calculated from: $Q = \frac{\varepsilon_{SiO_2}}{d_{SiO_2}} \Delta V_{FB}$, where Q is the charges stored in a MOS device, ε_{SiO_2} is the dielectric constant of SiO_2, d_{SiO_2} is the thickness of control oxide, which is 20nm in this work, and ΔV_{FB} is the V_{FB} shift between fresh state and programmed/erased state. The charge number per nanocrystal is calculated from:

$\#/dot = \frac{Q}{D*q}$, where D is the nanocrystal density, which is $1.5\times10^{12}cm^{-2}$ in this work and q is the electron charge. As the programming/erasing voltage increases, the threshold voltage shift and stored charges increase until saturated.

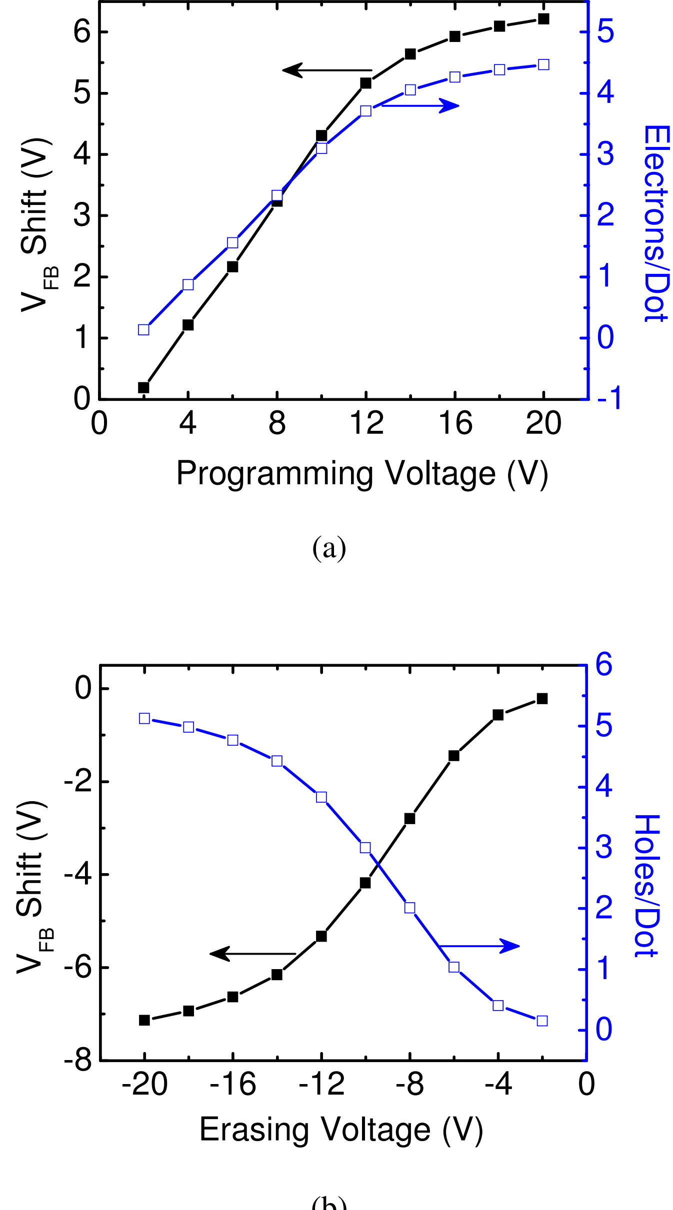

Figure 6-6 Plots of flatband voltage shift and corresponding electrons (a) and holes (b) per nanocrystal as a function of programming/erasing voltage.

Figure 6-7 shows retention characteristics of PtSi nanocrystal memory at programmed and erased states, respectively. The programming and erasing conditions are gate voltage of 10V/5sec and -10V/5sec, respectively. After programming, transient capacitance at the same read voltage is recorded intermittently. After 10^5 seconds, the charges remained in the nanocrystals at both programmed and erased states are about 70%, which is reasonable for a tunnel oxide of 3nm.

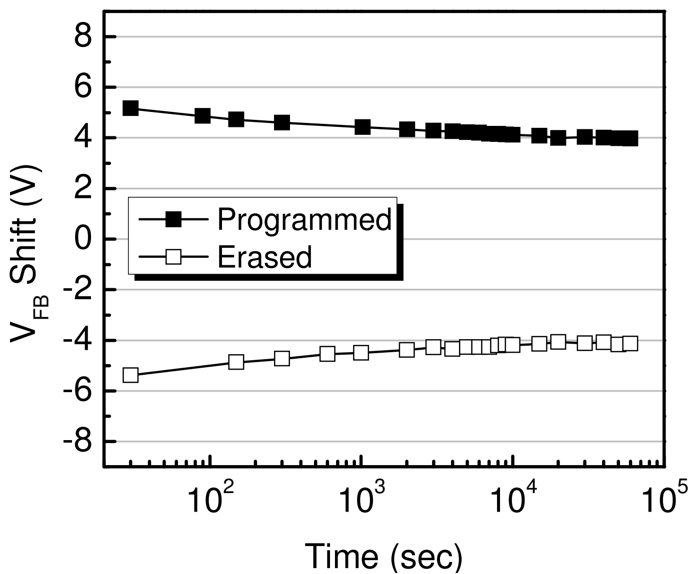

Figure 6-7 Retention characteristics of PtSi nanocrystal memory at programmed and erased states.

Endurance characteristics of PtSi nanocrystal memory is shown in Figure 6-8. Two sets of programming/erasing conditions, ±6V and ±10V, were used to measure the cycling performance. It is found that up to 10^5 times of operations, the memory window, i.e. V_{FB} difference between programmed and erased states, shows insignificant change for both sets of operation.

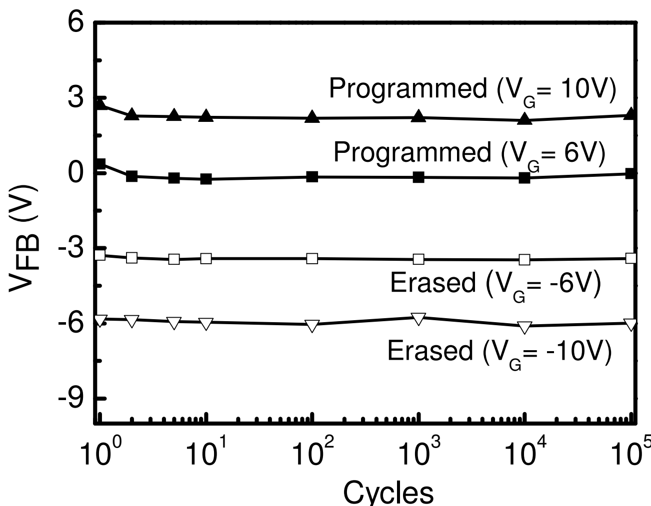

Figure 6-8 Endurance performance of PtSi nanocrystal memory

6.5 Summary

In summary, VSS mechanism was used to synthesize PtSi nanocrystals with high density and small size. The PtSi nanocrystal density can be easily tuned by adjusting the catalyst film thickness. MOS memory with PtSi nanocrystals embedded in SiO_2 was fabricated and characterized. Large memory window, long retention time, and good endurance performance were demonstrated in PtSi nanocrystal memory.

6.6 References

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Chapter 7: Conclusion

Nonvolatile memory devices with Si nanocrystals, Ge/Si heteronanocrystals, $CoSi_2$-coated Si nanocrystals and VSS-induced $NiSi_2$ and high density PtSi nanocrystals have been proposed and investigated. Standard MOSFET processes were used to fabricate these nanocrystal memory devices. Memory device performances were measured including memory window, transient programming/erasing, retention time and endurance characteristics. To operate these memory devices, both FN tunneling and HCI programming schemes were employed to demonstrate potential of the devices for NAND and NOR applications.

Ge/Si core/shell like heteronanocrystals were grown by LPCVD via self-assembly of Ge on Si. Growth parameters were tuned to achieve well self-aligned heteronanocrystal with dot density of $5\times10^{11}cm^{-2}$ and average dot size of 7nm. Experimental results of p-MOSFET Si nanocrystal and Ge/Si heteronanocrystal memories are described in Chapter 3. Longer retention time was observed in Ge/Si heteronanocrystal memory because of the artificially-created quantum well at Ge valance band for long time holes storage. In addition to hole storage, electron charging characteristics were also investigated in Ge/Si heteronanocrystal memory since there exists a quantum well at Si conduction band for electron storage.

In addition to hetero-semiconductor nanocrystal memory, we also developed slicide-based nanocrystal memory in order to achieve large storage capacity, fast operation speed and good retention performance. Three types of silcides were investigated in this thesis work, $CoSi_2$-coated Si nanocrystal, VSS-induced $NiSi_2$

nancorystal and VSS-induced high density PtSi nanocrystal and their experimental results are discussed in Chapter 4, 5 and 6, respectively.

For $CoSi_2$-coated Si nanocrystals formation, standard silicidation process was utilized by running twice thermal annealing with selective metal etching in between. Both n-MOS and n-MOSFET memories with Si nanocrystals and $CoSi_2$-coated Si nancorystals were fabricated simultaneously to compare their performances and demonstrate the improved device characteristics in silicide-based nanocrystal memory. Longer retention time, faster programming speed and comparable endurance performance were observed in $CoSi_2$-coated Si nanocrystal memory compared to Si only nanocrystal memory. The Fermi level pinning effect by $CoSi_2$ nanocrystals explains the enhanced device performance.

The highest process temperature involved in forming $CoSi_2$-coated Si nanocrystals is around 850ºC. To lower this thermal budget, VSS method was first introduced to synthesize $NiSi_2$ and PtSi nanocrystals. VSS is similar to VLS and generally used for nanowires growth. By controlling the growth time and shutting off the Si growth precursor before Si nanowires growth takes place, it should be grown silicide nanocrystals only. Growth parameters, such as growth time, growth temperature, catalyst initial thickness effects were investigated for the purpose of finding right condition for silicide nanocrystals formation only. The major advantage of this method over silicidation methods is the lower thermal budget because VSS growth happens at sub-eutectic temperature. From our experiments, both $NiSi_2$ and PtSi can be synthesized at 500ºC-600ºC, at least 250ºC lower than that used for $CoSi_2$ formation. Good memory performances were achieved in both $NiSi_2$ and PtSi memory devices. Among all the nanocrystals fabricated in this thesis work, PtSi nanocrystals

show the highest dot density, $1.5\times10^{12}cm^{-2}$ and tightest size distribution, which is about 5nm. High density nancorystals are necessary for the future scaled memory device because it minimizes the performance variation from one device to another.

In summary, from all the four devices shown in this thesis, we believe that using high-density silicide nanocrystals is very promising in achieving the performance superior to both conventional flash and Si nanocrystal memory.