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Time Domain Interference Cancellation for Cognitive Radios and Future Wireless Systems

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Time Domain Interference Cancellation for Cognitive Radios and Future Wireless Systems

By

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Abstract

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The discrepancy between perceived spectrum shortage and the actual availability by measurements motivates the use of cognitive radio concepts. In this approach the radio locates and then transmits in unused or lightly used bands. If a wideband digital approach (on the order of GHz) to channel selection is taken to provide the necessary radio flexibility, there is a stringent dynamic range and speed requirement in the analog to digital conversion process. This arises from the large interfering signals which are effectively in-band since they are not removed by analog pre-filters. Given this extremely challenging wideband dynamic range goal, a fundamentally different mixed signal architecture has been pursued which is based on time domain signal cancellation. The objective of this thesis is therefore to analyze and implement critical aspects of this approach, with particular focus on the power requirements and silicon area.

This approach explores the use of a mixed analog with digital assistance architecture which uses multiple low to medium resolution ADCs with digital adaptive filters. The effective dynamic range of the front-end is enhanced by cancelling the unwanted interference in the time domain.

Interference cancellation performance is improved using oversampling and a digital dual adaptive signal processing technique that provides a low mean squared error for cancellation together with a large processing gain. The system could achieve at least 11 bit equivalent dynamic range for the desired weak signals using two 5-bit ADC's and a 7-bit DAC. In general, the Effective Bits from Dynamic Range Reduction (EBDR) for the system is equal to, or more than N+M bits, where N and M are resolutions of the two ADC's used.

The key components of the system are high speed medium resolution ADC's and they have been implemented to demonstrate the path to a low power small area solution. An asynchronous 1GS/s ADC with a peak SNDR of 31.5*dB*, ENOB 5.0 bits, is achieved by time interleaving two

ADC's based on the binary equivalent successive approximation (SA) algorithm using a series capacitive ladder with input capacitance of 84*fF*. A simple extension of the SA algorithm essentially removes the ENOB degradation due to metastability from the comparator. The ADC's are fabricated in 65nm CMOS with an active area of $0.11mm^2$, with a total power consumption of 6.7mW.

It is believed that the time domain approach for wideband, high dynamic range applications which has been explored in this thesis is a step towards the goal of a future radio system, in which the A/D conversion process is directly after the front-end low noise amplifiers.

To my dear parents

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Chapter 1

Introduction

1.1 Motivation

1.1.1 Concept of Cognitive Radio

Through the years, the Federal Communication Commission (FCC) managed the spectrum allocations on a request-by-request basis, usually specifying the applications (TV broadcast, phone service, public safety, etc.) and technology that a licensee could use in its sliver of spectrum. However in the past few years, the FCC has realized that there is a need for change. It basically had no more spectra to allocate, yet the demand for new uses—primarily data—was accelerating.

Action has been set aside to take a continuous 7 gigahertz (GHz) of spectrum between 57 and 64GHz for wireless communications. In addition to frequency re-use, 60GHz band has the unique characteristics that make possible many other benefits, including high-data rates, excellent immunity to interference (due to short transmission distance), narrow antenna beam width and limited use of 60GHz spectrum. Yet the applications in millimeter wave regime typically have severe power and cost constraints.

Fig. 1-1 FCC Allocation Chart. a) 300MHz to 1GHz. b) 1GHz to 3GHz. c) 3GHz to 6GHz.

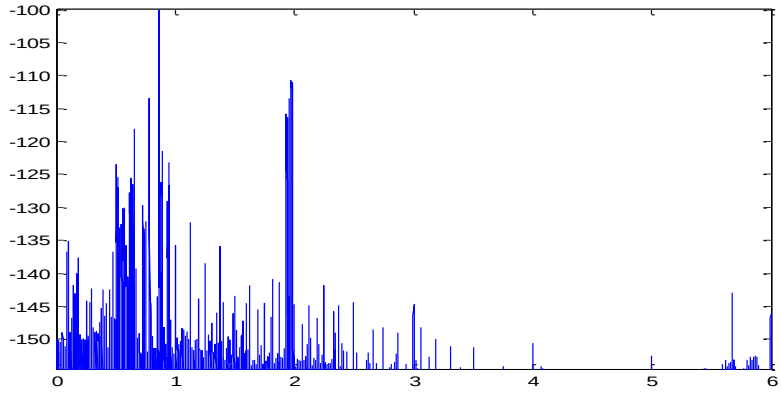


Fig. 1-2 A snapshot of the spectrum utilization up to 6 GHz in an urban area [1].

In the frequency bands, especially at those that can be economically used for wireless communications (e.g. spectra below 6GHz), there still seems to be a crisis of spectrum availability from the FCC allocation map (Fig. 1-1). However, measurements have shown that much of the spectrum allocated over the years was being grossly underused as seen by the snapshot of spectrum usage in an urban area (Fig. 1-2).

In the figure, there is very little usage at the time, place and direction that this measurement was taken. Analysis of the snapshot in Fig. 1-2 reveals that the actual utilization in the 3-4 GHz frequency band is 0.25% and drops to 0.13% in the 4-5 GHz band. Even in the most crowded bands, such as below 2GHz, the utilization is less than 50% (Tab. 1-1).

Frequency (Hz)	0~1G	1~2G	2~3G	3~4G	4~5G	5~6G
Percentage (%)	54.4	35.1	7.6	0.25	0.128	4.6

Tab. 1-1 Usage percentage of spectrum in an urban area.

1.1.1.1 Concept of Cognitive Radio

It is this discrepancy between FCC allocations and actual usage indicates that a new approach to spectrum licensing is needed. Extensions of the unlicensed usage to other spectral bands, while accommodating the present users who have legacy rights, are desired. With the explosive growth of the wireless services offered in the past few years, the demand for opportunistic sharing of the spectrum becomes stronger each day. With software defined radio a reality today, transition to the more intelligent or "cognitive" counterparts, which can give users the ability to adapt to the real time spectrum conditions, is not a very distant dream.

An approach, which can meet this goal, is to develop a radio that is able to sense the spectral environment over the wide available bands, use the spectrum and transmit only if communication does not interfere with licensed users [2]. According to Institute of Electrical and Electronic Engineers (IEEE), the cognitive radio is a radio transmitter/receiver that is designed to intelligently detect whether a particular segment of the radio spectrum is currently in use and to jump into (or out of) the temporarily-unused spectrum very rapidly without interfering with the transmissions of other existing users. These un-licensed low priority secondary users (SU) using Cognitive Radio (CR) techniques ensure non-interfering coexistence with higher priority users (PU) and thus reduce concerns of a general allocation to unlicensed use [3].

In the environment, where the SU co-existed with the PU, the CR transmitters would have to clear the corresponding band, giving priority to the licensed owner when licensed owner appears in a frequency band. There are two principle possibilities for a licensed owner to access spectrum [4]:

1. It searches for free frequencies within the licensed frequency range. The licensed owner has the right to reclaim frequencies from SU's who are operating within that band. This

approach requires the licensed owner to be able to detect SU's and probably even to communicate with them. There is an underlying assumption that the licensed owner does not necessarily need to use of all the controlled spectra and is willing to share them under certain constraints.

2. In the second approach, the licensed owner has no knowledge about SU's. Consequently it just claims some frequency within its frequency band forcing a SU to change to other unoccupied frequencies.

Based on the first approach, a control channel could be established, using dedicated logical channels for the exchange of control and sensing information. There are two different kinds of envisioned logical control channels, a Universal Control Channel (UCC) and Group Control Channels (GCCs). The UCC is globally unique and has to be known to every CR a priori. Without the knowledge of that control channel, a CR has no communication possibilities. The main purpose of the UCC is to announce existing groups and enable newly arriving users to join a group. In addition to the UCC, each group has one logical GCC for the exchange of group control information. These control channels might be located in some licensed spectrum specifically reserved for this purpose, e.g. in one of the ISM bands or UWB (Ultra Wide Band) [2]. The control channels know information about the PU's as a prior, in term of frequency, modulation, power level and etc.

The second approach usually involves a more dedicated sensing mechanism for the SU's, which facilitates a prompt switching out of the licensed owner band. The control channel will therefore exchange the information between the transmitter and receiver of the SU's for the consecutive operation frequency, modulation, etc. when the PU claim its frequency back. This requires the SU to monitor multiple available frequencies or store information from multi-SU's to enable cooperative operation.

The design of the CR systems involves the mechanism of sensing, transmitting and receiving. The information sharing through the control channel, which is mentioned as a licensed spectrum, is to improve the overall CR throughput and reduce the interfering to the PU's.

1.1.1.2 Uniqueness of Cognitive Radio Systems

To design the CR receiver, it is crucial to understand the special characteristics of the CR systems. First and most important, the sensing and transmission function of CR must be performed over the widest possible bandwidth to provide the maximum flexibility and to give the highest probability of detecting unused spectra. Yet more interfering signals will be present as the bandwidth of interest is extended. The possibility of facing more in-band interferes significantly increases. Due to these strong PU's, the dynamic range requirement of the receiver front-end increases dramatically.

The unique sensing function of Cognitive Radios therefore forces the receiver to provide wideband signal reception, from the antenna to the analog-to-digital converter (ADC) which requires a GHz sample rate if GHz bandwidths are to be exploited.

The new challenges of Cognitive Radios put a stringent requirement on RF sensitivity for received signals and the ability to detect different desired signal types and power levels. Measurements have been taken using a directional antenna (TEM horn) at multiple typical environments (Fig. 1-3, Fig. 1-4, Fig. 1-5). It is observed that, at the CR receivers, even when it is only desired to detect the CR signals at a power level that is a few *dB*, e.g. with SNR = 10*dB*, above the noise floor (-158*dB*/Hz @ 300K), the interference created by the PU's yields signal to interference (SIR) ratios ranging downwards to -70*dB*. This results in a large dynamic range requirement for the front-ends circuitry and in particular for the ADC which must accommodate the large interfering signals while still provides sufficient quantization performance for the weak CR signals.

Though the interfering signals are in-band, they are not desired. The wideband sensing needs a multi-GHz speed ADC, which together with a high resolution requirement (of 12-bit or more) might make the design infeasible. Therefore, reducing the strong in-band PU signals, which are of no interest to detect, is necessary and important to receive and process the weak signals.

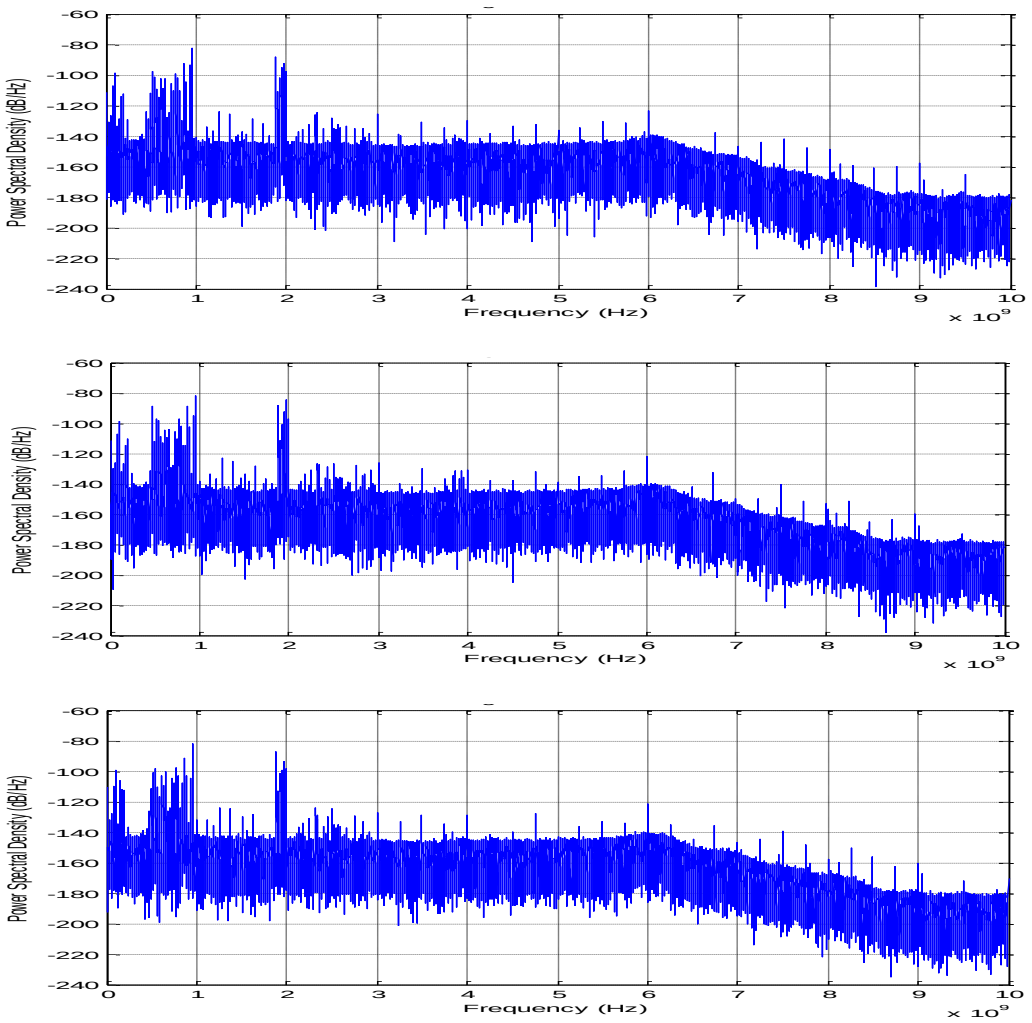


Fig. 1-3 Dirty Maps of indoor interference at positions with equal probability of inside and outside interferers.

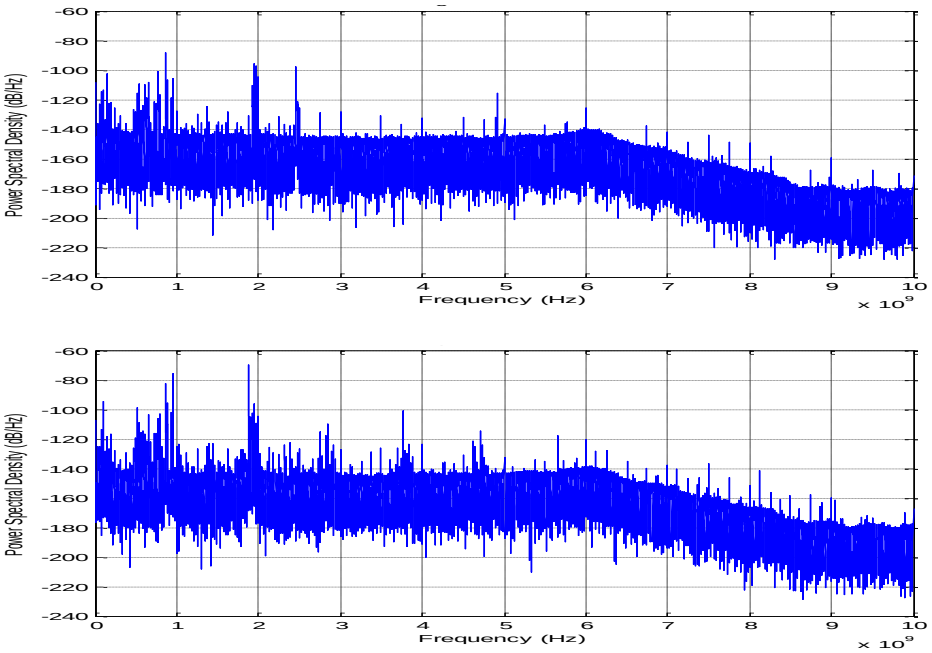


Fig. 1-4 Dirty Maps of interference next to a wireless LAN transmitter.

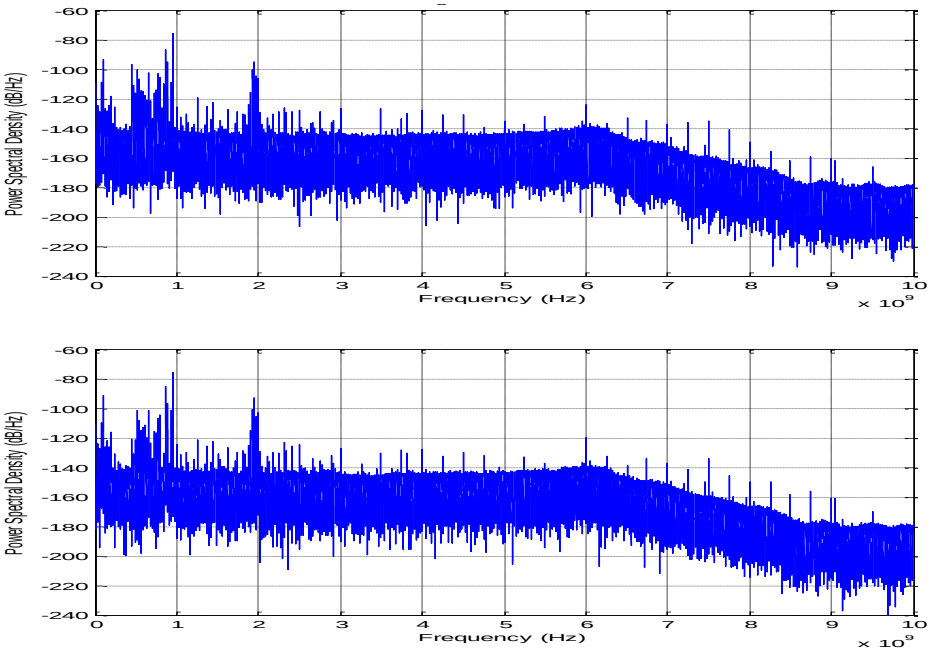


Fig. 1-5 Dirty maps of interference in a lab station.

1.1.2 Future Wideband Radio Systems

Traditional radio front-end includes multiple analog components. For instance, the receiver generally has a bandpass RF-filter, low noise amplifier (LNA), gain stage, mixer, low pass filter (LPF) and the ADC (Fig. 1-6). The received signal preserves in the presence of analog waveform, until it is been converted by the ADC into digital format.

With the technology scaling into ultra-deep-submicron, the cost of the digital logic is significantly lowered, and there is a great incentive to implement high-volume baseband signal processing in the most advanced process technology available. Concurrently, observed that the scaling adversely affects most other parameters relevant to analog designs, there is more incentive to move the lion's share of processing from analog to digital to avoid the difficulties in analog design and achieve the lower-power enhanced-flexibility goal for the wireless systems.

Eventually, an alternative structure needs to be provided that contains fewer portions of analog front-end components (Fig. 1-7). Majority of the filtering, amplification etc. are to be implemented with the lower cost digital circuits. However, achieving high linearity, high sampling speed, high dynamic range, with low supply voltages and low power dissipation in the scaled CMOS technology becomes a major challenge for the ADC's.

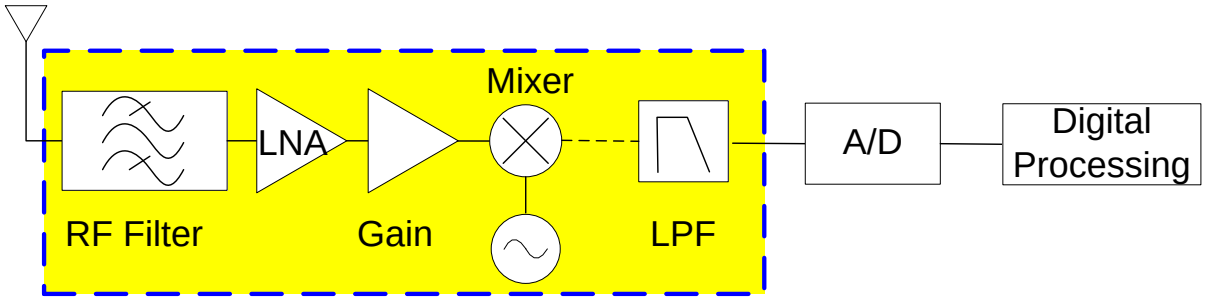


Fig. 1-6 Traditional radio front-end.

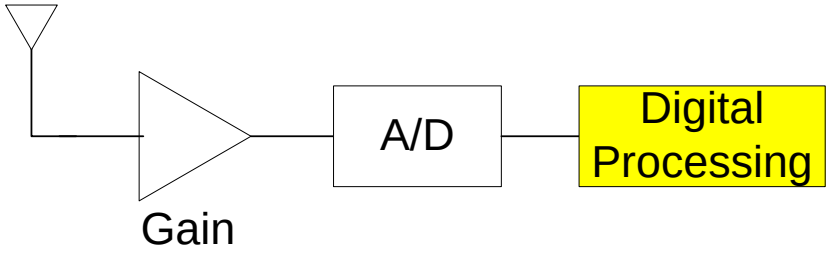


Fig. 1-7 Conceptual illustration for future radio front-end.

1.2 Approaches for Interference Cancellation

The key problem is how to enhance the dynamic range achievable by the mixed-signal circuits. For high-resolution converters, this inevitably leads to an increase of power consumption to maintain SNR that is set by the non-desirable interferes.

Our approach to resolve the high speed, high dynamic range problem for the CR receiver and future radio system involves active cancellation, because in the situation in which the dynamic range is high (interfering signal is extremely strong), it is possible to provide an active-cancelling signal before the A/D conversion process.

There is an interesting analogy between our approach and the information theoretic analysis of the interference channel [5]. It has been shown that very strong interference is almost innocuous as no interference at all. This comes from the fact that if the interfering signal has a high signal to noise ratio compared to the signal of interest, it can be accurately reconstructed, even treating the signal of interest as noise, and then subtracted off [6].

There are sufficient works to mitigate interference using sophisticated digital processing. But for the challenge presented in Section 1.1 , it is obvious that all the interference cancellation are required and limited to be implemented in analog domain, because the signal hasn't been quantized by and converted by ADC yet.

1.2.1 Frequency Domain Cancellation

By more aggressively reusing frequencies within a cluster of radio coverage cells, system operators increase the aggregate number of users that can be supported but such gains come at the expense of increased mutual interference between users, e.g. increased co-channel and adjacent channel interference between users.

As such, adequate cancellation of interference poses challenges for the interference canceling receiver. Because the conventional approaches to interference cancellation, suppression, etc., are based on frequency filters that creates large amount of attenuation over the specified band of frequencies, reducing the unwanted interference to a tolerable level while passing the desired frequency range with minimum attenuation.

High Q factor, wide tuning range (~GHz), fast tuning filter designs (Fig. 1-8) require either high power consumption filter banks, or MEMS designs [7] that are much less flexible.

1.2.2 Spatial Domain Cancellation

Acceptable communication receiver performance depends on more than just the ability to adequately suppress adjacent channel interference. Other phenomena (such as time-varying

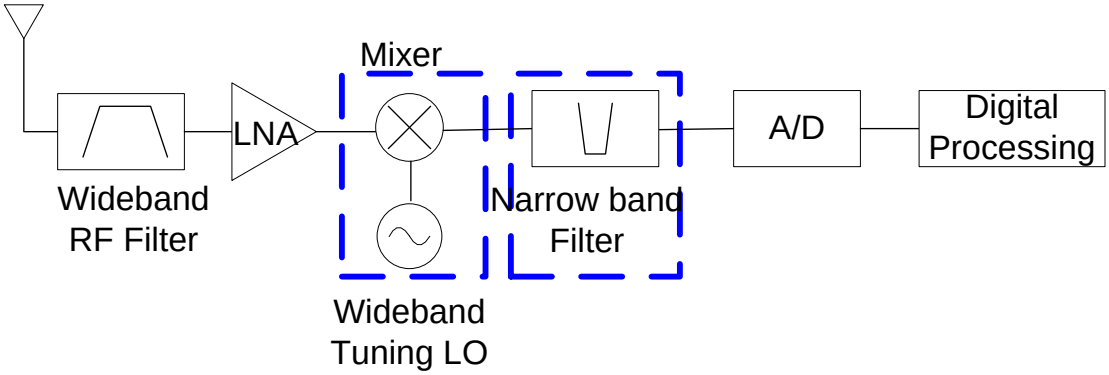


Fig. 1-8 Frequency notch filter approach for interference cancellation.

multi-path fading) complicate wireless communications and require special operations to ensure suitable receiver performance. Such operations typically include channel estimation and, particularly with widely dispersive communication channels, signal equalization. Some recent approaches to these signal processing operations are based on antenna array beamforming that senses the parameter of the interference, such as frequency, modulation, power spectrum density, etc. and generates a sharp spatial notch filter at the direction where the interferer is coming (Fig. 1-9). These approaches, however, are complicated. Phase shifter or digital calibration solutions are always involved [8], so as to compensate the non-reciprocity of the antenna array. Therefore, it could fundamentally be expensive. The cancellation performance is limited by the coherence time of the channel with respect to the responding time of the dynamically programmed antenna array. The performance of such operations may be complex and exceed the budget of a low power front-end, for instance, when a fast-changing channel is the dominant cause of a received signal disturbance.

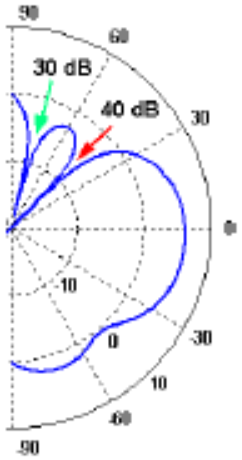


Fig. 1-9 Spatial notch filter approach to reduce the interference of 30*dB* and 40*dB* from two directions.

1.2.3 Time Domain Cancellation

The proposed cancellation scheme in Chapter 2, relates to wideband wireless communication systems. Particular focus on the dynamic range enhancement at the receiver is achieved by blind cancellation of strong narrowband interference from a received signal. Interference in the received signal is estimated using a correlation model matched to a few dominant sources of interference at the receiver. Such estimates may also be used to improve channel estimation, signal equalization, or both.

Our proposed RF architecture with digitally-assisted active cancellation through an adaptive linear prediction filter and reconstruction digital-to-analog converter (DAC) operates at high speed, but consumes little power. The key challenge in this approach is to perform analog subtraction with stringent timing constraints. While the active cancellation approach will consume significantly more hardware because of added digital circuitry and is very susceptible to distortions, it offers more flexibility through digital processing.

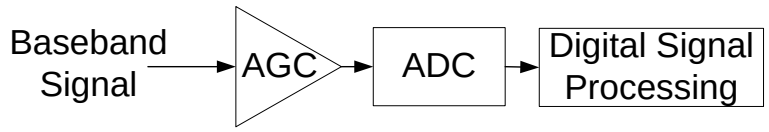
The mixed analog digital architecture will be illustrated in Chapter 2. Detail of the digital processing adaptive algorithm in the interference cancellation system is described in Chapter 3. A high speed, medium resolution, high performance analog-to-digital converter design is implemented to support the cancellation system. The design methodology and performance will be discussed in Chapter 4. Finally, in Chapter 5, we establish a proof-of-concept prototype to demonstrate the proposed time domain interference cancellation architecture, followed by the conclusions in Chapter 6.

Chapter 2

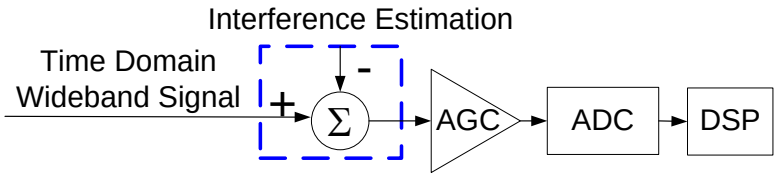
Time domain Interference Cancellation Architecture

As we have seen in the previous chapter, the actual utilization in the 3~4 GHz band is 0.25%, and drops to 0.13% for 4~5 GHz and does not exceed 5% in 5~6GHz. While all the bands have allocations, it is clear from the FCC map that the allocations are not all being utilized. The Cognitive Radio (CR) approach is to treat these allocated users as PU. To provide the maximum flexibility, this sensing and transmission function is performed over the wideband to give the highest probability of detecting unused spectra.

The unique sensing function of Cognitive Radios and the trend for future wireless system force wideband reception at the receiver. Furthermore, it is desirable to detect the weak signal in the presence of much stronger primary interference (low SIR environments). This results in a large dynamic range requirement for the front-end circuitry and in particular for the ADC which must accommodate the large interfering signals while still provides sufficient sensitivity for the CR signal.



a). Typical baseband radio system.



b). An approach to time domain interference cancellation.

Fig. 2-1 Time domain interference cancellation approach.

Fig. 2-1a) represents a typical radio system. The automatic gain control (AGC) is designed to present a full scale signal in front of the signal path ADC, so that all bits of the ADC are utilized. However, because the interfering signal is strong, the gain is limited and the CR signal cannot be amplified enough to achieve sufficient quantization accuracy. For example, to achieve a 20*dB* signal to quantization noise ratio, the required resolution of the ADC would be on the order of 12 bits or greater if there is an SIR of -50*dB*. This level of accuracy, with GHz sample rate results in an infeasible ADC implementation, under power and cost constraints [9].

To reduce the interfering signals to a level that doesn't result in such difficult dynamic range requirements, we have investigated interference mitigation in the time domain. If we can estimate the interference signal and simply subtract it off from the main signal path on a sample by sample basis (Fig. 2-1 b), we can eliminate the large interfering signals and thus reduce the signal path ADC dynamic range requirements to the level needed for simply decoding the desired signal (e.g., the 20*dB* level in the example mentioned previously).

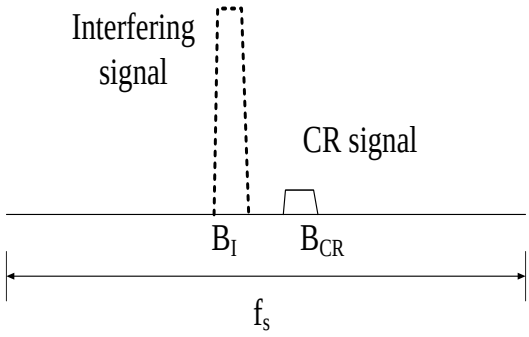


Fig. 2-2 The interfering and CR signal features.

To be able to estimate the interference and separate it out from the signal of interest, there must be some features that distinguish the desired signal from the interference. CR system will be used to illustrate the idea. We exploit two such distinguishing features, summarized in Fig. 2-2. First, we assume the interference is significantly stronger than the desired signal. This allows us to estimate the interference accurately by directly quantizing the wideband signal, with little error caused by the presence of the weak CR signal. Second, we assume that most of the power of the desired signal is outside the bandwidth of the interference. This allows us to filter away the desired signal from our estimate of the interference before subtracting it from the original signal, so that we are left with only the CR signal.

Measurements indicate most of the strong in-band interference can be treated as narrow band with respect to the GHz bandwidth that is focused. Therefore, due to the high over sampling ratio of interfering signal, there exists a high correlation between samples. This correlation provides us with a further gain in estimating the strong interference without actually decoding it.

Section 2.1 develops the mixed signal architecture for a time domain cancellation system and discusses the critical analog design issues including the delay element and mixed signal design requirements. Cancellation digital processing techniques are illustrated and explained in Section 2.2 In Section 2.3 , the proposed system is evaluated through simulation under different environments, and results show the effectiveness of the dynamic range reduction and feasibility of circuitry implementation.

2.1 Mixed Signal Architecture

The design of the ADC presents the biggest challenge in a wideband receiver of CR and future radio systems. As an example, let us consider use of a 1 GHz band for the detection of unused spectra. The ADC speed requirements are minimized if the signal is mixed to baseband, resulting in a 500MHz baseband bandwidth. Without assistance from the digital circuits and change in receiver architecture, the analog to digital conversion of such a wideband signal introduces unacceptable system complexity and power consumption.

In this section, two proposed mixed signal architecture will be discussed, the feedforward architecture and the feedback architecture. The former one composes a main signal path and an interfering signal estimate path, operating in an open loop. The latter one executes the estimation of the strong interference in a closed-loop manner, providing much accurate estimates, yet resulting in a requirement of more sophisticated algorithm and extra issues of stability.

2.1.1 Feedback Architecture

Block diagram in Fig. 2-3 shows the feedback architecture front-end design for active cancellation of interferers. The purpose of the loop is to subtract the interference signal, *I,* caused by the strong (undesired) interference. The feedback path (consisting of the adaptive filter,

predictor, and DAC) extracts the interfering signals for feedback cancellation. Because the ADC, DAC, and adaptive filter each has intrinsic delay, a multistep predictor is needed in order to compensate for this delay. Upon loop convergence, the cancellation signal (I_r) roughly approximates the incoming interference (I), so that the dynamic range of the residue signal (ε_r) is dramatically reduced, enabling the detection of the weak CR signal S. The interfering signals are quantized and extracted to provide an estimate which is used for subtraction.

At initialization, $I_r = 0$, $\varepsilon_r = I + (S + N)$, where N is the thermal noise at the front-end. The estimation error, ε_r, is dominated by the interference. It is quantized through the high speed low resolution ADC in the loop. The AGC amplifies the error signal such that the full range of the converter could be used. The linear adaptive filter extracts the ADC output to provide a raw estimation, which is further reconstructed by the DAC as I_r. The estimation of the interference, I_r, is improved throughout the loop. The accuracy replies on the complexity of the algorithm, and the capability of recovering interference from its subtraction residue. A few samples for training purpose are required.

There are several challenges in this feedback approach. Firstly, the adaptive filter used to regenerate the interference has a time-varying input signal and its estimation accuracy is affected by noise, quantization, prediction errors and speed, therefore limits the performance of the interference cancellation. Secondly, since this is a closed-loop structure, it is difficult to guarantee its stability because of the phase shift accumulation along the loop. Last but not least, the key challenge in this approach is to perform analog subtraction in a closed loop with stringent timing constraints.

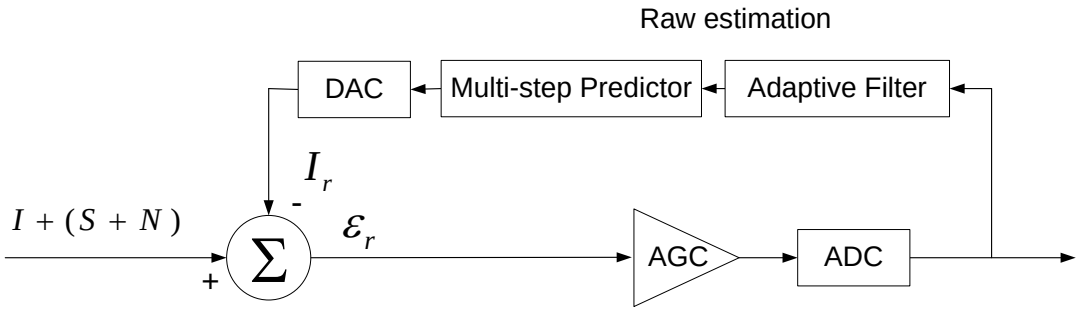


Fig. 2-3 Feedback architecture for time domain interference cancellation.

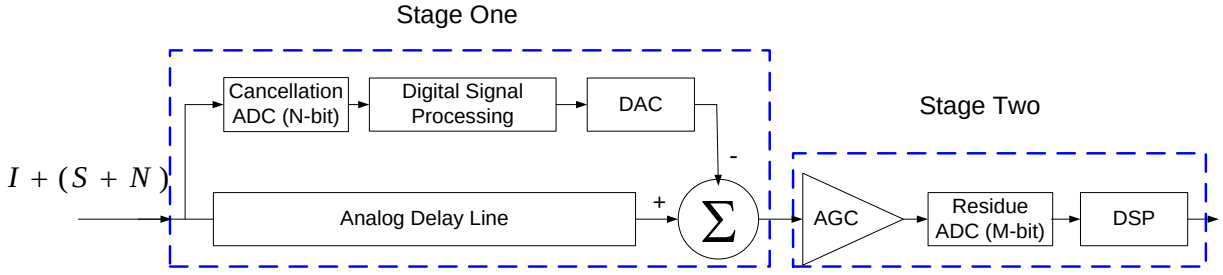


Fig. 2-4 Feedforward architecture for time domain interference cancellation.

2.1.2 Feedforward Architecture

To overcome the limitations of the feedback architecture, alternative feedforward architecture is proposed. Fig. 2-4 illustrates the proposed feedforward radio front-end architecture for active cancellation of strong interferers. An estimation of the interference is created in the cancellation path to be used for subtraction of the strong interference and thus reduces the dynamic range requirements of the ADC in the signal path (the Residue ADC).

We consider an input signal composed of the CR signal of interest, strong in-band interference and thermal noise. The input signal branches into two paths, one of which immediately quantizes through a high speed low resolution ADC (the Cancellation ADC). The active interference cancellation is achieved through the use of an adaptive linear filter and reconstruction DAC in the cancellation path. There might be a notch filter involved in the cancellation path. The purpose is to remove the desired cognitive radio signal from the interference for improved estimation, and to avoid unwanted cancellation/distortion of the desired signals. Since the ADC, digital signal processing (DSP) block and DAC involve a processing delay, *t*, this same delay must be added to the main signal path to align the signals in the two branches for proper cancellation. The noise level added through the delay line should be sufficiently below the CR signal level to retain high sensitivity for detection.

The whole system can be regarded as a selective AGC which amplifies the CR signal, but not interfering signals. This technique allows two low-resolution ADCs with N and M bits to substitute for a single high-resolution ADC of greater than $N + M$ bits.

The system is composed of two basic mixed signal stages (Fig. 2-4). Stage one involves the interference subtraction, with its output (residue signal) including the CR signal, the cancellation error and noise. Stage two then amplifies this residue to full scale of the Residue ADC, and performs additional digital filtering to pass only the CR signal.

The tradeoff between the number of bits in the cancellation ADC and residue ADC depends on the interference strength, that is, strong interference situations require more bits in cancellation ADC, as will be discussed in Section 2.3.2 . While the timing constraints of the feedback loop are avoided by this architecture, it still requires matching of the latency through the two paths using an analog delay line. The challenge of analog delay line is avoided by using a combination of multi-step digital prediction in the cancellation path and a fractional delay through a continuous analog delay line, as will be discussed in Chapter 5.

2.2 Cancellation Digital Processing

The digital signal processing in the cancellation path are required to estimate the interfering signals, while ignoring the desired signal, so that the CR signal is not subtracted off along with the interfering signals.

After the signal is quantized by the relatively low *N*-bit resolution Cancellation ADC, a white quantization noise will be added. As mentioned before, since it is assumed that the interfering signals are narrow band signals, a high oversampling ratio of the interfering signal can be exploited in the estimation.

The more accurately the interfering signal can be estimated, the more effectively can it be cancelled and hence the larger gain could be in the AGC before saturation will occur in the following Residue ADC. The goal is to be able to amplify the desired signal to full scale of the ADC so that the full *M*-bits of the Residue ADC will be available for quantizing the residue signal from the previous stage.

To measure the estimation accuracy, the time domain sample-by-sample difference between the interfering signal and its estimation needs to be tracked. We use the mean squared error (MSE) to estimate the power level attenuation achieved by cancelling the strong interference and reducing the in-band noise.

2.2.1 Dual Adaptive Filter (AF)

To estimate the interfering signal, we use a two stage adaptive filter process [10]. The first stage uses the time varying behavior of the normalized least mean square (NLMS) adaptive filter with a large step size to produce a frequency locked estimation of the interference. The second stage uses NLMS with a small step size as an approximation to the ideal Wiener filter [11] to correct the phase and magnitude of the output from the first stage and produce an interference estimate suitable for cancellation. Details of the adaptive filter approach of the interference cancellation will be discussed in Section 3.2 .

Here, two key points are to be noted:

1) The first adaptive filter uses a large step size. It enables us to track the time-varying interferer by rapidly adapting to any changes in the interfering signal, such as occurred with data modulation; The second adaptive filter operates more conventionally using a small step size to ensure that the passing band of that filter around the interference frequency is narrow enough to provide the least possible distortion to our CR signal and minimum filtered quantization noise.

2) Sampling at high speed yields a high oversampling ratio relative to the narrowband interferer, which results in more correlation between samples and therefore better estimation.

2.2.2 Processing Gain and Interference Attenuation

The high oversampling ratio not only brings the advantage of high correlation between samples, but also allows the implementation of a relatively narrow band pass filter created by the dual AF. It is therefore possible to achieve extra processing gain by filtering out the quantization

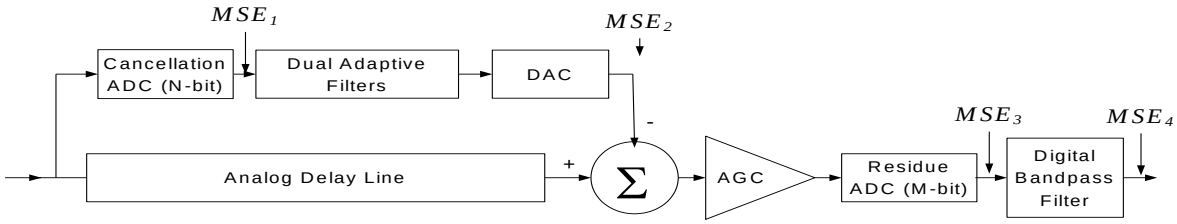


Fig. 2-5 The system architecture and MSEs interested in the cancellation.

noise outside of the interference band, which would contribute significant power to the residue after the subtraction of the interfering signal.

We also achieve additional processing gain when the CR signal is narrow band. By using a very narrow band digital filter around the center frequency of the CR signal, the quantization error from the Residue ADC can be significantly reduced by the following digital bandpass filter.

In the following analysis, we measure the processing gain and the interference attenuation by computing the MSE throughout the receiver signal path (Fig. 2-5).

Without loss of generality, we assume the power level of a single existing in-band interference to be P_I, and that of CR signal to be P_{CR}. Both are assumed to have a flat spectrum over their own signal bands with $P_I >> P_{CR}$ (Fig. 2-2). The bandwidth of interest is f_s, which is assumed to be wide compared to the interfering and the CR signals. The overlap bandwidth between the interfering signal and CR signal is B_{OL}, with B_I and B_{CR} the bandwidths of interfering and CR signals respectively. We assume $B_{OL} << B_{CR}$ so that most of the energy of the CR signal is outside the bandwidth of the interferer.

In contrast to ADC's, power efficient, high-resolution, and high-speed DAC's are significantly easier to implement [12]. Thus, we assume the DAC's resolution is sufficiently high that no quantization noise is added by the DAC in the cancellation path.

MSE will be dominated by quantization of the interfering signal, which in the case of an N-bit low resolution ADC is approximately,

$$MSE_1 = P_I \cdot 2^{-2N} \tag{2.1}$$

When there is little overlap between the interfering signal and the CR signal, namely, $B_{OL} << B_{CR}$, the dual AF will ideally have a transfer function which is narrow enough to pass only the interfering signals. The stop band attenuation is assumed sufficiently large that the quantization noise outside of the interference band and the CR signal would then be absent from the filtered interference estimation. After reconstruction by DAC, the MSE will be reduced to the following:

$$MSE_2 = MSE_1 \cdot \frac{B_I}{f_s} = P_I \cdot 2^{-2N} \cdot \frac{B_I}{f_s} \tag{2.2}$$

The thermal noise added by the high resolution delay line element in the main path is significantly below the CR signal level. After subtracting the interference estimate from the

delayed main signal, the residue becomes the CR plus the error in estimating the interference. This residue has the power of $MSE_2 + P_{CR}$.

By exploiting the AGC to amplify the residue up to the full scale of the Residue ADC, this low resolution converter would produce an MSE equal to:

$$MSE_3 = (MSE_2 + P_{CR}) \cdot 2^{-2M} \tag{2.3}$$

After stage one, a sharp narrow band digital filter could be applied to pass only the CR signal band, so that final MSE becomes:

$$MSE_4 = MSE_3 \cdot \frac{B_{CR}}{f_s} \tag{2.4}$$

Substituting (2.2) and (2.3) into (2.4), we get

$$\begin{aligned} MSE_4 &= (P_I \cdot 2^{-2N} \cdot \frac{B_I}{f_s} + P_{CR}) \cdot 2^{-2M} \cdot \frac{B_{CR}}{f_s} \\ &= P_I \cdot 2^{-2(N+M)} \cdot \frac{B_I \cdot B_{CR}}{f_s^{\,2}} + P_{CR} \cdot 2^{-2M} \cdot \frac{B_{CR}}{f_s} \end{aligned} \tag{2.5}$$

Clearly, it can be seem that the equivalent resolution of interfering signal could eventually become more than $N + M$ bits and there is a processing gain of the product of two oversampling ratios. Furthermore, almost the full resolution of the Residue ADC can be used for subsequent processing of the CR signal.

For comparison, without interference cancellation, a single ADC would lead to an MSE of

$$MSE_{BL} = (P_I + P_{CR}) \cdot 2^{-2M} \cdot \frac{B_{CR}}{f_s} \tag{2.6}$$

with quantization noise of strong interference dominates. Our approach indicates that it is possible to reduce the interference further by a factor of $2^{2N} \cdot f_s / B_I$, so that the MSE caused by interference would be on the order of the quantization noise of the CR signal. Thus, the total MSE is very well reduced.

In an actual implementation, due to the estimation error and limitation of number of taps used in the dual AF, the imperfectness of the digital filter, and the AGC clipping or limited amplification of the residue, the MSE attenuation determined above presents an upper limit.

2.2.3 CR Signal Protection

The requirement to protect the CR signal is of great importance. In our approach, when the CR signal is buried in the quantization noise, the dual AF is less sensitive to it. When it becomes relatively strong, such as in an environment with medium to low interference (ISR below 30*dB*),

it is no longer possible to distinguish the interfering and the CR signal through magnitude. Although dynamic range is not problematic in those situations, suitable measures have to be taken to protect the CR signal to avoid any distortion due to adaptation to the desired signal on the cancellation path.

One possible method is to use the pre-knowledge from the control channel that includes the possible band(s) of the desired signal, the features, include but not limited to, energy, signal footprint, such as modulation type, symbol rate, and overlapping in power spectrum density [13]. Therefore, digital notch filter in the cancellation path could be added that is aware of the transmitting band of CR. In addition to that, when ISR is below 0*dB*, it can be seen that the receiver dynamic range is determined by the CR signal. Therefore no interference cancellation is necessary. A pre-knowledge of the power spectrum density of the CR signal, used together with the output from the adaptive filter on the cancellation path, provides an option to turn off the first stage.

Among other degrees of freedom available, spatial domain beamforming [14] can create a notch at the direction that the CR signal is coming. Thus prevents the appearance of the desired signal in the subtractor.

Large stop band attenuation design leads to long delay in digital filters, and is power consuming. To avoid that, a more efficient way could explore a possible solution from a system design perspective. Instead of utilizing a narrow spectrum, when primary user allows for low power spectrum density interferer, it is applicable to choose the transmit CR signal modulation which codes the signal as random noise over a wide bandwidth, such as CDMA, so that dual AF will have no difficulty in ignoring the signal of interest. A demonstration of such modulation will be shown in Chapter 5, which significantly reduces the estimation error of the adaptive filter without extra effort of designing the digital CR-signal-notch filter, thus avoid any extended delay through the main path.

2.3 Performance Evaluation and System Design Specification

First, we inspect our proposed system by receiving a strong FSK modulated interfering signal and a FSK modulated CR signal. The Simulink model is built as shown in Fig. 2-6. The narrow band FSK signal has strong correlation between samples, which facilitates accurate estimation. FSK modulation inherently has time-varying characteristic, which could display the dynamic behavior of the CR signal. Fig. 2-7 are simulation results which verify the advantage of dynamic range reduction.

By using a 5-bit Cancellation ADC, a first stage 10-tap 1.0 stepsize together with a second stage 10-tap 0.01 stepsize dual AF, an 8-bit resolution DAC, with an appropriate delay for the analog subtraction, we can attenuate the strong interference and reduce the dynamic range to the Residue ADC by almost 35*dB*, thus extending the effective number of bits for this system by nearly 6 bits.

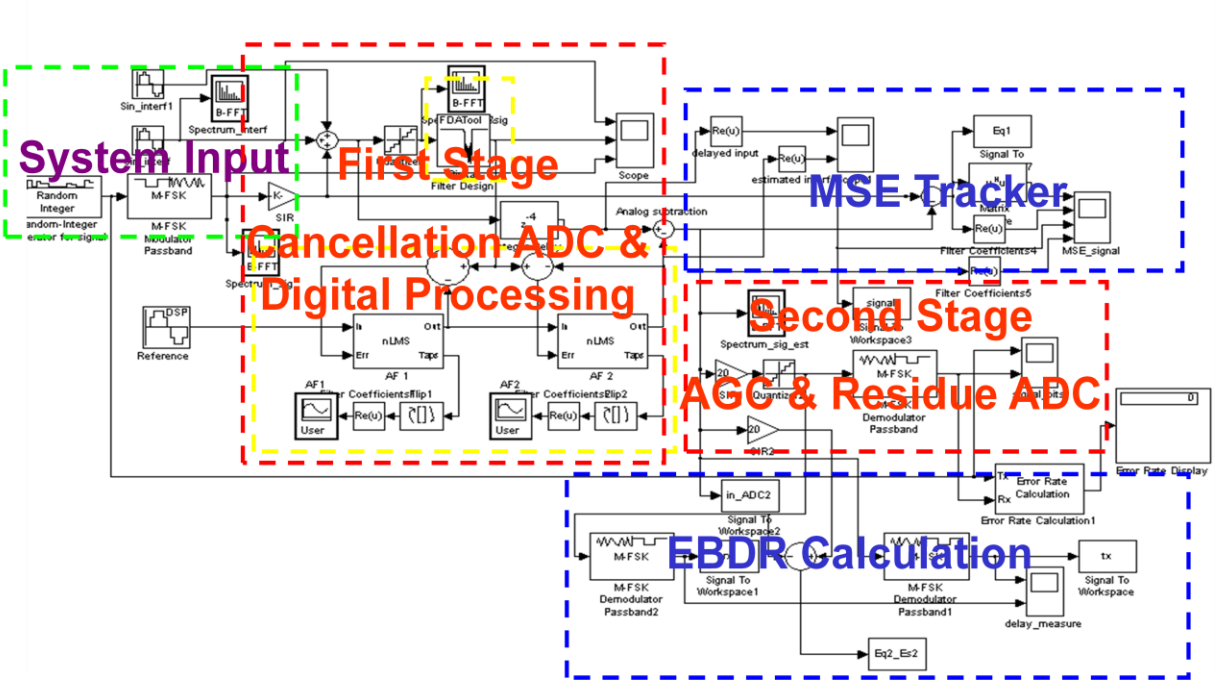
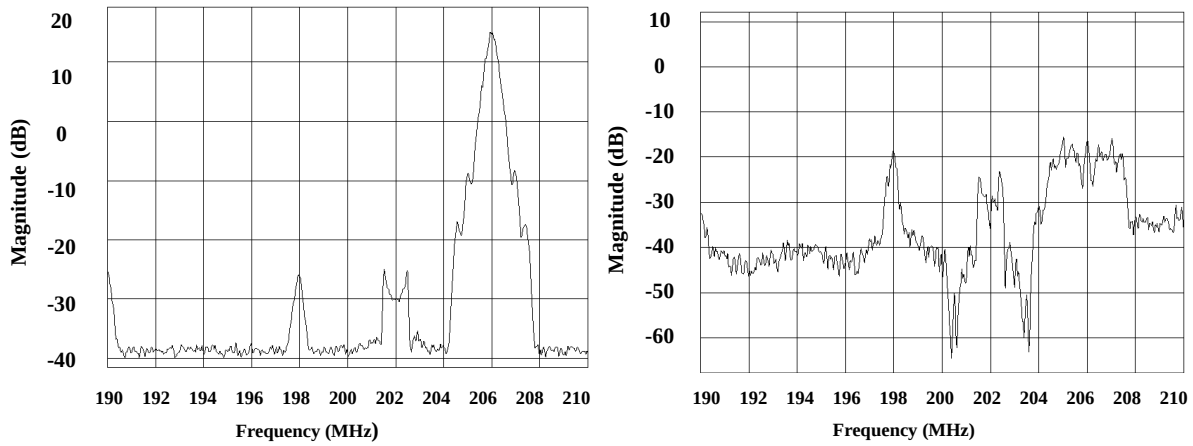


Fig. 2-6 Simulation Setup for the proposed time domain interference cancellation



a). An incoming of multiple interfering signals (a moderate sinusoidal interferer, a strong FSK modulated interferer) and an FSK modulated CR signal.

b). The power spectrum after interference cancellation with strong interfering signal been attenuated by almost 35*dB* when using 5 bits for the Cancellation ADC and 4 bits for the Residue ADC.

Fig. 2-7 Simulation showing interference attenuation using the cancellation approach.

2.3.1 SINR after Attenuation

The relationship between attenuated signal to interference ratio (SINR) and number of bits used in the Cancellation ADC is investigated in different environments, i.e. different CR signal to interference signal ratio (SIR). Fig. 2-8 presents, for a single 1MHz wide interfering signal, the SINR improvement as we increase the resolution of the ADC.

The curves' slope in Fig. 2-8 indicates that the incremental of SINR is 39*dB* when ADC resolution increases by 4 bits, which is 9.75*dB* per bit of the Cancellation ADC. This is more than a conventional ADC, in which each additional bit gives an SNR improvement of 6*dB*. The extra 3.75*dB* comes from the improved ability of the adaptive filter to reject quantization noise as resolution of the Cancellation ADC increases.

This is mainly due to the fact that we are only using 10 taps for the dual AF. The adaptability is limited when resolution of the Cancellation ADC is low, since the passing band bandwidth is relatively wider than that of the interfering signal. As a result, the quantization noise after the subtraction contributes comparably to the error in interference cancellation in the SINR. The more bits the Cancellation ADC has, the more gain we get by exponentially decreasing the in band noise.

The processing gain from oversampling is evident when the slope becomes 6*dB*/bit, thus, interference error dominates the denominator of the SINR. As an example, when SIR is -30*dB*, a 6-bit ADC results in a SINR after cancellation of 26*dB*. The interfering signal has been attenuated by 56*dB*, which is equivalent to 9.3 bits; the extra 3.3 bits come from the oversampling ratio as a result of the processing gain as explained in Section 2.2 . This gain is less than the theoretical gain (oversampling ratio of 500 implies 4.5bits of additional gain). This is mainly because we cannot form a brick-wall filter that strictly passes only the interfering signal, and therefore leads to a decreased attenuation.

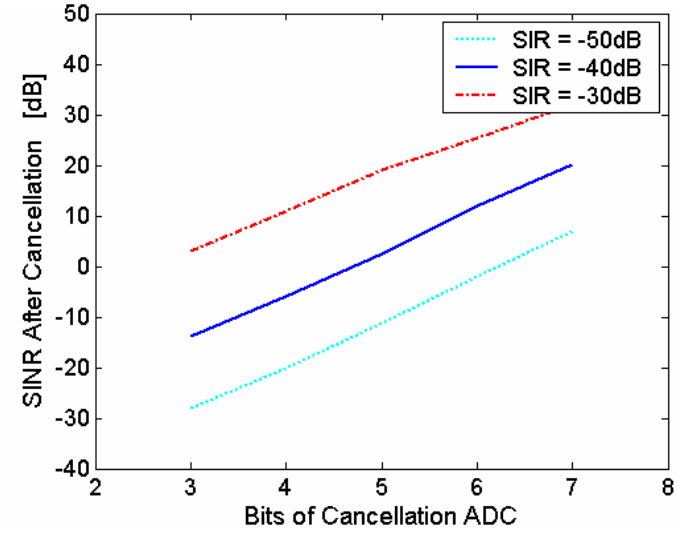


Fig. 2-8 SINR greatly improved using low resolution ADC in difference environments.

Another observation is for a given SIR, less resolution in the Cancellation ADC actually simplifies the design. Because, even without filtering, the dual AF is insensitive to the CR signal that are buried under the quantization noise.

As we increase the number of bits, we will finally reach a point where additional bits do not bring any benefits without active reduction of the CR signal in the cancellation path. For instance, when the Cancellation ADC has 6 bits, in an environment with an SIR of -20*dB*, if we calculate the slope of the curve, the attenuation rate drops to less than 6*dB*/bit. This comes from the dual AF which begins to consider the desirable CR signal as interference, since we are doing a blind adaptation.

2.3.2 Residue Signal Analysis

We calculate the residue signal at the input to the AGC of the second stage which includes the CR signal, the cancellation error of the interference and the filtered quantization noise (Fig. 2-9). The resolution for the desired CR signal is determined by the second stage, mainly, the effective gain provided by the gain stage.

2.3.2.1 Ratio of Signal Peak to Residue Peak

The AGC is assumed to amplify this composite signal to full scale of the Residue ADC, indicating that the CR component will still be less than full scale (Fig. 2-10). This fraction will depend on the time domain peak magnitude ratio between the CR signal and the residue as in Fig. 2-11. If the ratio becomes less than one, it will result in a loss of effective bits from the Residue ADC for the CR signal.

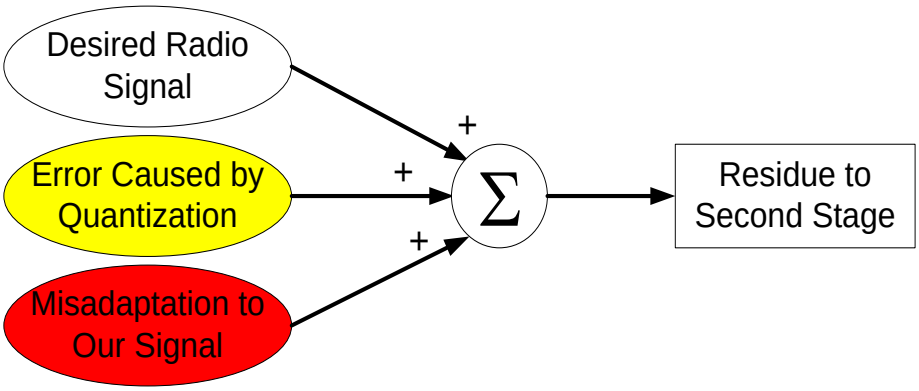


Fig. 2-9 Residue signal break down of the first stage.

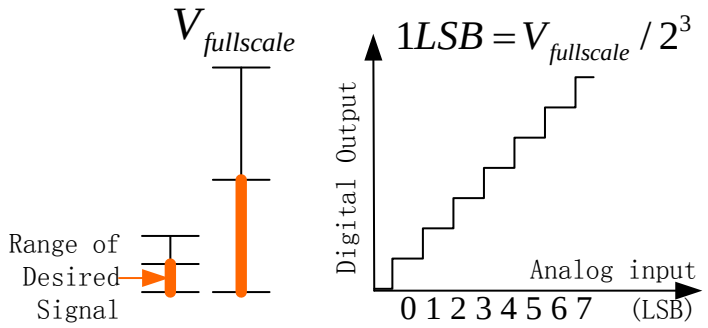


Fig. 2-10 Amplification of the residue signal from the first stage.

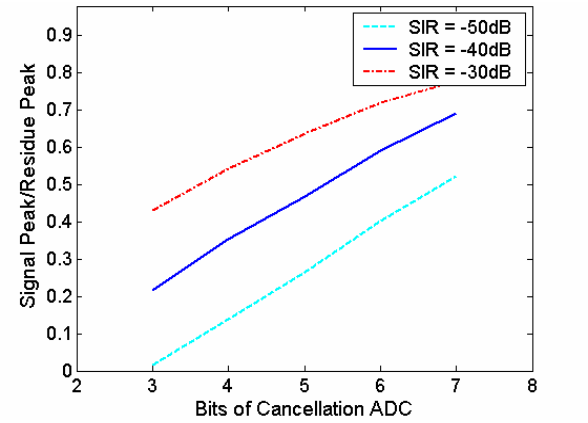


Fig. 2-11 Time domain peak ratio of the CR signal to the Residue.

We are expecting that as the CR signal becomes weaker, more bits in the Cancellation ADC should be used to attenuate the interference signals. At the same time, this leads to a reasonable peak magnitude ratio for limiting the requirement of the Residue ADC to keep maximum detection sensitivity.

2.3.2.2 Residue Power Analysis

To analyze the sensitivity of the system, we will calculate the input signal to system output noise ratio as is explained Fig. 2-12. The first term depicts the equivalent resolution through the Cancellation ADC and the adaptation. The second term is the effective resolution through the Residue ADC determined by the gain provided from stage two. The third term is dominated by the percentage of RMS of the desired signal power in the total power of the residue.

For different environments, this RMS ratio, as plotted in Fig. 2-13 sets a maximum number of bits we want to assign to the Cancellation ADC. The achievable improvement saturates as the Cancellation ADC resolution increases, which indicates overdesign of the converter. To avoid extra power consumption, it is desirable to reduces the Cancellation ADC resolution N in high SIR environments.

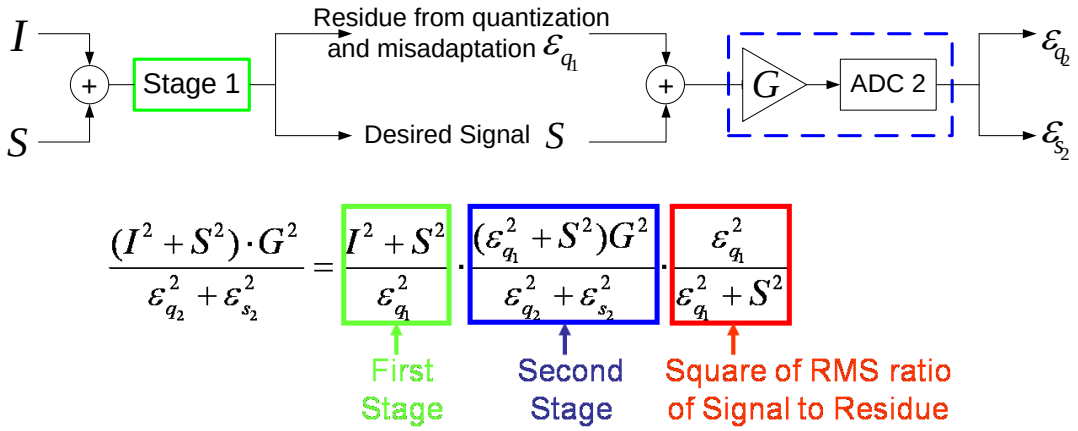


Fig. 2-12 Residue power analysis.

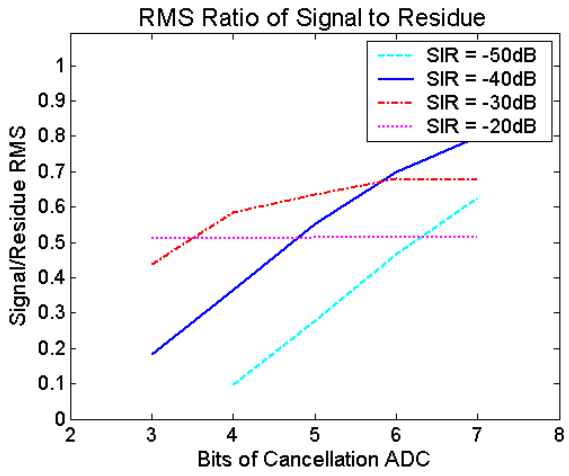


Fig. 2-13 RMS Ratio of signal to Residue versus Bits of Cancellation ADC

2.3.3 Overall EBDR for Different SIR

By combining two stages, our simulation shows the overall system Effective Bits from the Dynamic Range Reduction (EBDR) is close to $N + M$, as shown in Tab. 2-1, if the gain of the AGC is set equal to 2^N. Optimizing the resolution in the Cancellation ADC can avoid complex design of the CR signal protection by ensuring that the AF is not able to track that signal.

Also, we observed from the simulation, when using the FSK modulation for the interference, as the frequency of the interfering signal is modulated, there is a transient edge effect at the symbol boundaries. At these random transitions, there will be large error peaks. Therefore the gain of the second stage AGC may be limited by these spikes. If they can be made sufficiently short in duration by fast adaptation of the AF, then it may be possible to simply clip them without significant distortion of the CR signal.

A summary of specifications for a system implemented is given in Tab. 2-2, which uses 6 bits in the Residue ADC in order to accommodate the peak magnitude ratio drop due to spikes and clipping, while providing a worst case effective resolution of 3 bits for the CR signal, which is good enough for most communication systems. The table is based on simulation results with an OSR of at least 50.

Tab. 2-1 Overall EBDR for different SIRs using different resolution ADCs

SIR=-40*dB*

ADC resolution Cancellation ADC + Residue ADC	Without Notch Filter	With Notch Filter
3bits+4bits	8	7.9
4bits+4bits	9	8.8
5bits+4bits	9.9	9.4
7bits+4bits	10.2	9.8

SIR=-50*dB*

ADC resolution Cancellation ADC + Residue ADC	Without Notch Filter	With Notch Filter
4bits+4bits	9.2	8.6
5bits+4bits	10.4	9.7
7bits+4bits	11.5	11

Tab. 2-2 System specification summary

SIR	>-50*dB*
Cancellation ADC	1GHz / 3~6bits
Residue ADC	1GHz / 6bits
DAC	1GHz / 8bits
AGC Gain	<40*dB*
Maximum Dynamic Range Reduction	>40*dB*
Overall EBDR	11.6bits

2.3.4 System Specification for Cancellation ADC and DAC

To optimize the system specification with minimum power consumption, an illustration of how to choose the number of bit of the Cancellation ADC, *N*, is shown from the graphs in Fig. 2-14.

For instance, given an approximately known SIR around -40*dB*, required resolution for signal is 20*dB*, which is 3bits, maximum bits could be designed to residue ADC is 4bits. The RMS ratio plot provides a power efficient design of the Cancellation, sets the upper bound *N* to be 6bits. Because for stage two $M-3bits=1bit$, minimum peak ratio of signal to residue is ½. The peak ratio plot in Fig. 2-11 sets the lower bound of *N* to be 5-bit. Choosing *N* to be 5-bit, from Fig. 2-8, the SIR improvement is found to be *40+2= 42dB*, which specifies a DAC resolution of 7bits.

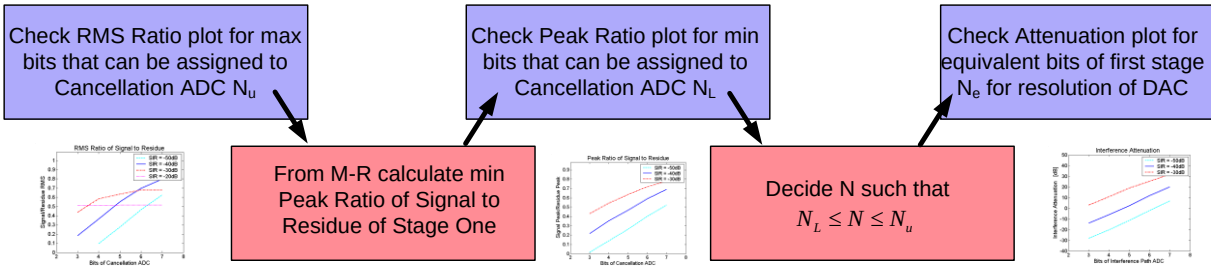


Fig. 2-14 Determine the resolution *N* of the Cancellation ADC and the DAC

2.4 Conclusion

By using the time domain interference cancellation, it is possible to reduce narrowband interferers so that an in-band signal can be more effectively detected. By using a mixed signal architecture, which contains two low resolution ADC's, it is possible to effectively act as a high-resolution ADC in terms of the ability to resolve a small desired signal in the presence of a large interfering signal.

Chapter 3

Digital Signal Processing in Interference Cancellation

In this chapter, we analyze the trade-offs, from digital signal processing aspect, among several design-related issues for active cancellation of interference and expand it further, combining equalization of a time-varying channel in a cognitive radio system. The analysis is further demonstrated through simulation.

In order to perform active cancellation of interference, we will have to make some assumptions about how the interference looks in various frequency bands. This a-priori information can be gained while sensing the use of spectrum by neighboring devices before a cognitive radio starts using a chunk of the spectrum. As we mentioned in Chapter 2, the most common form of interference is narrow-band interference. Since, it is assumed, the cognitive radio has found a hole in the spectrum (where there is no primary user), and to find such a preferred band to transit, the bandwidth of both the transmitter and the receiver of the cognitive radio system are required to maintain sufficiently high. Hence, the interference is generally comparably narrow band, and can be of very high power, with SIRs of -50*dB* occurring frequently.

Another major problem in a cognitive radio system is channel equalization. In fact, in receivers operating in wireless environments, the channel equalizer is the component that requires the most chip area and energy. The simulation of a linear least mean squares (LMS) equalizer and a decision feedback equalizer (DFE) are explicitly compared here.

In this chapter, we will focus on adaptive interference cancellation, channel equalization, and the combining of the above two. Several kinds of interference are considered. The performance of the two adaptive interference cancellation processing algorithms are compared, under two performance metrics, the Bit Error Rate (BER) and the Mean Square Error (MSE). Then, the effect of relative interference bandwidth on the performance of the system is presented to address the flexibility on the first assumption of the "narrow-band" interference. Finally, the equalizer and the test system are included when the channel is a time varying Rayleigh fading channel or an AWGN channel.

3.1 System Model

The model used for the system is divided into three stages shown in the Fig. 3-1, Fig. 3-2 and Fig. 3-3 below:

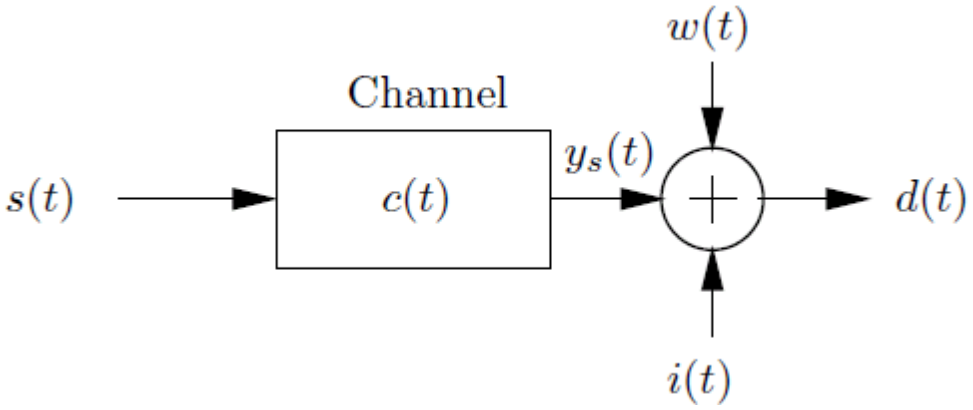


Fig. 3-1 Signal flow through the channel.

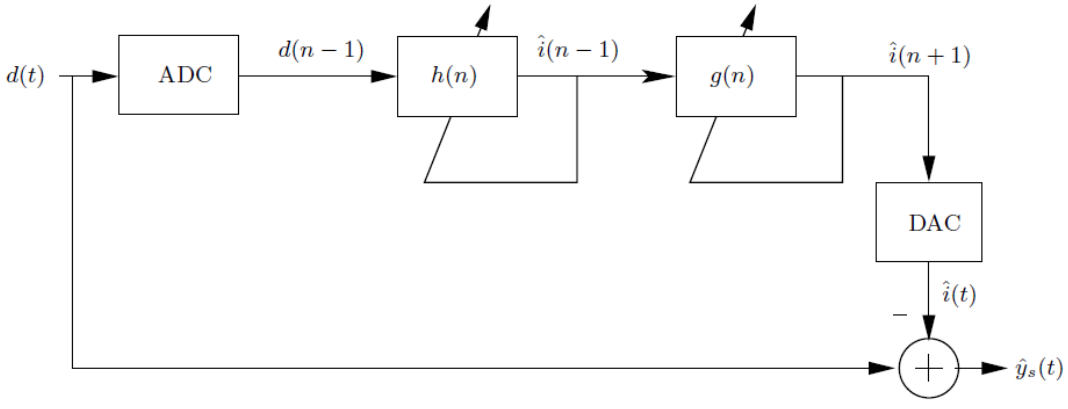


Fig. 3-2 Illustration of an interference cancellation system in cognitive radio.

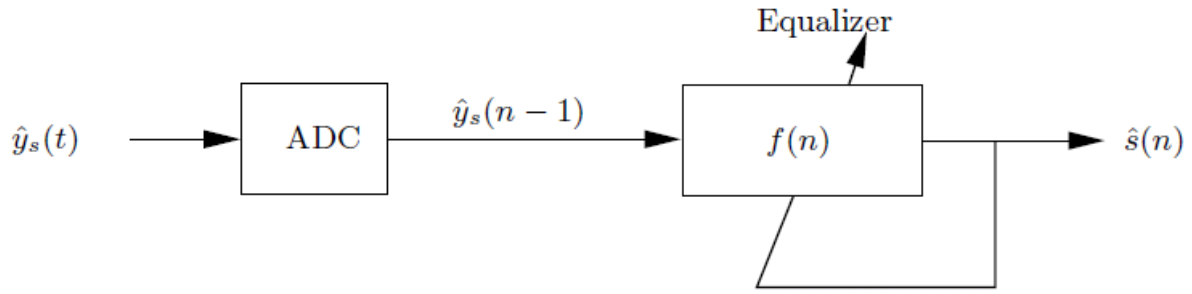


Fig. 3-3 A system illustrating channel equalization in cognitive radio.

In Fig. 3-1, $s(t)$ is the transmitted signal, $i(t)$ is the interference, $c(t)$ is the channel impulse response, and $w(t)$ is a white Gaussian noise process. The sum of $y_s(t)$, the interference and the noise is the received signal at the receiver, which has been called the signal $d(t)$.

In Fig. 3-2, the receiver then samples this signal and due to a delay inside the ADC of one sample, it is assumed that the output of the ADC is $d(n-1)$, a delayed version of $d(n)$ which is the ideal sampled version of $d(t)$. The adaptive filter tries to get an estimate of the delayed interference, $\hat{\imath}(n-1)$. This is not good from an interference cancellation point of view, as the current value of interference for cancellation is wanted. So, an adaptive two sample forward predictor, $g(n)$ is built to compensate for the delays in the ADC and DAC. Note that two samples are predicted ahead instead of one to take into account the delay in the DAC that follows the predictor since the DAC is assumed to have a delay which is the same as the ADC. The final output of the interference cancellation block is an analog estimate of interference which can be used for cancellation. Subtracting it from $d(t)$, gives the an estimate of $y_s(t)$. Of course, the estimate of the interference is noisy because the filtered signal and AWGN affect on the estimation.

Finally in Fig. 3-3, the estimate, $\widehat{y_s}(t)$ is passed through an ADC which is to be filtered by an adaptive equalizer to remove the effect of the channel on the signal. The estimate of the signal, $\hat{s}(n)$, is provided in the discrete time domain.

It is assumed that there are two samplers (ADCs) in the system and the sampler used in interference cancellation can be of comparable resolution to the sampler used in the equalization block. The time alias of the two paths, cancellation and the main path, is realized through the predictor. This model has been used under the observation that two samplers which do not have to be both high resolution and high speed will be cheaper than one sampler which is both high resolution and high speed. The multi-step predictor can be easily implemented in the system. In the simulation that follows, all computations are in discrete time.

The model is hence a baseband model in which timing and carrier synchronization are assumed to be handled perfectly. With these assumptions, in particular, fractionally spaced equalizers or the constant modulus algorithm (CMA) for equalizer adaptation are not considered because these techniques are used to help in the areas which are assumed not to be an issue.

3.2 Adaptive Filter Approaches

3.2.1 Assumptions

In this section, a scenario with the assumption that there is no channel and no noise is first exploited. Hence $d(n)$, the received signal is the summation of $s(n)$ and $i(n)$. It is also assumed that the signal $s(n)$ and interference $i(n)$ are uncorrelated. Even though this will likely not be the case, we assume the signal and interference are zero-mean jointly wide sense stationary processes. This is so we may assume properties about the autocorrelation functions of each, namely, the signal $s(n)$ has an autocorrelation function that decays much faster than the autocorrelation function of the interference $i(n)$. It is not restricted that the interference needs to be sinusoidal in the development of the two adaptive filter approaches. However, it is definitely wanted that the block should be able to estimate and cancel sinusoidal or "near-sinusoidal" interference such as an FSK signal. The two-step ahead predictor, $g(n)$, used in both approaches is an LMS adaptive linear predictor using estimation of the signal autocorrelation. Its performance was not the main concern for the system, as it is only desired to predict a fairly predictable signal such as a sinusoid two samples ahead.

Based on this fundamental scenario, the two adaptive filter approaches for the filter $h(n)$, which essentially extracts the interference from the sum of the signal and interference are to be explained and compared.

3.2.2 Single Adaptive Filter Approach

The single adaptive filter is based on an LMS adaptive filter. The computation of the estimation error is based on current estimate of the tap-weight vector. At each iteration or time update, the algorithm requires knowledge of the gradient, tap-weight and destination vector. Though the algorithm uses instantaneous estimates, it is recursive in nation. Thus during the adaptation, the adaptive filter could effectively averages these estimates in some sense. The details of LMS adaptive filter is discussed in [15]. To do interference cancellation, the single adaptive filter has been designed as shown in Fig. 3-4. Let us assume the signal, $s(n)$, is a wideband process with an autocorrelation sequence that is approximately zero for lags $k \geq k_0$ and $i(n)$ is a narrow band process that has an autocorrelation which dies off well after k_0. The mean square error that is formed by taking the difference between $d(n)$ and the output of the adaptive filter $y(n)$ can be expressed as follows:

$$\begin{aligned} E\left\{e^2(n)\right\} &= E\left\{\left[s(n)+i(n)-y(n)\right]^2\right\} \\ &= E\{s^2(n)\}+E\{[i(n)-y(n)]^2\}+2E\{s(n)[i(n)-y(n)]\} \end{aligned} \tag{3.1}$$

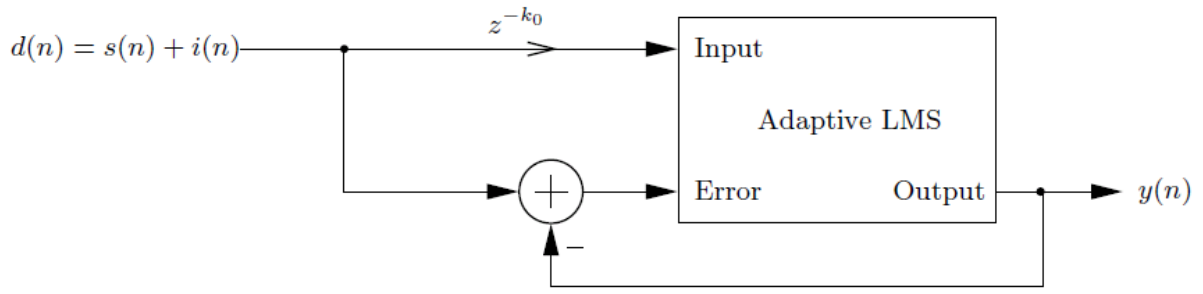


Fig. 3-4 Single adaptive filter approach for interference cancellation.

Since $s(n)$ and $i(n)$ are uncorrelated, $E\{s(n)i(n)\} = 0$, and the last term simplifies to

$$2E\left\{s(n)\left[i(n)-y(n)\right]\right\} = -2E\{s(n)\,y(n)\} \tag{3.2}$$

Since the input to the adaptive filter is $d(n-k_0)$, the output $y(n)$ is

$$y(n)=\sum_{k=0}^{p} w_n(k)\,d(n-k_0-k)=\sum_{k=0}^{p} w_n(k)[s(n-k_0-k)+i(n-k_0-k)] \tag{3.3}$$

Again, $s(n)$ and $i(n)$ are uncorrelated and $s(n)$ is uncorrelated with $s(n-k_0)$ from the wideband assumption, we get that $E\{s(n)y(n)\} = 0$ and the mean square error becomes

$$E\left\{e^2(n)\right\} = E\{s^2(n)\} + E\left\{\left[i\ n\ -y\ n\ \right]^2\right\}$$

Hence minimizing $E\{e^2(n)\}$ is equivalent to minimizing $E\{[i(n)-y(n)]^2$. Thus the output of the adaptive filter will converge to the linear least square estimate of $i(n)$, obtained by an FIR filter of length $p + 1$.

This could be used to estimate and predict the interference two samples ahead and cancel the interference from the received signal. The technique yields nearly zero error for sinusoidal interferences because they are perfectly predictable. However, as we will see in Section 3.2.4 , this approach gives big spikes in the MSE, which result in destabilization of the equalizer block that is added into the system later when the interference is a modulated signal like FSK. Hence, interference cancellation techniques with better *maximum squared error* performance for modulated interference signals are desired, which are required to ensure the stability and convergence of channel equalizer taps. The next section describes one such approach, which will be called, the "dual adaptive filter approach", or the "two adaptive filter approach".

3.2.3 Dual adaptive Filter approach

In order to get better MSE performance (and consequently a better overall system performance) for non-sinusoidal interferences, a technique called dual adaptive filter approach [10] is used. Two-stage adaptive filtering process is required to cancel narrow band interference from a wideband signal. The first stage uses the time varying behavior of the normalized least mean square (NLMS) adaptive filter with a large step size to produce a Doppler mitigated replica of the interference. The second stage uses NLMS with small step size as an approximation to the ideal Wiener filter to correct the phase and magnitude of the Doppler mitigated interference and produce an interference estimate suitable for cancellation. Fig. 3-5 shows the two stage adaptive filter process encapsulated as $h(n)$. The reference $r(n)$ is a Doppler shifted version of the interference. For sinusoidal interference, a sinusoid works as $r(n)$. For FSK modulated interference, sinusoidal signal could still be used as $r(n)$ companioned with a reasonable MSE output.

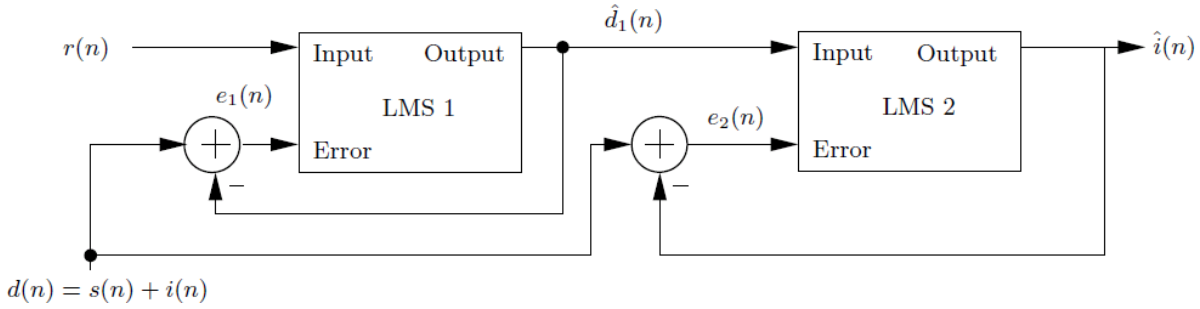


Fig. 3-5 The two adaptive filter approach to interference cancellation.

For single stage AF and sinusoidal interference and reference signals, we have

$$\begin{aligned} i_n &= A_i e^{j\phi_i} e^{j\omega_i n} \\ r_n &= A_r e^{j\phi_r} e^{j\omega_r n} \end{aligned} \tag{3.4}$$

So the interference can be rewrite as

$$i_n = A_i e^{j\phi_i} e^{j\omega_i (n-1)} e^{j\omega_i} = e^{j\omega_i} i_{n-1} \tag{3.5}$$

Let's assume a hypothetical NLMS input vector $\tilde{u}_n$ consisting of the immediate past of the interference signal and a single sample of the reference. The output of an LMS filter is

$$\hat{d}_n = \tilde{w}^H \tilde{u}_n = \tilde{w}^H \begin{bmatrix} i_{n-1} \\ r_n \end{bmatrix} \tag{3.6}$$

Using (3.5) we can produce an NLMS output that cancels the interference, as follows

$$\hat{d}_n = \tilde{w}^H \begin{bmatrix} e^{-jw_i} i_n \\ r_n \end{bmatrix} = \begin{bmatrix} e^{jw_i} 0 \end{bmatrix} \begin{bmatrix} e^{-jw_i} i_n \\ r_n \end{bmatrix} = i_n \tag{3.7}$$

From the adaptive filtering point of view, the desired signal can therefore be written as

$$d_n = \frac{A_i}{A_r} e^{j(\phi_i - \phi_r)} e^{j(\omega_i - \omega_r)n} r_n + s_n \tag{3.8}$$

For maximum NLMS stepsize, i.e. μ = 1, the *a posteriori* weight vector forces the *a posteriori* error to zero. This implies

$$\hat{d}_n = d_n \tag{3.9}$$

Comparing (3.8) and (3.9), we note that when the SIR is low, the *a posteriori* adaptive filter weight tracks the hypothetical – and optimal – time-varying weight in (3.8).

With the latter time-varying weight, the adaptive filter operation amounts to a modulation of the reference, together with a correction in its amplitude and phase, in an attempt to cancel the interference signal. Under the above circumstances, the error incurred by the adaptive filtering operation results from the fact that the tracking is very good *a posteriori*, i.e. mostly lag error is incurred. An expression for the steady-state a priori error can be found which includes the dependence on stepsize $\bar{\mu}$.

$$e_n = A_i e^{j\phi_i} e^{j\omega_i n} \frac{1 - e^{-j(\omega_i - \omega_r)}}{1 - (1 - \bar{\mu}) e^{-j(\omega_i - \omega_r)}} = i_n \frac{1 - e^{-j(\omega_i - \omega_r)}}{1 - (1 - \bar{\mu}) e^{-j(\omega_i - \omega_r)}} \tag{3.10}$$

The first filter is calculating a good estimate of the interference in spectral terms, $\hat{d}_1(n)$. The second filter then locks in the amplitude and phase of the interference. The latter provides a signal which can be used for interference cancellation in the form of $\hat{\imath}(n)$. The key point to note here is that the first adaptive filter uses a large step size (for instance "1"). This enables it to rapidly adapt to any changes in the interference signal, such as frequency shifts. The second adaptive filter functions in a more normal setup with a small step size, to ensure that the notch of that filter around the interference frequencies in thin enough, resulting in least possible distortion to our signal. The effect of step size of the second adaptive filter on the MSE and BER has been explored, under a sinusoidal interference. This is shown in Fig. 3-6 and Fig. 3-7. As can be seen from the plots, a small step size in the second adaptive filter is generally better. Given a maximum tolerable MSE value, the step size for the second stage is bounded. The MSE dependence on the step size of this stage is almost linear. Usually, it is not desirable to use step size of more than 0.03. Since the BER will significantly increase beyond this point.

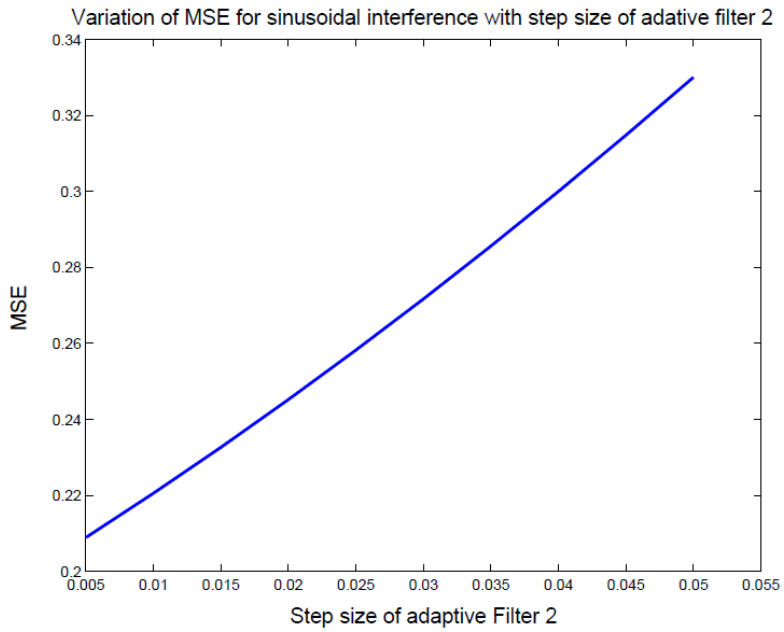


Fig. 3-6 Effect of step size of second AF on the MSE with sinusoidal interference.

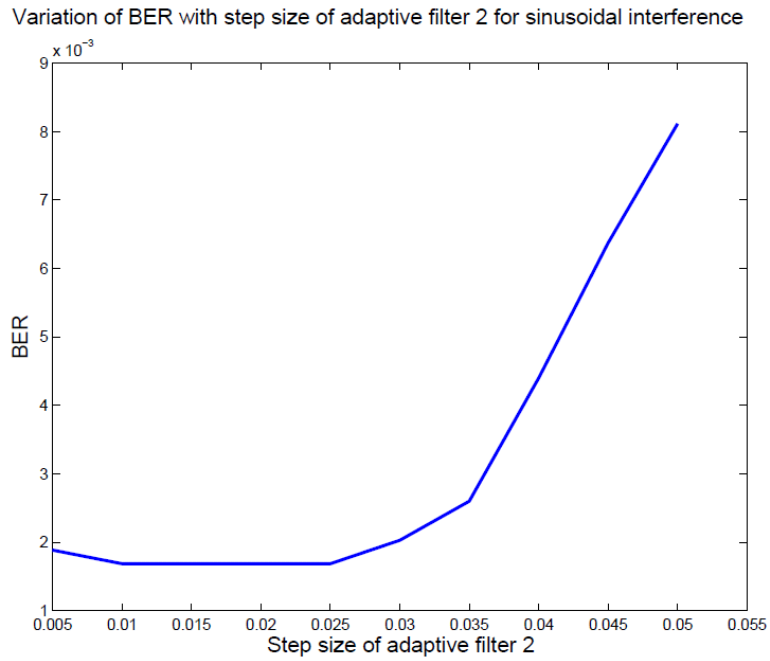


Fig. 3-7 Effect of step size of second AF on the BER with sinusoidal interference.

3.2.4 Performance Comparison of the Two Approaches

In the following subsections the two approaches to interference cancellation are compared from three different angles in the absence of any propagation channel.

3.2.4.1 Variation of MSE with SIR

As pointed out earlier for sinusoidal interferences, the single filter approach to interference cancellation works better. This is shown in Fig. 3-8. For the two filter approach, the sinusoidal interference does not give performance that the single filter approach offers, whatever be the SIR. In the low SIR regime, the single adaptive filter approach provides an MSE that is only one half of the dual filter. While hardly varies for the dual filter approach, the MSE for single filter could be observed to drop fast in the high SIR environment.

For modulated interference, at symbol edges the spikes in the error are huge, hence it is not informative to look at the MSE for comparison. It is however still possible to look at the BER for the two approaches under FSK interference. It is obvious that BER and MSE are highly correlated performance measures.

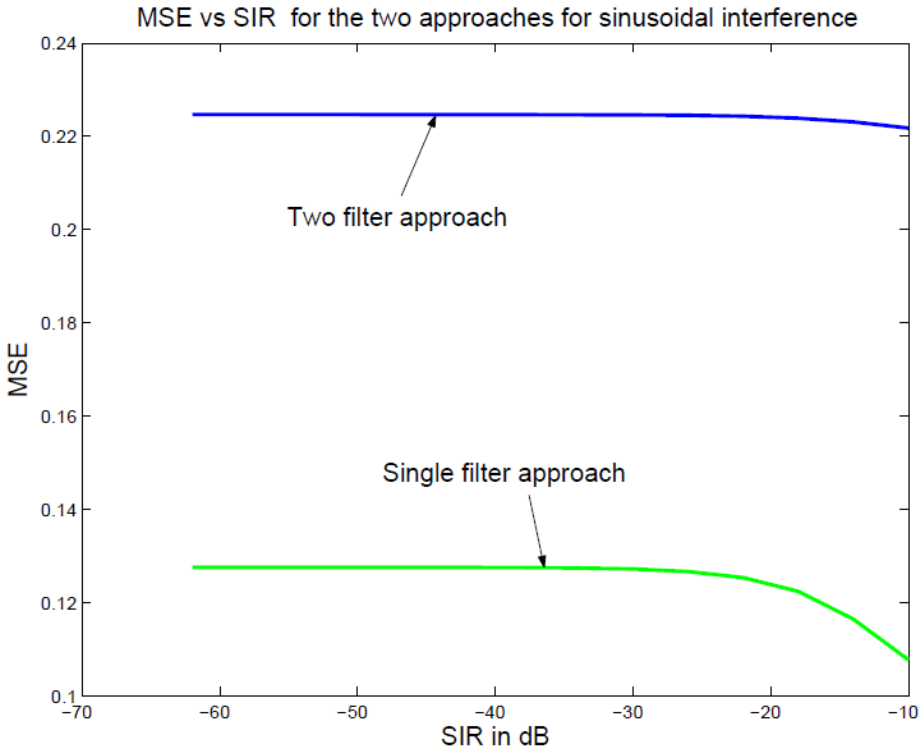


Fig. 3-8 MSE vs SIR for interference cancellation approaches with sinusoidal interference.

3.2.4.2 Variation of BER with SIR

For sinusoidal interferences, Fig. 3-9 shows the plot of BER vs SIR for the two approaches to do interference cancellation. The single filter approach gives zero error for high SIRs but the SIR-independent two filter approach performs much better at lower SIRs.

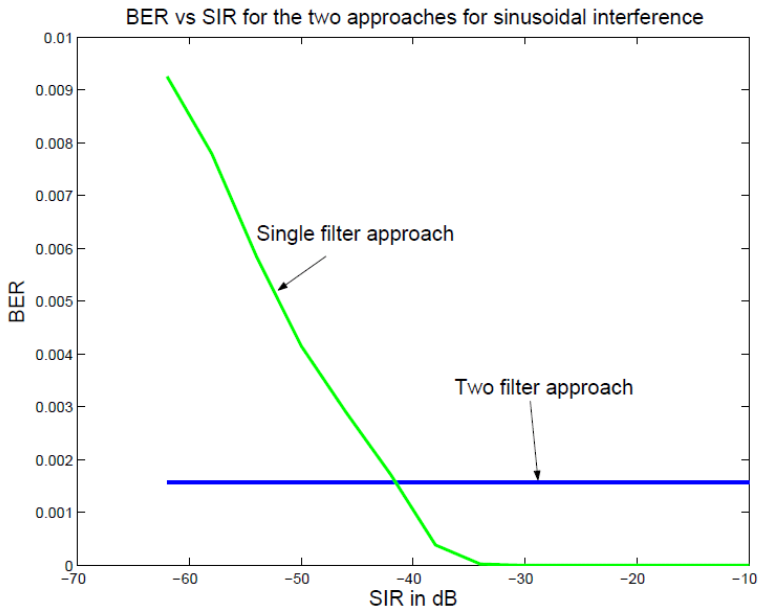


Fig. 3-9 BER vs SIR for interference cancellation approaches with sinusoidal interference.

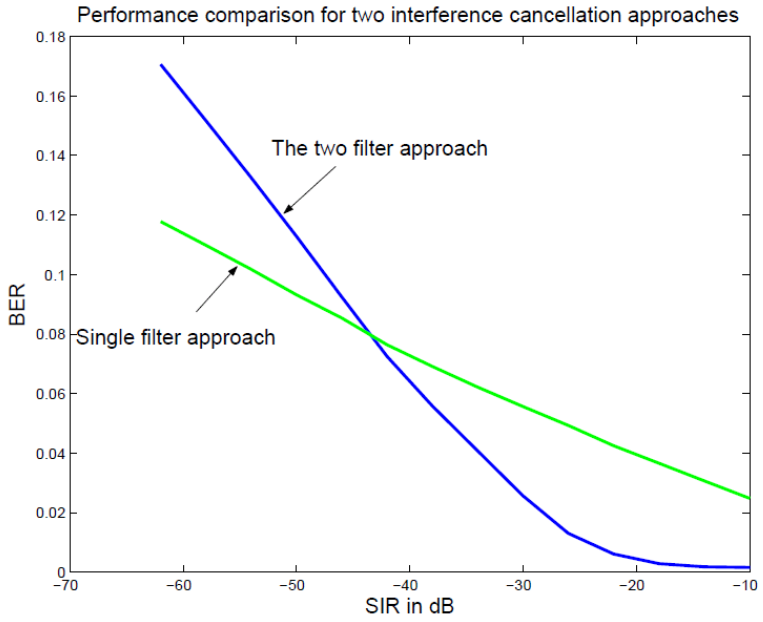


Fig. 3-10 BER vs SIR for interference cancellation approaches with FSK interference.

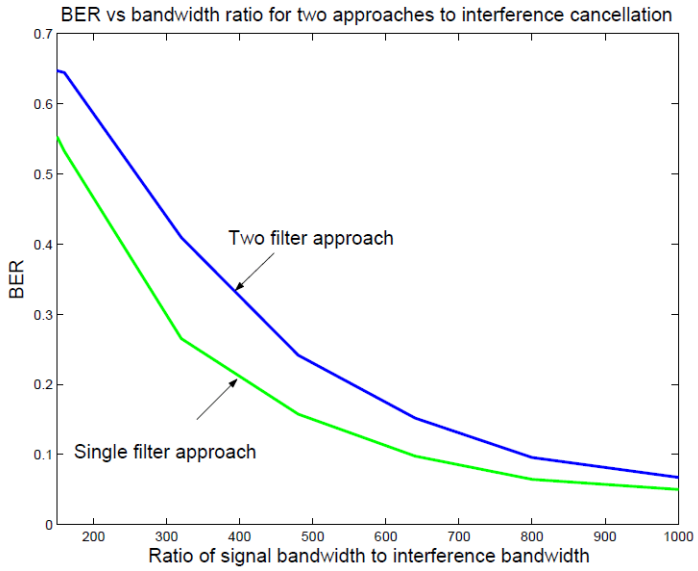


Fig. 3-11 BER vs ratio of signal bandwidth to interference bandwidth with FSK interference.

For FSK interference, Fig. 3-10 shows the comparison of BER vs SIR for the two approaches. The ratio of signal bandwidth to interference bandwidth is 1000 when plot the figure. It can be seen that, for modulated interference, the single filter approach performs better at lower SIRs and is less sensitive to SIR as compared to the two filter approach. However, the spikes created in error are bigger for the single filter approach.

3.2.4.3 Variation of BER with Bandwidth Ratio

Fig. 3-11 shows the curve for BER performance of the two approaches as the ratio of signal bandwidth to interference bandwidth for FSK interference is changed. Observed that the single adaptive filter approach works better at all ratios, the SIR is -37*dB* in this figure.

3.3 Equalizer

The channel model has already been shown in Fig. 3-1. Details are to be discussed when the dispersive portion of the channel, $c(t)$, is Rayleigh Fading with a time variation given by the one corresponding to a classical Jakes Doppler spectrum (uniform isotropic angle of arrivals). We have chosen the number of taps to be 5 (the inter-symbol interference is from the past 4 symbols). The taps' powers are given by an exponential power delay profile (PDP). Note that in most cases the sampling rate will not coincide with the tap delays. In those cases we can convert the channel PDP with tap delays not coinciding with sampling intervals, to an equivalent PDP with the desired sampling rate by using Fourier transform and inverse FFT [16].

In this section, we will describe the two types of equalizers used in our system, the linear LMS adaptive equalizer and the nonlinear LMS-adapted decision feedback equalizer.

3.3.1 Linear Adaptive Equalizer

For mitigating the inter-symbol interference, an LMS adaptive equalizer is used in the system. The LMS equalizer takes as input, the interference cancelled, but ISI containing signal, $\hat{y}_s(n)$, and gives as output the estimate, $\hat{s}(n)$, of the transmitted signal. The equalizer works with a training sequence intermittently to follow the changes in the channel, and then for a majority of the time works in a tracking mode with decision feedback. The basic structure of the equalizer is shown in Fig. 3-12.

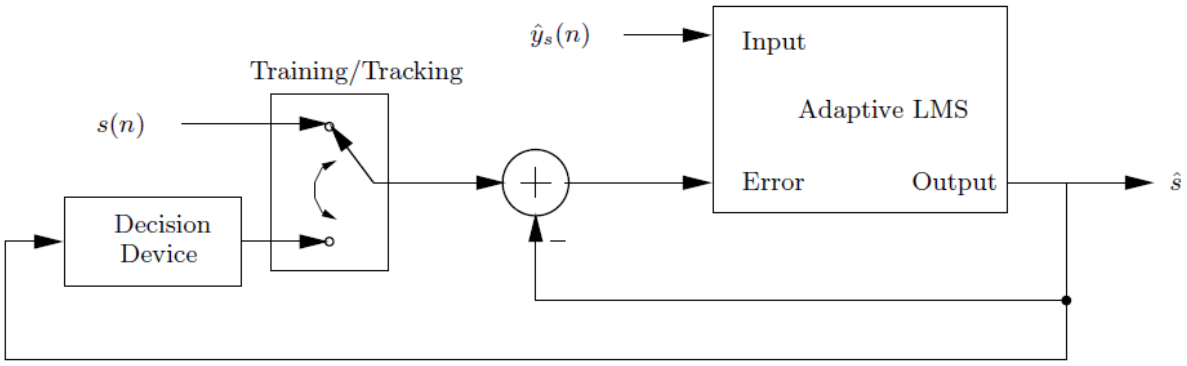


Fig. 3-12 Structure of a linear LMS adaptive equalizer used to remove ISI.

During the training mode, the receiver knows the transmitted symbol sequence. After a specified amount of time, it is switched to tracking mode. The decision device in this case (a QAM signal is used as $s(n)$, and was made of a QAM demodulator and a QAM modulator. Note that it needs to train repeatedly and this frequency is directly proportional to the Doppler spread of the wireless channel. Note that in a real world system there will be carrier synchronization and timing issues which are not considered here. For simplicity these issues are assumed to be taken care of perfectly.

3.3.2 Decision feedback equalizer

In order to try out an alternative equalization scheme and compare system performance, we also implemented a decision feedback equalizer (DFE).

Fig. 3-13 shows the basic structure of the decision feedback equalizer. The DFE consists of a feedforward equalizer, a decision device and a feedback equalizer using past decisions. The use of the decision device, usually including a quantizer, causes the equalizer to be non-linear, even

though the feedforward and feedback filters are usually linear. The equalizer also has a training mode in which the known symbols are substituted for the decisions. The DFE is subject to error propagation in a worse way than error propagation in the linear equalizer. If the feedback portion of the DFE has *N* taps, then the DFE requires not only the previous decision, but the previous *N* decisions. The adaptation for the linear LMS requires only the previous decision. Hence, once the DFE has made a few bad decisions in a row, it could be hard to get out of this stretch of errors without training. The linear LMS filter, on the other hand, requires only one right decision to move the filter in the right direction again.

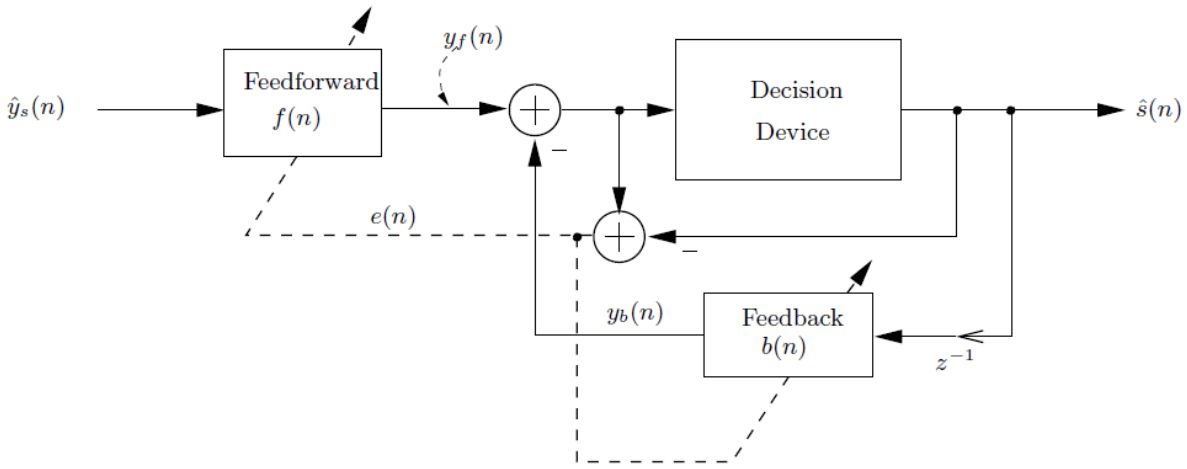


Fig. 3-13 Structure of an LMS-adapted DFE.

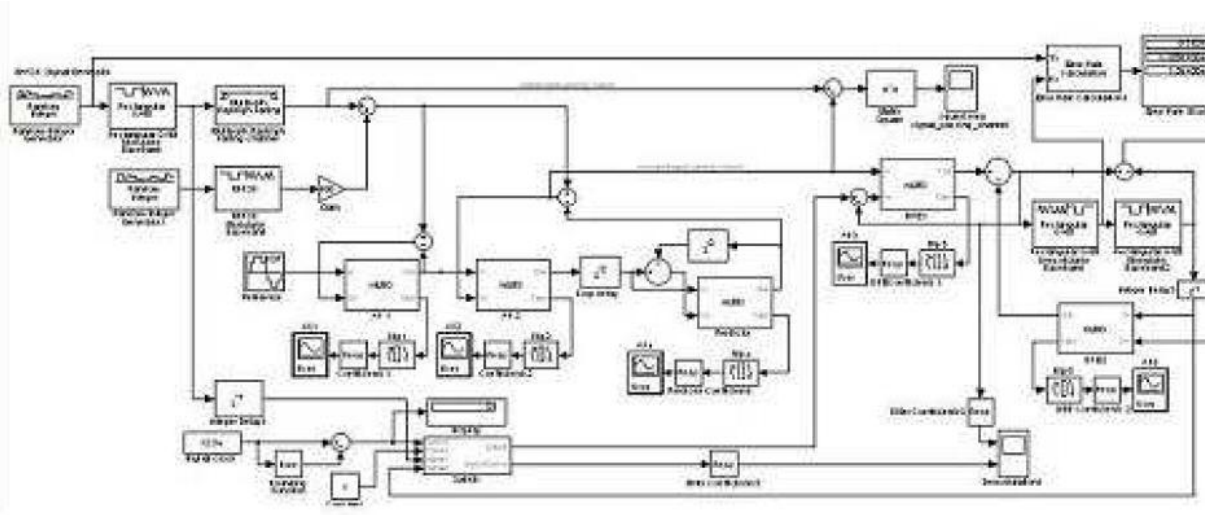


Fig. 3-14 Snapshot of the implementation (with all the blocks) in Simulink.

The decision feedback equalizer can be very powerful in all SIR and high SNR situations as will be seen in the next section when combined all the blocks of the system and look at overall system performance.

Six taps were used in the feed-forward filter, and seven taps in the feedback filter. The algorithm for adaptation in both filters was NLMS.

3.4 Combining Interference Cancellation and Equalizer Blocks

Fig. 3-14 shows the snapshot of the system built in Simulink. Note that for the overall system, the two-adaptive filter approach is always used for interference cancellation due to stability problems caused in the single filter approach equalizer. The next two sections analyze the overall system performance when all the blocks are combined together. The performance of the two channel equalization techniques are compared, with the dual adaptive filter used for interference cancellation.

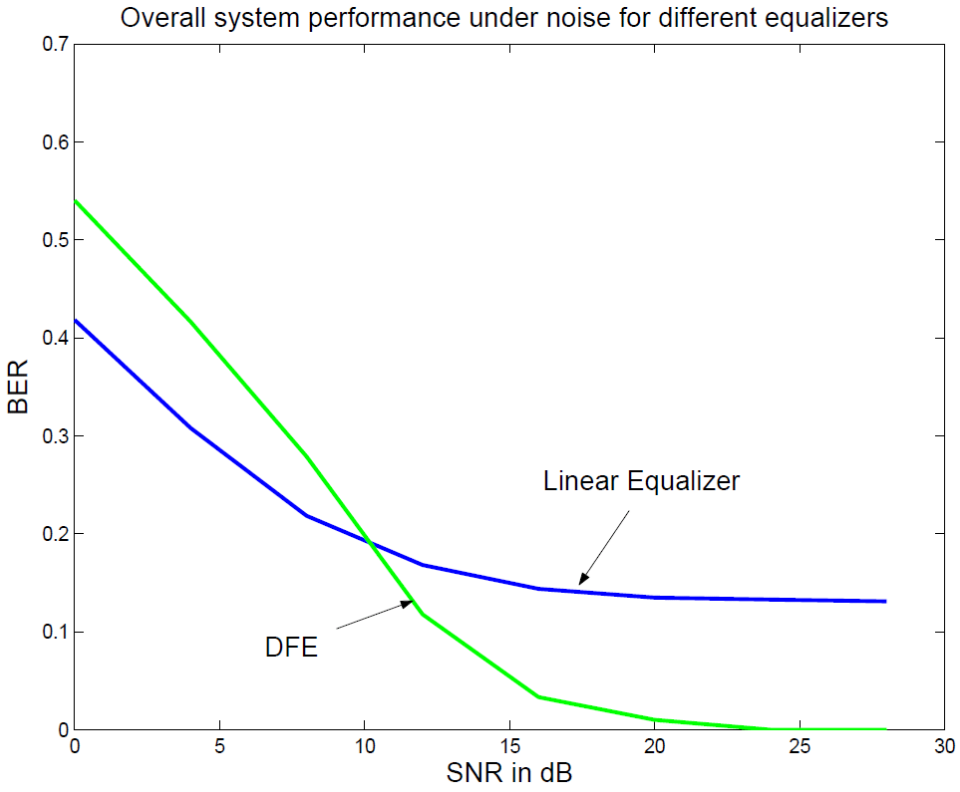


Fig. 3-15 Overall system performance for two equalization approaches.

3.4.1 Performance in the presence of noise

The performance of the overall system under noise by using the two equalization techniques was compared. Fig. 3-15 shows the overall system performance for the two approaches of equalization. The SIR is -37*dB* for this diagram, and the interference is sinusoidal. The interference cancellation approach is the dual filter approach. This happens because of the error propagation effect is associated with DFEs.

One can clearly see that at higher SNRs the DFE outperforms at linear equalizer. The reverse is happening at lower SNRs.

3.4.2 Effect of SIR on overall system performance

Fig. 3-16 shows the performance of the full system using different approaches of channel equalization versus SIR. It is clear from the figure that DFE is the clear winner at all SIRs. The system is under zero noise. It is believed that DFE removes some of the residual interference as well while equalizing the channel. The interference used is sinusoidal.

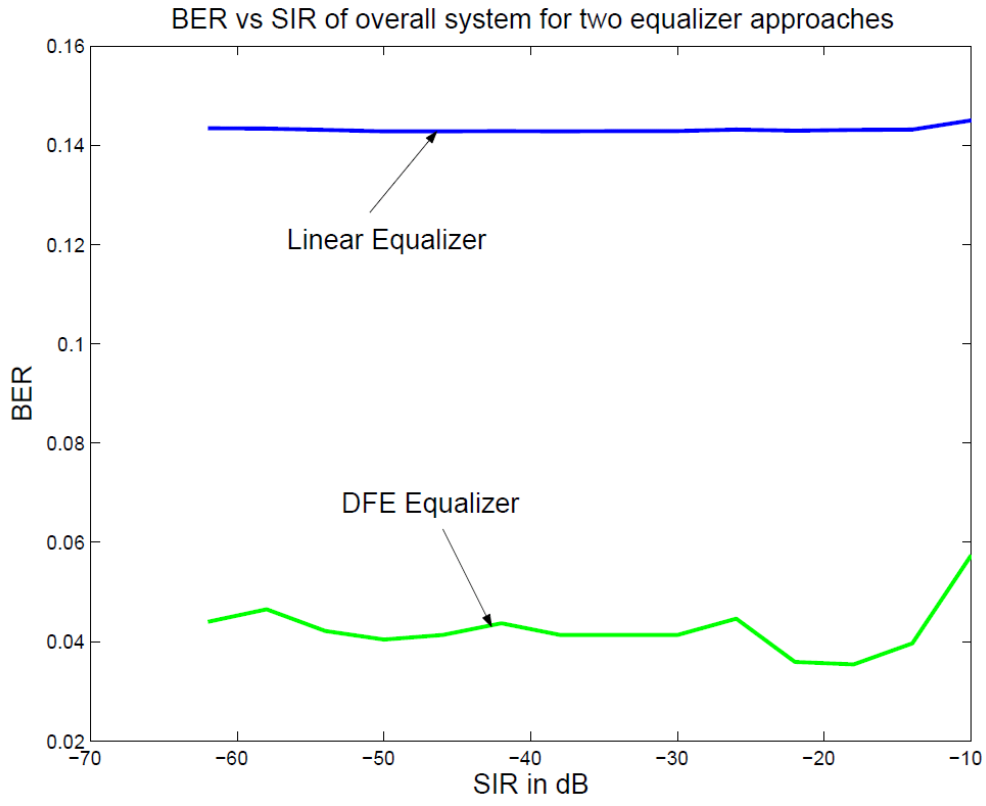


Fig. 3-16 Overall system performance for the two approaches of equalization.

3.5 Conclusion

In this chapter it has been shown that, even without channel coding, the BERs being achieved by the system are decent under very low SIR scenarios. With channel coding, any required non-zero probability of error can be achieved. It has therefore been concluded that a dual adaptive filter approach to interference cancellation followed by a DFE approach to channel equalization gives the best overall performance for an interference cancellation system for Cognitive Radios when the interference is narrow band. This work provide a solid background for further analyzing of more types of interferences and adopting approaches like spread spectrum to avoid interference.

Chapter 4

High Speed ADC

The high-speed (~GHz) medium-resolution low-power ADC's are the key components to resolve the high dynamic range problems in highly flexible, very wideband radio front-ends such as required in cognitive and software defined radios [1]. Using these techniques, a dynamic range on the order of 70*dB* can be achieved with multiple ADC's that have a moderate resolution of about 5 to 6 bits.

Also as wireless data rates increase into the multiple gigabit/sec range in the millimeter wave regime (e.g. 60 GHz), ADC's with bandwidths of GHz and higher are required[17; 18; 19], which again only need moderate resolutions since the interference problem is not at issue at those frequencies. These applications typically have severe power and cost constraints which can be achieved by using a standard CMOS processes.

We will present strategies and techniques to optimize the power and area efficiency of such an ADC using a power efficient semi-closed loop, successive approximation algorithm executed with asynchronous processing. A 65nm low leakage low power (LP) CMOS process is used with particular attention paid to increase the conversion speed of the asynchronous feedback loop, which is complicated by the severely limited overdrive voltages due to the 1.2 Volt voltage supply and the high threshold of the transistors. Metastability issues are carefully addressed and an error correction algorithm is developed which can remove any potential degradation. This algorithm, however, requires constraints in the design which are carefully discussed. In particular, the critical loop is composed of intervals which have variable delay (the comparator decision) and other portions which are kept constant (e.g. DAC settling).

The prototype design has a sample rate of 1GS/s ADC which achieves an ENOB of 5.0 at 1GS/s with a power consumption of analog and digital processing of 6.7mW. To achieve the Gsample/sec rate at low power, two ADC's were interleaved, with each ADC only occupying an area of $0.35\text{x}0.16\text{mm}^2$ for a total area of 0.11mm^2.

4.1 ADC Architecture

A conventional flash ADC (Fig. 4-1a) might seem to be the preferred choice for the above specifications of high speed and moderate resolution, considering its low latency and high-conversion speed since each conversion is completed in a single clock cycle [18; 12; 20; 21][22]. However, flash ADC's suffer from an exponential dependence of power and area on resolution and also has relatively difficult calibration required for the many parallel paths. It becomes ever more difficult as the process variation increases with technology scaling. In comparison, a successive approximation register (SAR) ADC only requires a single path, with one comparator, spreads one conversion over several cycles, and charges or discharges an internal DAC based on the decision made through the previous comparison (Fig. 4-1b)[23]. Because it only requires a single comparator and DAC, the SAR dissipates significantly less power and occupies a smaller area. This characteristic renders the architecture highly scalable and easier to calibrate.

In SAR implementations, as shown in Fig. 4-1b, a reset signal at the comparator is required, which is timed so that a reliable comparison is performed in every comparison cycle. The SA algorithm evaluates the data, generates the corresponding decision and the DAC settles with respect to that decision. In traditional designs, the reset phase should terminate after DAC is fully settled to ensure the evaluation of the comparator is performed on the correct input voltage [24].

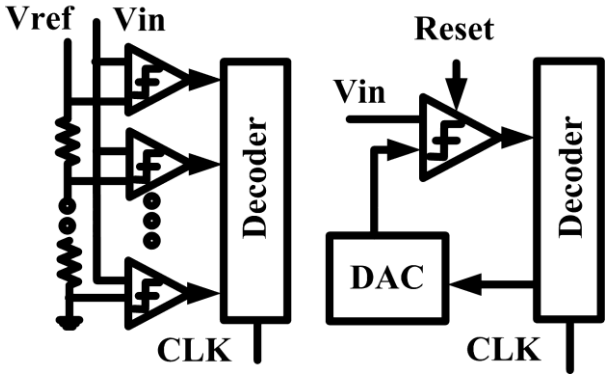


Fig. 4-1 High speed ADC architecture. a) Flash ADC, b) SAR ADC.

4.1.1 Asynchronous Processing

The sequential operation of the SA algorithm has traditionally been a limitation on high-speed applications, because a synchronous approach relies on a clock to divide the conversion phase into equally timed slots as the conversion proceeds from MSB to LSB [25; 26; 27]. This internal clock for an N bit ADC would therefore operate at a frequency of at least N × the sampling clock. Clock generation is less an issue when the ADC is working in a low speed regime, where SAR is traditional used [23; 28; 29], and if only the switching power is considered would require at least N × the clock power of an asynchronous approach in which the sampling frequency sets the highest clock rate. It is estimated that in this design, if it were synchronous, the percentage of the total power for the clocks would rise from 15%, to above 50%.

The high speed internal clock period in a synchronous design is chosen to accommodate the worst case scenario, including the comparator resolving time with a small residue voltage, (usually below $1V_{LSB}$, where V_{LSB} for an N bit ADC is $V_{LSB} = \Delta = V_{FS}/2^N$), the digital delay through the SA algorithm, and the maximum DAC settling time, even though the longest bit cycle seldom falls into this case.

Besides the problem of the high speed internal clock, metastability is a fundamental issue associated with all the ADC's that rely on comparators for conversion. When in a metastable state, the comparator spends an unbounded time on resolving an arbitrarily small input. An error will then be created when the comparator input is below a certain minimum value depending on the design, resulting in a degradation of the effective number of bits (ENOB). Interestingly enough, as will be shown, the use of asynchronous processing with metastability detection allows for a simple SA algorithm extension which can essentially eliminate the errors arising from metastability. This approach allows a design in which the requirement for the comparator speed is reduced by allowing operation in a metastable state once each conversion, thus reducing its power consumption.

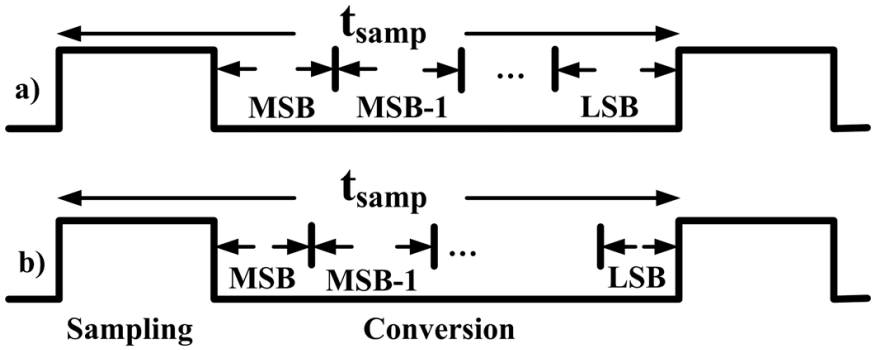


Fig. 4-2 a) Synchronous processing with equally divided bit comparison time. b) Synchronous sampling, asynchronous processing conversion with unequal time interval.

As opposed to a fully asynchronous approach [30], It is important to note that the analog input is actually synchronously sampled at a time interval of t_{samp} , with only the subsequent conversion processing being asynchronous (Fig. 4-2 b). The execution of the SA algorithm precedes from MSB to LSB sequentially (and asynchronously) under control of locally generated *rdy* signals [24].

The asynchronous processing also makes the average total conversion time significantly shorter than using synchronous processing. The SA asynchronous conversion efficiently utilizes the faster comparison cycles for large comparator inputs, since only one of the residual voltages will fall within 1/2 V_{LSB} by nature. The amount of conversion time savings between asynchronous and synchronous processing, as previous research [24] has shown, is a function of the number of bits, the profile of input-dependent residual voltages and the allowed ENOB degradation.

4.1.2 Architecture

Fig. 4-3 shows the proposed architecture. The external square-wave clocks initiate a tracking and settling phase followed by the SA comparisons (Fig. 4-4). The input is sampled by the capacitor array with effectively low input capacitance. A series non-binary C-2C capacitive ladder network is used [24]. The total input capacitance of the ladder is independent of the number of ADC bits due to the series connection. The input capacitance is significantly reduced compared to the conventional approaches of geometrically scaled or unitary capacitor arrays and enables an extremely high input bandwidth. The disadvantage of the series capacitor array is that the actual ratio of the capacitor network highly depends on the capacitance ratios and the parasitic capacitors associated with the interconnect circuitry, thus requires extra effort on layout and calibration.

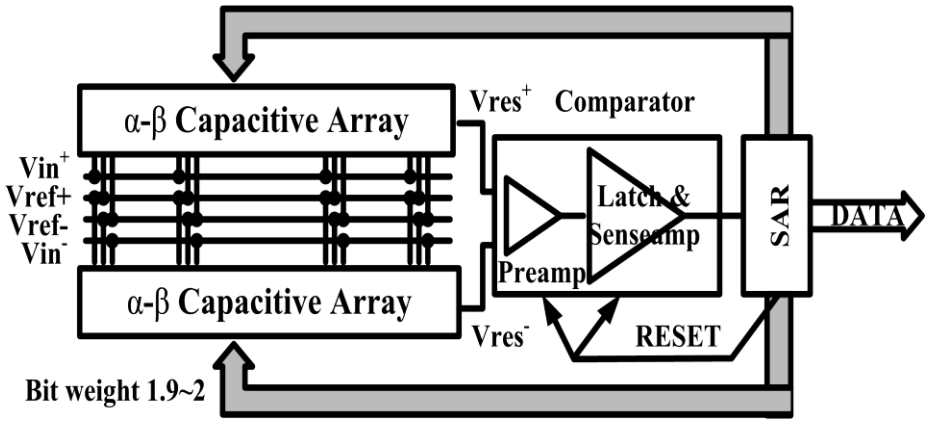


Fig. 4-3 Time interleaved asynchronous ADC architecture.

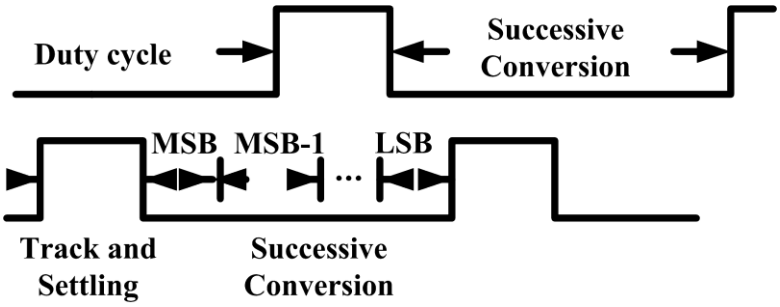


Fig. 4-4 Internal opposite phase clocks.

After tracking and settling phase of the input signal, the asynchronous SA proceeds from MSB to LSB, utilizing only one comparator. The single comparator design avoids the offset calibration between multiple comparators required in traditional flash ADC's. The offset from the comparator therefore becomes a global offset and this DC offset that can be digitally removed. A completion or ready (*rdy*) signal is generated after completing the comparison. The corresponding rising edge of *rdy* triggers the dynamic asynchronous SA logic. As shown in Fig. 4-5, two major operations are involved to execute the algorithm initiated by the rising edge of the *rdy* signal: 1) a pulse is generated which controls the duration of the reset phase, so that the comparator could reset itself after each evaluation; 2) a set of sequencer signals are driven, each with monotonic switching, to provide multiple-phase clocks for the switch logic and bit caches to store the correct corresponding bit comparison results. The charge redistribution network, which is formed by the capacitor array, functions as a digital to analog converter (DAC) to subtract or add a fraction of the reference voltage, with the voltage increment of the DAC being controlled by the switch logic.

The duration of the *rdy* signal is set such that the capacitor array is settled reliably and the full reset of the comparator is finished, thus the evaluation could start. Dynamic logic is used with the transistors sized optimally using logical effort [31] for dynamic gates to enhance the asynchronous processing speed.

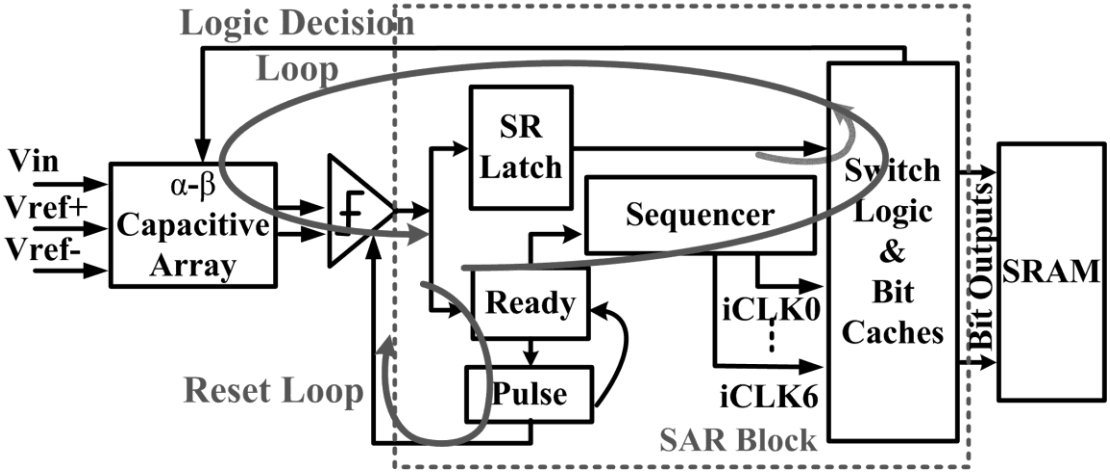


Fig. 4-5 Single-ended ADC architecture -- details of SA blocks and data paths.

In order to meet the speed specification of 1GS/s, two parallel converters have been time interleaved, since this approach is especially attractive when a single ADC area is small, as in this design. Interleaving two ADC's using non-overlapping clocks achieves twice the sampling rate at twice the power and area with a slight additional penalty of power and area for the parallel path synchronization and calibration.

4.2 Metastability Issue and Error Correction

A well-known issue related to SAR ADC's and flash ADC's is the metastability phenomenon. It is due to the occasional inability of a comparator to resolve a small differential input into a valid output logic level [32; 33]. This subtle characteristic of comparators can cause large errors (sparkle codes) in ADC's if not dealt with effectively. The probability of errors due to metastability increases exponentially with sampling frequency [33].

The residual voltage at bit i, V_{res_i}, is defined the sampled input minus the summation of all the voltage steps up to that bit.

$$V_{res_i} = V_{in} - \sum_{k=1}^{i-1} V_{step_k} \tag{4.1}$$

The resolving time of the comparator strongly depends on V_{res_i} as will be shown in Section 4.3 . Unfortunately, over-designing the comparator to reduce the range of the metastable state results in increased power consumption and larger area.

The conversion time of the N bit ADC has the constraint, such that N comparisons, (N-1) SA algorithm decisions, DAC settling, and finally sampling of the input, should be accomplished in one clock cycle. If the digital delay through the SA algorithm logic, $t_{digit\,al}$, and the settling time for the DAC, t_{DAC}, is fixed, the constraint becomes:

$$t_{samp} \geq (N-1)\left[t_{DAC} + t_{digital}\right] + \sum_{i=1}^{N} t_{comp_i} + T_{sw} \tag{4.2}$$

where t_{samp} is the total clock period, $t_{comp\,i}$ is the resolving time spent on the comparison at bit *i*, and T_{sw} is the sample pulse width.

The nature of the SA algorithm requires that there is going to be *one*, and only *one*, bit conversion for which $V_{res} \leq V_{LSB}/2$. Therefore, if the evaluation for each bit is reliable, only one conversion will be in the metastable state. Defining the threshold comparison time, t_{comp} (V_{comp_th}), as the maximum delay through the comparator to ensure a full N bit output when a minimum input residue voltage is at V_{comp_th}. Then if $V_{comp\_th} \leq V_{LSB}/2$, when $V_{res} > V_{LSB}/2$, no metastability will occur. However, when $V_{res} \leq V_{LSB}/2$, an extended time will be required for the comparator to evaluate. It is possible that if the comparator input is below V_{comp_th}, the comparison time could be extended so much that not all bits can be determined. As opposed to a flash ADC or synchronous SAR, which would generate an error, an asynchronous

SAR simply produces an output that has less than N bits. By designing the comparator to have a maximum delay of t_{comp} ($V_{LSB}/2$) for the slow corner, it is true across all process corners that an output of less than N bits can be inferred to mean the V_{res} for one of the evaluations was less than $V_{LSB}/2$. Based on this knowledge, a simple extension to the SA algorithm can be made that can yield correct conversion code values, even if the comparator enters metastability (i.e. when the output has less than N bits).

If the metastable state is sufficiently long that there are no additional bits output after the metastable state is entered, then the SA algorithm extension can be implemented without any additional on-chip circuitry. This off-line version starts by detecting that only M bits of data are output from the asynchronous loop (with $M<N$), so that we know the input to the comparator must be less than $V_{LSB}/2$ from the voltage level defined by $\sum_{i=1}^{k} V_{step\_i}$ ($k = 1,2 \ldots M$). We can therefore determine the correct voltage level (within $V_{LSB}/2$) since we assume that it is the last bit evaluation which took an extended time. A simple off-line algorithm is to just fill in the missing end bits with the complement of the last outputted bit. This algorithm was used in all the results presented.

For instance, in our 6-bit ADC with $V_{FS} = 1V$, if $V_{in} = 0.5V - V_{LSB}/16$, then $V_{res} = V_{LSB}/16$, and the comparison of the first bit will be extended, since $V_{LSB}/16 << V_{LSB}/2$. If it is assumed then that only one bit is evaluated, the output of the ADC is a single "0". After the algorithmic extension described here, the code becomes the correct value 011111.

There is however an improvement on this algorithm that requires additional on-chip circuitry, which covers the case where one bit comparison takes a long time due to a small V_{res}, but leaves sufficient time for subsequent bit evaluations. This means the assumption that the last bit output was the one within $V_{LSB}/2$ of the decesion level was not true. The actual metastable bit can be detected by creating a delayed version of the *Eq* falling edge signal. The delay t_{d_comp} is slighter longer than t_{comp} ($V_{LSB}/2$). When metastability (or more precisely when a long comparison time) occurs, both outputs of the comparator drop towards GND. An XOR output remains "0" unless the comparator outputs split. The delayed falling edge signal is used as an input control signal to a falling edge triggered register which latches the XOR output (Fig. 4-6 a). The register's output, DM<i>, is precharged to 1 and will be discharged to 0 if bit i is in metastable state. DM<i> ($i = 0,1 \ldots 5$) is further converted to a corresponding MUX output of 1 to 6.The *rdy* edge counter (REC) counts the actual evaluated number of bits (Fig. 4-6 b). In a 6-bit ADC, the error correction flag (EC_flag) could be generated by comparing REC and the MUX output. When the comparator managed to resolve at least another bit after a metastable state incurred, MUX output < REC, EC_flag is 0, thus the missing bits are filled the same as the last evaluated bit from the ADC. If MUX output=REC, EC_flag is 1, the comparator barely finished a metastable bit, thus the missing bits should be the complement of the last evaluated bit. If MUX output > REC, EC_flag is 2, the comparator is still converting the bit in metastability, an arbitrary filling of 011⋯1 or 100⋯0 is added as the missing codes.

Following our example above, instead of the last bit output being in metastability, we will take the case in which the comparator is sufficiently fast that two more bits are evaluated after an initial long comparison time. If the resulting output is then "011", REC = 3, MUX output = 1, and EC_flag = 0, the code after the correction is then again the correct value of 011111.

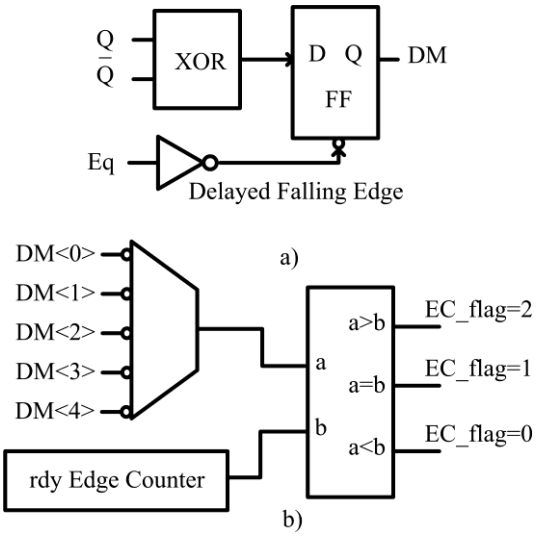


Fig. 4-6 a) DM register. b) Error correction circuit diagram to solve metastability.

Although this example is only for the MSB being in a metastable state, the algorithm works for all cases where metastability could happen at any arbitrary bit. Therefore metastability need not degrade the Effective Number of Bits (ENOB) when the comparator is designed to just meet the minimal timing requirement for $V_{comp\_th} = V_{LSB}/2$.

4.3 Circuit Implementation

This section describes the design issues involved in each component of the critical delay path, including $t_{digital}$, t_{DAC} and t_{comp} . Moreover, to further enhance ADC speed, possible overlaps between t_{comp} and $t_{digital}$, also t_{DAC} and t_{comp} (Fig. 4-7) have been exploited.

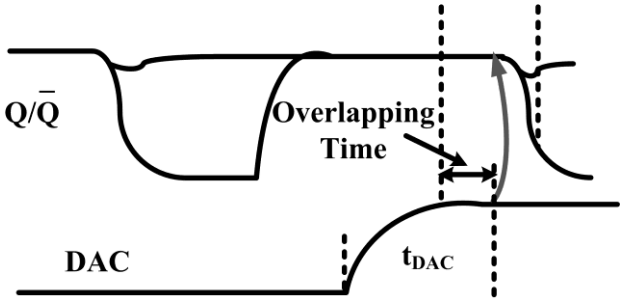


Fig. 4-7 Time overlapping between the comparator and the DAC.

4.3.1 Critical Path and Reset Loop

After each comparison, based on the buffered comparator output and the multiple-phase clocks, the switch logic determines the DAC capacitors to be switched which are then connected to either the positive or negative reference voltage. The DAC capacitor is allowed to resettle and then the next comparison starts.

There are two signal loops in the processing, the *logic decision* loop and the *reset* loop, as shown in Fig. 4-5. The logic decision loop executes the SA algorithm and the reset loop resets the comparator, the *rdy* signal, and other logic circuits, before the next bit cycle. Compared to the previous work [24], the reset loop in this design is semi-closed, in which a *rdy* triggered pulse, is used to reset both the comparator and the *rdy* signal itself. This semi-closed loop circuit facilitates a much earlier data reset, and gives extra time for the comparator to setup before making a reliable decision which increases the overall speed of the conversion. Also, using two different reset signals, *rdy* and *Eq*, in the two stages of the comparator, enhances the comparison speed by allowing the pre-amplifier to increase the voltage difference at the input of the dynamic latch, which will be further discussed in Section 4.3.3 .

Starting each bit cycle with the *rdy* signal, the critical delay is composed of the digital delay through the SA algorithm, $t_{digital}$, the DAC settling time, t_{DAC}, and the resolving time spent on the comparison, t_{comp} (Fig. 4-8). While$t_{digital}$ and t_{DAC} are designed to be relatively constant over each bit cycle, the comparison time is highly variable since the comparator resolving time strongly depends on its differential input voltage. To remove any memory effect between bit cycles, the comparator and *rdy* signal are reset, erasing the last comparison by pre-charging the differential outputs Q and $\overline{Q}$ to the same voltage and discharging the *rdy* signal to "0".

The comparator switches between two modes, reset mode and compare mode. As soon as the comparison is completed and the differential data has been reliably latched, the comparator turns into reset mode. The reset of the comparator is performed simultaneously with the decision logic and the DAC. An adequate DAC settling time is allowed to achieve a reliable comparison signal at the end of the reset phase, and the comparator switches back into the compare mode.

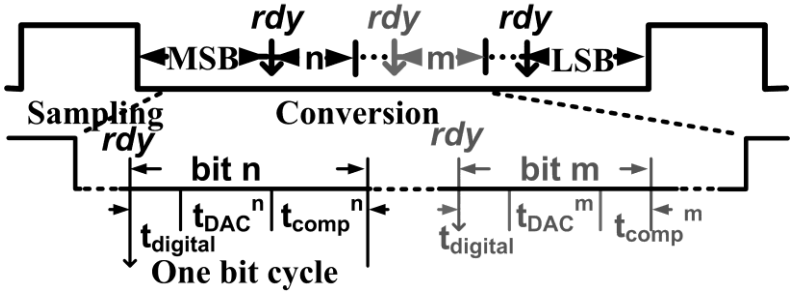


Fig. 4-8 rdy signals and critical delay in each conversion bit cycle.

Timing to pull down the *rdy* is designed to insure there is enough time for a stable DAC output. In addition, a key function of the *rdy* signal is to hold the pre-amplifier in the reset phase. The reset switch $M6$ (Fig. 4-9) that equalizes the pre-amplifier's outputs is designed such that the reset time of the pre-amplifier is shorter than the time required for subsequent charge redistribution.

4.3.2 Comparator Design

The comparator is composed of two-stages, a pre-amplifier followed by a dynamic regenerative latch [34] as shown in Fig. 4-9 The pre-amplifier gain is set to be $6dB$ based on a Monte-Carlo simulation over process, so that the pre-amplifier can accommodate a 3-σ gain error while allowing the comparator to respond to a minimum differential input of V_{LSB} , with V_{FS} the full scale voltage of 1 Volt. The pre-amplifier is automatically biased during the sampling phase by connecting a pair of switches (Fig. 4-9), which are controlled by a delayed sampling clock, at the input and output of the pre-amplifier. To keep all devices in saturation, a cascode current source is avoided, due to the limited headroom available with the low supply voltage of 1.2 V. A simple current source is implemented to minimize the V_{ds} drop on the tail current source. V_{dsat} of the differential pair is designed to be slightly less than $100mV$ to allow a minimum common mode voltage of $450mV$, as well as maintain a reasonable g_m/I_d ratio to improve the pre-amplifier's efficiency.

The necessary wide input bandwidth for the pre-amplifier could be achieved using poly-resistors to provide sufficient gain without the voltage drop of small W/L PMOS loads that is required to achieve the same gain. During auto biasing, a voltage drop of $I \times R_D$ is required from the supply, which is substantially less than $V_{th} + V_{dsat}$ of the PMOS's. Multi-finger poly-resistors provide good matching between *outp* and *outn*, and are therefore used for R_D's. This design yields a pre-amplifier with a *GBP* of around 40GHz.

$M3$ and $M4$ in Fig. 4-9 are used to separate the pre-amplifier and the regenerative latch, so the charge from the data logic levels injected back to the input capacitor array is minimized [35].

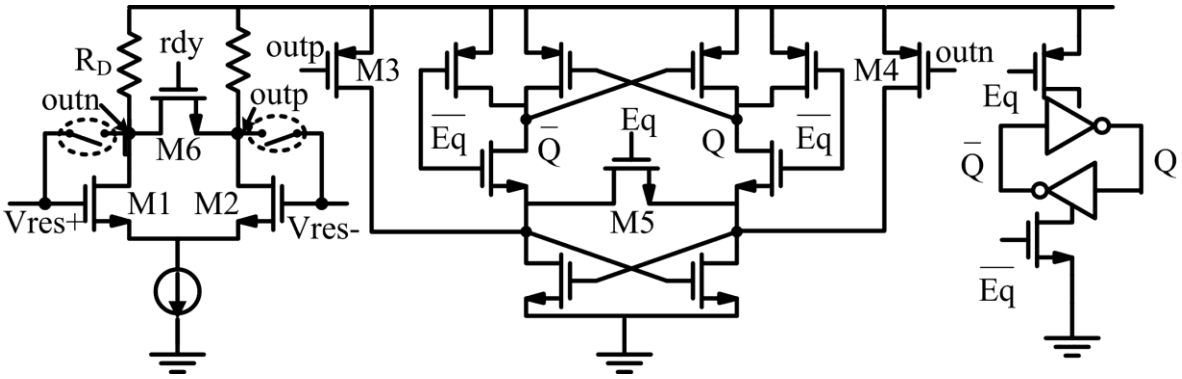


Fig. 4-9 Dynamic comparator circuit schematic with pre-amplifier, dynamic latch and dynamic sense-amplifier.

The charge difference built up on the output of the pre-amplifier's results in imbalanced charge between the equalizing transistor ($M5$) source and drain. After each reset phase, when the *Eq* signal is pulled down, the charge will set one of the Q or $\overline{\mathrm{Q}}$ to a logical level low.

Based on the regenerative latch resolving time, the comparator resolving time is found to be

$$t_{comp} = \frac{1}{Gain \cdot BW} \cdot ln \frac{V_{FS}}{V_{res}} \tag{4.3}$$

where V_{res} is the input voltage at the comparator and $Gain \cdot BW$ is regenerative latch gain bandwidth product. Note that as V_{res} decreases, the comparison takes longer. As discussed in Section 4.2 , the speed requirement of the comparator could be reduced to a minimum of t_{comp} ($V_{LSB}/2$). To achieve the 1GS/s sample rate, the specification for the comparator would require a resolving time of approximately 60*ps* with an input voltage of $V_{LSB}/2$, accounting for more than 20% of the bit cycle. Compared to previous approach [24], which avoids metastability by increasing the comparator speed, this relaxes the comparator requirements which allows for a lower power design.

The dynamic sense-amplifier is added to boost the comparator gain during the dynamic transitions (Fig. 4-9). It significantly reduces the resolving time when sensing small inputs, which are the bottle-necks of most of the previous comparator designs. The dynamic sense-amplifier switches between standby and operating modes, resulting in minimum static power consumption.

4.3.3 Semi-closed Loop Digital Circuits

To design the semi-closed loop digital circuits, first, we observe that both Q and $\bar{Q}$ are fully charged to V_{DD} at the end of each reset phase, thus, a voltage drop in either or both of them would indicate the start of a comparison. The *rdy* signal could therefore be generated ahead of the actual data completion time when the reliable data becomes available, and an approach for this is implemented as in Fig. 4-10. Detecting the start of the comparison shortens the overall delay of the critical path by allowing t_{comp} and $t_{digital}$ to overlap, thus allowing an increased speed without the power penalty. Second, as the comparator switches into the compare mode, both Q and $\bar{Q}$ are pulled down together by the regenerative latch to a level much lower than the supply voltage before one of them is charged back to V_{DD} and the other is discharged to *GND* as shown in Fig. 10. Therefore, both PMOS transistors in the *rdy* acknowledge signal generator are on during the pull-down transition, resulting in a significantly reduced delay from the complementary data to the *rdy* signal.

The *rdy* signal triggers a pulse generator to create the reset phase. During the reset phase, the SA decision and the charge redistribution on the capacitor array is performed. If the settling error for the DAC is less than V_{LSB}, the decision for the next comparison is reliable since further settling will not affect the result.

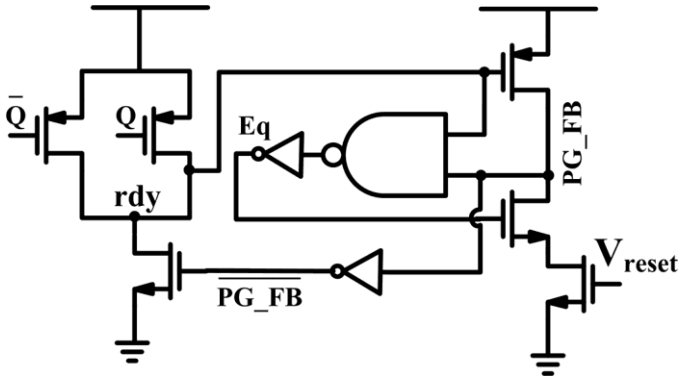


Fig. 4-10 Dynamic rdy acknowledge signal generator and pulse generator schematics.

The circuit for generating the reset signal *Eq* is shown in Fig. 4-10. The rising edge of the *Eq* signal flags the beginning of the reset phase and the pulse duration is adjusted through a biased MOS transistor. The voltage, V_{reset}, controls the duration of the reset phase by changing the delay from the equalizing clock (*Eq*) to the feedback node (*PG_FB*). Though V_{reset} is an externally fixed voltage in this implementation for testing purpose, it could also be set automatically using a 2~3 bit multiplying digital to analog converter controlled by a settling error sensing circuitry at the DAC's output, increasing the speed by 10~20%, at an estimated 10~15% power and area penalty.

The complimentary reset signal ($\overline{Eq}$) is used to reset the regenerative latch, charging both Q and $\bar{Q}$ to logical level high (Fig. 4-9). The feedback node (*PG_FB*) is used to reset the *rdy* signal shortly before the next comparison, such that the *rdy* signal turns off earlier than the equalizing clock, *Eq*. Because the *rdy* signal controls the reset switch in the pre-amplifier, the recovery phase is extended by allowing extra time for the DAC to settle towards the end (Fig. 4-11).

It is crucial that only the sign of the comparator differential input voltage matters, not the level. Towards the end of the DAC settling, when the input of the pre-amplifier is at a V_{res} level of a few millivolts, the pre-amplifier switches out of reset phase, starts to sense the DAC output (also noted as V_{res}) and track the settling direction. The pre-amplifier also monitors whether the V_{res} voltage changes its sign and accumulates charge at its output, in preparation for the latch operation. By allowing time overlapping of comparison and the DAC settling, the pre-amplifier's response time is merged with the DAC settling time. In this overlap time between t_{DAC} and the comparison time, the input voltage of the regenerative latch is significantly increased, so the resolving time is reduced, yet a reliable comparison is still guaranteed by controlling the latch with the *Eq* signal.

Towards the end of the current bit cycle if V_{res} is still relatively large (several 10's of mVs), then it is possible to allow time sharing, $t_{overlap}$, between the DAC and the pre-amplifier (Fig. 4-11) and thus relax the requirement of the DAC settling error to be larger than V_{LSB}, since it won't affect the current bit comparison result. Given that the entire bit conversion cycle is sufficiently long, this settling error will eventually diminish and have no effect on the next bit comparison. For a given bit, with the time overlapping and sufficient gain of the pre-amplifier, a

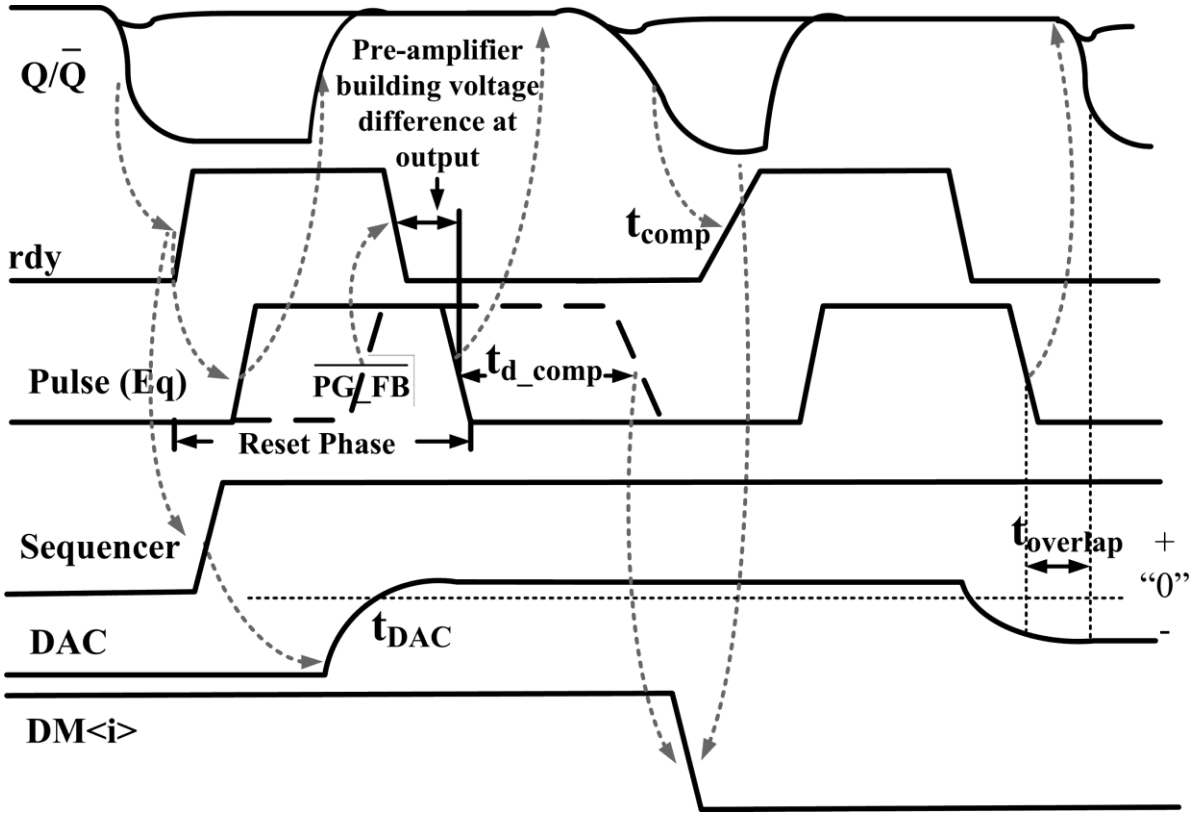


Fig. 4-11 Semi-closed loop timing diagram with extended reset phase.

larger V_{res} leads to a larger voltage difference at the pre-amplifier's output, thus helping the latch to evaluate the data faster, and reducing the resolving time.

The scheme of controlling the pre-amplifier and the regenerative latch separately helps to reduce the bit cycle substantially at both low and high V_{res} levels. The duration of a bit cycle thus mainly varies with the reset pulse width and the comparison time.

4.3.4 DAC Design and Non-Binary Capacitance Array

Because the reset pulse width strongly depends on the DAC settling time, to achieve high speed, we explored two design options for the DAC, 1) using the same size switches with low equivalent resistance in the DAC for all bits, such that the DAC R-C time constant τ, is reduced, 2) equalize the settling time from MSB to LSB with scaled switches.

If the time constant τ is designed to be the same for each bit, the DAC settling time to V_{LSB} level decreases from MSB's to LSB's. The longest bit cycle occurs when $V_{res} = \pm\frac{V_{FS}}{4} \pm V_{LSB}$, because the DAC settling step voltage is the maximum and the residue input voltage of the

comparator is minimum at this point. To achieve high speed, for LSB's, since the step voltage is small, the reset pulse width could be reduced to achieve higher speed. For MSB's, a detection circuit could be implemented, to sense the absolute value of V_{res} and the settling error ε at the end of each reset phase. Towards the end, if $V_{res} \gg \varepsilon$, shortening the reset pulse enables an reliable early evaluation, because the voltage level is sufficiently high from changing the sign and the remaining settling of the DAC is allowed to happen together with the comparison and even extended into the next bit cycle. If V_{res} is small, the long pulse width is required to satisfy the worst case scenario, which needs to wait for ε to become less than V_{LSB}. The sensing and controlling circuitry could be quite complicated and power consuming. Therefore, after careful analysis of the trade-offs among speed, area and power, the settling time of the DAC, t_{DAC}, is chosen to be fixed for all bit cycles. Though it leads to a slight sacrifice in speed, it yields a simpler, compact and lower power design.

The settling time t_{DAC} is found to be,

$$t_{DAC} = \tau_i ln \frac{|V_{step_i}|}{V_{LSB}} \tag{4.4}$$

where τ_i and V_{step_i} denotes the time constant of the i^{th} bit and the voltage step size required for the ith stage to settle.

In order to equalize t_{DAC} for all bits, τ_i needs to be scaled with respect to the voltage step size V_{step_i} for each bit. Given

$$\tau_i = R_{sw_i} \cdot C_{in\ Array} \tag{4.5}$$

R_{sw_i} is the equivalent turn-on resistance of the switches in the DAC, the scaling of τ_i is accomplished by scaling the corresponding switch size. Shown in Fig. 4-12, as the step size becomes smaller for the LSB's, τ_i is increased. While the primary reason to scale the switch sizes is to keep t_{DAC} constant, there is the usual substantial improvement in area in the DAC since the switch sizes for the LSB's are significantly reduced.

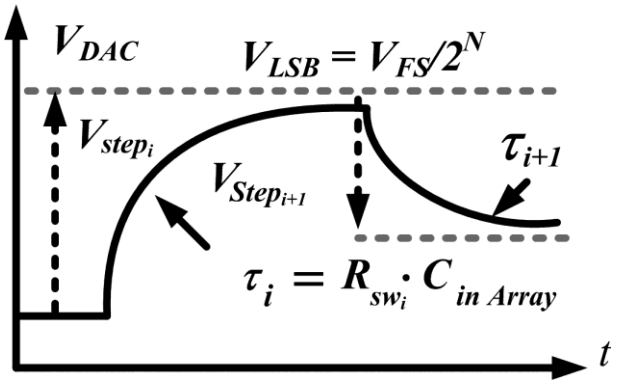


Fig. 4-12 Fixed DAC settling time by scaling switch sizes as opposed to the targeted step voltages.

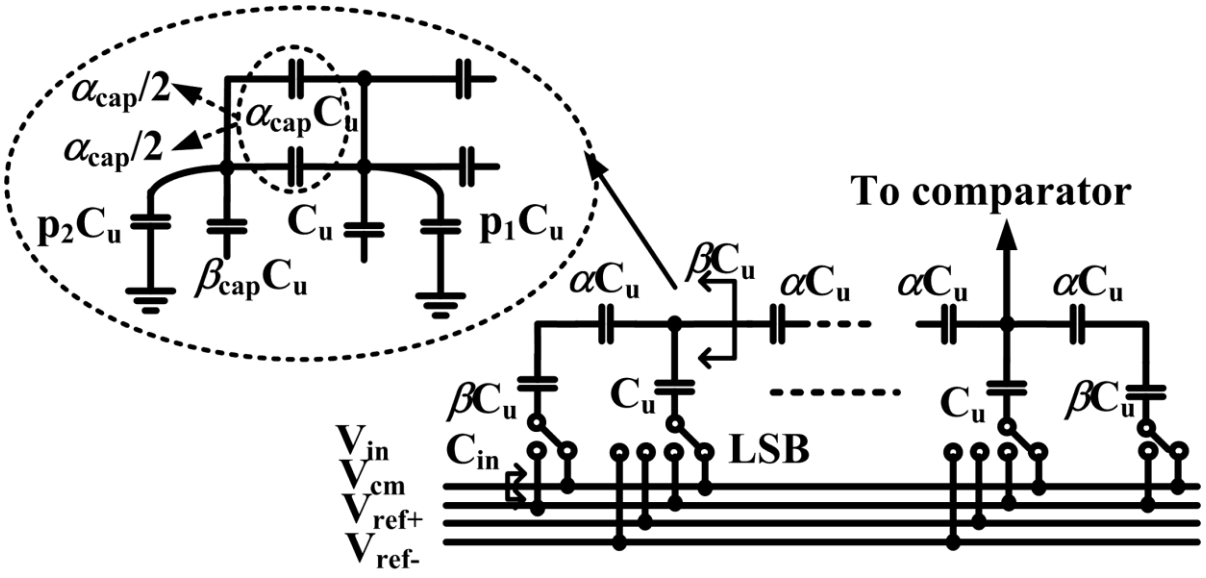


Fig. 4-13 Non-binary series capacitive ladder network: schematics and parasitic at the interconnects.

To reduce the input capacitor, a series non-binary capacitive ladder is used. The equivalent input capacitance is much lower than a parallel structure [25; 26]. An important disadvantage of the series ladder structure is its sensitivity to parasitic capacitance due to interconnects. This however, can be taken into account. The basic approach for the design of this network is to have the equivalent capacitance at each floating node be identical. The ideal design equation is:

$$\begin{aligned} \beta &= 1+\alpha \,\|\, \beta \\ radix &= 1+\beta/\alpha \end{aligned} \tag{4.6}$$

With α and β defined as the ratio between the ideal series capacitance and the unit capacitor [24] (Fig. 4-13).). However, the parasitic capacitances must be taken into account, also as shown in Fig. 4-13, α and β above can be modified to be:

$$\begin{aligned} \beta &= \frac{\beta_{cap}+p_2}{p_1+p_2+1} \\ \alpha &= \frac{\alpha_{cap}}{p_1+p_2+1} \end{aligned} \tag{4.7}$$

with p_1, p_2 is the ratio between the parasitic associated with these interconnects to the unit capacitance[24].

By iteratively estimating and simulating the capacitance at floating nodes and the corresponding ratio of α and β, for moderate resolution, the radix matching from bit to bit could be improved and compensated adequately over process.

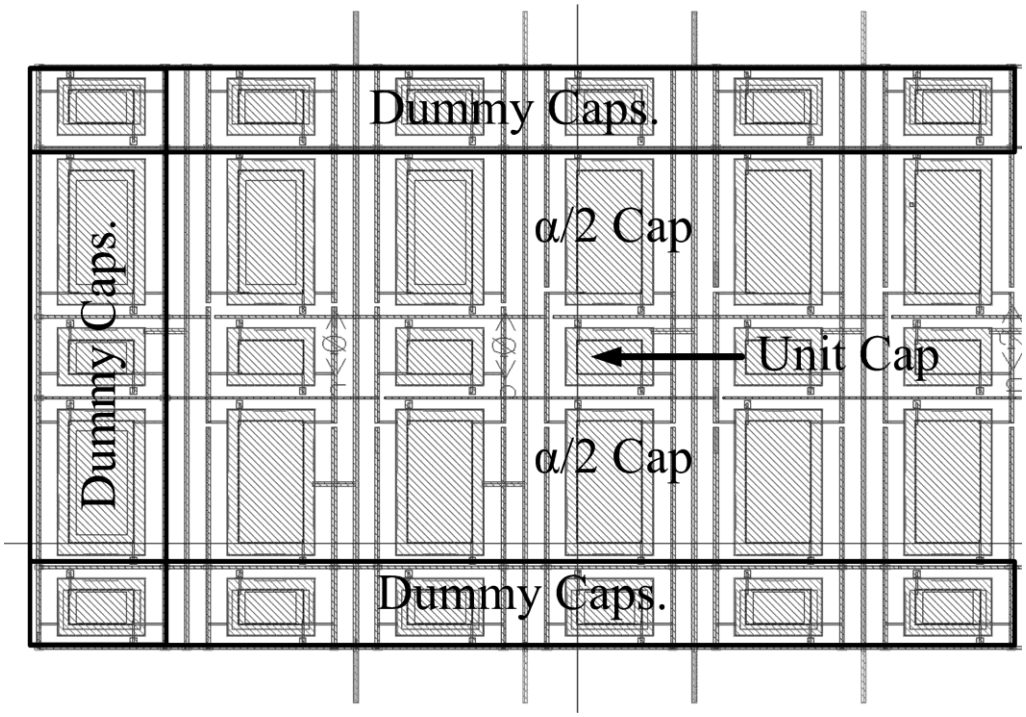


Fig. 4-14 Binary capacitive ladder with improved symmetry.

The resulting input capacitance is only 84fF, which significantly shortens the DAC settling time and increases the input bandwidth. The capacitor array is implemented with low-cost metal-oxide-metal plate-to-plate capacitors and particular care was taken to achieve adequate capacitor accuracy with layout. Each α capacitor is divided into two $\alpha/2$ capacitors, located at the top and bottom of a column cell (Fig. 4-13, Fig. 4-14). This not only compensates for the vertical process variation, but also provides better differential matching by interleaving the positive-side and negative-side capacitor arrays. Dummy capacitances are placed on each side to further improve matching. α and β values are chosen such that the equivalent radix for the capacitive ladder is 1.9~2 (essentially a binary network), but with the advantage of allowing some dynamic decision errors and avoiding missing codes. One bit redundancy is implemented for testing and to avoid significant bit weight loss. The passive bottom plate sampling network is combined with the binary capacitive ladder. Relatively small switches can be used but a high input bandwidth of greater than 10GHz was still achieved.

The unpredicted parasitic variation and capacitor mismatch results in a change of the effective radix for each bit. These discrepancies cause variations in the bit weights and lead to non-linearity of the ADC. This systematic error is, however, compensated by foreground off-chip calibration where a known full-range sinusoidal signal is injected. The converted digital outputs are used to reconstruct the initial input signal. The bit weights are then calibrated using an adaptive algorithm to minimize the mean-square error.

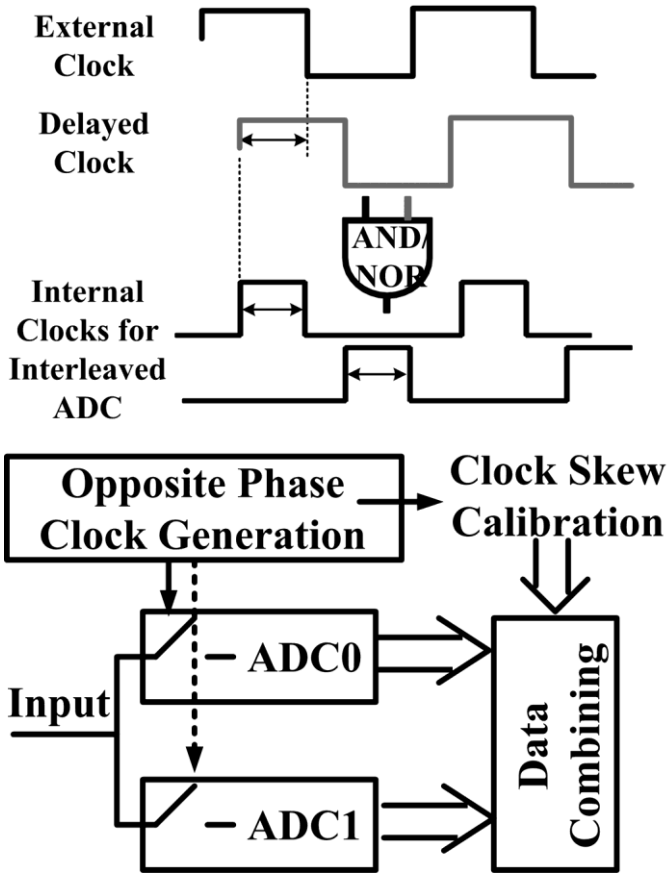


Fig. 4-15 Opposite phase clock generation for the time interleaving topology.

4.3.5 Opposite-Phase Clocks for Time Interleaving

To perform time interleaving, pair of internal clocks are generated from a 50% duty cycle square wave off-chip sampling clock as shown in Fig. 4-15. The internal non-overlapping sampling clocks with 180 degree phase shift are generated on-chip for the time interleaving. The input clock is buffered and delayed on chip. Particular care was taken in the layout to generate and distribute the opposite phased clocks to ensure 180 degree phase shift. It has been observed that any imbalance from the two sampling clocks, as well as undesired clock jitter caused by the noise from the generation and distribution network will result in ENOB degradation [36].

4.4 Measurement Results

The converter is implemented in a 1.2V 65nm Low-Power CMOS process. Each ADC only occupies an area of 0.35 x0.16mm^2. The total die size is 1.6×1.4mm^2 of which the active area

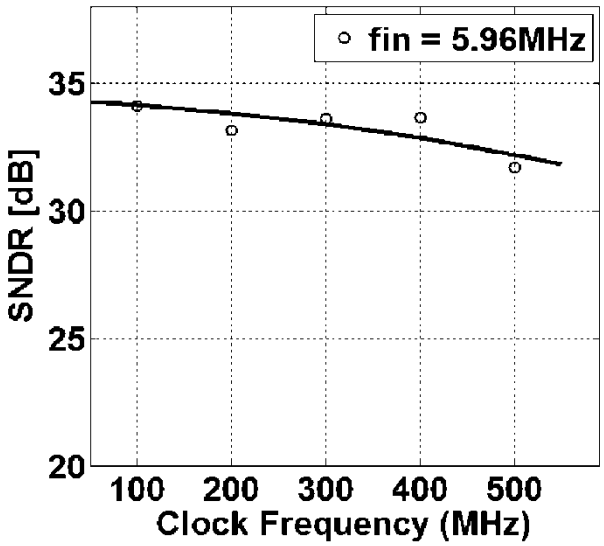


Fig. 4-16 Measured SNDR versus sampling frequency for one single ADC.

occupies only 0.11mm^2. The measured results show the ENOB of a single ADC scales from 5.6b at 100MS/s to 5b at 500MS/s (Fig. 4-16). The dynamic performance using input above Nyquist rate ranging up to 500MHz shows the signal to noise and distortion ratio (SNDR) at different sampling frequency remains above 28*dB* (Fig. 4-17, Fig. 4-18). We believe the 200MHz degradation when sampling at 500MS/s was due to a spur from an unknown source on the test circuit board. demonstrates the direct tradeoff between the ENOB and the conversion rate. Fig. 4-18 and Fig. 4-19 show the time-interleaved ADC performance is increased to 1GS/s at twice the power and area. The static performance of the interleaved ADC is also characterized by DNL and INL measurements (Fig. 4-20, Fig. 4-21).

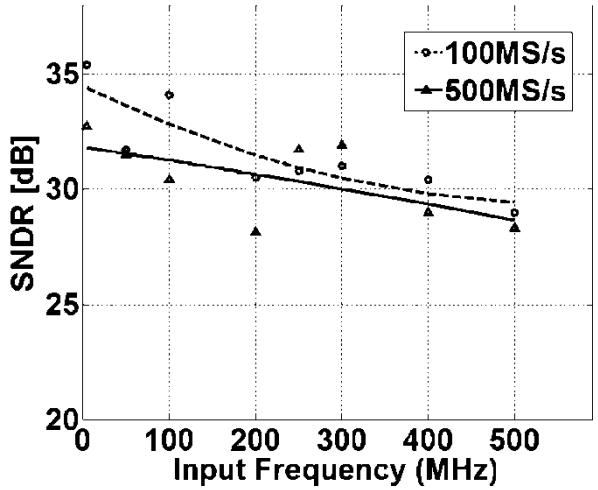


Fig. 4-17 Measured SNDR versus input frequency for one single ADC.

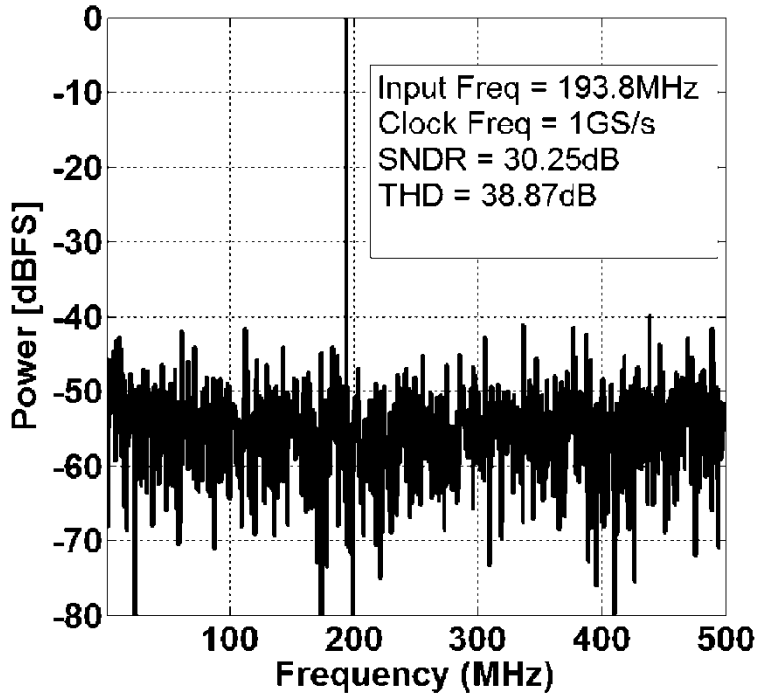


Fig. 4-18 Measured power spectrum and SNDR versus sampling frequency for the interleaved ADC.

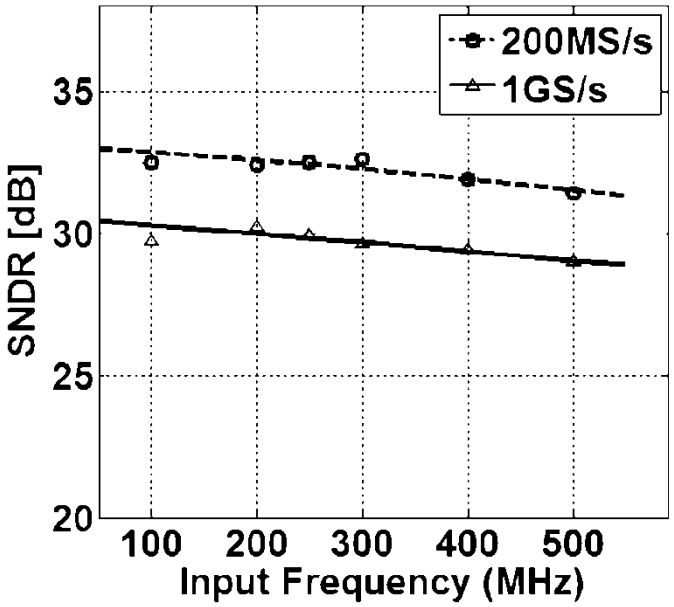


Fig. 4-19 Measured power spectrum and SNDR versus input frequency for the interleaved ADC.

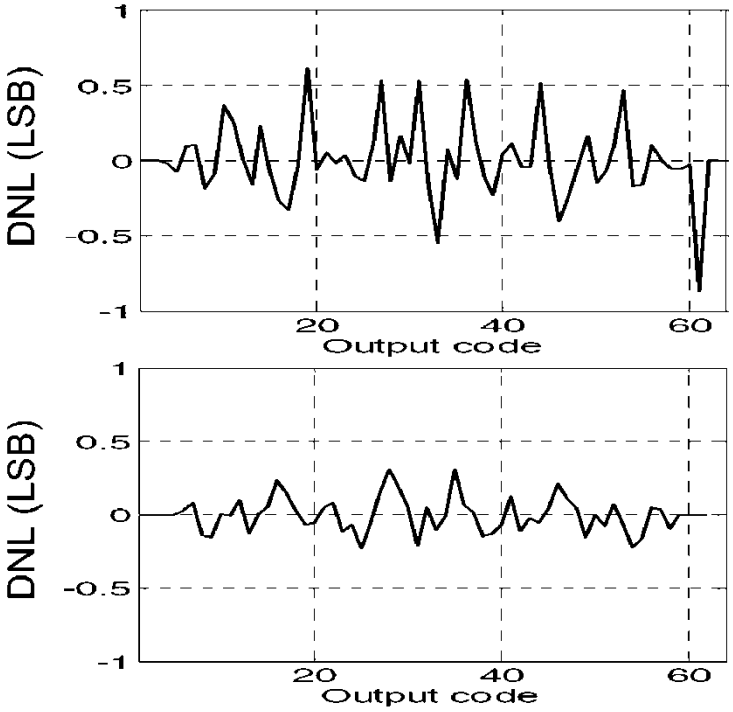


Fig. 4-20 DNL before and after calibration.

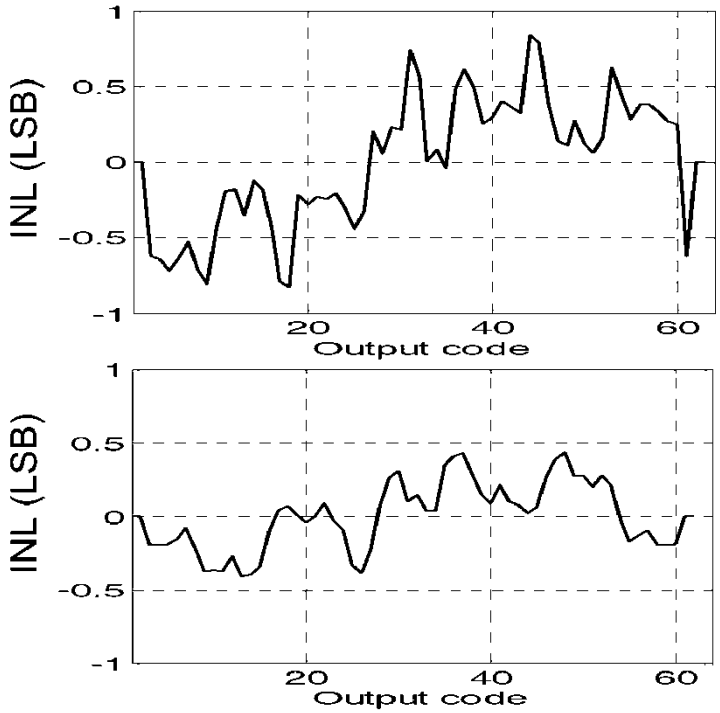


Fig. 4-21 INL before and after calibration.

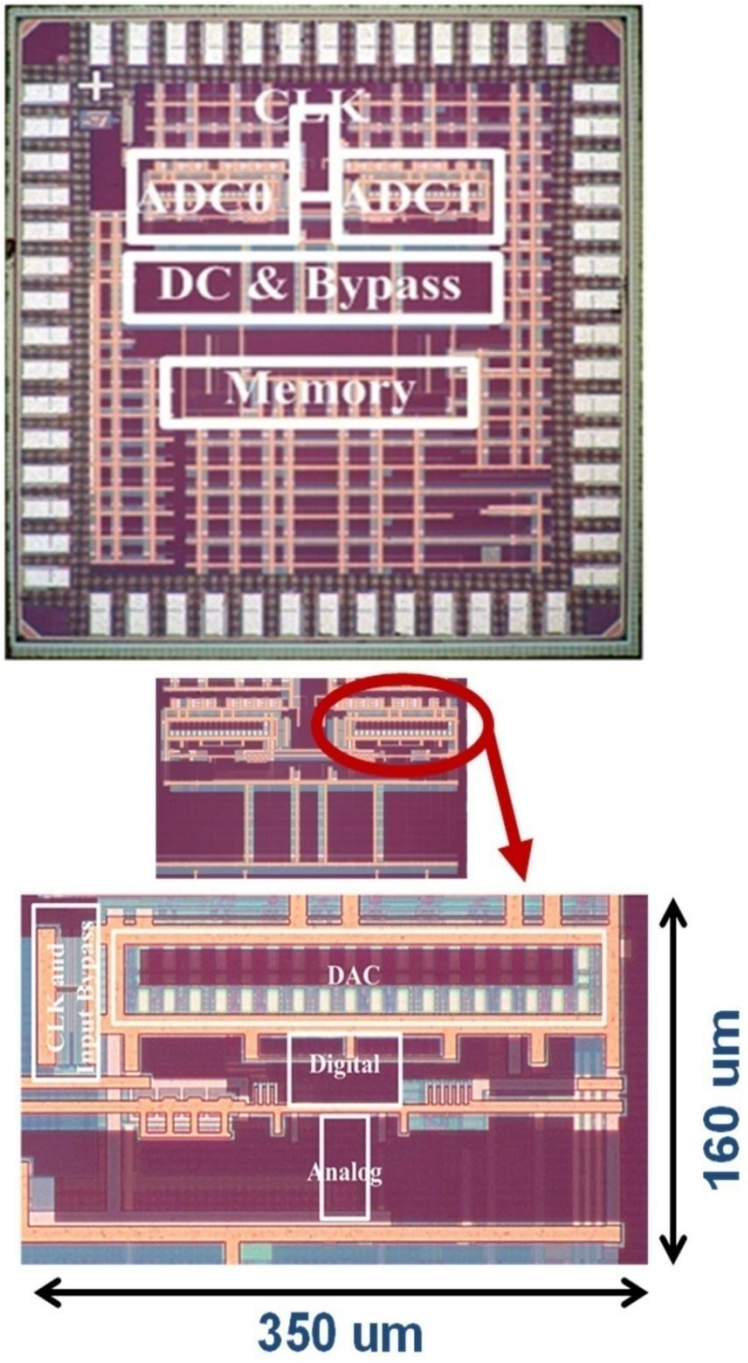


Fig. 4-22 Chip micrograph.

Among our relatively small samples of chips, even with the capacitance and parasitic variance due to process, DNL and INL are only around 0.8LSB. After the digital calibration for the bit weights and the subtraction of the offset, as mentioned in Section 4.3.4 , DNL improves by almost half an LSB and INL improves by more than 0.4LSB. This is equivalent to a 2-3dB improvement in SNDR. The clock skew between the two high frequency clocks is calibrated out, resulting in only 0.7dB degradation in SNDR from a single ADC performance. The chip microphotograph is shown in Fig. 4-22. Two ADC's, the clock generation and distribution network, as well as the DC bypass capacitors were implemented. In order to facilitate measurements, a 1K word memory is included on-chip. The total active area is 0.11mm^2. The analog, digital and clock circuitry consumes 1.51mW, 4.05mW and 1.16mW respectively at a sample rate of 1GS/s. With the standard FOM for ADC's is defined as $power/(2^{ENOB} \cdot f_s)$, the time-interleaved ADC's achieve 0.21pJ/conversion step, which compares favorably to other asynchronous architecture, SAR and high Speed ADC's [37; 38; 39; 40; 41]. The performance results are summarized in Tab. 4-1.

Technology		65nm 7M Low Power CMOS	
ENOB		5.0 bits	
Sampling rate		Up to 500 MS/s for single ADC (1GS/s with time interleaving)	
Supply voltage		1.2 V	
Peak SNDR		31.5 dB (f_s = 1GS/s for two ADCs)	
Area		0.11mm^2	
Figure of Merit		0.21 pJ/conversion step	
Power	Analog	1.51mW	Total (two ADCs): 6.72mW
	Digital	4.05mW	
	Clock	1.16mW	

Tab. 4-1 Performance summary.

4.5 Summary

In the asynchronous SAR ADC design, to enhance the performance, it is crucial to design a fast resolving comparator, fast digital circuits and a quick settling DAC. A dynamic sense amplifier is used to boost the gain during the comparator transition without adding static power consumption. The semi-closed loop digital circuits allow a much faster successive approximation decision and the series capacitive ladder significantly reduces the equivalent input capacitance, hence benefitting both input sampling and the DAC settling.

The asynchronous architecture not only achieves higher speed at lower power in comparison to a synchronous approach, but it allows the use of metastability detection which can be used with a simple extension to the SA algorithm to eliminate any ENOB degradation. This algorithm extension relies on the fact that there will only be one bit evaluation in metastability in an SAR architecture and thus metastability can easily be detected by simply determining if there is less than an N bit output. A simple algorithm was described which then creates the correct N bit code.

The proposed circuit implementation carefully addresses the asynchronous dynamic properties of the SAR design. The topology to generate completion signals is based on the analysis of the comparator dynamic transition, and the approach to create and optimize the overlap time between the DAC settling and the comparison, significantly increases the speed of the architecture.

A bit independent DAC settling was chosen, since reducing the switch sizes reduces the DAC area and a fixed time avoids complex DAC completion sensing circuitry thus saving power with only a slight penalty in speed.

In summary, a time interleaved asynchronous SAR ADC architecture has been demonstrated to achieve high power efficiency for a high-speed and medium-resolution converter requiring very small area in 65nm CMOS. It not only achieves a FOM of 0.21pJ/conversion step, but is believed to be an approach which will scale well into future technologies.

Chapter 5

System Demonstration

Besides the high speed (1GS/s) medium resolution (5-bit) ADC, the system includes several other important components, the subtractor and gain stage, the high speed DAC on the cancellation path and the analog delay line.

In this chapter, we will discuss the implementation issues by analyzing each element of its design strategy and provide a board demonstration towards the end to verify the conceptual idea of the interference cancellation system.

5.1 Subtractor and Gain Stage

The subtractor and the gain stage are usually implemented by differential programmable amplifier. Among the key blocks in the architecture is this residue amplifier that interfaces the two successive stages. The subtractor/gain element has to meet very stringent speed, noise, and linearity requirements and tends to be a significant fraction of power dissipation [42]. To address this issue, a variety of techniques have been developed to minimize amplifier power.

In addition to its significant power consumption, it has also been recognized that residue amplifier is most susceptible to complications that arise from continuing integrated circuit technology scaling [43], [44]. For implementations in future deep-submicron processes, it is

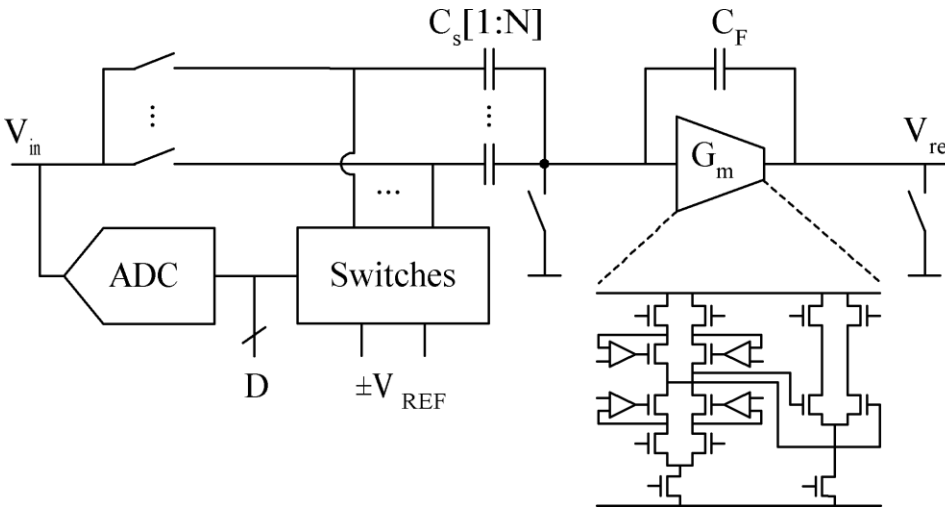


Fig. 5-1 Conceptual diagram of a conventional gain stage using feedback approach.

often predicted limited supply headroom and low intrinsic device gain may lead to a relative power increase in such noise-limited precision analog circuit blocks [45], [46].

Fig. 5-1 shows the traditional switch capacitor approach with feedback. The circuit operates in two main clock phases. During the sampling phase, the residue input signal Vin from the first stage is acquired. In a second phase, a residual is redistributed onto the feedback capacitor to produce the amplified stage residuum Vre. In this conventional scheme, the use of electronic feedback around the operational trans-conductance amplifier (OTA) results in a precise and drift insensitive stage transfer function. As in many other electronic systems, feedback in this circuit serves two main purposes: 1) to mitigate the impact of device nonlinearities in the OTA; and 2) to desensitize the overall transfer function to changes in ambient operating conditions, such as temperature. The cost of these desirable features is an excessive OTA voltage gain requirement. Since the effectiveness of feedback is proportional to the system's loop gain, high precision necessitates the use of complex high-gain OTA topologies [47]. As is typical, the front-end is required to use a two-stage gain-boosted amplifier with an open-loop gain over 100*dB* to meet the stringent design requirements. In fine-line technology with low intrinsic device gain and limited supply headroom, such amplifiers are hard to implement and tend to be power inefficient.

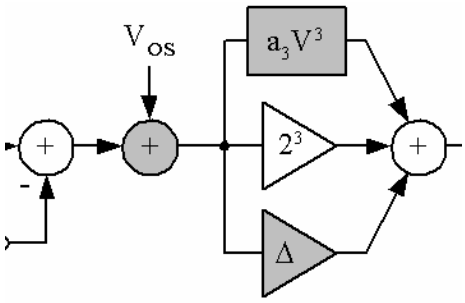


Fig. 5-2 Open-loop gain stage for residue amplifier with digital correction.

Recently, the benefits of using open-loop structures in high-speed ADCs have been recognized and demonstrated [48][49]. Continuous open-loop current-mode residue amplification is used to achieve excellent power efficiency at high conversion speeds. The voltage-mode topology in conjunction with appropriate calibration techniques could push the applicability of open-loop structures even into the 12-bit ADC domain. Unlike in the closed-loop implementation, the residual presents in place to produce a small voltage at node. This residuum is fed into a resistively loaded differential pair to produce the desired full-swing residue voltage. In this modified circuit, the high gain requirement in the trans-conductor is dropped, resulting in a simple power-efficient amplifier topology with improved deep-submicron compatibility. These advantages, however, come at the price of several new non-idealities in the stage transfer function. Particular focus had been addressed in previous work with analysis of these errors, and the implementation of their digital domain compensation (Fig. 5-2) [42].

5.2 DAC

The cancellation from stage uses the digital signal processing circuitry. The processing gain from the DSP calls for integration of high-performance DAC, which becomes a critical block in the architecture. When multiple interferers are presented simultaneously, it is very important that the DAC's meet a minimum SFDR, or the desired signal could be corrupted by spurious components from other channels. Therefore, the major challenge for designing DAC's for frequency domain applications is to obtain large *wideband* SFDR.

As the demand for bandwidth and information processing is growing, so is the speed and linearity of the DAC, while the power and area need to be kept low at the same time. Unlike standalone high-performance DACs, the requirement of these DACs on the power consumption and area are more stringent in order to contain the total budget of the entire system-on-a-chip (SOC). The linearity and noise associated with the DAC becomes directly distortion and noise source to the desired signal. This poses the greatest challenge in high speed DAC design. Very high sampling frequency (>500MHz) and high linearity DACs have been reported [50][51].

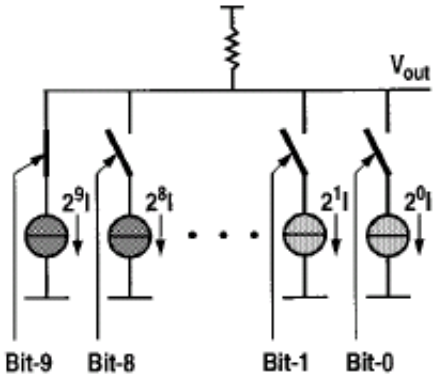


Fig. 5-3 Binary Weighted DAC

However, large number of power and area are used to get a low impedance over wide frequency range. Last but not least, an integrate DAC needs to survive and perform on a noisy substrate with large scale DSP circuitry on the same die. In this design, an 8~10-bit DAC is required depends on the dynamic range at the secondary user front-end.

Fig. 5-3 shows a conceptual circuit of a 10-bit binary weighted DAC [52]. The digital inputs directly control the switches. The current sources associated with the switches are binary weighted. The advantage of such a binary-weighted DAC is its simplicity, as no decoding logic is required. There are several major drawbacks, however, which are all associated with major bit transitions. At the mid-code transition (0 111 111 111->1 000 000 000), the MSB current source needs to be matched to the sum of all the other current sources to within 0.5 LSB's. This is difficult to achieve. Because of statistical spread, such matching can never be guaranteed. Therefore this architecture is not guaranteed monotonic. Matching is an issue for all bit transitions, which will result in a typical DNL. Glitch due to switching contains highly nonlinear signal components and will manifest itself as spurs in the frequency domain [52].

Fig. 5-4 shows an example of a 10-bit thermometer-coded DAC [52]. There are unit current sources. Each unit current source is connected to a switch controlled by the signal coming from the binary-to-thermometer decoder. When the digital input increases by 1 LSB, one more current source is switched from the negative to the positive side. Assuming positive-only current sources, the analog output is always increasing as the digital input increases. Hence, monotonicity is guaranteed using this architecture. In addition, there are several other advantages for a thermometer-coded DAC compared to its binary-weighted counterpart. First, the matching requirement is much relaxed. At the mid-code, a 1-LSB transition, causes only one current source to switch as the digital input only increases by one. This greatly reduces the glitch problem. On top of that, glitches hardly contribute to nonlinearity in the thermometer-coded architectures. This is because the magnitude of a glitch is proportional to the number of switches that are actually switching. So for small steps, the glitch is small, and for a large step, the glitch is large. Since the number of switches that switch is proportional to the signal step between two consecutive clock cycles, the magnitude of the glitch is directly proportional to the amplitude of the signal step.

Usually, to leverage the clear advantages of the thermometer-coded architecture and to obtain a small area simultaneously, a compromise is found by using segmentation. The DAC is divided

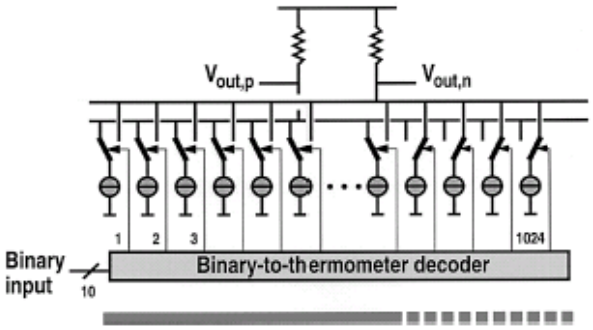


Fig. 5-4 Thermometer-coded DAC.

into two sub-DAC's, one for the MSB's and one for the LSB's. Thermometer coding is used in the MSB where the accuracy is needed most. Because of the reduced number of bits in this section, the size is considerably smaller than a true thermometer-coded design. The LSB section can either be done using the binary-weighted or the thermometer-coded approach. It is generally referred to a fully binary-weighted design as 0% segmented, whereas a fully thermometer-coded design is referred to as 100% segmented.

With a reasonable budget of several 10's of mW power consumption from the DAC, to minimize the chip area, under the constraints of maximum required 10-bit performance, while simultaneously trying to optimize frequency domain performance. One can choose a current-steering architecture with 6-bit MSB plus 4-bit LSB segmentation [53]. The 6 MSB's control the switching of 63 unary current sources by thermometer decoding, while the 4 LSB's control the switching of 4 binary weighted current sources. The segmentation scheme chosen here meets the linearity requirement. Further increase the number of bits in MSB will increase the area, power consumption and design complexity.

5.3 Analog Delay Line

A programmable delay is achieved through the analog delay line. Recall that the delay through the delay line and intrinsic delay from upper path should be equalized. For this purpose, a series delay line with series structure is desirable. The concept is simply to cascade several delay cells to achieve the time matching. Each delay component is required to pass the input signal with minimal distortion. The sensitivity and linearity must be high to maintain the resolution of the week received CR signal. For discrete-time analog delay line elements, they need to provide high unity gain bandwidth to ensure speed and fast setting. Moreover, besides the difficulties of fulfilling the high-speed high-accuracy requirement, the series structure is vulnerable to the error accumulation throughout the entire line driver due to component variations. With unity gain delay elements, each stage contributes equivalent amount of noise when calculating the input referred noise. Therefore, the noise tends to kill the sensitivity to the weak signal if significant amount of stages are cascaded.

Instead of discrete time delay line, we suggest a continuous-time series delay line to be used without tracking and hold. This avoids the tremendous power and area consumptions that are on the order of a wideband-high resolution ADC. The infeasible high speed, high accuracy ADC design is mainly due to the error requirement from the sampling circuits. By removing the sampler, the clock jitter requirement has therefore been significantly relaxed. At the same time, multi-step (integer) digital predictor with a fractional digital delay is used to reduce the delay requirement through the continuous analog delay line.

Among the options of implementing the delay cell, there are passive cells and active cells. The process variations in passive components, such as R and C, prohibited their application in high sensitivity delay cells. Time delay can be realized through transmission lines, lumped LC delay lines [54], or active devices [55]. Transmission line implementations often require an excessive chip area. For example, at 10Gb/s, a single period delay is about one centimeter long.

Lumped LC delay lines are also area-inefficient because of the required inductance values. Losses along both transmission lines and LC lines prevent cascading too many stages. Furthermore, the power consumption is large because of the low impedance of the lines.

Since the applications are sensitive to signal distortion, the active analog delay stage should demonstrate constant bandwidth at a variety of delay values [56]. Accurate delay requires robustness to process, voltage, and temperature variations. An active delay should conserve area without requiring excessive power consumption. A closed loop structure can be used to adjust the delay by either change the bias current or digitally control the segmented DAC of capacitors [57]. Proper delay tuning could also be achieved with a delay reference loop that employs a reference frequency to stabilize the time delay [58].

The block diagram of an analog delay line is shown in Fig. 5-5. The multipliers are MDAC's, so the weights are digital. A side effect of cascading these delay cells is that there is a reduction in gain as the signal travels down the delay line. While this gain loss could be compensated for in the MDAC's, small low gain buffers in series with the MDAC's could be used instead. Using these buffers allows the full MDAC range to be available for adaptation. These buffers cannot be placed in the delay line itself since their delay would be significant. The maximum number of taps for this architecture is limited by the gain of the delay cells [57].

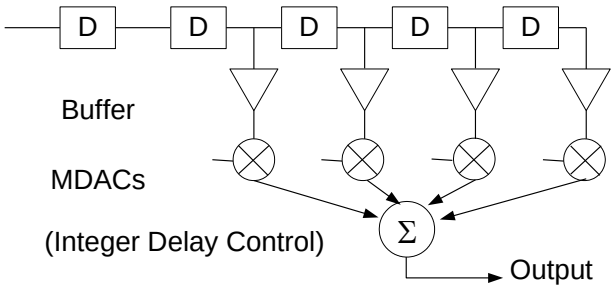


Fig. 5-5 Block diagram of analog delay line.

5.3.1 First and Second Order Analog Delay Cell

Fig. 5-6 illustrates an example of a first-order all-pass transfer function analog delay cell [59]. When choose $(W/L)_{M12,M13} = (W/L)_{M1,M2}$, the transfer function becomes,

$$H(s) = \frac{v_o}{v_{in}} = \frac{s - \frac{g_{m5,6}}{C}}{s + \frac{g_{m5,6}}{C}}, \left|H(s)\right| = 1$$

and the group delay is given by:

$$\tau(\omega) = \frac{2\frac{g_{m5,6}}{C}}{\omega^2 + \left(\frac{g_{m5,6}}{C}\right)^2}.$$

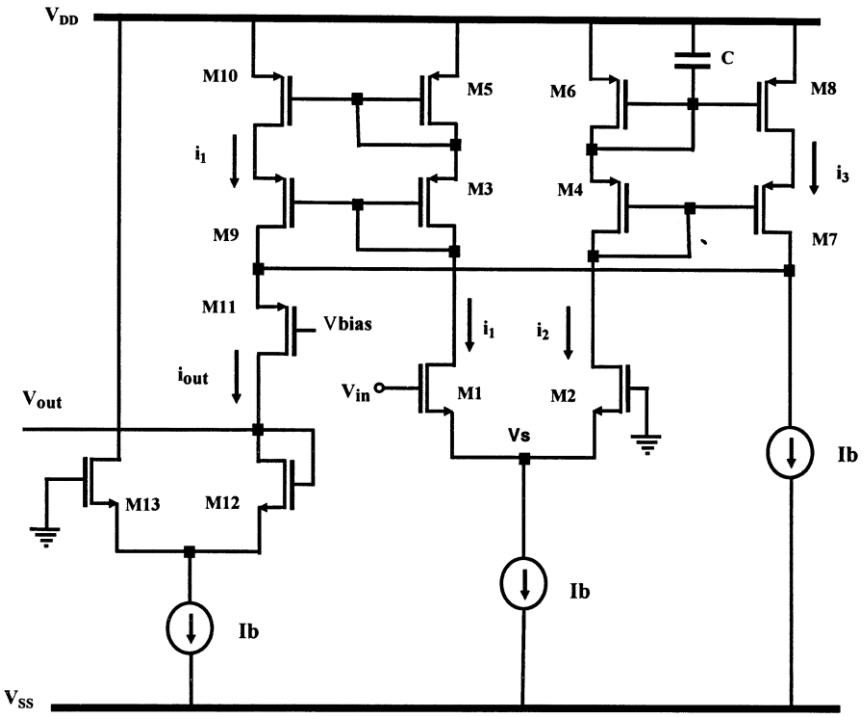


Fig. 5-6 A first order all pass analog delay cell

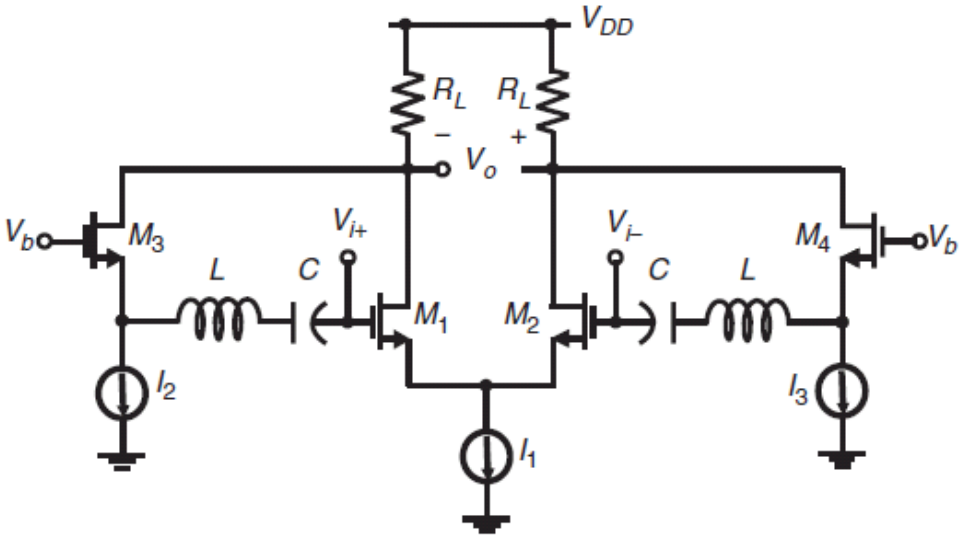


Fig. 5-7 A second order all pass analog delay line.

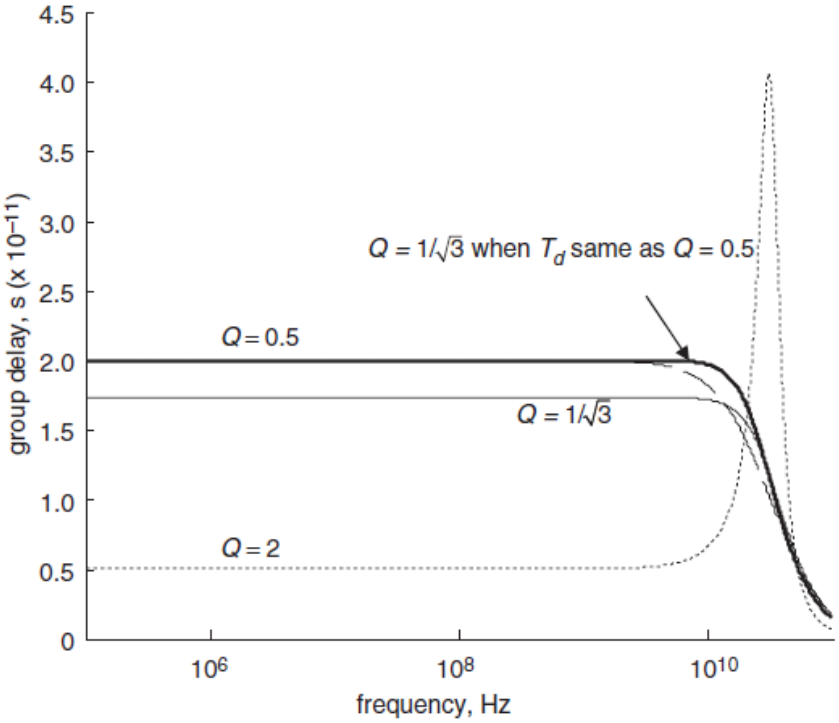


Fig. 5-8 Group delay of second order all pass analog delay line with different Q-factor.

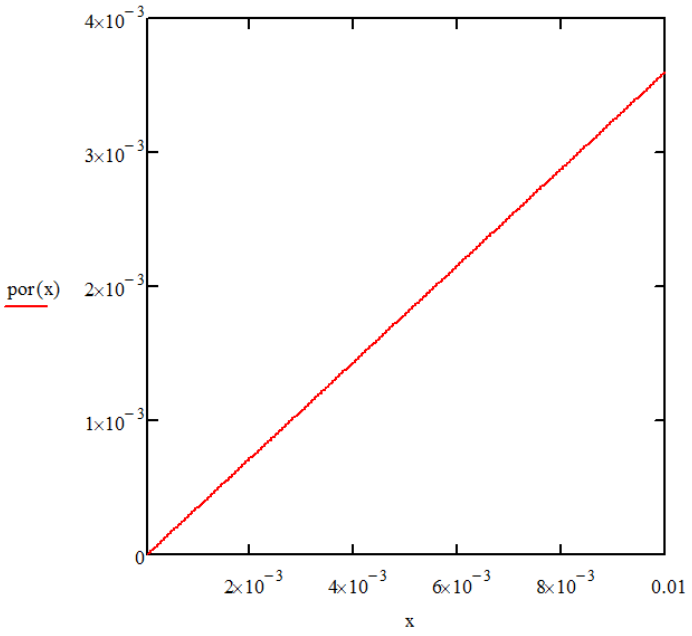


Fig. 5-9 Power vs. gm for first order system.

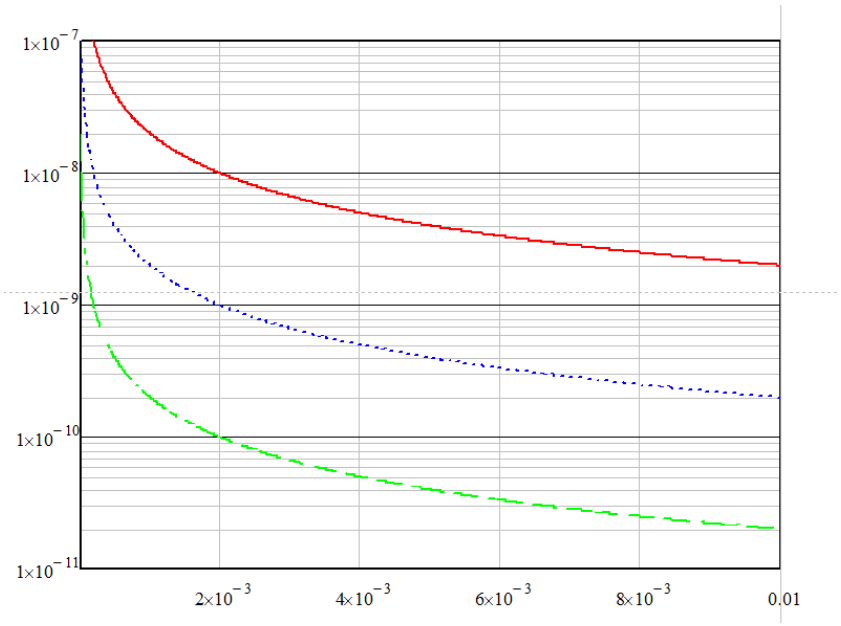


Fig. 5-10 Delay vs. gm for first order system given different capacitor values.

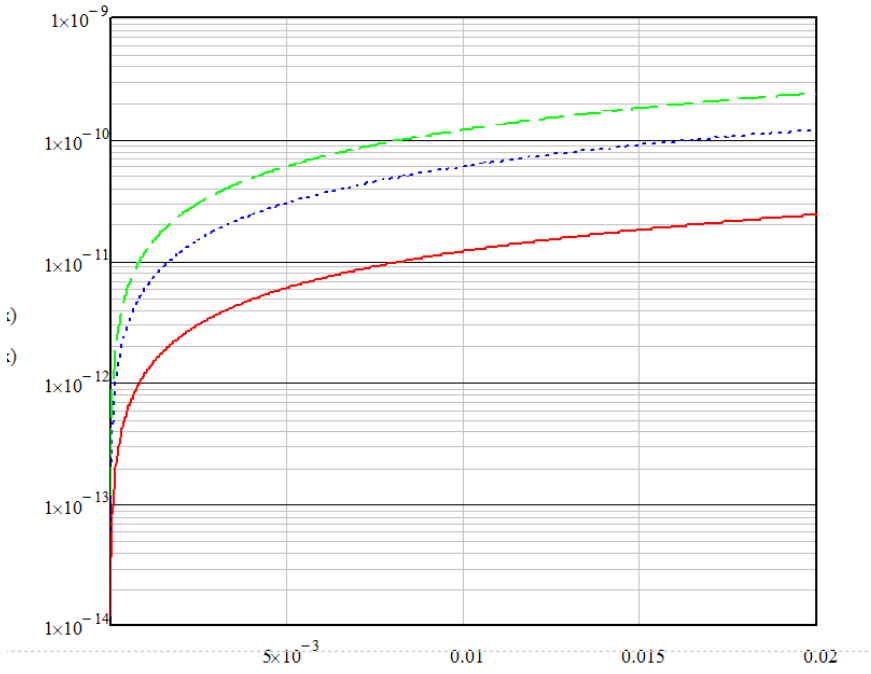


Fig. 5-11 Delay vs. gm for second order system given different inductor values.

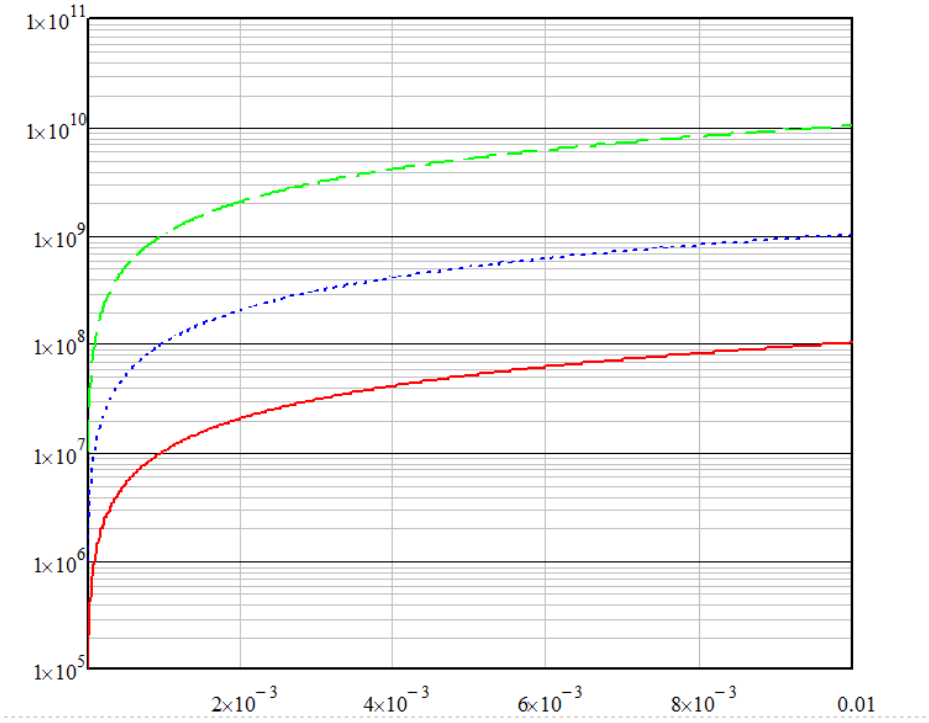


Fig. 5-12 -3*dB* bandwidth vs. gm for first order system given different capacitor values.

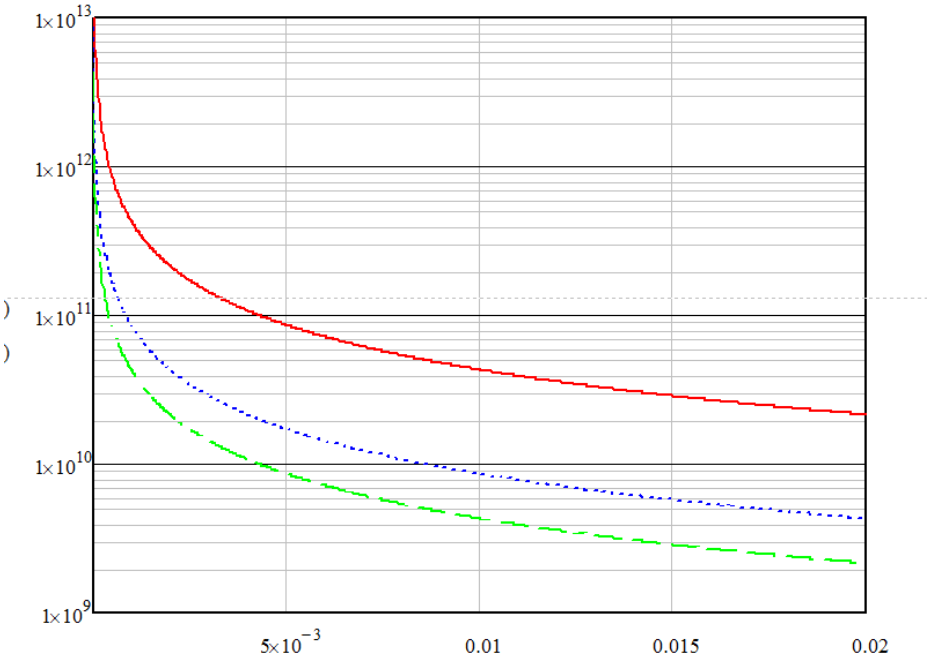


Fig. 5-13 -3*dB* bandwidth vs. gm for second order system given different inductor values.

A second order all pass analog delay line could be designed with different Q factors using circuits shown in Fig. 5-7 [60]. The transfer function of the circuit is as follows and the group delay with different Q value is illustrated in Fig. 5-8.

$$H(s)=\frac{v_o}{v_{in}}=\frac{g_{m1}R_L(s^2+s\frac{1}{L}(\frac{1}{g_{m3}}-\frac{1}{g_{m1}})+\frac{1}{LC})}{s^2+s\frac{1}{g_{m3}L}+\frac{1}{LC}}$$

We compared the above two topologies for the delay cell and further explore the transfer function. It can be seen that the delay is categorized into 100's pico-second and 10's pico-second range. Given the specification is between a few hundreds to pico-second, the first order gm-C cell, however, provides sufficient delay with a reasonable size capacitor, transistors and the bias current. Power of the gm-C cell increases linearly with gm (Fig. 5-9). It therefore, exists a power and area trade-off between the bias current and the size of the capacitor (Fig. 5-10, Red: C=10pF, Blue: C=1pF, Green: C=0.1pF). As the system speed increases, the second order LC cell becomes more preferable. Both the magnitude of gm and L significantly drop, facilitates a power efficient design (Fig. 5-11, Red: L=0.1nH, Blue: L=0.5nH, Green: L=1nH).

We have also have plotted the -3*dB* bandwidth for the two approaches in Fig. 5-12 (Red: C=10pF, Blue: C=1pF, Green: C=0.1pF) and Fig. 5-13 (Red: L=0.1nH, Blue: L=0.5nH, Green: L=1nH). This is clearly a delay bandwidth trade-off that requires to be explored when choosing the topology. When capacitance becomes larger, though the delay achieved through each cell is longer, and the total input referred noise level from each cell reduces, the bandwidth of the cell decreases. It can be seen the gm increasing results in a wider bandwidth for the first order system. For the second order system, the delay, the bandwidth decreases with the size of inductor and gm.

Though not fabricated, the analysis provides fundamental design tradeoffs for the continuous analog delay line implementation as a future work.

5.3.2 Digital Fractional Delay Filters

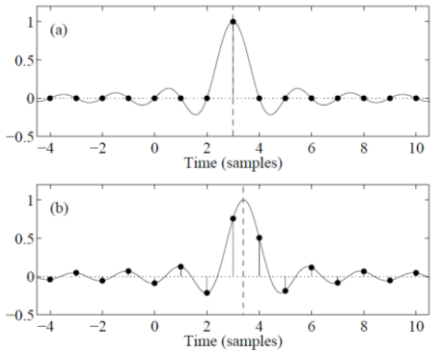


Fig. 5-14 Continuous time and sampled impulse response of the ideal fractional delay filter, where the delay is D = 3.0 samples and D = 3.4 samples

As mentioned before, instead of providing accurate long analog delay, it is also practical to design digital fractional delay filters to combine with a multi-step digital prediction, such as an asymptotic prediction using mean squared error [61], on the cancellation path.

The ideal fraction delay element is a digital version of a continuous time delay line. The delay system must be rendered bandlimited using an ideal lowpass filter where the delay merely shifts the impulse response in the time domain. Thus the impulse response of an ideal fractional delay filter is shifted and sampled sinc function, that is $h(n) = \sin c(n - D)$,where D is the delay with an integral part floor(D) and a fractional part $d = D - floor(D)$, as an example shown in Fig. 5-14[62].

5.4 System Test Bed

The Cognitive Radio Test Bed is a collection of hardware, software, Simulink models, and support tools and libraries. The two primary hardware units are the front-end board with radio and a BEE2. The front-end has a number of subsystems, each with parameters settable from BEE2 linux.

This schematic view in Fig. 5-15 shows the major components of the test bed, as implemented at BWRC, and how a user interacts with the system.

The system prototype is designed as shown in Fig. 5-16. Interference estimation and the CR signal protection is implemented with FPGA that communicates with BEE2. A programmable

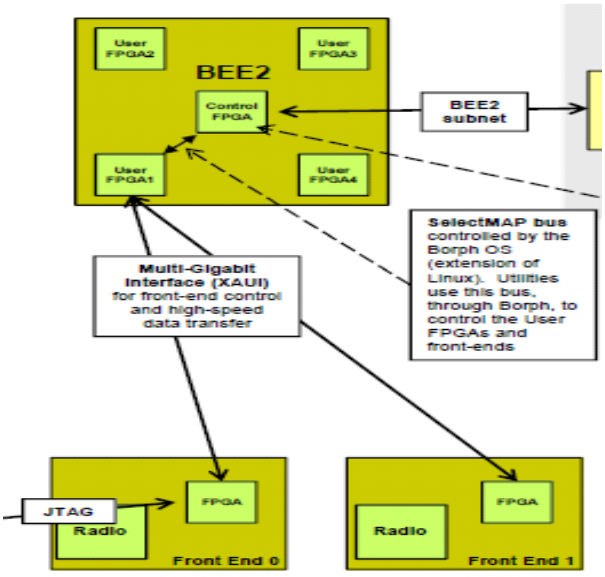


Fig. 5-15 System test bed interface with BEE2

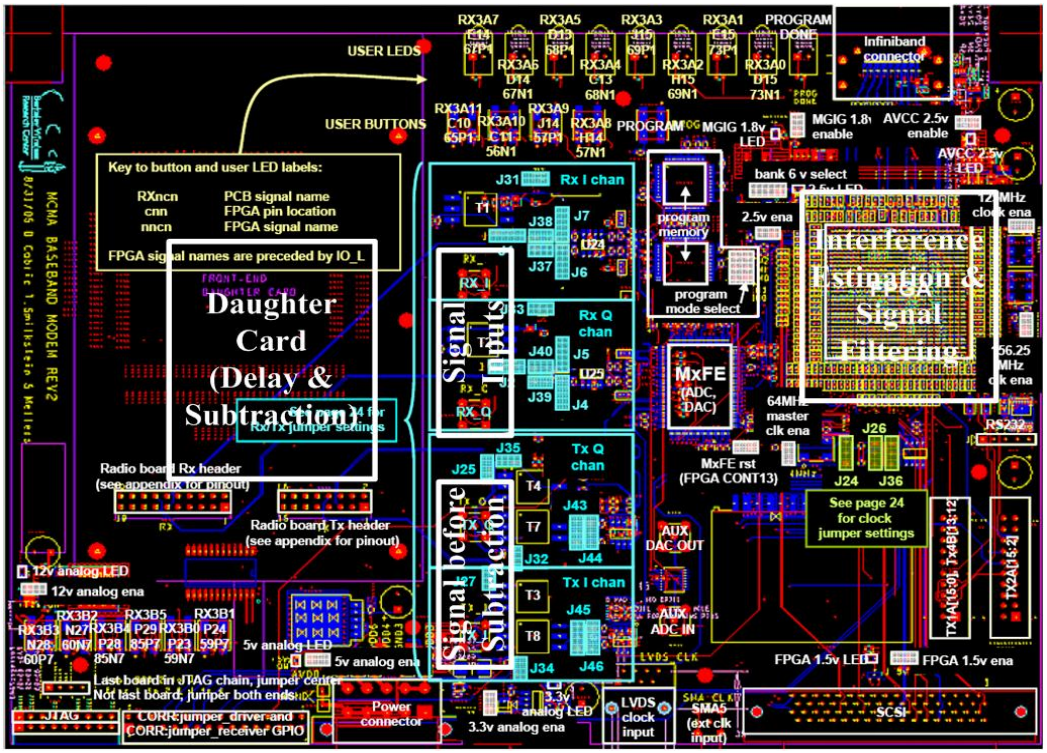


Fig. 5-16 System Prototype for active interference cancellation

resolution DAC with maximum 14 bits is included in the MxFE chip. The upper 4~6 bit MSB's could be shut down and the PGA on the chip provides a maximum gain of 20*dB*. Delay is realized by passing the input signal into a 12-bit ADC, and a 12-bit DAC, programmable delay (integer and fractional) is realized by controlled the digital parameter through FPGA. The system is further extended using a daughter card that has a serious of continuous delay cells and a programmable high gain open loop differential amplifier (0~60*dB*) that functions as the delay line, the subtraction and the gain stage respectively.

The noise level from the board allows a testing of maximum interference to signal ratio up to 30*dB*. Fig. 5-17 shows the input of *I*+*S* when both interference and the CR signal are narrow band signals, in this extreme case, with sinusoidal waveforms. When the ADC on the cancellation path is 5-bit, the DAC is 8-bit, Fig. 5-18 plots the residue signal from the first stage after the subtraction. It can be seen that the dynamic range has been reduces by 22*dB* after cancellation. It is slightly lower than expected, since the simple LMS adaptive filter implemented with FPGA could not filter out the disturbance from the desired signal, which contributes significant noise power at the cancellation path. The filtered CR signal after the second stage has been shown in Fig. 5-19. The signal is mildly distorted because no explicit protection method is employed in the DSP of cancelling.

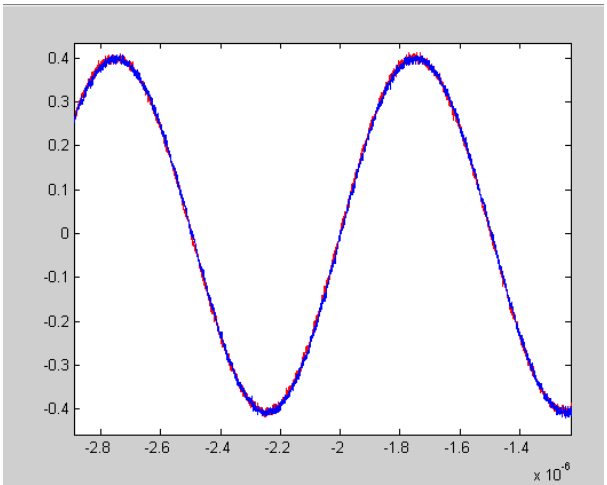


Fig. 5-17 Both interference and the desired signal are sine waves with SIR = -30*dB*.

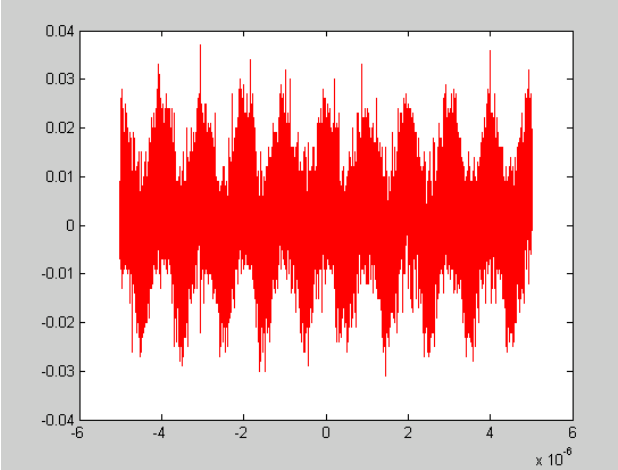


Fig. 5-18 Residue signal of the first stage after subtraction.

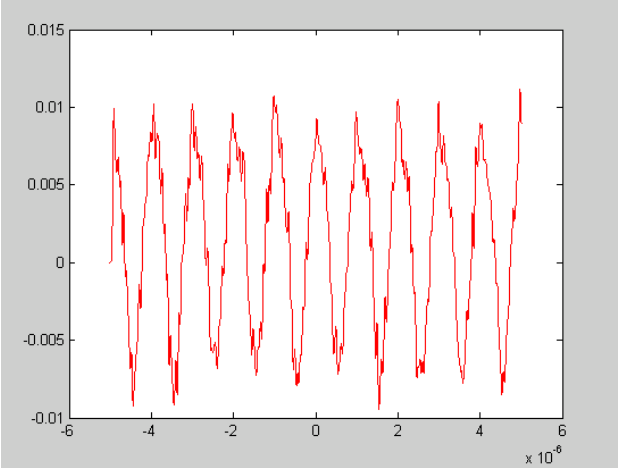


Fig. 5-19 Desired signal after filtering.

As we discussed in Chapter 3, the LMS algorithm is fundamentally insensitive to a Gaussian signal. We've further explored this characteristic by input a sinusoidal interference with a desired signal that is coded as random noise (Fig. 5-20). The estimation error (Fig. 5-21) depicts that the interference has been reduced by almost 40*dB*. Thus fully verifies a proper use of 5-bit ADC in the SIR environment of -25*dB*. The signal recovered through the second stage is shown in Fig. 5-22.

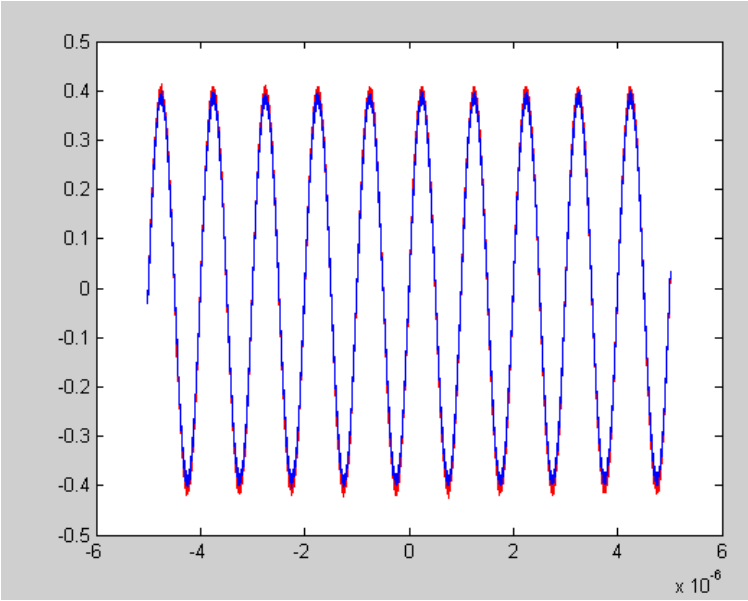


Fig. 5-20 Sinusoidal interference with a random-noise-like signal (SIR = -25*dB*)

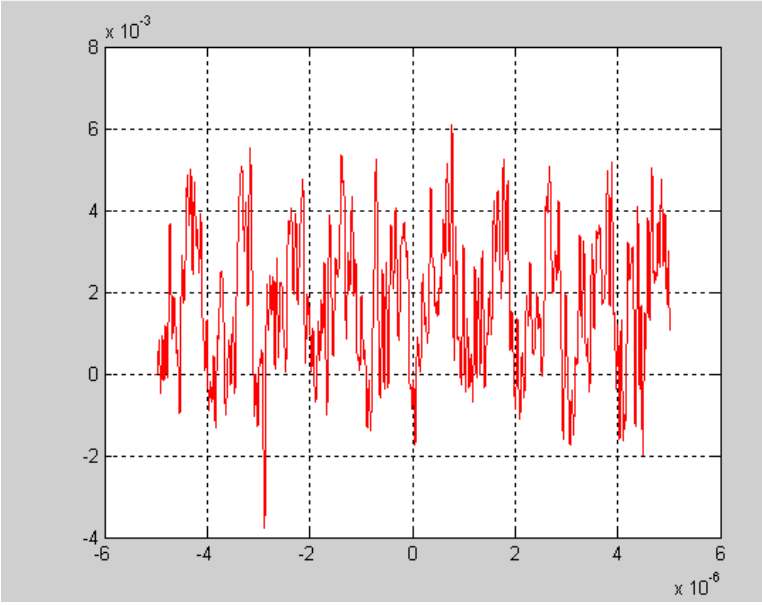


Fig. 5-21 Interference estimation error from stage one.

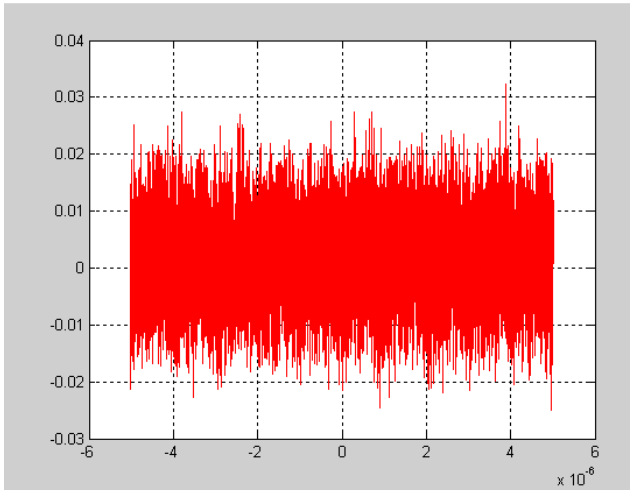


Fig. 5-22 Recovered CR signal after interference cancellation.

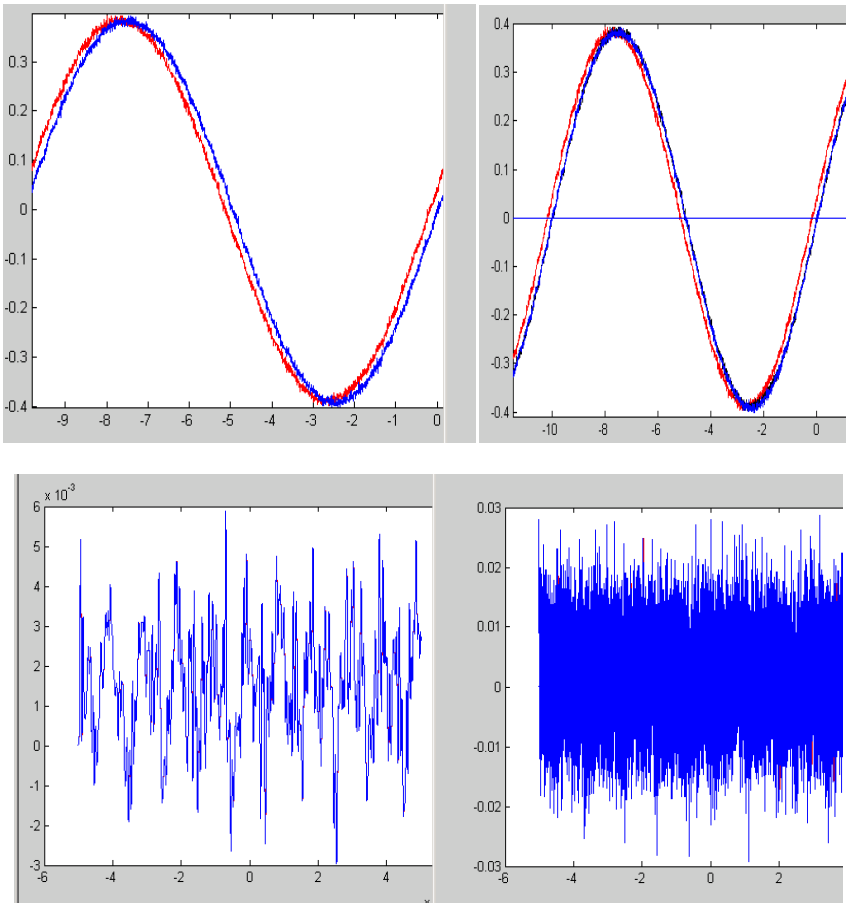


Fig. 5-23 Estimation error and the recovered CR signal when delay are not matched between two path.

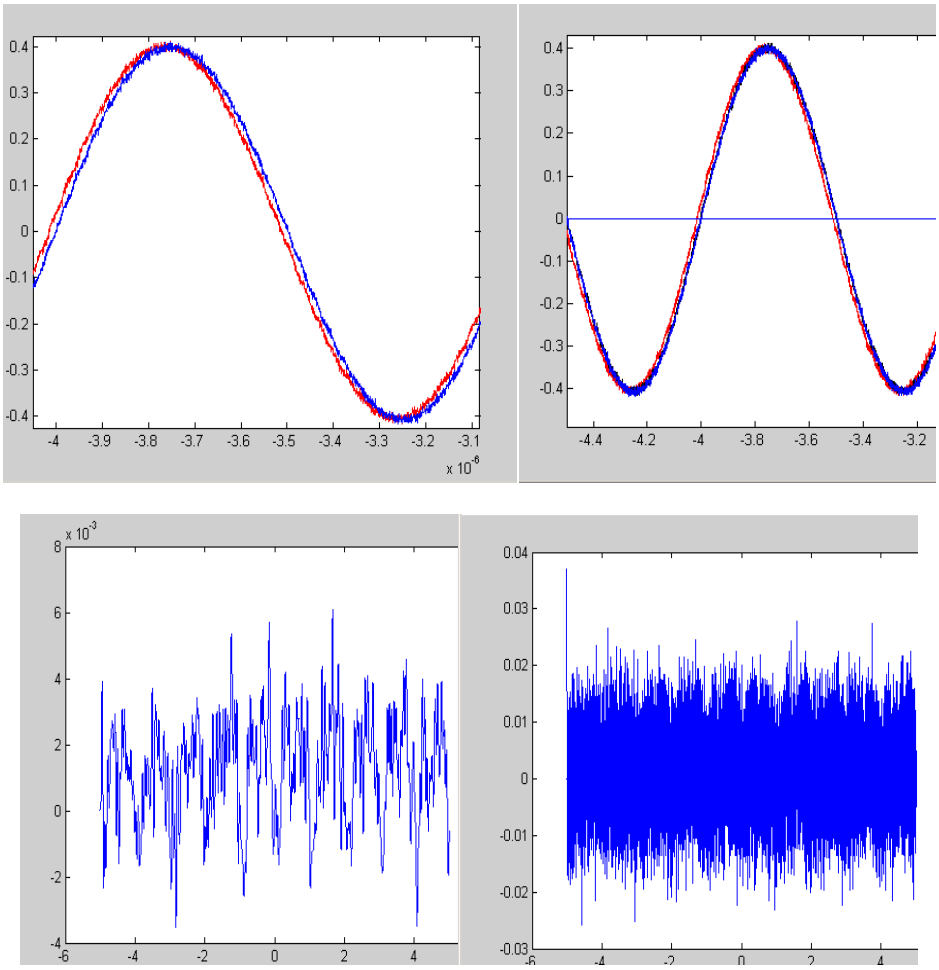


Fig. 5-24 The estimation error and the recovered CR signal when delay are better matched between the cancellation path and the main path.

The accurate delay through the analog delay line improves the estimation. This is explained in Fig. 5-23 and Fig. 5-24. The estimation error decreases almost 50% as the delay is properly matched between the cancellation path and the main path. The interference residue component shrinks significantly when signals from two paths are aliened.

From the above measured results, with a 5-bit ADC and 8-DAC, and a proper delay on the main path and desired signal protection on the cancellation path, we could achieve an interference reduction of 40*dB* in the environment of *SIR* of -30*dB*. The system is proved to significantly reduce the dynamic range of the front-end using medium resolution converters to achieve a reasonable sensitivity of the desired signal when oversampling ratio between the bandwidth of interest and the interference signal are large.

Chapter 6

Conclusions

In this thesis, an approach to reduce the dynamic range requirements for a digital radio approach which performs the analog to digital conversion after only amplification after the antenna reception. This approach is based on canceling interference using time domain subtraction. Compared to the frequency domain or spatial domain approaches, this work is believed to be eventually the most power efficient and lowest cost in terms of silicon area. It is inspired by theoretical work on interference channels identifying that strong interference can easily be detected and cancelled and is less harmful than weak interference.

This approach is especially attractive in the dynamic spectrum utilization applications, such as Cognitive Radios. These radios require vastly more frequency flexibility than present radio systems, in that they will exploit unused channels over multiple gigahertz of bandwidth.

Using a mixed analog digital system architecture which uses multiple low accuracy ADCs with digital adaptive filters, it is possible to increase the effective dynamic range of the input by subtracting off the unwanted signals in the time domain.

System architectures are proposed that serves the purpose of cancellation: both feedback and feed forward architectures. They are compared and contrasted with the feed forward structure being taken to a further level of prototype implementation. Interference cancellation is further addressed by investigating signal processing techniques (adaptive filtering) that provide processing gain to further increase radio sensitivity. A dual adaptive filter performs the function of interference estimation and signal protection which is critical to simplify the requirements of analog delay and to avoid distortion of the desired signal. Preliminary analysis on residue has

shown that by properly choosing the number of bits in the ADCs, we can achieve an Effective Bits from Dynamic Range Reduction (EBDR) equal to, or even more than N+M bits, where N and M are resolutions of the two ADCs used. The extra gain comes from the large oversampling radio between the bandwidth of interest and the narrow band interferers that improves time domain correlation between samples. System-level performance improvement has been demonstrated based on Simulink modeling.

Critical to the system implementation is a low power, cost effective solution for the analog to digital converter. An asynchronous 5 bit 1GS/s ADC is achieved by time interleaving two ADCs based on the binary successive approximation (SA) algorithm using a series capacitive ladder. The semi-closed loop asynchronous technique eliminates the high internal clocks and significantly speeds up the SA algorithm. A simple extension of the SA algorithm essentially removes the ENOB degradation due to metastability. Fabricated in 65nm CMOS with an active area of $0.11mm^2$, the ADC achieves a peak SNDR of 31.5*dB* at 1 GS/s sampling rate and has a total power consumption of 6.7mW. The power of the system is depicted low from the core ADCs.

When integrating the system, investigation revealed that a open loop gain differential amplifier, a segmented DAC, continuous-time series delay line with first order delay cell and delay control circuits facilitate a low power consumption system integration. This approach avoids the stringent requirement on sampling, compared to a traditional high speed high resolution ADC that achieves an equivalent sensitivity for the desire signal. Implementation and experimental testing of the proposed architecture proves the effectiveness of dynamic range reduction with proper delay and signal protection.

The key contributions of this work include:

- Development of mixed signal architecture for wideband time domain interference cancellation and analysis of performance under different environments.
- Algorithmic exploration for cancellation processing using adaptive filters to achieve extra processing gain and high EBDR and establishment of a system-level simulation model for optimizing specifications.
- Implementation of a low-power small-area, wide input bandwidth time interleaved high-speed successive approximation ADC whose ENOB is not degraded by metastability. These ADCs enable the interference cancellation system to be very power and area efficient.
- Experimental testing of proposed architecture to prove the effectiveness of dynamic range enhancement for Cognitive Radios and flexible future radio systems.

With a fundamental different time domain mixed analog digital architecture, this work has shown a general future radio front-end solution that allows wideband signal reception despite large in-band interference.

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