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Interconnect Aging—Physics to Software

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Doctor of Philosophy
in
Electrical and Computer Engineering

by

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To Mom and Dad

Acknowledgments

During my study and research, I have been extremely fortunate to meet and collaborate with many amazing people and machines. I could never have achieved what I did without them.

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Curriculum Vitae

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Abstract

Interconnect Aging—Physics to Software

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Device reliability or lifetime is often non-negotiable and crucial for sensitive applications such as medical devices, autonomous vehicles and space crafts. Inevitable technology advancement (e.g. miniaturization) has added unwelcome complications and unpredictability to the aging problem. Reliability of VLSI chips is jeopardized by mass transport in metallic interconnects. Material migration is caused by electrical, mechanical and thermal phenomena, and, therefore, is a complicated process. While all aspects of material migration have been studied, a comprehensive investigation that can explain and include all those phenomena simultaneously remains unsolved. Inaccuracies in modeling and predicting aging processes in wires cause that chipmakers often overdesign interconnects. This is an undesirable and expensive approach in terms of time and cost. In modern technologies, the predicted lifetime, aging, and failure mechanisms in interconnect very often do not match the observed behaviors. Unrealistic models used in CAD tools are the main culprit of such incompatibilities. In general, two situations may occur: (1) in some cases, the models may wrongly scrutinize reliability in unfailing parts and consequently impose unnecessary design tightening and (2) in some other cases, the models may underestimate serious reliability problems causing unpredicted behaviors or catastrophic failures to occur. The existing models for reliability evaluation are usually pessimistic in

case of interconnect voiding and optimistic when extrusions occur. Time-consuming and not converging reliability assessments, as well as undesired chip behaviors, are the common expensive outcome of such models.

We revisit the underlying physics of aging processes in dual-damascene copper lines. We demonstrate, that the simplistic modeling is the cause of the incompatibility of the existing models. We study all three main aging processes: electromigration, thermo-migration, and stress migration and offer several comprehensive yet compact models for realistic assessment of interconnect aging. These models explain many observations that have been inexplicable for decades. Ultimately, a computer-aided design tool, RAIN, is developed based on the proposed models and is capable of assessing the reliability of industry standard complex multi-layer, multi-segment interconnect networks. This tool can be readily integrated into other verification signoffs phases such as performance, timing, and power analyses. RAIN takes as inputs: (1) interconnect design, (2) technology specifications, (3) initial stress and temperature, (4) IR drop and lifetime requirements. It analyzes and assesses reliability and delivery requirements of all nets, and provides a report on voltage limitations, thermal violations and expected lifetime. It is validated on a wide spectrum of experimental results performed on various industry benchmarks.

Contents

Chapter 1

Introduction

Integrated circuits (ICs) constitute the core of almost all modern electronic machines that influence our day-to-day lives, from laptops, to smartphones and automotive applications. Modern digital ICs contain over a billion fundamental computing units connected by a network of billions of metal wires to perform functional and storage operations in a modern microprocessor. The computing performance of the IC is governed by two fundamental electronic components, namely: (1) transistors, which are the logic-computing units of the IC, and (2) interconnects, which are the network of metal wires linking the transistors to evaluate a desired logic function.

A consistent trend throughout the history of microelectronics has been a continuous reduction in scale. The research and development in the semiconductor industry have been guided by Moore's law [1], which states that the number of transistors in a dense IC doubles in approximately every two years. This trend has been realized in advanced IC chips by shrinking the dimensions of transistors.

The condense integration of billions of transistors and interconnects has been made possible by: (1) progress in the IC process technology enabling manufacturing minuscule

devices and wires (2) developments in IC design algorithms and methods implemented in computer-aided design (CAD) tools, enabling the efficient design of large circuits.

Improvements in IC manufacturing design and technology, guided by the predictions and guidelines from Moore's law, have resulted in an exponential increase in computing power per unit area. This arises from the individual transistor speedup and size shrinkage, allowing more transistors to be packed on a chip. Alongside with transistor shrinkage, the size of the interconnects must be also shrunk to be able to accommodate and connect the tightly packed devices. However, unlike the trend in transistor performance, which shows an improvement with technology advancement, the interconnect network shows performance degradation [2].

The rising gap between the performance of transistors and the interconnect, has become a challenge and resulted in an interconnect crisis for the world of IC design and technology.

The limited interconnect performance is unable to sustain the performance improvement in transistors which consequently creates a large stress in the interconnects. Such large electrical stress is often quantified by the current density, (i.e. the electrical current flowing per unit area through a wire). Shrinking sizes (i.e. wire cross-sectional area) and swelling performance requirements result in large current density which can cause wire wear-out, material degradation and ultimately affect the IC reliability or its capability to function properly over the lifetime of the product.

1.1. The Interconnect Crisis

Twenty years ago, for the very first time, copper was successfully employed in commercial IC chips, initially by IBM. Thanks to a wide spectrum of revolutionary advancements ranging from material science and engineering to theoretical mathematics and physics, copper could endure to date. In fact, dual damascene copper (Fig. 1.1 [3]) survived 10 technology nodes [4].

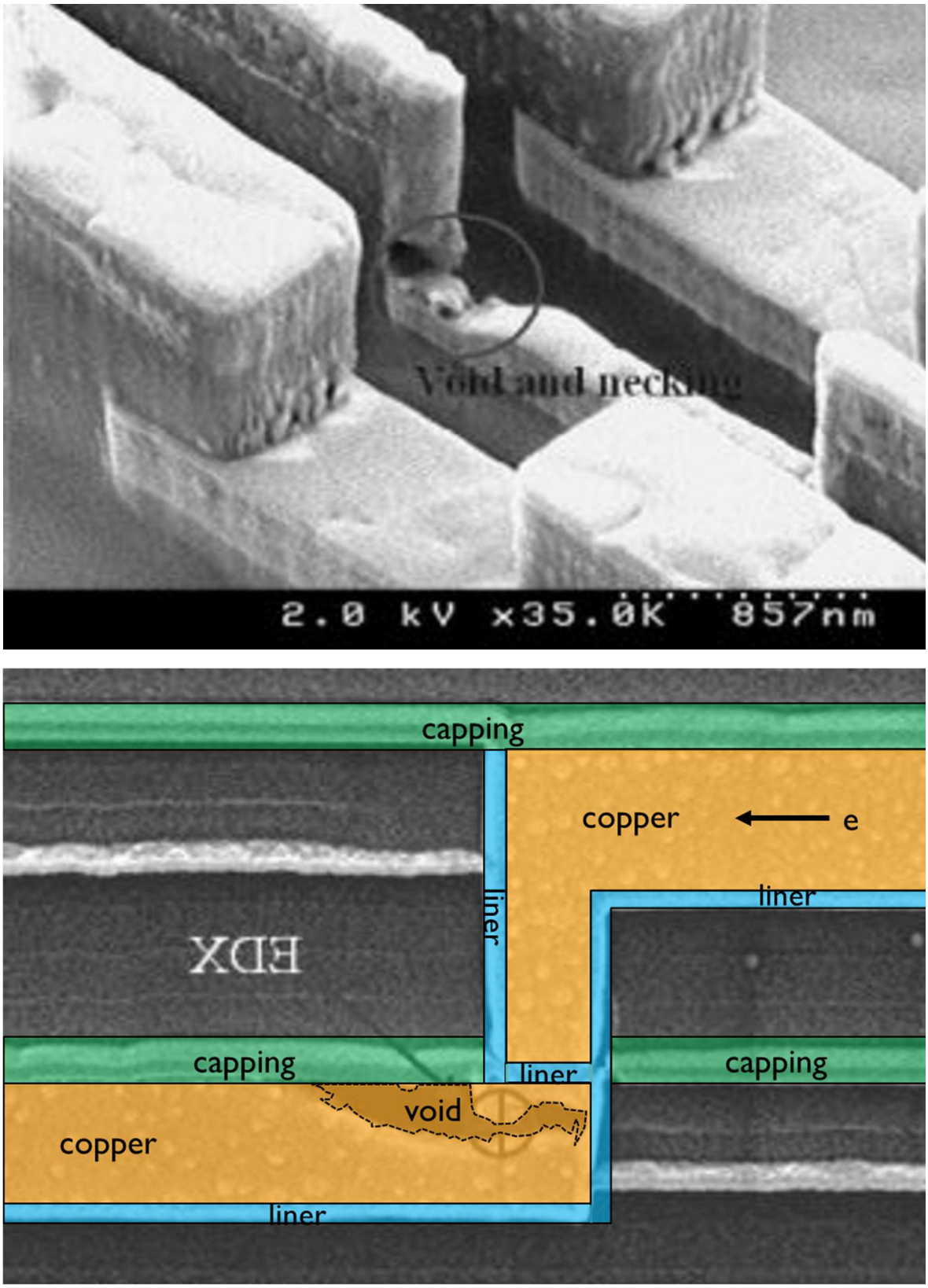


Figure 1.1. A common via structure manufactured in dual damascene Cu technology. Top view (top) and side view (bottom) of a via linking a top layer to a lower layer [3].

Moore's law, however, required much more care beyond the existing revolutionary advancements. Indeed, as it was briefly mentioned earlier, interconnect reliability presents imminent challenges to continued technology scaling. The major issues involve breakdown of porous low-*k* inter-level dielectrics and material migration induced failure in metals [5].

In one approach, reliability concerns are often mitigated by focusing on introducing new materials, alloys, or improving the capability of existing materials and processing conditions. Therefore, due to constraints such as reliability, thermal budget and manufacturing, it would not be surprising to see newer dramatic changes such as introduction of new materials. While it is expected that copper will continue to be used in coarse levels of metallization, the copper in finer interconnects is expected to be replaced by new metals or alloys such Co, Ru, Rh, Ir, Mo, or Ni with different liners and probably airgap [4].

Nevertheless, based on manufacturer and interconnect designer experiences such highly expensive approaches with an emphasis on alternative materials is unlikely to provide holistic solutions for continued scaling. As alternative solutions, the existing methods for reliability assessment are currently being adjusted hoping to explain and model newly emerged reliability problems. The latter approach has been attempted recently by many researchers. While tuning parameters and modifying existing models may offer short-term benefits, however, it also appears unlikely that merely parameter refinements of the existing methods will produce a clear path for scaling that is being sought [6].

As a result, we highlight in this thesis that a productive approach to assessing and mitigating interconnect reliability concerns lies with shifting the focus of reliability study from material explorations or existing model modifications towards understanding the underlying causes of material degradation and the impact of aging mechanisms on circuit functionality,

which has received relatively little attention up to the present. In this thesis, we focus on mass transport induced reliability and aging issues in dual damascene copper metallization-based technologies (Fig. 1.1).

1.2. Aging, Reliability and Lifetime of Interconnects

Aging in metallic interconnect in integrated circuits is due to material degradation. Such material deprivation is mainly caused by a diffusive mass transport process activated and controlled by complex electro-thermo-mechanical phenomena during or prior to device operation. While interconnect aging (i.e. material migration) involves complex degradation processes, it is simply referred to as *electromigration* [5].

Interconnect aging and lifetime have been critical reliability concerns for semiconductor industry over a long time. Recently, due to aggressive wire scaling and increasing number of interconnects on chips, electromigration has become an underlying cause of many IC chip failures. Based on International Technology Roadmap for Semiconductors (ITRS) report [2],

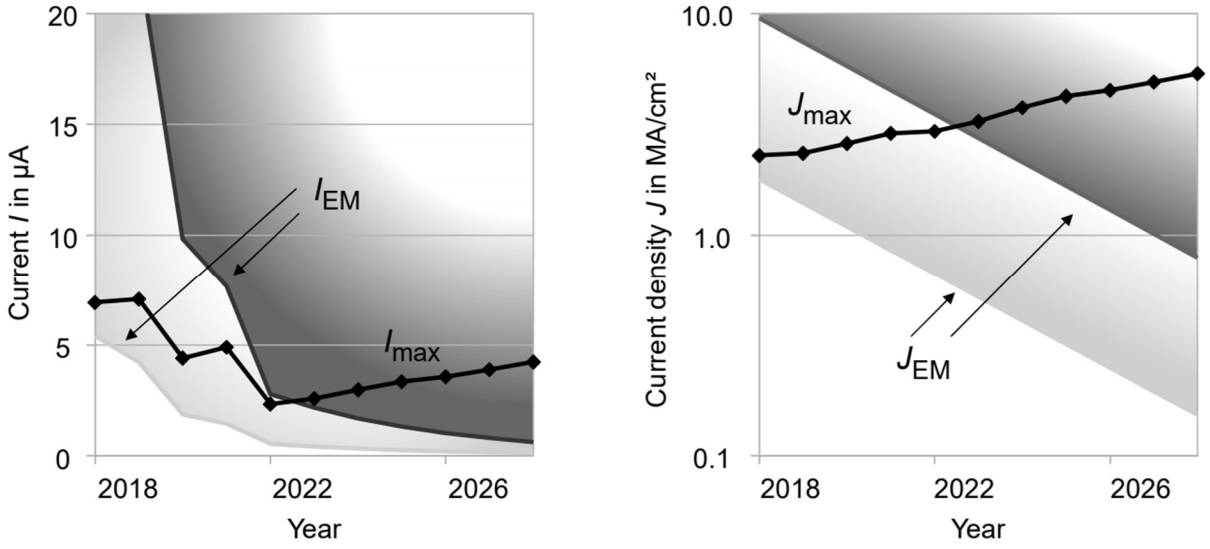


Figure 1.2. Projected values of currents, I_{max} (left) and current densities, J_{max} (right) needed for driving four inverter gates, according to ITRS [2].

on chips, the total wire length and the maximum current density exponentially increase. The trends clearly point to the increasing importance of electromigration modeling and prevention.

Fig.1.2 shows the values of currents, I_{max}, and current densities, J_{max}, needed for driving four inverter gates, according to ITRS [2]. EM degradation must be considered inside the brighter areas for both currents, I_{EM}, and current densities, J_{EM}. As of now, there are no known manufacturable solutions for the dark areas, according to ITRS [2].

1.2.1. Mass Transport

Material migration is a phenomenon of mass transport in metal wires stressed with high electrical current densities. In modern IC chips, due to the small cross-sectional area of the conductor lines, and performance requirements, the current density in wires is very high. The effect of mass transport in interconnect lines usually manifests itself first as resistance change and over time may result in shorts or opens. Fig. 1.3 shows void formation across the metal stripe causing an open (left) and hillock extrusion through a hole in overlying glass layer causing a short (right) [7].

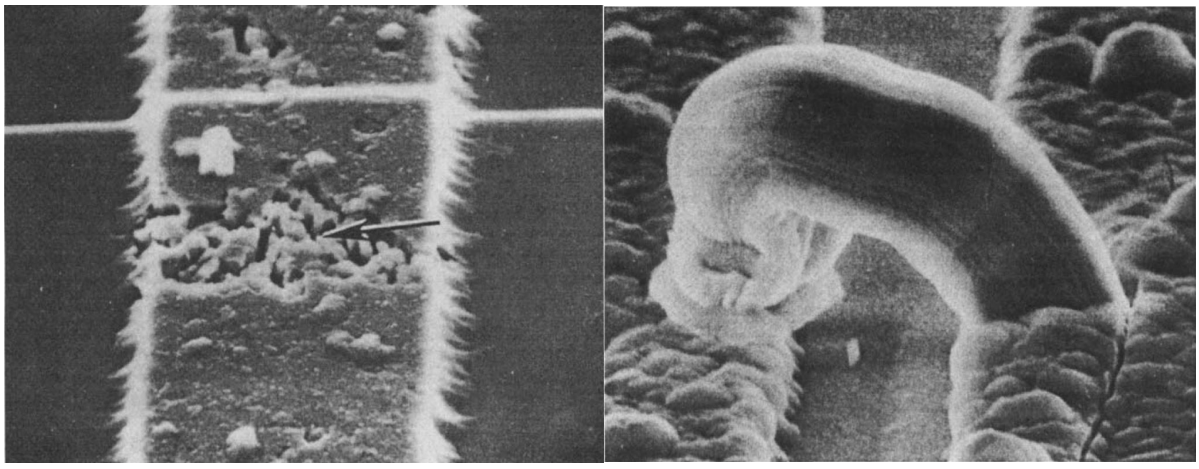


Figure 1.3. Void formation across the stripe causing an open (left) and hillock extrusion through a hole in overlying glass layer causing a short (right) [7].

A metallic interconnect is considered *reliable* if it has an almost constant material concentration across the entire length during a specific time period (i.e. several years). Change in atom concentration can occur due to different reasons ranging from electrical, mechanical, and thermal effects to material chemical properties. Atom migration occurs through a diffusion process via atom-vacancy exchange mechanism.

The mass transport can be described in terms of flux divergence of vacancies as well as their generation or annihilation by the following continuity equation:

$$\frac{\partial C}{\partial t} = -\nabla J + G \tag{1.1}$$

where C is the vacancy concentration, J is the vacancy flux, and G is the source/sink model for vacancy generation and annihilation. Diffusive fluxes of atoms or vacancies arise due to potential differences between various locations of the interconnect line [8]. These fluxes along the line depend on several driving forces, including the gradients of chemical and electric potentials. In general, the flux due to a driving force F can be written as follows:

$$\vec{J} = C\mu\vec{F} \tag{1.2}$$

where C and μ are the density and the mobility, respectively. Also, the mobility μ of a particle is given by the Einstein relation in kinetics theory as follows [9]:

$$\mu = \frac{D}{kT} \tag{1.3}$$

where D is the diffusivity, k is Boltzmann's constant and T is the absolute temperature [10]. Plugging (1.3) into (1.2) the flux related to any force can be expressed as follows:

$$\vec{J} = \frac{DC}{kT}\vec{F} \tag{1.4}$$

1.2.2. Electromigration – Action

Electromigration is the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms caused by electric field, E. It can lead to circuit failure through metal line resistance change or in the extreme the line opens or shorts.

Electric field produces an electrostatic force F_e. Collisions between electrons and ionized atoms caused by electric current also produce a force called wind force F_w. As these two forces oppose, the electric force on an activated ion in the electrical field is expressed by:

$$\overrightarrow{F_{\mathrm{EM}}} = \overrightarrow{F_e} + \overrightarrow{F_w} = eZ\vec{E} = eZ\rho\vec{j} = -eZ\nabla V \tag{1.5}$$

where e is the fundamental electron charge, Z is the effective atomic charge number, $E = \rho j$ is the electric field, ρ is the electrical resistivity of the metal, j is the current density and V is the electric potential. As F is smaller than F_w and negligible, ions tend to migrate toward the cathode end of the conductor while vacancies move toward the anode.

The flux due to electromigration (EM) can be expressed as follows (Fig 1.4):

$$\vec{J}_{\mathrm{EM}} = +\frac{CD}{kT} eZ\rho j \tag{1.6}$$

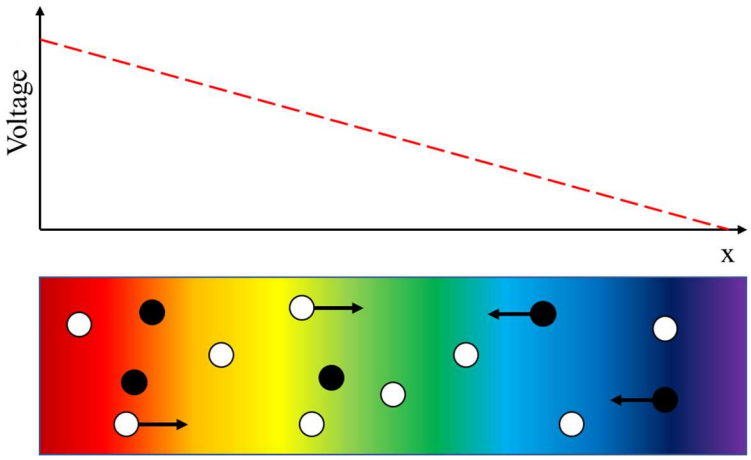


Figure 1.4. Atoms (dark) tend to travel from low to high voltages via atom-vacancy exchange.

1.2.3. Stressmigration – Reaction

As a reaction to atom accumulation at the cathode and depletion at the anode, tensile and compressive mechanical stresses develop. This stress development produces a mechanical driving force commonly called back-stress force acting against the total induced force. In other words, moving an atom (typically from the grain boundaries or dislocations) changes the volume by one effective atomic volume (i.e. Ω). This relaxation causes a strain that applies a driving force to the atom via the generated stress gradient. This relaxation causes a strain that applies a driving force to an atom or a vacancy which can be described as follows:

$$\overrightarrow{F_{\mathrm{SM}}} = -\Omega \nabla \sigma \tag{1.7}$$

where σ is the hydrostatic stress (Fig 1.5).

Accordingly, the flux due to stress migration (SM) can be expressed through:

$$\vec{J}_{\mathrm{SM}} = -\frac{CD}{kT}\Omega \nabla \sigma \tag{1.8}$$

To be precise, allowing relaxation of the atoms in a neighborhood leads to contraction where $f = (\Omega_a - \Omega_v)/\Omega_a$ is the contraction ratio. Thus, the total volume change is $(1-f)\Omega$ [11]. In addition to the stress migration caused by back stress force, high temperature

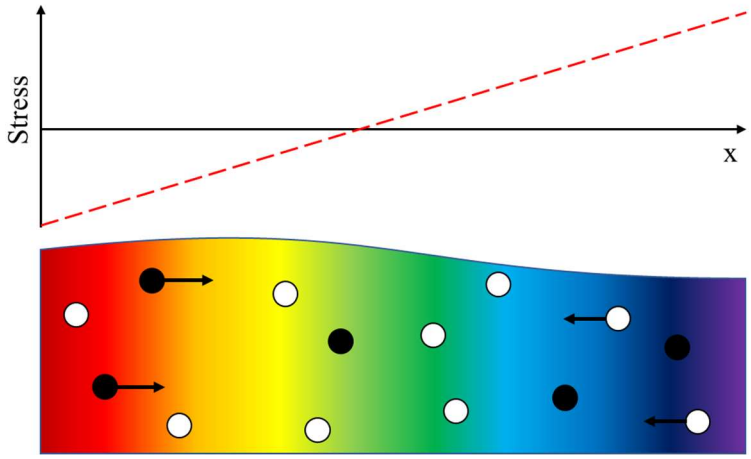


Figure 1.5. Atoms (darks) tend to travel from dense to sparse areas via atom-vacancy exchange.

processing of copper dual damascene structures leaves copper with a large residual stress due to the mismatch in thermal expansion coefficients of the materials involved in annealing process. The stress can relax with time through the diffusion of vacancies leading to the formation of voids or hillocks and ultimately open or short failures [5].

1.2.4. Thermomigration – Side Effect

Thermomigration (side effect): An immediate side effect of electromigration is thermomigration (TM). In fact, metal structure under high current density induces an inhomogeneous temperature distribution and thus an appearance of temperature gradients. These temperature gradients drive a force able to participate in the mass flow along the structure. This driving force can be described as follows (Fig 1.6):

$$\overrightarrow{F_{TM}} = -QT^{-1}\nabla T \tag{1.9}$$

where Q represents the specific heat of transport of the material.

Therefore, the flux due to TM can be expressed as [12, 13, 14, 15]:

$$\vec{J}_{\mathrm{TM}} = -\frac{CD}{kT}QT^{-1}\nabla T \tag{1.10}$$

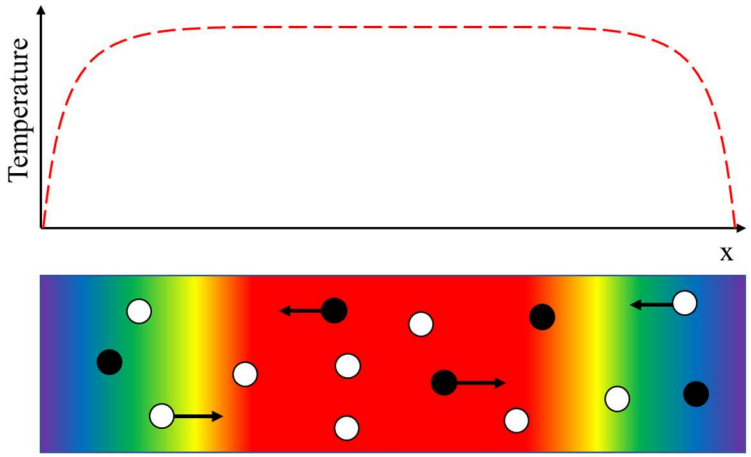


Figure 1.6. Atoms (dark) tend to travel from hot to cool places via atom-vacancy exchange.

1.2.5. Self-Diffusion Migration

A local variation in the atomic concentration can then occur during the fabrication and mostly in the grain boundary regions during the crystal growth. It can have a significant impact on degradation caused by particle diffusion induced migration.

Using the first Fick's law of diffusion [16], the relationship between the diffusive fluxes to the concentration distribution under the assumption of steady state can be expressed as:

$$\vec{J}_{\mathrm{DM}} = -D\nabla \mathrm{C} \tag{1.11}$$

It should be noted that this migration process, however, has several orders of magnitude smaller flux compared to those of EM, TM and SM and can be safely ignored.

Therefore, the overall continuity Eq. (1.1) can be written as:

$$\frac{\partial C}{\partial t} = -\nabla\ -D(\frac{C}{kT}eZ^{*}\rho j + \frac{C}{kT}f\Omega\nabla\sigma + \nabla c_{v} + \frac{C}{kT}\frac{Q^{*}}{T}\nabla \mathrm{T}) + G \tag{1.12}$$

where G is modeled differently in various works [11, 17, 18].

1.3. Life Cycle: Material Phases

Dual-damascene copper interconnect line (Fig. 1.1) encapsulated in a liner and capping layers, typically ages through a multi-phase process with various kinetics shown in Fig 1.7 [19]. The initial wire resistance R_0 changes during mass transport.

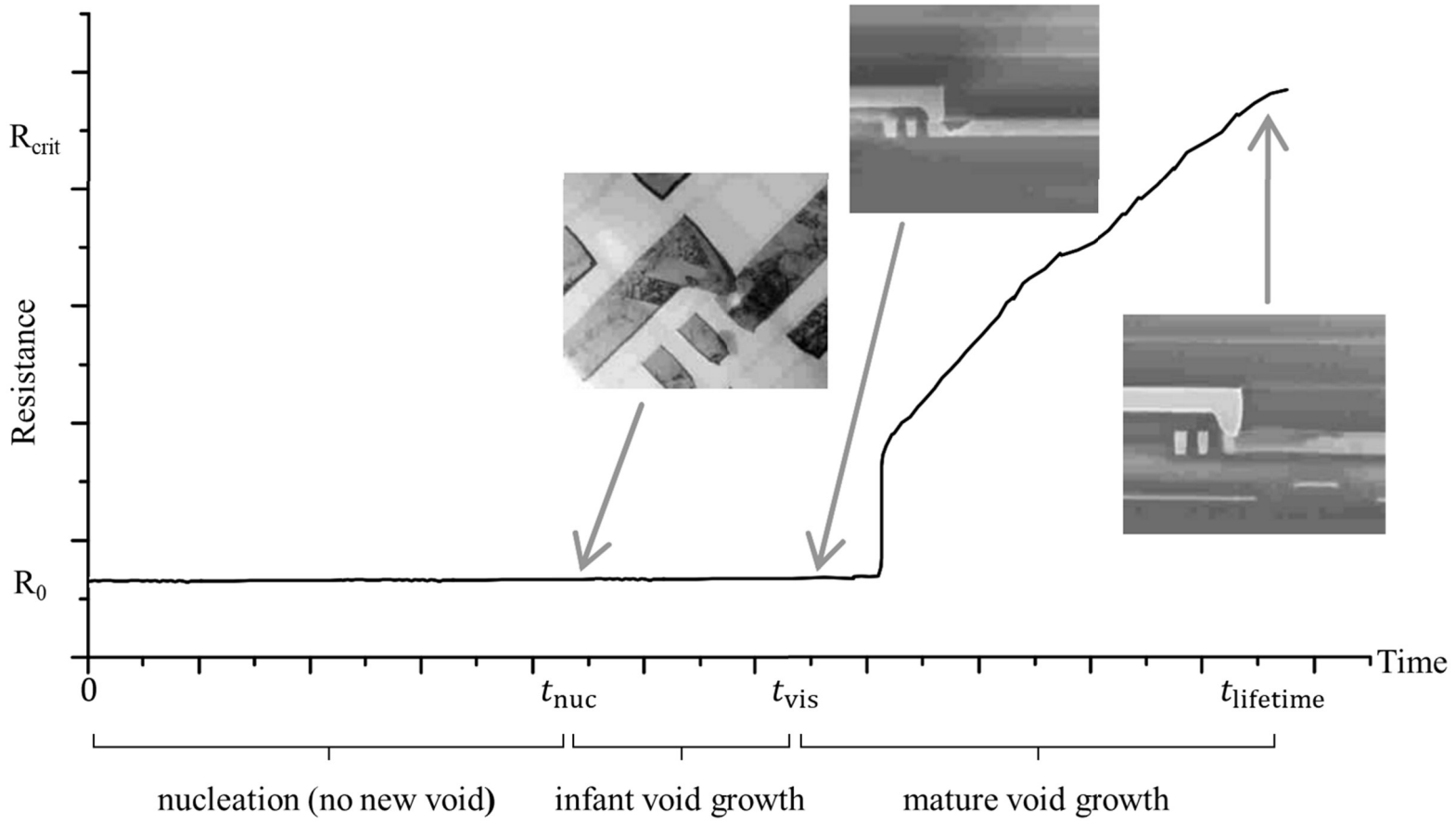


Figure 1.7: Resistance evolution during aging [19].

1.3.1. Initial Equilibrium

Before the application of electricity, the initial lattice contains pre-existing impurities, flaws or porosities created during processing (e.g. annealing).

1.3.2. Void-Free

As soon as a high current density is applied, atoms travel and their concentrations change across the network, however no voids or hillocks are formed yet. This stage can be considered as the evolution of atom concertation without appearance of new voids.

1.3.3. Nucleation

In some wire segments, if the applied current is large enough, atoms may be depleted or accumulated abundantly such that voids, or hillocks would sprout. Defects are usually nucleated around grain boundary dislocations, triple points (i.e. where three grain boundaries intersect and form a fast track atom-vacancy transport channel) and interfaces. The time to reach these critical points where a small defect nucleates is referred to as the *time to nucleate* and denoted as t_{nuc}. Critical atom or vacancy concentrations are required for a defect to form. It will be shown that these critical concentrations can be translated into hydrostatic stress. In other words, large depletion or accumulation of atoms inevitably generate tensile or compressive stress.

A critical tensile stress is required for a void to nucleate. Likewise, a critical level of compressive stress needs to build up for a hillock to extrude. The criteria for void nucleation or hillock formation are commonly referred to as *immortality conditions* and will be discussed in next chapters in detail. The condition for a void to nucleate in simple end-to-end strip can

be stated in terms of a critical stress. This criterion can be expressed as a current density-length product [20]:

$$jL > jL_{\text{crit}} = \frac{\Omega \Delta \sigma_{crit}}{eZ^* \rho} \tag{1.13}$$

1.3.4. Early Defect Growth

Still, during early stages of growth, induced flaws remain electrically undetectable (i.e. infant void or hillock embryos) since they affect the line cross section only over a small area. Thus, resistance is considered to be almost constant. Depending on the type of void (e.g. slit-like or trench like) and interconnect configurations, this stage may require void growth in both horizontal and vertical directions and thus due to its complexity, this stage is often ignored in reliability analysis. It can be seen in Fig 1.7, that the time for a void to be electrically visible is, indeed, not small and comparable to the entire lifetime (i.e. t_{vis}).

1.3.5. Late Defect Growth

Some induced flaws may become large enough (mature defects) to span the whole section of the line (i.e. critical volume), forcing the current to go through the highly resistive barrier layer. Indeed, the liner acts as a shunt layer and allows the further growth of the void, causing a progressive resistance change. The time where a defect is large enough to be electrically visible is referred as t_{vis}.

EM theory presented above can be employed for the description of the post-voiding stress evolution, by combining it with phase-field methodology [21]. This method allows to get zero normal stress on the void surface which is mathematically and physically crucial in stress based void motion analysis. Voids act as sinks for vacancies: outflow of atoms from the void surface

is considered as inflow of vacancies, resulting in motion of the void-metal interface. However, such methods due to their inevitable complexity are best fit for technology computer aided design (TCAD) analysis rather than those on the computer aided design (CAD) level.

Nevertheless, a void formed in a wire increases the resistance and may finally result in fatal failure. Einstein's equation relating the drift velocity of the void surface can be expressed using the atomic flux as [22]:

$$v = \frac{D}{kT} eZ^* \rho j \tag{1.14}$$

This relationship can be used to extract the wire resistance change. Yet, the complete analysis of growth phase is complicated and can be captured by morphological void evolution models based on phase field model techniques [21].

1.3.6. Failure

The void growth continues until a threshold resistance change occurs. Typically, 10-20% resistance change is a critical rate for declaring failure or poor performance (i.e. meant time to failure).

1.3.7. Saturation

The resistance continues to change until a new steady state is reached in any segment. Then, resistance evolution will be altered according to the new steady state. In any transitions between two stages listed above (e.g. nucleation and growth) a new steady state (e.g. no nucleation at all, saturated voids) may happen. In all cases, the defect volume is saturated, and the resistance will stop changing. This time for a defect to become bodily saturated is referred as *time to saturation* or t_{sat}.

If the void forms in an area that does not completely block the current flow the wire may still conduct current. A void may continue to grow as the current is shunted around it until the electron wind force and the back-stress force balance each other. In this situation, the interconnect line is considered immortal if the resistance change is less than the ΔR_{th}. In this case immortality is based in the saturation and expressed by:

$$(jL)_{\mathrm{sat}} = \frac{\rho/A}{\rho_1/A_1}\frac{\Delta R_{\mathrm{th}}}{R}\frac{2\Omega B}{Z^* e\rho} \tag{1.15}$$

where ρ and ρ_1 are the resistivity of conductor and shunt layers, respectively; and A and A_1 are the cross-sectional areas of metal and shunt layer; and R_0 is the initial resistance of the line.

While there might be some other possible mechanisms (e.g. void shrinkage, merging or division), this process has found to be the most common aging mechanism (See Fig. 1.6).

1.4. Critical Stress

Void (hillock) nucleates typically near the cathode (anode) end of a line when the ever-increasing tensile (compressive) stress creates a condition for a stable growth of flaws located at the loose locations such as metal-barrier interface. An estimation of the critical stress needed for forming the growing defect on the basis of the classical model of the homogeneous nucleation [23] can be found in [22, 24]. It is shown that introduction of a flaw (of a radius r_{f}) into a solid stressed with a tension σ changes its free energy. Assuming that a defect embryo can be originated from a pre-existing flaw only, we can conclude that the flaw with the initial size r_{f} will grow if the stress exceeds the following value:

$$\sigma_{\mathrm{crit}} = \frac{2\gamma}{r_{\mathrm{f}}} \tag{1.16}$$

where γ is the surface energy per unit area. The assumption about the pre-existing flaws needed for the void nucleation is supported by calculations done in [24]. They have demonstrated that an enormous energy is required for the homogeneous nucleation of the critical void by agglomeration of vacancies. By their estimation, performed with the representative values of $\gamma = 1\,J/\mathrm{m}^2$, a preexisting flaw with the size of 4nm will start growing when the hydrostatic stress will reach the level of 500MPa. Hence, the void nucleation time can be determined from the known kinetics of stress evolution caused by electric current density stressing as the instant in time when stress reaches the critical level of σ_{crit}.

In addition to defect formations at the end of a stripe, where divergence in atomic flux occurs (atom flux is terminated at the barrier interface), additional defects can be nucleated at any location characterized by the atom flux divergence. Essentially, the triple points are formed by intersections between grain boundaries (GB) and the top dielectric barrier, or contacts between three neighbor grains. Those triple points where the number of outward diffusion channels exceeds the number of inward channels, which can be responsible for the flux divergence, can cause depletion in metal density, leading to the development of tension and possible void nucleation [5].

1.5. Via Configuration

A mature dual damascene technology process involves many chemical and physical steps. What matters to the reliability community is where are the copper diffusion-stops and barriers. Also, physical properties of materials and surfaces further provide information on detecting fast track and finding out the effective diffusion. A simplified yet common dual damascene process is depicted in Fig. 1.8.

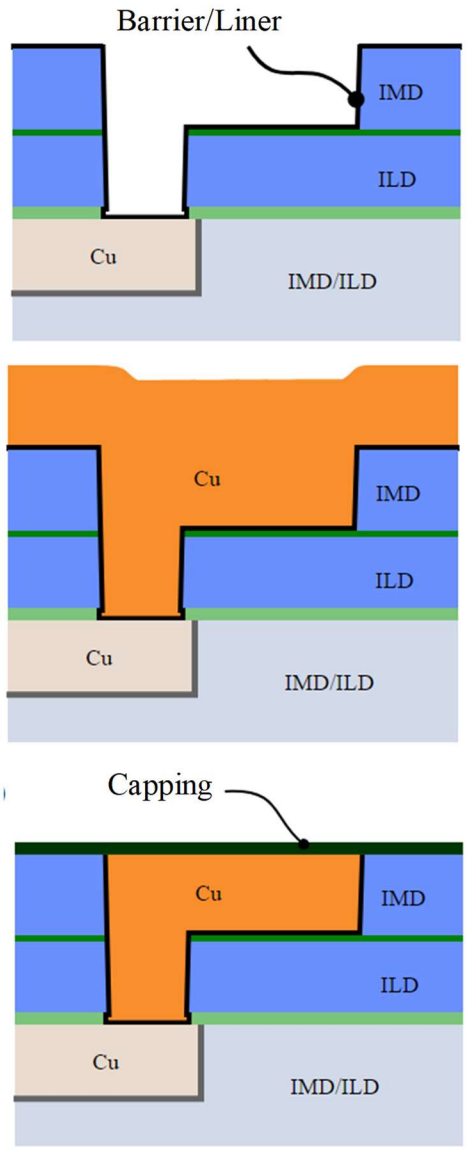


Figure 1.8: Last stages of a simplified common dual damascene process.

We show how via configurations affect the void formation and growths. There are two via configurations: (1) downstream where the electrons flow from the upper layer to the lower layer, (2) upstream where the electrons flow from the lower layer to the upper layer. Depending on the configuration and void type the time to failure as well as the failure mechanisms may vary.

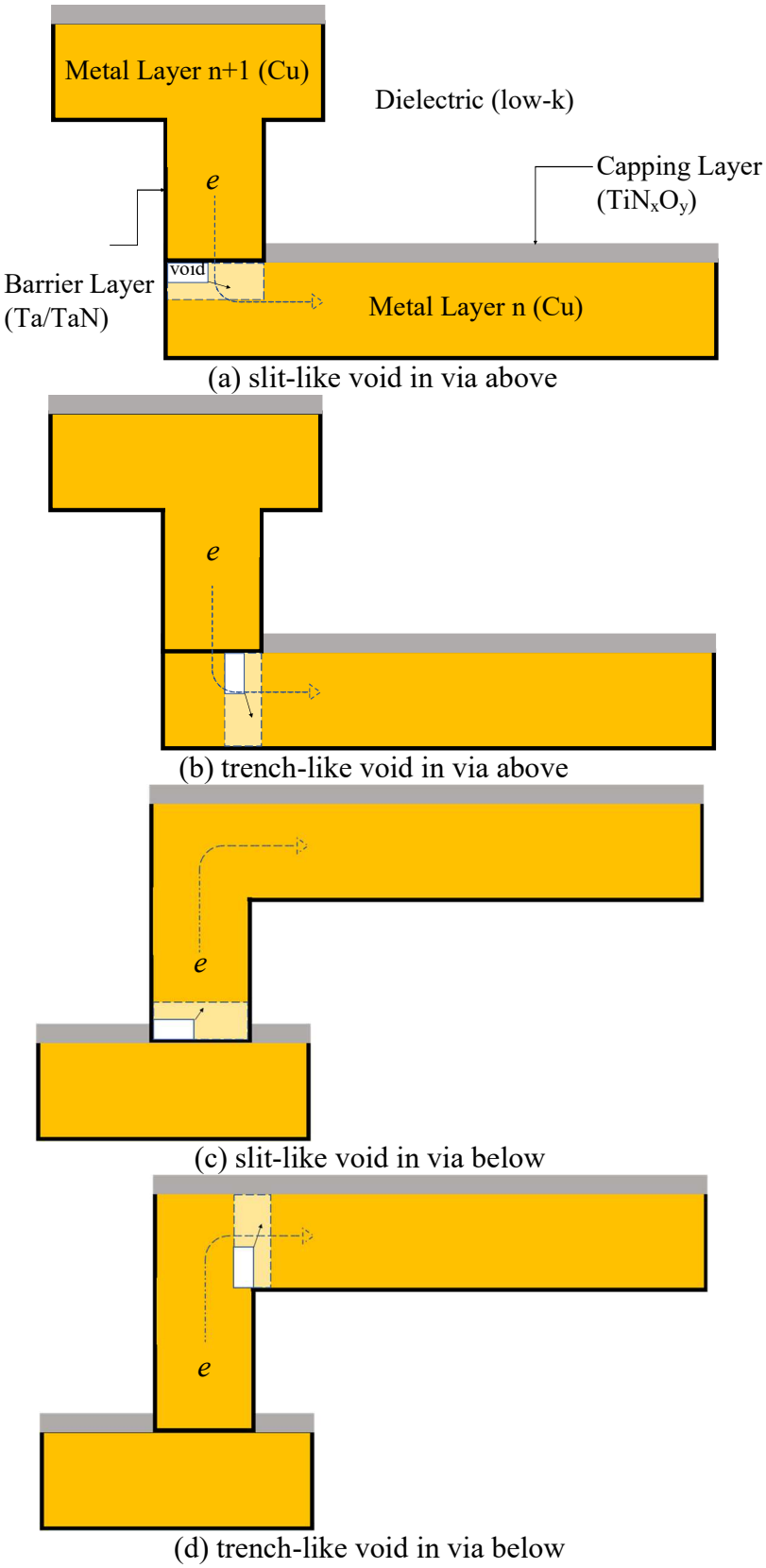
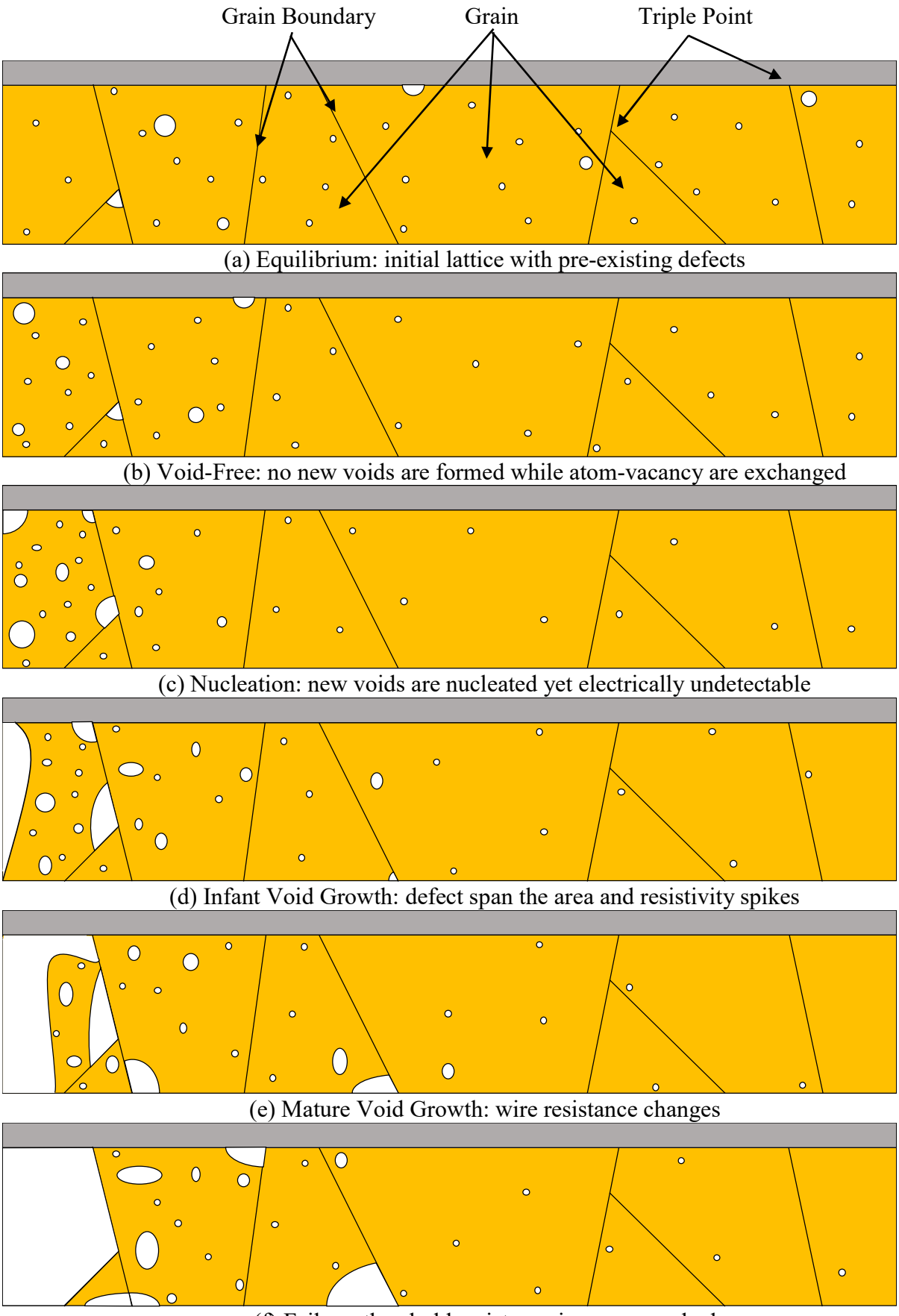


Figure 1.9: Failure modes in via above/below configurations in a common dual damascene manufactured wire.

For a slit-like void which usually nucleates under or above a via, the failure happens when the void spans the cross section enough to block the whole current path. This failure mechanism is often referred to as early mode failure. On the other hand, for a trench-like void which usually appears somewhere inside the line, rather than at a via location, sprouted from a triple point or weak interface the void usually needs to span vertically (and/or horizontally) and form a detrimental void. This failure mechanism is often called the late mode failure. Different line and via configurations in presence of various voids are depicted in Fig 1.9. A more general and realistic kinetics for void formation and motion in each stages of evolution are illustrated in Fig. 1.10.

Authors in [20, 25] show that in mature dual damascene technology, $(jL)_{\mathrm{crit}}$ in (1.13) depends on the via configuration at the end of interconnect line. For a via-above structure (i.e. via to the upper level metallization), a tiny void under a via may result in a complete blockage of the current path (Fig. 1.9 (a) - (b)). In this case, $(jL)_{\mathrm{nuc}}$ value is of about 1500 A/cm. On the other hand, for via-below (Fig. 1.9 (c) - (d)) current path is more resilient to EM, the void needs to grow and span across the width and height of the line. In this case, $(jL)_{\mathrm{crit}}$ is reported to be of about 3700 A/cm. While the extrusion is not the primary failure mode, similar studies and experiments were carried out to obtain the critical compressive stress and jL product for extrusion and dielectric breakage [26]. The via configuration effect will be discussed in the next section with further details.



(a) Equilibrium: initial lattice with pre-existing defects

(b) Void-Free: no new voids are formed while atom-vacancy are exchanged

(c) Nucleation: new voids are nucleated yet electrically undetectable

(d) Infant Void Growth: defect span the area and resistivity spikes

(e) Mature Void Growth: wire resistance changes

(f) Failure: threshold resistance increase reached

Figure 1.10: Defect life span during mass transport.

1.6. Classical Models

1.6.1. Lifetime Analysis

An important objective in electronic design is to deliver a device which ages slowly enough such that during its use time it may be considered reliable with expected performance. Therefore, a key information in the context of reliability is the device's mean time to failure or lifetime.

Since the wire resistance is progressively changing during mass transport, it is, therefore, critical to make sure that the interconnect networks can deliver the required signal or power. Voiding and extrusion, which are the extreme manifestations of mass transport alter the interconnect resistance and consequently affect the voltage or signal levels. A certain level of increase or decrease in resistance can be tolerated. Typically, when a considerable amount of change in resistance (e.g. accumulation or depletion leading to 10 to 20% change) occurs, the wire is considered permanently damaged. This change in resistance can end up causing: (1) Voiding: open or very low performance due to poor signal (2) Extrusion: short, leakage current or overheating due to current crowding in hillock area. One of the most widely employed for mean time to failure estimation is Black's model [27].

Black's model: Black considered electromigration (EM) as the sole driving force for material transport induced failure. He assumed that the mean time to failure is inversely proportional to the rate of mass transport due to atom flux caused by EM. Since EM is the consequence of momentum transfer between conducting electrons and metal atoms, the rate of mass transport is proportional to the density of ions, the density of conducting electrons and their momentum. He further assumed that the two latter quantities are proportional to the

current density, j. The former quantity is also known to follow an Arrhenius equation, where E_a is the activation energy for the reaction, k is the Boltzmann constant and T is the temperature. Hence, he derived the following model for the mean time to failure:

$$MTF = \frac{A}{j^2} \exp\left(\frac{E_a}{kT}\right) \tag{1.17}$$

where A is a constant which encompasses the material and geometrical properties of the interconnect [27].

1.6.2. Stationary Analysis

As it can be seen in Fig.1.7, the time for a defect to nucleate is quite a significant fraction of the whole aging process and the overall lifetime. Indeed, the nucleation of a defect is the most critical information in reliability analysis context as it determines whether a wire is immortal or not. The most commonly used model for immortality checking was developed by Blech [25, 20].

Blech's model (defect nucleation): Mass-transfer induced aging in metallic interconnect caused by application of electric field, electromigration, has mechanical manifestations. Blech studied electromigration in thin aluminum films on titanium nitride, linked the electrical load to mechanical stress and suggested that stress build up is a possible explanation for EM retardation (Fig. 1.11). This relationship is stated as [20]:

$$\frac{\partial \sigma}{\partial x} = \frac{eZ\rho}{\Omega} j \tag{1.18}$$

where σ is the hydrostatic stress, e is the fundamental electron charge, Z is the effective charge number, ρ is the electrical resistivity of metal and Ω is the effective atomic volume.

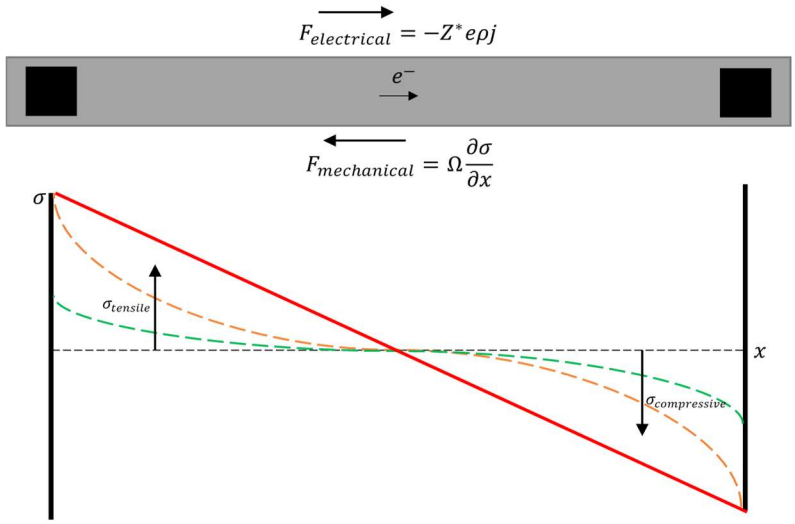


Figure 1.11: Stress evolution as a result of electron wind force and back stress force.

Blech showed that the steady-state condition for wire mortality threshold requires that the forward electromigration flux is balanced by a backflow flux due to gradient of stress (i.e. zero net flow). In other words, critical amount of hydrostatic stress is required for electromigration to occur. If the stress difference between the cathode and anode ends is less than that needed for nucleation, the stress profile will evolve towards a steady state at which point the net atomic flux becomes zero and the wire is considered immortal. This is captured as a criterion on current density and length product:

$$\Delta\sigma = \frac{eZ\rho}{\Omega} jL \tag{1.19}$$

Given the critical stress, the maximum stress that a conducting line can withstand, a critical jL product for electromigration in relation to stress-migration is called *Blech produc*t. There are usually two critical stresses for the maximum compressive and tensile stresses required for extrusion/hillcok (σ_{crit}^{h}) and voiding (σ_{crit}^{v}) to occur. They are essentially filters for determining the interconnect resilience to mass transport failure. This model is widely used in many reliability assessment CAD tools.

1.6.3. Transient Analysis

Blech observed and formulated the relationship between electromigration and stress. His work laid out the foundation for further advanced models. However, he did not explicitly address the hydrostatic stress evolution during the mass transport process. Korhonen developed a new model for transient evolution of voids [11, 28]. This model has been widely accepted by the research community.

Korhonen's model (evolution): As it was mentioned, a true reliability assessment must be obtained through material concentration. Prior to Korhonen's model, there existed some older models based on Eq. (1.1) such as those presented in [17, 18]. However, gradient of concentration and electromigration were only considered as atomic flux driving forces. These modelling faced several limitations, among them an unrealistically low vacancy concentration for reaching the steady state and therefore unrealistic time for reaching the steady state. Consequently, employing those models for failure assessment results in inaccurate judgment. Shortcomings of those models were caused by not considering the back-stress force against electromigration that was observed by Blech.

Kirchheim [11] introduced the first model based on Eq. (1.1) where he added an explicit driving force and therefore an individual atomic flux due to stress gradient beside electromigration flux. His model is the first true model reflecting the basis in Eq. (1.1) and is capable of capturing many physical effects. The model was devised based on volume change due to lattice relaxation. In this formulation, the generation/annihilation term, G, was modelled through the volumetric strain caused due to generation or annihilation of vacancy. The rate of volume change around a relaxed vacancy was described via Hooke's law as the deviation of

vacancy concentration from its equilibrium, c_{eq}, within the characteristic vacancy relaxation time, τ. His model for vacancy generation and annihilation was similar to that of [17] but more accurate as he also considered a stress dependent equilibrium concentration. He further elaborated on different mechanisms of vacancy generation and annihilation in interfaces, grain boundaries and dislocations. The characteristic vacancy relaxation time is often considered as constant value and it has a significant impact on the overall stress development. In addition to this drawback, those models form a non-linear system of differential equations which must be solved numerically. To overcome such complications, Korhonen, cleverly eliminated the direct dependency on atom concentration and described the stress evolution along with electromigration by the following equation (Fig. 6) [29]:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[D\left(\frac{\partial \sigma}{\partial x} - \frac{q\rho}{\Omega} j\right)\right] \tag{1.20}$$

where $D = \frac{D_a B \Omega}{kT}$ is denoted for diffusivity, D_a is the atom diffusivity and B is the applicable bulk modulus. One may notice the similarity between Korhonen's model and the ones in [17, 18] where D_v is replaced by $D_a B\Omega/kT$. However, it was discussed by Korhonen that even though these models have similar expressions, using D_v as the diffusion coefficient leads to a significant difference as $D_v/D \gg 1$ [10]. That is why the models in [17, 18] resulted in unrealistically faster than expected steady state. Later, authors in [30] presented a more general model based on (1.12) in terms of both concentration and stress where they essentially obtained an identical model to Korhonen's verifying that his assumptions were reasonable. The steady state condition presented by Blech (1.19), can be deduced from Korhonen's model, (1.20). We later review the advanced models such as those presented in [31, 32, 33] which are essentially based on the extensions of classical models.

1.7. Classical Models Limitation

Classical models for interconnect aging and reliability analysis reviewed in the previous sections suffer from three main limitations:

Single Segment: These models (i.e. Black's lifetime model, Blech's criteria and Korhonen's model) are devised for single segment end-to-end interconnect lines and cannot accommodate complex structures. Devising new models based on the existing modes that can handle complex multi-segment interconnect networks is addressed in this thesis.

Temperature Agnosia: The aforementioned models are temperature agnostic as they do not take temperature effects into account as an individual aging process. The focus of those models are electromigration and stress migration as perhaps in older technologies for which those experiments were conducted, thermal effects were not as problematic in terms of aging. However, for modern technologies heating in general and its repercussions have been a life-threatening factor to interconnect reliability.

Poor Integrability: In common verification methodologies, reliability analysis takes the very last stage of physical signoff checks. Also, as it was discussed before, examining material migration induced reliability of interconnect fundamentally requires multi-physics analyses. The classical models and their extended versions are based on hydrostatic stress analysis. The multi-physical nature of mass transport phenomenon (e.g. dealing with non-electrical or mechanical factors such as hydrostatic stress) makes this stage of verification hard to integrate with other signoff steps (performance, delay, power). Due to such poor integrability, many redundant iterations between various verification steps might occur. For example, a naïve change towards EM improvement may affect other critical factor such as timing. Indeed, lack of a homogenous methodology results in unwelcome cost and time.

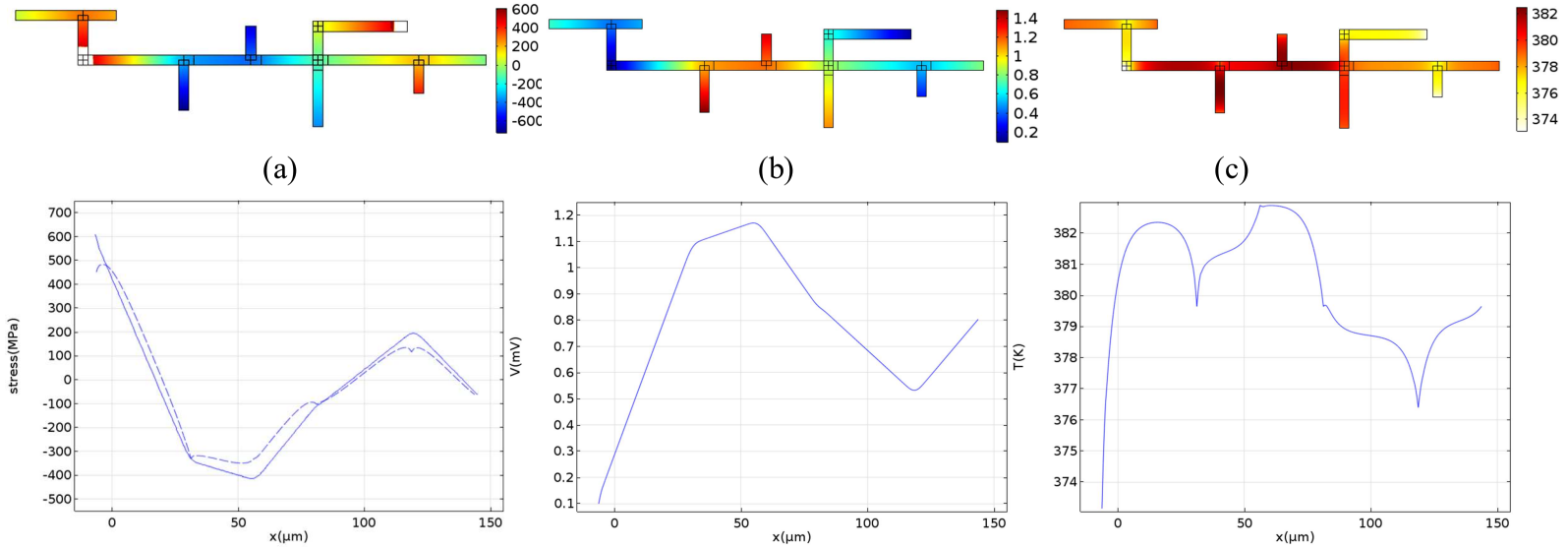


Figure 1.12: Distribution of (a) stress (b) voltage (c) temperature across a complex structure.

1.8. Motivation and Contribution

The limitations mentioned in the previous sections have been of a great concern for chip makers for a long time. Fig. 1.12, as a big picture of this thesis, shows that the explicit use of classical models for advanced technologies may result in significantly erroneous interconnect reliability misevaluation. In this thesis, we address all the three limitations stated above and propose novel models to overcome them.

Multi-Segment: Material migration in complex interconnect structures with multi-segment branches are not straight-forward. In other words, classical models for end-to-end wires cannot be employed for reliability analysis of complex nets. We investigated the mass transport phenomenon in multi-segment structures by studying stress evolution across the branches in a net. A new set of models are proposed which can accommodate complex interconnect networks with multiple nodes and branches.

Temperature-Aware: Using temperature agnostic models in verification flow is shown to be dangerous in terms of reliability misevaluation or unnecessary overdesign. Temperature has a very sophisticated mutual relationship with material migration. Since mass transport occurs through a diffusive process, therefore reliability is highly sensitive to temperature. Temperature and its distribution affect interconnect aging in various ways. Temperature profile characteristics namely temperature rise and temperature gradients not only affect other aging processes such as electromigration and stress migration but also considerably affect the aging directly through thermomigration. We discuss thermal effects on reliability of interconnects and propose new models which take temperature effects correctly into account through thermomigration.

High Integrability: True and comprehensive reliability analyses require multi-disciplinary physics where all electro-thermo-mechanical aspects of material migration are taken into account. However, other parts of verification flow mostly deal with merely electrical notations and factors. This has made the integration of reliability signoffs into other verification steps challenging. We observed an interesting relationship between non-electrical factors such as stress and temperature with electrical ones. We propose a novel mapping from hydrostatic stress and temperature to voltage. Then, a new voltage-based formalism is developed to translate non-electrical factors to voltage and can be universally used among different stages of verification such as performance, delay and power. This makes the mass transport induced analysis desirably integrated into common methodologies.

While there have been some more recent works such as [31, 32, 33] addressing some of these limitations, this thesis delivers a comprehensive research on mass transport induced aging in interconnect networks considering all electro-thermo-mechanical factors. This research contains a profound amount of experiments, observations, mathematical models based on underlying aging physics, numerical analyses and a great body of discussion.

The ultimate contribution of this research is the CAD tool, RAIN, which takes industry standard interconnect networks (consisting of multi-layer metallization stack with complex multi-segment layers) as input plus circuit analysis (e.g. SPICE) information and provides comprehensive reliability analysis taking all electro-thermo-mechanical factors into account with the focus on life time and immortality analyses.

1.9. Thesis Organization

The thesis is organized as follows:

Chapter 2 proposes a new model for immortality analysis of complex interconnect networks. The model is devised based on how stress is evolved and distributed across a multi-segment structure based on atom conservation. We show that the different segments in a multi-segment structure affect each other's lifetime and immortality.

Chapter 3 discusses the significance of thermal effects on interconnect aging. We propose a new model for non-uniform temperature distribution in interconnects under Joule heating. We show that neglecting thermal effect in temperature agnostic models and not modeling it through thermomigration may result in misevaluation of interconnect health or catastrophic unexpected failures. We propose a set of temperature-aware models for reliability assessment. We further discuss thermal effects in global and local interconnects in detail.

In Chapter 4 we present new reliability assessment models for complex multi-segment structures by extending the models in the previous chapters taking thermal effects into account via thermomigration.

In Chapter 5 we address the poor integrability limitation in classical models and propose a new voltage-based model where all electro-thermo-mechanical factors and effects are translated to voltage via a novel 1-to-1 mapping between stress evolution and voltage in interconnects line. This new transformation makes reliability signoff desirably integrable with other parts of verification methodologies such as performance and power analyses.

In Chapter 6 we present a set of algorithms which are developed based on the findings in the previous chapter. The proposed algorithms employ the models presented in this research. These algorithms are used by RAIN, which is a tool developed for full chip reliability assessment of industry standard interconnect networks.

In Chapter 7, the heat generation, its non-uniform development and distribution within interconnect is investigated in detail. We developed a completely new model based on the fundamental heat generation. The developed model not only can be utilized for reliability analysis but also for a thermal analysis standalone tool.

Chapter 8 concludes the dissertation and offers future research directions.

Chapter 2

Models for Complex Multi-Segment Interconnect Structures

Majority of the existing experimental, theoretical and modeling works on electromigration (EM) are focused on simple, via-to-via structures, but complex interconnect structures have not been studied well. The lack of correct models for such interconnects may result in either conservative or weak design decisions which may result in catastrophic reliability failures. In this Chapter, we propose a physical model which holds for material migration as well as for lattice vacancy generation/annihilation. Using the developed model, we examine well known circuit level EM assessment methods by finite element modeling and simulation. This Chapter provides a compact model for EM analysis which can be employed in CAD tools. We also explain some recent experimental results and empirical models published by other researchers.

2.1. Introduction

EM in IC chip interconnects, especially in power delivery network has been investigated for a long time. Many experiments have been carried out to help finding more EM resilient materials [34]. Several physics-based and TCAD models have been developed to capture the EM phenomenon including material and topology effects [11, 35]. On the other hand, circuit level EM assessment and validation techniques have not advanced at the same rate. Pioneering research conducted by Blech resulted in a compact EM validation criterion which determines the critical current density – wire length (jL) product for void nucleation [20]. This study was performed for simple via-to-via interconnects. However, extending of Blech criterion to complex structures is still an active research. Foundries usually provide EM rules-based conditions on the interconnect geometry and current density for a specific technology. Industry standard CAD tools still use end-to-end Blech-effect-based techniques to determine mortality and immortality of net segments. Recently some EM assessment techniques have been developed [36, 37, 38] to address EM in complex structures.

Establishing an EM assessment method is difficult because modeling of EM involves many underlying physical phenomena – those are difficult to observe, perceive and therefore model. Moreover, solving multi-physics equations of electromigration requires computationally complex numerical methods and capturing the results as a descriptive, comprehensive, scalable and accurate model is challenging.

Most of the circuit-level EM studies have been performed for simple interconnect segments with blocking boundary conditions at both ends. Authors in [37] developed a methodology for circuit level EM assessment based on the findings in [36]. This method extends the Blech

criterion (jL_{crit}) from one segment to a multi-segment tree. They showed that the maximum stress difference in an interconnect tree $\Delta\sigma_{max}$ is given by the path with the greatest sum of segment jL products. The effective jL product (jL_{eff}) is then calculated and compared to the jL_{crit_nuc}. In this method, $\Delta\sigma_{max}$ was assumed to be equal to $2\sigma_{crit\_nuc}$ where σ_{crit_nuc} is the critical tensile stress for a void to nucleate. This assumption can be valid for symmetric structures. However, in multi-branch nets with arbitrary topology, jL_{eff} may reach $\Delta\sigma_{max}$ but void nucleation may not occur since the stress in cathode is less than σ_{crit_nuc}. Such situations occur for critical compressive stress for low-k dielectric breakage or extrusion. Immortality of a wire should be studied jointly with other wires connected within the same net. The amount of hydrostatic stress experienced by a wire depends on the stress in other segments. Therefore, a true EM validation can be achieved by obtaining stress distribution in the entire net. To include the effect of other connected segments, authors of [38] proposed a method to calculate effective current density based on atomic flux divergence at via nodes. This method only explains the effect of immediately adjacent segments and does not include the effect of other segments in the net, passive extensions or their material properties. It is known that Blech criterion for the end-to-end connection cannot be directly applied to multi-branch nets as it does not explain how connected segments affect each other.

In this Chapter we present a detailed, systematic study of Blech effect-based model for EM in complex structures including the effect of adjacent segments and take into account current density as well as geometry, topology and material properties of interconnect. The presented model applies to passive and active elements.

The model is justified not only by FEM simulations but is also matched to experimental observations. Finally, the Chapter provides insights for designers to take advantage of some

structures and adopt them to make the design more robust to EM. The presented model can easily replace the limited solutions in CAD tools which are mainly based on Blech analysis of straight end-to-end wires.

2.2. Extending Blech's Model to Multi-Segment Complex Interconnect Networks

Electromigration has been studied extensively for simple interconnect segments with blocking boundary conditions at both ends. Stress evolution, void nucleation and failure conditions are well established for such structures. The compact model for simple structures is known as *Blech length* or *Blech effect* [20, 25]. In this work we consider copper (Cu) interconnects manufactured in dual damascene technology. We say that a connection is simple if it consists of a straight segment of Cu wire terminating at both ends at a via or a contact. An interconnect tree, also referred to as a net or a complex interconnect, consists of a Cu structure within one layer of metallization which terminates at diffusion barriers such as vias or contacts. The diffusion barriers allow electrons to pass through but block the movement of atoms. The finite element simulations are performed for direct current (DC) in bamboo-like dual damascene Cu interconnects with Ta liner, and SiN_x capping embedded in a low-k dielectric.

Authors in [36] extend the Blech criterion (jL_{crit}) from one segment to a multi-segment tree. They showed that the maximum stress difference in an interconnect tree, $\Delta\sigma_{max}$, is given by the path with the greatest sum of segment jL products:

$$\Delta\sigma_{max} = \frac{\rho e Z^*}{\Omega}(jL)_{eff} \tag{2.1}$$

where

$$(jL)_{\text{eff}} = \max_{\substack{\text{all junction} \\ \text{pairs i,j}}} \sum_{k} j_k L_k \tag{2.2}$$

The effective jL product (jL_{eff}) is then calculated and compared to the jL_{crit}. Using their method the failure due to the void saturation can be checked by comparing jL_{eff} to jL_{sat}. In this method, $\Delta\sigma_{\max}$ is assumed to be equal to $2\sigma_{\text{crit}}$ where σ_{crit} is the critical tensile stress for a void to nucleate. This assumption can be valid for symmetric structures. However, in multi-branch nets with arbitrary topology, jL_{eff} may reach $\Delta\sigma_{\max}$ but void nucleation may not occur because the stress at the cathode may be less than σ_{crit}. Such situations occur for critical compressive stress for low-k dielectric breakage or extrusion. Although this model is very powerful, it does not capture the effect of segments adjacent to the path with the highest sum of the jL products, yet not belonging to it. In other words, while the max jL product remains the same, the entire stress distribution might be affected by the segments not on the path with the maximum sum of the jL products. For instance, consider two nets shown in Fig. 2.1; the only difference between these nets is the connectivity at node b_1 (or $b_1{}'$). In Fig 2.1 net *I* has a branch a_1a_2 which is connected to the net on the same layer. On the other hand, net *II* has an alternative configuration in which the segment $a_1{}'a_2{}'$ is connected through a via below at $b_1{}'$. Based on the method developed in [36] and continued in [37], both configurations, have the same $jL_{\text{eff}} = \frac{29}{4}jL$ (the path with greatest summation of jL is marked by the broken line arrow). This is, both structures should experience the same EM conditions. But the stress distributions on net *I* and net *II* are different. In other words, even though $(jL)_{\text{eff}}$ are the same in these structures, due to the other segments configuration (i.e. a_1a_2 in net *I* and $a_1{}'a_2{}'$ in net *II*), the overall stress distribution is different.

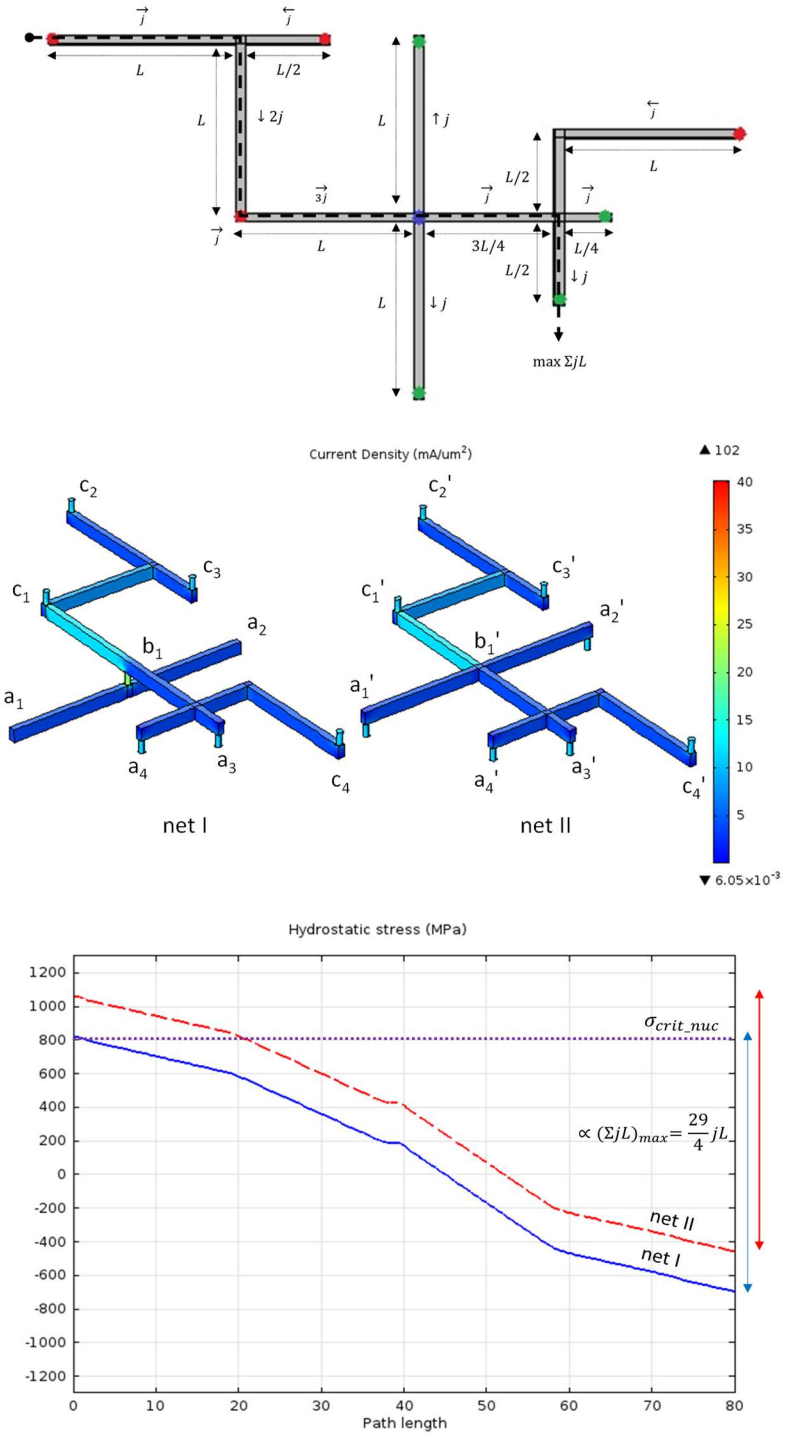


Figure 2.1: A multi-segment net. $jL_{\text{eff}} = \max\Sigma jL$ is the same when segment $a_1{}'a_2{}'$ is connected to $b_1{}'$ as a side branch directly in the same layer or when a_1a_2 is connected through a via to the lower layer. Red and green dots indicate a via above and via below, respectively. Hydrostatic stress along the broken line near the interface is shown at the bottom (in all figures arrows show electron flow $j = 10$ mA/um^2).

Fig. 2.1 shows the hydrostatic stress along the broken line (i.e. the path with greatest ΣjL). In this particular example, analyzing stresses in different nodes and juxtaposing them with the corresponding nodes in the other structure demonstrates this disparity. The number of atoms accumulated in the anodes a_3 and a_4 of net *I* is greater than in the anodes a_3' and $a_4'$of net *II*, since the only places for accumulation of atoms migrating from the cathode ends are a_3 and a_4 . On the other hand, in net *II*, atoms can be accumulated in a_1',a_2', a_3' and a_4' . Therefore, the compressive stresses in nodes a_3 and a_4 are less than those of node a_3' and a_4' . Similarly, node b_1 is experiencing a large atom flux divergence since the segment b_1c_1 supplies more atoms than what is taken by segments b_1a_3 and b_1a_4. However, in net *II*, b_1' is experiencing less atomic flux divergence since $b_1'a_1'$ and $b_1'a_2'$ also contribute in atom accumulation (i.e. atom suction). This disparity in stress is caused by the fact that the via located in b_1 in net *I* only supplies electrons but no atoms. Yet, node b_1' is supplied with atoms by the wire segments $b_1'a_1'$ and $b_1'a_2'$. Likewise, cathode c_2' of net *II* experiences less back stress (since atoms can distribute among more branches) and therefore supplies more atoms (i.e. more atoms are depleted) compared to cathode c_2 in net *I*. Thus, the tensile stress in cathode c_2 is less than that of cathode c_2'. These differences may result in different failure mechanisms. One structure may even be immortal and the other one may be mortal.

Another effort to model immortality in complex interconnect is presented in [38]. The authors propose a method to calculate effective current density based on atomic flux divergence at each via node. This method states that the effective atomic flux can be expressed as $j_{\text{eff}} = (F_L F_W F_B)j$ where F_L, F_W and F_B model the non-electrical effects such as length, width and wire segment interaction on the atomic flux of a lead. Then, effective current density divergence at each node is calculated by $j_{\text{eff.div}} = \Sigma j_{\text{eff}}$. The limitation of this model is that it

only explains the effect of the immediately adjacent segments and does not include the effect of other segments in the net, passive extensions, or their material properties.

We believe that the method presented in this work has broader and more accurate applications. It not only includes the non-electrical and interaction effects of adjacent segments but also explains the non-electrical effects of all connected segments as well as the effects of passive wire extensions.

2.3. New Models

2.3.1. Immortality

In the previous Section, using complex structures (Fig 2.1), we have shown that the sole usage of jL_{eff} does not capture the effect of connected segments. In this Section, we present a model that together with (2.1) can capture the effect of all connected segments. This model offers a systematic way of determining the actual $(jL)_{eff}$ and the actual stress distribution based on the atom conservation principle:

$$\iiint_{net} c\, dV = N_0 \tag{2.3}$$

where c is the concentration of atoms along the net and N_0 is the total number of atoms. The total number of atoms must be equal in the initial state and in the steady state. In other words, the number of atoms accumulated and depleted in different segments of the net is zero:

$$\iiint_{net} \Delta c\, dV = 0 \tag{2.4}$$

From Blech's equation (2.1), it can be seen that the maximum stress difference ($\Delta\sigma$) is proportional to jL. A first order approximation of σ depends linearly on the concentration of atomic lattice sites C by:

$$c = c_0 \exp\left(-\frac{\sigma}{B}\right) \approx c_0\left(1 - \frac{\sigma}{B}\right) \tag{2.5}$$

where c_0 is the initial concentration, B is the effective bulk modulus. At the steady state Δc is equal to $c_0 \frac{\sigma}{B}$. Thus, the total number of added/removed atoms in a segment (or branch):

$$\int_{\text{segment}} \Delta c dV = \int_{\text{segment}} c_0 \frac{\sigma}{B} dV = \left(c_0 \frac{\sigma_{anode}}{B} - c_0 \frac{Z^* e\rho}{2B\Omega} jL\right) V \tag{2.6}$$

Thus,

$$\int_{segment} \Delta c dV = \left(c_0 \frac{\sigma_{anode}}{B} - c_0 \frac{\Delta\sigma}{2B}\right) V = \frac{\sigma_{anode} + \sigma_{cathode}}{2B} V. \tag{2.7}$$

Therefore, the original integral of atom concentration change is written as follows:

$$\int_{net} \Delta c \, dV = \sum_{net} \int_{segment} \Delta c \, dV. \tag{2.8}$$

Thus,

$$\sum_{segments\ k} \frac{\sigma_{k-anode} + \sigma_{k-cathode}}{2B_k} V_k = 0 \tag{2.9}$$

where V_k is the volume of segment-k [39].

If the cross-sectional area of the net is assumed to be constant everywhere as well as the effective bulk modulus, the model can be compacted to:

$$\sum_{\text{segment } k} (\sigma_{a_k} + \sigma_{c_k})\, L_k = 0 \tag{2.10}$$

where σ_{a_k}, σ_{c_k} and L_k are the hydrostatic stress in anode and cathode ends and the length of segment-k, respectively.

The presented model, indeed, consists of equation (2.10) together with Blech's original equation (2.1) and the maximum summation of the jL products (2.2). This model holds true for any multi-segment complex structure.

As an example, the stress distribution is calculated for the nets shown in Fig 2.2. It is assumed that the cross sectional area of the net is constant everywhere as well as is the effective bulk modulus.

For net *I*:

$$\sigma_b - \sigma_a = -\frac{Z^* \mathrm{e} \rho}{\Omega} jL \tag{2.11}$$

$$\sigma_c - \sigma_b = -\frac{Z^* \mathrm{e} \rho}{\Omega} 2jL \tag{2.12}$$

and using (2,9):

$$\frac{\sigma_b + \sigma_a}{2B_{ab}} V_{ab} + \frac{\sigma_c + \sigma_b}{2B_{bc}} V_{bc} = 0 \tag{2.13}$$

$$\frac{\sigma_b + \sigma_a}{2B_{ab}} A_{ab} L_{ab} + \frac{\sigma_c + \sigma_b}{2B_{bc}} A_{bc} L_{bc} = 0 \tag{2.14}$$

therefore,

$$\sigma_a = \frac{5Z^* \mathrm{e} \rho}{4\Omega} jL, \sigma_b = \frac{Z^* \mathrm{e} \rho}{4\Omega} jL, \sigma_c = -\frac{7Z^* \mathrm{e} \rho}{4\Omega} jL. \tag{2.15}$$

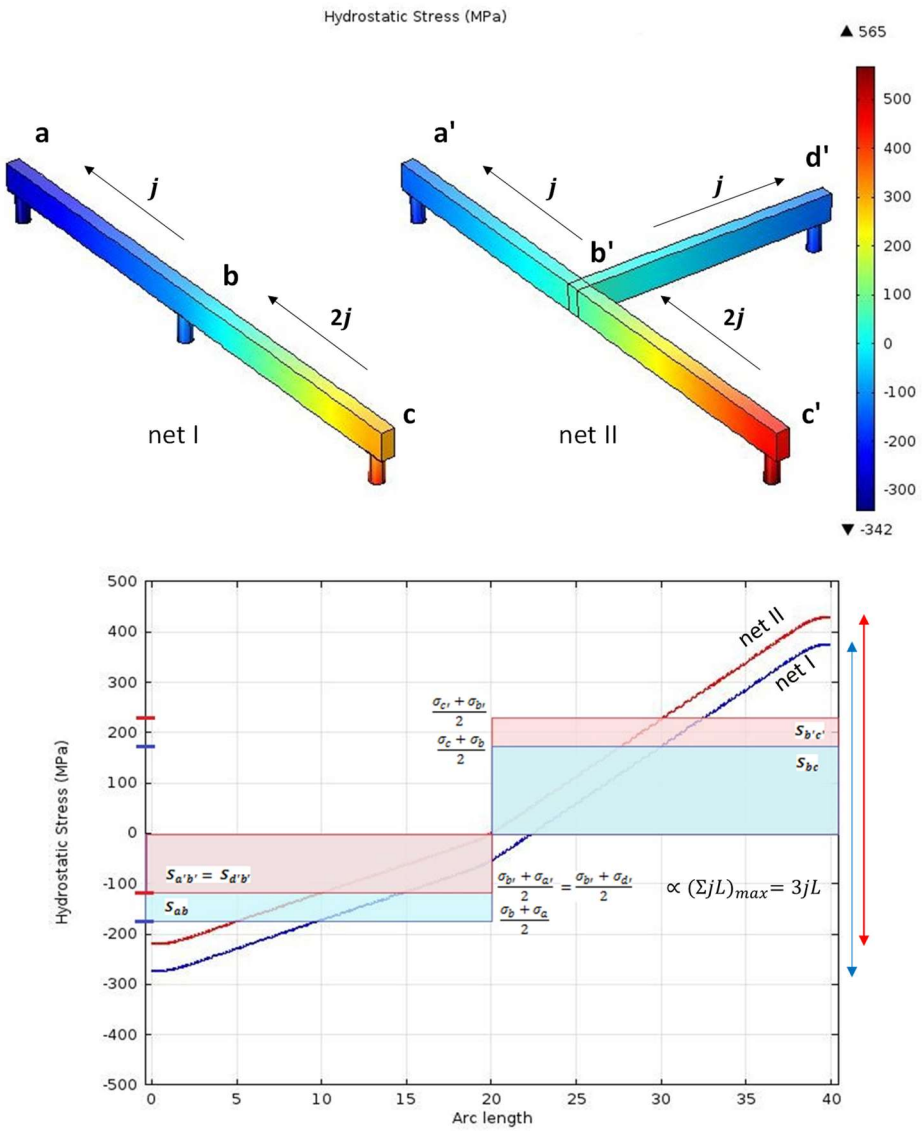


Figure 2.2: Graphical proof of atoms conservation based the hydrostatic distribution (j= $\mathbf{10mA/um^2}$).

Similarly for net *II*,

$$\sigma_{b\prime} - \sigma_{a\prime} = -\frac{Z^* e\rho}{\Omega} jL \tag{2.16}$$

$$\sigma_{c\prime} - \sigma_{b\prime} = -\frac{Z^* e\rho}{\Omega} 2jL \tag{2.17}$$

$$\sigma_{c\prime} - \sigma_{b\prime} = -\frac{Z^* e\rho}{\Omega} 2jL \tag{2.18}$$

and

$$\frac{\sigma_{b\prime}+\sigma_{a\prime}}{2B_{a\prime b\prime}}V_{a\prime b\prime}+=\frac{\sigma_{b\prime}+\sigma_{d\prime}}{2B_{d\prime b\prime}}V_{d\prime b\prime}+\frac{\sigma_{c\prime}+\sigma_{b\prime}}{2B_{b\prime c\prime}}V_{b\prime c\prime}=0 \tag{2.19}$$

accordingly,

$$\frac{\sigma_{b\prime}+\sigma_{a\prime}}{2B_{a\prime b\prime}}A_{a\prime b\prime}L_{a\prime b\prime}+\frac{\sigma_{b\prime}+\sigma_{d\prime}}{2B_{d\prime b\prime}}A_{d\prime b\prime}L_{d\prime b\prime}+\frac{\sigma_{c\prime}+\sigma_{b\prime}}{2B_{b\prime c\prime}}A_{b\prime c\prime}L_{b\prime c\prime}=0 \tag{2.20}$$

therefore,

$$\sigma_{a\prime}=\frac{Z^{*}\mathrm{e}\rho}{\Omega}jL,\sigma_{d\prime}=\frac{Z^{*}\mathrm{e}\rho}{\Omega}jL,\sigma_{b\prime}=0,\sigma_{c\prime}=-\frac{2Z^{*}\mathrm{e}\rho}{\Omega}jL. \tag{2.21}$$

Fig 2.2 illustrates these computations, where $\frac{\sigma_b+\sigma_a}{2}L_{ab}$ and $\frac{\sigma_c+\sigma_b}{2}L_{bc}$ are the marked areas of rectangles S_{ab} and S_{bc}. Based on the atomic conservation, the absolute values of these areas must be equal. On the other hand, for net *II*, $\frac{\sigma_{b\prime}+\sigma_{a\prime}}{2}L_{a\prime b\prime}$ and $\frac{\sigma_{b\prime}+\sigma_{d\prime}}{2}L_{d\prime b\prime}$ represent the areas of rectangles $S_{a\prime b\prime}$ and $S_{d\prime b\prime}$ which correspond to the segments $a'b'$ and $d'b'$ respectively.

According to the atomic conservation, the summation of these areas must be equal to the area of $S_{b\prime c\prime}$ which is calculated as $\frac{\sigma_{c\prime}+\sigma_{b\prime}}{2}L_{b\prime c\prime}$. Comparing hydrostatic stress of corresponding nodes in net *I* and *II* shows that having segment $d'b'$ affects the stress distribution by $-\frac{Z^{*}\mathrm{e}\rho}{4\Omega}jL$ tensile stress. Note that, node b is experiencing an atom flux divergence since the segment bc supplies more atoms than what is taken by segment ba. This atomic flux divergence results in stress. However, in net *II*, $b'$is not experiencing atomic flux divergence since $b'a'$ and $b'd'$ together take same amount of atoms depleted from segment $c'b'$. Therefore, b' experiences zero stress.

This model provides an accurate systematic way to find EM prone sections of any multi-segment interconnect structure by calculating the stress distribution over the entire net using (2.10) together with Blech's equation (2.1) and the max summation of the jL products (2.2).

2.3.2. Length Effect – Active Element

In addition to current density, the stress growth in an interconnect depends not only on its geometry but also on the geometry of other segments of the same net. The effect of geometry, including length, width and thickness are all captured by (2.2) and (2.10).

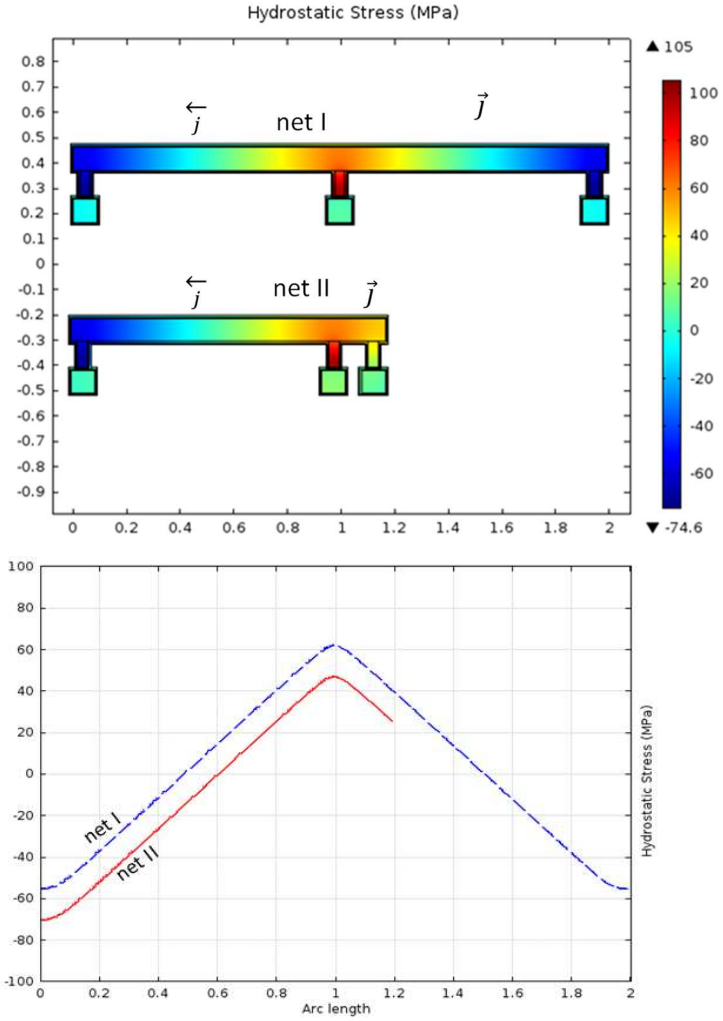


Figure 2.3: Current and stress distribution in two back-to-back connected segments with different lengths. The graph shows the effect of length on immortality (j= $\boldsymbol{10mA/um^2}$).

Fig. 2.3 shows the effect of length of adjacent segments. In both nets, all segments carry the same current density *J*, flowing into the middle via. This can also be explained by the back stress built up in a shorter segment. In net *II*, the shorter segment sucks fewer atoms from the middle via compared to symmetric situation in net *I*. Such effects have been explained in [38] based on atomic divergence. However, we show that the model consisting of jL_{eff} and (2.10) is also able to explain the effect of geometry with no new conventions and holds for segment interactions as those discussed in [38]. The effect of width and thickness are also captured similarly using the proposed compact model [39].

2.3.3. Length Effect – Passive Elements

The effects of passive elements (i.e. metal extensions with zero current) such as those added at cathode (reservoir), or anode (sink), or dummy vias have been investigated in many works [40]. However, a compact model suitable for CAD tools that can explain and model the underlying physics has not been proposed.

Our method not only explains the active segments but also offers a general model for reservoir and sink extension. Fig. 2.4 shows interconnect of a length L. This segment is connected to a reservoir of lengths L_r and sink of length L_s. Solving equations (2.9) and (2.10) for the net shown in Fig. 2.4 is as follows:

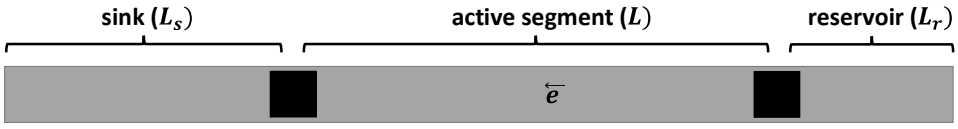


Figure 2.4: An arbitrary active segment, attached to two inactive segments (sink and reservoir with the length of $\boldsymbol{L_s}$ and $\boldsymbol{L_r}$, respectively).

$$\sigma_c - \sigma_a = -\frac{Z^* \mathrm{e}\rho}{\Omega} jL \tag{2.22}$$

$$\sigma_r - \sigma_c = -\frac{Z^* \mathrm{e}\rho}{\Omega} 0L \rightarrow \sigma_r = \sigma_c \tag{2.23}$$

$$\sigma_a - \sigma_s = -\frac{Z^* \mathrm{e}\rho}{\Omega} 0L \rightarrow \sigma_s = \sigma_a \tag{2.24}$$

$$\frac{\sigma_r + \sigma_c}{2B_{rc}} V_{sc} + \frac{\sigma_c + \sigma_a}{2B_{ca}} V_{ca} + \frac{\sigma_a + \sigma s_r}{2B_{as}} V_{as} = 0 \tag{2.25}$$

We assume that the cross sectional area of the net is constant everywhere as well as is the effective bulk modulus. Thus, the stresses at the cathode and anode ends of the active segment in presence of the extensions are:

$$\sigma_a = \frac{L + 2L_r}{2(\mathrm{L_s} + \mathrm{L} + \mathrm{L_r})} jL \tag{2.26}$$

$$\sigma_c = -\frac{L + 2L_s}{2(\mathrm{L_s} + \mathrm{L} + \mathrm{L_r})} jL \tag{2.27}$$

Therefore, the critical current density for interconnect void nucleation in a wire connected to a passive reservoir and a sink is:

$$j_{\mathrm{extension-critical}} = \frac{\mathrm{L_s} + \mathrm{L} + \mathrm{L_r}}{L + 2L_s} j_{critical} \tag{2.28}$$

The critical current density for extrusion can be similarly obtained.

Fig. 2.5 shows the effect of extension on the active segment. Reservoirs in general improve EM performance as they provide extra atoms to the cathode and decrease the tensile stress. On the other hand, sinks in general degrade EM performance by reducing the back stress built up at anode. The simulation results explain experimental results reported in [41].

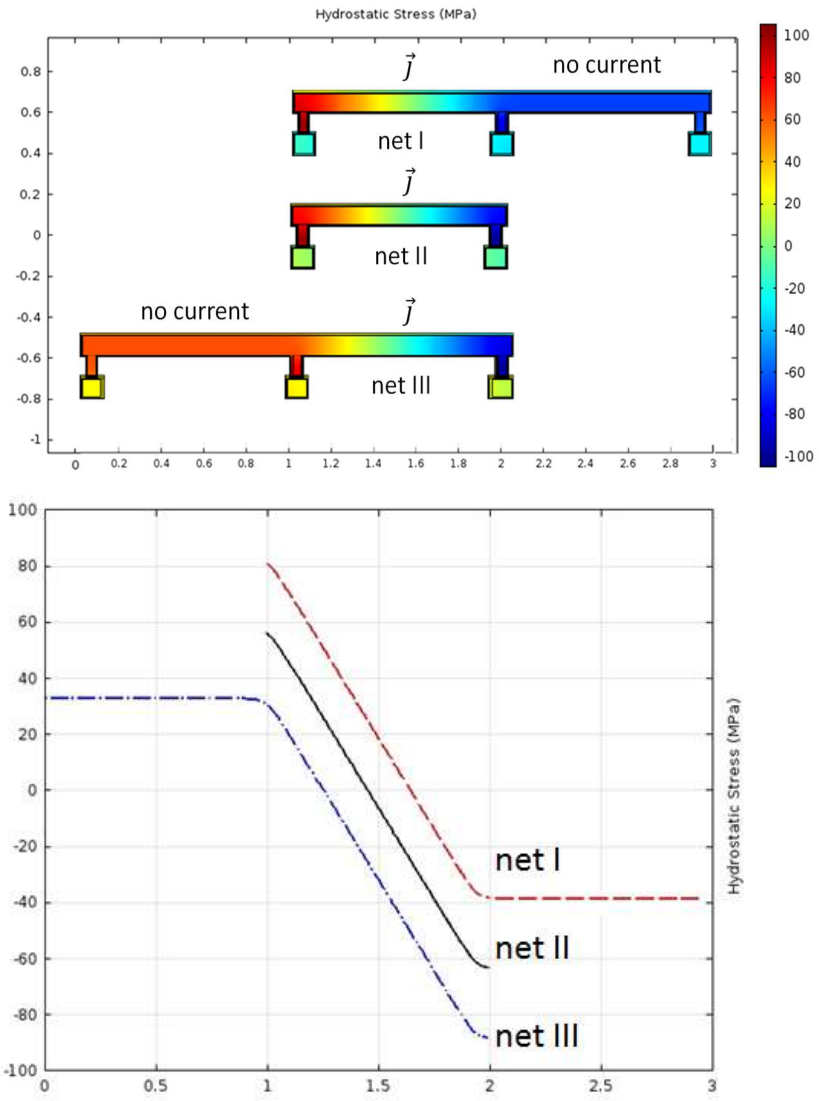


Figure 2.5: Current and stress distribution in two back-to-back connected segments with no electric current. The graph shows the effect of passive segments (j= $\mathbf{10}\boldsymbol{mA/um^2}$).

2.4. Conclusion

Electromigration has been studied extensively for simple interconnect segments with blocking boundary conditions at both ends. Stress evolution, void nucleation and failure conditions are well established for such structures. The compact model for simple structures is known as *Blech length* model or *Blech effect*. In [20], the steady state solution for vacancy/atom

continuity equation was studied by Blech. The result is a compact EM validation criterion which determines the critical product of current density and wire length (jL) for void nucleation [20]. However, these studies were performed for simple via-to-via interconnects and could not be used for multi-segment structures. While extending Blech criterion to complex structures was studied in some papers [36, 38], they have limitation in terms of either capturing all effects or in accuracy. The model proposed in this Chapter computes the stress distribution and captures the electrical and non-electrical effects of all segments connected in a net. The presented compact model can be easily used in CAD tools to replace inaccurate EM failure prediction. This model is also capable of capturing the effect of passive extensions. Application of this model offers design guidance. This model is justified by finite element implementation of vacancy continuity equation and matched with similar experimental results.

Chapter 3

Models Considering Thermal Effects

In this Chapter, we investigate the effect of electrically induced thermal effects on interconnect reliability and aging. We provide an overview of the material transport underlying physics and study all aging processes including electromigration, stress-migration, and thermomigration. We discuss the impact of technology scaling on electro-thermo-mechanical reliability with an emphasis on Joule heating. We propose new models for uniform and non-uniform temperature evolution and its steady state distribution in interconnects. We demonstrate that neglecting thermal effects in modern technologies may lead to incorrect conclusions about interconnect mortality. We introduce new models for reliability assessment capturing thermal, electrical and mechanical requirements simultaneously leading to criteria for accurate temperature-aware mortality assessment of interconnects. The proposed models are employed in many experiments to demonstrate how various temperature profiles affect voiding and hillock formation. These models are verified by comparing the results against finite element experiments. We also provide a detailed explanation of aging in advanced-technology-manufactured local and global wires.

3.1. Introduction

Device reliability is often nonnegotiable, and is crucial for sensitive applications such as medical, autonomous vehicles, and space craft. Interconnect aging and failures induced by mass transfer has become a key reliability issue due to the scaling of interconnects in modern ICs.

In accurate interconnect reliability and lifetime assessment models, all thermal, electrical, and mechanical aspects of mass transfer need to be simultaneously taken into account. Electric field applied to a wire causes gradual movement of ions due to momentum transfer between conducting electrons and diffusing metal atoms. This phenomenon is called electromigration (EM). EM has been linked to mechanical effects via hydrostatic stress buildup by Blech [25, 20]. Thermal aspects of mass transport induced aging, due to complexity, have not been fully coupled with electro-mechanical models. It has been experimentally observed that aging and failure of interconnects in VLSI chips are temperature-dependent [42, 12, 43, 44] but the existing reliability models do not capture thermal effects correctly. Common approach is to add a non-varying temperature rise ΔT due to Joule heating obtained from thermal analysis to models used for EM analysis without considering the true mutual relationships of thermal and electro-mechanical effects [45, 5]. This simplistic treatment ignores thermal gradient and thermal migration issues leading to incorrect reliability assessment and catastrophic failures. This is particularly worrying in stressed scenarios such as scaled interconnect in 3D IC devices.

Temperature has three main effects on mass transfer induced aging: (1) during the annealing process, residual stress builds up due to differences in thermal expansion coefficients of materials adjacent to the interconnect line [5, 28, 46]; (2) electromigration is enhanced at

high temperatures due to faster atomic diffusion [42, 12, 43, 44, 10]; (3) heat transfer creates temperature gradients which themselves cause atomic motion from hot to cool places due to thermomigration (TM) [12, 13, 14, 15].

The first problem (initial built-in stress) occurs prior to device use. Residual stress may cause atomic motion before EM and TM during circuit operation. Initial stress is generated during the system cooling process from the stress free annealing temperature T_{anneal} down to the use temperature T. This problem is relatively straight forward and has been investigated by many researchers [47]. A primary source of this thermally induced residual stress, σ_T, is the difference in the coefficients of thermal expansion of the metal, α_m, and confinement α_c, modeled by $\sigma_T = K(\alpha_m - \alpha_c)(T_{anneal} - T)$ where K is the modulus of elasticity. The atomic motion due to stress gradients is called stress-migration (SM) [5, 28].

The second problem (thermally enhanced EM) is significant since atomic diffusion is very sensitive to temperature. Temperature-varying diffusion lifetime analysis is required for including the thermal effects in defect nucleation or growth [48].

The third problem (thermomigration) relates heat flow to atomic flow. Temperature gradients created by Joule heating cause atoms to move from hot to cool places. Complete description of mass flow requires considering Joule heating, electromigration, and stress migration, together [49].

This Chapter investigates thermomigration under steady state conditions to obtain temperature-dependent mortality criteria. The main contributions are: Section 2: (a) reviews existing methodologies combining thermal effects and electro-mechanical effects, (b) reviews Blech's model and shows the inaccuracy of simplistic methods. Section 3: (a) briefly revisits

material transport underlying physics, (b) presents new models for reliability assessment including thermal effects and (c) introduces new criteria capturing both thermal requirements and EM. Section 4: (a) discusses the effect of technology scaling on electro-thermo-mechanical reliability including thermal effects and (b) provides a detailed explanation of aging processes in local and global wires manufactured in advanced technologies. Section 5: (a) presents experimental results for various benchmarks to validate the proposed models, (b) presents a discussion how various temperature profiles affect voiding and hillock formation. Chapter 8 provides a detailed derivation of the new models for temperature evolution and its non-uniform distributions.

To our best knowledge, these are the first compact models to analyze the aging of interconnects including EM, SM and TM effects. The new models explain several experimental observations (e.g. unexpected mortality or immortality) that were inexplicable before.

3.2. Existing Methodologies and Models

3.2.1. Existing Methodologies

It is a common practice that a uniform temperature rise ΔT due to Joule heating obtained from thermal analysis is simply added to temperature T in expressions used for EM analysis (e.g. Blech based model) without considering the true mutual correlation of thermal and electro-mechanical effects [44, 45, 50]. Undesired chip behaviors as well as time-consuming and non-converging reliability assessments are the common expensive outcomes of such models. It is not surprising that chip designers often overcompensate the inaccuracy of the models embedded in the tools by overdesigning the interconnects or employing overly

tightened rules. This is an undesirable and expensive approach in terms of time and cost [51, 52].

An advanced model such as [53] considers time-varying temperature, however, temperature is assumed to be uniform across the entire long line. The relationship between the temperature profile (Joule heating) formation and current density (EM) is not addressed. To model the underlying physics of thermal effect correctly, temperature effect caused by Joule heating should be modeled through thermomigration. The authors in [54] present a hierarchical wire mortality conditions related to lifetime. However, the model does not take temperature gradients and thermomigration into account and complex numerical procedures are required in this method. Also, the effect of temperature on diffusion coefficient is often ignored or treated simplistically in many existing models [55]. Other filtering approaches exist for multi-segment interconnects in nominal temperature [56, 31]. These recent approaches in their core employ the model presented in [29] describing hydrostatic stress evolution which does not consider TM.

In current physical design practices and verification methodologies, lifetime checks, and thermal analysis are commonly done in different signoff steps without considering their true correlation. It is a common practice that critical current density and wire length are often determined by temperature-agnostic EM models and then combined with temperature rise threshold. However, they should be coupled and modeled jointly. Electromigration changes the resistivity and causes Joule heating. Joule heating, on the other hand, affects electromigration due to diffusivity (temperature rise or ΔT) and atoms motion due to thermomigration (temperature gradients or ∇T).

Due to temperature agnostic electromigration models, two hazardous situations may occur: (1) in some cases, the models may wrongly scrutinize reliability in unfailing parts and consequently impose unnecessary design tightening; (2) in some other cases, the models may underestimate serious reliability problems causing unpredicted behaviors or catastrophic failures to occur. The existing models for mass transfer induced reliability evaluation are usually pessimistic in case of interconnect voiding and optimistic when extrusion occurs.

3.2.2. Existing Models

Blech's model is devised for metallic wire aging induced by application of electric field and its relationship with mechanical stress. In this model, thermal aspects of aging are not considered. As a result, this model is not sufficient for a comprehensive reliability evaluation. To account for thermal effects, it is often employed with extra design rules enforced by thermal load (e.g. a threshold for ΔT) due to Joule heating [44].

Fig. 3.1 demonstrates that excluding thermal effects from material migration induced aging results in ever-increasing inaccuracy in reliability evaluations. Thermal effects caused by Joule heating influence stress evolution in advanced technologies more severely than before. Depending on the temperature distribution caused by ohmic heating, the final stress profile predicted by Blech-based models may have non-negligible errors. In the experiment shown in Fig. 3.1, global wires are layer 8 (M8) metal wires in 45nm and 10nm Intel's technology interconnect stacks, with lengths of 192um and 48um, respectively. Local wires are layer 2 (M2) metal wires in 45nm and 10nm Intel's interconnect stacks, with lengths of 44um and 15um, respectively. Even though by technology scaling jL product increases, in this experiment, jL is conservatively kept constant for the wires in both technologies.

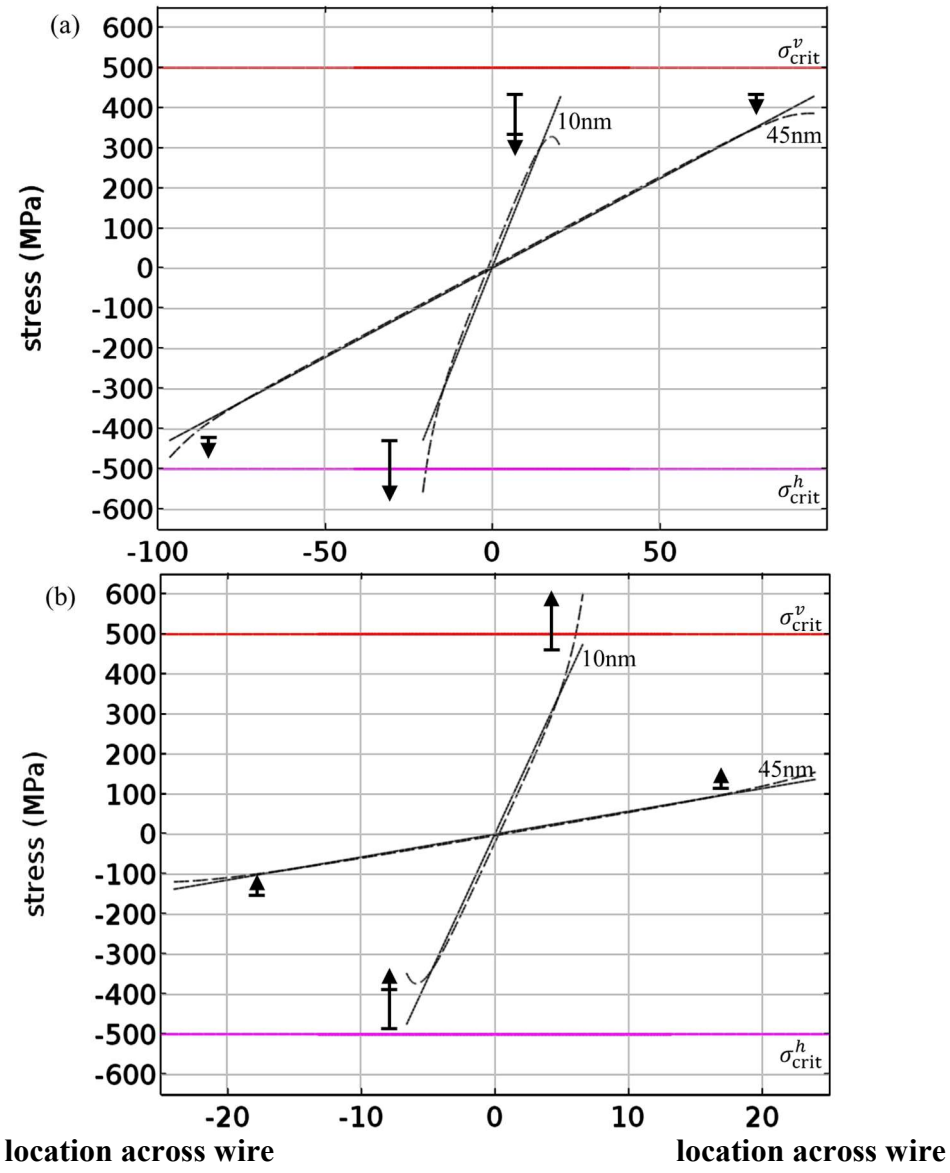


Figure 3.1: Impact of thermal effects on stress formation through technology scaling. The stress profile in (a) a global and (b) a local interconnect without (solid line) and with (dashed line) thermal effects.

The wires are typical end-to-end straight wires extracted from technology-scaled interconnect stacks from IBM benchmark [57]. The wires are constructed with geometrical and material properties for copper, liners, cap and dielectric by Intel [58, 59].

The global wire in 10nm technology experiences higher temperature rise and greater temperature gradients due to technology enforced requirements such as denser design, higher current density, lower dielectric constant and thermal conductivity. Blech's model indicates that the wire will not suffer from voiding or extrusion. As it can be seen in Fig. 3.1 (a), Blech's model predicts higher tensile stress (pessimistic) and lower compressive stress (wrong/optimistic) in the wires under a typical ∩ shape temperature distribution caused by Joule heating. This ever-increasing effect is more severe in advanced technologies. In Fig. 3.1 (a), thermal effect causes the anode to experience greater compressive stress that cannot be detected by the existing models. The finite element method (FEM) experiments reveal that Blech's model does not assess correctly the overall reliability of global interconnects under thermal loads.

More interestingly, local wires are typically considered to be safe using Blech short length effect. However, for advanced technologies, they not only suffer from similar problems as global wires (e.g. higher current density and lower thermal conductivity), but technology scaling additionally depresses the electrical and thermal conductivity of copper wires with dimensions finer than copper mean free path. The higher electrical resistivity and lower thermal conductivity accompanied by higher current density greatly affect stress evolution. In Fig. 3.1 (b), local wires are both under the same condition (e.g. ambient temperature) with a typical ∪ shape temperature profiles. Tensile stress in the cathode of the wire in 10nm technology exceeds the critical stress for voiding and therefore a dangerous voiding is missed by simply Blech model-based filtering.

The test conditions (e.g. current density and temperature distribution) in our experiments are relatively conservative, whereas the wire can easily experience more acute temperature

loads and gradients due to microstructure nature of metal [60, 61]. Nevertheless, our experiments indicate that not including thermal effect properly and simultaneously with electromigration may be the culprit for many unexpected behaviors and device failures [42, 43, 44, 62]. The technology-dependent data in our experiments setup are extracted from [58, 63].

The gap between the stress profiles when Joule heating is included and not included is much greater in more advanced technologies [64].

3.3. New Models for Reliability Assessment with Thermal Effects

In Blech's model only the effects of electromigration and stress migration are taken into account. The model is derived from the conditions on dynamic equilibrium between atomic flux due to EM and the flux due to SM (i.e. $J_{\mathrm{EM}} + J_{\mathrm{SM}} = 0$). However, this model has two shortcomings: (1) It does not allow us to distinguish between the relative contribution to $\Delta\sigma$ of the anode and cathode regions (i.e. (1.19)). (2) Thermal effects are not captured (i.e. TM is not considered).

The first shortcoming is resolved in [39] where a model for determining the individual stress values at anode and cathode rather than the stress difference is proposed. The second shortcoming is addressed in [65] and resolved in this work with a focus on various thermal profiles in local and global interconnects.

3.3.1. Modeling $\Delta\sigma$

In contrast to other models such as Blech's model, we consider the mutual interactions between electrical, thermal and mechanical aspects of interconnects aging. Steady state of a system under material migration is achieved when all atomic fluxes cancel each other out (i.e. $J_{\mathrm{EM}} + J_{\mathrm{SM}} + J_{\mathrm{TM}} = 0$). Considering fluxes in (2.6) - (2.11), in one dimensional model, yields:

$$\frac{\partial \sigma}{\partial x} = \frac{eZ}{\Omega} j\rho + \frac{Q}{\Omega T}\frac{\partial T}{\partial x} \tag{3.1}$$

This is similar to Eq. (3.1) with thermal effects. Solving this ordinary differential equation by integration, yields a useful and accurate model for stress distribution as follows:

$$\sigma(x) = \frac{eZ\rho}{\Omega} jx + \frac{Q}{\Omega}\ln T(x) + \text{constant} \tag{3.2}$$

where *constant* can be readily obtained by boundary conditions. Hence, the difference between the stripe ends can be expressed through:

$$\Delta\sigma = \frac{eZ\rho}{\Omega} jL + \frac{Q}{\Omega}\Delta \ln T \tag{3.3}$$

One may argue that temperature is usually distributed symmetrically (i.e. ∩ shape) along the wire due to vias [66] (i.e. the ends carry the same temperature as underlying metal layer), therefore $\Delta \ln T$ on the right side of (3.3) may be small causing the last term to vanish. While the assumption that both wire ends carry the same temperature can be easily violated in dense 3D integrated circuits, ignoring temperature rise *even with the same temperature at cathode and anode* will miss some significant information. In other words, even though having the same temperature at both ends results in the same $\Delta\sigma$ as when temperature is not considered, the stress profile in the steady state as well as time to failure are very different. In all experiments conducted in Fig 3.1 (a) and (b), the strip ends carry the same temperature.

However, the stress profile is distinctly different for the case where TM is included versus the case it is not included. In the next Section, we will show that the main effect of temperature is on the absolute value of stress at each point including anode and cathode, rather than their difference.

3.3.2. Modeling σ

Blech's condition, (1.19) distinguish between the relative contribution to $\Delta\sigma$ of the anode and cathode regions. In other words, it does not provide values for stress in anode, σ_{a}, or cathode, σ_{c}. In [39], we proposed a formula (based on atom conservation) that offers an extra relationship between σ_{a} and σ_{c}. Such extra relationship between the stress at the wire ends is as follows:

$$\sigma_c + \sigma_a = 0 \tag{3.4}$$

(3.4) accompanied with Blech's condition, (1.19), provides the explicit values for the stress at wire end points:

$$\sigma_C = -\sigma_a = \frac{eZ\rho}{2\Omega} jL \tag{3.5}$$

We can have a similar expression when thermal effect is included. To achieve this, we need to know temperature distribution and Joule heating across the interconnect. Due to lack of a suitable model for interconnects with different initial and boundary conditions, we propose a new model that determines temperature distribution in interconnects due to Joule heating and heat convection. Derivation details of the model are discussed in Chapter 8. According to the model, for a wire of length L $(-L/2 < x < L/2)$ under stationary condition and initial conditions of $T(-L/2) = T_{-}$ and $T(+L/2) = T_{+}$, temperature distribution can be expressed as follows:

$$T(x) = T_0 + T_m\left[1 - \frac{\cosh\left(\frac{x}{\Gamma}\right)}{\cosh\left(\frac{L}{2\Gamma}\right)}\right] + T_n\left[\frac{\sinh\left(\frac{x}{\Gamma}\right)}{\sinh\left(\frac{L}{2\Gamma}\right)}\right] \tag{3.6}$$

where $T_0 = (T_- + T_+)/2$, $T_n = (T_- - T_+)/2$ and $T_m = j^2\Gamma^2\rho/k_{cu}$ is the maximum temperature rise. Γ represents the heat convection or transfer in a wire w.r.t. its adjacent elements. It is determined by the geometry and topology of surrounding interconnects and can be modeled differently depending on wire relative geometrical position. The proposed model is valid regardless of Γ derivation. For the simple case where the anode and cathode have the same temperature (T_0), (3.6) matches the solutions in [66, 67].

The stress model in (3.1) and the temperature model in (3.6), accompanied by the condition that the number of atoms is a conserved quantity [39] (i.e. the change in atom concentration within an encapsulated metallic body is 0 or $\int_{-L/2}^{+L/2} \Delta C dV = -\frac{C_0 HW}{B}\int_{-L/2}^{+L/2} \sigma dx = 0$), yields:

$$\sigma_c + \sigma_a = -\frac{eZ\rho}{\Omega} j^2 \mathcal{L}^2 \tag{3.7}$$

where $\mathcal{L}^2 \approx 2QT_0\Gamma^2/eZkT_aT_c$. The derivation of (3.7) is presented in Chapter 8. (3.3) and (3.7) provide explicit stress values at end points as follows:

$$\sigma_c = +\frac{eZ\rho}{2\Omega}(jL - j^2\mathcal{L}^2) \tag{3.8}$$

$$\sigma_a = -\frac{eZ\rho}{2\Omega}(jL + j^2\mathcal{L}^2) \tag{3.9}$$

This is similar to the model in [39], however, the temperature effect is now included.

3.3.3. Immortality Criteria

Having the critical stresses for voiding and hillock formation, σ^{v}_{crit} and σ^{h}_{crit}, respectively, Blech conditions for immortality of interconnects can be expressed as:

$$jL < \frac{2\Omega}{eZ\rho}\sigma^{v}_{\text{crit}} \tag{3.10}$$

$$-jL > \frac{2\Omega}{eZ\rho}\sigma^{h}_{\text{crit}} \tag{3.11}$$

Similar immortality conditions yet including thermal effects, can be obtained using Eq. (3.8) and (3.9) as follows:

$$jL - j^2\mathcal{L}^2 < \frac{2\Omega}{eZ\rho}\sigma^{v}_{\text{crit}} \tag{3.12}$$

$$-jL - j^2\mathcal{L}^2 > \frac{2\Omega}{eZ\rho}\sigma^{h}_{\text{crit}} \tag{3.13}$$

3.3.4. Guidelines for physical design: maximum *J* and *L*

Various sub-models and criteria can be derived from the model in (3.8) and (3.9). The maximum current density that a length *L* wire can withstand is:

$$j^{v}_{\text{max}} = \frac{-L + \sqrt{L^2 - 4\mathcal{L}^2\tau^{v}_{\text{crit}}}}{2\mathcal{L}^2} \tag{3.14}$$

$$j^{h}_{\text{max}} = \frac{+L - \sqrt{L^2 + 4\mathcal{L}^2\tau^{n}_{\text{crit}}}}{2\mathcal{L}^2} \tag{3.15}$$

where, for the sake of presentation, $\tau^{v}_{\text{crit}} = 2\Omega\sigma^{v}_{\text{crit}}/eZ\rho$ and $\tau^{h}_{\text{crit}} = 2\Omega\sigma^{h}_{\text{crit}}/eZ\rho$.

The model can be integrated into various physical verification methodologies. For instance, when a critical temperature rise is a key thermal criterion, an alternative form of (3.8) – (3.9) can be written as follows:

$$\sigma_c = +\frac{eZ\rho}{2\Omega} jL - \frac{Q}{\Omega}\frac{T_m}{T_0} \tag{3.16}$$

$$\sigma_a = -\frac{eZ\rho}{2\Omega} jL - \frac{Q}{\Omega}\frac{T_m}{T_0} \tag{3.17}$$

where $\theta_{\text{crit}} = T_m/T_0$ is a critical value for temperature rise. (3.16) and (3.17) yield immortality conditions under non-uniform temperature due to Joule heating:

$$jL < +\frac{2\Omega}{eZ\rho}\sigma^{v}_{\text{crit}} + \frac{2Q}{eZ\rho}\theta_{\text{crit}} \tag{3.18}$$

$$jL < -\frac{2\Omega}{eZ\rho}\sigma^{h}_{\text{crit}} - \frac{2Q}{eZ\rho}\theta_{\text{crit}} \tag{3.19}$$

This model implies precise length criteria reflecting the effect of temperature. Hence useful tools for guiding physical design can be obtained in terms of void-immune and extrusion-safe wire lengths as:

$$L^{v}_{\max} = \left(1 + \frac{Q}{\Omega}\frac{\theta_{\text{crit}}}{\sigma^{v}_{\text{crit}}}\right) L \tag{3.20}$$

$$L^{h}_{\max} = \left(1 - \frac{Q}{\Omega}\frac{\theta_{\text{crit}}}{\sigma^{h}_{\text{crit}}}\right) L \tag{3.21}$$

The models presented in (3.20) and (3.21) imply that taking the temperature effect into account for any current density j, the maximum length for void-immune and extrusion-safe can be relaxed or tightened by $Q\theta/\Omega\sigma$, respectively. This means designers can take advantage of a more accurate short length effect and apply greater current densities.

Note that the models presented here assume a common case where the temperature at ends are almost the same (i.e. $\Delta \ln T \approx 0$ or $Q\Delta \ln T\,/\Omega \ll eZ\rho(jL \pm j^2\mathcal{L}^2)/\Omega$). Even though such assumptions were validated in many experiments, exact general forms of (3.10) – (3.21) are presented in Chapter 7.

3.3.5. Extrema

The models presented in (3.7) – (3.21), in their core, check the hydrostatic stress against the critical stress on the end points of a wire where stress have the extreme values (i.e. the max tensile and compressive stresses occur in the cathode and anode, respectively). However, the exact positions of the extrema depend on temperature profile and may no longer happen in the wire ends. The maximum stress can be found by solving the following equation:

$$\frac{\partial \sigma}{\partial x} = \frac{eZ}{\Omega} j\rho + \frac{Q}{\Omega T}\frac{\partial T}{\partial x} = 0 \tag{3.22}$$

Plugging equation (3.1) into (3.22), yields a very accurate approximation for the location of the maximum stress as follows:

$$x_s = \Gamma \cosh^{-1}\left(\frac{eZT_0 k}{Qj\Gamma}\cosh\left(\frac{L}{2\Gamma}\right)\right) \tag{3.23}$$

where t_{Cu} and t_{ILD} are the thickness of the wire and the surrounding dielectric and also k_{cu} and k_{ILD} are thermal conductance of the wire and the dielectric, respectively.

The location for maximum stress under EM, TM and SM can be found based on the geometrical, electrical and thermal characteristics of a wire and dielectric which are readily available. The stress distribution under temperature effect for a complex net is shown in Fig. 3.1 (b). The maximum stress within two end points may not necessarily occur at ends.

3.4. How Significant is the Impact of Temperature on Aging? EM vs SM vs TM

In this Section, we discuss the impact of technology scaling on electro-thermo-mechanical reliability of interconnects with emphasis on the significance of thermal effects. We later provide a detailed explanation of aging processes in advanced local and global interconnects.

3.4.1. Impact of Technology

It is widely observed and reported in numerous experiments that thermal effects are no longer negligible [42, 12, 62, 68] and including them conventionally as side additive rules may result in false assessments. In fact, due to technology scaling, Joule heating which happens concurrently with EM and SM has a significant influence on overall aging and failure more than ever before.

Technology scaling exacerbates the effect of temperature on interconnect aging not only through miniaturization but also through many other thermal related factors. (1) Current density: current density increases in modern technologies due to reduced geometries and performance requirements. (2) Thermal conductivity: technology scaling demands lower dielectric constant (e.g. materials with ever-decreasing low-k for noise prevention). Decreasing dielectric constant negatively affects interconnect reliability. It causes lower thermal conductivity and thus heat trapping within interconnect stack resulting in temperature rise [44, 69, 70].

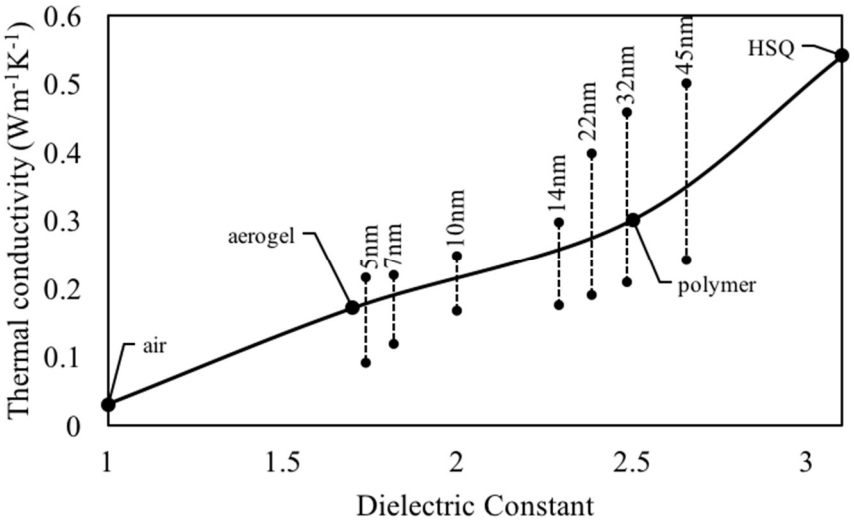


Figure 3.2: Technology scaling enforces lower dielectric constant and lower dielectric thermal conductivity.

Fig. 3.2 demonstrates the impact of technology scaling on permittivity and thermal conductivity of a dielectric. The graph is produced based on data reported by several foundries [42, 68, 71, 72, 73, 74, 75]. In addition to the conductivity of dielectric, the interconnect effective thermal conductivity is also affected as feature sizes scale, especially the layer thickness. Higher temperature results in increased thermomigration. (3) Electrical resistivity of interconnect lines: dimension shrinking increases resistivity of wires. Barriers are hardly scaled and have much higher resistivity compared to copper. Consequently, due to decreasing aspect ratio of metal to liner, the effective resistivity is ever-increasing. A smaller surface area ratio of the conductor to the area of liners increases the effective resistivity. As the surface area to volume ratio of the metallization increases, the electron surface scattering effects become a significant contributor to resistivity [76, 77]. Also, line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness all adversely affect electron scattering in copper lines and increase resistivity [78, 79, 80]. The rise in resistivity is faster for copper compared to that of aluminum. This directly results in aggravated Joule heating [52, 68, 69, 70, 81] (see the model in (3.6)).

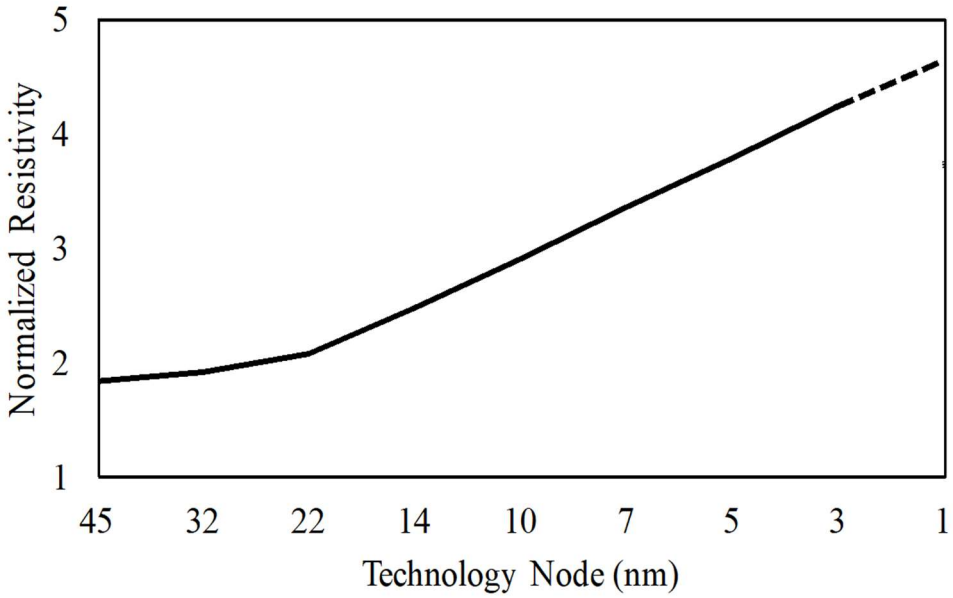


Figure 3.3: Effective resistivity of copper for various metal layers normalized to the bulk resistivity of copper at 100C (2.204 [uΩ-cm]).

Fig. 3.3 shows the impact of technology scaling on electrical resistivity of local wires. The graph is obtained with data reported in a vast spectrum of references taking into account various parameters such as interface and barrier quality and thickness, and wire aspect ratios. It is worth mentioning that, interconnects easily experience greater non-uniform temperature fluctuations during operation which additionally increases the resistivity [68, 82, 83, 84, 85].

3.4.2. EM vs SM vs TM

In this Section, we compare the significance of EM, TM and SM in terms of driving force triggers, fluxes and flux divergences. For a conservative case when the temperature difference between anode and cathode is small the flux due to TM compared to that of EM via (1.6), (1.9) and (3.6) can approximately be obtained as follows:

$$\left|\frac{J_{TM}}{J_{EM}}\right| = \frac{Q/\mathrm{T}}{eZ\rho}\left|\frac{\nabla T}{j}\right| \approx \frac{Q}{eZT_0k_{Cu}}\left(j\Gamma\frac{\sinh\left(\frac{x}{\Gamma}\right)}{\cosh\left(\frac{L}{2\Gamma}\right)}\right) \tag{3.33}$$

Taking the average and maximum temperature gradients across entire wire length yields the following ratios:

$$\text{avg}\left|\frac{J_{TM}}{J_{EM}}\right| = \frac{2Q}{eZT_0}\left(-\frac{j\Gamma^2}{k_{Cu}L}\right) \tag{3.34}$$

$$\max\left|\frac{J_{TM}}{J_{EM}}\right| = \frac{2Q}{eZT_0}\left(-\frac{j\Gamma}{k_{Cu}}\right) \tag{3.35}$$

It can be seen in (3.34) and (3.35) that both technology (e.g. electrical and thermal conductivities) and design (e.g. j and L) affect these ratios as well as the maximum temperature rise (i.e. $j^2\Gamma^2\rho/k_{cu}$).

Fig. 3.4 shows the significance of temperature on various interconnect technologies. In Fig. 3.4 (a), the temperature rises in intermediate interconnects for various technologies and design parameters (such as current and width) vary. The values for all technologically enforced parameters such as thickness, aspect ratios, minimum pitch, thermal and electrical properties are obtained from recent experimental reports on modern manufacturing processes of major foundries [42, 44, 86, 68, 69, 75, 81, 87, 88, 89].

Fig. 3.4 (b) shows the relative significance of TM flux with respect to the EM flux (3.35). Thermomigration has roughly the same order of magnitude as electromigration and can no longer be ignored for advanced technologies. These effects are shown for intermediate interconnects only; similar computations can be made for other layers with corresponding geometry and properties.

To clarify, the following realistic example shows that none of EM, SM or TM can be ignored.

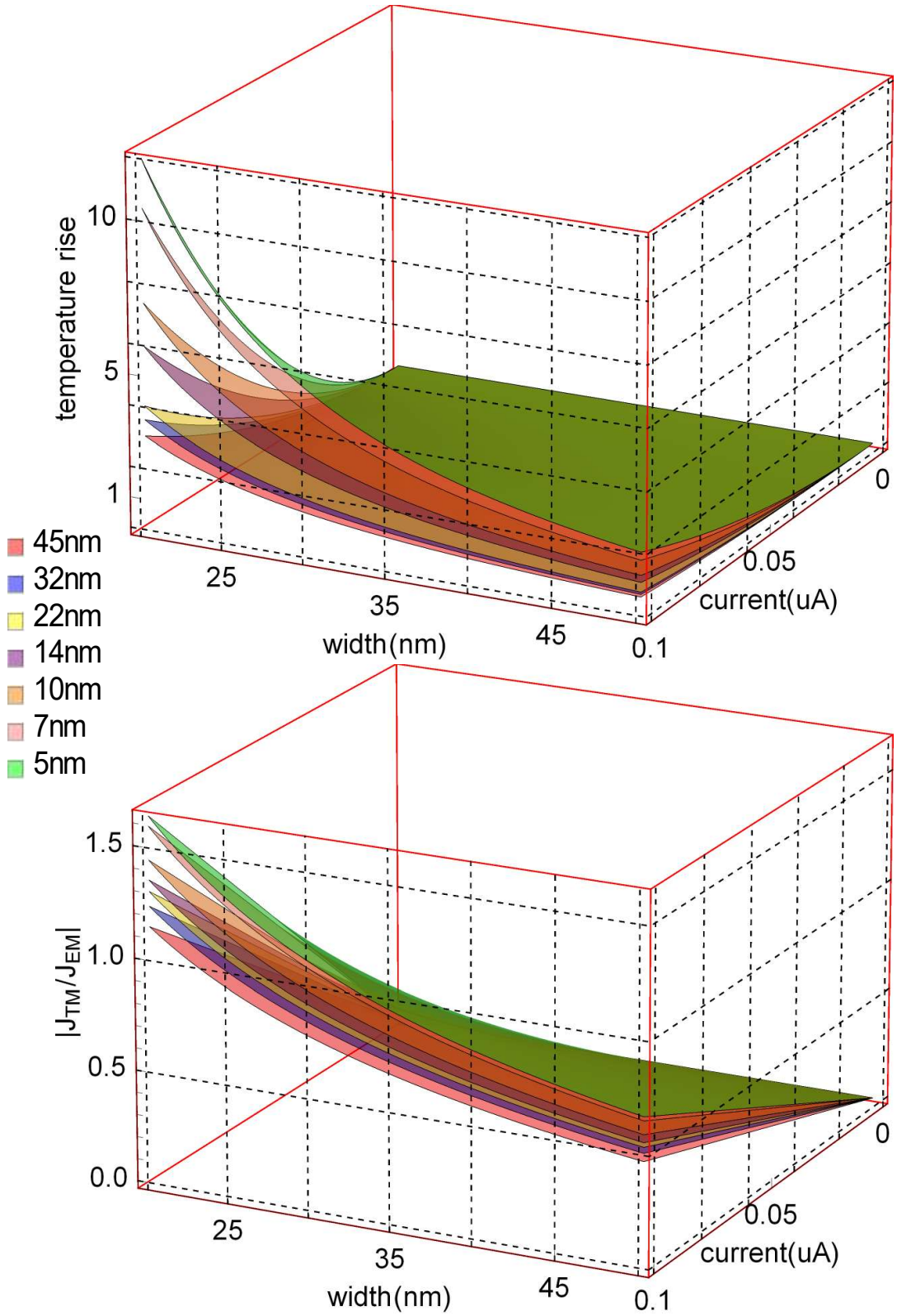


Figure. 3.4: The effect of current, width and technology scaling on (a) temperature rise; (b) the ratio of TM flux to EM flux, for intermediate interconnect via (3.35).

Example 1. We study a dual-damascene copper interconnect stack of a microprocessor chip (MPU) in 10nm technology node with proper passivation. Fig. 3.5 shows a miniature part of this interconnect network. Geometrical, electrical and material properties are realistically adopted from the average values reported by Intel [59] and verified by major semiconductor foundries. Without loss of generality, we discuss the findings for an arbitrary segment (i.e. the middle layer in Fig. 3.5). Wire: L=100um, W=48nm, H=36nm, J=5e10A/m^2, $T_{ambient}$=373K. Low-k dielectric: H=38nm, k=2.1. Barrier (Ta/TaN): H=1nm. Capping (TiN_xO_y): H=5nm. (L=length, W=width, H=thickness).

FEA experiments with fine meshing is used to compute the fluxes caused by EM, TM and SM. Example 1 was run in COMSOL Multiphysics [90] (as a golden model) with realistic thermal setups (e.g. heat generation, transfer and convection), solid mechanic settings (e.g. elasticity and boundary conditions) and electrical conditions (e.g. insulation and conservation). The maximum triggering forces, fluxes and flux divergence ranges due to each process are measured and presented in Table 3.1.

Table 3.1: Atomic fluxes for the interconnect described in Example 1

	Max Trigger [a]	Flux Range [b]	Flux Divergence [c]
EM	∇V=0.83 mV/um	3.80e15 – 5.15e15	-1.87e20 – 1.9e20
TM	∇T=0.61 K/um	8.48e09 – 7.73e15	-9.42e20 – -7.27e17
SM	$\nabla \sigma$=23.96 MPa/um	1.85e12 – 1.16e16	2.09e18 – 1.1e21

Atomic fluxes caused by electromigration, thermomigration and stress migration.
[a] The trigger of the driving forces in EM, TM and SM TM fluxes are the gradients of electric potential, temperature, stress and concentration, respectively.
[b] Fluxes are absolute norm values in $m^{-2}s^{-1}$.
[c] Flux divergence unit is $m^{-3}s^{-1}$.

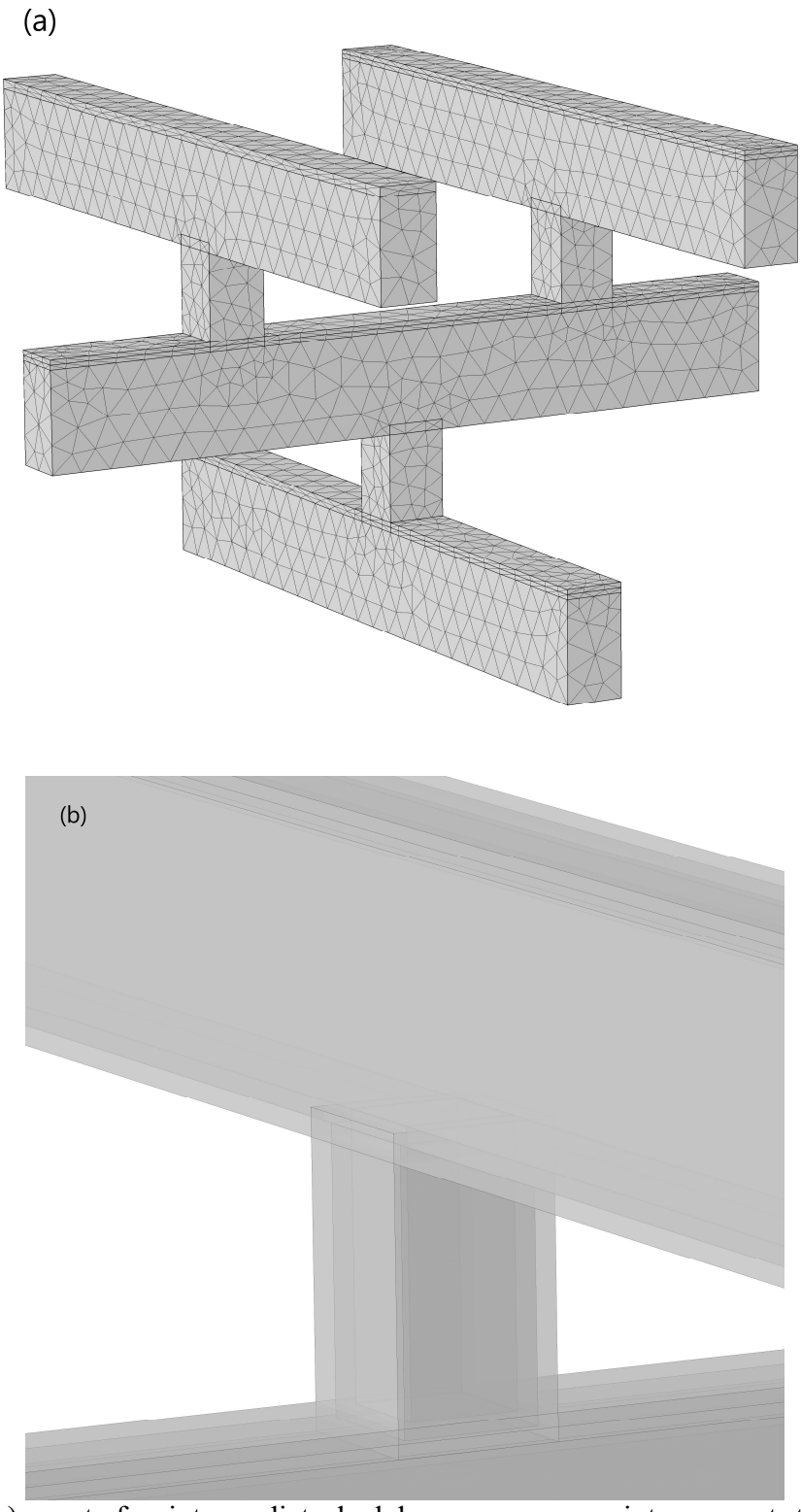


Figure. 3.5: (a) a part of an intermediate dual damascene copper interconnect stack of a MPU in 10nm technology finely meshed for numerical experiments. (b) A transparent zoomed area of interconnect structure, illustrating the via and wire junction with barrier and capping layers confined in a low-k dielectric.

Fluxes: As it can be seen through equations (1.5), (1.7), and (1.9), the gradients of voltage, temperature and stress are the triggers of the driving forces and thus fluxes due to EM, TM, SM and DM, respectively. The application of a current density of 50 mA/um^2 to a wire of 100 um results in a gradient in electric potential of 0.83 mV/um. This gradient creates a max EM flux of 5.15e15 m^{-2} s^{-1}. As a side effect, it causes a non-uniform temperature rise where temperature at the ends is assumed to be fixed. This temperature rise causes gradients with a max of 0.61 K/um occurring close to the ends. This acute gradient forms a great TM flux with a maximum of 7.73e15 m^{-2}s^{-1} which is clearly non-negligible. The TM flux is small only in locations with almost uniform temperature. Yet, this can be easily violated not only near the ends, but also at surfaces and grain boundaries. In addition, the hydrostatic stress force is generated by the gradient of stress with a maximum of 23.96 MPa/um. This gradient creates SM flux of up to 3.73e15 m^{-2} s^{-1}.

These exact findings in Table 3.1 are validated by computing the fluxes quantitatively using equations (1.6), (1.8) and (1.10) in 1D space. The corresponding comparison is as follows:

$$\left|\frac{J_{TM}}{J_{EM}}\right| = \frac{Q/\mathrm{T}}{eZ\rho}\left|\frac{\nabla T}{j}\right| \approx \frac{0.1eV \times (373.15\mathrm{K})^{-1}}{1.6\times10^{-19}\mathrm{C}\times 1\times 1.67\times10^{-8}\Omega\mathrm{m}} \times \frac{0.1\,\mathrm{K/um}}{10\mathrm{mA/\mu m^2}} \approx 1 \qquad (3.36)$$

$$\left|\frac{J_{SM}}{J_{EM}}\right| = \frac{\Omega}{eZ\rho}\left|\frac{\nabla \sigma}{j}\right| = \frac{1.66\times10^{-29}\mathrm{m^3}}{1.6\times10^{-19}\mathrm{C}\times 1\times 1.67\times10^{-8}\Omega\mathrm{m}} \times \frac{10\,\mathrm{MPa/\mu m}}{10\mathrm{mA/\mu m^2}} \approx 1 \qquad (3.37)$$

In above calculations, e and ρ are the fundamental electron charge and copper resistivity. The average operating temperature of chips are typically around 100°C with some fluctuations, we assume T=373.15 K. Z is reported to be in the range of 1 to 10 and mostly assumed to be 1. Q is measured with different techniques and reported in a wide range (0.9-0.09 eV). The widely accepted value of 0.1 eV is used in this thesis [12, 91].

Despite the coefficients, flux triggers highly depend on experiments. However, in modern technologies, j in problematic interconnects is often observed to be up to between 1 MA/cm^2 and 10 MA/cm^2 [42, 44, 68, 69, 75, 81]. Although the exact values are measured through our experiments, for quantitative comparison 1 MA/cm^2 is used. $\nabla\sigma$ strongly depends on the location and settings (e.g. bulk, grain boundaries, surface or pre-existing voids and impurities). Whereas the exact values are measured in our example, the gradient of stress is reported to be within 1 to 100 MPa/um [12, 92, 91]. Thus, 10 MPa/um was found to be a good average for everywhere within the segment. Similarly, based on the location, ∇T can be easily up to 1 $\mathrm{K/um}$ (e.g. at interfaces) [12, 91, 93] . For quantitative purposes, we assumed to be on average around 0.1 K/um.

While the values are selected conservatively, Example 1 shows that these gradients can be often much greater. For instance, $\nabla\sigma$ and ∇T were measured to be as high as 23.96 MPa/um and 0.61 K/um, respectively (see Table 3.1). In particular, during reliability testing due to the higher temperature and stress load, these fluxes are even more intense.

It is worth mentioning that while the data presented in Table 3.1 is obtained from Example 1 in a three-dimensional setting with very detailed lithography information, the one-dimensional model is in a strong agreement with the golden detailed FEM experiments where the same segment is simulated properly in COMSOL Multiphysics. It is not surprising, because electrons move in one direction along the wire length (either *x*-direction in wires or *z*-direction in vias) where the electric potential is applied. Also, the strict boundary conditions in 1D (such as zero flux at interfaces and ends) precisely imitate the rigid interfaces in 3D setup. Thus, fluxes in other dimensions are insignificant.

Remark 1. Fluxes created by EM, TM and SM depend on the magnitude of the gradients of voltage, temperature and stress. In a simple homogenous and straight end-to-end line the gradient of voltage tends to be constant, but in complex structures with corners and branches, voltage gradients might vary a lot. The gradients of temperature are small in the neighborhood with uniform temperature distribution (e.g. usually central area of wires). However, this uniformity can be disrupted due to many factors such as heat generation, transfer or convection at the boundaries and abrupt geometrical changes such as ends or grain boundaries. Temperature gradients are usually acute at ends and interfaces which trigger thermomigration. Similarly, for SM, the hydrostatic stress gradients can sharply change when shape of the interconnect alters sharply (e.g. ends or interfaces) or the homogeneity of lattice is disrupted (e.g. grain boundaries). These fluxes are shown to be non-negligible.

Flux Divergence: We discussed the significance of driving force triggers (i.e. gradients of electric potential, temperature, stress and concentrations). We also talked about the importance of fluxes which cause the movement of particles. In this Section, we discuss the flux divergences which is the change in concentration of the total inflow and outflow of particles. We later show how flux divergence is related to the mean time to failure of a metallic interconnect.

Using flux divergences, a comparison similar to that of fluxes can be performed. The expressions are derived in Chapter 4 when a new model for lifetime is proposed so that readers can justify the values in Table 3.1. It was shown that EM, TM and SM are comparatively significant. This necessitates that accurate reliability assessments that require models and methods which are able to take all those factors into account fairly. In the following Section,

we propose a new model for both transient and stationary analysis which is able to include all three major causes for material migration.

3.4.3. Global Interconnects

In this Section, we discuss how global interconnects suffer from mass-transfer induced aging and how this is affected by thermomigration. Global wires suffer from excessive heat generation due to many technological and design reasons mentioned in Section 3.1. Current density is increasing due to performance requirements and results in increased Joule heating. Also, circuits are becoming denser and thermally less conductive. Therefore, heat generated due to Joule heating cannot be transmitted outside and becomes trapped.

In Fig 3.1 (a), solid lines demonstrate the steady state excluding thermal effects. jL product is conservatively assumed to be the same in both old and new technologies, this is in both wires $\Delta\sigma$ is the same (i.e. 860MPa). Joule heating, however, affects the overall aging through thermomigration (dashed lines). It can be seen that this effect is much greater in 10nm technology. It is not only due to technological parameters but more importantly due to higher current density in jL product. Technology scaling enforces larger current density while the length of global wires is not scaling so much. It can be seen in Fig 3.1 (a) that while jL product or $\Delta\sigma$ are the same, Joule heating makes a big change in the ultimate stress profile. Joule heating, in a shorter wire with higher current density in 10nm technology, creates a temperature profile of $\cap$ shape with a maximum temperature rise of only 5.5K. The acute local temperature gradients and high global gradients push atoms from hot places to cool locations so that a large compressive stress is produced. The hydrostatic compressive stress in anode increases by 144MPa which violates the critical stress for extrusion. On the other hand, TM caused by

temperature gradients around the cathode opposes default electromigration direction and pushes back atoms moved from the cathode due to EM. In this particular case, temperature gradients alleviate voiding and aggravate extrusion formation.

In this research, without loss of generality and for the sake of discussion, the absolute values of the corresponding critical stress are assumed to be 500MPa [25, 20, 94] . In this example, the wires just violate the critical threshold.

3.4.4. Local Interconnects

We provide a discussion on how local interconnects are prone to mass-transfer induced aging problem when thermal effects are non-negligible. For local interconnect, while current density has a swelling trend with technology scaling, the length is also shrinking. Since the lengths of local wires are pretty small, jL product usually does not violate the critical value and thus, due to short length effect [25, 20, 94] , they are often assumed to be safe. However, it is widely reported by many manufacturers and researchers that local wires also suffer from aging yet in different ways for advanced technologies such as 10nm [76, 77, 85, 95].

In Fig 3.1 (b), both wires in older and newer technologies have conservatively the same jL product. However, this time, even with excluded TM effect, $\Delta\sigma$ is not the same and proportional to jL product as Blech based method suggests. The reason for counterintuitive incident is hidden in electrical resistivity. In jL product-based analysis the resistivity of material (e.g. copper) is assumed to be constant and independent of its temperature and geometry (e.g. thickness).

In reality, the electrical resistivity of a metal varies with temperature and thickness. The change in resistivity due to temperature rise has been studied and there exist many useful

models such as those in [84]. The resistivity of metals such as copper are independent of wire thickness or width for dimensions above the mean free path length. However, at very small dimensions the resistivity of copper film increases due to electron scattering. Below the mean free path, the copper electrons begin to scatter far more often from the various surfaces and grain boundaries because they are so area-constrained [76, 77, 85, 96]. Copper wires in advanced local interconnect can easily have dimensions smaller than mean free path (40nm). This excess scattering increases the resistivity of copper. Also, copper requires thick high-resistivity barrier layers that do not scale down in thickness and at small dimensions become a significant percentage of the cross-sectional area of the interconnect. In other words, as interconnect continue to shrink, the thickness of the high-resistivity liner/barrier for the copper interconnects stays more or less the same. This is due to the difficulty in liner thinning any further than the few nanometers it already is. This means that as the wires scale, the barrier itself takes up a larger and larger portion of the interconnect cross-sectional area. With the high-resistivity barriers slowly making up a larger portion of interconnect, scattering begins to dominate the resistivity of the wire itself.

Such greater resistivity affects overall aging in two ways: (1) EM: ρ is larger in (3.3) (2) TM: ρ is larger in (3.7). In other words, larger resistivity aggravates both electromigration and thermomigration. (3.7) – (3.21) remain valid for the change in resistivity of advanced local interconnects. Electron scattering not only decreases the electrical conductivity of metal but also its thermal conductivity. Since thermomigration inversely depends on both electrical and thermal conductivities, it is more sensitive to change in resistivity compared to EM.

A more suitable mortality conditions including varying resistivity of advanced local metal films, can be derived from (3.12) and (3.13) and expressed as follows:

$$\rho jL - \rho^2 j^2 \mathcal{L}^2 < \frac{2\Omega}{eZ}\sigma^{v}_{\text{crit}} \tag{3.38}$$

$$-\rho jL - \rho^2 j^2 \mathcal{L}^2 > \frac{2\Omega}{eZ}\sigma^{h}_{\text{crit}} \tag{3.39}$$

where $\mathcal{L}^2 \approx 2Q\Gamma^2/eZL_oT_aT_c$, is modified $\mathcal{L}^2$ where Wiedemann–Franz law is utilized to relate the thermal conductivity to the electrical resistivity (L_o is Lorentz number).

In Fig 3.1 (b), since the wire in 10nm technology has its width less than the mean free path, the resistivity is adjusted accordingly. The resistivity of a wire is modeled based on [82, 83, 96] and verified with experimental measurements [97, 98]. EM partially contributes to excessive stress buildup. With jL product the same and strip ends at the same temperature, $\Delta\sigma$ is not the same in different wires (solid lines). Joule heating also makes another large change in ultimate stress profile. Joule heating, in a shorter wire with higher current density in 10nm technology, makes the temperature profile of ∪ shape with a maximum temperature rise of only 6°C when strip ends are assumed to be connected to underlying hot devices (e.g. 100°C) and carry the same temperature based on via effect [66]. Yet, the acute local gradients and high global gradients of temperature multiplied with large electrical and thermal resistivity form a great TM flux that pushes atoms from hot places to cool locations. According to temperature gradient sign, such motion creates a large tensile stress. The excessive hydrostatic tensile stress due to thermal migration in cathode is increased by 131MPa which violates the critical stress for voiding. On the other hand, TM via the temperature gradients alleviates compression around the anode due to EM. Effects of different temperature profiles and gradients are discussed in the next Section.

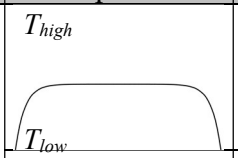
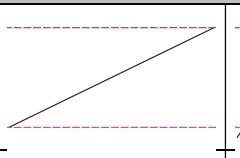
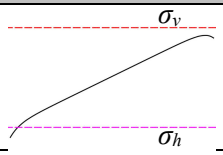
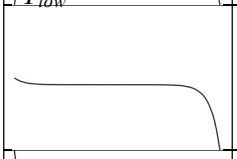
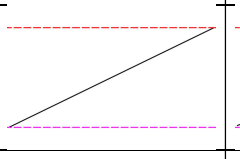
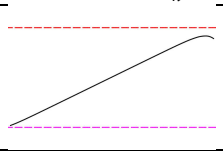
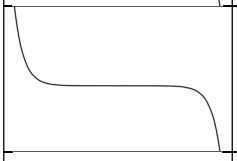
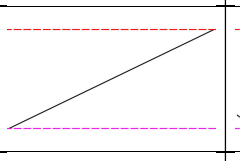
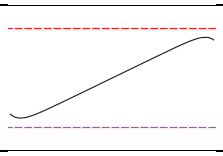
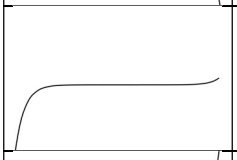
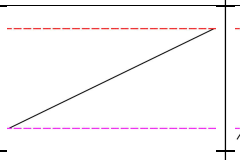
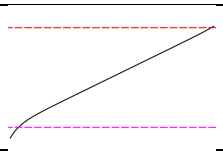
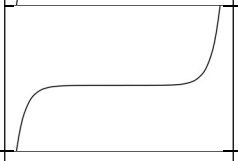
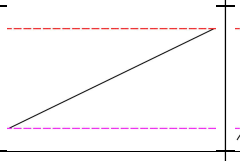
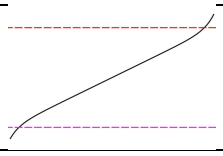
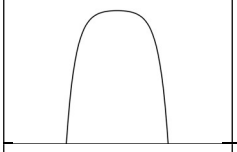
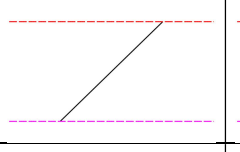
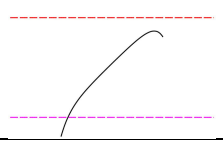
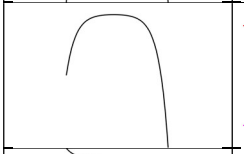
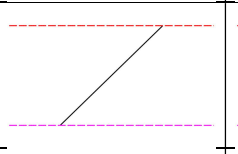
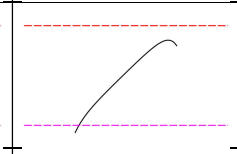
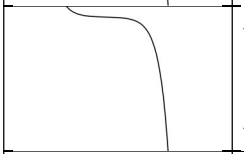
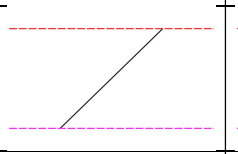
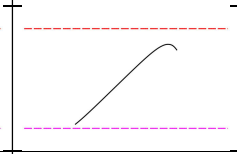
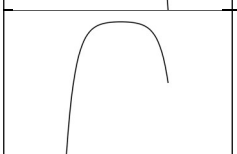
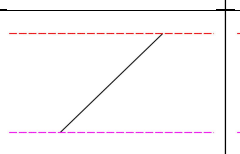
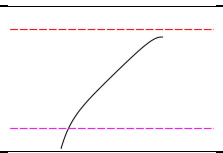
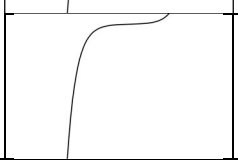
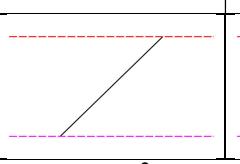
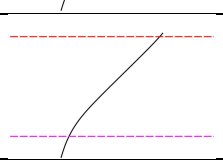
3.5. Experiments and Discussion

3.5.1. Temperature Profile and Failure Mechanism

Extensive experiments are performed to verify the validity of our findings and models. Table 3.2 shows the application of our model to intermediate-length interconnects in 10nm technology under various temperature profiles (due to Joule heating). The values for geometrical, electrical, mechanical and thermal properties of technology are obtained from [42, 66, 67, 68, 69, 81, 87, 88, 86]. Table 3.2 presents experimental results on two similar wires with lengths of 50um and 100um. Current density of $3x10^{10}A/m^2$ and $6x10^{10}A/m^2$ are applied with different boundary conditions to cover several non-uniform solutions of heat equation. The presented model is technology independent and is valid regardless of thermal profile derivation. It can accommodate any wiring configuration and technology through different values for material, electrical and thermal properties of components. As it can be seen in Table 3.1 there are considerable differences in terms of violations predicted by the proposed model and the existing ones. They are caused by not considering TM in the existing models. (In Table 3.1: Units: L: um ($-l \leq L \leq l$), J: MA/cm^2, T: K, Stress: MPa. Temperature and stress ranges: 100C (T_{low}) to 109C (T_{high}) and -800MPa to 800MPa. Critical stresses ($\sigma_v = |\sigma_h|$): 500MPa (dotted lines). Anode:$-l$, Cathode: $+l$. ✓: violated, ×: not violated, $\underline{✓}$: aggravated).

In particular, when the temperature gradients are negative towards the cathode from the anode, such gradients alleviate the tensile and compressive stresses. This can be exploited by designers to have a greater reliability margin in terms of the maximum length or current density as temperature increases the resilience of interconnect. On the other hand, positive temperature gradients towards the cathode from the anode, aggravate the tensile and compressive stresses.

Table 3.2: Stress profile vs various thermal profiles (violation checking).

			Finite Element Methods		Models			
			Blech [3]	New	Extrusion		Voiding	
L	J	Temperature	Stress		Blech	New	Blech	New
100	3				✓	✓	✓	×
					✓	✓	✓	×
					✓	×	✓	×
					✓	✓	✓	✓
					✓	✓	✓	✓
50	6				✓	✓	✓	×
					✓	✓	✓	×
					✓	×	✓	×
					✓	✓	✓	×
					✓	✓	✓	✓

Units: L: um ($-l \leq L \leq l$), J: MA/cm^2, T: K, Stress: MPa. Critical stresses ($\sigma_v = |\sigma_h|$): 500MPa (dotted lines). Anode: $-l$, Cathode: $+l$. ✓: violated, ×: not violated, ✓: aggravated

Table 3.2 demonstrates the impact of different temperature distributions on immortality conditions. The conventional Blech based EM rules may assess the EM violations incorrectly (last columns in Table 3.1). Such effects are more severe for greater current density (compare cases $3x10^{10}A/m^2$ vs $6x10^{10}A/m^2$).

In general, two situations may occur: (1) in some cases, the existing models may wrongly scrutinize reliability in unfailing parts and consequently impose unnecessary design tightening and (2) in some other cases, they may underestimate serious reliability problems causing unpredicted behaviors or catastrophic failures to occur. The existing models for reliability evaluation are usually pessimistic in case of interconnect voiding and optimistic when extrusion occurs.

For a detailed discussion on how temperature evolution and stress evolution are mutually related we consider now case 1 in Table 3.2. The results are presented in Fig 3.5. To have a clearer discussion, the flux values are normalized by their common factor (i.e. BD/kT). Application of electric potential or current density results in EM. As an immediate side effect, temperature rise occurs through Joule heating process. The temperature gradient produces atomic flux and consequently causes TM. While electrical current is applied and temperature raises, stress develops simultaneously. These three fluxes compete against each other and reconcile in the steady state.

Application of electric potential or current density across the segment results in EM. As an immediate side effect of applying electric potential, a temperature rise occurs through Joule heating effect. The temperature gradients, thus, produce atomic flux and consequently TM begins promptly. While electrical current is applied, and temperature is raised, stress will develop simultaneously. These three fluxes (i.e. EM, TM and SM) evolve and, analogically,

compete against each other and reconcile in a steady state. A simple schematic of this kinetics is depicted in Fig. 3.5.

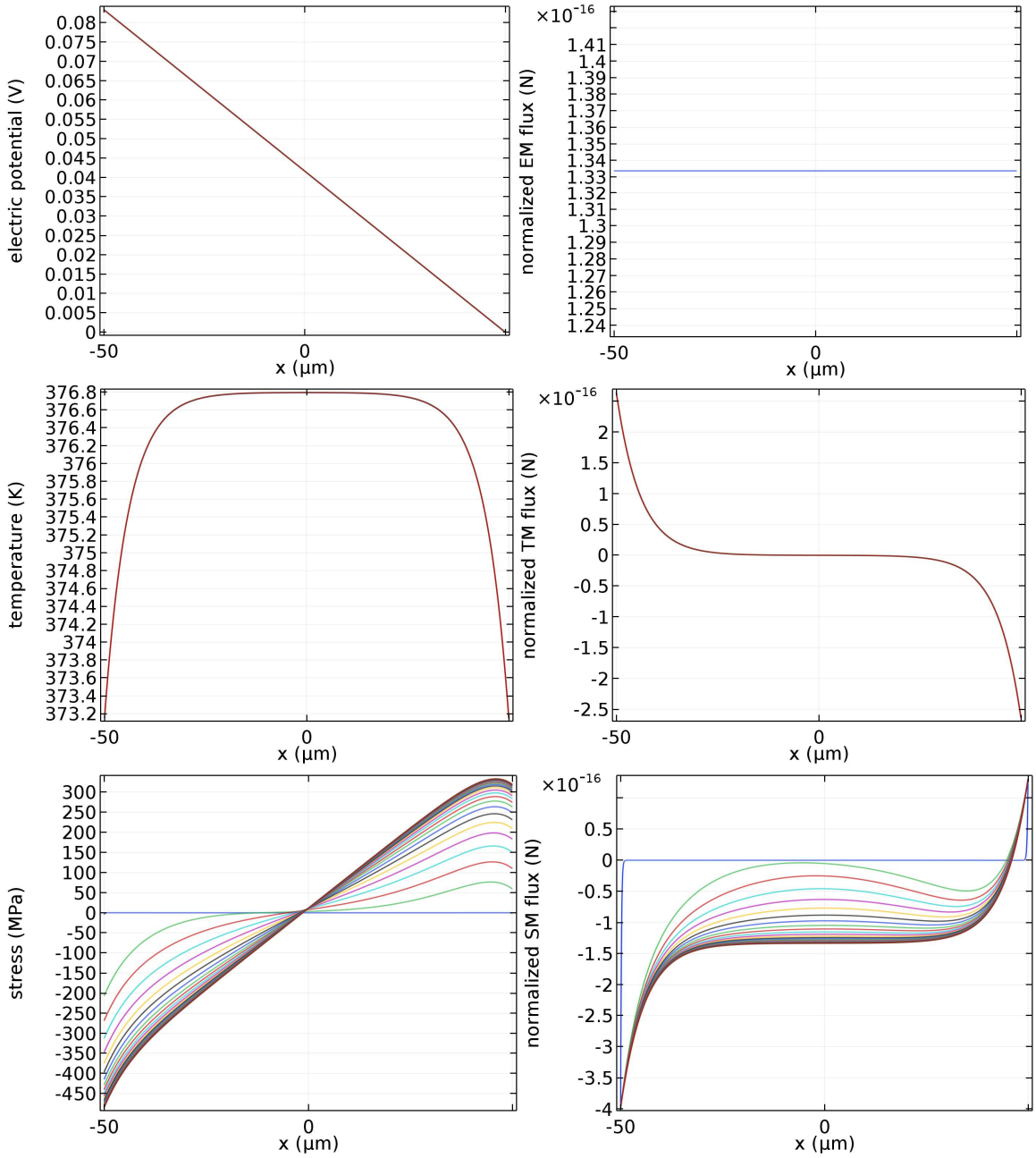


Figure 3.5. Left column: Applied electric potential, temperature rise (due to Joule heating) and evolving stress (top to bottom, respectively). Right column: normalized fluxes due to EM, TM and SM (top to bottom, respectively). The experiment shows stress evolution from a no-stress state ($t = 0$ s) to the steady state ($t = 7e7$ s $= 2.2$ years).

Yet, the evolution of mechanical stress in interconnect lines is more complicated. For mechanical stresses to develop, there must be both a volume expansion/contraction of the line and a mechanical constraint (with respect to the surrounding material). Atoms (exchange place with vacancies and) travel towards the anode (due to EM) and at the same time tend to move from hot places to cool places (due to TM). The final destination has no longer to be the anode necessarily. It indeed depends on temperature as well as electric potential. Thus, atom depletion or accumulation might happen in places different than the wire ends (we call them extrema, see Fig. 3.5 and Fig. 3.6).

Since atoms are conserved (no source or sink), this results in a supersaturation at one extremum and a deficiency at other extremum. Since there is a small relaxation of the lattice (surrounding a vacancy), depletion of atoms would produce volume contraction at one extremum and their accumulation would produce volume expansion at another extremum. However, due to the constraints imposed by the surrounding materials (i.e. capping layer, barrier layer, and passivation in copper dual-damascene), these volumetric changes cannot be accommodated, which results in the development of stress in the line.

At the depletion of atoms extremum tensile stress is produced, while compressive stress develops at the accumulation extremum. As a result, these produced stress gradients act as additional driving forces for material transport. Extrema are the places where the developed stress is minimum or maximum due to high accumulation or reduction of atoms. It can also be interpreted in in terms of fluxes: in extrema stress is very high and atoms are supersaturated, and, for voiding, the local stress gradient is zero (i.e. stress does not change that much), therefore, there is no stress induced driving force and thus no stress migration (i.e. zero SM

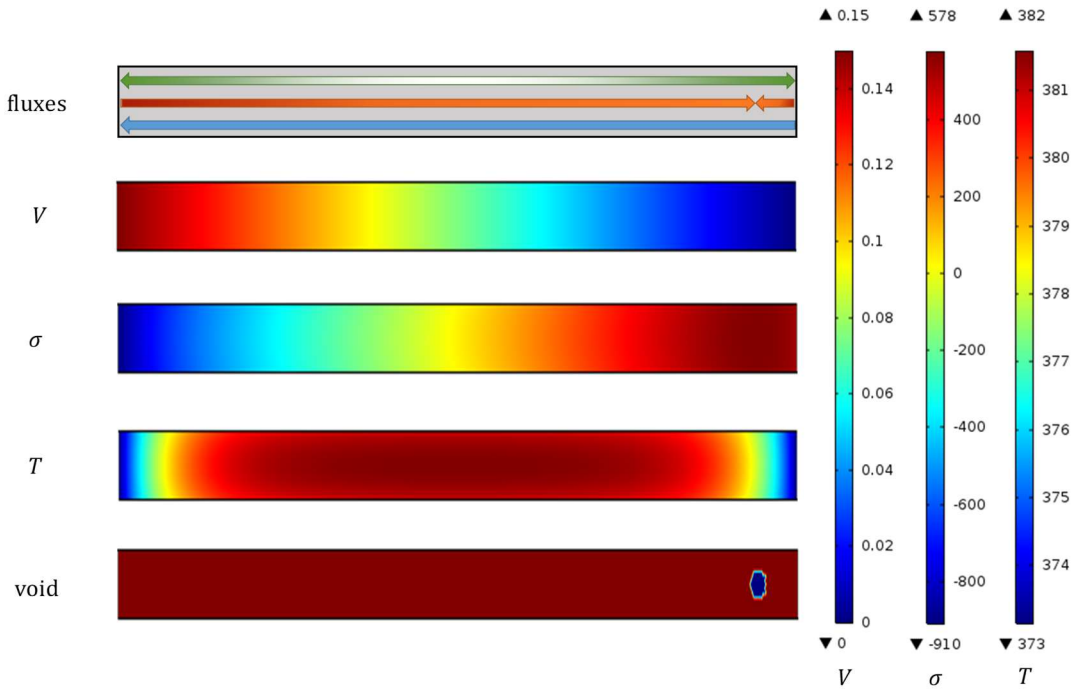


Figure 3.6: Finite element analysis of Example 2. The top-left figure illustrates the fluxes due to EM (blue arrow), SM (red arrow) and TM (green arrow). The figures below display voltage, stress and temperature distribution, respectively from top to bottom. EM (action) pushes atom from places with lower electric potential towards places with higher potential. Rapidly, temperature rises and TM (side effect) causes atoms to travel from hot to cool locations. Stress commences to develop, as a result SM (reaction) competes against atoms movement. Due to the competition between EM, TM and SM, stress evolution dictates a void to nucleate towards the cathode but not exactly at the end of the line. The final destination has no longer to be the anode necessarily.

flux). In contrast, other migration processes (i.e. EM and TM) cancel each other out. This is why mechanical stress is a key metric for the void nucleation condition.

Ignoring TM always results in having the extrema near the ends, however as it was shown it is no longer valid for interconnects under thermal loads. Determining the extrema is discussed in the next section through steady state analysis.

The new model confirms that thermomigration usually (i.e. for the thermal profile of ∩) tends to aggravate compressive stress and potentially exacerbate the risk of extrusion or shorts. On the other hand, thermomigration mitigates tensile stress and possibly alleviates the risk of

voiding or opens. Indeed, atoms tend to migrate from hot to cool areas. Since the hottest location is usually towards the center of the interconnect line, some atoms travel to anode and increase the compression, and some atoms move back to cathode and compensate depletion and consequently reduce the tensile stress. Intuitively, increasing temperature usually mitigates shrinkage and intensifies expansion. This may cause serious effects (i.e. stress aggravation.) Thermomigration interacts with electromigration and stress migration, it may result in (1) asymmetric stress distribution, (2) early hillock formation (shorter lifetime), (3) late voiding (longer lifetime) and (4) non-end failures. The experimental results indicate that due to such effects many expected failures may not occur or some new may occur.

3.5.2. Guidelines for physical design: jL vs $j^2\Gamma^2$

The proposed models offer many useful guidelines to assist physical designers. Table 3.3 shows an application of our model to interconnects with various current density and length. The highlighted rows in Table 3.3 show that Blech based models relying on jL product can wrongly evaluate the health of interconnects. In all cases the product of current density and length are the same and thus they are assessed to have the same reliability and lifetime. However, the proposed model distinguishes these two cases properly. Indeed, immortality of a wire should be evaluated by $\alpha jL \pm \beta j^2\mathcal{L}^2$ (or $\alpha\rho jL \pm \beta\rho^2 j^2\mathcal{L}^2$ for including varying resistivity) rather than jL where α and β are constant and can be readily obtained from (3.17) and (3.18). Also, the contribution of each term (via α and β) can determine the arguable current density exponent in well-known Black's equation for mean time to failure [91] [27]. The results are in a good agreement with detailed FEA experiments.

Table 3.3: Application of the new model on various interconnects (10nm)

		ΔT (K)			Maximum tensile stress Voiding (MPa)			Minimum compressive stress Extrusion (MPa)		
J (MA/cm^2)	L (um)	Blech	New	FEM	Blech	New	FEM	Blech	New	FEM
3	50	-	0.79	0.79	412	391.69	393.7	-412	-432.40	-430.4
3	100	-	0.79	0.79	824.1	803.74	804.8	-824.1	-844.45	-843.4
6	50	-	3.15	3.15	824.1	742.67	751.1	-824.1	-905.52	-897.2
6	100	-	3.15	3.14	1648.2	1566.77	1571.2	-1648.2	-1729.61	-1725.3
9	50	-	7.09	7.09	1236.1	1029.93	1083.8	-1236.1	-1419.34	-1399.9
9	100	-	7.09	7.07	2472.3	2266.08	2310.8	-2472.3	-2655.49	-2645.3

The average disparity between new model and experiments is below 1% while the error in Blech based models is up to 14% and can be worse under various technologies and loads.

The proposed model also explains several experimental observations that may have been inexplicable before. For instance, Fig 3.7 illustrates the admissible values for current density and length of an interconnect under different thermal loads. Thermal load is presented in terms of $\mathcal{L}$ which indicates the heat generation due to Joule heating. The highlighted regions show permissible combinations of jL for a wire to be immortal due to voiding with respect to the thermal load. When $\mathcal{L}$ is zero, i.e. Joule heating is negligible, the space for safe values of j and L can be estimated and verified by Blech's model (i.e. the outer region of 1/xy-like curve). However, for non-negligible Joule heating effect, i.e. $\mathcal{L} \neq 0$ (e.g. cases (b), (c) and (d)), term $j^2\mathcal{L}^2$ in $\alpha jL \pm \beta j^2\mathcal{L}^2$, allows having larger current density without experiencing voiding violations for the same length. Similar analysis can be performed for hillock violations under different distributions. It implies increasing thermal load may potentially loosen design rules in terms of maximum current density and increase design flexibility.

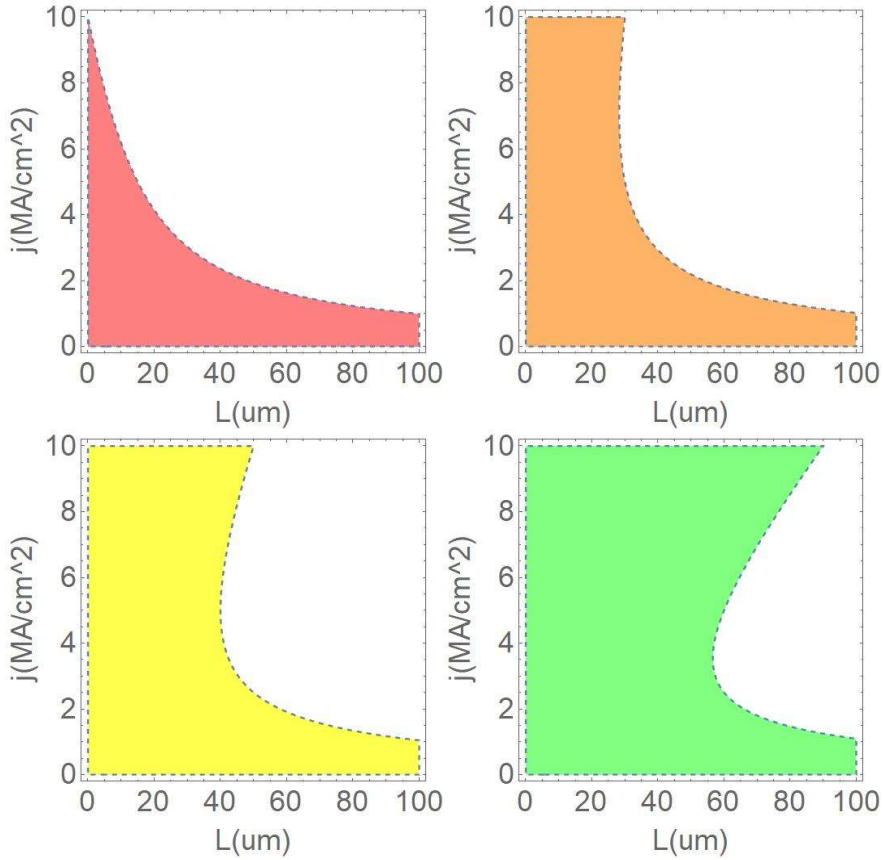


Fig. 3.7 The permissible values for j and L under different thermal loads. Contour lines correspond to different values of normalized thermal effect (due to Joule Heating) (a) $\mathcal{L}$=0, (b) $\mathcal{L}$=2, (c) $\mathcal{L}$=4 and (d) $\mathcal{L}$=8.

3.6. Conclusion

We demonstrate that simplistic combination of thermal models and temperature-agnostic electromigration models without considering their true correlation no longer provide correct reliability assessment for wires manufactured in advanced technologies. We propose a compact aging model that captures the impact of Joule heating on material migration via thermomigration.

Our new model provides a steady state temperature profile under any arbitrary non-uniform conditions and is used to capture thermomigration. We investigate the stress development considering thermomigration, an aging process induced by Joule heating. We show that neglecting thermal effects during reliability assessment may lead to wrong evaluation for wires manufactured in modern technologies. We propose a new criterion for checking immortality of wires under any thermal, electrical and mechanical conditions. We demonstrate that many wires considered mortal based on Blech criterion may never experience aging problems during the product lifetime and many Blech-immortal wires may become damaged and cause catastrophic failures.

We investigate in detail various temperature profiles. We show that depending on the steady state profile of temperature, the voiding and hillock potential appearance will be affected, and therefore agnostic Blech based method may not be trusted. The new model confirms that thermomigration usually (i.e. for the thermal profile of $\cap$) tends to aggravate compressive stress and potentially exacerbate the risk of extrusion or shorts. On the other hand, thermomigration mitigates tensile stress and possibly alleviates the risk of voiding or opens. In general cases, when the temperature gradients are negative towards the cathode, such gradients alleviate the tensile and compressive stresses. On the other hand, positive temperature gradients towards the cathode, aggravate the tensile and compressive stress. Our models are validated by numerous COMSOL-based experiments.

Chapter 4

Models for Complex Multi-Segment Interconnect Structures Considering Thermal Effects

In this Chapter, we study the main interconnect aging processes: electromigration, thermomigration and stress migration in complex multi-segment structures and propose comprehensive yet compact models for transient and steady states based on hydrostatic stress evolution. The model also explains many experimental observations, introduces temperature-dependent Blech's length criterion and a new time-to-failure formula replacing Black's empirical model. Experimental results obtained on IBM benchmarks validate the model [57].

4.1. Introduction

It has been experimentally observed that aging and failure of interconnects in VLSI chips are highly sensitive to temperature [42, 12, 43, 44, 99] but the reliability models do not capture the thermal effects correctly. Temperature, due to Joule heating, affects the aging of

interconnects through a complicated process but in the existing models it is typically considered as a corrective factor to a constant temperature analyses [45]. Recent works study reliability of interconnects in terms of electromigration (EM) and stress migration (SM) but neglect the true physics of temperature effects. [53] presents a model considering time-varying temperature. Yet, temperature rise occurs relatively spontaneously compared to the entire long-term material migration. Therefore, temperature effect caused by Joule heating should be modeled through thermomigration (TM). Such recent approaches in their cores employ the model in [29] describing hydrostatic stress evolution which does not include the effect of temperature through thermomigration. It has been shown that for modern technology due to high Joule heating, thermomigration has large impact on both initiation of failure (e.g. void nucleation) and its growth and therefore ignoring it may result in unexpected behavior [12, 45].

Including TM adds extra complexity to modeling. Most of the advanced works [53], only propose models for specific interconnect structures. They also do not consider TM effect on the failure growth rate as their velocity is based only on EM. The accuracy and efficiency of such methods highly depend on numerical methods (e.g. eigen functions). EM as the sole driving force is a crude assumption since EM-induced side effects such as mechanical back stress flow and Joule heating affect voids motion. In fact, temperature affects the whole process of forming the steady state profile and time to nucleation. It also may accelerate, slow down or stop growths. Due to absence of correct physics-based models, even recent industrial works such as [42, 89], model empirical data using a large-scale statistical analysis method under various temperatures using a corrective constant fixed temperature increase (ΔT) with the average operating temperature or attempt to fit an exponent in Black's MTF equation [27].

In this Chapter, we demonstrate that omitting the effect of temperature in existing models is the culprit of reliability expectation and observed behavior incompatibilities. We study all main aging processes: EM, TM and SM and propose comprehensive yet compact models for realistic interconnect reliability assessment. The models for both transient and steady states are derived based on stress evolution. Also, a new temperature-dependent length criterion is derived which can replace Blech's length criterion widely used in CAD tools [20]. A new CAD tool is developed to assess reliability of large multi-segment interconnect nets.

4.2. New Stress Evolution Based Models

4.2.1. Transient Analysis

The theory of metal plasticity employs an incremental strain definition which was first introduced in [100]. Extending the concept of incremental strain ($\delta\varepsilon$) to 3D space yields:

$$\delta\varepsilon = \frac{\delta V}{V} = \delta\left(\frac{m}{C_a}\right)/\frac{m}{C_a} = -\frac{\delta C_a}{C_a} \tag{4.1}$$

where $V = m/C_a$ is the volume and m is the mass which is constant.

The mean hydrostatic stress ($\sigma = (\sigma_{xx} + \sigma_{yy} + \sigma_{zz})/3$) relates to volumetric strains by:

$$\sigma = \frac{E}{3(1-2v)}\varepsilon = B\varepsilon \tag{4.2}$$

where $B = E/3(1-2v)$ is the bulk modulus, E is the Young's modulus and v is the Poisson's ratio. Therefore, an analytical model based on only voltage, temperature and stress can be obtained as:

$$\frac{\partial\sigma}{\partial t} = B\nabla.\left(-\frac{D}{kT}eZ\rho j + \frac{D}{kT}\frac{Q}{T}\nabla\mathrm{T} - \frac{D}{kT}\Omega\nabla\sigma\right) \tag{4.3}$$

In can be readily seen that the term for concentration is cleverly eliminated. In other word, this expression enables modeling the material migration without dealing with the nontangible atom concertation quantity. As a result, studying concentrations of atoms can be done by analyzing stress. The presented model is similar to the one proposed in [53]. The distinction, however, is that the model in [53] assumes fixed temperature without TM.

Eq. (4.3) for a single wire ($-L/2 < x < L/2$) in 1D can be seen as a diffusion equation with spatially variable source and inhomogeneous boundary conditions (BCs):

$$\sigma_t = j_x = k\sigma_{xx} + ks_x \tag{4.4}$$

$$j(-L/2, t) = j_- \tag{4.5}$$

$$j(+L/2, t) = j_+ \tag{4.6}$$

$$\sigma(x, 0) = \sigma_{\text{res}} \tag{4.7}$$

where σ_{res} is the initial residual stress before device operation, and j, k and s can be readily obtained by comparing (4.3) and (4.4). The subscripts for j indicate evaluation at the corresponding endpoint. Such formulation with non-zero boundary conditions and variable source terms which is not solved in [53] allows us to extend the model to arbitrary multi-segment network where fluxes at intermediate nodes are non-zero [101].

Theorem 4.1: Defining α_n as $\frac{(2n+1)\pi}{L}$, the solution for (4.4) is as follows:

$$\sigma(x, t) = u(x) + \sum_{n\in\mathbb{Z}} v_n(t)\cos(\alpha_n x) \tag{4.8}$$

$$u(x) = ax^2 + bx \tag{4.9}$$

$$v_n(t) = \frac{1}{L}\int_{-L/2}^{L/2}\left(\frac{p(x)}{e^{k\alpha_n^2 t}} + \frac{q(x)}{k\alpha_n^2}\right)\cos(\alpha_n x)\,\mathrm{d}x \tag{4.10}$$

where $\alpha_n = (2n+1)\pi/L,\ p = \sigma_0 - u,\ q = k(u_x + s)_x,\ a = (j_+ - j_- - s_+k + s_-k)/2kL$ and $b = (j_+ + j_- - s_+k + s_-k)/2k$.

Proof 4.1: The inhomogeneous boundary conditions are transformed to homogeneous ones. To achieve that u and v are introduced such that $\sigma = u + v$ and u satisfies the non-homogeneous BCs:

$$x = -L/2: \quad u_x = j_-/k - s_- \tag{4.11}$$

$$x = +L/2: \quad u_x = j_+/k - s_+ \tag{4.12}$$

where the subscripts for j and s indicate evaluation at the corresponding endpoint. A simple function u and hence v can be defined as follows:

$$u(x) = Ax^2 + Bx \tag{4.13}$$

where

$$A = \frac{(j_+ - j_-) - (s_+ - s_-)k}{2kL} \tag{4.14}$$

$$B = \frac{(j_+ + j_-) - (s_+ + s_-)k}{2k} \tag{4.15}$$

Hence, the problem for v is homogenous as follows:

$$v_t = kv_{xx} + q \tag{4.16}$$

$$v_x(-L/2, t) = v_x(+L/2, t) = 0 \tag{4.17}$$

$$j(+L/2, t) = j_+ \tag{4.18}$$

$$v(x, 0) = \sigma_{res} - u(x) \tag{4.19}$$

where

$$q = k(u_x + s)_x \tag{4.20}$$

The solution for (4.14) can be written as:

$$v(t) = \sum_{n\in\mathbb{Z}} v_n(t)\cos(\alpha_n x) \tag{4.21}$$

where

$$v_n(t) = w_n e^{-k\alpha_n^2 t} + \frac{1}{k\alpha_n^2}\frac{1}{L}\int_{-L/2}^{+L/2} q(x)\cos(\alpha_n x)\,\mathrm{d}x \tag{4.22}$$

$$w_n = \frac{1}{L}\int_{-L/2}^{+L/2} f(x)\cos(\alpha_n x)\,\mathrm{d}x \tag{4.23}$$

$$f(x) = \sigma_0 - u(x) \tag{4.24}$$

Due to superposition, the problem has now homogeneous boundary conditions but contains a nonzero, in general, source term. The solution is provided in (4.18) ■.

4.2.2. Stationary Analysis

Blech studied the dynamic equilibrium between flux due to EM and SM ($J_{EM} + J_{SM} = 0$) which can be stated as the stress difference between the ends:

$$\Delta\sigma_{\mathrm{Blech}} = \frac{eZ\rho}{\Omega} jL \tag{4.25}$$

However, the steady state of a system under material migration is achieved when all three main sources of atomic fluxes cancel each other out ($J_{EM} + J_{SM} + J_{TM} = 0$). Indeed, solving Eq. (4.3) under steady state via integration, results in a similar useful and accurate model introduced in the previous Chapter for the stress difference between the stripe ends can be obtained as:

$$\Delta\sigma_{\mathrm{new}} = \frac{eZ\rho}{\Omega} jL + \frac{Q}{\Omega}\Delta \ln T \tag{4.26}$$

While Blech model has been used for many years, it is temperature agnostic. This new criterion captures the effect of temperature, stress and current density.

4.2.3. Lifetime Analysis

As it was mentioned the classical mean time to failure of an interconnect is often evaluated by the well-known Black's equation where A is a constant and n is a model parameter which are obtained empirically. Yet, determining the current density exponent is a crital task which may vary for interconnects with different electrical, thermal and mechanical loads. We propose to determine a true mean time to failure based on the atomic flux divergences. In other words, the parameters in Black's model can be determined readily by the following method.

Here we build a novel systematic basis for lifetime modeling based the fundamental definition of lifetime. As it was shown in the previous Section, an interconnect may experience different aging stages during its lifetime. Thus, based on the general failure or aging mechanism, a generic lifetime expression can be stated as (Fig. 1.4):

$$t_{\text{lifetime}} = \max\{t_{\text{nuc}} + t_{\text{vis}} + t_{\text{grow}}\} \tag{4.27}$$

In order to find t_{lifetime}, in (4.27), we decompose the expressions to: t_{nuc}, t_{vis} and t_{grow}. Regarding t_{nuc}, it can be obtained when the stress reaches the critical value via equating as follows:

$$\sigma(t) = \sigma_{\text{crit}} \tag{4.28}$$

While a closed form for t_{nuc} can be found based on the strongest term in the series in (4.3), classical numerical methods can be applied to solve (4.28) in which mathematical complexity is very straightforward and not challenging. For t_{vis}, depending on the void type and its motion velocity (e.g. (1.14)) and the visibility criteria (e.g. specific length or volume), the time to

visibility can be obtained. Similarly, the late growth phase, t_{grow} can be obtained when void is grown up to a critical length, L_{crit}. Thus, having the speed of void presented in (1.14), the time for a void to cause a total failure can be computed.

Korhonen solved (1.20) which is similar to (4.3) without including thermomigration caused by Joule heating for straight line with various boundary conditions [29]. Based on solutions in [29] , authors in [102] using a simplified version of (4.27) where t_{vis} is ignored, propose a time to failure model for slit-like void for a semi-infinite line (i.e. one blocking end and long length) which is as follows:

$$t_{\mathrm{lifetime}} = t_{\mathrm{nuc}} + t_{\mathrm{grow}} = \frac{\pi}{4}\frac{\Omega kT}{(eZ\rho j)^2 BD_v}{\sigma_{\mathrm{crit}}}^2 + \frac{kT}{eZ\rho j D_s}L_{crit} \tag{4.29}$$

Indeed, t_{nuc} in (4.29) is obtained by solving (4.28) for a semi-infinite line (i.e. one blocking end and long length). Also, t_{grow} is when void is grown up to a critical length, L_{crit}. Thus, having the speed of void presented in (1.14), the time for a void to cause a total failure can be computed.

A more advanced work is done by the author in [103] where again t_{nuc} is obtained by solving (4.28) for a finite line (i.e. blocking boundaries).

$$t_{\mathrm{nuc}} \approx \frac{L^2 kT}{2D_a B\Omega} ln\left\{\frac{\frac{eZ\rho jL}{2\Omega}}{\sigma_{\mathrm{res}} + \frac{eZ\rho jL}{2\Omega} - \sigma_{\mathrm{crit}}}\right\} \tag{4.30}$$

In (4.30) σ_{res} is the residual stress due to thermal expansion. For the growth phases they employ a progressive model for resistance change based on the length and the speed of void growth, and resistivity of line and liner.

It should be noted that the condition for saturation must be checked making sure whether a new steady state is achieved. The time needed to reach the saturated volume is as follows:

$$t_{\text{sat}} = t_{\text{nuc}} + \frac{L^2 kT}{2D_a B\Omega}\left(1 + \frac{2\sigma_{\text{res}}\Omega}{eZ\rho jL}\right) \tag{4.31}$$

As it can be seen, none of these models include thermomigration due to Joule heating as they all borrow Korhonen's model in their core.

In addition to exclusion of thermal effects in the aforementioned models and similar ones [47, 31], extending them to complex structures and real-world interconnect networks is difficult due to many assumptions made during these models derivations.

To overcome such complexity, we propose a new approach for looking at lifetime. As it was discussed before, the key to determine the depletion or accumulation of atoms in a region is to look at the overall intake and outtake of atoms due the multiple fluxes. This quantity can be measured accurately by atomic flux divergence. Therefore, it can be stated that

$$\text{MTF} \propto \frac{1}{\nabla . \vec{J}} \tag{4.32}$$

The individual flux divergences can be mathematically obtained as follows:

$$\nabla . \overrightarrow{J_{EM}} = \left[\frac{\nabla C}{C} + \left(\frac{E_a}{kT} - 1\right)\frac{\nabla T}{T} + \frac{\nabla^2 V}{\nabla V}\right] . \overrightarrow{J_{EM}} \tag{4.33}$$

$$\nabla . \overrightarrow{J_{TM}} = \left[\frac{\nabla C}{C} + \left(\frac{E_a}{kT} - 2\right)\frac{\nabla T}{T} + \frac{\nabla^2 T}{\nabla T}\right] . \overrightarrow{J_{TM}} \tag{4.34}$$

$$\nabla . \overrightarrow{J_{SM}} = \left[\frac{\nabla C}{C} + \left(\frac{E_a}{kT} - 1\right)\frac{\nabla T}{T} + \frac{\nabla^2 \sigma}{\nabla \sigma}\right] . \overrightarrow{J_{SM}} \tag{4.35}$$

$$\nabla . \overrightarrow{J_{DM}} = \left[\frac{E_a}{kT}\frac{\nabla T}{T} + \frac{\nabla^2 C}{\nabla C}\right] . \overrightarrow{J_{DM}} \tag{4.36}$$

Considering EM, TM and SM, the total flux divergence can be written as follows ($E_a/kT \gg 1,2$)::

$$\nabla . \vec{J} \approx \left[\frac{E_a}{kT}\frac{\nabla T}{T} + \frac{\nabla^2 V}{\nabla V}\right].\overrightarrow{J_{EM}} + \left[\frac{E_a}{kT}\frac{\nabla T}{T} + \frac{\nabla^2 T}{\nabla T}\right].\overrightarrow{J_{TM}} + \left[\frac{E_a}{kT}\frac{\nabla T}{T} + \frac{\nabla^2 \sigma}{\nabla \sigma}\right].\overrightarrow{J_{SM}} \quad (4.37)$$

Plugging the fluxes due to EM, TM and SM and rewriting (31) quantitatively from (2) yields:

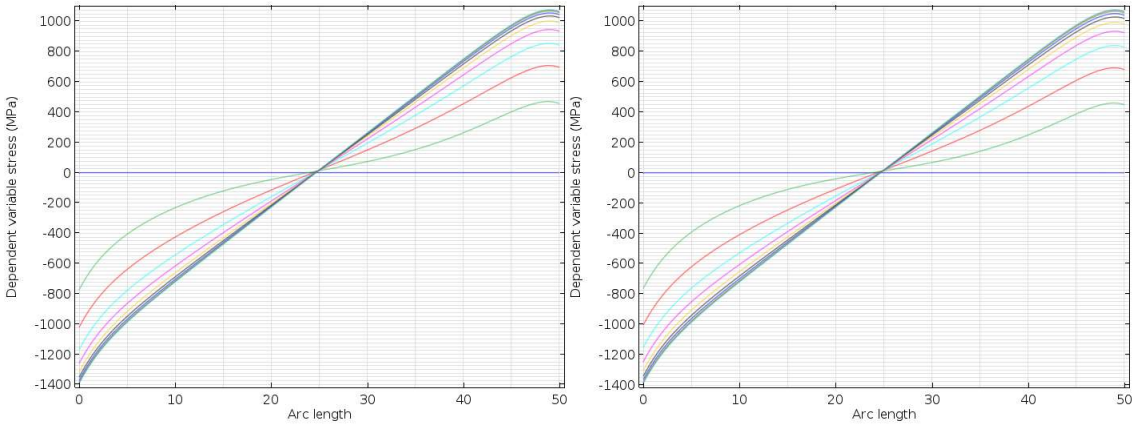
$$\text{MTF} \propto \frac{1}{D(\alpha j^2 + \beta j^3 + \gamma j^4)} \approx A j^{-n} e^{\frac{E_a}{kT}} \quad (4.38)$$

where α, β and γ are determined by the parameters in experiments or equivalently the ones in previous equations. The rightmost-hand side equation is the well-known Black's equation where A is a pre-exponential constant factor and n is an empirically found parameter. As it can be seen there is an intuitive agreement between flux divergence with Black's equation where the current density exponent n and constant A are traditionally determined empirically. In other words, flux divergence analysis can enrich Black's empirical equation by enlightening the model parameters. Empirical extractions of n also usually set it to be between 2 to 4 – depending on which terms are more dominant [27].

Material Effects: Microstructures and Interfaces: Interconnect aging is a diffusive process and thus very sensitive to diffusion coefficients and constants. In the above calculation diffusivity is assumed to be temperature dependent described as follows:

$$D = D_0 e^{-\frac{E_a}{kT}} \quad (4.39)$$

where D_0 is the self-diffusion coefficient of the conductor material and E_a is the activation energy for diffusion [10]. It should be mentioned that the more accurate model for activation energy depends on hydrostatic stress, vacancy formation and diffusion energy. Nevertheless,



(a) (b)

Figure 4.1: Stress evolution using (4.3) for the cases where (a) D is costant (b) D is not constant.

this dependency is found to be weak and a constant activation energy is widely used by researchers.

Korhonen [29] discusses the effect of different parameters such as stress and temperature on diffusion coefficient while solving (1.14) under various settings. His numerical results turned out to be not too different from the analytic solutions with a constant D. Similar observations were made when solving (4.3) in which TM is included. Fig. 4.1 shows the solutions of (4.3) when diffusion depends on the parameters mentioned above versus the case where diffusion coefficient is constant. As it can be seen the solutions for both cases are matching quite well.

Furthermore, the rate of mass transport and void growth in dual damascene process largely depend on lattice microstructure such as grain boundaries and interfaces. The fastest path for atoms to migrate is at the capping layer interface. The effective diffusivity in copper interconnects, D_{eff}, can be written in terms of diffusions and dimensions of bulk, grain boundaries, liner interface and capping surface as follows:

$$D_{\text{eff}} = D_{\text{b}} n_{\text{b}} + D_{\text{gb}} \delta_{\text{gb}} \frac{1}{d} + D_{\text{l}} \delta_{\text{l}} \left(\frac{1}{h} + \frac{2}{w}\right) + D_c \delta_c \left(\frac{1}{h}\right) \tag{4.40}$$

where the subscripts correspond to the diffusion pathway, D_{b}, D_{gb}, D_l, and D_{c} are diffusion constants, δ_{gb}, δ_{l} and δ_{c} denote the effective thicknesses, d is the grain size, and n_{b} is the fraction of atoms diffusing through the bulk. Also, w and h are the width and thickness of a wire [91].

Fig. 4.2. demonstrates how a passive dummy via with no electric current can affect the lifetime of a wire through diffusion. The proposed systematic way of computing lifetime explained above can distinguish between the structures shown in Fig 4.2. The structure shown in Fig 4.2 (b) differs from that in Fig 4.2 (a) in that it has one dummy via above the active wire. Even though it does not carry current, it affects the EM process by slowing down the atom and vacancy fast track at the interface of the copper and capping layers. Note that the effective diffusivity of interconnect is affected and can be modeled using (4.40). A huge slack in the interface by introducing more dummy vias can lead to a very long time to failure and therefore the wire might practically be considered immortal [104]. This is observed in finite element simulation [20] as the steady state for net I is reached 5 times earlier than that for net II (Fig 4.2).

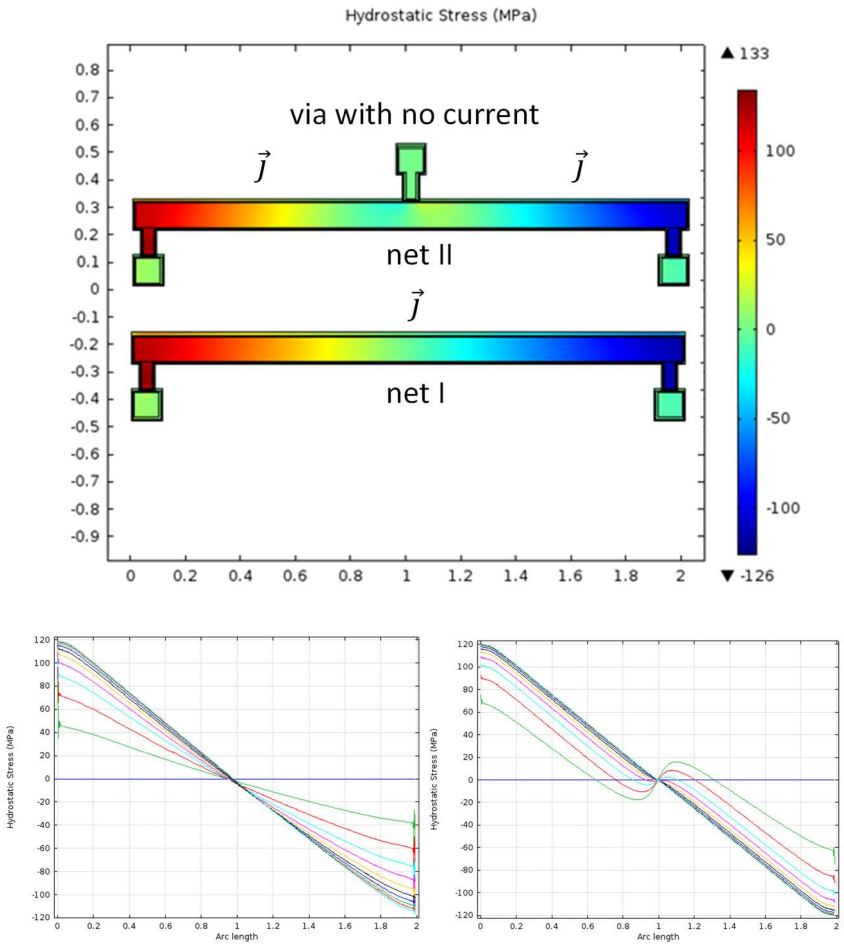


Figure 4.2: Current and stress distribution in two segments. (a) a simple interconnect (b) the same interconnect segment with a dummy via in the middle. The via does not carry current but changes the bulk effective diffusion which prolongs the time to reach steady state. Yet, the effect is not visible in steady state. (J=1mA/um^2).

In addition, impurity or bulk imperfection which usually appear in a form of pre-existing voids in capping interface or dislocations, can be included similarly. These embryo voids are mainly produced by the thermal mismatch between copper and the surrounding dielectric and can significantly affect the electromigration lifetime [105].

In short, to include the microstructural effect of lattice, detailed lifetime analysis may be needed. Fig. 4.3 shows detailed experiments including microstructure effects. In these experiments, different diffusion coefficients are used in different regions within the lattice.

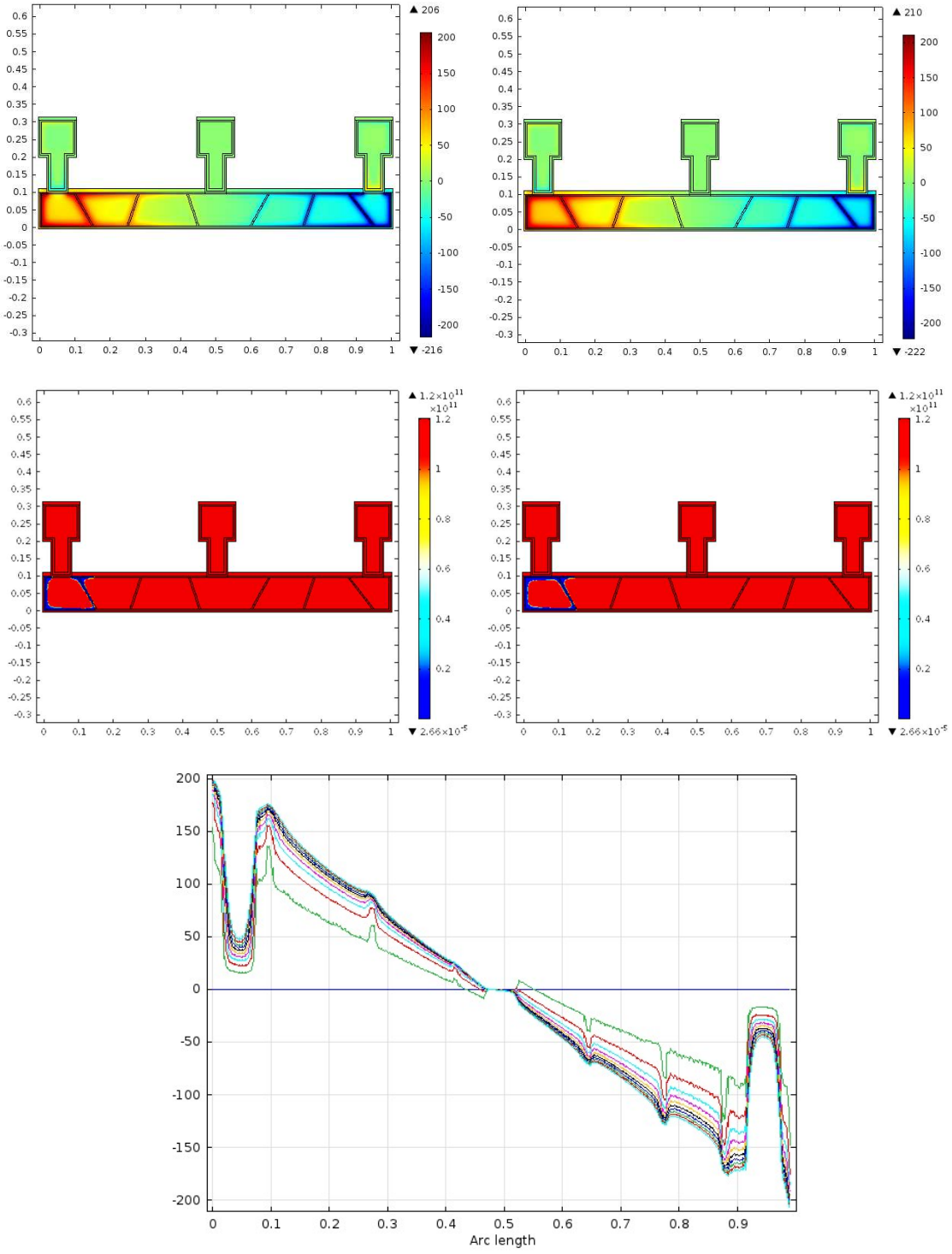


Figure 4.3: Stress evolution and void nucleation in bamboo-like interconnect obtained using COMSOL Multiphysics. $D_{Cu\text{-}SiN\_cap} > D_{Cu\text{-}Ta\_liner}$ (left), $D_{Cu\text{-}SiN\_cap} = D_{Cu\text{-}Ta\_liner}$(right).

4.3. New Models for Interconnect Networks

We employ the presented models for temperature and stress across the line and present models for interconnect network.

Definition 4.1: Let G be an interconnect network graph with n nodes $N = \{1, \ldots, n\}$ and b branches $B = \{1, \ldots, b\}$. G has c metallic connected components $G_{cc} = \{G_1, \ldots, G_c\}$ (i.e. a multi-segment which are continuously connected with metal without detaching by barrier layer) where G_k has n_k nodes $N_k = \{1, \ldots, n_k\}$ and b_k branches $B_k = \{1, \ldots, b_k\}$. Each branch i connects two nodes c_i (cathode) and a_i (anode) with voltages V_{c_i} and V_{a_i} and nodal temperatures T_{c_i} and T_{a_i}. Let σ_i, be the stress distribution of branch i with nodal stresses σ_{c_i} (cathode) and σ_{a_i} (anode). Let T_{m_i} and T_{0_i} be the max temperature rise and the external temperature of branch i. Let $j_i$be the current density of branch i. Let L_i and W_i be the length and the width of branch i and $A_i = W_i L_i$.

4.3.1. Transient Model

Having the transient solution for each section, $\sigma_i(x, t)$, by (4.8) – (4.11), we only need to make sure the boundary conditions are satisfied for all junctions (zero overall inflow/outflow fluxes):

$$\forall\, i \in N \qquad \sum_{k,l \in b\{i\}} j_k = 0, \;\; \sigma_k(x_i, t) = \sigma_l(x_i, t) \tag{4.28}$$

where $b\{i\}$ are the branches ending at i and x_i is its location.

4.3.2. Steady State Model

To extend the model for interconnect networks, we need to study the atom conservation under temperature effect stated as follows (a given interconnect network G, $\forall\, G_k \in \mathrm{G_{cc}}$):

$$\int_{G_k} \Delta C\, dV = \int_{G_k} \Delta C\, dV = -\frac{C_0 H}{B} \int_{G_k} \sigma\, dA = 0 \tag{4.29}$$

where C and C_0 are atom concentration and its initial value. B is the bulk modulus. Assuming the same thickness, H, in a layer, $dV = HW_i dx$, (4.29), in terms of its branches, yields:

$$\int_{G_k} \sigma\, dA = \sum_{i \in B_k} \int_0^{L_i} \sigma_{\mathrm{i}}(x)\, W_i\, dx = 0 \tag{4.30}$$

Plugging σ_{i} into (4.30), taking integral and plugging (3.2) into (4.30) (assuming $\Gamma_{\mathrm{i}} \ll \mathrm{L_i}$), yields an important expression:

$$\sum_{i \in B_k} \left(\frac{\sigma_{a_i} + \sigma_{c_i}}{2} + \frac{Q}{\Omega} \frac{T_{m_i} T_{0_i}}{T_{a_i} T_{c_i}} \right) W_i L_i = 0 \tag{4.31}$$

Hence, (4.26) ($\sigma_{c_i} - \sigma_{a_i} = eZ\rho j_i L_i/\Omega + (\ln T_{c_i} - \ln T_{a_i})Q/\Omega$) and (4.31) over the net provide stress at nodes. Application of this model to a complicated multi-branch structure extracted from an IBM benchmark is shown in Fig 1.8 (a). It confirms the model provides very accurate stress distribution matching the results from FEA experiments. The solid line shows the stress distribution along the long wire without considering temperature effect. The dotted line shows the results when the temperature is included. The new model confirms that thermomigration tends to aggravate compressive stress and potentially exacerbate the risk of extrusion or shorts. On the other hand, it mitigates tensile stress and possibly alleviates the risk of voiding or opens. Since the hottest location is usually towards the center of the line, some

atoms travel to anode and increase the compression, and some atoms move back to cathode and compensate depletion and consequently reduce the tensile stress. Intuitively, increasing temperature usually mitigates shrinkage and intensify expansion.

4.4. Conclusion

Due to the complex mutual dependencies, thermal and other aging factors are often assessed independently without considering their true physics-based correlations. Using the underlying physics of stress evolution, we developed a new analytical transient model and a compact steady state model for reliability assessment that accurately captures electrical, thermal and mechanical aspects. The proposed models are applied to IBM benchmarks. Further experiments on complex multi-segment interconnect networks are presented in the next Section when a novel formalism is introduced. The results indicate that ignoring temperature or not modeling it through thermomigration may lead to incorrect conclusions regarding mortality and lifetime. The proposed models can be used to determine: (1) transient analysis of aging of wires; (2) stress analysis of signal and power interconnect networks; (3) accurate conditions for voiding and extrusion; (4) new criteria for designers and CAD tools in terms of current density and lengths.

Chapter 5

Models Translating Electro-Thermo-Mechanical Effects into Voltage

We observed a very interesting relationship between electric potential and hydrostatic stress development during aging. We show that stress at nodes is a key factor to determine the health of an interconnect structure. We later introduce a novel formalism showing that it can be obtained only by knowing their voltages. Essentially, voltages are the necessary and sufficient information needed to analyze the reliability performance.

5.1. 1-to-1 Mapping (Stationary Analysis)

5.1.1. Single end-to-end line

Revisiting the Blech Effect presented in (1.19) for a simple end-to-end stripe line (Fig. 5.1) yields:

$$jL = \frac{\Omega}{eZ\rho}\Delta\sigma \tag{5.1}$$

jL

Figure 5.1: A simple end-to-end stripe line

where $\Delta\sigma_{max}$ is the maximum stress difference between the cathode and anode ends. For a symmetric interconnect, assuming zero initial stress, $\sigma_{cathode\_max} = -\sigma_{anode\_min} = \sigma_{ss}$.

$$jL = \frac{2\Omega\sigma_{ss}}{eZ^*\rho} \tag{5.2}$$

If the critical tensile stress for void nucleation, σ_{nuc}, is greater than the maximum steady state tensile stress, σ_{ss}, developed at the cathode end, no void will form and the line will not fail.

$$jL = \frac{2\Omega\sigma_{ss}}{eZ^*\rho} < (jL)_{crit} = \frac{\Omega\Delta\sigma_{nuc}}{eZ^*\rho} = \frac{2\Omega\sigma_{nuc}}{eZ^*\rho} \tag{5.3}$$

This is called the "Blech Product". The critical product provides a measure of the interconnect resistance against electromigration failure.

Rearranging (5.3) using the fact that $\Delta V = V_s - V_c = \rho jL$ yields a very interesting expression as follows:

$$\Delta V_{ac} = V_a - V_c = \rho jL = \frac{2\Omega\sigma_{ss}}{eZ^*} < \rho(jL)_{crit} = \frac{\Omega\Delta\sigma_{nuc}}{eZ^*} = \frac{2\Omega\sigma_{nuc}}{eZ^*} = \Delta V_{nuc} = V_{crit}^{v} \tag{5.4}$$

where ΔV_{ac} is the voltage difference between interconnect ends and ΔV_{nuc} is the equivalent voltage difference for a void to nucleate.

Definition 1. Let σ_{crit}^{v} and σ_{crit}^{h} be the critical stress for void and hillock. Thus, critical voltages can be defined as:

$$V_{\mathrm{crit}}^{\mathrm{v}} \stackrel{\mathrm{def}}{=} \frac{2\Omega}{eZ}\sigma_{\mathrm{crit}}^{\mathrm{v}} \tag{5.5}$$

$$V_{\mathrm{crit}}^{\mathrm{h}} \stackrel{\mathrm{def}}{=} \frac{2\Omega}{eZ}\sigma_{\mathrm{crit}}^{\mathrm{h}} \tag{5.6}$$

Indeed, the Blech condition is essentially a voltage constraint for immortality failure. In other words, for a single segment wire the immortality checking in terms of voltage (instead of conventionally mechanical stress) is:

$$\mathrm{V_a} - V_c < V_{\mathrm{crit}}^{\mathrm{v}} \tag{5.7}$$

Assuming $\mathrm{V_c} = 0$, the criteria for check

$$\mathrm{V_a} < V_{\mathrm{crit}}^{\mathrm{v}} \tag{5.8}$$

5.1.2. Complex Multi-Segment

The advantage of using voltage instead of ρjL is that, it can benefit from symmetrical arithmetic operations and thus be extended easily to multi-branch interconnects which led us to develop a new formalism. For example in the structure shown in Fig. 5.2, we can represent the mechanical stress in terms of voltage difference as follows:

$$\sigma_c - \sigma_b = \frac{Z^*\mathrm{e}\rho}{\Omega} j_1 L_1 = \frac{Z^*\mathrm{e}}{\Omega}(V_a - V_b) \tag{5.10}$$

$$\sigma_b - \sigma_a = \frac{Z^*\mathrm{e}\rho}{\Omega} j_2 L_2 = \frac{Z^*\mathrm{e}}{\Omega}(V_b - V_a) \tag{5.11}$$

Figure 5.2: Three terminal interconnect line.

While the relationship between stresses at two adjacent nodes (e.g. c-b and b-a) can be represented in terms of the jL product, a similar relationship cannot be obtained for non-adjacent nodes (e.g. c-a). In other words

$$\sigma_c - \sigma_a = \frac{Z^* \mathrm{e} \rho}{\Omega}(j_1 L_1 + j_2 L_2) \tag{5.12}$$

which requires to know the information between intermediate current density and wire lengths. However, this can be readily represented merely based on voltages at ending points (e.g. c and a) by:

$$\sigma_c - \sigma_a = \frac{Z^* \mathrm{e}}{\Omega}(V_a - V_c) \tag{5.13}$$

This facilitates the computation of stresses only based on the voltage of corresponding nodes. This can be extended easily to multi-branch interconnects which led us to developing a new formalism. Thus, for a given interconnect net graph G, we can rewrite (2) for all $G_k \in \mathrm{G_{cc}}$ with respect to any node $x \in N_k$. Rewriting (4.31) in terms of any arbitrary node x (e.g. node with the lowest voltage), yields:

$$\sum_{i \in B_k} \left(\sigma_x - \frac{Z^* \mathrm{e}}{\Omega}(V_{a_i} - V_x) + \sigma_x - \frac{Z^* \mathrm{e}}{\Omega}(V_{c_i} - V_x) \right) W_i L_i = 0 \tag{5.14}$$

Thus,

$$\sigma_x + \frac{Z^* \mathrm{e}}{\Omega} = \frac{Z^* \mathrm{e}}{2\Omega W L} \sum_{i \in B_i} (V_{c_i} + V_{a_i}) W_i L_i \tag{5.15}$$

Since usually the lowest voltage in an interconnect tree is zero, the condition required for immortality check in terms of voltage can be expressed as follows:

$$\sigma_x = \frac{Z^*\mathrm{e}}{2\Omega WL}\sum_{i\in B_i}\left(V_{c_i}+V_{a_i}\right)W_iL_i < \frac{\Omega\Delta\sigma_{nuc}}{eZ^*} = \frac{2\Omega\sigma_{nuc}}{eZ^*} = \Delta\mathrm{V}_{\mathrm{nuc}} = V_{\mathrm{crit}}^{\mathrm{v}} \tag{5.16}$$

Which can be further rewritten as:

$$\frac{1}{WL}\sum_{i\in B_i}\left(V_{c_i}+V_{a_i}\right)W_iL_i < V_{\mathrm{crit}}^{\mathrm{v}} \tag{5.17}$$

Interestingly, the summation of voltages appears in such formalism. It is surprising because, it does not seem to have an intuitive meaning from an electrical point of view as opposed to voltage difference. Apparently, this summation is in an implicit relationship with atomic conservation. The following example clarifies the new formalism.

Example 5.1: Fig. 5.3 shows stress development in a 3-terminal interconnect versus a 4 terminal interconnect structure. The current density and voltage distributions in the structures shown in Fig. 5.3 are shown in Fig. 5.4. We show reliability assessment via (5.13) is identical to analysis based on stress. Fig. 5.4 demonstrates current density and voltage distributions in both structure along the horizontal length (name the nodes). As it can be seen both stems in both structures carry the same current density, however, in Fig 5.3 (a) half of the incoming current is routed through a different layer through the via in the middle while in Fig 5.3 (b) the current flows through a branch in the same layer.

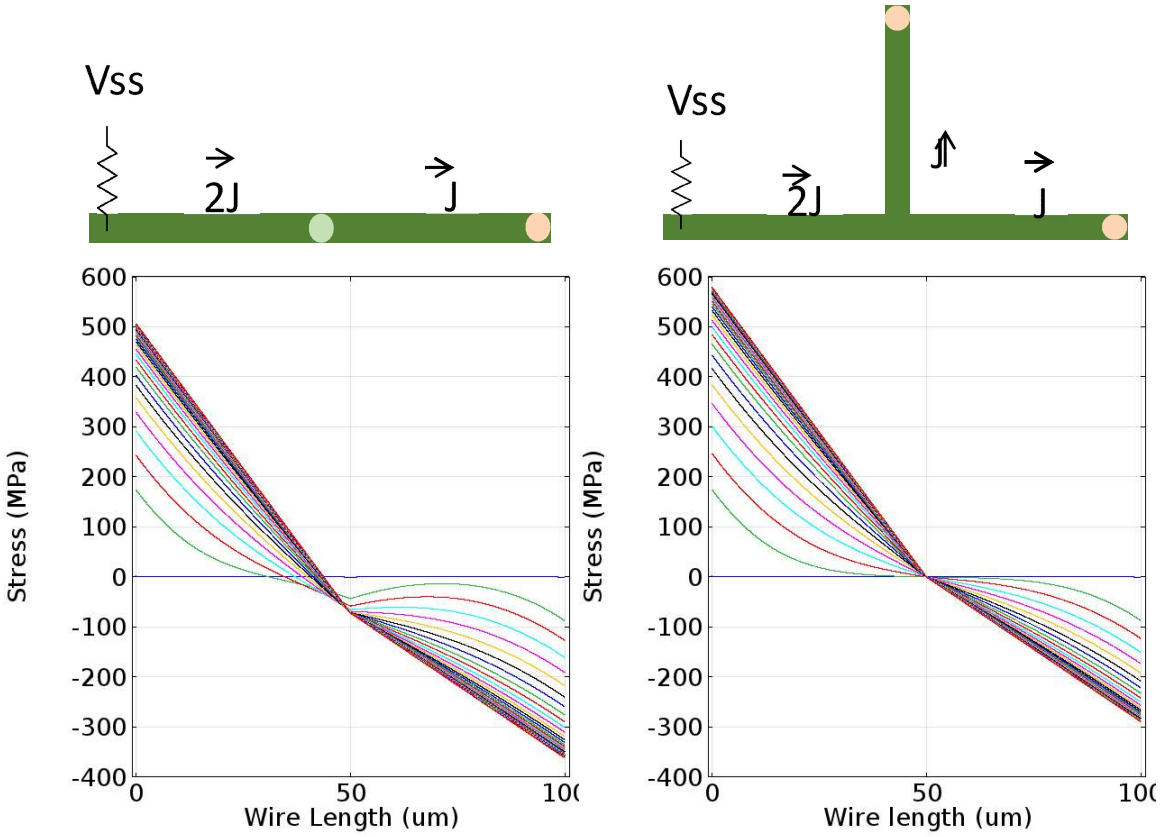


Figure 5.3: 3-terminal interconnect vs 4 terminal structure.

The mortality of the structure shown in Fig 5.3 (a) can be checked by evaluating (5.17) using their nodal voltages as follows:

$$\frac{(0+6mV)L/2+(6mV+9mV)L/2}{L}=10.5mV<11.4mV \tag{5.18}$$

Similarly, the condition can be checked for the structure shown in Fig 5.3 (a) by evaluating (5.17) as follows:

$$\frac{(0+06mV)L/2+(6mV+9mV)L/2+(6mV+9V)L/2}{3L/2}=12mV>11.4mV \tag{5.19}$$

The mortality violation ratios (which are useful information for physical designers to sort out the violations and their priorities for further layout manipulation) obtained using (5.17) can be expressed as follows for both structures, respectively:

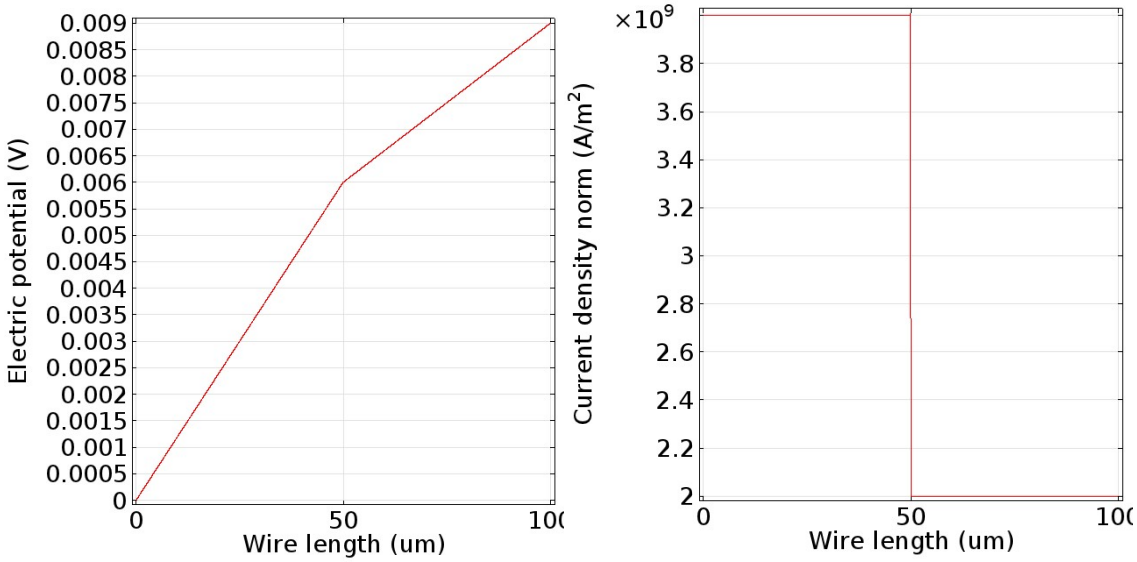


Figure 5.4: Current density and voltage distribution along the horizontal line in both structures shown in Fig. 5.3.

$$\frac{10.5mV}{6.34mV} = 92\% \tag{5.20}$$

$$\frac{12mV}{6.34mV} = 105.3\% \tag{5.21}$$

The mortaility violations ratios can also be obtained by comparing stress level with critical stress. The results obtained by detailed FEM experiments are as follows for both structures, respectively (See Fig 5.3):

$$\frac{506MPa}{550MPa} = 92\% \tag{5.22}$$

$$\frac{579MPa}{550MPa} = 105.3\% \tag{5.23}$$

It can be seen that (5.13) can offer an identical check with better representation and capability of being scaled freely to any complex structure. The voltage, V_n, can be obtained for a certain critical stress. For a stress of 550MPa, critical voltage is computed to be $(2\Omega\sigma_{nuc}/eZ^* = V_n)$ 11.4 mV.

Remark 5.1: EM assessment based on mechanical stress and physics-based models seems not intuitive to physical designers. This Chapter not only abstracts away the physics notations and concepts from the EM analysis, but also offers a compact model for EM immortality checking which is purely based on nodal voltages. Another immediate superiority of the proposed model to stress-based analysis is that nodal voltages are already available to the designers and no further computation is required to perform the EM analysis. The other advantage of this method is that while the well-known jL product cannot be directly extended to multi-segment tree interconnects (e.g. $(jL)_{eff} = max \sum_k j_k L_k$ method is limited to detect the impact of adjacent branches), the presented model can be easily employed by any complex structure.

5.1.3. Single end-to-end line considering thermal effect

Reworking the new stationary model (3.3) proposed in Chapter 3 with substituting ρjL with its nodal voltages yields:

$$\sigma_c - \sigma_a = \nu(V_a - V_c) + \tau(\ln T_c - \ln T_a) \tag{5.24}$$

where $\nu = Ze/\Omega$ and $\tau = Q/\Omega$ are constants.

Significant expression in (5.9), indeed, obtains its powerful simplicity from taking advantage of the following subtle techniques: (1) This substitution: $\Delta V = V_{\mathrm{s}} - V_{\mathrm{c}} = \rho jL$ (2) natural log form of temperature effect. These adjustments and the new formalisms increase flexibility and scalability of the original models where intended for handle only end-to-end structures. Also, as it was discussed, eliminating the notation of an intangible quantity (hydro static stress) and representing it in terms of nodal voltages is not only very useful for physical designers but it also increases the integrability of our method into the rest of the signoff stage

verifications (e.g. power and performance analyses with reliability or voltage drop signoff checks) can readily interact with each other using a universal language, voltage.

5.1.4. Complex Multi-Segment Structure considering thermal effects

For an arbitrary end-to-end segment i, we reformulate (4.26) using the fact that $\Delta V_i = V_{a_i} - V_{c_i} = \rho j_i L_i$. As it was mentioned the advantage of using voltage instead of ρjL is that, it can benefit from symmetrical arithmetic operations and thus be extended easily to multi-branch interconnects. This will help to build a relation between node voltages and temperatures and their stresses for multi-segment.

For instance, in the structure in Fig. 5.2, we can represent the stress in terms of voltage difference as:

$$\sigma_c - \sigma_b = \nu(V_b - V_c) + \tau(\ln T_c - \ln T_b) \tag{5.25}$$

$$\sigma_b - \sigma_a = \nu(V_a - V_b) + \tau(\ln T_b - \ln T_a) \tag{5.26}$$

While the relationship between stresses at two adjacent nodes (e.g. c-b and b-a) can be represented in terms of the jL product, a similar relationship cannot be obtained for non-adjacent nodes (e.g. c-a). In other words, $\sigma_c - \sigma_a = \nu(\rho jL_{cb} + \rho jL_{ba})$ requires knowing the intermediate current densities and wire lengths. However, this can be readily represented based on voltages at end points (e.g. c and a) by:

$$\sigma_c - \sigma_a = \nu(V_a - V_c) + \tau(\ln T_c - \ln T_a) \tag{5.27}$$

This facilitates the computation of stresses only based on voltage. Thus, for a given interconnect net graph G, we can rewrite (5.27) for all $G_k \in \mathrm{G_{cc}}$ with respect to any node $x \in N_k$. Rewriting (4.31) in terms of any arbitrary node x, yields:

$$\sum_{i\in B_k}\{\frac{1}{2}[\,\sigma_x-\nu\big(V_{a_i}-V_x\big)+\tau\big(\ln T_{a_i}-\ln T_x\big)$$

$$+\sigma_x-\nu\big(V_{c_i}-V_x\big)+\tau\big(\ln T_{c_i}-\ln T_x\big)] \tag{5.28}$$

$$+\tau\frac{T_{m_i}T_{0_i}}{T_{a_i}T_{c_i}}\}W_iL_i=0$$

Hence, for any node x, we have

$$\sigma_x=\frac{1}{2WL}\sum_{i\in B_i}\left(\nu\big(V_{c_i}+V_{a_i}\big)-\tau\big(\ln T_{c_i}+\ln T_{a_i}\big)-\frac{\mathcal{L}'^2}{L_i^2}\left(V_{c_i}-V_{a_i}\right)^2\right)W_iL_i \tag{5.29}$$

$$-\nu V_j+\tau\ln T_j<\sigma_{\text{crit}}$$

where $\mathcal{L}'^2=\frac{2Q\Gamma^2}{\rho\Omega T_0k_{Cu}}$ (see Chapter 4). With an approximation (5.14) can be expressed as follows:

$$\sigma_x+\nu V_x-\tau\ln T_x=\frac{1}{A}\sum_{i\in B_i}\left(\nu\frac{V_{a_i}+V_{c_i}}{2}-\tau\ln\frac{T_{a_i}+T_{c_i}}{2}\right)A_i \tag{5.30}$$

Definition 2. Let T_{0_i} and V_{0_i}be the end-point average voltage and temperature of line i. V_x^T and $\mathrm{V_k^T}$ associated with node x and net G_k are defined as the follows:

$$V_x^T\overset{\text{def}}{=}V_x-\frac{\tau}{\nu}ln\,T_x \tag{5.31}$$

$$V_k^T\overset{\text{def}}{=}\frac{1}{A}\sum_{i\in B_k}\left(V_{0_i}-\frac{\tau}{\nu}\ln T_{0_i}\right)A_i \tag{5.32}$$

Therefore, using (5.31), (5.32), definition 1 and definition 2, the criteria for voiding and extrusion are (for all $x\in N_k$ and $G_k\in \mathrm{G_{cc}}$):

$$V_x^T>V_k^T-V_{\text{crit}}^{\text{v}} \tag{5.33}$$

$$V_x^T<V_k^T-V_{\text{crit}}^{\text{h}} \tag{5.34}$$

Authors in [106] try to address the same problem. However, since they do not present the concept of critical voltage, their model adopts stress. The structure shown in Fig. 1.9 is a part of IBM Benchmarks for power/ground grid. This grid is studied with detailed FEM experiments and juxtaposed with proposed model. Voltages are obtained by SPICE. One may notice the similarity of stress and the voltage distribution (i.e. Fig. 1.9 (a) and (b)). It confirms that having nodal voltages, we can compute Joule heating or temperature distribution and thus stress can be obtained by transformation in (5.30).

5.2. IR-drop based Model (Transient Analysis)

The ultimate goal is to achieve a reliable interconnect delivery of power and signals across the chip, so that the device functions and performs predictably and long. In VLSI chip design, this goal is achieved in an iterative process; analysis and layout alternation. To analyze the health of an interconnect network, the problem is mainly narrowed down into two major sub-problems: voltage drop analysis (IR) and electromigration analysis (EM).

A large spectrum of techniques is used to perform IR drop analysis to make sure the interconnect network delivers the certain amount of power [107]. On the other hand, EM as a standalone problem has been studied vastly in terms of material concentration or hydrostatic stress evolution based on extending ideas in [20] and also in terms of mean time to failure by improving models such as [27].

While these two problems are traditionally investigated individually, they are mutually coupled in multiple ways: (1) due to redundancy the failures of some interconnect segments do not necessary result in the unacceptable voltage drop on the grids and may not be of concern [108, 109]. (2) EM-induced resistance degradation directly affects IR drop.

Modern approaches evaluate the resistance of network based on underlying physics [29] during EM – instead of investigating via-to-via wire segments reliability independently. During resistance evolution, they check the mixed criteria of electromigration conditions (i.e. minimum lifetime) and IR drop thresholds (minimum voltage). These approaches in their cores employ the model proposed in [29] which describes the material migration process due to EM based on hydrostatic stress evolution.

In [110], authors based on the steady state profile of stress distribution across the net determine the voids nucleation times and perform iterative void growth. They ultimately formulate the resistance change in terms of hydrostatic stress and void surface growth and check delivery requirements (voltage level). In [110], the nucleation time required for commencing the growth phase is obtained through steady state condition. Whereas, we discuss how steady state analysis provides useful information about violations and their severity, the nucleation time cannot be obtained by steady state analysis as it only provides the potential locations of failures. To mitigate this problem, authors in [53] provide an analytical model for stress distributions during nucleation phase. However, they manage to solve basically the model in [29] for a few simple interconnect structures and therefore, their approach cannot be directly used for complex multi-segment structures. To obtain the nucleation times from such methods, complicated and fast numerical methods are required to check a system of solutions (stress distributions in multi segments) against critical stress. Authors in [111] tried to mitigate the structural limitations by proposing a new analytical model for 1 dimensional multi-segment structures. In other work their model is the result of solving model in [29] in x- direction, by ignoring the effect of branches in y or z dimensions. However, it is very common that modern power grids or rails have multiple orthogonal branches for local power delivery which their

effects are shown to be non-negligible [39]. In general, they solve a single model in [29] for a single multi-segment wire where each segment has different current density with two zero atomic flux conditions at two ultimate ends. The intermediate nodes, however, are assumed to share the same atomic flux in both branch stems. However, it is very common to have a 3-way or 4-way nodes with long and complicated attached multi-segment sub nets. Therefore, the atomic flux of joining segments might not be the same. This may result in substantially different evaluation. Since their model and consequently their algorithm is an infinite series based model it did not let them to offer a closed form expression or approximation for nucleation time. Therefore, their approach will suffer from a big reliance on numerical model (e.g. Newton's method or bi-section search) to solve non-linear infinite series equation to find out nucleation time. Moreover, their model accuracy and efficiency tremendously depend on the number of eigen functions used to represent the transient solution. There are some other similar recent works suffering from similar problems, yet here we only discuss the most advanced ones.

In addition to specific limitations mentioned above, recently proposed methods share other common limitations which are motivations for this work: (1) Change in resistance is modeled by assuming that effective length of a wire is decreasing due to material degradation (and void surface motion) using the following relationship:

$$r = \rho \frac{l}{A} \tag{5.35}$$

where r is the resistance of a wire, ρ, l and A are the electrical resistivity, length and cross section area of the wire. However, it is physically not correct and misleading. In fact, it is the electrical resistivity of wire that is changing. We offer a new model for observing resistance

change which models the change in resistance through change in resistivity which is material property rather than wire geometrical properties. (2) In growth phase, the length is shrinking with a pace of the void surface. This velocity is also assumed to be constant in existing models by having a simplified constant current density-based rate of void surface movement (i.e. drift velocity). However, the rate of growth may vary during aging depending on time, location, temperature, and stress. In particular, considering EM as the sole driving force for voids motion is a very crude assumption since EM-induced side effects such as mechanical back stress flow and Joule heating will affect the speed of void motion and thus resistance change. Such factors only can be ignored when the products of metal length and current densities are far greater than the reported threshold values of the Blech short length effect of (i.e. 3000–7000 A/cm) or thermal conditions [112]. We offer a new void motion model to include all factors and will incorporate it into ultimate network reliability assessment procedure. (3) The common misinterpretation of time to nucleate is also worth mentioning as there are many works where it is considered (including the aforementioned works). They basically assume that the nucleation time is the initial time for void growth phase. Yet, it is a myth. In reality, during early stages, induced flaws (i.e. void or hillock embryos) remains electrically undetectable since they affect the line cross section only over a small area. Thus, resistance is considered to be almost constant [19]. Also, the morphological aspect of voiding is very simplified in these models by assuming a cross-sectional-wide void volume will form. The shape of a void embryo depends on the conditions and pre-existing impurities.

A new model will be presented for resistance change in the next section which address the aforementioned complications.

In addition to the limitations mentioned above, all existing models seriously lack taking thermal effects on IR and EM problems. In fact, as it was mentioned above, not only EM and IR drop problems are mutually related through change in resistance but also through Joule heating. In other words, Joule heating which is a byproduct of the entire thermo-electrical process also affect EM and IR. The recent developments are based on stress evolution models proposed in [29]. However, these models do not include the true effect of temperature on stress and ultimately wire resistance. Temperature affects the whole process in forming the steady state profile and time to nucleation. It also may accelerate, slow down or stop growths. The lack of a comprehensive model which can take the thermal effects on IR and lifetime result that researchers perform empirical data extraction and feed them into temperature-unaware models. Thermal effect is often, even still in new industrial research such as [42] (Samsung), modeled by empirical external data as a corrective constant fixed temperature increase or fluctuation (ΔT) to the average operating temperature. For instance, in [89] (Global Foundries), authors use a large-scale statistical analysis method under various experimental temperature, and attempt to fit an appropriate exponent in Black's MTF equation. While they showed the significance of thermal effect on interconnect lifetime, their approach still suffers from the empirical nature of statistical methods.

5.2.1. Resistive Model

An interconnect delivery network is healthy if the chip power requirement is met. In other words, voltage drops considering redundancy must be kept under a certain threshold. IR drop is a dynamic phenomenon due to material migration aging. Change in network resistance is therefore of concern. Resistance of a copper line during material migration initially varies

slowly, followed by an abrupt resistance jump due to extreme mass depletion or accumulation (i.e. critical void or hillock).

Dual-damascene copper interconnect lines empowered by barrier layer, typically ages through a multi-phase process: (1) Atoms travel and their concentration change across the network, however no voids or hillocks have formed yet. (2) In some segments the steady state may be achieved. In some other segments, however, atoms may be depleted or accumulated abundantly such that voids or hillocks sprout (i.e. t_{nuc} or t_{hillock}). Still, during early stages, induced flaws (i.e. void or hillock embryos) remain electrically undetectable since they affect the line cross section only over a small area. Thus, resistance is considered to be almost constant. (3) Some induced flaws may become large enough to span the whole section of the line (i.e. critical volume), forcing the current to go through the highly resistive barrier layer. It acts as a shunt layer and allows the further growth of the void, causing a progressive resistance change (i.e. t_{init}). (4) The resistance continues to change unless a new steady state is reached. In this case the void or hillock volume is saturated, and the resistance will stop changing (i.e. t_{sat}). While there might be some other possible mechanisms, this process has found to be the most common aging mechanism. Fig 1.7 shows such typical aging process for voiding.

Therefore, wire resistance chance in terms of atom concentration during material migration can be modeled as follows (Fig. 5.5):

$$r(t) = \frac{1}{A}\int_0^l \rho \, \mathrm{d}x \tag{5.36}$$

$$\rho(x,t) = \frac{\rho_b \rho_c}{\rho_b A_c + \rho_c A_b} A \tag{5.37}$$

$$\rho_c(x,t) = \rho_{c0}/H(x - x_v) \tag{5.38}$$

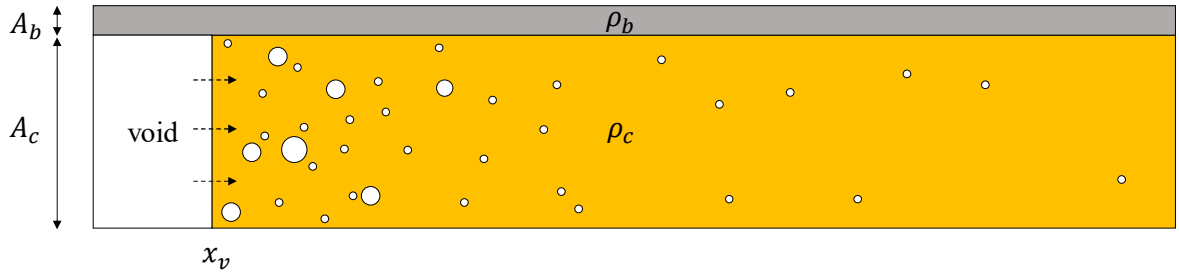


Figure 5.5: The evolution of the overall wire resistance in terms of barrier and metal resistivity and their geometry during void growth.

where $r(t)$ is the resistance at specific time t, ρ and A are the effective resistivity and cross-sectional area of the wire where subscript b and c denote the barrier layer and the metal resistivity. $H(x)$ is also the Heaviside step function. Thus

$$r(t) = \frac{\rho_b}{A_b} x_v + \frac{\rho_b \rho_{c0}}{\rho_b A_c + \rho_{c0} A_b} (l - x_v) \tag{5.39}$$

where x_v is the current location of the void and can be obtained by:

$$x_v(t) = \int_0^t \vartheta \, \mathrm{dt} = \Omega \int_0^t J \, \mathrm{dt} \tag{5.40}$$

$$\vec{\vartheta} = \begin{cases} \Omega \vec{J} & t_{\text{init}} < t < t_{\text{sat}} \\ 0 & t \leq t_{\text{init}}, t_{\text{sat}} \leq t \end{cases} \tag{5.41}$$

where ϑ is drift velocity or void/hillock surface growth rate, Ω and J are the atomic density and flux, respectively.

5.3. Conclusion

This chapter shows how designers can use the circuit nodal analysis to assess the reliability of the circuit without dealing with non-electrical concepts such as mechanical stress and physics-based models. Essentially, this Chapter offers fast models for reliability assessment which abstracts away the complex physics aspects of electromigration and help designers to perform EM analysis of the entire circuit merely based on the electrical nodal information.

Chapter 6

Algorithms and Tools for Full Chip Reliability Assessment of Interconnect Networks

In this Chapter, we describe novel algorithms based on the models we proposed throughout the previous chapters. We also introduce a new tool for full chip reliability assessment of interconnect networks which takes industry standard interconnect designs and performs stationary, transient and lifetime analyses.

6.1. Algorithms

6.1.1. Stationary

Algorithm 6.1 implements a thorough stationary assessment for determining immortality or vulnerability of the nodes (or vias) and branches (or wires). It takes interconnect design with reliability requirements (i.e. critical voltage or stress) as input. The algorithm performs circuit

analysis to obtain nodal voltages and temperatures. This stage can be externally done. In our experiments, we employ one-time SPICE simulation.

Parsing the interconnect network, we build a graph and find all connected components where interconnect components are continuously connected through copper without any barrier or liner. This is critical, while electrons can travel freely between connected components, atom conservation holds true within a closed connected component, which is the bases of our model presented in Chapter 2.

Algorithm 6.1 reliability assessment (SS)

Input: interconnect design (G), requirements (σ_{crit} , V_{crit})

Output: violations and severity

1: perform circuit analysis (obtain V_i and T_i)
2: find all connected components (G_{cc})
3: **for** $k = 1$ to c
4: Compute $V_k^T = \frac{1}{A}\sum_{i \in B_k}\left(V_{0_i} - \frac{\tau}{\nu}\ln T_{0_i}\right) A_i$
5: **end**
6: **foreach** $x \in N$
7: Find connected component G_{k} containing x
8: **if** ($V_x^T < V_k^T - V_{\text{crit}}^{\text{v}}$)
9: Voiding violation at node x - severity:$(V_k^T - V_x^T)/V_{\text{crit}}^{\text{v}}$
10: **end if**
11: **if** ($V_x^T > V_k^T - V_{\text{crit}}^{\text{h}}$)
12: Hillock violation at node x - severity:$(V_k^T - V_x^T)/V_{\text{crit}}^{\text{h}}$
13: **end if**
14: **end foreach**
15: **return** list

Having all connected components, we compute (5.31) for each component. Then, for each node we check the immortality conditions (5.33) and (5.34) using the computed (5.31) and (5.30) corresponding to the connected component which the node belongs to. The algorithm produces a report on both void and hillock violations and their severity including all electrical, thermal and mechanical effects.

6.1.2. Transient and Lifetime

A generic algorithm for evaluating the health of delivery network can be seen in Algorithm 6.2 where the interconnect design is given as well as the maximum tolerable voltage drop and minimum life expectancy.

The algorithm performs one-time circuit analysis using SPICE to obtain nodal and branch information. Then, the algorithm performs transient analysis based on the models presented in (5.36) - (5.41). While the voltage level and lifetime requirement are met, the wire resistance will be updated using (5.36) with proper boundary conditions shown in (4.4) - (4.10). The resistance continues evolving until a nucleation conditions happens anywhere within the components (i.e. a critical stress has been reached). In case of violation, an induced flaw starts to nucleate. In our experiments we considered both voiding and extrusion problems.

Also, depending on the failure mode, time to developing of an electrically detectable void is calculated using the model (in our experiments all voids are considered slit-like). In each update iteration, we also need to check if any saturation has occurred to stop the growth in that branch.

Algorithm 6.2 reliability assessment (TL)

Input: interconnect design (G), requirements ($V_{\mathrm{drop-max}}$, $\mathrm{MTF}_{\mathrm{min}}$)

Output: Lifetime

1: $\mathrm{t} = 0$
2: Perform circuit analysis.
3: **while** voltage drops in $\mathrm{G} < V_{\mathrm{max}}$ and $\mathrm{t} < \mathrm{MTF}_{\mathrm{min}}$
  4: Update resistance via (5.36)
  5: **if** anywhere atom concertation is beyond critical via (4.8) (t_{nuc})
    6: Induced flaw is nucleated
  7: **end if**
  8: **if** anywhere induced flaw is filling cross section (t_{vis})
    9: Induced flaw is grown via (2)
  10: **end if**
  11: **if** anywhere steady state is reached (t_{sat})
    12: Induced flaw is saturated
  13: **end if**
  14: Perform circuit analysis
15: **end while**
16: **return** t

6.2. RAIN – a tool

The algorithms for both steady state and transient analyses as well as lifetime analysis are implemented as an all-in-one solution software, RAIN (Reliability Assessment of Interconnect Networks). The languages used for building this tool include but are not limited to C, C++, Python, Perl, Matlab, Mathematica, JavaScript and R.

RAIN takes four inputs (1) interconnect design, (2) technology specifications, (3) initial stress and temperature, and (4) lifetime requirements. It takes voltages, computes Joule heating and assesses the reliability of a given multi-segment interconnect net taking all electrical, thermal and mechanical effects into account. It determines lifetime, violations and their severity in every metal layer. The code is available online [113] and can be run on desktop machines. For more accuracy, one may implement the complete form of series-based solution in (4.8) – (4.10) used in (5.36) – (5.41) which require more powerful machines.

6.3. Discussion

Models and algorithms presented in this Chapter are applied to various IBM power grid benchmarks. Table 6.1 shows the results comparing the violation predicted by the proposed model and the existing ones [29, 20, 39]. There is a considerable number of different violations which are not detected or wrongly detected by the existing models. The average disparity between the new model and experiments shown in Table 6.1 is below 1% while the error in classical based models is up to 14% and can be worse under various technologies and loads.

6.4. Conclusion

We show that first the interconnect network must be decomposed into connected components and then based on geometrical and electrical information of the components reliability analysis is performed.

We showed that two hazardous situations may occur: (1) in some cases, the existing models may wrongly scrutinize reliability in unfailing parts and consequently impose unnecessary design tightening and (2) in some other cases, the models may underestimate serious reliability

Table 6.1: Experimental results (predicted violations) proposed model vs existing models

Name	Nodes	Branches	Incompatible Violations
IBMPG1	30638	30027	155
IBMPG2	127238	208325	683
IBMPG3	851584	1401572	3126
IBMPG4	953583	1560645	5726
IBMPG5	1079310	1076848	95901
IBMPG6	1670494	1649002	43696

problems causing unpredicted behaviors or catastrophic failures to occur. The existing models for reliability evaluation are usually pessimistic in case of interconnect voiding and optimistic when extrusion occurs. Time-consuming and not converging reliability assessments as well as undesired chip behaviors are the common expensive outcomes of such models. (σ_{crit}=500MPa.)

In brief, the incompatibles can be explained as follows. The application of current density results in EM. As an immediate side effect, a temperature rise occurs (Joule heating). The temperature gradient produces flux and consequently causes TM. While electrical current is applied and temperature raises, stress develops simultaneously. These fluxes compete against each other and reconcile in the steady state. In fact, atoms travel towards the anode (due to EM) and at the same time tend to move from hot to cool places (due to TM). Intuitively, increasing temperature usually mitigates shrinkage and intensify inflation. This may cause serious temperature effects (i.e. various stress aggravation or alleviation) that can be missed by the existing models. Thermomigration interacts with electromigration and stress migration, and may result in (1) asymmetric stress distribution, (2) early hillock formation (shorter lifetime), (3) late voiding (longer lifetime), (4) non-end failures. The proposed model explains

many experimental observations that may have been inexplicable before. Fig. 6.1 shows the interface of the tool we developed for reliability assessment of large interconnect grids under thremo-electro-mechanical stress.

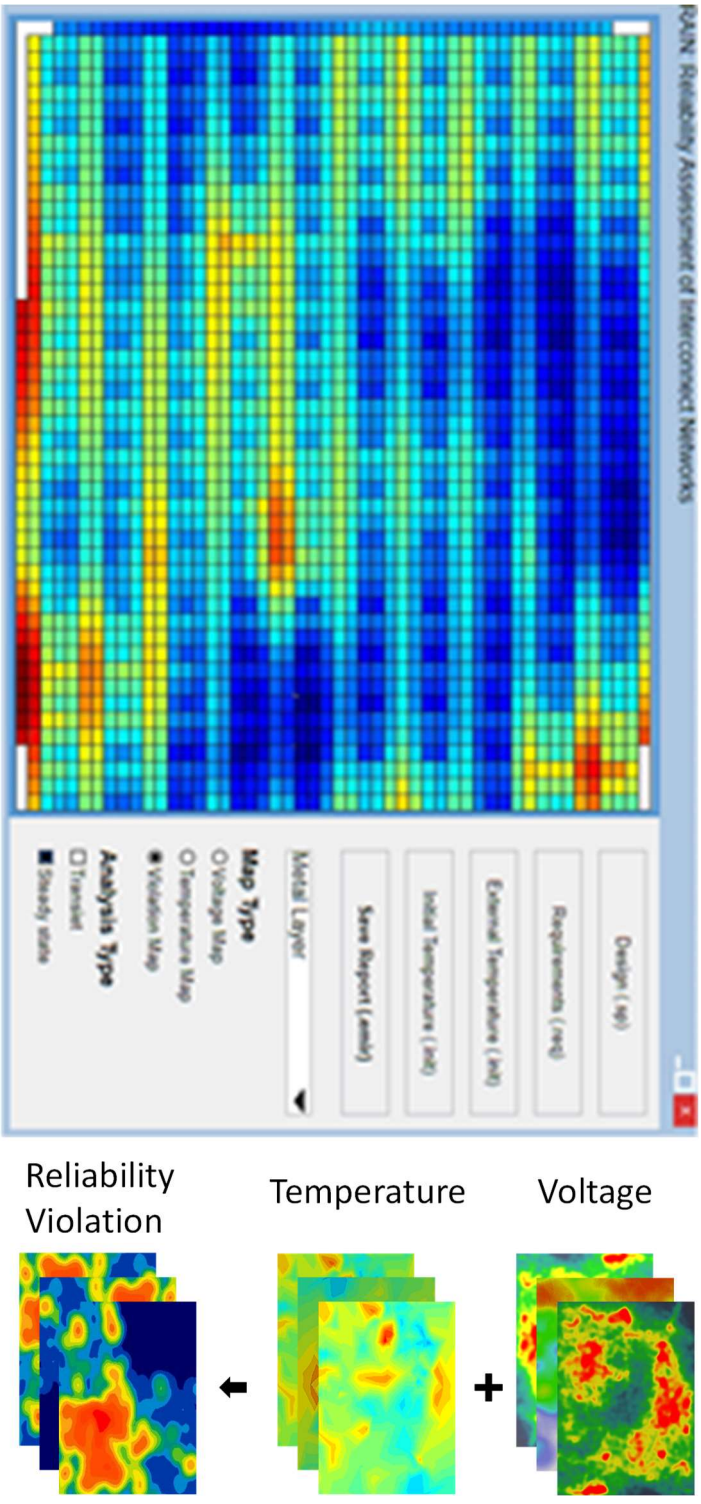


Figure 6.1: Tool: Reliability assessment of interconnect networks. It receives voltages and temperature, translates them to stress and reports violations. [113]

Chapter 7

Model for Temperature Distribution in Interconnect

In this Chapter, the heat generation and its development and distribution within interconnect is investigated in detail. While there is a large body of research studying a similar problem [67, 99], they are devised for mass transport induced aging context and therefore limited in practical use. In short, they are limited in modeling non-uniform temperature distributions where they assume the wire ends carry the same temperature. Moreover, since mass transport is a thermally activated process, the geometrical and thermal properties of wires need to be modeled almost without compromising which were done in similar works.

Since temperature rise and gradients are the trigger forces for thermomigration, we developed a completely new model based on the fundamental heat generation. The developed model can be considered for reliability and thermal analysis as a standalone tool. We also present several useful mathematical tools which are able to compute important quantities and thus embedded in various physical design tools where various thermal aspects or phenomena are of interests.

7.1. The Model

Heat distribution due to the transient electro-thermal behavior is captured by the following equation [74]:

$$\rho_m c_p \frac{\partial T}{\partial t} + \nabla q = Q \tag{7.1}$$

The left term describes the transient behavior of temperature where ρ_m and $c_p$are the mass density and the specific heat, respectively. The product, $\rho_m c_p = \theta$, commonly termed as the volumetric heat capacity, measures the ability of a material to store thermal energy). The middle term is due to the heat flux descried by the Fourier's heat conduction law. The right term,Q, is due to various heat generation processes.

The net heat transfer process is described by the Fourier's law of heat conduction:

$$q = -k\nabla T \tag{7.2}$$

where q is the local heat flux, k is the material's thermal conductivity.

The total heat can be generated by several sources as follows:

$$Q = Q_{jh} + Q_{Thomson} + Q_{convection} \tag{7.3}$$

The heat terms in the right side of (7.3) are due to the Joule heating effect, the Thomson effect and the convective heat transfer, respectively from left to right.

Thermal energy generation caused by Joule heating effect can be described by the following equation:

$$Q_{jh} = |\nabla V|^2 \rho(T)^{-1} = j^2 \rho(T) \tag{7.4}$$

where Q_{jh} is the rate of heat transfer due to the Joule heating, V is the electric potential and $\rho(T) = \rho_0(1 + \beta(T - T_0))$ is the electrical resistivity (with ρ_0 as the electrical resistivity at the temperature T_0, and β as the temperature coefficient of resistivity). The effect of temperature on electrical resistivity (ρ) is found to be very small and thereafter negligible.

The heat produced by the Thomson effect can be expressed as:

$$Q_{Thomson} = -\kappa j \nabla T \tag{7.5}$$

where κ is the Thomson coefficient. The Thomson effect is generally small compared to other sources and can be safely neglected.

The basic relationship for the rate of heat transfer per volume by convection is:

$$Q_{convection} = \frac{h}{\ell}(T_0 - T) \tag{7.6}$$

where T_0 is the external temperature, h is the coefficient of heat transfer and ℓ is the thermal characteristic length for heat transfer. The heat transfer coefficient for conductor surrounded by dielectric is widely modeled by $h = \frac{k_{ILD}}{t_{ILD}}$ with k_{ILD} and t_{ILD} being the thermal conductivity and thickness of the dielectric, respectively.

To model the multi-dimensional heat spreading phenomenon (i.e. taking the effect of convection through dielectric and vias –which is usually heat loss downwards-- into account properly), ℓ must be calculated precisely based on the geometrical, topological and thermal attributes of interconnects, dielectric as well as layout (i.e. adjacent wires). In this Chapter we used the following model [67, 99] which matches perfectly with our FEM simulation:

$$\ell = \frac{wt}{t_{ILD}}\left(\frac{w + d}{2w} + \frac{t_{ILD} - d/2}{w + d}\right) \tag{7.7}$$

where w, t, t_{ILD} and d are the width of wire, thickness of wire, the thickness of dielectric and the wire spacing (i.e. the distance between two adjacent wire). The common dimensions in modern technology nodes has the trend of $t = t_{ILD} = 2w = 2d$.

Depending on different layout and operating conditions, ℓ may be described by different expressions. However, all the equations derived here are still valid as long as the appropriate ℓ is determined by either an appropriate analytical expression or extracted from simulation.

Thus, under stationary condition (7.1) can be written as follows:

$$k\nabla^2 T - \frac{h}{\ell}(T - T_0) + j^2\rho = 0 \tag{7.8}$$

Definition 7.1. *Given the geometrical, topological and thermal attributes of interconnects, dielectric as well as layout, we can define an effective thermal length*

$$\Gamma^{-2} = \frac{1}{k}\frac{h}{\ell} \tag{7.9}$$

Thus, using Definition 7.1, (7.8) in 1-dimension (1D) can be seen as a second order linear homogeneous differential equation with constant coefficients:

$$T'' - \left(\frac{1}{\Gamma^2}\right)(T - T_0) + \frac{j^2\rho}{k} = 0 \tag{7.10}$$

The solution to (7.10) for a single wire with initial conditions of $T(-L/2) = T_1$ and $T(+L/2) = T_2$ (temperature at both ends where $-L/2 < x < L/2$), is obtained as:

$$\begin{aligned} T(x) = &\left(\frac{T_1 + T_2}{2} - \frac{j^2\rho\Gamma^2}{k} - T_0\right)\operatorname{sech}\left(\frac{L}{2\Gamma}\right)\cosh\left(\frac{x}{\Gamma}\right) \\ &+ \left(\frac{T_1 - T_2}{2}\right)\operatorname{csch}\left(\frac{L}{2\Gamma}\right)\sinh\left(\frac{x}{\Gamma}\right) + \left(\frac{j^2\rho\Gamma^2}{k} + T_0\right) \end{aligned} \tag{7.11}$$

Since the heat loss is mainly downwards through vias, T_0 (i.e. external temperature in convection) can fairly be assumed to be the average temperature of the ends. Therefore, assuming $T_0 = (T_1 + T_2)/2$, $T_n = (T_1 - T_2)/2$ and $T_m = j^2\rho\Gamma^2/k$ (T_m is the maximum temperature rise). *T(x)* can be written as:

$$T(x) = T_0 + T_m\left[1 - \frac{\cosh\left(\frac{x}{\Gamma}\right)}{\cosh\left(\frac{L}{2\Gamma}\right)}\right] + T_n\left[\frac{\sinh\left(\frac{x}{\Gamma}\right)}{\sinh\left(\frac{L}{2\Gamma}\right)}\right] \tag{7.12}$$

One may interpret equation (7.12) in a way that a portion of temperature comes from the external temperature (e.g. offset temperature), another portion of temperature is caused by Joule heating, the rest due to the temperature difference (as well as geometry).

For a simple case where the anode and cathode have them same temperature (T_0), the solution [67, 99] is:

$$T(x) = T_0 + T_m\left[1 - \frac{\cosh\left(\frac{x}{\Gamma}\right)}{\cosh\left(\frac{L}{2\Gamma}\right)}\right] \tag{7.13}$$

To eliminate the thermal parts (i.e. conductivity) and describe the model with electrical elements only, T_m, the maximum temperature rise can be written using Wiedemann–Franz law (i.e. $k\rho = L_o T$ where Lorentz number) as follows:

$$T_m = \frac{j^2\rho\Gamma^2}{k_{Cu}} = \frac{\mathrm{t_{Cu}t_{ILD}}j^2\rho}{\mathrm{k_{ILD}}} = \frac{1}{L_o T_0}\rho^2 j^2 \Gamma^2 \tag{7.14}$$

Γ can be modeled differently depending on the layout topology and wire relative geometrical position. The proposed model is valid regardless of Γ derivation. Based on a common structural model in [67] and using (7.7), the following model is shown to be very accurate for modern layout trend.

$$\Gamma \approx \sqrt{t_{Cu} t_{ILD} \frac{k_{cu}}{k_{ILD}}} \tag{7.15}$$

7.2. Temperature Log Integral

The natural logarithm of temperature is a significant quantity as it appears in many other quantities such mean time to failure. In this section we derive a compact expression for *logT(x)*.

The equations describing the temperature distribution and profile are stated in the previous Sub-section. They were organized in such a manner so that each segment of the expression corresponds to the associated physics. But, for integration, we rewrite these equations in a more convenient form.

Definition 7.2. *Let a, A, B and C be:*

$$a = \frac{1}{\Gamma} \tag{7.16}$$

$$A = -T_m \operatorname{sech}\left(\frac{L}{2\Gamma}\right) \tag{7.17}$$

$$B = T_n \operatorname{csch}\left(\frac{L}{2\Gamma}\right) \tag{7.18}$$

$$C = T_0 + T_m \tag{7.19}$$

Using Definition 7.1 and 7.2, (7.17) can be readily expressed as follows:

$$T(x) = A\cosh(ax) + B\sinh(ax) + C \tag{7.20}$$

Thus, the natural logarithm of temperature profile can be written as follows:

$$\log T(x) = \log(A\cosh(ax) + B\sinh(ax) + C) \tag{7.21}$$

But, taking the integration in of $\log T(x)$, in (7.21), is not straightforward due to complex hyperbolic nature of temperature distribution (i.e. $T(x)$).

Definition 7.3. *Let p and q be zeros of the following quadratic polynomial.*

$$\frac{A+B}{2}t^2 + Ct + \frac{A-B}{2} = 0 \tag{7.22}$$

They satisfy the identity polynomial $\frac{A+B}{2}t^2 + Ct + \frac{A-B}{2} = \frac{A+B}{2}(t-p)(t-q)$ where with plugging $t = e^{ax}$, (7.20) can be expressed as:

$$T(x) = \frac{A+B}{2}e^{ax}(1-pe^{-ax})(1-qe^{-ax}) \tag{7.23}$$

Hence, the natural logarithm of temperature, in (7.21) can be stated as follows:

$$\log|T(x)| = \log\left|\frac{A+B}{2}\right| + ax + \log|1-pe^{-ax}| + \log|1-qe^{-ax}| \tag{7.24}$$

Lemma 7.1. *Given $\alpha, \beta \in \mathbb{R}$ the following integral holds true*

$$\int \log|1-\beta e^{-\alpha x}|\,dx = \frac{1}{\alpha}\mathrm{Re}\{\mathrm{Li}_2(\beta e^{-\alpha x})\} + \text{constant.} \tag{7.25}$$

Proof. In order to prove (7.25), a special function called *dilogarithm* is needed. It is denoted by Li_2 and defined by

$$\mathrm{Li}_2(z) = -\int_0^z \frac{\log(1-t)}{t}dt = -\int_0^1 \frac{\log(1-zu)}{u}du\,, z \in \mathbb{C}\setminus[1,\infty). \tag{7.26}$$

Here, the first integral is taken along the line segment joining 0 and z. The equivalence of two integrals can be shown by the substitution $t = zu$. So $\mathrm{Li}_2(z)$ is not differentiable along the branch cut $[1,\infty)$. On the other hand, its real part behaves much better since

$$\mathrm{Re}\{\mathrm{Li}_2(z)\} = -\int_0^1 \frac{\log|1-zu|}{u}du \tag{7.27}$$

Performing complex analysis confirms that both sides of (7.27), considered as a function of real variables x and y (with $z = x + iy$), extends to a smooth on all of $\mathbb{R}^2 \setminus \{(1,0)\}$. Thus, for any $0 < a < b$, (7.26) yields:

$$\begin{aligned} -\int_a^b \frac{\log|1-zu|}{u}du &= -\int_0^b \frac{\log|1-zu|}{u}du - \left(-\int_0^a \frac{\log|1-zu|}{u}du\right) \\ &= -\int_0^1 \frac{\log|1-bzv|}{v}dv - \left(-\int_0^1 \frac{\log|1-azw|}{w}dw\right) \\ &= \mathrm{Re}\{\mathrm{Li}_2(bz)\} - \mathrm{Re}\{\mathrm{Li}_2(az)\} \end{aligned} \tag{7.28}$$

Here, we utilize the substitution $u = bv$ and $u = aw$ for respective terms. Using the substitution $u = e^{-\alpha}$, the following expression can be obtained:

$$\int \log|1-\beta e^{-\alpha x}|dx = -\frac{1}{\alpha}\int \frac{\log|1-\beta u|}{u}du = \frac{1}{\alpha}\mathrm{Re}\{\mathrm{Li}_2(\beta e^{-\alpha x})\} + \text{constant.} \quad \blacksquare \tag{7.29}$$

Using Lemma 7.1, we can write the integral of (7.24) as follows:

$$\begin{aligned} \int \log T(x)dx = x\log\left|\frac{A+B}{2}\right| + \frac{ax^2}{2} + \frac{1}{a}\mathrm{Re}\{\mathrm{Li}_2(pe^{-ax})\} + \frac{1}{a}\mathrm{Re}\{\mathrm{Li}_2(qe^{-ax})\} \\ + \text{constant} \end{aligned} \tag{7.30}$$

Thus, the definite integral of natural logarithm of temperature along a given wire ($-L/2 < x < L/2$) is:

$$\begin{aligned} \int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx = \\ = \log\left|\frac{A+B}{2}\right|L + \frac{1}{a}\mathrm{Re}\left\{\mathrm{Li}_2(pe^{-\frac{aL}{2}}) - \mathrm{Li}_2(pe^{+\frac{aL}{2}})\right\} \\ + \frac{1}{a}\mathrm{Re}\left\{\mathrm{Li}_2(qe^{-\frac{aL}{2}}) - \mathrm{Li}_2(qe^{+\frac{aL}{2}})\right\} \end{aligned} \tag{7.31}$$

7.3. Compact Temperature Log Integral

While (7.31) holds true for any given values of A, B, C and a, we can take advantage of the numerical facts regarding values in (7.12) in thermal context to perform a clever compaction.

Because T_m and $\frac{L}{2\Gamma}$ are both positive, A is negative. A freedom on choosing x direction allows us to pick end points so that $T_1 < T_2$ and therefore $T_n < 0$. It results in B negative. Also C is clearly positive.

In addition, considering the behavior of functions $\operatorname{sech}\left(\frac{L}{2\Gamma}\right)$ and $\operatorname{csch}\left(\frac{L}{2\Gamma}\right)$, it is not difficult to see that $|A| < |C|$ and $|B| < |C|$. Essentially, considering the range of a chip operating temperature (i.e.$T_n = \frac{T_1 - T_2}{2} \ll T_0 = \frac{T_1 + T_2}{2}$) (300K) and interconnect dimensions (i.e. L and Γ) (microns), it can be seen that $|A| \ll |C|$ and $|B| \ll |C|$.

These insights allow us to benefit from some numerical properties and identities. In particular, as p and q are zeros of the quadratic polynomial $\frac{A+B}{2}t^2 + Ct + \frac{A-B}{2} = 0$, without loss of generality, we can assume p and q to be:

$$p = \frac{-C + \sqrt{C^2 - A^2 + B^2}}{A + B} \tag{7.32}$$

$$q = \frac{-C - \sqrt{C^2 - A^2 + B^2}}{A + B} \tag{7.33}$$

According to the numerical facts mentioned above, we conclude that $|p| < 1$ and $|q| > 1$ (essentially $|p| \ll 1$ and $|q| \gg 1$). Consequently, we conclude that $|pe^{-aL}| < 1$ and $|qe^{-aL}| > 1$ (note that we defined $a = \frac{1}{\Gamma}$).

Throughout our numerical discussion above, we do not lose any generality. In other words, in the context of thermal analysis of VLSI chips, these numerical findings are independent of values and indeed are enforced by the context of the problem (e.g. Temperatures have positive values). In the remaining, we use these findings along with some mathematical properties to eliminate the *dilogarithm* functions and lastly compact the final result.

In contrast to its complexity, *dilogarithm* has nice properties that enable us to compute its value efficiently.

Property 1. *For* $|z| < 1$ *the following series converges absolutely*

$$\mathrm{Li}_2(z) = \sum_{n=1}^{\infty} \frac{z^n}{n^2} \tag{7.34}$$

Thus, it is no more complicated than computing the value of $-\log(1-z) = \sum_{n=1}^{\infty} \frac{z^n}{n}$. To handle the case where $|z| > 1$, we use the following transformation identity.

Identity 1. *A reflection property*

$$\mathrm{Li}_2(\frac{1}{z}) = -\mathrm{Li}_2(z) - \frac{\pi^2}{6} - \frac{1}{2}\log^2(-z) \tag{7.35}$$

Using Property 1 and Identity 1, the following expression can be derived:

$$\mathrm{Li}_2(z) = \begin{cases} \sum_{n=1}^{\infty} \frac{z^n}{n^2} & , \quad |z| < 1 \\ -\sum_{n=1}^{\infty} \frac{1}{z^n n^2} - \frac{\pi^2}{6} - \frac{1}{2}\log^2(-z), & \quad |z| \geq 1 \end{cases} \tag{7.36}$$

Considering the fact that the problem is solved in the context of thermal analysis in VLSI chips (i.e. large $|z|$), convergence analysis shows that the property in (7.36) can be further simplified as follows:

$$\mathrm{Li}_2(z) = \begin{cases} z & , \quad |z| < 1 \\ -\frac{1}{z} - \frac{\pi^2}{6} - \frac{1}{2}\log^2(-z), & |z| \geq 1 \end{cases} \tag{7.37}$$

Therefore, (7.37) can be written as:

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx$$

$$= \log\left|\frac{A+B}{2}\right| L + \frac{1}{\alpha}\mathrm{Re}\left\{pe^{-\frac{aL}{2}} - pe^{-\frac{aL}{2}}\right\} \tag{7.38}$$

$$+ \frac{1}{\alpha}\mathrm{Re}\left\{-\frac{e^{+\frac{aL}{2}}}{q} - \frac{1}{2}\log^2(-qe^{-\frac{aL}{2}}) + \frac{e^{-\frac{aL}{2}}}{q} + \frac{1}{2}\log^2(-qe^{\frac{aL}{2}})\right\}$$

Further simplification yields:

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx$$

$$= \log\left|\frac{A+B}{2}\right| L - \frac{2}{a}\sinh\left(\frac{aL}{2}\right)(p + q^{-1}) \tag{7.39}$$

$$+ \frac{1}{2a}\mathrm{Re}\left\{\log^2(-qe^{\frac{aL}{2}}) - \log^2(-qe^{-\frac{aL}{2}})\right\}$$

Thus, (7.39) can be written as:

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx = \log\left|\frac{A+B}{2}\right| L - \frac{2}{a}\sinh\left(\frac{aL}{2}\right)(p + q^{-1}) + \log|q|\, L \tag{7.40}$$

Plugging p and q from (7.32) and (7.31) into (7.40) yields the following expression:

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx$$

$$= \log\left|\frac{A+B}{2}\right| L - \frac{2}{a}\sinh\left(\frac{aL}{2}\right)\left(\frac{-2A}{C+\sqrt{C^2-A^2+B^2}}\right) \tag{7.41}$$

$$+ \log\left|\frac{-C-\sqrt{C^2-A^2+B^2}}{A+B}\right| L$$

As it was shown before, $|A| \ll |C|$ and $|B| \ll |C|$, therefore q and $p+q^{-1}$can be fairly substituted with $-2C/(A+B)$ and also A/C resulting in the following expression:

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx = (\log C)L + \frac{2}{a}\sinh\left(\frac{aL}{2}\right)\left(\frac{A}{C}\right) \tag{7.42}$$

Plugging A, B, C and a into Eq. (70) yields the following compact expression

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx = \log(T_0+T_m)\, L - 2\Gamma\tanh\left(\frac{L}{2\Gamma}\right)\left(\frac{T_m}{T_0+T_m}\right) \tag{7.43}$$

Also, since $T_0 \gg T_m$

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \log T(x)dx = \log(T_0+T_m)\, L - 2\Gamma\tanh\left(\frac{L}{2\Gamma}\right)\left(\frac{T_m}{T_0}\right) \tag{7.44}$$

Where $T_m = \frac{j^2\rho\Gamma^2}{k}$ is the maximum temperature.

7.4. The Exact Model

As it was mentioned in Chapter 2, to obtain another relationship between the stresses at line ends with temperature, we need to study the atom conservation under temperature effect stated as [39]. In this section, we present further details on the derivations of the extract form of the models in Chapter 3.

$$\iiint \Delta C \mathrm{d}v = -\frac{C_0}{B} HW \int_{-\frac{L}{2}}^{+\frac{L}{2}} \sigma \mathrm{d}x = 0 \tag{7.45}$$

where $C_0$is the initial concentration, $V = HWL$ is the wire volume.

Plugging (3.2) into (7.45), yields

$$\int_{-\frac{L}{2}}^{+\frac{L}{2}} \sigma \mathrm{d}x = \frac{\sigma_- + \sigma_+}{2} L - \frac{Q}{\Omega} \frac{\ln T_+ + \ln T_-}{2} L + \frac{Q}{\Omega} \int_{-\frac{L}{2}}^{+\frac{L}{2}} \ln T(x)\, \mathrm{d}x = 0 \tag{7.46}$$

Since temperature at ends (typically ~100°C) is much higher than the temperature rise (usually several degrees), i.e. $T_m \ll T_0$, plugging (7.44) into (7.46) yields to an important relationship as follows:

$$\frac{\sigma_+ + \sigma_-}{2} L + \frac{Q}{\Omega} \frac{T_m T_0}{T_+ T_-} L \left(1 - \frac{2\Gamma}{\mathrm{L}} \tanh\left(\frac{L}{2\Gamma}\right)\right) = 0 \tag{7.47}$$

If in a structure, the thermal characteristic length happens to be much smaller than the length of a wire (i.e. $\Gamma \ll \mathrm{L}$), one may use the following approximation instead:

$$\frac{\sigma_+ + \sigma_-}{2} + \frac{Q}{\Omega} \frac{T_m}{T_0} = 0 \tag{7.48}$$

Chapter 8

Conclusions and Future Work

8.1. Reliability – Significance

Our everyday lives rely heavily on our electronic gadgets and devices. We expect them to function dependably and often last long. For sensitive applications such as medical devices, autonomous vehicles and space crafts, reliability or lifetime is often crucial and nonnegotiable. Soon with the appearance of Internet of Things, we will constantly be interacting with many tiny intelligent devices that are supposed to function reliability.

Throughout the history of microelectronics, improvements in IC manufacturing design and technology, guided by the predictions and guidelines from Moore's law, have resulted in an exponential increase in computing power per unit area. This arises from the individual transistor speedup and size shrinkage, allowing more transistors to be packed on a chip. Alongside with transistor shrinkage, the size of the interconnects also shrinks to be able to accommodate and connect the tightly packed transistors. However, unlike the trend in transistor performance, which shows an improvement with technology advancement, the interconnect network shows performance degradation.

The limited interconnect performance is unable to sustain the performance improvement in transistors which consequently creates a large stress in the interconnects. Such large electrical load is often quantified by the current density. Shrinking sizes and swelling requirements result in large current density which can cause wire wear-out and material degradation due to **mass transport** controlled by a complex electro-thermo-mechanical process which ultimately affect the IC reliability or its capability to function properly over the lifetime of the product. The effect of mass transport usually manifests itself first as resistance change, void or hillocks formation and over time may result in shorts or opens.

8.2. Reliability – Approaches

Physics and Material Science: In this category, reliability concerns are often mitigated by focusing on introducing new materials, alloys or improving the capability of existing materials and processing conditions (e.g. adding liner, cap and seed layers). Therefore, due to constraints in the experimental approaches such as thermal budget and manufacturing, it would not be surprising to see newer dramatic changes such as introduction of new material or airgaps [3]. Nevertheless, since the cost and scale of experimental approaches cannot mimic large circuits as a whole, thus true reliability lifespan of interconnect nets cannot be observed using such approaches. Also, based on manufacturer experiences such highly expensive approaches on alternative materials is unlikely to provide long term solutions for continued scaling.

Computer Engineering: As alternative solutions, the existing methods for reliability assessment are currently being adjusted hoping to explain and model newly emerging reliability problems [114, 115, 116, 117]. The latter approach is often criticized for being inaccurate due to over simplification or the lack of including true underlying physics. While

tuning parameters and modifying existing models may offer short-term benefits, it also appears unlikely that merely parameter refinements will produce a clear path or a holistic solution for scaling that is being sought [3].

Our Approach: As a result, we highlight in this thesis that a productive approach to assessing and mitigating interconnect reliability concerns lies with shifting the focus of investigation from material explorations or existing model modifications towards understanding the underlying causes of material degradation (Physics and Material Science) and the impact of aging mechanisms on circuit functionality, which has received relatively little attention up to the present (Computer Engineering).

8.3. Models

We examine "*whether the existing models—which are developed based on limited experiments and for specific technologies under certain circumstances—are capable to be adjusted so that they can capture ever-emerging challenges imposed by aggressive scaling*?".

This thesis demonstrates that in advanced technologies, merely adjusting the parameters in existing models leads to intolerable inaccuracy. In some technologies, new challenging physical phenomena (such as electron scattering in sub 10nm) may arise and contribute to overall aging through completely new mechanisms which are not captured in the existing models. Indeed, dealing with the ever-ongoing challenges imposed by scaling (e.g. thermomigration and electron scattering), requires revisiting physics and devising new models by including new aging processes rather than tweaking the existing ones.

Classical Models: **Lifetime Assessment**: A key information in the context of reliability is the device's mean time to failure or lifetime. Black's empirical model has been widely used as

a metric for the lifetime of interconnects. **Mortality Check**: Another critical information is to determine whether a wire is immortal or not. The most commonly used model for immortality checking was developed by Blech. **Lifespan Analysis (transient defect evolution)**: Korhonen developed a new model for transient evolution of voids. This model has been widely accepted by the research community. The transient defect evolution during the lifespan due to aging is also an important information for a comprehensive reliability assessment. Korhonen developed a model for transient evolution of voids which has been widely used in the research community.

Classical Models Limitations: **Single Segment**: Classical models for end-to-end wires cannot be employed for complex nets. We investigated the mass transport in multi-segment structures by studying stress evolution across the branches in a net. A new set of models are proposed which can accommodate complex interconnect networks with multiple nodes and branches. **Temperature Agnosia**: The existing models are temperature agnostic as they do not take temperature effects into account as an individual aging factor. However, for modern technologies heating in general and its repercussions have been a life-threatening to interconnect reliability**.** Using temperature agnostic models in verification flow is shown to be dangerous in terms of reliability misevaluation or unnecessary overdesign. Temperature not only affects electromigration and stress migration but also affects the aging directly through thermomigration. We discuss thermal effects on reliability of interconnects and propose new models which take temperature effects correctly into account through thermomigration. **Poor Integrability**: In common verification methodologies, reliability analysis usually takes the very last stage of physical signoff checks. Also, as it was discussed before, examining material migration induced reliability of interconnect fundamentally requires multi-physics analyses. The classical models and their extended versions are based on hydrostatic stress analysis. The

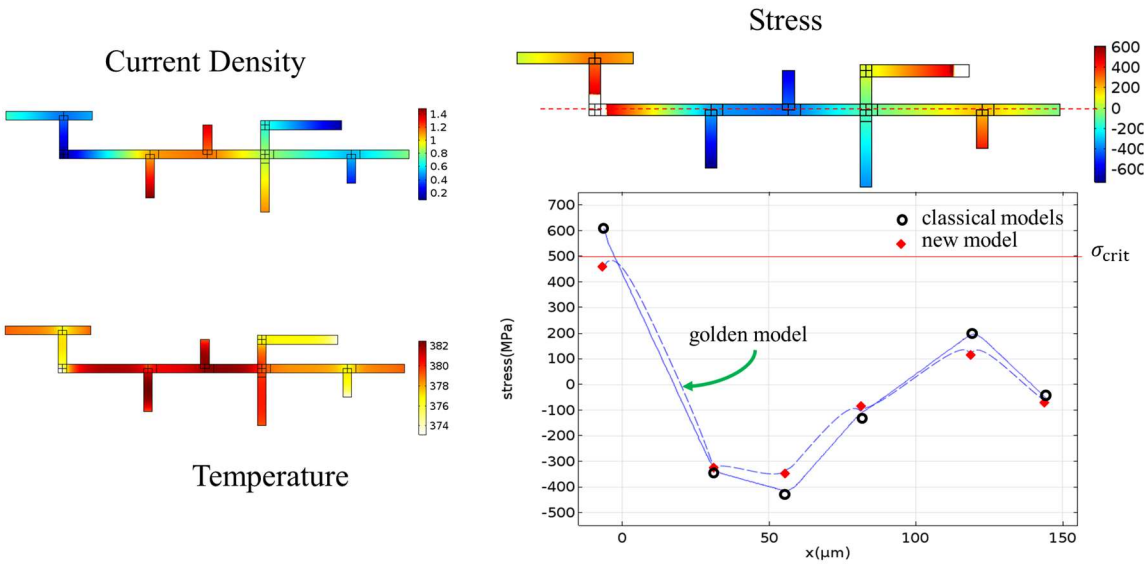


Figure 8.1: Demonstrating disparity between classical models and new model versus the golden model (experiments).

multi-physical nature of mass transport phenomenon (e.g. dealing with non-electrical or mechanical factors such as hydrostatic stress) makes this stage of verification hard to integrate with other signoff steps (performance, delay, power). Due to such poor integrability, many redundant iterations between various verification steps might occur. For example, a naïve change towards EM improvement may affect other critical factor such as timing. Indeed, lack of a homogenous methodology results in unwelcome cost and time. We observed an interesting relationship between non-electrical factors such as stress and temperature with electrical ones. We propose a novel mapping from hydrostatic stress and temperature to voltage. Then, a new voltage-based formalism is developed to translate non-electrical factors to voltage and can be universally used among different stages of verification such as performance, delay and power. This makes the mass transport analysis desirably integrated into common methodologies.

Fig. 8.1, as a big picture of this thesis, it shows that the explicit use of classical models for advanced technologies may result in significantly erroneous reliability misevaluation. While

there have been some works addressing some of these limitations, this thesis delivers a comprehensive research on mass transport induced aging in interconnect networks considering all electro-thermo-mechanical factors. This research contains a profound amount of experiments, observations, mathematical models based on underlying aging physics, numerical analyses and a great body of discussion.

8.4. Concluding Findings

Complex Net with Multi-segment Extension: We show that classical models (i.e. Black, Blech and Korhonen's models) for end-to-end wires cannot be employed for complex nets. We extend these models to complex structures using the principle of atom conservations in an encapsulated body of connected interconnects which desirably replaces incorrect utilization of end-to-end models. The model proposed computes the hydrostatic stress distribution and captures the electrical and non-electrical effects of all segments connected in a net. This model is also capable of capturing the effect of passive extensions.

Temperature is a big culprit for aging: We demonstrate that simplistic combination of thermal models and temperature-agnostic electromigration models without considering their true correlation no longer provide correct reliability assessment for wires manufactured in advanced technologies. We propose a compact aging model that captures the impact of Joule heating on material migration via thermomigration. We investigate the stress development considering thermomigration, an aging process induced by Joule heating. We show that neglecting thermal effects during reliability assessment may lead to wrong evaluation for wires manufactured in modern technologies. We propose a new criterion for checking immortality of wires under any thermal, electrical and mechanical conditions. We demonstrate that many

wires considered mortal based on Blech criterion may never experience aging problems during the product lifetime and many Blech-immortal wires may become damaged and cause catastrophic failures. We also investigate in detail various temperature profiles. We show that depending on the steady state profile of temperature, the voiding and hillock potential appearance will be affected, and therefore temperature-agnostic Blech based method may not be trusted. The new model confirms that thermomigration usually (i.e. for the thermal profile of ∩) tends to aggravate compressive stress and potentially exacerbate the risk of extrusion or shorts. On the other hand, thermomigration mitigates tensile stress and possibly alleviates the risk of voiding or opens. In general cases, when the temperature gradients are negative towards the cathode, such gradients alleviate the tensile and compressive stresses. On the other hand, positive temperature gradients towards the cathode, aggravate the tensile and compressive stress. Our models are validated by numerous COMSOL-based experiments. Intuitively, increasing temperature usually mitigates shrinkage and intensifies inflation. This may cause serious temperature effects (i.e. various stress aggravation or alleviation) that can be missed by the existing models. Thermomigration interacts with electromigration and stress migration and may result in (1) asymmetric stress distribution, (2) early hillock formation (shorter lifetime), (3) late voiding (longer lifetime), (4) non-end failures. The proposed model sexplain many experimental observations that may have been inexplicable before. Due to the complex mutual dependencies, thermal and other aging factors are often assessed independently without considering their true physics-based correlations. Using the underlying physics of stress evolution, we develop a new analytical transient model and a compact steady state model for reliability assessment that accurately captures electrical, thermal and mechanical aspects. Our experimental results indicate that ignoring temperature or not modeling it through

thermomigration may lead to incorrect conclusions regarding mortality and lifetime. The proposed models can be used to determine: (1) transient analysis of aging of wires; (2) stress analysis of signal and power interconnect networks; (3) accurate conditions for voiding and extrusion; (4) new criteria for designers and CAD tools in terms of current density and lengths.

Improving Integrability: We show how designers can use the circuit nodal analysis to assess the reliability of the circuit without dealing with non-electrical concepts such as mechanical stress and physics-based models. Essentially, we offer fast models for reliability assessment which abstract away the complex physics aspects of electromigration and help designers to perform EM analysis of the entire circuit merely based on the electrical nodal information.

RAIN: Ultimately, we develop a computer-aided design tool, RAIN (Reliability Assessment of Interconnect Networks), based on the proposed models and capable of assessing reliability of industry standard complex multi-layer, multi-segment interconnect networks (e.g. IBM Benchmark with 4.1 million nodes). The tool is very efficient and accurate and can be run using desktop or laptop computers. The languages used for building this tool include but are not limited to C, C++, Python, Perl, Matlab, Mathematica, JavaScript and R.

RAIN can be readily integrated into other verification signoffs phases such as performance, timing and power analyses. RAIN takes as inputs: (1) interconnect design, (2) technology specifications, (3) initial stress and temperature, (4) IR drop and lifetime requirements. It analyzes and assesses reliability and delivery requirements of all nets, and provides a report on voltage limitations, thermal violations and expected lifetime. It is validated on a wide spectrum of experimental results performed on various industry benchmarks.

We show that first the interconnect network must be decomposed through extracting the connected component and then based on geometrical and electrical information of component perform reliability analysis. We show that two hazardous situations may occur: (1) in some cases, the existing models may wrongly scrutinize reliability in unfailing parts and consequently impose unnecessary design tightening and (2) in some other cases, the models may underestimate serious reliability problems causing unpredicted behaviors or catastrophic failures to occur. The existing models for reliability evaluation are usually pessimistic in case of interconnect voiding and optimistic when extrusion occurs. Time-consuming and not converging reliability assessments as well as undesired chip behaviors are the common expensive outcome of such models. Fig. 6.1 shows the interface of the tool we developed for reliability assessment of large interconnect grids under thremo-electro-mechanical stress.

8.5. Future Directions

The presented research and associated development, such as RAIN, provide a framework for future research in various directions which are briefly listed here.

(1) Scaling may consequences in some new aging mechanisms which have not been observed in current technologies but speculated about the future such as aging due to fatigue in extremely small lines such as those which carry bidirectional currents for a long time. Exploring other aging mechanisms may open new horizons in the context of reliability analysis.

(2) Stepping to replace copper interconnects has already initiated and expected to continue in the long term (e.g. cobalt wire or carbon nanotubes have been investigated as viable options). While some of these substituting technologies may not suffer from EM in a conventional sense,

it seems that due to the nature of microelectronics performance requirements, thermally-induced aging has been a persistent common reliability issue. Therefore, incorporating the associated underlying physics into the presented model can be a possible extension for future technologies.

(3) A sensitivity level can be desirably added to RAIN so that designer can enable and disable some detailed and in-depth analyses (e.g. current crowding in corners and lines with angels). Also, it is not difficult yet convenient to add a feature to RAIN to perform fractional analyses where only specific segments are required to be analyzed.

(4) We showed, beside the traditional intangible metrics such as critical stress, other key components in developing a lifetime model are atomic divergence and critical voltage. A possible direction is to devise more enhanced lifetime models based on the presented notations.

(5) While RAIN never experienced performance limitations for analyzing even extremely large interconnect designs, further optimization in transient analysis might be possible.

(6) RAIN can be efficiently utilized for extracting insights and ultimately developing aging mitigation techniques. Indeed, the reliability violation reports generated by RAIN provide valuable perceptions that can lead to developing aging prevention schemes, redundancy-aware design practices and optimal repair strategies.

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