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Electronic Properties and Device Applications of van-der-Waals Thin Films

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Jacqueline de Dios Renteria

March 2014

Dissertation Committee:
Dr. Alexander A. Balandin, Chairperson
Dr. Roger K. Lake
Dr. Alexander G. Khitun

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2014

The Dissertation of Jacqueline de Dios Renteria is approved:

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Committee Chairperson

University of California, Riverside

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Dedicated

To

My Family

ABSTRACT OF THE DISSERTATION

Electronic and Optoelectronic Properties and Applications of Van der Waals Thin Films

by

Jacqueline de Dios Renteria

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, March 2014
Dr. Alexander A. Balandin, Chairperson

Successful exfoliation of graphene and discoveries of its unique electrical and thermal properties have motivated searches for other quasi two-dimensional (2D) materials with interesting properties. The layered *van der Waals* materials can be cleaved mechanically or exfoliated chemically by breaking the relatively weak bonding between the layers. In this dissertation research I addressed a special group of inorganic van der Waals materials – layered transition metal dichalcogenides (MX_2, where M=Mo, W, Nb, Ta or Ti and X=S, Se or Te). The focus of the investigation was electronic properties of thin films of $TaSe_2$ and MoS_2 and their device applications. In the first part of the dissertation, I describe the fabrication and performance of all-metallic three-terminal devices with the $TaSe_2$ thin-film conducting channel. The layers of 2H-$TaSe_2$ were exfoliated mechanically from single crystals grown by the chemical vapor transport method. It was established that devices with nanometer-scale thickness channels exhibited strongly non-linear current-voltage characteristics, unusual optical response, and electrical gating at room temperature. It was found that the drain-source current in thin-film 2H-$TaSe_2$–Ti/Au devices reproducibly

shows an abrupt transition from a highly resistive to a conductive state, with the threshold tunable via the gate voltage. Such current-voltage characteristics can be used, in principle, for implementing radiation-hard all-metallic logic circuits. In the second part of the dissertation, I describe the fabrication, electrical testing and measurements of the low-frequency 1/*f* noise in three-terminal devices with the MoS_2 thin-film channel (*f* is the frequency). Analysis of the experimental data allowed us to distinguish channel and contact noise contributions for both as fabricated and aged devices. The noise characteristics of MoS_2–Ti/Au devices are in agreement with the McWhorter model description. The latter is contrary to what is observed in graphene devices, where the noise spectral density does not follow the carrier number fluctuation model. The trap density extracted from the noise measurements is on the order of 2×10^{19} $eV^{-1}cm^{-3}$ and 2.5×10^{20} $eV^{-1}cm^{-3}$ for as fabricated and aged samples, respectively. These values are of the same order of magnitude as those in high-k MOSFETS. These results of this dissertation research may lead to new applications of van der Waals materials.

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Chapter 1

Introduction

In order to investigate the characteristics, performance metrics, and to understand the physical phenomenon behind the electronic behavior of field-effect transistors with novel channel materials, such as thin films of the transition metal dichalcogenide tantalum diselenide ($TaSe_2$), device fabrication and characterization were undertaken in this work. In Sec. 1.1, a brief introduction to the motivation behind radiation-hard materials for use in electronics and the device demonstrations achieved to meet the demand for radiation-hardness. In Sec. 1.2, an introduction to the proposed materials and material structure to complement silicon based devices. In Sec. 1.3, the need for low-noise devices is reviewed. In Sec. 1.4, the issues and challenges associated with device fabrication and characterization of FETs with $TaSe_2$ thin film channels is discussed. Finally, in Sec. 1.5, the outline of this dissertation is presented.

1.1 Radiation-hard All-metallic Logic Circuits

As motivation, scientists and engineers are continuing efforts to increase radiation hardness of electronic components. Sources of damaging ionizing radiation come from cosmic rays,

x-rays, gamma rays and even alpha particle emission from radioactive contaminants of chip packaging materials.[2] For this reason, implementation of transistors, diodes and other circuit elements with metallic materials rather than semiconductors would offer a number of potential benefits including inherent radiation hardness and low cost. There have been a number of proposals and attempts to implement all-metallic switches and circuits ranging from metal dot single electron transistors[3-5] to metallic carbon nanotube (CNT) devices,[6-8] metallic nanowire transistors[9] and all-metallic spin transistors.[10,11]

1.2 Van der Waals Materials in FETs

To date the most successful demonstration of an electrically-gated metallic channel device is a graphene field-effect transistor (FET) type device.[12-14] Graphene devices have high mobility[13,14] high saturation velocity,[15] low flicker noise[16,17] and can be gated at room temperature (RT).[12-14] The V-shaped transconductance characteristics of graphene devices and their low $1/f$ noise level offer increased functionalities for signal processing (f is the frequency).[17-19] However, the absence of a band gap, the high carrier concentration, and the high mobility in graphene result in substantial leakage currents. In addition, graphene-based devices cannot be switched off, and the single-atom thickness of graphene leaves it susceptible to radiation damage.[20]

1.3 Low-Frequency Noise

Low-frequency electronic noise with spectral density that depends inversely on the frequency *f* is a ubiquitous phenomenon, which hampers operation of many devices and circuits. A high level of 1/*f* noise can become an impediment for practical applications of any new material system. In this research characteristic features of 1/*f* noise in $TaSe_2$ and MoS_2 devices are reviewed and investigated. Their implications for prospective applications of $TaSe_2$ and MoS_2 in transistors, diodes, and other electronic devices are discussed. Since device downscaling results in a higher noise spectral density this research helps to elucidate noise mechanisms from which methods can be developed for noise reduction.

1.4 Outline of the Dissertation

This dissertation is divided into the following chapters:

- Chapter 2 (page 5): This chapter offers an introduction to van der Waals materials with a focus on a specific class of van der Waals materials called transition metal dichalcogenides. The motivations behind this material class' research and the decision to focus on $TaSe_2$ and MoS_2 thin films.
- Chapter 3 (page 17): This chapter details the thermal characterization of $TaSe_2$ material from bulk to thin films 45 nm thick.
- Chapter 4 (page 23): This chapter presents the results of $TaSe_2$ device fabrication and the electrical and optical characterizations performed to determine device metrics and the practical applications for such a transistor. Surprising

optoelectronic results are presented with a behavior observed with and without light illumination that is contrary to a typical photoresistor.

- Chapter 5 (page 40): This chapter presents possible logic gates with $TaSe_2$ FETs.
- Chapter 6 (page 43): This chapter presents the results of MoS_2 device fabrication and the output characteristics to understand device performance and possible use in practical applications.
- Chapter 7 (page 63): A summary of the dissertation is presented here.

Chapter 2

2.1 Van der Waals Materials

These materials are layered with strong in-plane bonds that could be covalent or ionic, but with weak coupled van der Waals bonds between layers. The name originates from Dutch scientist Johannes Diderik van der Waals (1837-1923) who is known for his equation of state contribution and work on intermolecular forces, which awarded him the Nobel Prize in Physics in 1910. These van der Waals materials are also called 2-dimensional (2D) materials, because of the dimensionality of the flat layers that make up their structure. They include materials such as graphite, 2D dichalcogenide Molybdenum Disulfide (MoS_2), and the 2D *metallic* dichalcogenide Tantalum Diselenide ($TaSe_2$) that are explored in detail in this dissertation. They were originally thought to not exist or be unstable in a few-layer state. Theoretically, a few-layer state would become thermodynamically unstable and the material would decompose when separated into layers that were under a certain thickness. However, discovery of graphene through the use of a mechanical exfoliation technique in 2004 by A. Geim and K. Novoselov sparked interest in this and later other 2D materials once extraordinary properties of electronic and phononic properties were revealed. These so called van der Waals materials is the basis of this dissertation.

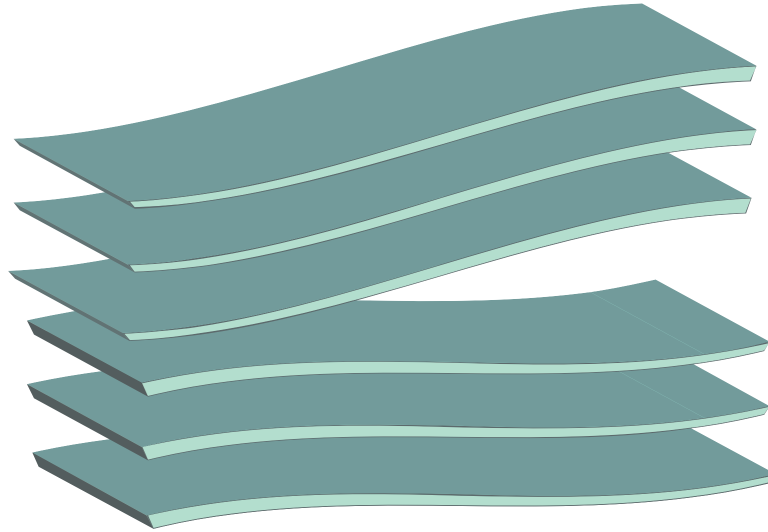


Figure 1: Illustration of layered structure of van der Waals material.

2.2 Transition Metal Dichalcogenides

Layered compounds of transition metal dichalcogenides, an interesting subgroup of inorganic van der Waals materials, arouse much interest due to structural instabilities caused by the two dimensional electronic structure. At low temperatures the crystal periodicity is modulated and the charge density wave (CDW) state is formed. The CDW state is stabilized only by an accompanying a periodic lattice distortion through the electron-phonon interactions, in contrast with a spin density wave phase transition. Therefore the investigation of the lattice vibration, in other words the dynamics of CDW, is very important in the study of the CDW phase transition.[21] The transition metal dichalcogenides VSe_2, $NbSe_2$, TaS_2 and $TaSe_2$ are metallic and show CDW phase transitions.

2.3 Material Synthesis of $TaSe_2$ and Polytypes

$TaSe_2$ is representative of the layered transition metal dichalcogenides, MX_2, where M is a transition metal like Mo, W, Nb, Ta or Ti, and X is a chalcogenide ion being S, Se or Te.[22] This material exists as layers with each layer consisting of a sandwich of Tantalum atoms in between Selenium atoms on either side. The unit cell consists of three atoms at high temperature. Some of these layered transition metal dichalcogenide materials manifest charge density wave (CDW) phenomena in the temperature range from ~100 K to RT. We have reported previously that FETs with $TiTe_2$ channels can show unusual non-linear I-V characteristics.[23] Unlike MoS_2, which is a semiconductor with a bulk band gap energy of E_G = 1.29 eV (1.9 eV for a monolayer),[24] 2H-$TaSe_2$ is a metal (or semi-metal) with no band gap.[25] The crystal structures of $TaSe_2$ contain Ta in a trigonal prismatic coordination within Se-Ta-Se layers. The weak interlayer van der Waals bonding leads to various $TaSe_2$ polytypes, which differ simply in the relative orientations of the layers and their stacking arrangements. In this work, we focus on 2H-$TaSe_2$. As illustrated in Figure 3, the structure of the 2H polytype has a two-layer repeat pattern (AcA BcB); the view down the c-axis clearly shows how the trigonal prismatic units are rotated 60° with respect to each other.[26]

Many transition metal dichalcogenides (TMDCs) are polymorphic and $TaSe_2$ can exist in a considerably larger number of room temperature metastable polymorphs than any of the other TMDCs. Among the various polymorphs, 1T- and 2H- structures are basic. In the 1T- structure (D_{3d}) the metal atoms are octahedrally coordinated by six neighboring chalcogen atoms, and in the 2H- structure (D_{6h}) the metal atoms are located at the center

of a trigonal prism of six chalcogen atoms.[21] The source material of $TaSe_2$ was determined by Raman spectroscopy to be of the 2H-TaSe2 polytype. In 2H-$TaSe_2$ the transition from the undistorted to the incommensurate state occurs at 122 K and the commensurate superlattice of $3a_o * 3a_o * c_o$ is set up at 90 K.[27]

High purity and crystallinity are essential to ensure desirable electron transport characteristics. Thus, the 2H-$TaSe_2$ thin films used in this work were exfoliated mechanically from single crystals grown by the chemical vapor transport (CVT) method. Preparative details and analysis data can be found in a recent report.[28] Representative images of 2H-$TaSe_2$ crystals are shown in Figure 2: (a) Optical microscopy image of metallic gray clusters of crystals and (b) Scanning electron microscopy (SEM) image highlighting an individual 2H-$TaSe_2$ crystal. Lateral dimensions ranged from 200 to 800 μm and thicknesses were typically 5 to 30 μm.

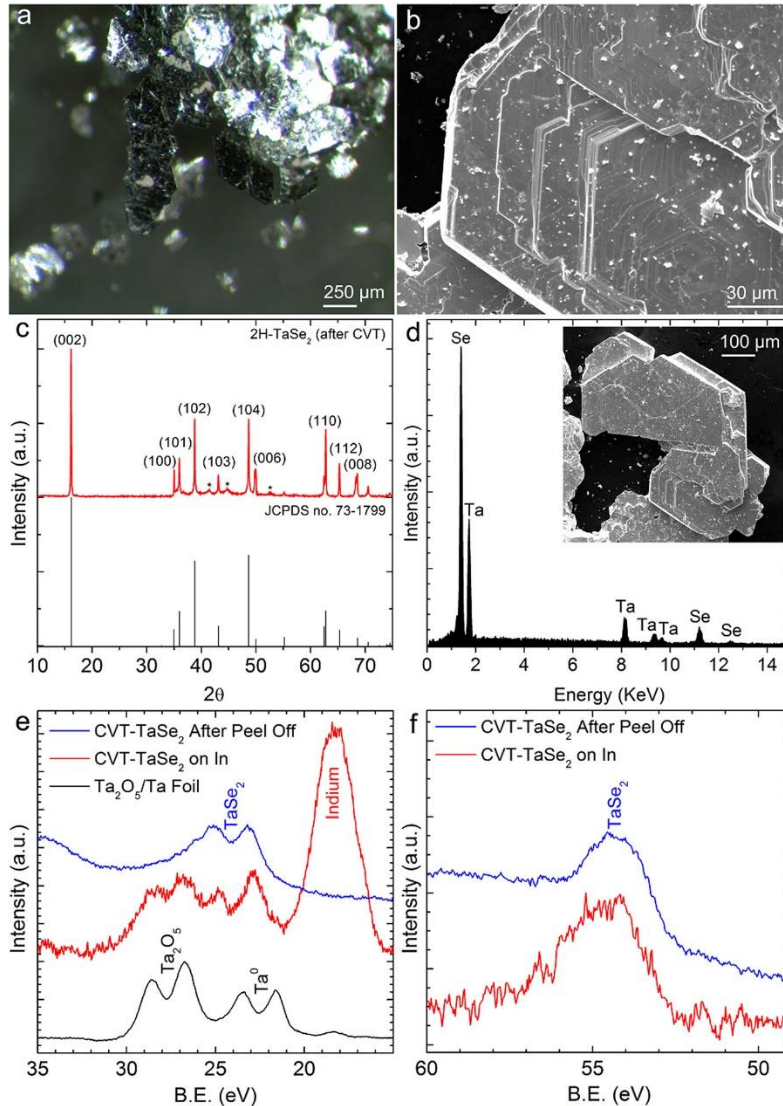


Figure 2: Characterization of 2H-$TaSe_2$ crystals grown by the chemical vapor transport method: (a) Optical microscopy image (scale bar is 250 lm). (b) SEM image (scale bar is 30 lm). (c) Powder X-ray diffraction data. The top red trace shows the pattern from as-grown TaSe2 crystals; the primary component is 2H-$TaSe_2$ (database comparison shown at bottom) with traces of 3R-$TaSe_2$ (marked with *). (d) Energy dispersive X-ray spectroscopy data for a 2H-$TaSe_2$ crystal (SEM (inset), scale bar is 100 lm). (e) XPS spectra showing the Ta 4f photoelectric peaks from 2H-$TaSe_2$ crystals before (red curve) and after (blue curve) peel-off of surface layers. The spectrum of Ta_2O_5 on Ta foil (black curve) is included for reference. (f) XPS spectra showing the Se 3d photoelectric peaks from 2H-$TaSe_2$ crystals before (red curve) and after (blue curve) peel-off of surface layers. Reprinted with permission from Z. Yan, C. Jiang, T. R. Pope, C. F. Tsang, J. L. Stickney, P. Goli, J. Renteria, T. T. Salguero, and A. A. Balandin, *J. Appl. Phys*. **114**, 204301 (2013), © 2013 2014 AIP Publishing LLC.

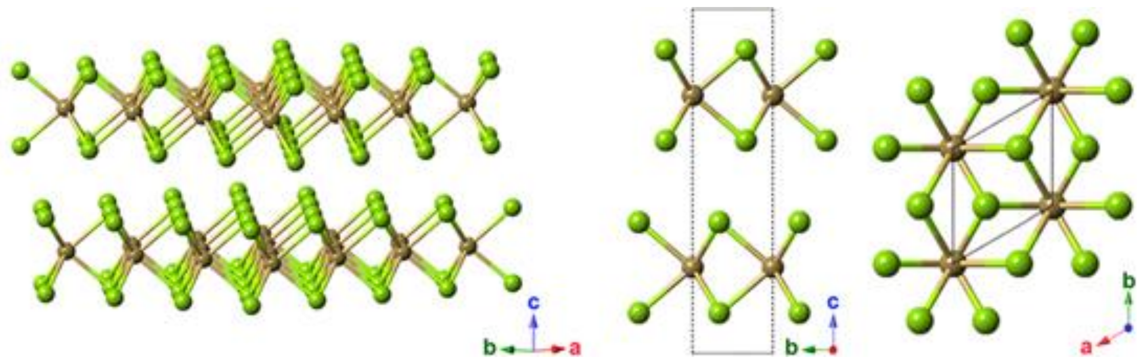


Figure 3: Three views of the 2H-$TaSe_2$ structure (box indicates unit cell). Reprinted with permission from J. Renteria, R. Samnakay, C. Jiang, T. R. Pope, P. Goli, Z. Yan, D. Wickramaratne, T. T. Salguero, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.* **115**, 034305 (2014), © 2014 AIP Publishing LLC.

2.4 $TaSe_2$ Thin Film Preparation

A simple method of producing $TaSe_2$ flakes starts with single crystals of $TaSe_2$. These crystals of 2H-$TaSe_2$ were exfoliated and transferred onto Si/SiO_2 substrates following the standard "graphene-like" approach.[12-14] It was believed that graphene and other single layers of van der Waals materials did not exist in a stable state at a finite temperature. It was not until 2004 that Britain researchers, using this simple technique of micro-mechanical exfoliation with adhesive tape, that the thinnest material from graphite was realized. It is a method used readily now with other van der Waals materials which does not require expensive and sophisticated equipment.

Before using this micro-mechanical exfoliation method, it is important to keep source crystals in a vacuum box and in cool storage to inhibit possible oxidation or contamination. When preparing flakes for device fabrication it is also crucial that they be prepared in a cleanroom environment, again to maintain the quality of any fabricated

devices. The use of disposable gloves and tweezers are recommended to avoid contact and cross-contamination. Figure 4 illustrates the preparation of thin flakes using the micro-mechanical exfoliation method. The preparation starts with a $TaSe_2$ single crystal being placed onto a strip of adhesive tape. It is pressed down gently with a pair of tweezers or another piece of adhesive tape. The source crystal is gently removed and stored back into its vial or container and placed back to its appropriate storage. Then, using multiple pieces of adhesive tape you peel off and "thin" down your van der Waals material. Place the $TaSe_2$ side down onto a clean SiO_2/Si substrate. Apply light and even rubbing with a dry sponge. Finally, lift off the adhesive tape leaving behind flakes of $TaSe_2$ on the substrate. Using optical microscopy you can identify *randomly* sized and *randomly* located mono- to few layer flakes of $TaSe_2$.

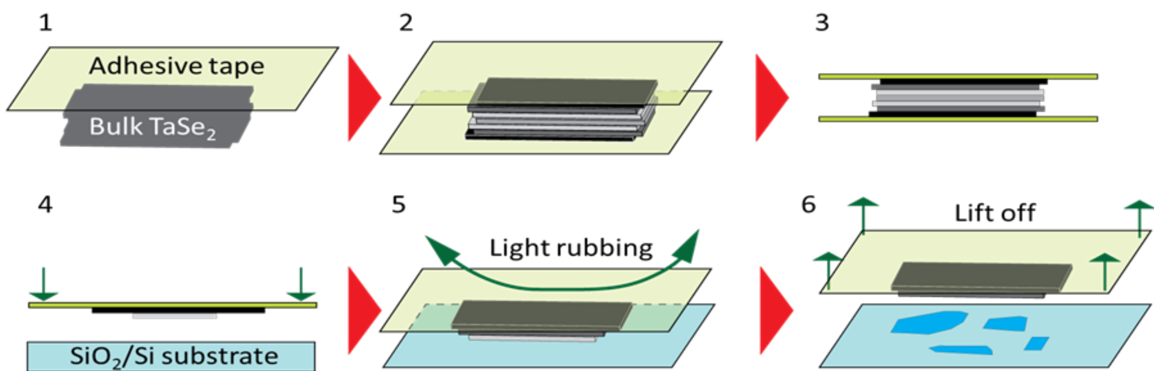


Figure 4: Mechanical exfoliation process from a single crystal. (1) Pull multiple layers off bulk crystal using adhesive tape, (2-3) Use multiple pieces of adhesive tape to "thin" van der Waals material, (4) Place van der Waals layer side down onto SiO_2/Si substrate, (5) Rub lightly and evenly with a dry sponge, (6) Lift off adhesive tape and use optical microscopy to identify randomly sized and randomly located mono- to few layer flakes that remain on SiO_2/Si surface.

2.5 $TaSe_2$ Thin Film Characterization

In order to study properties of the exfoliated material, one should first know exactly how many layers of it are on the sample. There are several ways of counting the layers by using optical microscopy, atomic force microscopy and Raman spectroscopy. Optical microscopy could help to roughly find few-layer graphene, but it cannot tell exactly number. It also gives us an indication on the thickness and therefore the number of layers present in flakes of $TaSe_2$ by using the color of the observed flake. Atomic force microscopy (AFM) can give accurate thickness of our van der Waals (vdW) material, but since its mechanism can only provide relevant thickness of the two interfaces, it is difficult to determine the interface is between substrate and single layer van der Waals material or single layer vdW material between bi-layer one. It is also hard to find the rough location of vdW material under AFM since flakes are relatively small; therefore AFM has a drawback of low efficiency. However, Raman spectroscopy can tell exactly the number of layers and also has high efficiency in characterization.

The thickness H of the films ranged from a few tri-layers to $H \approx 40$ nm. Micro-Raman spectroscopy (Renishaw InVia) was used to verify the crystallinity, polytype and thickness of the flakes after exfoliation. It was performed in a backscattering configuration and $\lambda = 633$ nm excitation laser. The excitation laser power was limited to less than 0.5 mW to avoid local heating. Figure 5 shows informative bands at 207 – 210 cm^{-1} (E^1_{2g}) and 233 – 235 cm^{-1} (A_{1g}), consistent with previous reports for bulk and thin film 2H-$TaSe_2$.[28-30] The band at 300 cm^{-1} corresponds to the Si/SiO_2 substrate.

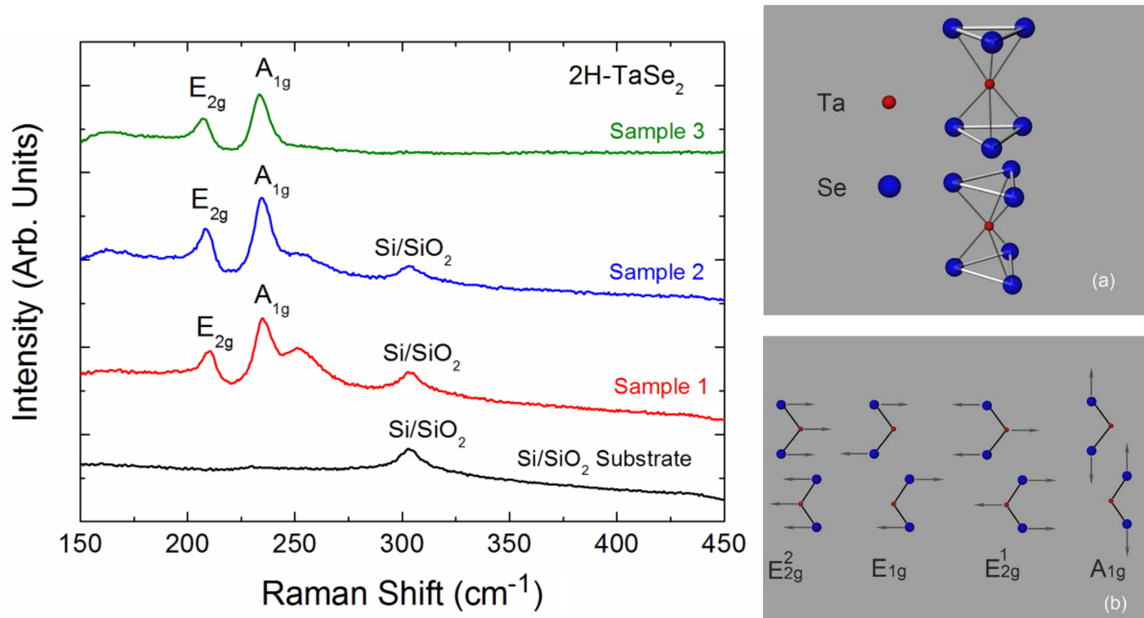


Figure 5: Raman spectra of 2H-$TaSe_2$ exfoliated films on Si/SiO_2 substrate. The bands at 207 – 210 cm^{-1} and 233 – 235 cm^{-1} correspond to E^1_{2g} and A_{1g}, respectively. Samples were excited by the 633 nm laser in a backscattering configuration. Reprinted with permission from J. Renteria, R. Samnakay, C. Jiang, T. R. Pope, P. Goli, Z. Yan, D. Wickramaratne, T. T. Salguero, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.* **115**, 034305 (2014), © 2014 AIP Publishing LLC. Crystal structure of 2H-$TaSe_2$ (a) and schematic of its main vibrational modes (b). Reprinted with permission from Z. Yan, C. Jiang, T. R. Pope, C. F. Tsang, J. L. Stickney, P. Goli, J. Renteria, T. T. Salguero, and A. A. Balandin, *J. Appl. Phys*. **114**, 204301 (2013), © 2013 AIP Publishing LLC.

2.6 Raman Spectra: Layer Thickness Determination

The thickness of flakes less than 20 layers can be determined within a one layer uncertainty using Raman spectroscopy.[30] It has also been observed that the thickness of flakes can be determined visually using an optical microscope. Device fabrication with $TaSe_2$-film channels started with this careful visual inspection and selection of thin (<30 nm thick) and uniform flakes after "graphene-like" exfoliation. It was observed and verified by AFM that

as the thickness of the $TaSe_2$ flake would decrease the color of the flake would change from a dark opaque yellow to a transparent light blue (Figure 6).

Figure 6 shows Raman spectra of $TaSe_2$ for nine exfoliated thin films with different thicknesses H ranging from a few nm to > 250 nm. The thicknesses of the exfoliated films were measured by atomic force microscopy (AFM). The 2H-$TaSe_2$ crystal possesses 12 zone center lattice vibrational modes. Four of these modes (E_{1g}, E^1_{2g}, A_{1g}, and E^2_{2g}) are Raman active and have prominent peaks at 150 cm^{-1}, 207 cm^{-1}, 235 cm^{-1} and 519 cm^{-1}. The peak around 207 cm^{-1} (labeled as E^1_{2g}) corresponds to the excitation of a vibrational mode in which the Se and Ta atoms oscillate, in anti-phase, parallel to the crystal surface. The peak around 235 cm^{-1} (labeled as A_{1g}), on the other hand, is due to the vibration of the Se atoms, in anti-phase, perpendicularly to the crystal surface while the Ta atoms are fixed. Finally, the peak at 519 cm^{-1} is due to the vibration of the lattice of the silicon substrate underneath. The atomic displacements for these vibrational modes are shown in Figure 5 (b). The modes with energy lower than 130 cm^{-1} are blocked by the Rayleigh filter of the spectrometer. There have been few reports of Raman data for $TaSe_2$.[31-34] In contrast, earlier studies used bulk $TaSe_2$ samples and focused on the lower frequency portion of the spectrum.[31-33] Comparison of our data with that in Ref. 34 indicates that the peak positions and mode assignments are consistent.

The pronounced Si peak from the substrate appears at 522 cm^{-1}. The intensity of the Brillouin zone-center Si peak is proportional to the interaction volume. It explains why the peak intensity is increasing with decreasing thickness of $TaSe_2$ film placed on top of Si substrate. The ratio of the intensity of the Si peak to that of A_{1g} or E^1_{2g} can be used for

determining the thickness of the exfoliated film. Figure 6 (b) presents the ratio of the intensity of the Si peak to that of the E_{2g} peak, $I(Si)/I(E^1_{2g})$, as a function of thickness H. This ratio decreases exponentially with increasing film thickness and can be fitted to the equation $I(Si)/I(E^1_{2g}) = 11.2\exp(-H/54.9) - 0.11$ (here the thickness H is in the units of nm).

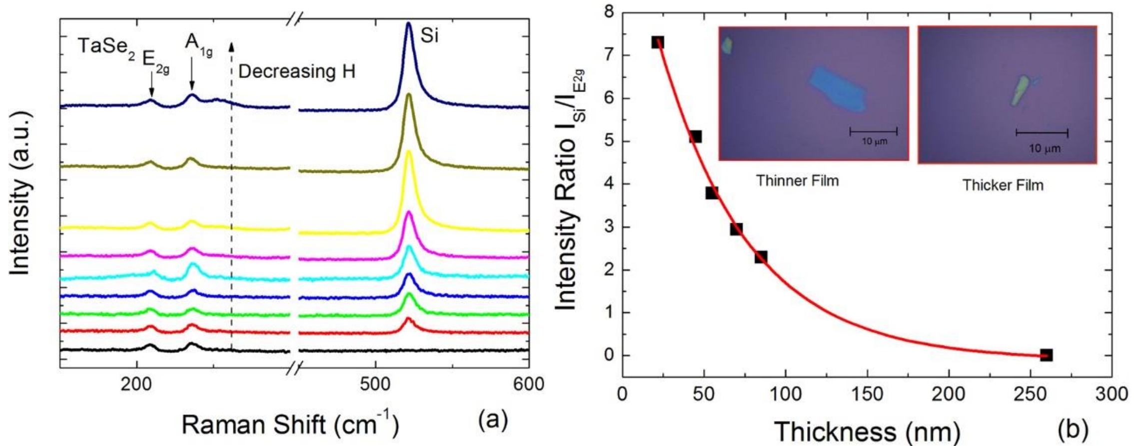


Figure 6: (a) Raman spectrum of the exfoliated thin films of $TaSe_2$ on Si substrate. The data is shown for the films thickness ranging from ~260 nm to below 30 nm. The characteristics E_{2g} and A_{1g} peaks of $TaSe_2$ are clearly observed. The intensity of Si peak at 522 cm^{-1} is increasing with the decreasing thickness of $TaSe_2$ film. (b) The ratio of the intensity of Si peak to E_{2g} peak in Raman spectrum of $TaSe_2$. The calibrated intensity ratio can be used for nanometrology of $TaSe_2$ films. The insets show optical microscopy images of two flakes of $TaSe_2$ with substantially different thickness. The thinner flakes appear blue in color whereas the thicker flakes appear yellow. Reprinted with permission from Z. Yan, C. Jiang, T. R. Pope, C. F. Tsang, J. L. Stickney, P. Goli, J. Renteria, T. T. Salguero, and A. A. Balandin, *J. Appl. Phys*. **114**, 204301 (2013), © 2013 AIP Publishing LLC.

2.7 Summary

One of the goals in this dissertation was to fabricate devices with layered transition metal dichalcogenide (TMDC) materials which would enable us to investigate properties of these materials. Initially, the graphene device fabrication steps would be used and modified to suit the TMDC materials. In order to make devices from any van der Waals' materials one should start from making flakes of the respective material, characterize the number of layers of flakes and then make micrometer size metal contacts according to the symmetry and shape of the flakes made. As shown earlier in this document Raman spectroscopy is recommended for $TaSe_2$ characterization in order to determine the number of layers. The methodology works well with 300 nm SiO_2 on silicon substrate. The obtained dependence can be used as a calibration curve for the Raman-based nanometrology of $TaSe_2$ films and the approach can be extended to other layered van der Waals material. From a practical perspective, the Raman metrology of exfoliated films is easier and faster than AFM inspection.

Chapter 3

2H-$TaSe_2$ Thermal Characterization

Raman spectroscopy is one of the most effective and non-destructive techniques for characterizing and analyzing materials in various forms such as bulk, thin film, device or other nanostructures. It has been used in this investigation for layer thickness determination as described in Chapter 2 and thermal characterization (i.e. thermal conductivity) as described in this chapter. It has been widely used on other van der Waals materials such as graphene on Si/SiO_2 substrate.[35] The ease and popularity at which this technology was used with the structural characterization of graphitic materials, for identifying graphene layers and counting of such layers, made it a convenient tool to employ for similar characterizations of 2H-$TaSe_2$ thin films with minimal sample preparation.

3.1 Introduction

Obtained temperature coefficients characterize the inharmonicity of the $TaSe_2$ crystal lattice. They also can be used to extract the thermal conductivity data using the Raman optothermal technique, which was originally developed for graphene.[36] The data presented in Figure 7 (b) can be used as calibration curves for determining the local temperature rise

in $TaSe_2$ flakes. The temperature is extracted from the shift of Raman peak positions. In a sense, the Raman spectrometer is thus used as a thermometer.

3.2 Raman Spectroscopy and Thermal Conductivity

Reported here are the results of the investigation into the thermal properties of thin films of tantalum diselenide (2H-$TaSe_2$) obtained via the "graphene-like" mechanical exfoliation of crystals grown by chemical vapor transport. The temperature dependence of Raman spectra of 2H-$TaSe_2$ were studied in the temperature range from 83 K to 613 K. The sample as an exfoliated $TaSe_2$ flake was put in a hot-cold cell where the temperature was controlled externally with 0.1 °C accuracy. Figure 7 (a) shows the Raman spectrum of a typical $TaSe_2$ flake measured at different temperatures. The Raman peak positions of both A_{1g} and E^1_{2g} modes move to a lower wavenumber range (red shift) when temperature increases. The Raman peak positions of $TaSe_2$ A_{1g} and E^1_{2g} mode at the different temperatures are shown in Figure 7 (b). In the measured temperature range, the temperature dependence of A_{1g} and E^1_{2g} modes can be represented by a linear relation $\omega = \omega_o + \Gamma T$, where ω_o is the Raman peak frequency when temperature T is extrapolated to 0 K, and Γ is the first-order temperature coefficient. The extracted temperature coefficients for two main Raman peaks, A_{1g} and E^1_{2g}, were Γ_1 = -0.013 cm^{-1}/°C and Γ_2 = -0.0097 cm^{-1}/°C, respectively.

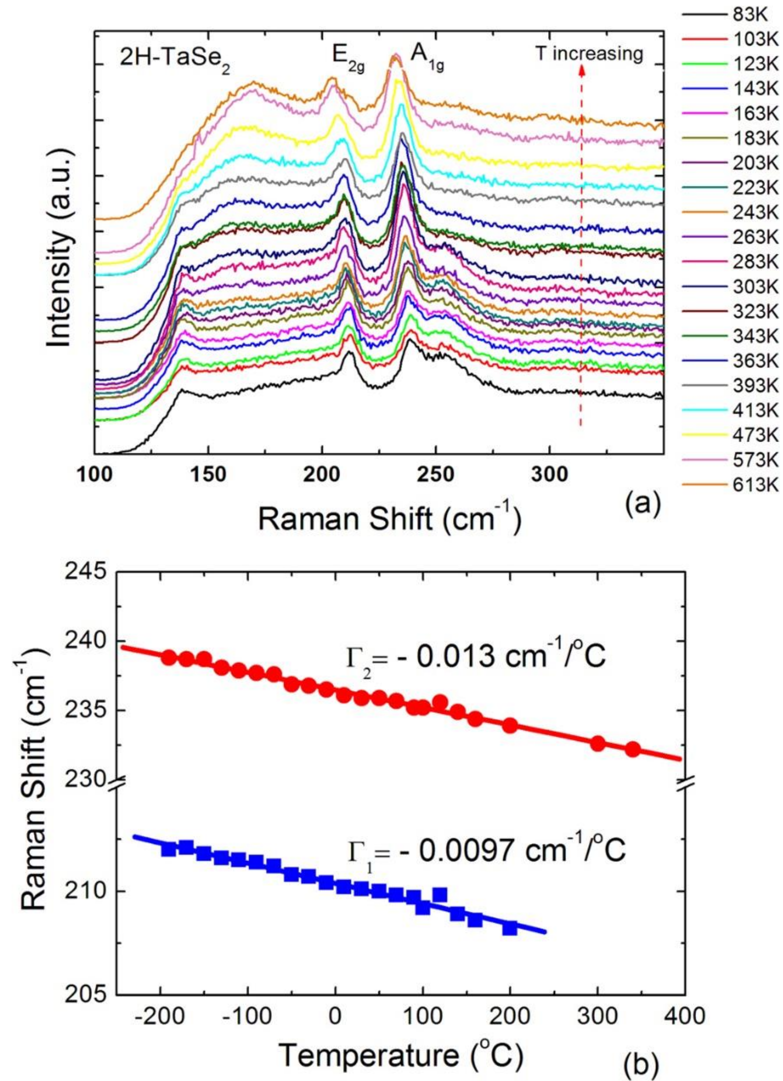


Figure 7: (a) Evolution of Raman spectrum of 2H-$TaSe_2$ thin film with temperature. A new peak appears in the spectra at about 250 cm^{-1} after temperature decreases below ~220 K. The peaks shift their position with temperature. (b) Temperature coefficients C1 and C2 for E_{2g} and A_{1g} Raman peaks of 2H-$TaSe_2$, respectively. The temperature coefficients can be used for the extraction of the thermal conductivity of thin films using the Raman optothermal method. Reprinted with permission from Z. Yan, C. Jiang, T. R. Pope, C. F. Tsang, J. L. Stickney, P. Goli, J. Renteria, T. T. Salguero, and A. A. Balandin, *J. Appl. Phys*. **114**, 204301 (2013), © 2013 AIP Publishing LLC.

For the thermal measurements, we intentionally increased the intensity of the excitation laser so that it induces a local heating of the sample. The low thermal conductivity of $TaSe_2$ allows one to achieve local heating at the power level of about 1–2 mW. Figure 8 (a) shows a characteristic Raman mode of the tested $TaSe_2$ flake at low and high excitation power. The Raman peak position of the E^1_{2g} peak shifts from 209.1 cm^{-1} to 207.7 cm^{-1} as the power increased by 90%. The calculated change in the local temperature introduced by the laser is ~144 °C. The measurements were repeated using another Raman peak of $TaSe_2$ to ensure reproducibility of the local temperature measurement. The temperature rise for a known dissipated power and sample geometry allows one to determine the thermal conductivity.[36] The finite element method (FEM) to simulate the heat dissipation in the samples under test were used. The thermal conductivity was determined via the iteration approach. Details of this FEM based procedure for extraction of thermal conductivity are described in Ref. 37.

The inset to Figure 8 (b) presents a schematic of the simulated sample structure. The radius of the simulated domain size is 100 μm. The radius of the $TaSe_2$ flake and the laser spot are 4 μm and 0.5 μm, respectively. The thicknesses of $TaSe_2$ flakes used for extraction of thermal conductivity were H = 45 nm, H = 55 nm, and H = 85 nm. The thickness of the silicon dioxide layer and silicon substrate were 300 nm and 0.5 mm, respectively. The silicon substrate was placed on an ideal heat sink so that the temperature at the bottom side was fixed at 300 K. Adiabatic conditions were assumed at other external boundaries.

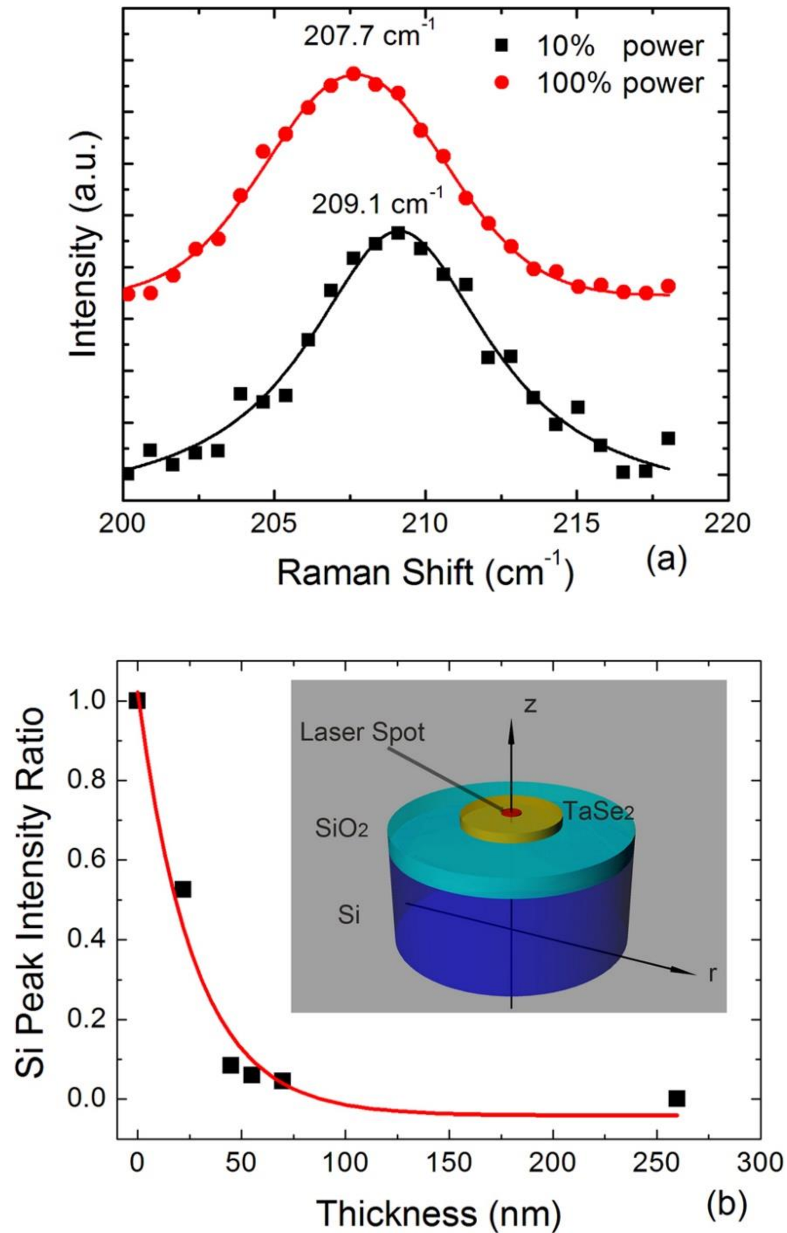


Figure 8: (a) Shift and broadening of the Raman peaks of 2H-$TaSe_2$ as a result of local heating with the excitation laser. (b) Intensity ratio of the Si Raman peak from the substrate without thin film to that of the substrate covered with 2H-$TaSe_2$ thin film. The data allows one to estimate the amount of power absorbed by the film. The inset shows a model used for extraction of the thermal conductivity of thin films of 2H-$TaSe_2$. Reprinted with permission from Z. Yan, C. Jiang, T. R. Pope, C. F. Tsang, J. L. Stickney, P. Goli, J. Renteria, T. T. Salguero, and A. A. Balandin, *J. Appl. Phys*. **114**, 204301 (2013), © 2013 AIP Publishing LLC.

It has been reported that the room temperature thermal conductivity of bulk 2H-TaSe2 is ~16 W/mK.[38] These results for mechanically exfoliated thin films are consistent with prior measurements for bulk 2H-TaSe2.[38-40]

Thickness H (nm)	45	55	85	Bulk
K (W/mK)	9	11	16	16

Table 1: Thermal conductivity of exfoliated 2H-$TaSe_2$ thin films at room temperature.

3.3 Summary

These results are important for understanding lattice dynamics of $TaSe_2$ films and for device applications of metal dichalcogenide thin films. Specifics of electron and phonon transport in thin films of 2H-$TaSe_2$ exfoliated from single crystals grown by chemical vapor transfer method were investigated. Raman optothermal measurements indicated that the room temperature thermal conductivity in thin films is dominated by phonons and that it decreases from its bulk value of ~16 W/mK to ~9 W/mK in 45 nm thick films. Scaling of thermal conductivity with the film thickness suggests that the phonon scattering from the film boundaries is substantial despite the sharp interfaces of the mechanically cleaved samples.

Chapter 4

$TaSe_2$ FETs: Electrical Performance, Optical Response, and Temperature Effects

4.1 Introduction

Implementation of transistors, diodes, and other circuit elements with metallic materials rather than semiconductors would offer a number of potential benefits including inherent radiation hardness and low cost. There have been a number of proposals and attempts to implement all-metallic switches and circuits ranging from metal dot single electron transistors[41-43] to metallic carbon nanotube devices,[44-46] metallic nanowire transistors,[47] and all-metallic spin transistors.[48,49] To date, the most successful demonstration of an electrically gated metallic channel device is a graphene field-effect transistor (FET) type device.[50-52] Graphene devices have high mobility,[51,52] high saturation velocity,[53] low flicker noise[54,55] and can be gated at room temperature (RT).[50-52] The V-shaped transconductance characteristics of graphene devices and their low $1/f$ noise level offer increased functionalities for signal processing (f is the frequency).[55-57] However, the absence of a

band gap, the high carrier concentration, and the high mobility in graphene result in substantial leakage currents. In addition, graphene-based devices cannot be switched off, and the single-atom thickness of graphene leaves it susceptible to radiation damage.[58] In this dissertation, it has been demonstrated that electrically gated devices with strongly non-linear current-voltage (I-V) characteristics can be based on thin films of metallic van der Waals materials. The drain-source current in such devices reveals an abrupt transition from a highly resistive to a conductive state with the threshold tunable via the gate voltage. It has been further shown that such I-V characteristics can be used to implement all-metallic logic circuits that are potentially radiation-hard. These devices are based on tantalum diselenide ($TaSe_2$) thin-film conducting channels.

4.2 $TaSe_2$ FETs: Device Fabrication

Device fabrication with thin films of $TaSe_2$ channels enabled the investigation of this transition metal dichalcogenide's properties and the observation of any CDW effects at transition temperatures. The processes used for fabrication are similar to the popularized van der Waals material, graphene, where fabrication starts with the mechanical exfoliation of thin flakes on the micrometer size. The following steps of flake characterization by optical microscopy and/or Raman spectroscopy, custom contact patterning, contact metal deposition, and electrical characterization are also similar. As discussed in Chapter 2, the micro-mechanical exfoliation method produce flakes that are irregularly shaped, randomly sized, and randomly located. As a result, the customization of electrodes and pads require

the use of high resolution lithography techniques, like Electron Beam Lithography (EBL). The energy of electrons used in this Electron Beam Lithography system is on the order of 20 keV and offers a high pattern resolution without the need for photomasks. It uses a focused beam of electrons to "write" patterns drawn by CAD software, part of a Nanometer Pattern Generation System (NPGS) system. This system is used to accurately locate flakes and position the desired electrodes and pads. Such versatility makes it convenient to adapt to any van der Waals, like $TaSe_2$.

The devices with 2H-$TaSe_2$-film channels were fabricated using electron beam lithography (LEO SUPRA 55) for source and drain electrode patterning and electron-beam evaporation (Temescal BJD-1800) for metal deposition. Silicon substrates with 300-nm thick SiO_2 layers were spin coated (Headway SCE) and baked consecutively with two positive resists: methyl methacrylate (MMA) and then polymethyl methacrylate (PMMA). The MMA was spin coated at 4,000 rpm for 40 seconds and baked at 180 C for 10 minutes on a hotplate. Then, the PMMA was likewise spin coated, but baked for 15 minutes. The use of bilayer positive resists is a standard practice which allows for better lift-off and more defined metal electrodes/contacts as the MMA (below the PMMA) has a faster developing time than PMMA, providing for a slight undercut for metal deposition.

After patterning of the source and drain contacts to the 2H-$TaSe_2$ flakes, the sample(s) were put in a solution of MIBK: IPA 1:3 for 65 seconds for development. The areas exposed by EBL dissolve for positive resists. Metal layers of Ti/Au (10-nm / 70-nm) were then deposited. The titanium layer helps the gold to adhere to the SiO_2 on the Silicon substrate. The final steps involve soaking the sample(s) overnight in acetone for lift-off of

the positive resists and unwanted metal deposition, rinsing in a bath of isopropyl alcohol (IPA), drying with nitrogen gas, thus leaving behind the patterned electrodes/contacts and completing the devices. The heavily doped Si/SiO_2 wafer served as a back gate. Most of the devices had two source and drain terminals on top, whereas a few others were made with four terminals to probe metal contact effects. Figure 9 shows the schematic of a $TaSe_2$ device.

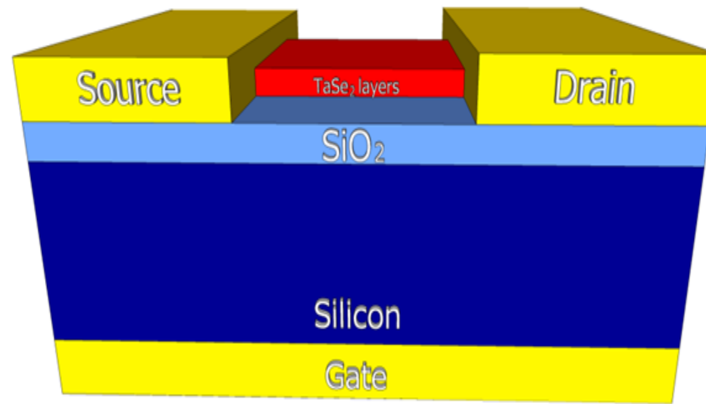


Figure 9: $TaSe_2$ device schematic.

Microscopy images of the representative 2H-$TaSe_2$-Ti/Au devices are show in Figure 10. The majority of the devices had a channel length, *L*, in the range from 3 to 12 μm, and the channel width, *W*, in the range from 3 to 4 μm. The estimated average thickness of the devices selected for the study was *H*~20-35 nm. The metal contacts appear yellow in the image and the CDW channel blue. It was noted that devices with thinner channels were less robust.

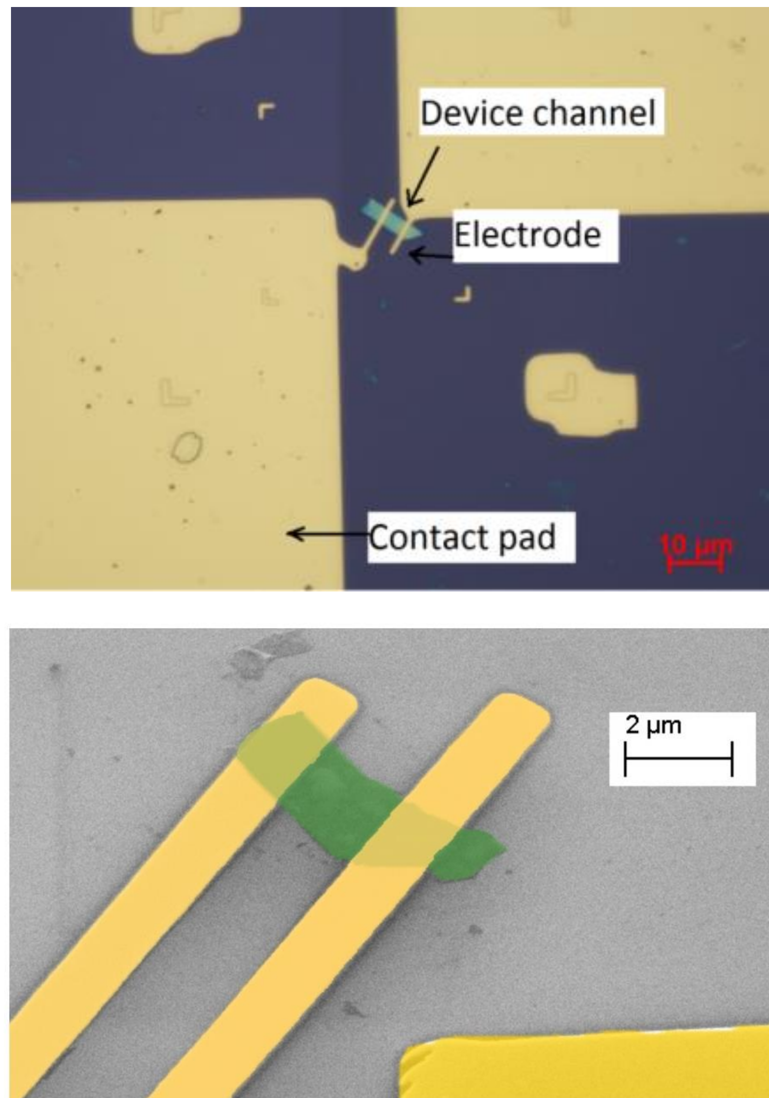


Figure 10: Optical (a) and SEM (b) images of representative all-metallic devices with 2H-$TaSe_2$ thin-film channels and Ti/Au source and drain contacts. The pseudo colors in the SEM image were used for clarity: yellow corresponds to metal contacts, green corresponds to 2H-$TaSe_2$. Reprinted with permission from J. Renteria, R. Samnakay, C. Jiang, T. R. Pope, P. Goli, Z. Yan, D. Wickramaratne, T. T. Salguero, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.* **115**, 034305 (2014), © 2014 AIP Publishing LLC.

4.3 $TaSe_2$ FETs: Electrical Characteristics

Two-terminal $TaSe_2$ devices were tested for their IV characteristics and according to theory we expected to see an ohmic IV curve through the devices at room temperature. This was then expected to change below the Peierls transition temperature T_C, which for $TaSe_2$ was around 122 K. However, upon testing at room temperature we saw the appearance of a diode like behavior, and the device seemed to allow current to flow after a certain threshold voltage had been reached. Current-voltage (I-V) measurements of $TaSe_2$ are presented in Figure 11. The different curves correspond to different devices of varying channel dimensions and thicknesses as listed in Table 1.

The measured I-V characteristics are asymmetric and strongly non-linear with clear threshold voltages between V_{DS}=5 V and V_{DS}=7 V as seen in Figure 11. The behavior of these curves are comparable to those observed in other CDW materials.[59,60] In CDW conductors, the threshold V_{DS} indicates the electrical field at which the CDW depins and slides relative to the lattice.[59] This surprising trend was consistent for all $TaSe_2$ devices tested with different dimensions and thicknesses ranging from approximately 10 nm to 40 nm. The graph below shows different $TaSe_2$ devices of different dimensions and their IV curves showing uniformity of results in their response.

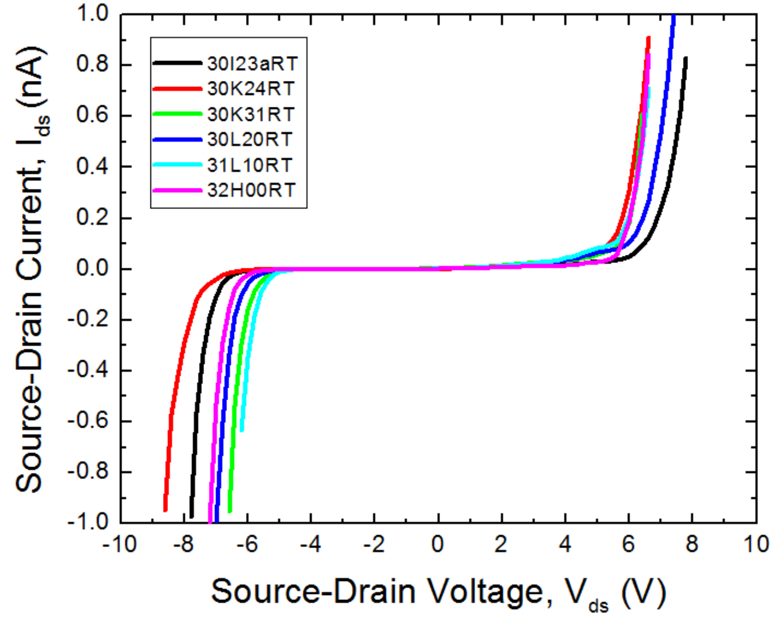


Figure 11: Current-voltage characteristics of several $TaSe_2$ devices at room temperature.

Device ID	Length (µm)	Width (µm)	Thickness (µm)
30I23a	3	4	30
30K31	3	3	25
30L20	4	3	35
31L10	12	3	20

Table 2: $TaSe_2$ device dimensions and thicknesses.

In Figure 12 source-drain I-V characteristics of 2H-$TaSe_2$ – Ti/Au all-metallic devices at room temperature are presented. The different colored curves correspond to different sizes of the 2H-$TaSe_2$ channels (L, W and H). The source – drain current, I_{DS}, was intentionally limited to a low value to avoid damaging the devices. The maximum current passed through these devices was in the µA range. One can see that all devices reproducibly

reveal a well-defined threshold voltage, V_{TH}, for the transition from the "negligible-current" regime to the "high-current" regime. In this sense, these all-metallic devices operate as switches. The value of V_{TH} varied from device to device depending on the channel size. The high value of the source drain voltage, V_{DS}, which changed from -9 V to +9 V at room temperature, is related to the high contact resistance and imperfections of the technology used to fabricate these proof-of-concept devices from exfoliated 2H-$TaSe_2$. The inset shows I-V characteristics at T=100 K. The transition from the "Off" to "On" state is even more pronounced at low temperature.

4.4 $TaSe_2$ FETs: Gating of All-metallic Devices

The all-metallic 2H-$TaSe_2$ – Ti/Au devices were gated at room temperature. Figure 13 shows the normalized drain-source I-V characteristics for several values of the back-gate bias, V_G. The gate bias changes from -25 V to +25 V with maximum V_{DS}=20 V. The large absolute values of the applied gate bias are explained by the fact that it was applied via thick SiO_2 layer (300 nm). The large V_{DS} value is attributed to the voltage drop on the contacts and electrodes. The important observation for the proposed all-metallic circuits is the fact that the threshold voltage V_{TH} can be shifted by the gate voltage V_G. The fabricated all-metallic 2H-$TaSe_2$ – Ti/Au devices can operate as gate-controlled switches. It is expected that the values of V_G and V_{DS} can be decreased and I_{DS} increased as the device fabrication technology matures. It was found that as-grown 2H-$TaSe_2$ samples had at least three orders-of-magnitude lower resistance values than the exfoliated thin film channels.

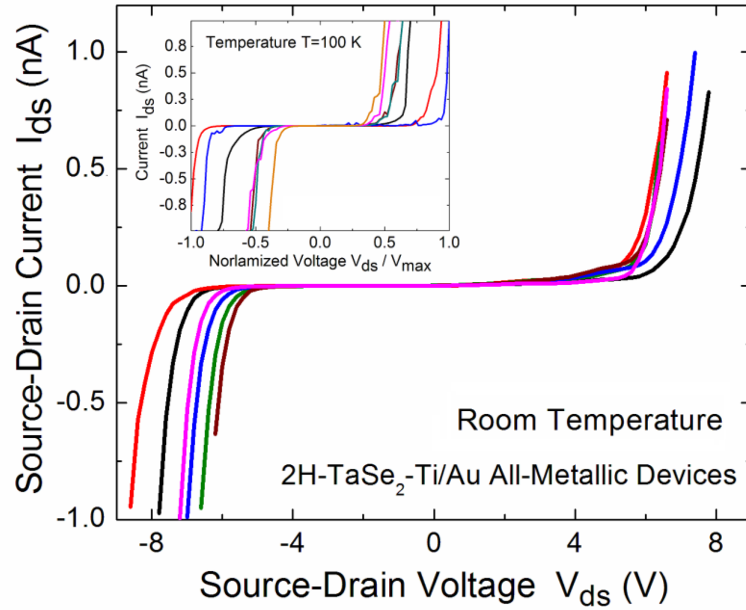


Figure 12: Source-drain I-V characteristics of 2H-$TaSe_2$ – Ti/Au all-metallic devices at RT. Curves of different colors correspond to different sizes of the 2H-$TaSe_2$ channels. Note that all devices revealed a well-defined threshold voltage, V_{TH}, for the transition from the "Off" to "On" state. The inset shows I-V characteristics at T=100 K. Reprinted with permission from J. Renteria, R. Samnakay, C. Jiang, T. R. Pope, P. Goli, Z. Yan, D. Wickramaratne, T. T. Salguero, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.* **115**, 034305 (2014), © 2014 AIP Publishing LLC.

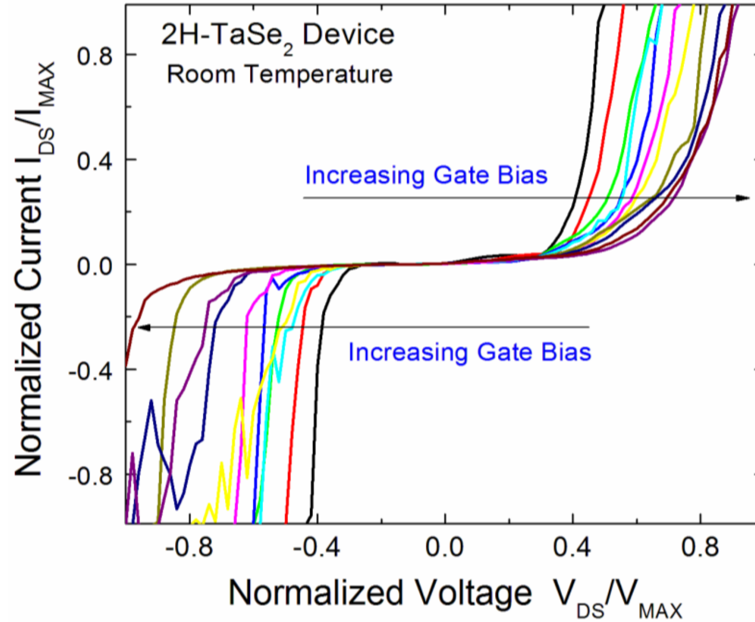


Figure 13: Source-drain I-V characteristics of a representative 2H-$TaSe_2$ – Ti/Au all-metallic device for different gate biases at RT. The gate is changing from -25 V to +25 V in the direction indicated by arrows. The high absolute values of the gate bias are due to the thick SiO_2 layer used as gate dielectric in the back-gate design. The source-drain voltage and currents are normalized to facilitate explanation of the proposed all-metallic logic gate design. Reprinted with permission from J. Renteria, R. Samnakay, C. Jiang, T. R. Pope, P. Goli, Z. Yan, D. Wickramaratne, T. T. Salguero, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.* **115**, 034305 (2014), © 2014 AIP Publishing LLC.

It has been suggested that metallic MX_2 are more reactive and after exfoliation may undergo different chemical transformations.[61] In two of the fabricated devices we changed the metal contact technology and instead of Ti/Au deposited pure Au. The measured I-V characteristics still revealed the same non-linearity. Experiments with bulk crystals of 2H-$TaSe_2$ indicate that the resistivity of material in device channels with a few-nanometer thickness is substantially higher than that in bulk form. It has also been found that I-V characteristics in bulk 2H-$TaSe_2$ resistors are linear. There was also the possibility that an avalanche effect was occurring where voltage applied is great enough to accelerate and

knock other electrons free from the material creating an avalanche of current. This was disproved, however, because the curves are reproducible after repeated testing. An avalanche effect normally destroys an FET. The devices with thin exfoliated 2H-$TaSe_2$ channels and different contact electrode areas revealed similar characteristics in the forward and reverse current directions, suggesting that the device channel itself is responsible for the observed phenomena.

4.5 $TaSe_2$ FETs: Optoelectronic Properties

The source-drain current as a function of the source-drain voltage was measured under dark and illuminated conditions. At small bias, the channel was resistive allowing for negligible current only. As a threshold field was reached (corresponding to some threshold voltage), one observed a fast increasing non-linear current. The light illumination shifted the on-set of the high non-linear current regime to larger voltages. There was a substantial difference between the threshold voltages at dark and illuminated conditions allowing for optical switching applications. It is interesting to note that unlike a conventional photo-resistor, the $TaSe_2$ device switched on in the dark and switched off under illumination. The physical mechanism of the observed optical effects in $TaSe_2$ thin films was different from that in conventional semiconductors and can be related to collective or excitonic effects. The light sensitivity of $TaSe_2$ thin films was tested between 645 nm and 340 nm light wavelengths. It was found that the threshold voltage of the $TaSe_2$ devices increases as the wavelength of light decreases.

An experiment was conducted to characterize the optical response of these $TaSe_2$ devices under light illumination as was done with similar CDW materials.[60] These $TaSe_2$ devices were exposed to white light measured at 10,000 candelas/m^2 or equivalently 14.6W/m^2. Figure 14 shows a most interesting result that is in contrast to the behavior of typical optoelectronic devices. The graph includes the I-V response of the same two-terminal device under different conditions. The curve labeled “A” is the device in the dark and “B” is the device under light illumination. Both curves demonstrate the non-linearity already seen in $TaSe_2$ devices. A peculiarity is noted when it was observed that the threshold voltage increases under light illumination. This is inconsistent with the sensitivity of I-Vs to light exposure of typical optoelectronic devices where a decrease of threshold voltage is expected due to the excitation of carriers resulting in increased current and less non-linearity in the I-V response. It was also observed that after allowing the device to sit in the dark after being illuminated that the I-V curve began to “recover” back to its original form (i.e. before exposure to light) as seen in the I-V response labeled “C” in Figure 15.

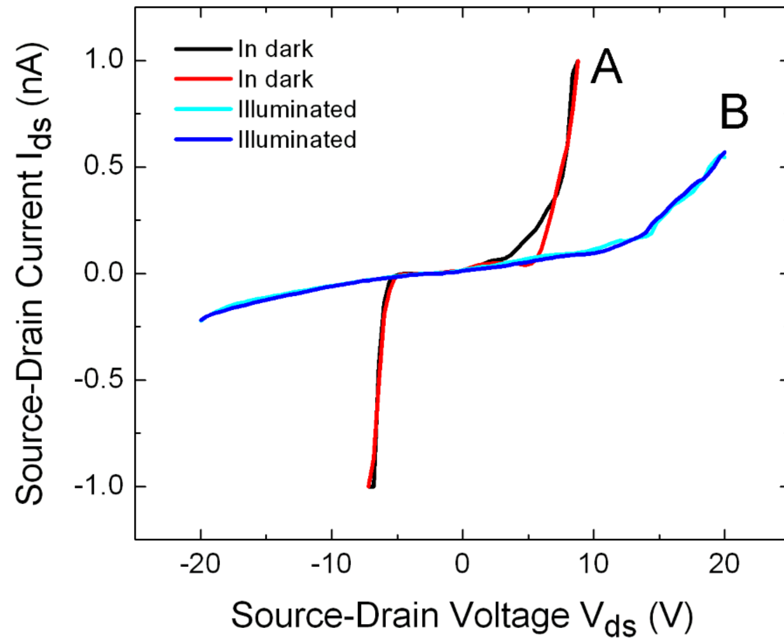


Figure 14: Current-voltage characteristics of $TaSe_2$ in the dark (A) and illuminated (B).

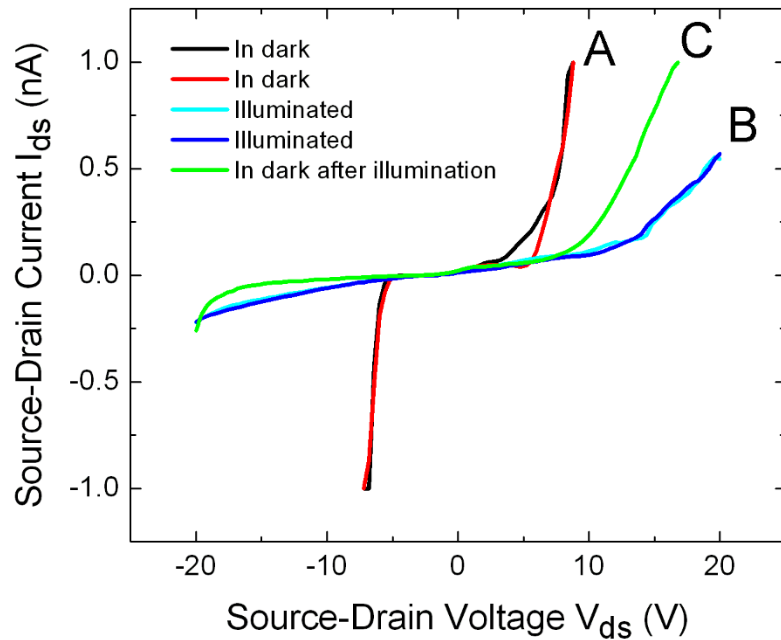


Figure 15: IV characteristics of $TaSe_2$ in the dark (A) and illuminated (B) including the "recovery" effect (C) after being left in the dark for one hour.

A further addition to the light experiments was to see the effect of lights of different wavelengths on the IV characteristics of the fabricated $TaSe_2$ devices to see if the response was unique to particular wavelengths or if there was a correlation between wavelength and response. This was done by using the same Lakeshore probe station with its white light source by using color filters that filtered out all light of unwanted wavelengths. This use of color filters is shown below.

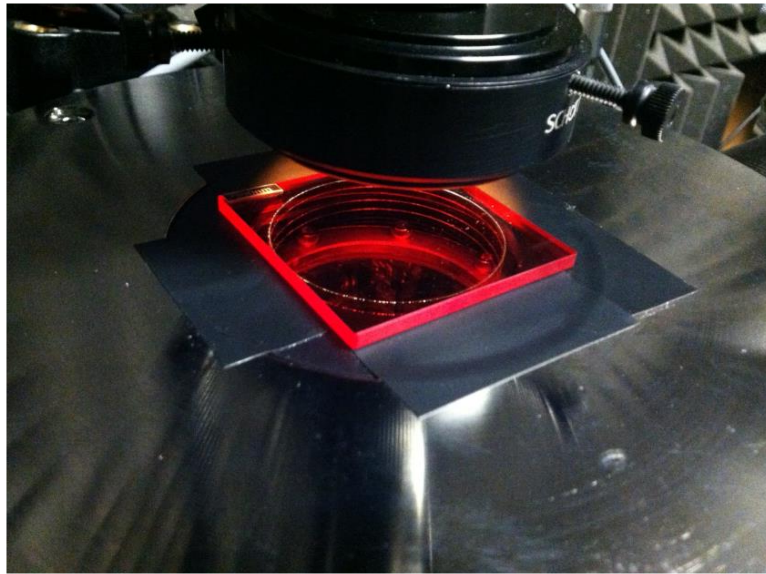


Figure 16: Use of color filters to filter out light of unwanted frequencies on the Lakeshore probe station.

The sequence of testing for light of different wavelengths was as follows. Note that white light was used at the start and at the end of the tests to see the variation that may have occurred.

Step	Description	Label
1	Initial test with white light source, no color filter	30K_3_1_lt100
2	Test with light source, 645nm color filter	30K_3_1_lt100_645nm
3	Test with light source, 590nm color filter	30K_3_1_lt100_590nm
4	Test with light source, 550nm color filter	30K_3_1_lt100_550nm
5	Test with light source, 495nm color filter	30K_3_1_lt100_495nm
6	Test with light source, 455nm color filter	30K_3_1_lt100_455nm
7	Test with light source, 395nm color filter	30K_3_1_lt100_395nm
8	Test with light source, 340nm color filter	30K_3_1_lt100_340nm
9	Re-test with white light source, no color filter	30K_3_1_lt100

Table 3: Table showing the order in which light of different wavelengths was used on our devices.

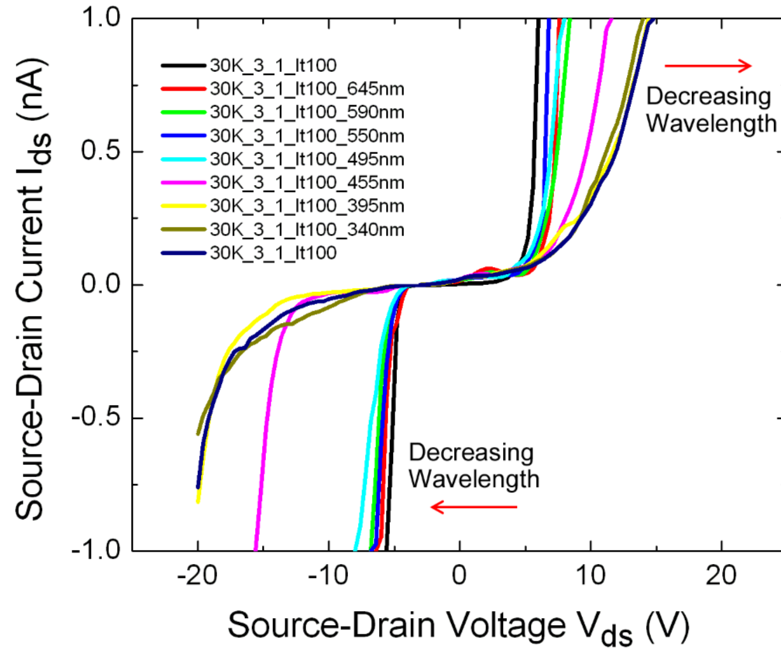


Figure 17: Effect of color filters on $TaSe_2$ after filtering out light of unwanted frequencies.

The effects of light illumination on the I-V characteristics of 2H-$TaSe_2$ – Ti/Au devices were studied. Figure 18 shows the normalized drain-source current for the device in the dark and under natural light at T=100 K. The behavior at room temperature was

similar, but the on-off transition was less pronounced. One can see that the onset of the conductive regime shifts to higher voltages in devices under illumination. This rather unusual trend is opposite to that observed in conventional photoresistors, where the current increases under light illumination due to electron – hole pair generation. However, such behavior was previously reported for CDW devices with the threshold for collective current shifting to larger V_{TH} under light illumination.[62] The sharp on-off transition and strong dependence of V_{TH} with light indicate some potential for optoelectronic device applications.

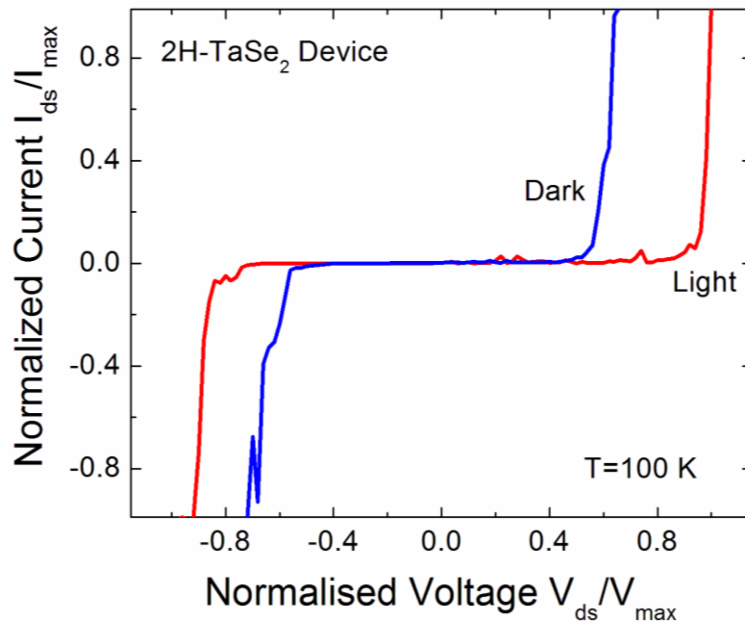


Figure 18: Normalized drain-source current for the device in dark and under natural light at T=100 K. One can see that the onset of the conductive regime shifts to higher voltages in devices under illumination, which is opposite to what is expected for a conventional photoresistor. Reprinted with permission from J. Renteria, R. Samnakay, C. Jiang, T. R. Pope, P. Goli, Z. Yan, D. Wickramaratne, T. T. Salguero, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.* **115**, 034305 (2014), © 2014 AIP Publishing LLC.

4.6 Discussion of Physical Properties and Summary

The physics of the process in the 2H-$TaSe_2$ channel or $TaSe_2$ – Ti/Au interface, which results in the observed current characteristics, is not entirely clear. The things that can be stated now is that the effects are reproducible in many tested devices (about 20) and in the same devices over a substantial time period (about a month for some devices). The gating of the source-drain current in the metallic channel with H~20 nm is surprising due to the small carrier screening length in such materials. It is possible that the flakes have non-uniform thickness (smaller at the edges) and part of the current goes via a much thinner film allowing for gating. One should note that similar gating was observed in CDW devices with rather thick channels as well.[63] No commonly acceptable explanation exists for gating of CDW devices at RT. The measured I-V characteristics with the threshold voltage appear similar to those of CDW devices where the abrupt increase in current results from the onset of the collective current regime.[64-66] This mechanism would explain the I-Vs of 2H-$TaSe_2$ – Ti/Au devices at low temperature. However, the incommensurate CDW transition temperature, T_P, in 2H-$TaSe_2$ is T=122 K which is followed by a commensurate CDW transition at T=90 K.[67] Our previous work indicated that T_P increases in some 2D materials with decreasing film thickness.[68] It still remains to be shown if thinning 2H-$TaSe_2$ to 20-nm thickness can result in substantial T_P change. The following chapter will describe how such I-V characteristics can be exploited for use in a possible circuit application consisting of *all-metallic* logic circuits that are potentially *radiation-hard* and based on these tantalum diselenide ($TaSe_2$) thin-film conducting channels.

Chapter 5

$TaSe_2$ FETs: Possible Circuit Applications

The measured I-V characteristics of the all-metallic 2H-$TaSe_2$ – Ti/Au devices are completely different than those of conventional transistors. However, they can be used for information processing. The high transconductance near V_{TH}, strong gating effect, and low leakage current are the three unique and rather surprising characteristics of the fabricated $TaSe_2$ devices. These characteristics are unusual for the metallic-channel transistors. The measured I-V characteristics of the $TaSe_2$ devices can be fitted with the following formula[69]

$$I_{DS} \approx I_0 \times e^{\left(\frac{V_{GS}-V_{TH}}{V_t}\right)} \times \left(1 - e^{\frac{-V_{DS}}{V_t}}\right) \times e^{\frac{\alpha V_{DS}}{V_t}}, \qquad (1)$$

where I_{DS} is the source-drain current, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, V_{TH} is threshold voltage, I_0 is a constant depending on the channel geometry, V_t is a parameter similar to the thermal voltage in conventional devices, α is a constant reflecting drain-to-channel coupling. It is interesting to note that the same equation describes the subthreshold current of a metal-oxide-semiconductor (MOS) device taking into account the drain-induced barrier lowering effect.[69] This effect becomes prominent in

sub-micron technologies, where the source and drain depletion regions penetrate significantly into the channel and control the potential and the field inside the channel. In our case of all-metallic switches, similar I-V characteristics are observed in the long channel devices.

Another feature, which makes these devices potentially suitable for practical applications, is the experimentally observed asymmetry in the I-V characteristics for 2H-$TaSe_2$ – Ti/Au devices with different channel sizes. In Figure 19 (a) we show the experimental I-Vs for a selected bias voltage that provide the functionality. The red and the blue curves correspond to the devices with two different channels: device A and device B. The threshold voltages of these experimental I-V curves are shifted by several volts. For example, device A is in the low-conductance state in the V_{DS} region from -18 V to -15 V while device B shows an exponential current increase. The situation is opposite in the voltage range from +15 V to +18 V, where device B is in the "on" state while device A is in the "off" state. This asymmetry provides the possibility for implementing a complementary pair logic based on the $TaSe_2$ devices with different channels.

The schematics of the all-metallic inverter comprising two $TaSe_2$ devices are shown in Figure 19 (b). The devices are assumed to have a shift in their threshold voltages ΔV_{TH}. The latter makes it possible to realize an all-metallic complementary pair. The same input voltage applied to the gates of these devices makes one of the transistors in the highly conducting (On state), while reducing source-to-drain current in the second transistor (Off state). As a result the whole circuit operates a NOT gate similar to the standard design with two metal-oxide-semiconductor field-effect transistors (MOSFETs). The proposed all-

metallic logic gate can occupy a niche for certain applications together with conventional MOSFETs, similar to recently reported non-Boolean graphene circuits.[70]

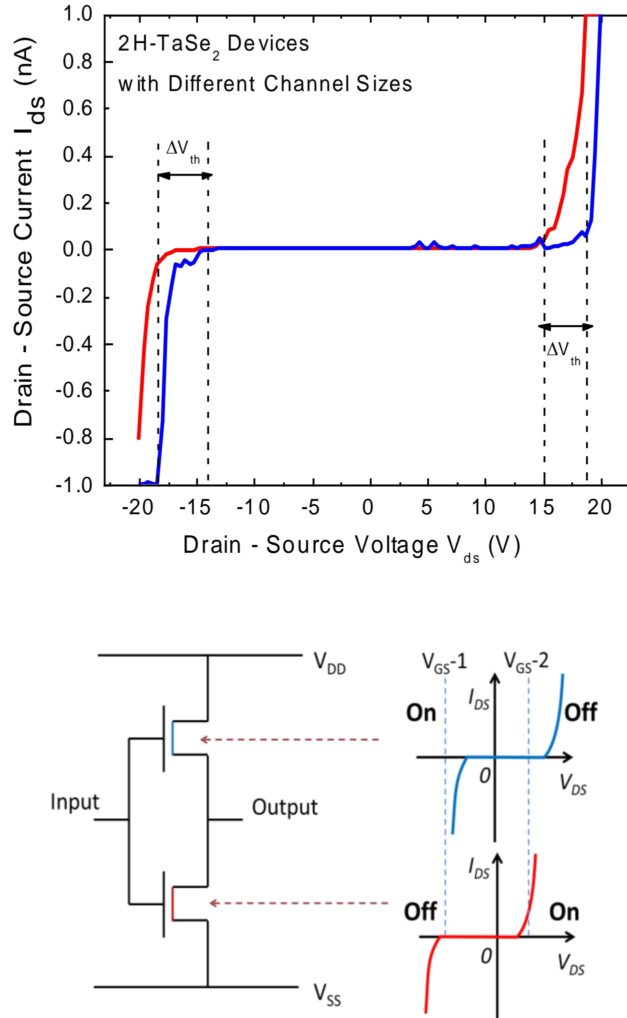


Figure 19: Experimental I-Vs for two $TaSe_2$ devices A (red curve) and B (blue curve) with different channels (a). The curves show a shift of the threshold voltages ΔV_{TH} for positive and negative bias. Schematic shows the all-metallic inverter comprising devices A and B (b). The devices are arranged in a complementary pair, whereby the same gate voltage turns one of the switches to the conducting (on state) while reducing the source-to-drain current in the second transistor to negligible (off state). Reprinted with permission from J. Renteria, R. Samnakay, C. Jiang, T. R. Pope, P. Goli, Z. Yan, D. Wickramaratne, T. T. Salguero, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.* **115**, 034305 (2014), © 2014 AIP Publishing LLC.

Chapter 6

MoS_2 Field-Effect Transistors

6.1 Introduction

Molybdenum disulfide is another transition metal dichalcogenide that has been researched for its direct bandgap (1.9 eV) at monolayer thicknesses being comparable to that of silicon.[71-73] In this investigation the fabrication and low-frequency 1/*f* aging performance of MoS_2 three-terminal devices were studied. MoS_2 thin films were exfoliated mechanically from single crystals. For both aged and as-built samples both channel and contact noise can be seen and clearly distinguished. Noise measurements of MoS_2 – Ti/Au devices comply with and are well supported by the McWhorter's model[74] of carrier concentration contributions to conduction fluctuations, which is contrary to the popular van-der-Waals material graphene. The results, however, do not comply with Hooge's theory that conduction fluctuations is a bulk phenomenon whose contributions are the result of mobility fluctuations and not carrier concentration fluctuations. The calculated trap density of these fabricated devices is 2×10^{19} $eV^{-1}cm^{-3}$ and 2.5×10^{20} $eV^{-1}cm^{-3}$ for virgin and aged samples, respectively. This is on the same order of magnitude as high-k MOSFETS.[75] As the devices age, it can be shown that noise degradation is mostly due to the channel and not the contacts.

6.2 Noise Measurement Setup

The overall noise measurement setup, including a Lakeshore probe station enclosed within an environmental chamber, connections to the device under test (DUT), and other instrumentation, is pictured in Figure 20. The Lakeshore probe station is very much like the ones often used in small scale electronics labs with a sample holder stage, adjustable micro-manipulator probes, and coaxial or triaxial cables to gain access to devices. This probe station is enclosed within an environmental chamber about the size and shape of a coffee can and is capable of a temperature range of 4 K to 450 K as seen in Figure 22. We can tune to any temperature in this range with the use of a controller, built-in heaters, liquid cryogens (like liquid nitrogen or liquid helium), and the chamber being under vacuum (10^{-5} Torr at R.T. → 10^{-7} Torr at low temp).

A source-drain bias (V_{ds}) is applied to the device under test (DUT) via a biasing circuit illustrated in Figure 21. The source-drain bias of the DUT may include a gate bias (V_g) as well. The source-drain bias comes from a single rechargeable 6 V lead acid battery. The gate bias ranges from 0 V to 70 V and is provided by up to six rechargeable 12 V lead acid batteries connected in series. Multi-turnable 2 W potentiometers are used to tune the applied biases, 100 Ω in the source-drain biasing circuit and 1 kΩ in the gate biasing circuit.

Figure 20: Lakeshore test setup. Nano-Device Laboratory, UC Riverside, 2013.

Signal from the drain of the DUT goes to the low-noise preamplifier (model SR560) via co-axial cables to a dynamic signal analyzer (model SR785). On the low-noise preamplifier, the AC coupling mode with a differential input source of A-B are selected. Gain is set at 100. The settings of the dynamic signal analyzer may be controlled directly from the equipment control panel or via a Labview program. The measurements are broken up into smaller bandwidths to improve frequency resolution and to reduce the noise floor of the measurement (there is less noise power in a narrower bandwidth). The start frequency and span sets are defined in intervals as follows: [1 Hz - 90 Hz], [100 Hz - 1,600 Hz], [1,600 Hz - 14,000 Hz], [14,000 Hz - 39,000 Hz], [39,000 Hz - 89,000 Hz].

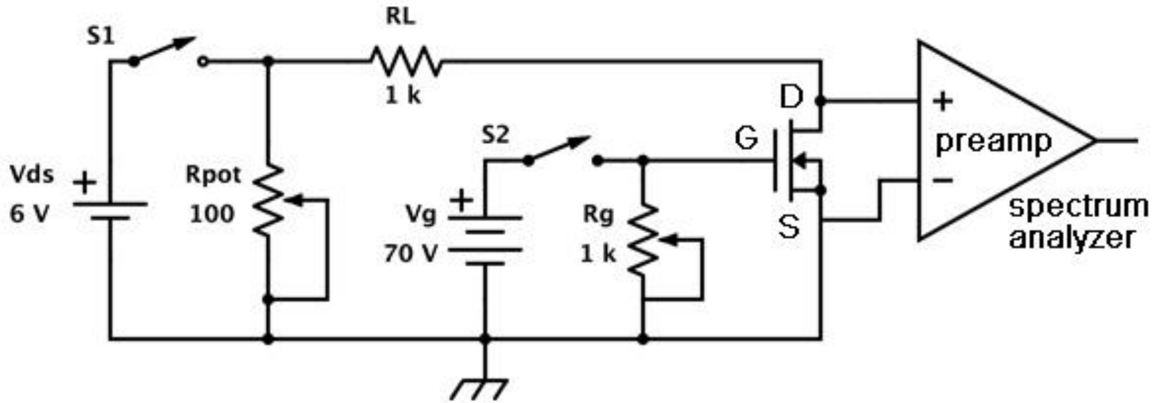


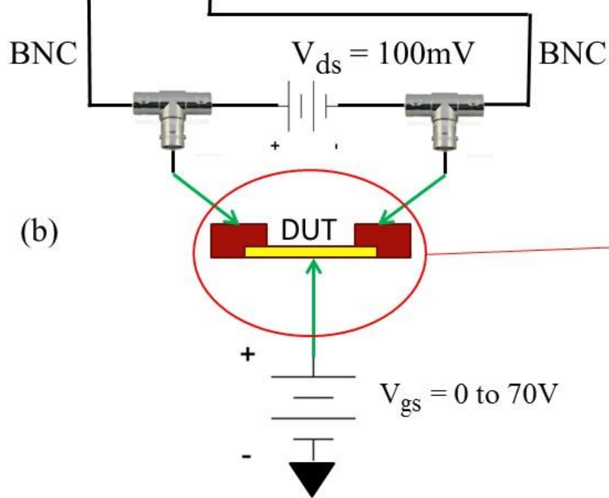
Figure 21: Biasing circuit for device under test (DUT).

Prior to performing noise measurements, an Agilent (4142B) Modular DC Source/Monitor was used to verify the functionality of the fabricated devices with I-V measurements. Allowing a pause (of approximately 1-2 minutes) between measurements seemed to produce device results with more consistent threshold voltages. The spectrum analyzer will measure voltage fluctuations on the drain. The output from the spectrum analyzer is in V^2/Hz which is power spectral density, S_v. The amplitude of the voltage fluctuations depends on the load resistance. Therefore, the so called short circuit current fluctuations are calculated. This is then normalized to current S_I, as defined in equation (1).

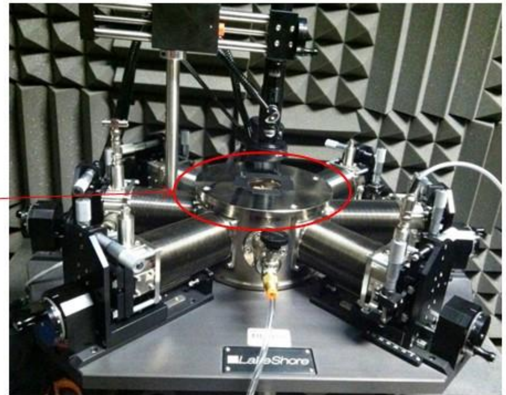
$$S_I = S_V \left(\frac{R_L + R_D}{R_L \cdot R_D} \right)^2 \tag{1}$$

S_I is the short circuit current noise. S_V is the measured voltage fluctuations. R_d is the device under test differential resistance. R_L is the load resistance.

(a) Low-noise Preamplifier (SR560)



(d) Lakeshore Probe station



(c) Dynamic Signal Analyzer (SR785)

Figure 22: (a) Low-noise preamplifier (model SR560), (b) Connection to DUT, (c) Dynamic Signal Analyzer (model SR785), and (d) Lakeshore probe station with temperature controller. Nano-Device Laboratory, UC Riverside, 2013.

6.3 Model Description of Low-Frequency Noise

Noise by definition is a random fluctuation in an electrical signal characteristic of all electronic devices. There are several different types, but four of the fundamental ones are shot noise, flicker 1/*f* noise, thermal or Johnson-Nyquist noise, and generation-recombination noise. There are others like avalanche noise and burst noise, but these are derivatives of the fundamental four.

Noise is typically characterized by its frequency spectrum, amplitude distribution, and physical mechanism. Since the focus is on device performance, the source of noise is intrinsic to the device and every effort is made to eliminate the external sources from interfering with measurements. Once we are able to properly characterize intrinsic noise by these parameters and try to understand the possible physical mechanism behind them are we able to mitigate it by material selection and/or design. Noise spectrums were captured for several devices.

Recent data collected in NDL (Nano-Device Laboratory, UC Riverside, 2013) supports the McWhorter's theory that flicker noise is primarily a surface effect whose generation is caused by fluctuations in the number of carriers captured and released from surface states. This model has been the accepted low-frequency model for MOS transistors since its application by Christensson in 1968.[76] The data, however, does not support the bulk phenomenon proposed by Hooge's theory that conduction fluctuations, and hence 1/*f* noise, are the result of mobility fluctuations and not carrier concentration fluctuations.[77]

6.4 Noise Measurement Results

Reported here are the results of low-frequency ($1/f$, where f is frequency) noise measurements in MoS_2 field-effect transistors revealing relative contributions of the MoS_2 channel and the Ti/Au contacts to the overall noise level. The investigation of the $1/f$ noise was performed for both as fabricated and aged transistors. It was established that the McWhorter model of the carrier number fluctuations describes well the $1/f$ noise in MoS_2 transistors, in contrast to what is observed in graphene devices. The trap densities extracted from the $1/f$ noise data for MoS_2 transistors, are 2×10^{19} $eV^{-1}cm^{-3}$ and 2.5×10^{20} $eV^{-1}cm^{-3}$ for the as fabricated and aged devices, respectively. It was found that the increase in the noise level of the aged MoS_2 transistors is due to channel rather than contact degradation. The obtained results are important for proposed electronic applications of MoS_2 and other van der Waals materials.

6.4.1 Introduction

Recent advances in the exfoliation and growth of two-dimensional (2D) layered materials have allowed for investigation of their electronic and optical properties.[78-81] Among these material systems, molybdenum disulfide (MoS_2) is one of the more stable layered transition-metal dichalcogenides (TMDCs).[82,83] Each layer of MoS_2 consists of one sub-layer of molybdenum sandwiched between two other sub-layers of sulfur in a trigonal prismatic arrangement.[84] Single-layer MoS_2 has a direct band gap of approximately 1.9 eV, while bi-layer and bulk MoS_2 exhibit an indirect band gap of ~1.6 eV and ~1.3 eV,

respectively.[85-87] It has been demonstrated that bi- and few-layer MoS_2 devices are promising for sensing, optoelectronic, and energy harvesting applications.[88-90] Owing to its relatively large energy band gap, MoS_2 field-effect transistors (FETs) offer reasonable on-off ratios, which suggests possibilities for digital or analog electronic applications of this 2D *van der Waals* material.[90,91]

Like other material systems, practical applications of MoS_2 devices in sensing and in digital or analog electronics are only possible if the material and devices meet the minimum level requirements for low-frequency $1/f$ noise.[92-100] The sensitivity of amplifiers and transducers used in sensors is ultimately defined by the flicker ($1/f$) noise.[100] The accuracy of a system limited by $1/f$ noise cannot be improved by extending the measuring time, t, because the total accumulated energy of the $1/f$ noise increases at least as fast as the measuring time t. In contrast, the system accuracy limited by white noise, e.g. shot or thermal noise, increases the measuring time as $t^{1/2}$. For this reason, the sensitivity and selectivity of many types of sensors, particularly those that rely on electrical response, is limited by $1/f$ noise. Although $1/f$ noise dominates the noise spectrum only at low frequencies, its level is equally important for electronic applications at high frequencies, because $1/f$ noise is the major contributor to the phase noise of the oscillating systems. The up-conversion of $1/f$ noise is a result of unavoidable non-linearity in devices and the electronic systems, which leads to phase noise contributions.

Meeting the requirements for $1/f$ noise level could be particularly challenging for 2D materials, where the electrons in the conducting channels are ultimately exposed to the charged traps in the gate dielectrics and substrates.[101] The contributions of contacts to the

low-frequency noise can also be significant owing to imperfection of the technology for metal deposition on TMDCs. Investigations of the low-frequency 1/*f* noise in MoS_2 devices are in its infancy,[102-104] and many questions regarding the specific physical mechanism of 1/*f* noise in this material remained unanswered, including the role of metal contacts and aging. The nanometer-scale thickness of the device channel may change the noise level compared to devices with conventional feature sizes.[96-101] These issues were addressed with a focus on separating the contributions from the MoS_2 channel and Ti/Au contacts to the overall noise level. The devices selected for this study used bi-layer and tri-layer MoS_2 films, because they are more robust for practical electronic applications.

6.4.2 Device Fabrication

Thin films of MoS_2 were exfoliated from bulk crystals and transferred onto Si/SiO_2 substrates following the standard "graphene-like" approach.[105-107] The thickness *H* of the films ranged from bi-layer to a few layers. Micro-Raman spectroscopy (Renishaw InVia) verified the crystallinity and thickness of the flakes after exfoliation. It was performed in the backscattering configuration under λ=488-nm laser excitation laser using an optical microscope (Leica) with a 50× objective. The excitation laser power was limited to less than 0.5 mW to avoid local heating. In Figure 23, informative bands exist at ~382.9 cm^{-1} (E^1_{2g}) and 406.0 cm^{-1} (A_{1g}), consistent with previous reports of MoS_2 Raman spectra.[108] Analysis of the Raman spectrum indicates that this sample is a tri-layer MoS_2 film. The latter follows from the frequency difference, $\Delta\omega$, between the E^1_{2g} and the A_{1g} peaks. The increase in the number of layers in MoS_2 films is accompanied by the red shift of the E^1_{2g}

and blue shift of the A_{1g} peaks.[108] This sensitivity of the Raman spectral features of MoS_2 to the film thickness was used to reliably determine the thickness of the samples used for fabricating FETs.

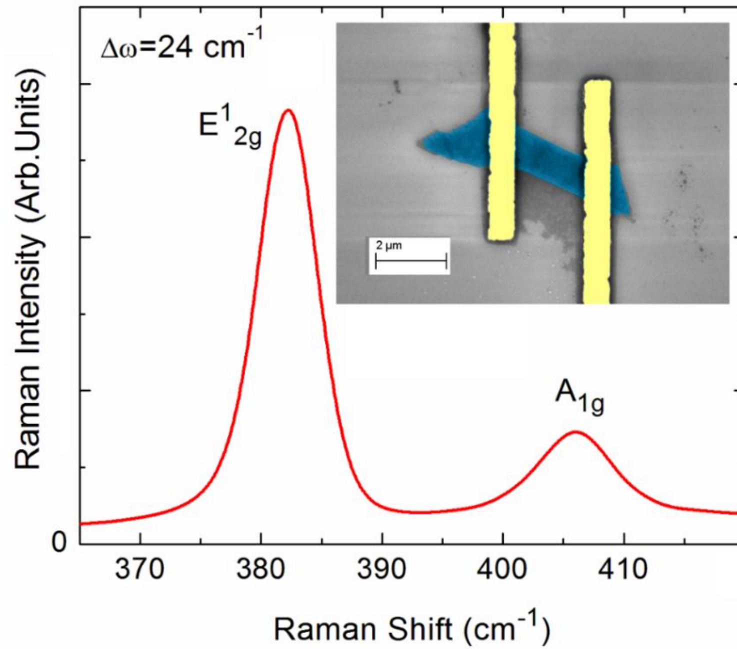


Figure 23: Raman spectrum of an MoS_2 thin film showing the E^1_{2g} and the A_{1g} peaks. The increase in the number of layers in MoS_2 films is accompanied by the red shift of the E^1_{2g} and blue shift of the A_{1g} peaks. The energy difference, $\Delta\omega$, between E^1_{2g} and the A_{1g} peaks indicates that the given sample is a tri-layer MoS_2 film. Inset shows an SEM image of a representative MoS_2 – Ti/Au field-effect transistor. The pseudo colors are used for clarity: yellow corresponds to the metal contacts while blue corresponds to MoS_2 thin-film channel. The data is after J. Renteria, R. Samnakay, S. L. Rumyantsev, C. Jiang, P. Goli, M. S. Shur, and A. A. Balandin, "Low-Frequency 1/*f* Noise in MoS_2 Transistors: Relative Contributions of the Channel and Contacts", *Appl. Phys. Lett.* (under review).

Devices with MoS_2 channels were fabricated using electron beam lithography (LEO SUPRA 55) for patterning of the source and drain electrodes and electron-beam evaporation (Temescal BJD-1800) for the metal deposition. Conventional Si substrates with 300-nm thick SiO_2 layers were spin coated (Headway SCE) and baked consecutively

with two positive resists: first, methyl methacrylate (MMA) and then, polymethyl methacrylate (PMMA). These devices consisted of MoS_2 thin-film channels with Ti/Au (10-nm / 100-nm) contacts. The heavily doped Si/SiO_2 wafer served as a back gate. Inset in Figure 23 shows a scanning electron microscopy (SEM) image of representative MoS_2 – Ti/Au devices. The majority of the bi-layer and tri-layer thickness devices had a channel length, *L*, in the range from 1.3 μm to 3.5 μm, and the channel width, *W*, in the range from 1 μm to 7 μm.

6.4.3 Electrical and Mobility Characteristics of MoS_2 Devices

Figure 24 (a-c) shows the room-temperature (RT) current-voltage (I-V) characteristics of the fabricated MoS_2 devices. Figure 24 (a) presents repeated sweeps of the source-drain voltage in the range from -0.1 V to +0.1 V. The linear I-V characteristics suggest that the MoS_2 – Ti/Au contacts are Ohmic. Figures 24 (b) and (c) show the drain-source current, I_{ds}, as a function of the back-gate bias, V_g, in the semi-log and linear scale, respectively. As seen, the device behaves as an *n*-channel field effect transistor. The curves of different colors correspond to the source-drain bias, V_{ds}, varying from 10 mV to 100 mV. As seen from Figure 24 (b), a representative device reproducibly reveals a well-defined threshold voltage, V_{th}=(-7) – (-8) V obtained from the linear extrapolation of I_d versus V_g characteristics (in the linear scale). The threshold voltage varied from device to device depending on channel size. It steadily shifted more negative as a result of aging. The current

on/off ratio greater than 6.6×10^3 was determined at a drain-source bias of 80 mV. We deduced a subthreshold slope of 549 $mVdec^{-1}$ at the bias of V_{ds} = 100 mV. The mobility values for these devices were in the range of 1 - 8 cm^2/Vs, which are typical for similarly fabricated MoS_2 FETs.[88,91,109-111]

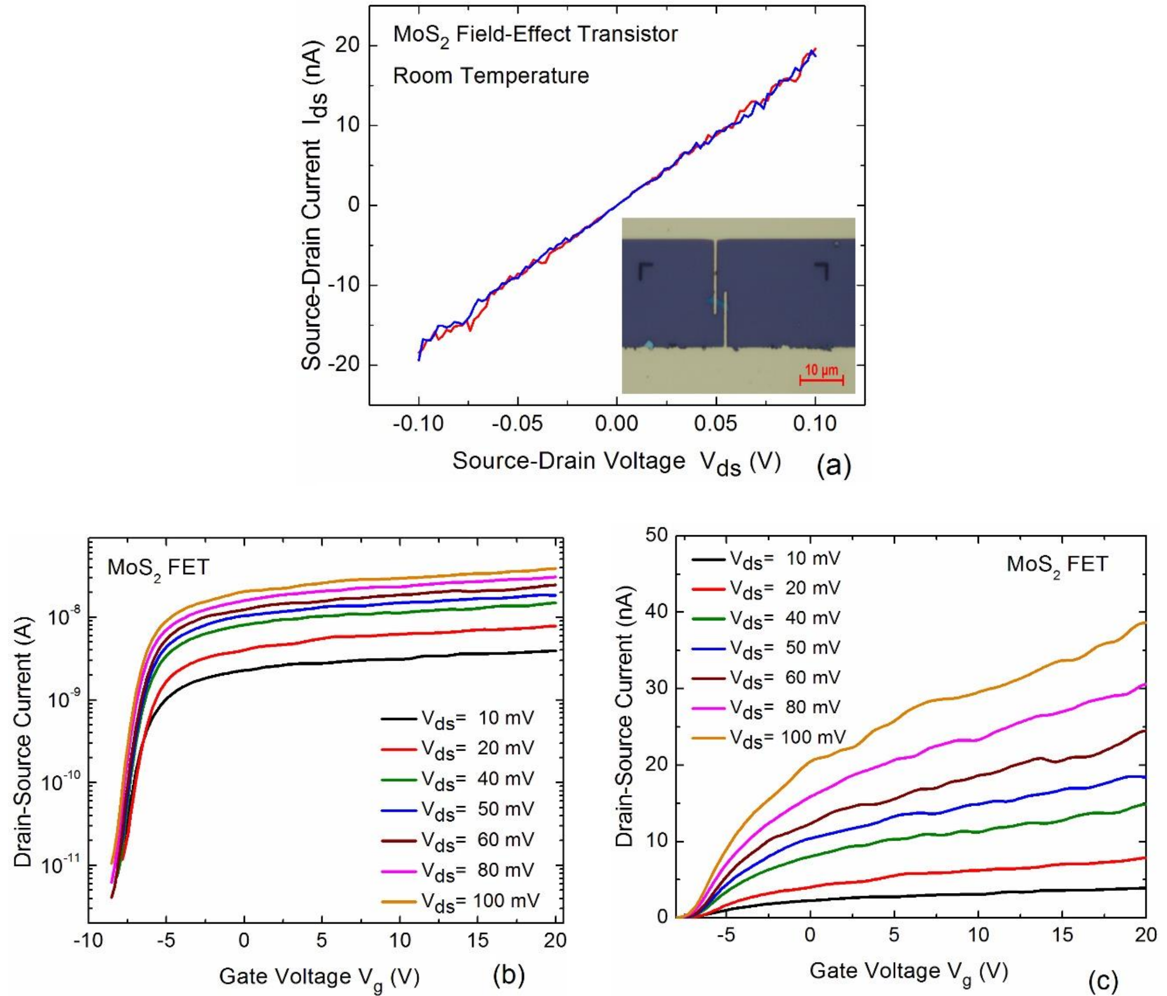


Figure 24: (a) Current-voltage characteristics of the fabricated MoS_2 FET at room temperature. The drain-source current for repeated sweeps of the source-drain voltage in the small-voltage range between -0.1 V and +0.1 V at V_g=0 V. (b) The drain-source current, I_{ds}, shown as a function of the back-gate bias, V_g, in the semi-log (c) and linear scale. The data is after J. Renteria, R. Samnakay, S. L. Rumyantsev, C. Jiang, P. Goli, M. S. Shur, and A. A. Balandin, "Low-Frequency 1/*f* Noise in MoS_2 Transistors: Relative Contributions of the Channel and Contacts", *Appl. Phys. Lett.* (under review).

In Figure 25 we compare the transfer I-V characteristics and calculated effective mobility for as fabricated and aged transistors. Aging results in the threshold voltage shift from V_{th}=-7 V to V_{th}= -7.5 V and a current increase at high gate voltages. A rough estimate for the total contact resistances, R_C, can be obtained by plotting the drain-to-source resistance, R_{ds}, versus $1/(V_g-V_{th})$, and extrapolating this dependence to zero as shown in the inset to Figure 25. For this particular device, the procedure yields the contact resistance of $R_C \approx 2$ MΩ and $R_C \approx 1.5$ MΩ for as fabricated and aged devices, respectively. The contact resistance, R_C extracted from the intercepts in the inset to Figure 25 was used for the effective mobility calculation:[112]

$$\mu_{eff} = \frac{L_g}{C_{OX}(R_{ds} - R_C)(V_g - V_{th})W}. \quad (1)$$

Here $C_{OX} = \varepsilon_o \varepsilon_r / d$ = 1.15 $\times 10^{-4}$ (F/m^2) is the oxide capacitance, where ε_o is the dielectric permittivity of free space, ε_r is the dielectric constant and d is the oxide thickness. We used ε_r=3.9 and d=300 nm for the SiO_2 layer. As seen from Figure 25, the extracted effective mobility is virtually the same for virgin and aged devices, and only weakly depends on the gate voltage.

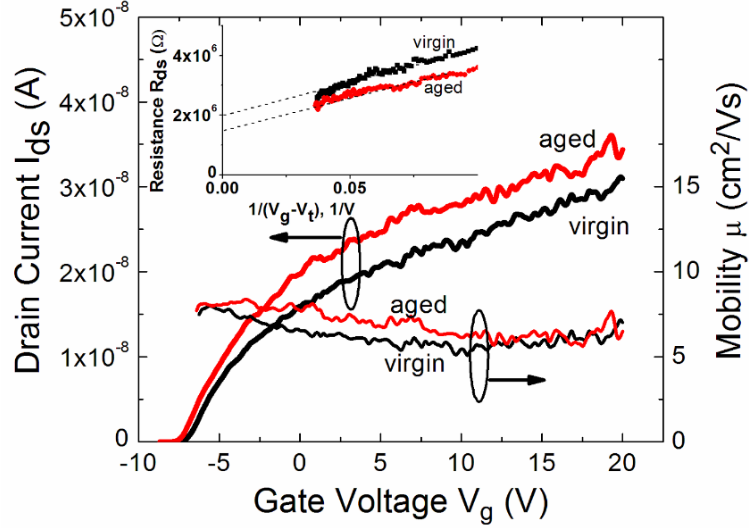


Figure 25: Transfer current-voltage characteristics and effective mobility for as fabricated and one week aged transistors at V_d=80 mV. The inset shows the plot of the total drain to source resistance versus $1/(V_g-V_{th})$ used for contact resistance estimate. The data is after J. Renteria, R. Samnakay, S. L. Rumyantsev, C. Jiang, P. Goli, M. S. Shur, and A. A. Balandin, "Low-Frequency 1/*f* Noise in MoS_2 Transistors: Relative Contributions of the Channel and Contacts", *Appl. Phys. Lett.* (under review).

6.4.4 Low-Frequency 1/*f* Noise Characteristics

Noise was measured in the linear region at V_d=50 mV keeping the source at the ground potential. Voltage fluctuations from the drain load resistance of R_L=50 kΩ were analyzed with a dynamic signal analyzer (SR785). Measurements were conducted under ambient conditions at room temperature. Figure 26 shows typical low-frequency noise spectra of voltage fluctuations, S_v, as a function of frequency for several values of drain-source and gate biases. One can see that the low-frequency noise is of the 1/*f* type without any signatures of generation-recombination bulges. To verify how closely the noise spectral density follows 1/*f* dependence, the experimental data was fitted with $1/f^{\alpha}$. The

parameter α varied in the range from ~0.75 to ~1.25 without revealing any clear gate bias, V_g, dependence. The latter suggests that the traps contributing to the noise distributed uniformly in space and energy.[100]

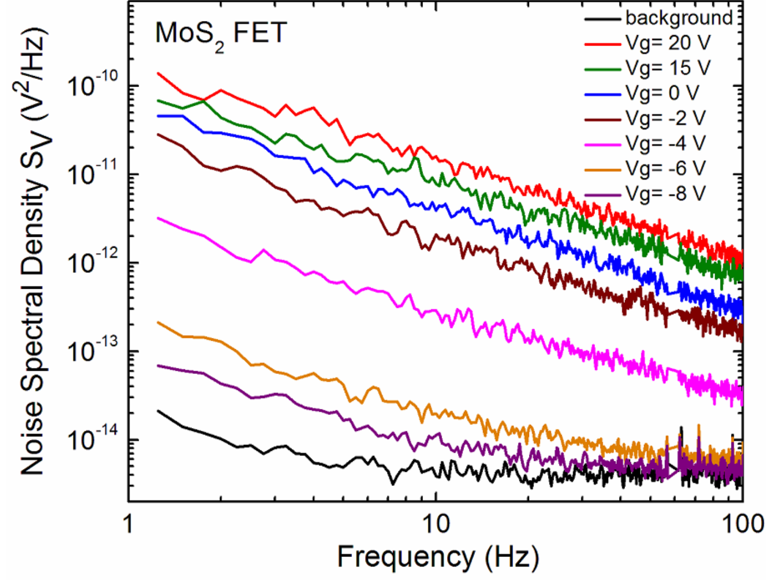


Figure 26: Typical low-frequency noise spectra of voltage fluctuations, S_v, as a function of frequency f for different values of the gate bias. The data is for the linear regime at V_d=50 mV and the source contact at a ground potential. The measurements were conducted under ambient conditions at room temperature. The data is after J. Renteria, R. Samnakay, S. L. Rumyantsev, C. Jiang, P. Goli, M. S. Shur, and A. A. Balandin, "Low-Frequency 1/*f* Noise in MoS_2 Transistors: Relative Contributions of the Channel and Contacts", *Appl. Phys. Lett.* (under review).

For any new material technology it is important to analyze the relative contributions of the device channel and contacts as well as to assess the effects of aging. To accomplish this goal, we calculated the short-circuit current fluctuations in the usual way as $S_I=S_v[(R_L+R_{ds})/(R_LR_{ds})]^2$, where R_L and R_D are the load and device resistances, respectively. The noise spectrum density at different drain-source biases was consistently proportional to the current squared at a constant gate voltage V_g: $S_I \sim I_{ds}^2$. The latter implies

that the current does not drive the fluctuations but merely makes the fluctuations in the sample visible via Ohm's law.[96] The noise was measured in the same devices within the span of two weeks. As a result of aging, the threshold voltage shifted to a more negative value and total drain to source resistance decreased. The circular symbols in Figure 27 represent the normalized current noise, S_I/I_{ds}^2, as a function of the gate bias for the as fabricated device and device aged for a week in ambient atmosphere (Transfer current voltage characteristics of these devices are shown in Figure 25). One can see that the normalized noise spectral density is an order of magnitude larger in the week old device. The latter suggests that capping of MoS_2 with some protective layer may be a technologically viable way for reducing 1/*f* noise for practical applications.

Let us now investigate the relative contribution of the metal contacts and device channels to the overall level of 1/*f* noise. This issue is of particular importance for MoS_2 devices due to the fact that the technology of metal contact fabrication to TMDCs is still rudimentary. Since the contact resistance is not negligible we consider that both the metal contact and MoS_2 channel contribute to the measured noise. In this case, we can write that[100]

$$\frac{S_I}{I_{ds}^2} = \frac{S_{RCH}}{R_{CH}^2}\frac{R_{CH}^2}{\left(R_{CH}+R_C\right)^2} + \frac{S_{RC}}{R_C^2}\frac{R_C^2}{\left(R_{CH}+R_C\right)^2}\,. \quad (2)$$

Here S_{RCH}/R_{CH}^2 is the noise spectral density of the channel resistance fluctuations, R_{CH} is the resistance of the channel, R_C is the contact resistance, and S_{Rc}/R_C^2 is the noise spectral density of the contacts resistance fluctuations.

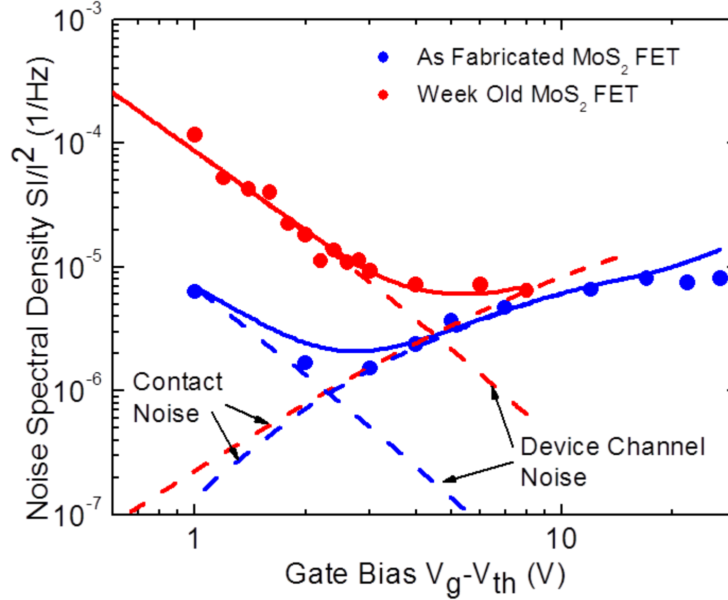


Figure 27: Measured and simulated low-frequency noise response of MoS_2 FETs. The circular symbols represent the experimental data points for the normalized current noise spectral density, S_I/I_{ds}^2, as a function of the gate bias for the as fabricated device (blue symbols) and device aged for a week under ambient conditions (red symbols). The normalized noise spectral density is an order of magnitude larger in the week old device. The dashed lines represent the model fitting for the noise dominated by the channel contribution and, separately, by the contact contribution. The solid lines show the sum of both contributions. The agreement between the theoretical fitting and experimental data indicate that the 1/*f* noise in MoS_2 FETs follow the carrier number fluctuation model. The data is after J. Renteria, R. Samnakay, S. L. Rumyantsev, C. Jiang, P. Goli, M. S. Shur, and A. A. Balandin, "Low-Frequency 1/*f* Noise in MoS_2 Transistors: Relative Contributions of the Channel and Contacts", *Appl. Phys. Lett.* (under review).

Assuming that the channel noise complies with the McWhorter carrier number fluctuation model, we can write for the noise spectral density, S_{RCH}/R_{CH}^2, the following equation[92,97]

$$\frac{S_{RCH}}{R_{CH}^2} = \frac{kTN_t}{\gamma fWLn_s^2}, \tag{3}$$

where k as the Boltzmann constant, T is the temperature, γ is the tunneling parameter taken to be γ=10^8 cm^{-1}, n_s is the channel concentration, and N_t is the trap density. In the strong inversion regime, the concentration n_s can be estimated as $n_s=C_{ox}(V_g-V_{th})/q$. Since the total resistance, $R_{CH}+R_C$, was measured directly, and contact resistance can be extracted from the current voltage characteristics there are just two fitting parameters in our analysis, N_t, S_{RC}/R_C^2.

In Figure 27, we show with the dash lines the model fitting for the noise dominated by the channel contribution and, separately, by the contact contribution (i.e. the first term and the last term in Eq. (1), respectively). The solid lines show the sum of both contributions. The fitted values of the contact noise were determined to be $S_{RC}/R_C^2=0.25\times10^{-4}/f$, and $0.5\times10^{-4}/f$ for the as fabricated and aged devices respectively (with the contact resistances R_C=2 MΩ and R_C=1.5 MΩ for the as fabricated and aged devices, respectively). The extracted trap densities are $N_t=2\times10^{19}$ eV^{-1}cm^{-3} and $N_t=2.5\times10^{20}$ eV^{-1}cm^{-3} for as fabricated and aged samples, respectively. The uncertainty in the trap density estimation is close to 20% (due to the inaccuracy of the contact resistance estimate which we varied within the range 1.3-2.2 MΩ for both as fabricated and aged devices). The agreement of the model fitting (Eq. (2) and Eq. (3)) with the experimental results indicates that the *a priori* assumption of the McWhorter model description was valid. The model description allows one to clearly distinguish the contributions to the noise from the MoS_2 channel and from the metal contacts. The absolute value of the trap density extracted is within the range found in MoS_2-based transistors by other methods.[110,113]

Let us now compare the noise mechanism in MoS_2 thin-films with that in conventional semiconductors, metals and graphene devices. It is known that 1/*f* noise is either due to the mobility fluctuations or the number of carriers fluctuations. In conventional semiconductor devices, such as Si complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs), 1/*f* noise is described by the McWhorter model,[92] which is based on the carrier-number fluctuations. In metals, on the other hand, 1/*f* noise is usually attributed to the mobility fluctuations.[96] There are materials and devices where contributions from both mechanisms are comparable or cross-correlated. By assuming the McWhorter model for the MoS_2 channel noise we were able to successfully reproduce the overall noise gate-bias dependence in MoS_2 FETs. The latter indicates that the 1/*f* noise mechanism in MoS_2 FETs is similar to that in conventional Si CMOS transistors: carrier number fluctuations with the traps widely distributed in space and energy. It is important to note here such 1/*f* noise behavior is quite different from that of another important 2D material, graphene, where the gate voltage dependence of noise does not follow the McWhorter model.[92] It was shown that 1/*f* noise in graphene can be more readily described by the mobility fluctuation.[101] The latter was concluded on the basis of analysis of the gate bias dependence,[114-116] effect of electron beam irradiation damage,[117] noise scaling with the thickness[118,119] and measurements of noise in graphene devices under magnetic field.[120]

There is another important observation from the experimental data and model fitting presented in Figure 27. The amplitude of noise and corresponding trap density in the MoS_2 channel increased more than an order of magnitude as a result of aging.

Meanwhile, the contact noise only slightly increased and contact resistance even decreased in the aged device. Therefore, we can conclude that aging results mainly from the deterioration of the MoS_2 channel. Contrary to our observations, the studies of the low-frequency noise in a single-layer exfoliated MoS_2 device[102] and a few-layer CVD grown MoS_2 device[103] revealed the compliance of the noise behavior with the Hooge empirical relation. On the other hand, transistors based on the multilayer exfoliated MoS_2 structures revealed the McWhorter mechanism of noise in the accumulation mode.[104] At this point, it is not clear if these discrepancies in the noise mechanism interpretations are due to the different number of layers in the tested devices or different fabrication technology and quality of the device structures.

6.5 Summary

In conclusion, results of low-frequency noise investigations in MoS_2 FETs with Ti/Au contacts were reported. It was established that both the channel and contacts contribute to the overall $1/f$ noise level of the as fabricated and aged transistors. The intrinsic noise characteristics in MoS_2 devices are well described by the McWhorter model relating to carrier number fluctuations, in contrast to graphene devices. It was found that the increase in the noise level in aged MoS_2 transistors is due to channel rather than contact degradation. The obtained results can be used for the optimization of devices with channels implemented with MoS_2 and other van der Waals materials.

Chapter 7

Conclusions

In this dissertation I reported results from the fabrication and testing of three-terminal devices with all-metallic tantalum diselenide ($TaSe_2$) and molybdenum disulfide (MoS_2) thin-film conducting channels. The "graphene-like" exfoliation process was used to prepare thin films of $TaSe_2$ and MoS_2. These films were utilized as the channel layers in three-terminal devices with Ti/Au or pure Au metal contacts. For the proof-of-concept demonstration of 2H-$TaSe_2$ devices, layers of 2H-$TaSe_2$ were exfoliated mechanically from single crystals grown by the chemical vapor transport method. These devices were then characterized for their electrical performance at a range of temperatures. MoS_2 devices were similarly prepared also from single crystals and characterized with additional analyses of their low-frequency 1/*f* noise characteristics.

$TaSe_2$ devices with nanometer-scale channel thicknesses exhibit strongly non-linear current-voltage characteristics, unusual optical responses, and electrical gating at room temperature. Measurements demonstrated expected nonlinear I-Vs of this CDW material. However, they yielded surprisingly similar results at room temperature and

equally surprising optical responses contrary to typical optoelectronic materials.[121] It is speculated that such anomalous results can be applied to novel photo detection sensor technologies. It was also demonstrated that electrically-gated devices with strong non-linear current-voltage (I-V) characteristics can be based on thin films of metallic *van der Waals* materials. The drain-source current in thin-film 2H-$TaSe_2$–Ti/Au devices reproducibly undergoes an abrupt transition from a highly resistive to a highly conductive state, within which the threshold is tunable by the gate voltage. The combination of such current-voltage characteristics with all-metallic components may be ideal for the implementation of radiation-hard all-metallic logic circuits, among other applications.

In MoS_2 devices, results of low-frequency noise investigations with Ti/Au contacts were reported. It was established that both the channel and contacts contribute to the overall $1/f$ noise level of the as fabricated and aged transistors. The intrinsic noise characteristics in MoS_2 devices are well described by the McWhorter model relating to carrier number fluctuations, in contrast to graphene devices. It was found that the increase in the noise level in aged MoS_2 transistors is due to channel rather than contact degradation. Results obtained from both $TaSe_2$ and MoS_2 devices open up a new application space in or optimization for thin films of van der Waals materials.

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