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Santa Barbara

In-situ Oxide, GaN interlayer based vertical trench MOSFET (OG-FET)

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

Chirag Gupta

Committee in charge:

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June 2018

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June 2018

In-situ Oxide, GaN interlayer based vertical trench MOSFET (OG-FET)

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by

Chirag Gupta

DEDICATION

This dissertation is dedicated to my grandparents, Srinath Gupta, Sukhi Devi, Kishanlal Ji Mor and Bansi Devi

ACKNOWLEDGEMENTS

My academic and non-academic experience at UCSB would not have been possible without the support and help from a lot of people. I would like to take this opportunity to express my gratitude towards them.

First and foremost, I would like to express my thanks and gratitude to my advisor Prof. Umesh K. Mishra for accepting me as a graduate student in his research group. Umesh is an ideal advisor for a graduate student. He allows his students to work on challenging and technologically relevant problems while providing a great deal of guidance and support. I especially admire his optimism, pragmatism, dedication and faith in his students.

I would like to thank rest of my committee. Stacia Keller was practically a second advisor to me. Her expertise in MOCVD growth helped tremendously in developing MOCVD regrowth for the OG-FET. I am extremely grateful to her for taking time and patiently answering my questions and explaining growth processes. I owe all my understanding pertaining to materials to her. Also, her contribution and encouragement in publishing scientific results has been of great help. I would also like to thank Prof. Steven DenBaars, Prof. Bob York and Dr. Yifeng Wu for their critical feedback and guidance. Especially, Prof. Denbaars for providing constructive and useful comments during SSLEEC practice talks and annual reviews.

Apart from my committee members, I would like to thank our collaborators on ARPA-E SWITCHES program, Prof. Srabanti Chowdhury and her research group. The shared enthusiasm for vertical GaN devices and close collaboration resulted in numerous insightful, interesting and fun conversations.

I thank the funding agencies for this project, ARPA-E SWITCHES program monitored by Dr. Timothy Heidel and Dr. Isik Kizilyalli, SSLEEC and UC Solar. The ARPA-E quarterly reviews helped me in checking my progress and are to some extent responsible for timely completion of my dissertation work.

Next, I would like to thank my colleagues in Mishra group with direct contribution towards this dissertation work. Anchal and Silvia, for growing a ton of material for vertical devices. It was fun developing OG-FETs with your support and learning a little bit about growth as well. Thank you Silvia for such a cool device name. Matt L., Cory, Haoran, Niru, Ryo, and Yuuki for providing the support with growths. Dong, for fabricating large area OG-FETs and pushing OG-FET further. Onur, for all the help with FIBs. Yuuki and Yusuke, for introducing and involving me into projects outside my thesis work. It has been a great learning experience. Geetak, thank you for training me in the cleanroom and all the help with understanding device physics. Matt Guidry, Davide and Jeffery Haller (Transphorm) for helping me out with measurements and Brian Romanczyk for all the help regarding process development. My interns Anna, Eugene, Jq and Will for performing a ton of measurements.

I would like to thank the remaining Mishra group members (Aditya, Athith, Christian, Elaheh, Jeong, Jing, Karine, Matt L., Maher, Pawana, Ramya, Shalini, Steven, Takuro, Trey, Shubhra, Weiyi, Xiang, Xun) for providing a great support system and a lively workplace. I would especially like to thank Steven for attending my wedding in India and all the fun conversations over the years. I thank all the past members of the Mishra group for creating a huge knowledge base which has enabled this work.

I thank the UCSB Nanofab staff for providing an excellent, up and running cleanroom facility. I would like to thank Val and Yukina for all the paperwork related to ECE and SSLEEC respectively.

Outside Mishra group, my friends (Abhishek, Akhilesh, Anusha, Anchal S., Arjun, Ekta, Guru, Tanya, Tanmoy, Sagar, Udbhav and many more) and my room-mates (Geetak, Advait, Anant, Anirudha, Prashansa, Hsin-Ying) provided great company and helped me through the grind of grad school.

I thank my parents (Shivraj Guptra and Usha Gupta) and sister (Paridhi Gupta) for all the support and inspiration.

Finally, I would like to thank my wife Shubhra for all the unconditional love, encouragement and support. I consider myself extremely fortunate to have you as a colleague, friend and life partner. I love you.

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ABSTRACT

In-situ Oxide, GaN interlayer based vertical trench MOSFET (OG-FET)

by

Chirag Gupta

The surge in world-wide energy consumption places a growing need for highly efficient power electronics for generation, transportation, and utilization of electricity. With the advent of new markets such as electric vehicles, PV solar inverters, the market for these power electronics components is predicted to reach $15 billion by 2020. Silicon-based devices are most commonly used in traditional power electronics applications, however, wide bandgap semiconductors such as gallium nitride (GaN) are more efficient and thus, useful for future energy applications.

Consequently, Gallium Nitride (GaN) based power devices have gained increased attention in recent years. For 600 V class power devices, lateral GaN high electron mobility transistors are available today. However, it is generally considered that for high voltage/high current applications (>900V/100 A), vertical device structures might be more suitable owing to their capability of achieving lower specific on-resistance and high breakdown voltage simultaneously.

Amongst numerous vertical device structures, the trench MOSFET is an attractive device structure to reduce on-resistance due to the capability of high cell density and the absence of a JFET region. However, high channel resistance in trench MOSFETs due to poor electron mobility in the channel creates reliability issues as a higher gate bias needs to be applied to reduce the channel resistance.

In this dissertation work, we developed a novel device design (called OG-FET) to enhance the channel mobility and therefore, lower the channel-resistance for the trench MOSFET structure while maintaining normally-off operation and the same breakdown voltage. In OG-FET, a GaN interlayer is regrown followed by *in-situ* dielectric deposition via MOCVD on the n-p-n trenched structure to enhance the channel mobility. In addition, the *in-situ* gate-dielectric growth onto the GaN interlayer allows this device to achieve lower interface trap density compared to devices with *ex-situ* dielectrics deposited onto the trenched structure.

This thesis discusses the OG-FET device design, growth and fabrication process alongside device results and analysis. With sustained efforts, OG-FETs with high DC performance were achieved. The OG-FETs demonstrated threshold voltage between 1-4 V, breakdown voltage beyond 1 kV with a low on-resistance between 1.5-3 $m\Omega.cm^2$. The on-resistance values were achieved at a relatively low gate bias (~12 V-15 V) and low gate-dielectric field (~2-3 MV/cm) compared to conventional GaN trench MOSFETs.

These results are promising for the future application of OG-FETs for high voltage and high-power electronics.

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Chapter 1: Introduction

Electricity is fast becoming a necessity of human life. The pervasive utilization of electricity brings a large strain on non-renewable sources of energy which are the major source of electricity generation (as of now). Consequently, in the past decade, rapid advances have been made towards generation of electricity from renewable sources of energy. However, such technologies are still far from wide deployment. Therefore, efficient generation, transmission and utilization of electricity is of paramount importance.

Power generated at the base stations is not utilized as it is by the consumer. It needs to be converted multiple times from one form to another before it is finally consumed. These power conversion processes are not 100 % efficient and thus, incur losses. With increased system complexity, number of power conversion processes increases and total efficiency decreases. According to recent studies, approximately 10 % of the total generated electricity gets wasted due to these inefficient power conversion processes [1]. This inefficiency drives the need towards developing efficient power conversion processes.

At the heart of every power conversion process is a semiconductor switch/transistor. The performance of power semiconductor transistor drives the overall system design, cost and efficiency. Therefore, a power semiconductor device can be considered as the most basic and critical building block of a power system.

The most basic requirements of a power device are high breakdown voltage (V_{BR}) and low on-state resistance (R_{ON}) [2]. Together these characteristics allow for a highly efficient switch/transistor. There are few figures of merit (FOM) that are commonly used to benchmark power device performance [2]. One of the simplest FOM is V_{BR}^2/R_{ON}. The V_{BR} and R_{ON} of a

device are strongly related to the material properties of the semiconductor [2] used by the following relation known as Baliga's FOM,

$$\frac{V_{BR}^2}{4R_{ON}} = \mu_{bulk}\varepsilon_S E_C^3 \quad 1.1$$

here, μ_{bulk} is the bulk electron mobility, ε_S is the dielectric constant, and E_C is the critical electric field for breakdown. This result defines the one-dimensional material limit line on the transistor performance. However, using advanced device designs such as cool MOS or super-junction MOSFET, device performance can be pushed beyond this one-dimensional material limit [3].

Silicon (Si) has long been the preferred material choice for power semiconductor devices. However, akin to logic devices, Si power semiconductor devices are now rapidly approaching fundamental limits [4]. This has driven the need for alternative materials to satisfy ever growing demand for efficient power electronics. Consequently, in the past two decades, wide band gap (WBG) semiconductors have been actively pursued [4]. With superior material properties such as high breakdown field, high bulk mobility, high thermal conductivity etc., WBG semiconductors have the potential to improve the size, weight, efficiency, power density, current density, and high temperature reliability for the power conversion system. Such improvements could revolutionize the entire power system design. Table 1 shows the material properties of various WBG semiconductors and silicon [5]. Amongst WBG semiconductors, silicon carbide (SiC) and gallium nitride (GaN) have emerged as suitable candidates for next generation power electronics beyond Si. In addition, gallium oxide and diamond are being explored for future enhancements.

GaN and SiC based power devices are commercially available today [6]. Their performance is approximately 2-5 times higher than that of fundamental limit of Si. However,

Material	Breakdown field, E_C (MV/cm)	Bulk Mobility μ (cm^2/V-s)	Dielectric Constant (ε_S)	BFOM
Silicon	0.3	1400	11.8	1
4H-SiC	2.5	1000	9.7	340
GaN	3.3	1200	9	870
β-Ga_2O_3	8	300	10	3444
Diamond	10	2000	5.5	24664

Table 1.1 Material parameters of different semiconductors and BFOM

these material systems are relatively immature compared to Si and their performance is not yet close to one-dimensional material limit, therefore, with technological advances much higher performance can be expected in next few years.

Power devices can be fabricated using both lateral and vertical device structures. SiC based power devices were extensively explored using vertical device structures such as MOSFETs and JFETs. MOSFET device design is more suitable than JFET because (ideally) the MOSFET can be applied in a similar way as Si MOSFETs and IGBTs and is potentially more reliable than JFET. However, in SiC MOS devices, high MOS channel resistance was observed due to low inversion channel mobilities [6]. This limits the application of SiC MOS devices in low and medium power applications as channel resistance dominates the total on-resistance of the device. Although, for high voltage applications ($\geq$ 1200 V), drift resistance is either comparable or sufficiently larger than the channel resistance. Thus, allowing fundamental one-dimensional material limits to be approached in high voltage (> 1200 V) applications.

Unlike SiC, majority of GaN power device development was targeted towards lateral structures. AlGaN/GaN hetero-structure based high electron mobility transistors (HEMTs) becomes a natural choice because an AlGaN/GaN interface easily forms a highly conductive two-dimensional electron gas (2DEG) and offers very low sheet resistances. Consequently, lateral GaN HEMTs on Si are commercially available today for medium range power

conversion applications [7]. However, it is considered that for high voltage, high current applications (1200 V/100A), vertical structures might be more suitable [8], [9], [10], [11]. There are multiple reasons for the same. First, in a vertical device, the die area is weakly dependent on the breakdown voltage. Second, vertical devices hold the strong electric fields in the bulk rather than along the surface, resulting in lower trapping. Third, avalanche breakdown can be achieved in these devices. Fourth, relatively easier current extraction/wiring is possible due to the placement of the source and drain on vertically opposite sides and better thermal management.

Even in the presence of SiC vertical commercial devices, GaN vertical devices are worth exploring as the material properties of GaN are superior to that of SiC. The reason for slow progress of vertical GaN compared to SiC was lack of high quality native GaN substrates. In the past few years, research on p-n diodes have shown that the GaN substrate quality has significantly improved and these substrates can be applied for the fabrication of high voltage devices [12], [13]. Consequently, GaN power devices have been demonstrated with blocking voltages between 1-2 kV with low specific on-resistance and normally-off operation [10], [14], [15], [16], [17], [18]. Even though, these results are encouraging, however, to fully realize the potential of GaN vertical devices, significant research on multiple fronts still needs to be done.

1.1 Vertical GaN Devices

Numerous vertical GaN power transistors have been demonstrated in the past few years. Predominantly, vertical device structures can be divided into two broad device designs. The first type is a current aperture vertical electron transistor (CAVET) [9], [15], [16], [19]. The second type is a trench MOSFET device with a sidewall gate [10], [11], [14], [17], [18], [20], [21], [22].

1.1.1 CAVET Device Design

The CAVET device was first reported in 2000 by Yaacov *et al* [23]. However, the first report on CAVETs was targeted towards RF power applications for dispersion free device performance. Later, CAVET device design was explored for power switching applications by Chowdhury *et al* [9]. The CAVET device design to some extent is analogous to D-MOSFET which has been explored in Si and SiC. CAVET is a merged lateral-vertical device. Figure 1.1 shows the CAVET cross sectional schematic.

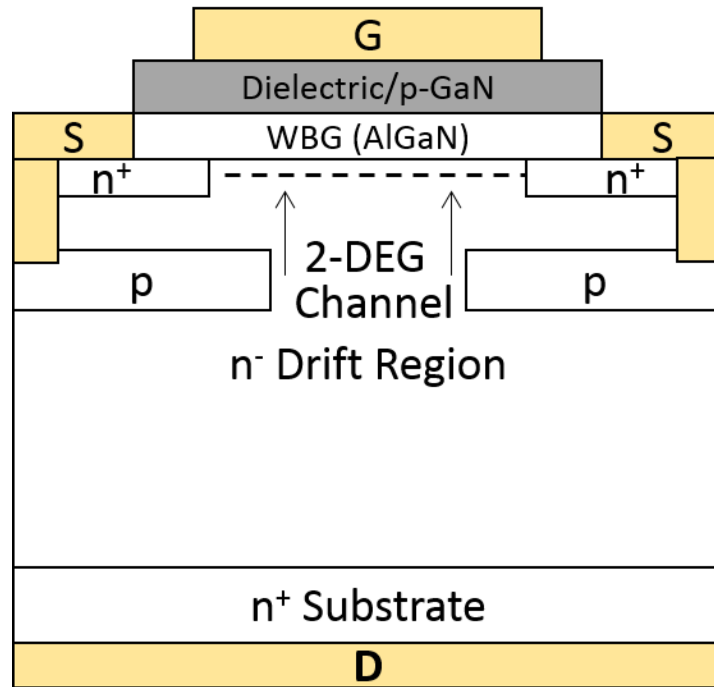


Figure 1.1 CAVET cross sectional schematic.

In CAVET, in the on-state, the flow of electrons is in lateral direction from the source through the channel which is modulated by planar gate. Then, electrons flow vertically through an aperture or JFET region into the drift region and are collected by the drain contact. This is illustrated in Figure 1.2. The design of conductance of the JFET or aperture region has a

considerable impact on device performance [24]. The total on-state resistance components are shown in the following equation,

$$R = R_S + R_{CH} + R_{JFET} + R_{DRIFT} + R_D \qquad 1.2$$

Here, R is the total resistance of the device extracted in the linear region. R_S, R_{CH}, R_{JFET}, R_{DRIFT}, R_D are the source, channel, JFET region or aperture, drift and drain resistances respectively. These resistance components are illustrated in Figure 1.3.

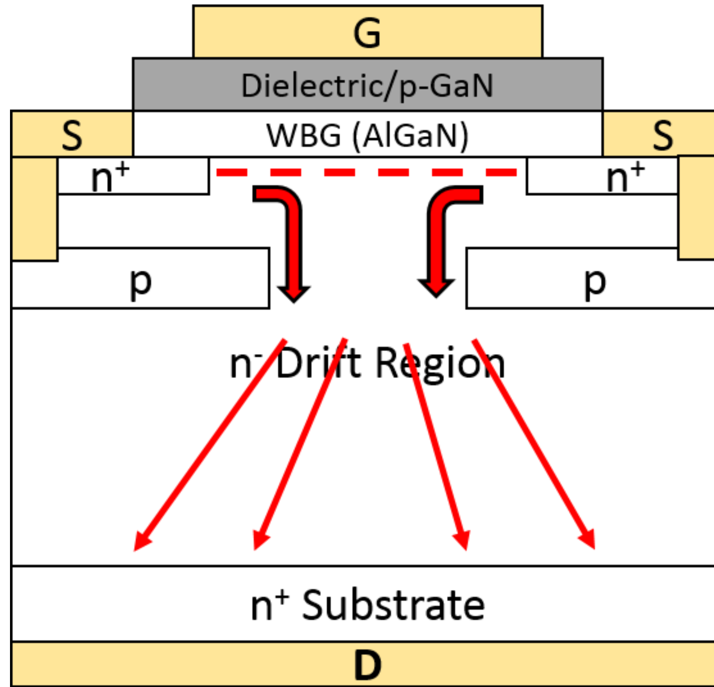


Figure 1.2 Flow of electrons in CAVET.

In high voltage vertical devices, R_S and R_D contribution to the total on-resistance is negligible. Also, due to the presence of highly conductive 2-DEG in CAVETs, the R_{CH} is also negligible compared to other resistances. Therefore, the major resistance components are R_{JFET} and R_{DRIFT}. The equation 1.2 can be approximated as,

$$R \sim R_{JFET} + R_{DRIFT} \qquad 1.3$$

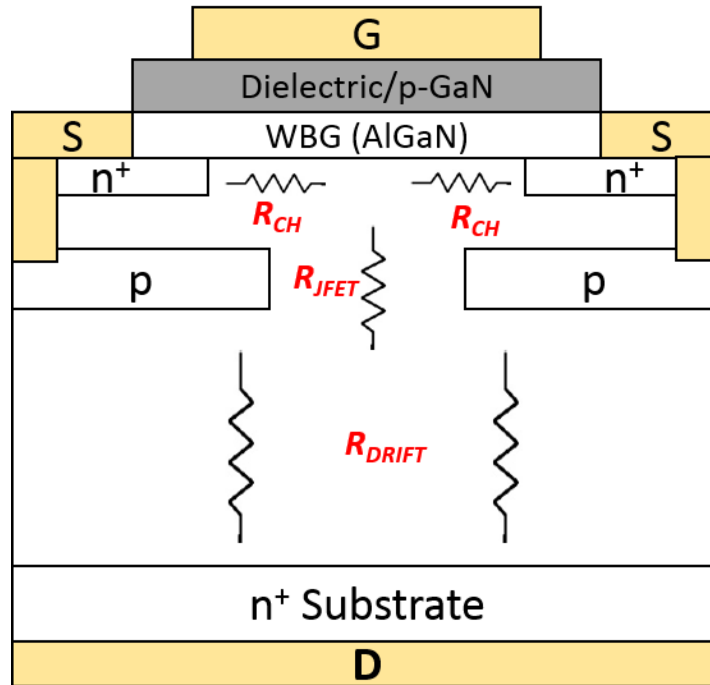


Figure 1.3 Major resistance contributions in a high voltage CAVET.

The drift resistance depends on the doping, mobility, and thickness of the drift region. Doping and thickness of the drift region determines the expected blocking voltage from the device. The conductivity of the JFET region determines the total on-resistance of the device. A resistive aperture can result in poor saturation of drain current with increasing drain voltage and can increase the on-resistance of the device. A conductive aperture can result in improved saturation behavior and device pitch can be reduced. However, higher doping in the aperture region would reduce the breakdown voltage of the device. Therefore, optimization of aperture or JFET region conductivity is of paramount importance in CAVETs.

Apart from aperture conductivity design, there are other challenges with the device design. One such aspect is the design of the current blocking layer (CBL). The CBL prevents the flow of electrons from source to drain both in the off-state and in the on-state. Ion implantation of Al and Mg have been used for the CBL [9], [25]. Ion implantation allows the planarity of the

region to be maintained for subsequent re-growths. However, in GaN, p-type ion implantation does not work as efficiently as it does in Si and SiC. Recent reports are showing improvement in p-type ion implantation, but its performance is still far from as grown p-type layers [26], [27]. As grown p-type layer on top of the drift region can also be used as CBL as demonstrated in first CAVET report. In this type of CBL device design, the aperture is formed by etching through the CBL followed by regrowth of the aperture. The re-growth within the trenched structure has proved to be challenging [24], [28]. However, recently, good device performance has been demonstrated by Nie *et al.* with regrown aperture [16].

Another challenge of CAVET device design is to achieve enhancement mode operation with MOS or MIS gate structure in Ga-Polar orientation (with AlGaN/GaN heterojunction). Since, the gate structure of CAVET is similar to lateral HEMT structure, achieving reliable normally-off operation in CAVET is almost equally challenging as AlGaN/GaN HEMTs. With use of a junction gate (p-GaN), normally-off devices can be achieved [16]. As mentioned in the previous section, like in SiC devices, MOSFET type gated structure will always be preferred over JFET gate. Therefore, achieving normally-off operation with a MOS/MIS gate is another big challenge of this device design.

1.1.2 Trench MOSFET Device Design

The trench MOSFET basic device design dates to early 1990s [29]. In Si, the trench MOSFET has grown into a 3-billion-dollar annual market [29]. Trench MOSFET device design has also been extensively explored in SiC. SiC trench MOSFETs are also commercially available today. The success of trench MOSFET device design in Si and SiC indicates that reliable MOSFET could be manufactured on a vertically etched sidewall. Trench MOSFET has also been explored in GaN alongside CAVET. The first GaN trench MOSFET was reported

in 2007 by Otake *et al* [30]. Thereafter, there have been multiple reports on trench MOSFETs. In 2015. Oka *et al.* demonstrated high DC performance trench MOSFET with 1.2 kV breakdown voltage and an on-resistance of 1.8 mΩ.cm^2 [14].

A cross-sectional schematic of a trench MOSFET is shown in Figure 1.4. The functioning of a trench MOSFET is in principle similar to a conventional Si MOSFET. Akin to the Si MOSFET, when a gate bias more than the threshold voltage is applied, the channel forms via inversion in the p-GaN layer at the p-GaN/dielectric interface on the sidewall. Subsequently, the electrons flow vertically from the source via the sidewall channel and spreads out into the drift region and are finally collected by the drain contact. The electron flow in a trench MOSFET is illustrated in Figure 1.5.

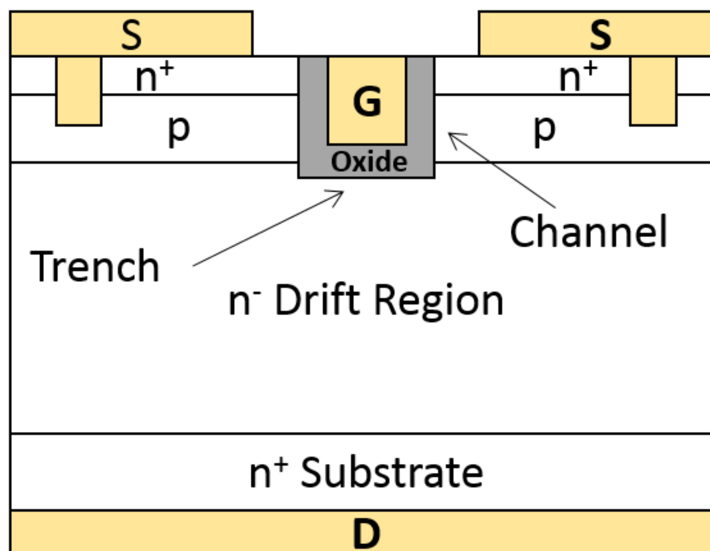


Figure 1.4 Trench MOSFET cross sectional schematic.

Trench MOSFETs have some basic advantages over the CAVET type device design. First, normally-off or enhancement mode operation can be achieved with relative ease in trench MOSFETs with MOS gate in trench MOSFETs. Second, the absence of regrowth makes

fabrication process relatively shorter and less challenging. In CAVETs, as discussed earlier, regrowth of channel region is challenging and becomes even more challenging due to the need for conformal growth in the trenched structure. Third, the absence of a JFET or aperture region in these devices. This allows high cell density which results in lower specific on-resistance of the device. Unlike the CAVET, the trench MOSFET is a fully vertical device. Since, the device is fully vertical, the pitch of the device can be significantly reduced in comparison with the CAVET.

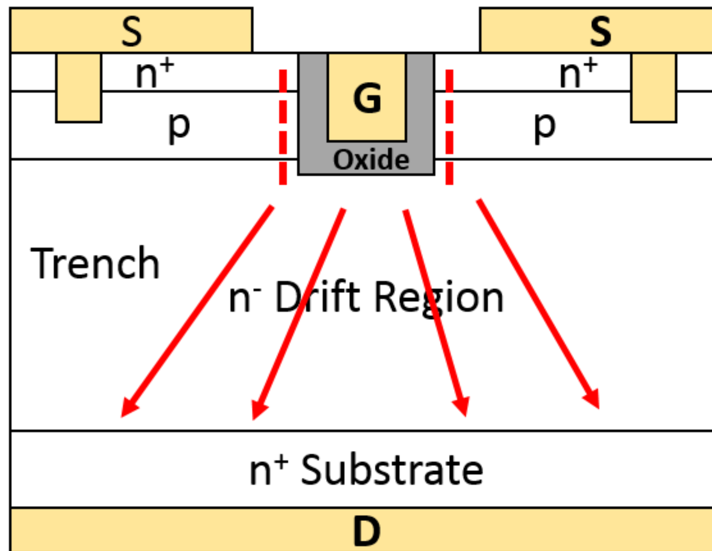


Figure 1.5 Electron flow in a trench MOSFET.

Such advantages of the trench MOSFET makes it an attractive device design for vertical devices. However, one of the biggest challenges of a trench MOSFET is the channel resistance in these devices [29], [31]. The formation of a channel on the etched sidewall results in poor electron channel mobility which increases the channel resistance. Low electron mobility can potentially create reliability issues as a higher gate bias needs to be applied to reduce the channel resistance by inducing high inversion charge. Similar issues were encountered in Si

and SiC trench MOSFETs as well. In both Si and SiC, etch damage caused on the sidewall was removed by depositing a “sacrificial oxide”. The oxide is grown on the trench sidewall and completely removed by wet etch. After this sacrificial oxidation process, the gate dielectric is grown. This process step has proved to a major breakthrough in developing reliable and high-performance trench MOSFETs in Si and SiC [29].

Unfortunately, application of such “sacrificial oxide” technique to improve the semiconductor/dielectric interface in GaN is difficult. The oxidation of GaN at high temperatures is not well behaved and makes the application of the above technique difficult or almost impossible. Therefore, to improve the channel properties, an alternate technique is needed for GaN trench MOSFETs.

In this work, a solution to the aforementioned problem was proposed by introducing a novel device modification in trench MOSFETs. In this device design, a GaN interlayer is regrown followed by *in-situ* dielectric deposition on the trenched structure to enhance the channel electron mobility. As per the functionality, the device was named in-situ Oxide, GaN interlayer based vertical trench MOSFET (OG-FET) and illustrated in Figure 1.6.

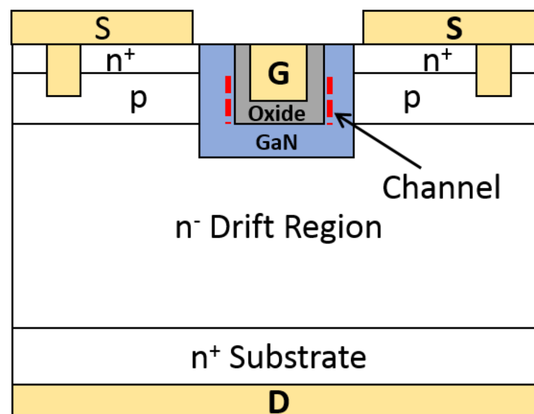


Figure 1.6 OG-FET cross sectional schematic.

1.2 Thesis Overview

This dissertation focuses on the development of the OG-FET for high power switching applications. The basic or bare minimum requirements of high power transistor are high breakdown voltage, low on-resistance, and normally-off operation. Since, the OG-FET device design had never been previously reported, majority of this work was focused on obtaining state of the art DC performance.

Chapter 2 describes the material requirement for high voltage vertical devices. Experiments pertaining to substrate choice and threading dislocation density performance on vertical devices are described. Also, the role of impurity incorporation in epitaxial layers affecting device performance is also discussed.

Chapter 3 describes the conceptualization and fabrication process of the OG-FET. The advantages of the OG-FET device design over a trench MOSFET are described. Important fabrication modules critical to the device performance are also discussed in detail.

Chapter 4 discusses the high voltage OG-FETs. Device results, experiments and analysis are described in detail.

Chapter 5 summarizes this dissertation work and provides research ideas to further the OG-FET performance.

Chapter 2: Epitaxial requirement for vertical GaN devices

Vertical GaN devices require the highest material quality for prolonged safe operation. The development of vertical GaN devices compared to SiC devices have been slower primarily due to the limited availability of bulk GaN substrates [32]. Threading dislocations in GaN are another big concern for the development of failsafe high voltage vertical GaN power electronics. GaN has been traditionally grown on heterogeneous substrates such as Si, SiC, and sapphire, for use in lateral devices. This material has a high threading dislocation density of 10^8-10^{10} cm^{-2}. These dislocations arise from the lattice mismatch between GaN and the substrate. Bulk GaN substrates have lower dislocation density (10^6 cm^{-2}) and are more suited for vertical GaN devices. However, current bulk GaN substrates suffer from uniformity issues and are significantly more expensive than heterogeneous substrates [33].

Another important aspect of GaN epitaxial growth is the unintentional impurity incorporation in GaN layers. Impurities such as carbon in GaN layers result in donor compensation. This limits the lower bound of free carrier concentration that can achieved and could lead to various issues in epitaxial growth and subsequent device behavior.

In subsequent sections, the role of substrate, threading dislocations and impurity incorporation are discussed.

2.1 Substrate

The starting substrate for the epitaxial growth of GaN plays an important role in determining the device performance. Initial vertical GaN development was done on heterogeneous substrates due to the absence of high quality bulk GaN substrates [23]. GaN

grown on heterogeneous substrates such as Si, SiC, sapphire etc. result in high threading dislocation density due to lattice mismatch between GaN and the substrate. The dislocation density on heterogeneous substrates vary from 10^8-10^{10} cm^{-2}. Threading dislocations have been shown to affect off-state performance in GaN p-n diodes [13], [32]. Due to threading dislocations, increased off-state leakage was observed in p-n diodes. Furthermore, the development of vertical GaN on heterogeneous substrates is challenging due to the limitations in the thickness of the layers grown on substrates due to the thermal mismatch. Vertical devices targeted towards achieving breakdown voltage of 1200 V and above requires the nominal drift region to be thicker than at least 10 µm [34]. Therefore, due to threading dislocations and limitations in the drift region thickness, realization of high performing vertical GaN devices on heterogeneous substrates is difficult. However, when bulk GaN substrates are used, low dislocation density epitaxial GaN (~10^6 cm^{-2}) layers can be obtained. High performance p-n diodes and FETs were demonstrated on bulk GaN substrates. Numerous reports demonstrating avalanche breakdown in p-n diodes demonstrate the improved quality of bulk GaN substrates [12], [13], [35]. However, the uniformity of substrate quality from wafer to wafer or within different areas of a wafer is still a concern and needs to be improved [33].

2.2 Threading dislocations in GaN

Numerous researchers have studied the impact of threading dislocations on the performance of p-n diodes. Researchers observed that with the increased density of threading dislocations, higher off-state leakage was observed in p-n diodes [32]. Higher off-state leakage in p-n diodes due to threading dislocation could be attributed to two reasons. First, due to the presence of threading dislocation, local lowering of the p-n junction barrier height. Second, a threading dislocation could act as an electron-hole pair generation center. Under reverse bias,

the electron-hole pair generated in the depletion region will move towards cathode and anode respectively under the influence of electric field, thus, contributing to increased off-state leakage.

MOSCAPs and p-n diodes are an integral part of GaN power devices. Even though understanding both MOSCAP and p-n diode off-state behavior is important, MOSCAP reverse bias studies are non-existent. Therefore, the impact of threading dislocations on GaN vertical power devices was studied for the first time by fabricating metal-oxide-semiconductor capacitors (MOSCAPs). MOSCAPs were fabricated on both sapphire and bulk GaN substrates. In the next sub-sections, the experiments and results are discussed.

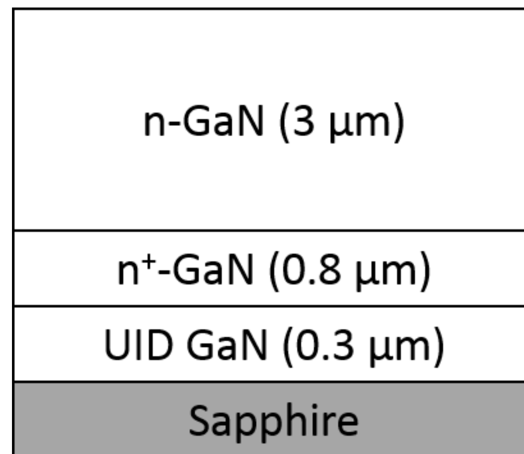


Figure 2.1: GaN layers grown by MOCVD for MOSCAPs.

2.2.1 GaN MOSCAPs: SiN vs Al_2O_3

In this study, the dielectrics were chosen to study the impact of dislocations on different gate-dielectrics. The dielectrics (SiN and Al_2O_3) in this experiment were deposited by MOCVD. First, a lightly doped GaN epi was grown by MOCVD shown in fig 2.1. Prior to dielectric depositions, the samples underwent UV ozone and 48 % hydrofluoric acid (HF) treatment to remove residual silicon (Si) at the dielectric/semiconductor interface [31]. The

presence of Si at the regrowth interface can cause high electric field in the gate-dielectric under reverse bias and can cause early breakdown of the gate-dielectric. Therefore, it is important to remove and/or reduce Si at the interface. Immediately after UV ozone and HF cleaning, the samples were loaded in the MOCVD reactor and dielectric growths were performed. The thicknesses of the gate dielectrics were 50 nm. Ti/Au (300 nm/2000 nm) was used as both the gate and the ohmic contact. The MOSCAP cross sectional schematic is shown in fig. 2.2.

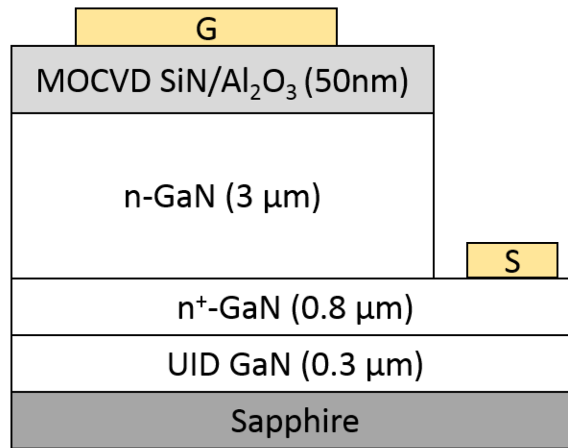


Figure 2.2: MOSCAP cross sectional schematic.

Forward and reverse current-voltage characteristics of both MOSCAPs are shown in fig 2.3 and fig. 2.4 respectively. Both lower forward and reverse leakage current was observed with Al_2O_3 compared with SiN. High forward leakage current is a characteristic of SiN on GaN and has been observed by numerous researchers. Al_2O_3 demonstrated catastrophic breakdown at 120 V. However, no catastrophic breakdown was observed with SiN up to the measurement limit of 200 V. Under reverse bias, higher leakage was observed with SiN compared with Al_2O_3. The major difference between these two dielectrics is their band lineup with GaN as shown in fig. 2.5. SiN has negative valence band offset with GaN while Al_2O_3 has positive valence band offset with GaN.

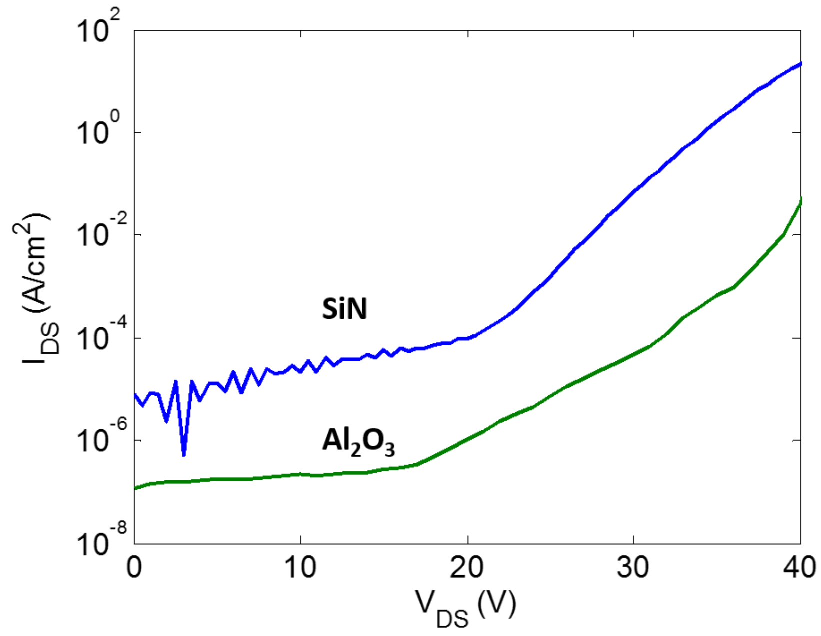


Figure 2.3: Forward I-V characteristics of both MOSCAPs.

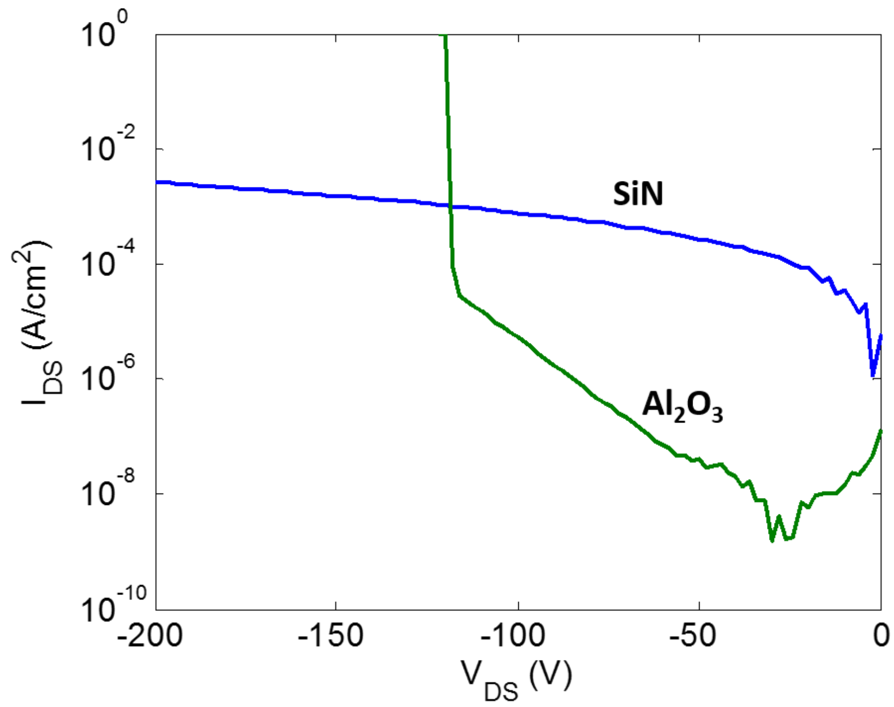


Figure 2.4: Reverse I-V characteristics of both MOSCAPs.

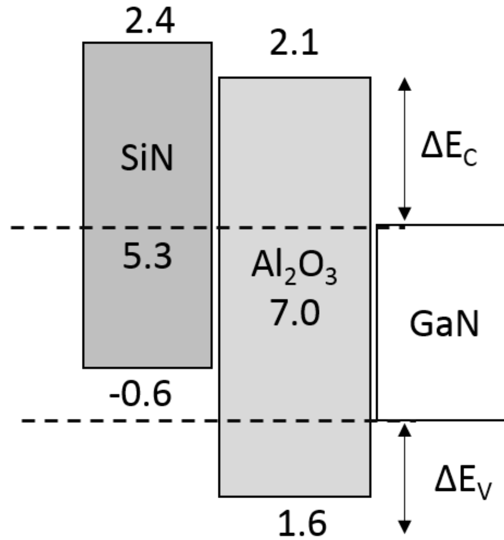


Figure 2.5 Conduction and valence band line up of SiN and Al_2O_3 with GaN.

The reverse bias behavior of two dielectrics could be explained by considering threading dislocations to be the generation centers for electron-hole pairs. Fig. 2.6 a) shows the band diagram of MOSCAP (assuming gate dielectric has positive valence band offset with respect to GaN) under reverse bias with a gate voltage V_G (here, it is assumed that V_G is more negative than the flat-band voltage of the MOSCAP). Electron-hole pairs generated in the depletion region under the influence of electric field will move towards ohmic and gate contact respectively. However, in Al_2O_3, due to the presence of positive valence band offset between semiconductor and the gate dielectric, the holes experience a barrier between the semiconductor and the gate electrode. Due to this barrier, holes start piling up at the semiconductor-dielectric interface and electrons flowing through the external circuit pile up at the gate electrode to maintain system charge neutrality. The piling up of holes and electrons across the gate-dielectric increases the electric field in the gate-dielectric. This can potentially result in early breakdown of the gate-dielectric.

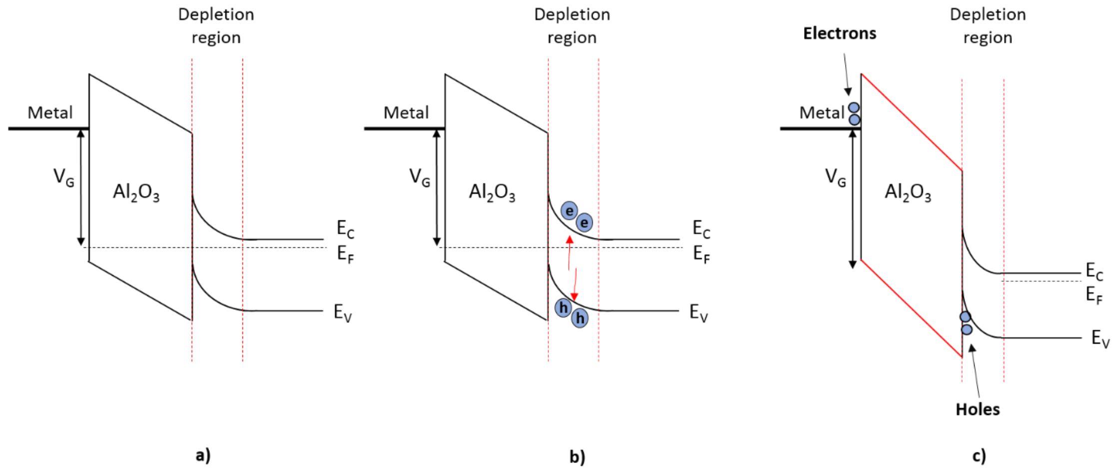


Figure 2.6: a) shows the depletion region of n-type GaN under the application of reverse bias (with a gate voltage V_G). The electron-hole pair generation in the depletion region by threading dislocations acting as generation centers (b). The presence of an electric field in the depletion region moves electrons and holes in the opposite direction. The positive valence band offset between Al_2O_3 and GaN results in holes (generated by threading dislocations in the depletion region) piling up at the semiconductor-dielectric interface as shown in c). The piling up of holes and electrons results in an increased electric field in the gate-dielectric.

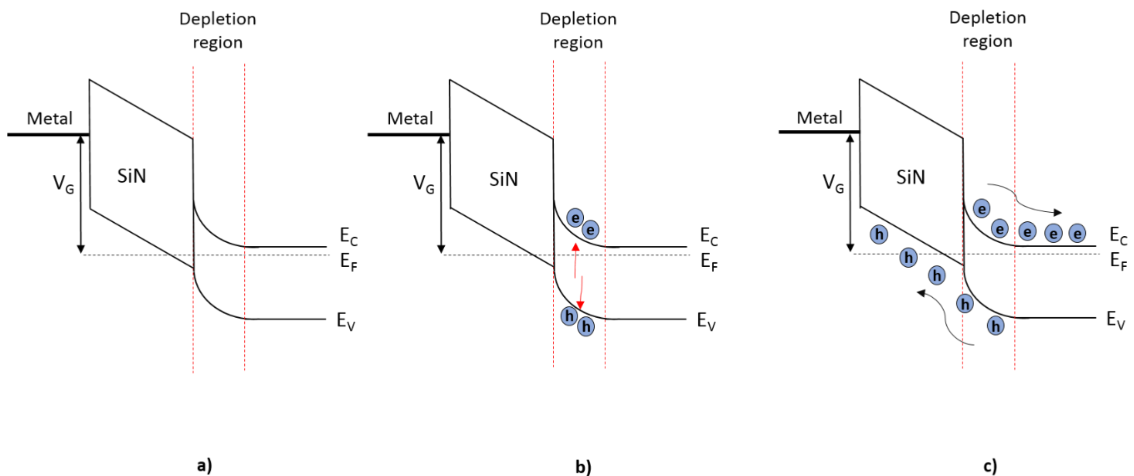


Figure 2.7: a) shows the depletion region of n-type GaN under the application of reverse bias (with a gate voltage V_G). The electron-hole pair generation in the depletion region by threading dislocations acting as generation centers (b). The presence of electric field in the depletion region moves electrons

and holes in the opposite direction. The absence of barrier for holes (unlike Al_2O_3) with SiN results in free movement of holes towards gate electrode (c). Similarly, electrons move towards ohmic electrode resulting in increased reverse leakage current (c).

Similar effect was not observed in SiN due to the presence of negative valence band offset between SiN and GaN [36]. Therefore, the absence of a hole barrier allows the generated holes to be collected by the gate electrode and electrons to be collected by ohmic electrode [37]. This results in an increased reverse leakage current in SiN MOSCAPs compared with Al_2O_3.

This experiment shows how threading dislocations affect power devices. Apart from increasing reverse or off-state leakage current, it could result in early catastrophic breakdown of the device. In the next sub-section, MOSCAPs were fabricated on both bulk GaN and sapphire to study this phenomenon in more detail.

2.2.2 GaN MOSCAPs: Bulk GaN vs Sapphire

Motivated by the experiment in the above section which showed that dislocations could result in the early breakdown of the gate-dielectric (with positive valence band offset to GaN), the next step was to investigate MOS capacitor off-state performance on bulk GaN with low threading dislocation density. Since, our final goal was to fabricate trench MOSFETs, etched MOSCAPs were fabricated to mimic the trench MOSFET gate-drain structure as shown in the figure. In a trench MOSFET as shown in figure 2.8, the gate-drain region is like a MOSCAP structure. In the trench MOSFET, the trench-etch ends on n-type semiconductor region, therefore, the semiconductor-dielectric interface is ex-situ and is not ideal [10]. Therefore, studying etched MOSCAPs behavior is important.

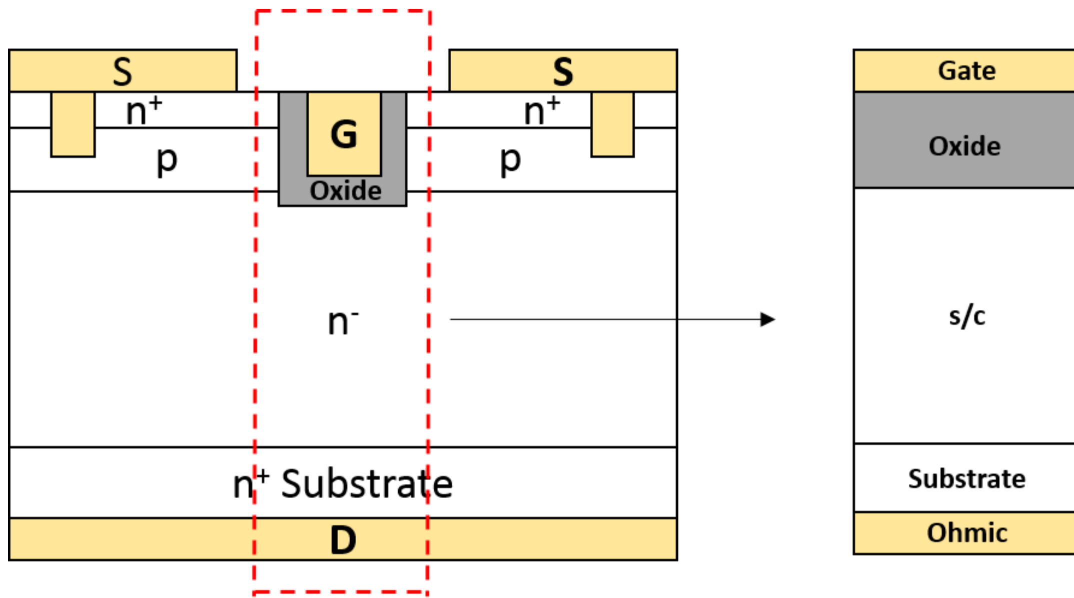


Figure 2.8: Gate-drain region of a trench MOSFET structure (shown in dashed lines) mimics a MOS capacitor structure.

In this study, the planar MOSCAPs were fabricated on both sapphire and bulk GaN to study the impact of dislocations on the gate-dielectric. To mirror the trench MOSFET fabrication process, first, a trench MOSFET epitaxial structure was grown on both bulk and sapphire. Thereafter, the top n^+-GaN and p^+-GaN layers were etched like a typical trench MOSFET fabrication process [10]. Since, the trench-etch was not selective between n- and p-type GaN, n-type GaN underneath p-type GaN was etched to ensure the complete etching of p-GaN layer. To improve the interface quality between etched semiconductor and the gate-dielectric, a thin GaN interlayer was added by MOCVD. Prior to MOCVD regrowth process, the samples underwent UV ozone and 48 % hydrofluoric acid (HF) treatment to remove residual silicon (Si) at the dielectric/semiconductor interface as described in the previous section. The MOCVD regrowth process was performed in two steps. First, the samples were annealed in N_2/NH_3 for 30 min. at 930 °C to recover etch damage [38]. Following annealing, UID-GaN interlayer was grown on the sample. The GaN interlayer regrowth was followed by the in-situ

deposition of the gate-dielectric (Al_2O_3) [39]. The thickness of the MOCVD Al_2O_3 was 50 nm. Ti/Au (300 nm/2000 nm) was used as both gate and ohmic contact. For sapphire, due to thick drift region, a large pad (3mm x 3mm) was deposited which was used as the ohmic contact [31]. For bulk GaN, metal was deposited on the backside.

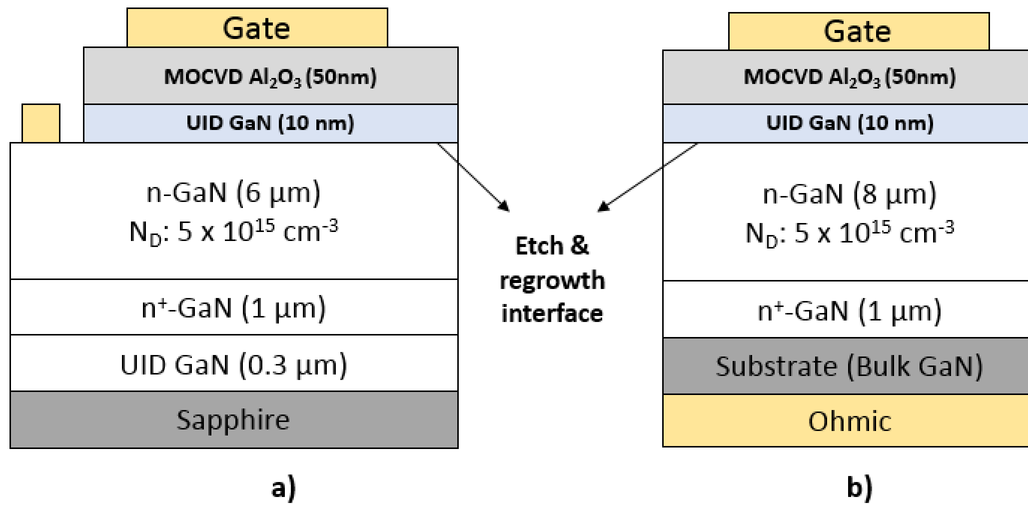


Figure 2.9: a) GaN MOSCAP on sapphire substrate. The ohmic contact was made far from the gate contact. On a separate die, the gate dielectric was etched off entirely and ohmic metal was deposited on the entire die area (3 mm x 3 mm). This was used as ohmic contact for the MOSCAP. b) GaN MOSCAP on bulk GaN substrate. In both MOSCAPs, GaN interlayer was added to obtain improved semiconductor/dielectric interface.

Similar forward bias behavior was observed for both MOSCAPs (on bulk GaN and sapphire). However, a stark difference in reverse bias behavior of both MOSCAPs was observed. The MOSCAP fabricated on sapphire demonstrated a significantly low breakdown of 90 V compared to 700 V for MOSCAP fabricated on bulk GaN.

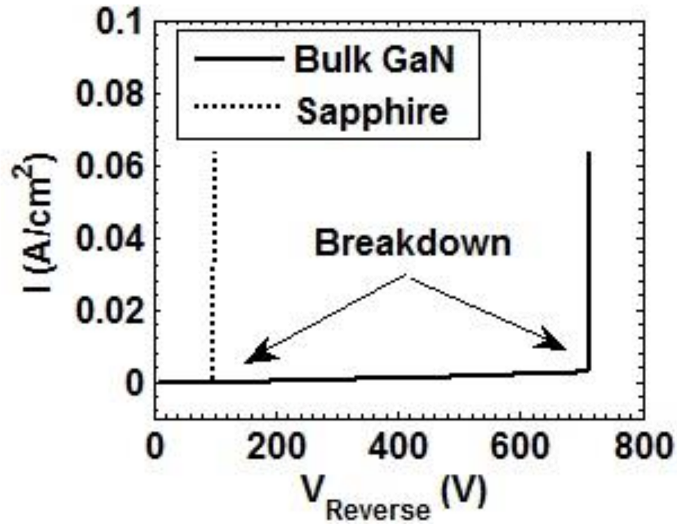


Figure 2.10: The MOSCAP reverse bias characteristics. The reverse leakage current for both MOSCAPs was in the noise and they both broke down catastrophically.

The associated breakdown fields in GaN at which the gate-dielectric breaks down for sapphire and bulk GaN MOSCAPs were estimated to be ~0.3 MV/cm and ~1.4 MV/cm respectively. For GaN on sapphire MOSCAP, at such low breakdown field of ~0.3 MV/cm, the breakdown of GaN layers is not expected and cannot be explained. However, considering dislocations as generation centers, these results can be understood. We hypothesize that with sapphire substrate, due to high dislocation density, the holes piling up at the semiconductor/dielectric interface would be higher compared to bulk GaN substrate. This would result in an increased electric field in the gate-dielectric and would cause an early breakdown in sapphire devices as observed.

2.3 Role of Carbon on device performance

Vertical GaN devices are attractive for high voltage, high power switching applications. To service these applications, a lightly n-type doped GaN layer that is tens of micrometers thick is required; furthermore, the free carrier concentration must be 10^{16} cm^{-3} or lower to

provide a breakdown voltage of several kilovolts [34]. Reliably achieving free carrier concentration of 10^{16} cm^{-3} in the thick drift layer is a big challenge, as the interplay between unintentional acceptors or other point defects and donors must be well controlled [40]. Numerous researchers have demonstrated good linearity between Si dopant and free carrier concentrations above 10^{16} cm^{-3}. However, due to the presence of residual impurity concentration such as carbon (C), it is difficult to control free carrier concentration lower than 10^{16} cm^{-3}. Nitrogen-site carbon incorporation in GaN has been reported to act as an acceptor and compensate donors. This results in a non-linear behavior of Si dopant and free carrier concentration [34]. This lack of controlled doping can inadvertently result in low free carrier concentrations or insulating layers and can significantly increase the resistance of the GaN layers.

Carbon incorporation in MOCVD grown GaN films occurs due to the methyl groups present in the Ga precursor, trimethylgallium (TMGa). High temperature, high V-III ratio, and high growth pressure are effective to reduce carbon incorporation in GaN films [40]. Therefore, growth conditions need to be optimized to obtain GaN layers with free carrier concentration of 10^{16} cm^{-3} or lower.

The incorporation of carbon in n-type GaN layers affect unipolar and bipolar transport differently. In compensated layers, where, incorporated carbon (N_T) is greater than the targeted doping (N_D), the fermi level lies at the trap (carbon) level. For unipolar transport, for example, a schottky diode fabricated on compensated layers will exhibit a high turn-on voltage and high on-resistance. The electrons injected in the semiconductor instead of being mobile will fill the empty trap states. The voltage applied (V_{AP}) will be governed by the following equation,

$$V_{AP} = \frac{qN_T W^2}{2\varepsilon_{O\varepsilon_r}} \qquad 2.1$$

where, N_T is the incorporated carbon density and W is the thickness of the drift layer with carbon. Only after entirely filing the trap states, the injected electrons will flow as mobile electrons i.e. current. Therefore, the amount of voltage needed is significantly high as for power devices, the drift regions are relatively thick. For example, an incorporation of 10^{16} cm^{-3} carbon in 1μm thick drift region would give an approximate turn-on voltage of 10 V.

However, in bipolar transport, for example, a p-n junction, the injection of holes and electrons under forward bias neutralizes the trap and low on-resistance is observed compared to schottky diode. Since, power devices are unipolar in nature, to avoid high resistances, it is of paramount importance to control impurity incorporation in GaN layers.

Chapter 3: The OG-FET innovation; device design and fabrication

In trench MOSFETs, the channel forms on the tapered/vertical etched sidewall. Roughness of the etched sidewall along with impurity incorporation prior to the dielectric deposition results in poor channel properties, especially poor channel mobility [10]. Poor channel properties can potentially cause reliability issues and limit the realization of full potential of this device design [29]. As discussed in the introduction chapter, in Si and SiC trench MOSFETs, the sidewall etch damage was reduced by using a "sacrificial oxide" technique [29]. In this method, a thick gate oxide (SiO_2) was formed on the trenched structure by oxidation and was completely removed by wet chemistry. This method removes sidewall roughness and improves interface quality. Following the sacrificial oxidation process, the gate dielectric is deposited. This technique played a significant role on producing reliable and high-performance trench MOSFETs in Si.

However, the absence of native oxide and lack of oxidation of GaN even at high temperatures makes the adoption of "sacrificial oxide" technique for GaN difficult. In GaN, using tetramethylammonium hydroxide (TMAH) sidewall roughness can be reduced. TMAH selectively etches sidewall plane and stops on the non-polar planes while c-plane (0001) remains unaffected [11], [21], [41] as shown in figure 3.1. However, the roughness on the c-plane remains unaffected and the damage caused underneath the sidewall surface is difficult to recover. Therefore, to improve channel properties, alternate technique is needed for GaN trench MOSFETs.

The OG-FET device design was targeted towards improving channel properties in GaN trench MOSFETs. In the OG-FET, a GaN interlayer is regrown followed by *in-situ* dielectric deposition on the trenched structure to enhance the channel (electron) mobility (Fig 3.2). As per the construction, the device was named in-situ Oxide, GaN interlayer based vertical trench MOSFET (OG-FET) [31], [42]. In the next section, the OG-FET device design is discussed and compared with conventional trench MOSFET device design.

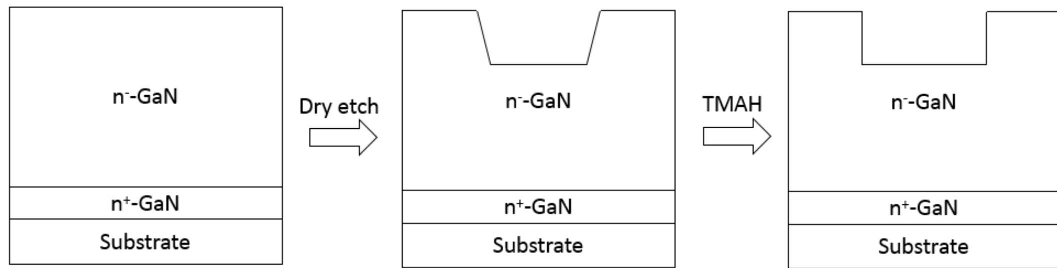


Figure 3.1: TMAH selectively etches GaN sidewall planes and helps in achieving true vertical sidewalls.

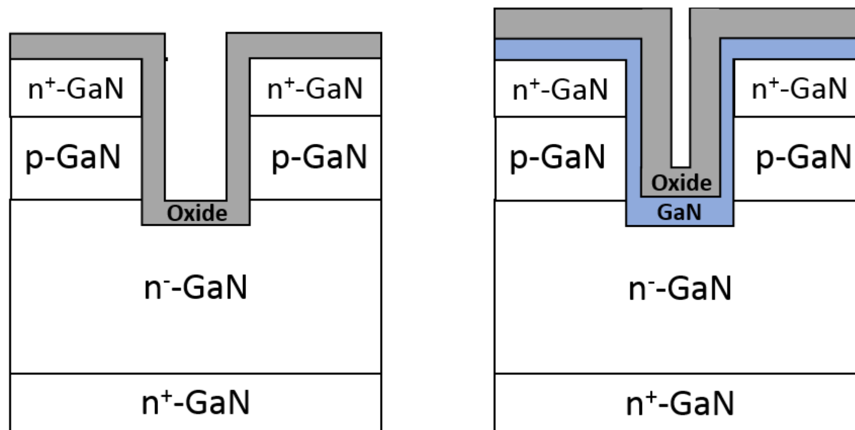


Figure 3.2: A conventional trench MOSFET structure where gate-dielectric is deposited after gate trench-etch (Left). An OG-FET device design, where after gate trench etch, a GaN interlayer is re-grown followed by the gate-dielectric deposition (Right).

In the remaining part of this chapter, the OG-FET epitaxial design and fabrication process is described. In addition, important fabrication process modules are also discussed.

3.1 OG-FET vs Trench MOSFET

The functioning of the OG-FET is akin to a conventional trench MOSFET as shown in fig. 3.3. When a gate bias more than the threshold voltage is applied, the channel forms at the UID-GaN interlayer/*in-situ* gate-dielectric interface and the electrons flow from the source into the drift region through this sidewall channel modulated by the sidewall gate.

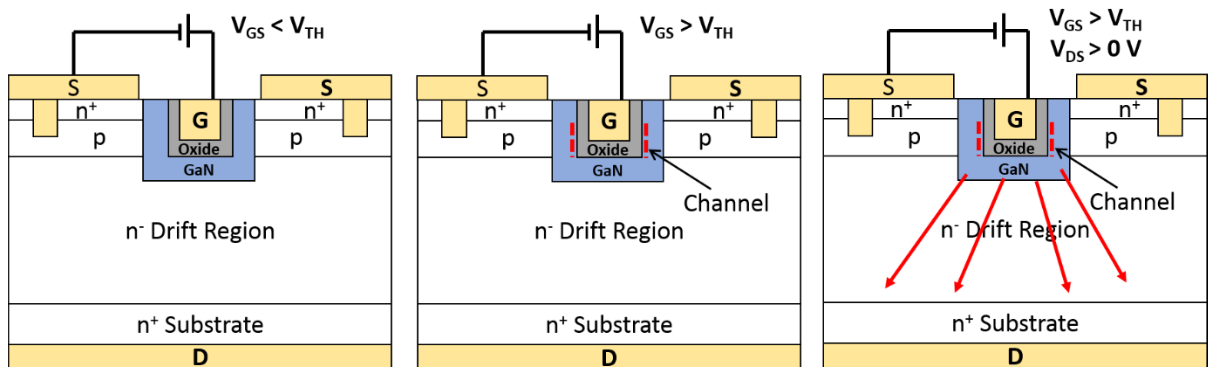


Figure 3.3: With gate-voltage lower than the threshold voltage, the OG-FET remains in the off-state (Left). When a gate voltage greater than the threshold voltage is applied, the channel forms (Middle) and with a positive drain source voltage, the electrons flow from source to drain via the channel and the drift region (Right).

The OG-FET device design builds up on the advantages offered by the conventional trench MOSFET device design. The improvement in channel properties is expected with the OG-FET due to primarily two reasons. First, because of the separation of the channel and the p-GaN layer introduced by the UID-GaN interlayer results in reduced ionized impurity scattering (Fig 3.4). Second, is the *in-situ* channel interface. The growth of in-situ dielectric after the growth of GaN without breaking vacuum offers an improved channel interface compared to

conventional trench MOSFET. In addition, the *in-situ* dielectric growth onto the GaN interlayer allows this device to achieve lower interface trap density (D_{IT}) compared to devices with ex-situ dielectrics deposited onto the trenched structure which is of paramount importance for gate-stack reliability [43], [44]. Third, addition of GaN interlayer lowers the sub-threshold slope in this device design compared to trench MOSFET without GaN interlayer.

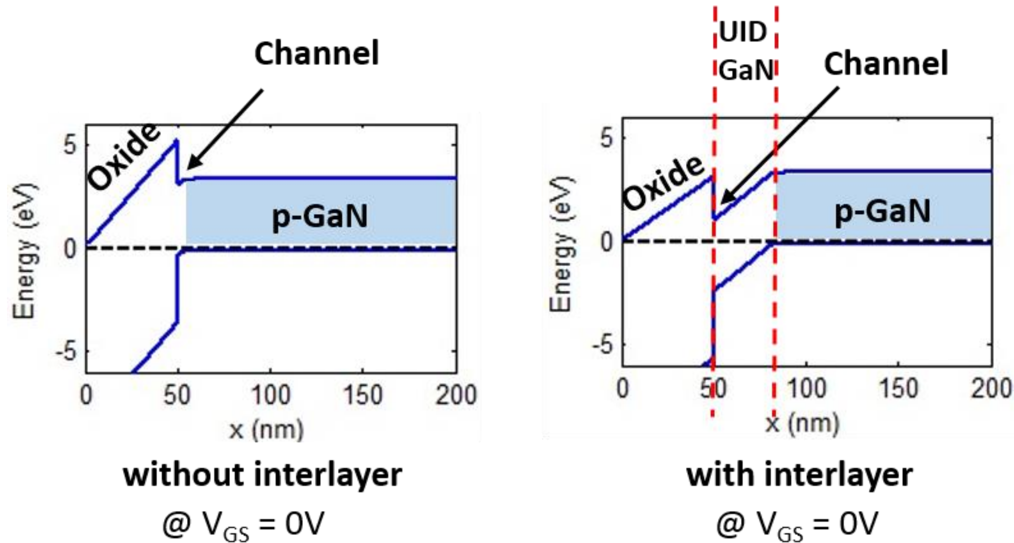


Figure 3.4: Sidewall band diagram (Gate/Oxide/UID-GaN/p-GaN) comparison of OG-FETs with and without interlayer at zero gate-bias. The figure clearly shows with increasing UID-GaN interlayer thickness the channel is further spaced from p-GaN, thereby, reducing ionized impurity scattering.

Compared to the conventional trench MOSFET, the OG-FET requires an additional regrowth step [31]. However, the regrowth involved in OG-FET is blanket and mask-less as shown in fig. 3.2. Unlike the CAVET, planarity of the surface after regrowth is not preferred with the conformal nature of regrowth being desirable which is easily attainable. Also, with the III-N growth followed by the gate-dielectric without breaking vacuum in MOCVD reduces additional step of growing GaN interlayer separately.

Enhancement mode operation is a key requirement in power devices to facilitate reliable and failsafe operation. Reliable normally-off GaN HEMTs are achieved by using Si MOSFETs in cascode configuration with GaN HEMT [45]. With the trench MOSFET, obtaining normally-off behavior in intrinsic device is relatively easier. Compared to the conventional trench MOSFET, the OG-FET is expected to have a lower threshold voltage. This is a negative consequence of the addition of the GaN interlayer in the gate stack. With GaN interlayer, the conduction band in OG-FET is closer to the fermi level compared to the trench MOSFET at zero gate bias as shown in fig. 3.4. However, as shown in the figure, the conduction band in the OG-FET is still above the fermi level at zero gate bias, therefore, normally-off device can be achieved. The threshold voltage of an OG-FET can be controlled by GaN interlayer thickness design and p-GaN doping. Using both these parameters, good normally-off behavior with threshold voltage > 2 V can be achieved [31], [46].

Regrown channel in a GaN trench MOSFET has been reported by Okada *et al*. in 2010 [47]. However, they employed AlGaN/GaN regrown channel on a shallow (75° from vertical) sidewall with a schottky gate. With the regrown AlGaN/GaN interlayer, normally-off operation was achieved with a low threshold voltage of 0.3 V. For high voltage power devices, a threshold voltage above 2-5 V is preferred to facilitate failsafe reliable operation [48]. The results obtained by Okada *et al* indicates that with regrown AlGaN/GaN channel, it is difficult to achieve normally-off operation above 2 V and hence an alternate approach deserves investigation.

With the mentioned on-state advantages, similar off-state, and normally-off behavior, OG-FET device design is very interesting and was explored in this thesis. State-of-the art DC performance was demonstrated in this work [17], [18], [46].

3.2 Epitaxial structure design and device fabrication

In this work, the OG-FETs were fabricated on both sapphire and bulk GaN substrates. Initial OG-FET development and optimization of the fabrication process was done on sapphire substrates. This was due to the high cost of bulk GaN substrates. The device epitaxial structure and fabrication process were similar on both substrates except for few details.

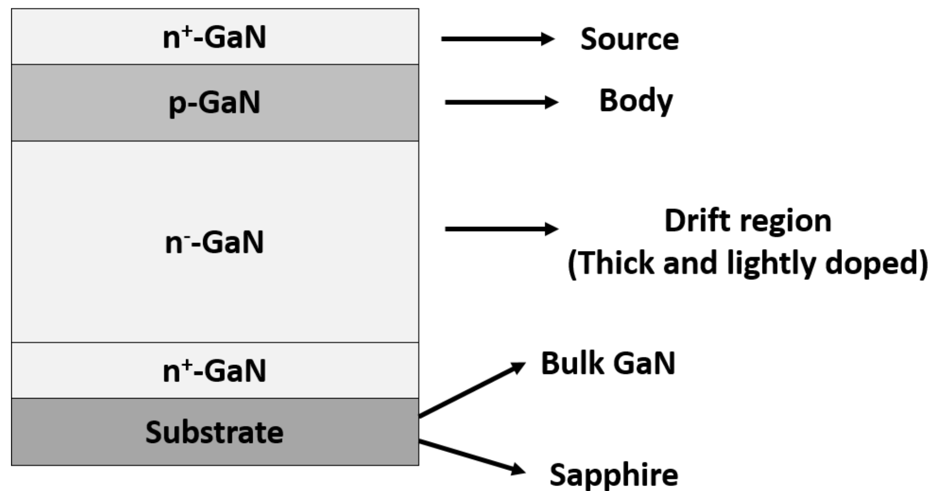


Figure 3.5: OG-FET epitaxial structure.

3.2.1 Epitaxial Design

The OG-FET epitaxial structure consists of n^+-GaN/p-GaN/n^-GaN/n^+-GaN layered stack as shown in fig. 3.5. The OG-FETs in this dissertation were grown in an MOCVD reactor using trimethyl gallium (TMGa), silane, bis-cyclopentadienyl magnesium (Cp_2Mg), and NH_3 as precursors. The bottom n^+-GaN serves as the drain in GaN on sapphire, while, on Bulk substrates in serve as conducting buffer layer. It has been shown that a buffer layer on bulk GaN substrates results in improved off-state performance [49]. The targeted thickness and the doping of the bottom n^+-GaN layer was 1µm and 2-5 x 10^{18} cm^{-3} in this work on both sapphire and bulk substrates.

Following the drain layer, the drift region was grown. The drift region thickness (W) and doping concentration (N_D) is related to the breakdown voltage (V_{BR}) and specific drift-resistance ($R_{DRIFT}A$) by following equations,

$$V_{BR} = \frac{qN_DW^2}{2\varepsilon_S} \quad 3.1$$

$$R_{DRIFT}A = \frac{W}{qN_D\mu} \quad 3.2$$

Where, q is the charge, μ is the mobility of the drift region, ε_S is the permittivity of GaN. It should be noted that these abovementioned equations assume ideal device design. Also, the ideal device design is also related to critical field of GaN as,

$$E_C = \frac{qN_DW}{2\varepsilon_S} \quad 3.3$$

Therefore, in an ideal power device design, the device breaks down when the drift region is fully depleted, and the breakdown voltage corresponds to critical field of the material (Figure 3.6). This ideal device design allows the realization of one dimensional material limit. It can be seen from above equations, that there is an inherent trade-off between the drift resistance and the breakdown voltage. High drift region mobility is advantageous as it reduces on-resistance without affecting the breakdown voltage. The drift region thickness and doping concentration were varied in this dissertation to achieve the desired device characteristics.

After the drift region, the p-GaN body region was grown. Here, the p-GaN thickness is the nominal gate-length of the device. In this dissertation work, the targeted p-GaN (Mg) doping was 3 x 10^{19} cm^{-3}. Such high concentration was chosen to avoid short channel effects, to avoid punch-through and achieve threshold voltage > 2V. After p-GaN growth, the sample was taken out of the MOCVD reactor and a 5 minute, (48%) HF dip was used to remove excess Mg from the surface and the sample was again loaded into the MOCVD reactor for the source growth

[50]. This was done to prevent the surface riding of magnesium into subsequent layers (Figure 3.7). This is an important step as incorporation of Mg into source layer could potentially increase source resistance and therefore, the total on-resistance of the device.

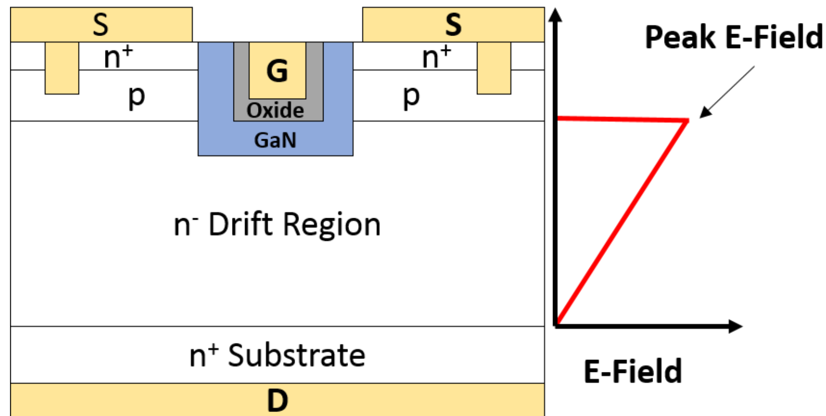


Figure 3.6: Desired electric field profile along the drift region is shown at the breakdown voltage. The peak electric field, therefore, should occur at the p-n junction and the electric field goes down to zero at the end of the drift region resulting in this triangular electric field profile.

Finally, 0.2 μm thick heavily doped n^+-GaN was grown for the source. High doping of the source layer reduces both contact and sheet resistance resulting in reduction of the source resistance. However, with higher doping, good surface morphology is imperative. Therefore, in this dissertation the source layer doping was kept between 2-5 x 10^{18} cm^{-3} as higher doping could result in the degradation of surface morphology.

In the future, to avoid MOCVD regrowth and simultaneously address surface riding of magnesium into subsequent layers a couple of techniques can be utilized. First, employing an AlN blocking layer following p-GaN growth as shown in fig 3.8. It has been shown that AlN is effective in reducing Mg incorporation in subsequent layers [51]. Second, using low temperature flow modulation epitaxy (LT-FME). With LT-FME, Mg incorporation in subsequent layers can be controlled remarkably [52]. However, high source layer doping (>2-

5×10^{18} cm^{-3}) with good surface morphology has proved to be challenging to obtain with flow modulation epitaxy.

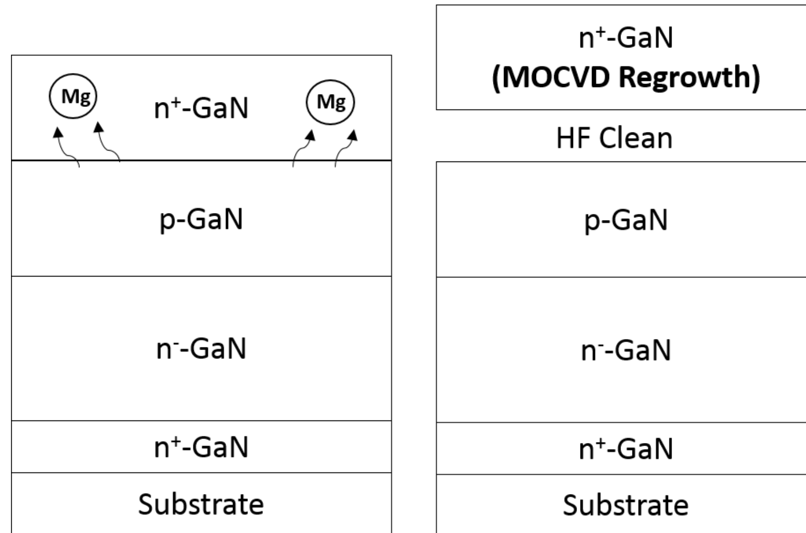


Figure 3.7: Surface riding of magnesium (Mg) in subsequent layers (Left). Surface riding can be reduced by removing excess Mg from the surface by introducing a HF clean (Right).

3.2.2 Device Fabrication Process

The OG-FET fabrication process starts with the formation of nearly vertical trench structures by dry etching. Tapered sidewalls provide longer channel length and thus result in an increased channel resistance of the device. However, it is difficult to obtain low damage perfect vertical sidewalls with only a dry etch. A combination of dry and wet etch can be used to obtain true vertical sidewalls. TMAH selectively etches sidewall planes such as *a*- and *m*-plane without affecting the c-plane (0001). Following dry etch, TMAH treatment can result in perfect vertical sidewalls [53]. However, in this dissertation, TMAH based wet etch was not utilized. Although, in future OG-FET fabrication process, TMAH based wet etch can be readily incorporated. The dry etches used in this dissertation work resulted in trench angle of less than

or equal to 15° from vertical. Further details regarding etch and etch chemistry are provided in next section.

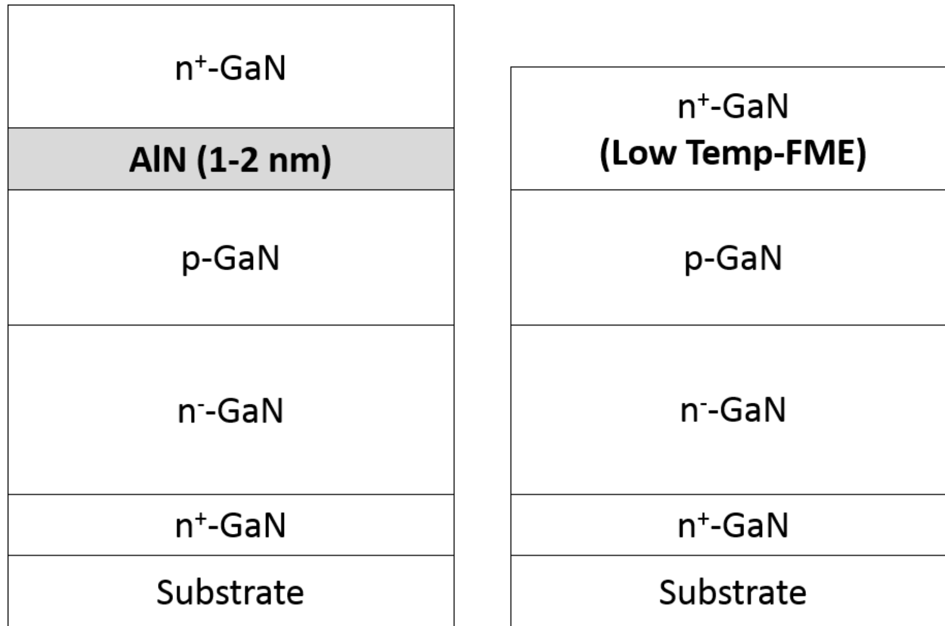


Figure 3.8: Alternative techniques to suppress Mg incorporation in subsequent layers without taking the sample out of reactor. By using a thin AlN interlayer (Left) and by growing n^+-GaN layer by low temperature flow modulation epitaxy (Right).

Following the trench-gate etch process, a cleaning procedure was developed prior to the MOCVD regrowth (Figure 3.9). The samples underwent UV-Ozone and HF treatment to remove residual Si, which is commonly observed at regrowth interfaces [51]. The UV-ozone and HF treatment were always performed immediately before MOCVD regrowth process. It involves 3 cycles of 15 minutes of UV ozone treatment followed by 1 minute 48 % hydrofluoric acid dip followed by a deionized water rinse. The presence of Si can result in negative threshold shift and early breakdown of devices [54]. Therefore, it is imperative to perform cleaning prior to MOCVD regrowth process.

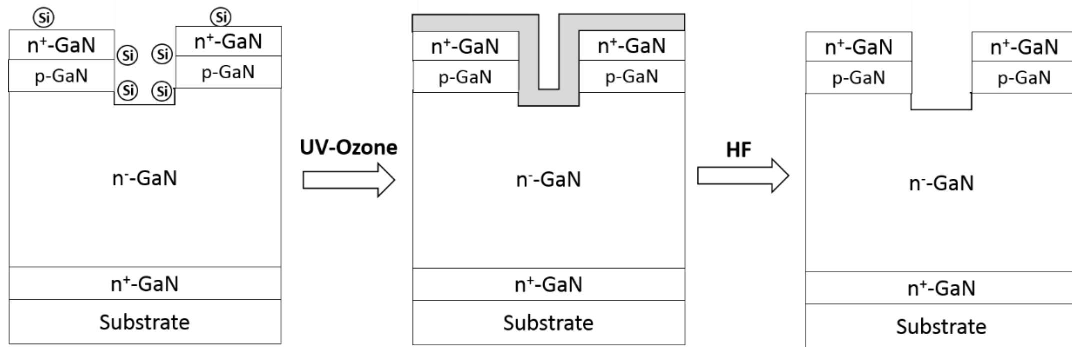


Figure 3.9: UV-ozone and HF treatment. First, the elemental silicon present at the interface is oxidized to SiO_2 by performing UV-ozone treatment. HF dip removes the SiO_2, thereby reducing Si at the interface.

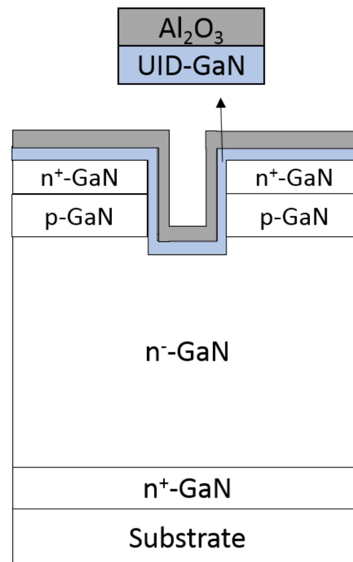


Figure 3.10: Sample after MOCVD regrowth process. On the etched surface shown in fig 3.9, UID-GaN interlayer followed by Al_2O_3 were regrown.

Thereafter, the sample goes through MOCVD trench channel regrowth process as shown in fig. 3.10. The MOCVD regrowth process consisted of two steps. First, the samples were annealed in N_2/NH_3 for 30 min. at 930 °C to recover trench-gate etch damage [38]. Even though this recovery anneal was performed, the extent to which this helps in healing etch damage is

not known and studies need to be performed to characterize the impact of recovery anneal on the device performance. Following annealing, the UID-GaN interlayer (of desired thickness) was grown on the sample at 950 °C. At this temperature, no mass reflow was observed. Conformal regrowth of GaN interlayer was desired and achieved. GaN exhibits varied growth rates on different growth planes. The trench offers one such situation. The bottom part of the trench was c-plane GaN and sidewalls were oriented towards either *a*- or *m*-plane. It was observed that the sidewall growth rate was slower (approximately half) than the c-plane growth rate. This was estimated by performing transmission electron microscopy (TEM) studies. Multiple samples with gate trenches were prepared. On the first sample, the GaN interlayer was regrown followed by MOCVD oxide and gate metal deposition (Figure 3.11). On the second sample, GaN interlayer regrowth was followed AlGaN interlayer and MOCVD oxide regrowth and gate metal deposition. For the first sample, the GaN interlayer was not clearly visible as GaN on GaN was difficult to differentiate (Figure 3.11 a)). The oxide was visibly crystallizing at the GaN/oxide interface on the c-plane as shown in fig. 3.11 a). However, no such crystallization was observed at the sidewall GaN/oxide interface (Figure 3.11 b)). Therefore, it can be inferred that the oxide was amorphous on the sidewall. For the second sample, since AlGaN was used, regrown AlGaN layer was identified and characterized. Additionally, an AlN marker layer was also added as shown in fig. 3.12 and fig. 3.13 to identify the regrown GaN/AlGaN interface. The thickness observed on the c-plane was as targeted (~10 nm). However, on the sidewall, a thinner interlayer was observed (~5nm). Similar results were obtained for both *a*- and *m*-plane sidewalls. More details regarding regrowth conditions are described in the later sections.

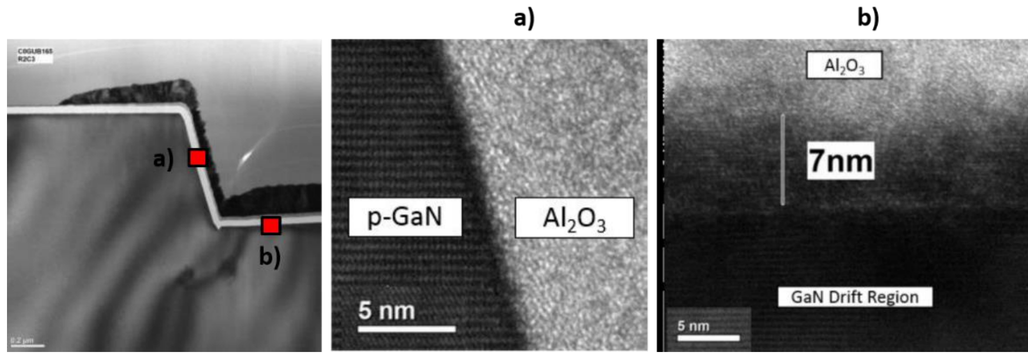


Figure 3.11: TEM images of GaN interlayer sample. No Al_2O_3 crystallization occurs on the sidewall as can be seen from a). However, on the etched c-plane Al_2O_3 crystallizes (b). It can be seen from the left figure that Al_2O_3 thickness on sidewall and c-plane was almost similar. (Copyright © 2016, IEEE)

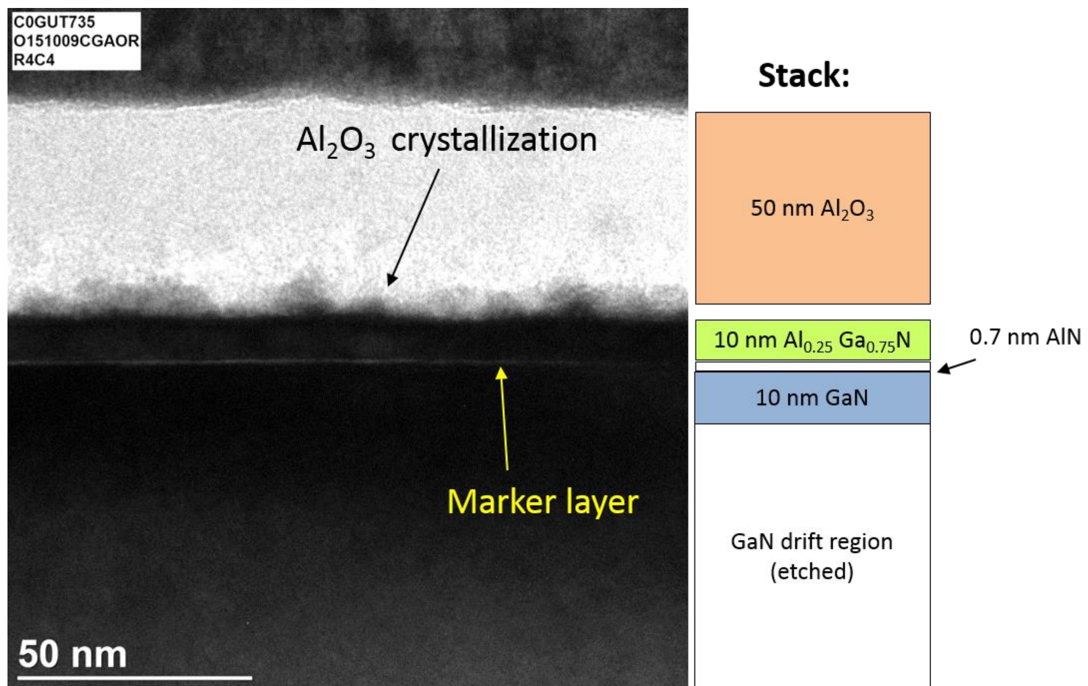


Figure 3.12: The c-plane cross-section TEM image of the second sample. Here, a thin AlN interlayer was grown to identify the GaN/AlGaN interface. Here, it can be clearly observed that AlGaN regrows followed by Al_2O_3 growth. Non-uniform crystallization of Al_2O_3 can be observed as well.

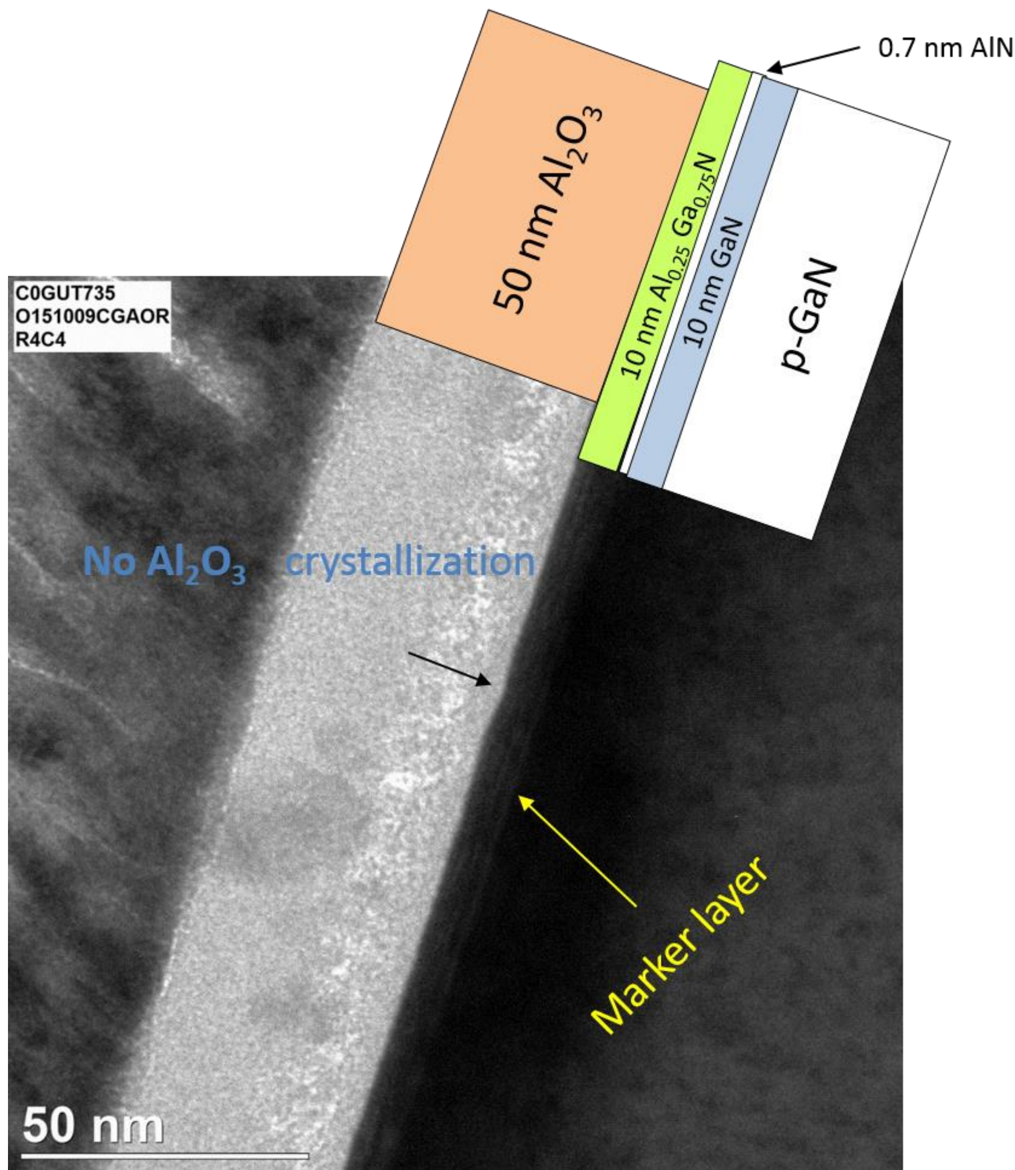


Figure 3.13: The c-plane cross-section TEM image of the second sample. The AlGaN layers and marker layer are clearly visible. The amorphous nature of the oxide was again observed on the sidewall. It should be noted that the lower AlGaN thickness (~5nm) was observed on the sidewall compared to c-plane regrown AlGaN (~10 nm).

The GaN interlayer regrowth was followed by the in-situ deposition of the gate-dielectric. This is very important as an *in-situ* deposition of the gate-dielectric improves semiconductor/dielectric interface and channel properties compared to an *ex-situ* dielectric

deposition. MOCVD grown aluminum oxide (Al_2O_3) deposited at 700° C was predominately used as the gate-dielectric in this dissertation [39]. This dielectric was extensively studied through c-plane GaN planar *in-situ* MOSCAPs. In the later stages of this dissertation, Si alloyed aluminum oxide (AlSiO) was used due to improved gate-dielectric characteristics. The thickness of MOCVD Al_2O_3 and AlSiO were kept 50 nm and 60 nm throughout this dissertation.

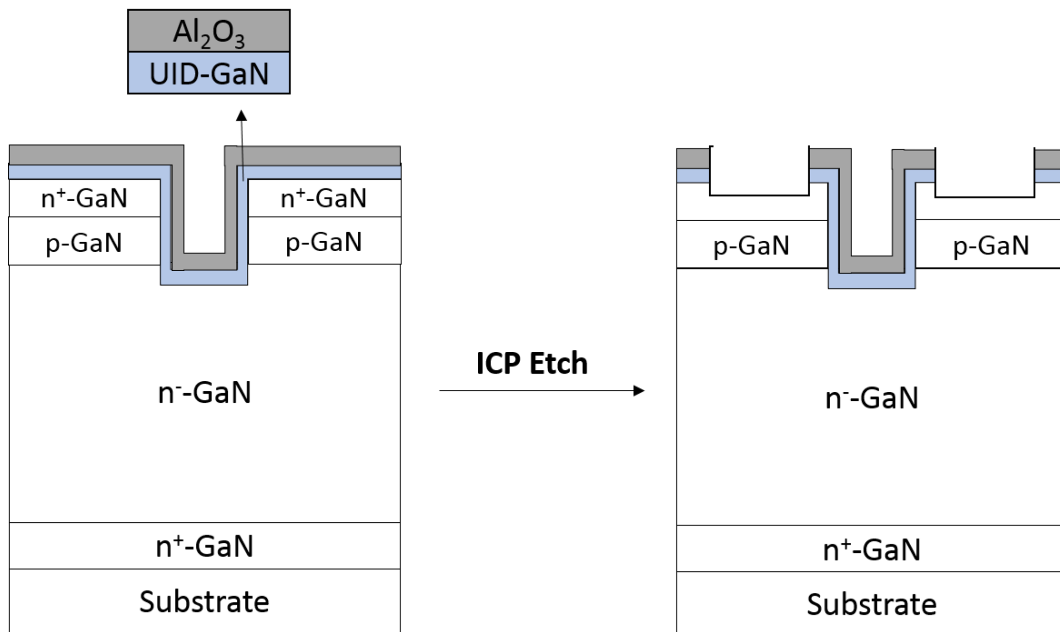


Figure 3.14: Cross-sectional schematic after source etch.

After the MOCVD regrowth, the gate-dielectric (Al_2O_3) and UID-GaN interlayer were etched in an inductive coupled plasma (ICP) system using CF_4/O_2 (Recipe #134) gas mixture (Figure 3.14). The non-selective nature of dielectric and GaN interlayer etch results in source region etch as well. In this dissertation, this etch was timed such that 20-40 nm of source region was etched. This was done to ensure n^+-GaN region exposure to form good ohmic (source) contact.

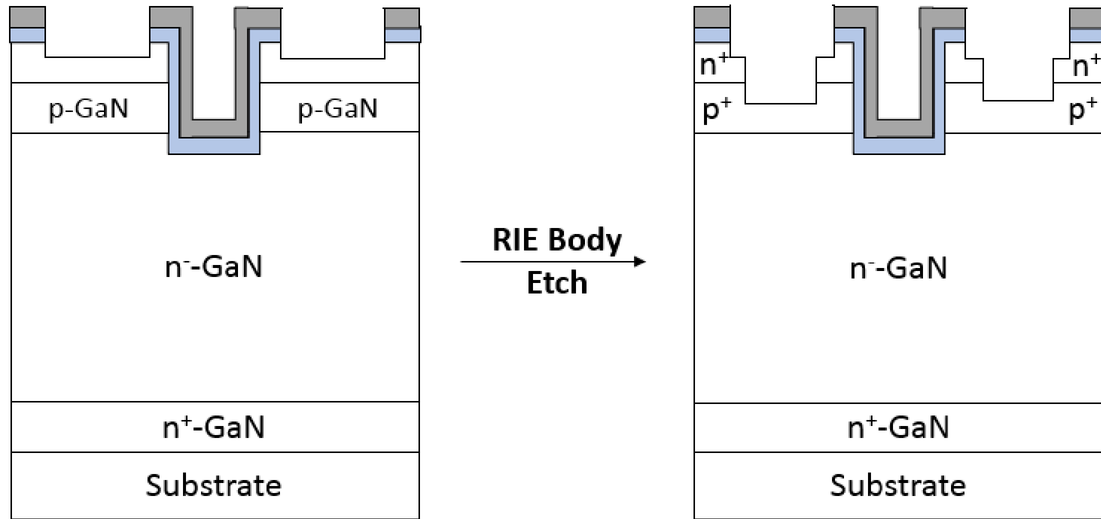


Figure 3.15: Cross-sectional schematic after body etch.

Thereafter, in the exposed source region (n^+-GaN) from previous CF_4/O_2 etch, a part of the source region (n^+-GaN) was etched to activate and form contact to the p-GaN body region (Figure 3.15). This etch was performed in a reactive ion etching (RIE) system with BCl_3/Cl_2 gas mixture at a low power of 15 W. The etch utilized for this step was same as the low damage gate-trench etch described earlier. However, the non-selective nature of this etch results in the etching of p-GaN. In this dissertation work, this RIE etch was timed to etch 30-40 nm of p-GaN. A higher damage etch or deeper etch into p-GaN could result in source-drain leakage. Since, the body (RIE) etch penetrated p-GaN, a recovery anneal was performed in the MOCVD (10min in N_2 /NH_3 at 875 °C) chamber to mitigate type conversion of p-GaN to n-GaN. Following MOCVD recovery anneal, the samples were again annealed in N_2/O_2 ambient (air) at 700 °C for 15 minutes to activate the p-GaN prior to electrode depositions.

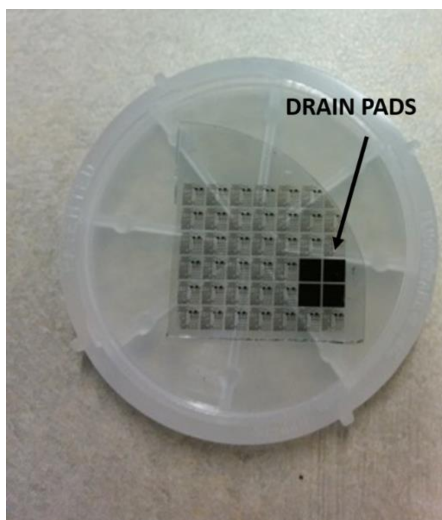


Figure 3.16: Image of a GaN on sapphire OG-FET wafer. These large dark squares were used as the drain contact for the devices present in other dies.

Un-annealed Ti/Au (30nm/200 nm) deposited by electron beam deposition (E-Beam 1) was used as the source, body, gate, and the drain electrode. However, in the later stages of this dissertation, Ni was used as the body contact metal. Since, gate electrode requires conformal deposition on the gate dielectric, Ti was chosen, as it had a better adhesion than Ni or other high work function metals. For devices fabricated on bulk GaN substrates, the drain contact was made on the backside. However, for GaN on sapphire samples, a large area pad (3 mm x 3 mm) was deposited on the surface for the drain contact as shown in the fig 3.16.

Thereafter, mesa isolation was performed for these devices. Low damage etch is again required to reduce sidewall leakage and early breakdown of the device. Therefore, the gate trench etch was used for mesa isolation. It should be noted that the device process described here lacks edge termination and passivation. To obtain high voltage OG-FETs, edge termination is imperative. The edge termination process for high voltage OG-FETs will be described later in this chapter.

The complete device fabrication process without edge termination is shown in fig. 3.17.

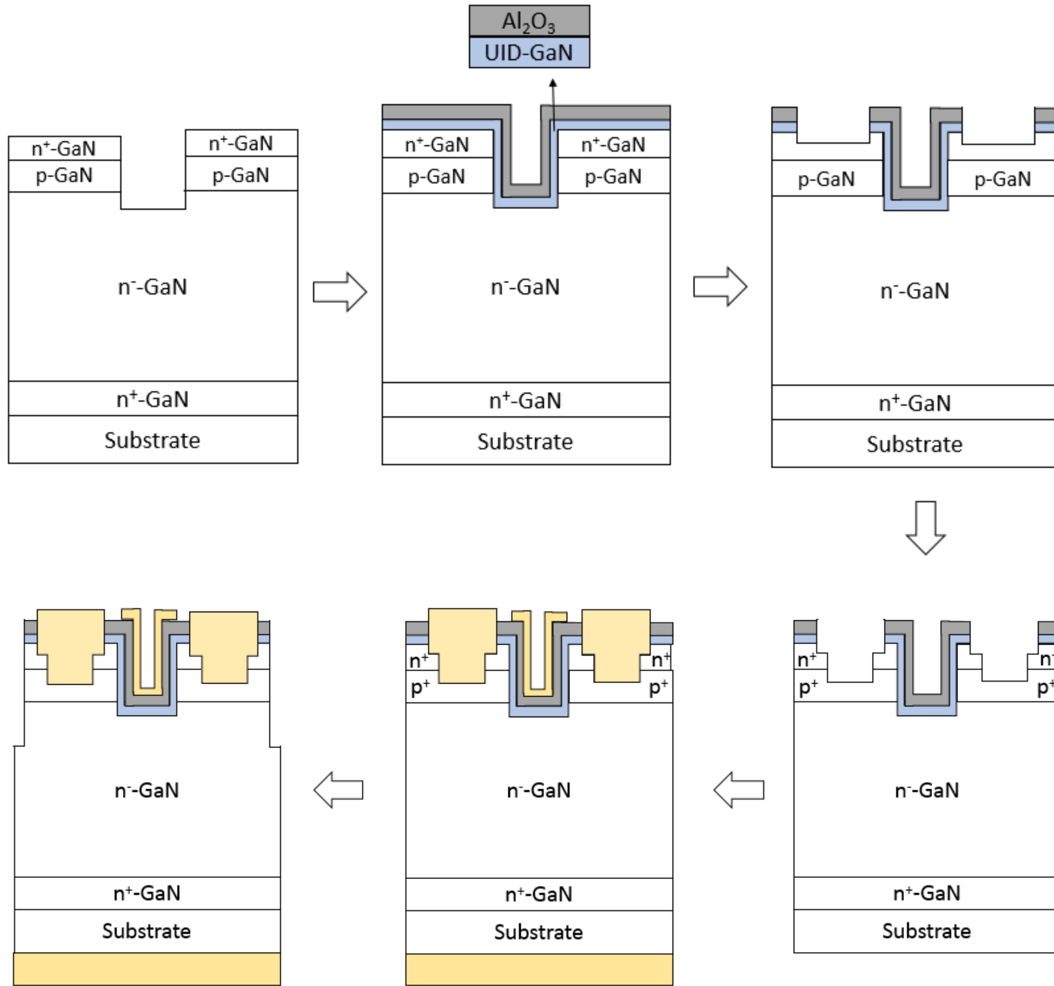


Figure 3.17: Device fabrication process of OG-FET. The fabrication process starts with the formation of trench structures followed by MOCVD regrowth. Thereafter, source and body etches were performed followed by electrode deposition and device isolation.

3.3 Important Fabrication Modules

In this section, the important fabrication modules for OG-FET will be discussed. Three important modules were identified and studied in detail.

3.3.1 Etch

Trench-gate etch is perhaps the most important fabrication module in the OG-FET fabrication process. Dry etch is used for trench-gate etch process due to the absence of simple wet etch technology to transfer lithographic patterns in nitrides. Dry etch has been known to cause crystal defects such as vacancies or/and interstitials in GaN [10]. Since, the high electric fields in the off-state at high drain bias are going to occur along the trench, the etch damage must be minimized. Many approaches to heal this etch damage and recover electrical characteristics have been studied [55], [56]. However, only partial recovery of damaged active regions has been achieved with high temperature anneals (> 900°C), therefore, avoiding any etch damage or minimal etch damage is preferred.

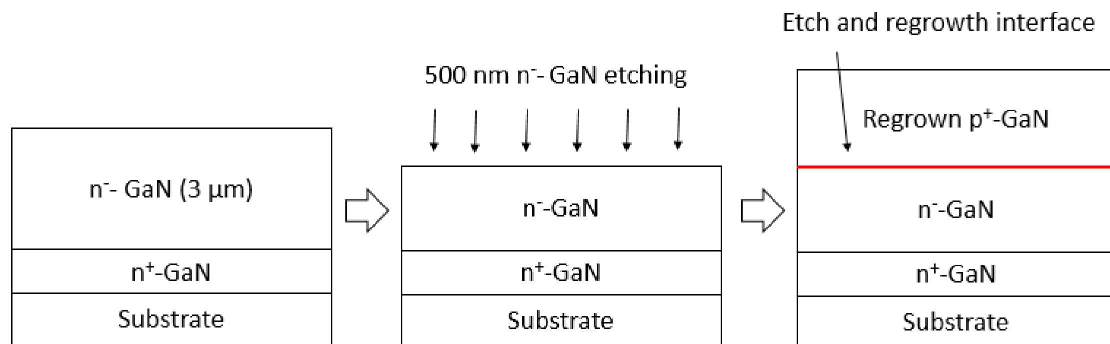


Figure 3.18: Etch damage study process flow by fabricating etched and regrown p-n diodes.

Etch damage studies were performed using regrown p-n diodes in collaboration with Ryo Tanaka. In this study, the n-type GaN was dry etched (~500 nm) followed by the regrowth of p-GaN on the etched surface (Figure 3.18). Prior to p-GaN regrowth, the samples underwent cleaning processes such as UV ozone and HF treatment and TMAH treatment as described earlier. Regrown p-n diode test structure was chosen as the active region was on the etched region and peak field occurs at the etched and regrown p-n junction. The off-state behavior was used as an indicator for the etch damage. Two low damage etches developed in Mishra

group were used. The first dry etch was done in an inductively coupled plasma (ICP) system with Cl_2/Ar at a high power of 75 W (300 W). Details of this etch and its development can be found in ref. [57]. The other etch was a low power (15 W), low pressure (10 mT) BCl_3/Cl_2 etch performed in a RIE system. The former etch was faster with an etch rate of approximately 150 nm/min while the latter etch rate was 6 nm/min. The etch profiles of both etches ICP and RIE are shown in fig. 3.19 and 3.20 respectively. Both etches were vertical with 10-15° from vertical and had low surface roughness on the etched surface (Figure 3.21). Different etch profiles were observed for both etches. For an ICP Cl_2/Ar etch, a notch shape feature can be observed at the trench corner. This was undesirable as it could potentially give rise to electric field at the trench corner. Additionally, during GaN regrowth, this region under mass reflow can get heavily doped. With similar etch profiles in SiC, high breakdown voltage proved to be difficult to obtain.

However, for RIE etch, a 'shoe' type feature was observed at the trench corner which could help in alleviating or managing the electric field at the trench corner. The difference in two etch profiles is also related to the nature of how these etches work. The ICP high power Cl_2/Ar was more physical etch while RIE low pressure, low power BCl_3/Cl_2 etch behaves more like a chemical etch.

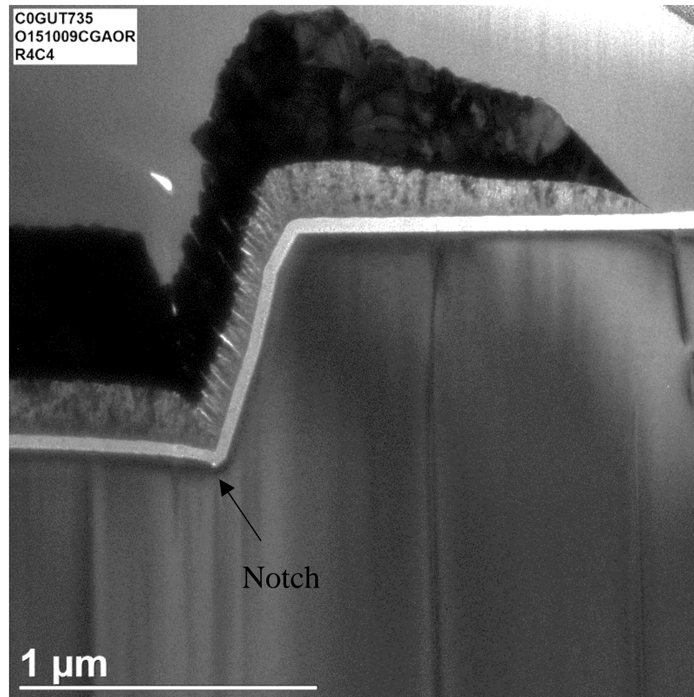


Figure 3:19: Cross-sectional transmission electron microscopy (FIB-TEM) image of ICP gate-trench etch.

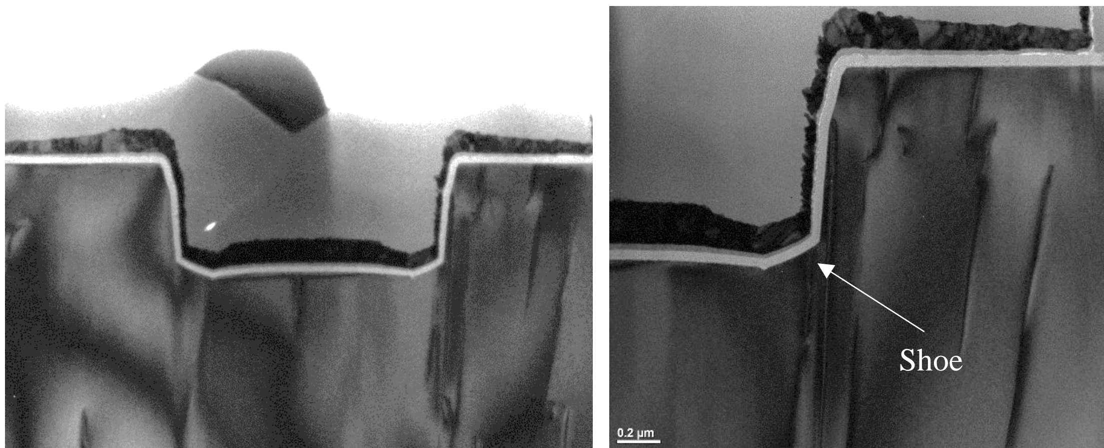


Figure 3.20: Cross-sectional transmission electron microscopy (FIB-TEM) image of RIE gate-trench etch.

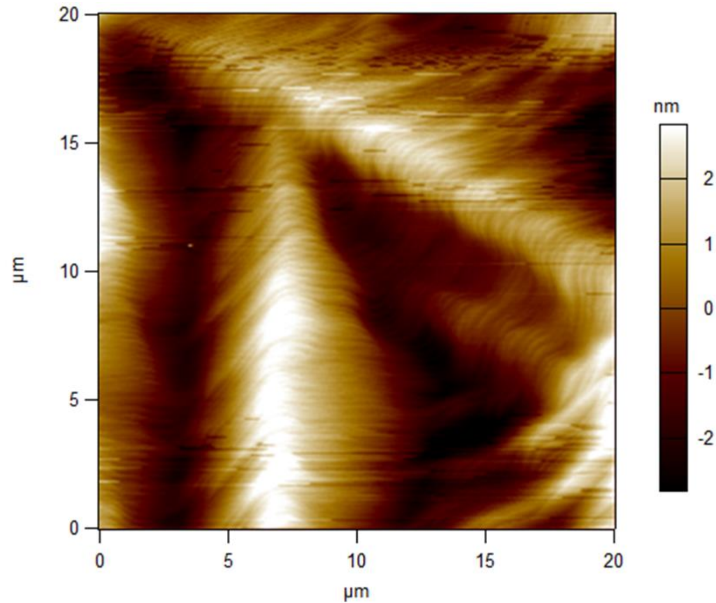


Figure 3.21: AFM of a test sample after dry etch.

The current voltage characteristics are shown in fig. 3.22. The samples that underwent ICP etch demonstrated almost no or less than one order of magnitude of rectification. However, with RIE low power etch, 6 orders of magnitude of rectification were observed. Multiple variations of p-GaN regrowth conditions were modified such as regrowth temperature, carrier gas, Mg pre-flows prior to Ga flow etc., however, no (different) significant trends in the I-V characteristics were observed. The results obtained from this study clearly demonstrate that the damage from etching was a dominant variable and the low power RIE etch is less damaging and more likely to produce high voltage OG-FETs. In the initial development part of this dissertation work, ICP etch was used, later, RIE etch was used to produce high voltage OG-FETs (> 200 V_{BR}).

As etch mask, both oxide (SiO_2) and photo-resist options were available. Due to the low etch rate of the RIE etch (~5-6 nm/min) and deep trench requirement (> 500 nm), using photo-resist mask (SPR 220-3) was challenging. Since, this etch would require approximately 90-150

min. depending on the desired depth, the heating of the photo-resist was a potential problem. On the other hand, hard mask (oxides) requires additional processing steps. Therefore, easy solution to photo-resist heating issue was developed. To circumvent the potential heating of photo-resist, etch was broken into equal time intervals with a maximum permissible time of 30 min. For example, a 112 min. etch was divided into 4 intervals of 28 min. each. After every etch interval, a nitrogen (N_2) pump-purge-pump cycle was introduced to avoid heating of the resist. This enabled a photo-resist mask to be used without taking the sample out of RIE chamber in between.

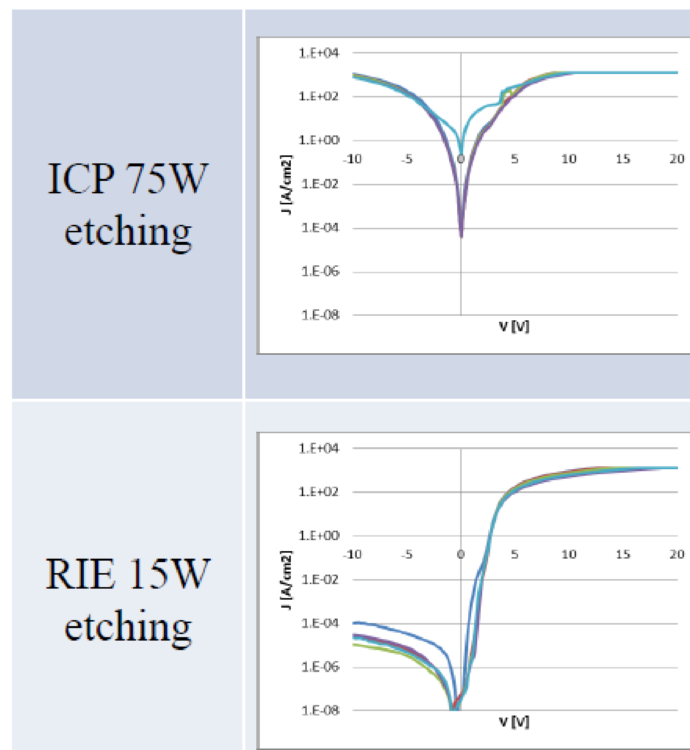


Figure 3.22: I-V characteristics of regrown p-n diodes with ICP and RIE etch. High reverse leakage was observed with ICP etch compared to RIE etch.

The depth of the trench-gate etch is an important factor in determining the breakdown voltage of the device. To allow the current flow and no barrier in the electron flow from the

source into the drift region, the depth of the trench should be greater than the sum of thicknesses of source and the body region. However, simulations (performed by Dong Ji, UC Davis) show that with increasing trench depth beyond the body region, the peak field increases in the off-state and causes early breakdown of the device (Figure 3.23 and 3.24).

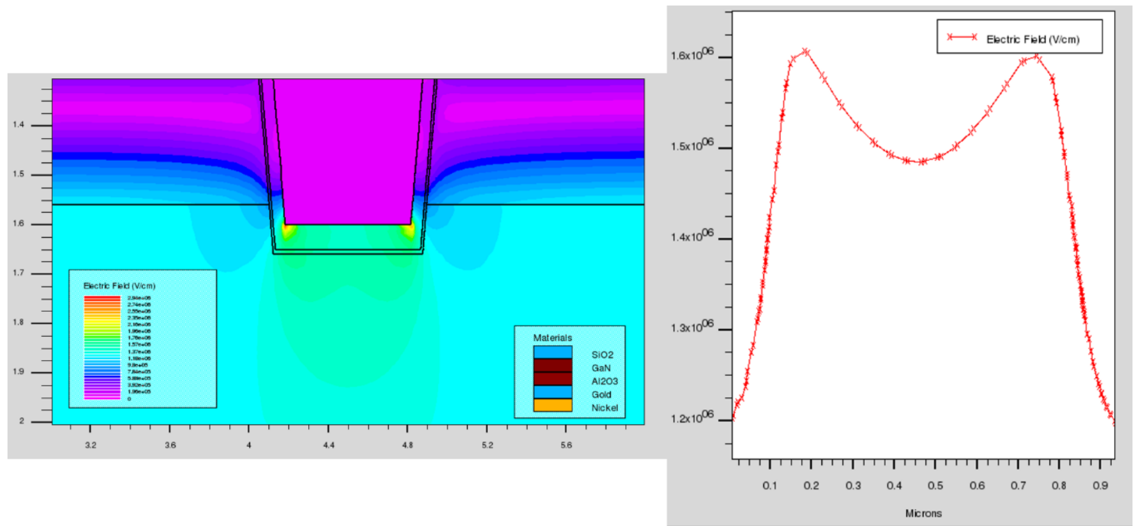


Figure 3.23: Electric-field profile for 100 nm over-etch (beyond the p-GaN into the drift region). The peak electric field occurs at the trench corner with E_{PEAK}~1.6 MV/cm.

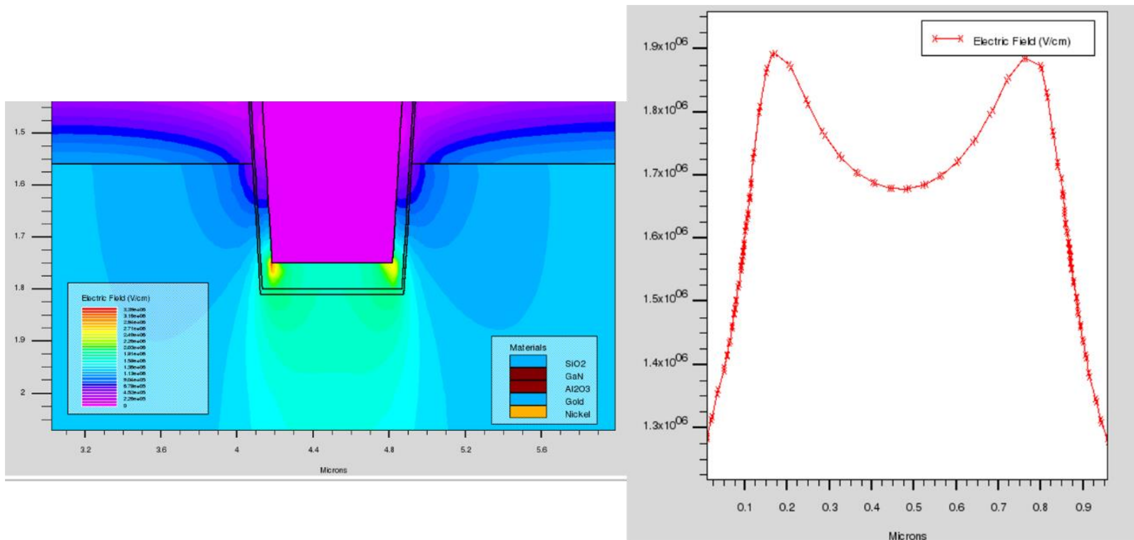
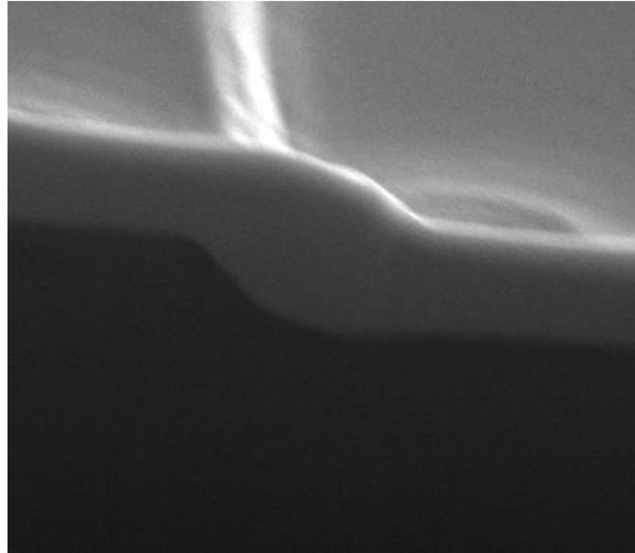


Figure 3.24: Electric-field profile for 250 nm over-etch (beyond the p-GaN into the drift region). Apart from over-etch depth, all the parameters were kept similar to simulations shown in fig. 3.23. The E_{PEAK}~ 1.9 MV/cm and higher than the 100 nm over-etch case. Therefore, minimizing over-etch is preferable to obtain high voltage devices.



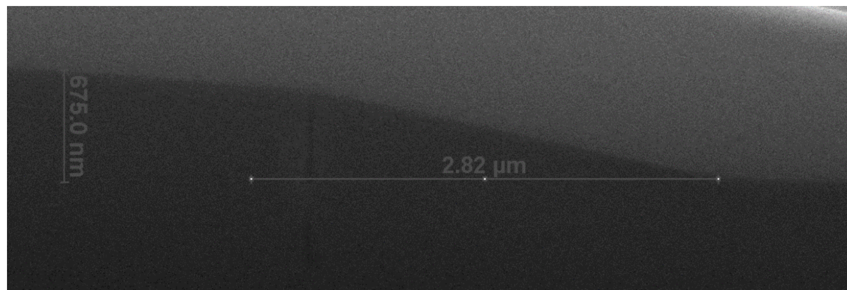


Figure 3.25: 45° angle (top) and 15° angle (bottom) etch profiles with thermal photo-resist reflow technique.

Therefore, to obtain good off-state performance and manage peak electric fields in the device, the over-etch should be minimized. In this dissertation, the trench over etch was targeted to be between 50 nm-250 nm.

Even though vertical etch is preferred in the trench, angled etches may be required either in the trench or in the isolation mesa region to manage high electric fields [58]. Therefore, alongside vertical, low damage shallow angle etches were also developed. The concept of thermal photo-resist reflow was used to obtain shallow angle etches. Two etches were developed with 45° and 15° angle from horizontal-plane respectively. To obtain these, immediately after the development of the exposed photo-lithographic pattern, the sample (or photo-resist (SPR-220-3)) was heated for 5 min. at 110°C (Courtesy: Dong Ji) and 150° C for 45° and 15° angled etches respectively (Figure 3.25). Temperature can be varied to obtain other desired angles. RIE low power (15 W), low pressure (10 mT) BCl_3/Cl_2 etch as described earlier was used for etching the underlying GaN.

3.3.2 MOCVD Channel Regrowth Process

The trench channel regrowth process is an important module in the OG-FET fabrication process. Prior to the MOCVD regrowth, the sample must be cleaned. In this work, before regrowth, a UV Ozone and HF treatment was done and the samples were immediately transferred to the MOCVD reactor. This treatment reduces residual Si, which is commonly observed at regrowth interfaces. The presence of Si can result in negative threshold voltage shift and can cause early breakdown of devices. The MOCVD regrowth was a two-step process. First, the samples were annealed in N_2/NH_3 for 30 min. at 930 °C to recover trench-gate etch damage. Following annealing, the UID-GaN interlayer on the sidewall is grown on the sample. The GaN interlayer regrowth was followed by the in-situ deposition of the gate-dielectric. In the initial stages of this work, only the GaN interlayer regrowth conditions were optimized while the annealing conditions and gate dielectric growth was kept the same. The impact of the GaN interlayer thickness, temperature and carrier gas was studied by fabricating

OG-FETs and evaluating the impact on device characteristics. These regrowth process development studies were performed on GaN on sapphire OG-FETs due to expensive bulk GaN substrates. First, a GaN interlayer thickness series experiment was performed as discussed below.

3.3.2.1 GaN interlayer thickness series

In this experiment, the GaN interlayer thickness was varied while other parameters were kept the same. The epitaxial stack is shown in fig. 3.26. For this experiment, a 75 W Cl_2/Ar ICP etch was used to obtain vertical sidewalls. After the trench etch, the samples went through MOCVD regrowth process where two different GaN interlayers with thicknesses of 10 nm and 30 nm were deposited [42]. In addition, a sample without a GaN interlayer (0 nm) was also grown to compare the OG-FET with the trench MOSFET. The GaN interlayer regrowth was followed by 50 nm thick MOCVD Al_2O_3. The fabrication process that followed is described in the device fabrication process section. Ti/Au (30nm/200 nm) was used as contact for body, source, drain and gate. The device cross sectional schematic is shown in fig. 3.26.

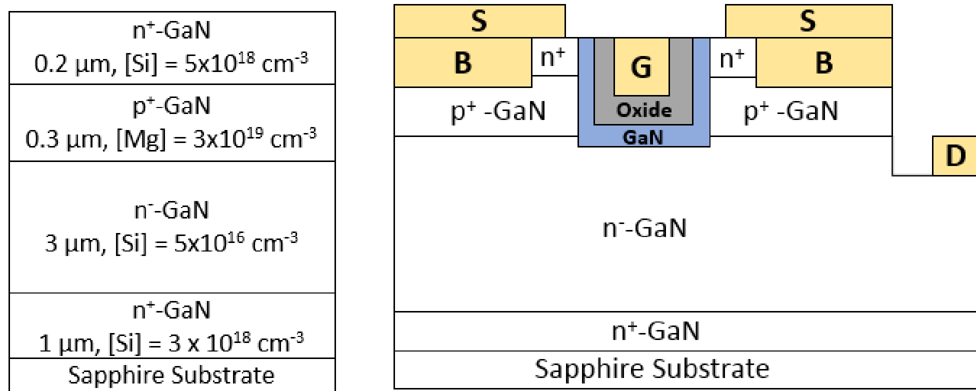


Figure 3.26: Epitaxial structure (Left) and cross-sectional schematic for GaN interlayer series experiment.

The DC characteristics of drain current (I_{DS}-V_{DS}) normalized by the gate-width (trench-width +trench-length = 164μm) for different GaN interlayer thickness at several gate voltages is shown in fig. 3.27 [42]. The drain current density was significantly higher in the devices with the GaN interlayer in comparison with the one with no interlayer. This is a strong evidence of the enhancement in the electron mobility in the channel. As the GaN interlayer thickness increases, the channel is spaced further away from the p-GaN interface, thereby increasing electron mobility. Almost similar current density was observed for samples with GaN interlayers potentially due to on-resistance being limited by the drift resistance [42].

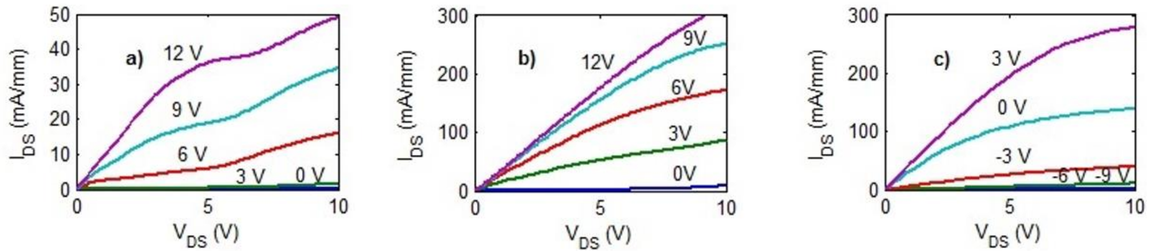


Figure 3:27: Output I–V characteristics ($I_{DS} – V_{DS}$) normalized by the gate-width for different GaN interlayer thickness 0 nm (a), 10 nm (b) and 30 nm (c) at different gate voltages in steps of 3V. (Copyright © 2016, IEEE)

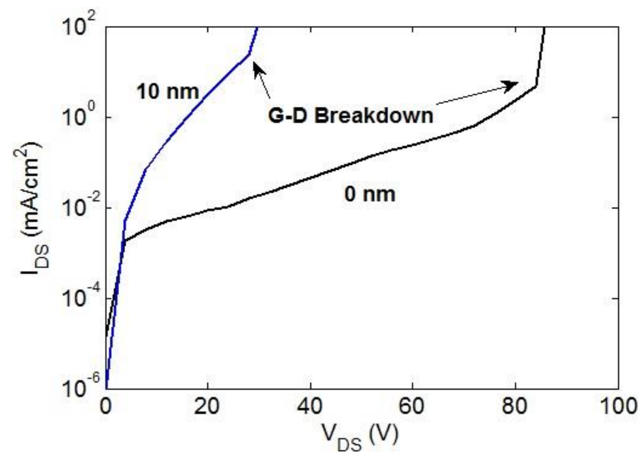


Figure 3.28: Breakdown characteristics for 0 nm and 10 nm GaN interlayer at V_{GS} =-5 V. (Copyright © 2016, IEEE)

It can also be noticed from fig. 3.27 that the 30 nm GaN interlayer sample was normally-on. However, 0nm and 10 nm GaN interlayer samples were normally-off. These results are in accordance with the discussion in sec. 3.1 (Fig. 3.4). As GaN interlayer thickness increases, the conduction band comes closer to the fermi level and therefore, the threshold voltage decreases.

Figure 3.28 shows the breakdown characteristics of devices with 0 nm and 10 nm GaN interlayer thickness. The breakdown in both devices occurred at the gate-drain junction and was catastrophic in nature. The 30 nm GaN interlayer thickness sample suffered from source-drain leakage. The device with no GaN interlayer achieved a breakdown voltage of 85 V. The breakdown occurred at the gate-drain junction and was catastrophic in nature. The low breakdown and source-drain leakage in devices with GaN interlayer indicates the presence of positive charges at the regrown interface or in the regrown GaN interlayer [42]. The positive charges could arise from the etch damage and subsequent regrowth. Therefore, regrowth conditions need to be further optimized to improve device breakdown. The high source-drain leakage could also be due to the passivation (by H_2 carrier gas in MOCVD chamber) of p-GaN during regrowth.

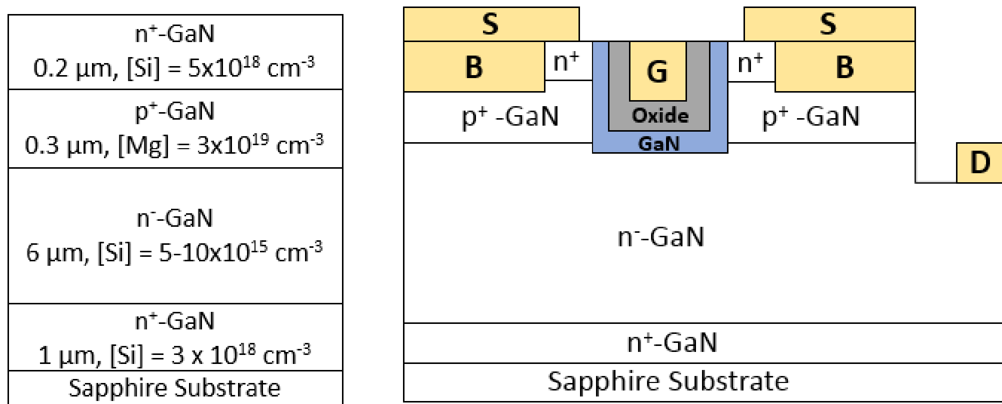


Figure 3.29: Epitaxial structure (Left) and cross-sectional schematic for carrier gas experiment.

3.3.2.2 Carrier gas (N_2 vs H_2) used during GaN interlayer regrowth

Since, one of the possible causes for source-drain leakage could be passivation of p-GaN on the sidewall, in this experiment, impact of carrier gas during GaN regrowth was studied. Since, hydrogen (H_2) can potentially passivate the magnesium (Mg) ions near the etched surface (by forming complex MgH_2), thereby, causing reduced threshold voltage and increased source-drain leakage, a non-Mg passivating carrier gas should be utilized. Therefore, in this experiment, 10 nm thick GaN interlayer was grown in H_2 for the first sample and N_2 for the second sample. The device fabrication process was similar to the process described in the previous section (3.3.2.2). The epitaxial stack and cross-sectional schematic is shown in the figure 3.29.

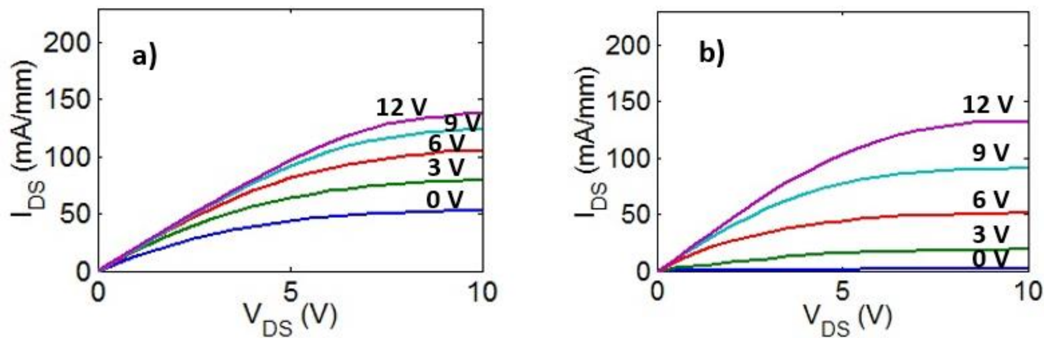


Figure 3.30: Output I–V characteristics ($I_{DS} - V_{DS}$) for H_2 (a) and N_2 (b) carrier gas normalized by the gate-width.

The DC characteristics of drain current (I_{DS}-V_{DS}) normalized by the gate-width for H_2 and N_2 as carrier gas at several gate voltages is shown in fig. 3.30. As noticeable from the figure, the current densities of both the samples were comparable. However, source-drain leakage was much higher in the sample grown with H_2 as carrier gas. The hydrogen gas during GaN interlayer regrowth could potentially passivate the buried p-GaN layer, add undesirable positive charge at the regrowth interface and affect the regrowth interface due to uncontrolled

etching of GaN in hydrogen. Nitrogen, as carrier gas, alleviates these aforementioned problems to a certain extent, as demonstrated by the device results. A reduction in source-drain leakage and higher breakdown voltage was observed (Figure 3.31) with N_2. The H_2 sample demonstrated high source-drain leakage and did not pinch-off.

Therefore, GaN interlayer regrowth was then performed with N_2 as the carrier gas and thickness was kept at 10 nm.

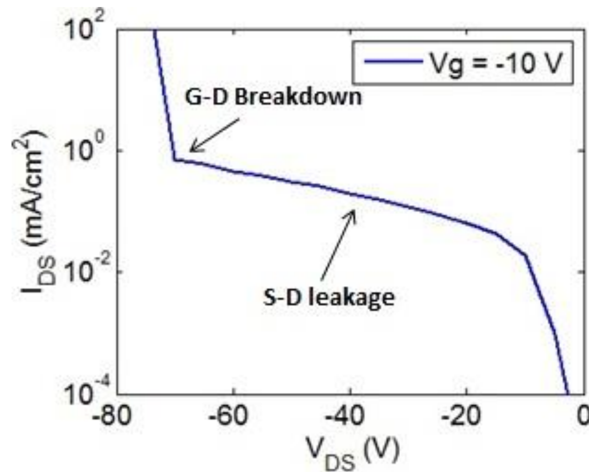


Figure 3.31: Off-state characteristics of N_2 sample.

3.3.2.3 GaN interlayer regrowth temperature series

After the GaN interlayer thickness and carrier gas optimization, the GaN interlayer regrowth temperature series was performed. Regrowth temperature plays an important role in the incorporation of impurities. Therefore, in this experiment, regrowth temperature was optimized. Since, mass reflow occurs at 950° C, the regrowth temperature was kept below 950° C [24].

In this experiment, both annealing and regrowth temperatures were modified. The annealing temperature was kept below the regrowth temperature for each regrowth. Three different GaN interlayer regrowth were performed on three samples as shown in fig. 3.32. The

device fabrication process was similar to the process described in the previous section (3.3.2.2). The epitaxial stack and cross-sectional schematic is shown in the fig. 3.33.

GaN IL thickness (nm)		Pre-Deposition Annealing (30 min)		GaN IL Deposition		
		Temperature (°C)	Gas Flows	Temperature (°C)	Gas Flows	Growth rate (A/s)
10	Reference	930	5L N_2 + 2L NH_3	950	2L N_2 + 5L NH_3	0.48
10		870	5L N_2 + 2L NH_3	890	2L N_2 + 5L NH_3	0.32
10		810	5L N_2 + 2L NH_3	830	2L N_2 + 5L NH_3	0.32

Figure 3.32: Pre-deposition annealing and GaN interlayer regrowth conditions.

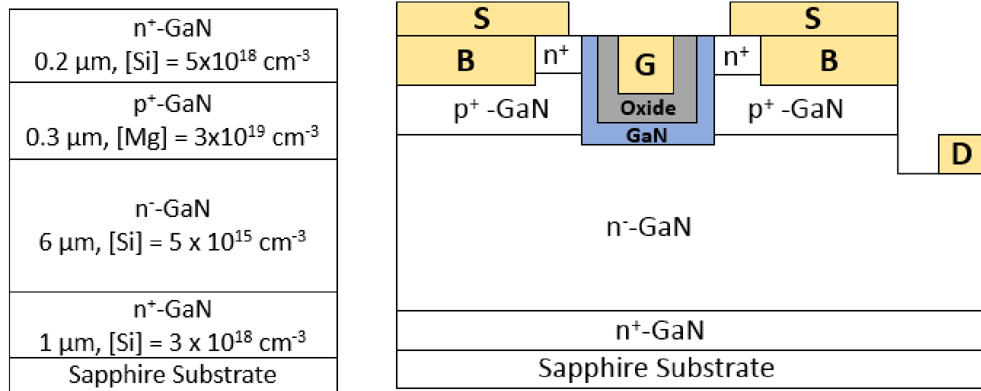


Figure 3.33: Epitaxial structure (Left) and cross-sectional schematic for GaN interlayer regrowth temperature experiment.

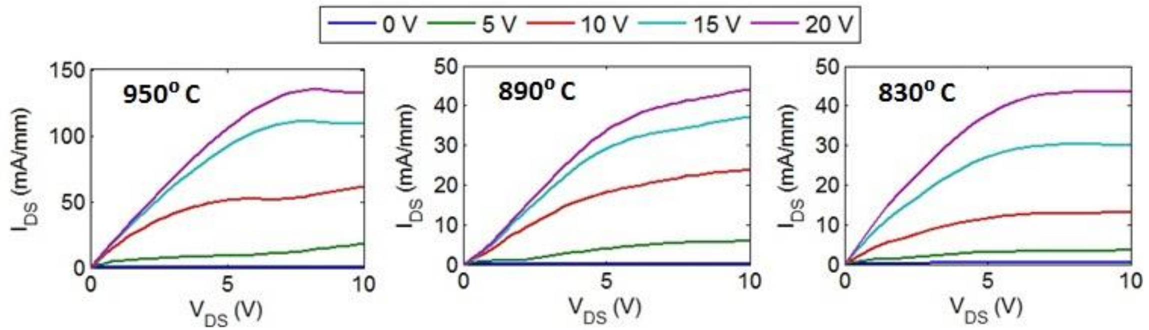


Figure 3.34: Output I-V characteristics for GaN interlayer temperature series.

The DC characteristics of drain current (I_{DS}-V_{DS}) for different GaN interlayer regrowth temperature at several gate voltages is shown in fig. 3.34. As noticeable from the figure, the current density decreases with a decrease in the regrowth temperature. The decrease in current density could be related to increased impurity incorporation with lower regrowth temperature. Impurity incorporation such as carbon could potentially result in reduced channel mobility and increased on-resistance.

With these experiments, GaN interlayer regrowth was optimized. In subsequent GaN interlayer regrowth, the regrowth temperature was kept at 950° C, N_2 was used as the carrier gas and 10 nm thick UID GaN was grown.

3.3.3 Edge termination

Large critical field of GaN compared to Si makes it an attractive semiconductor material for power devices. The critical field of GaN is more than 10 times higher than that of Si [5]. However, realizing this high critical field in GaN is not trivial at high breakdown voltages (>600 V). Due to field crowding effect at the device edge, breakdown voltages for devices are severely reduced. Therefore, development of proper edge termination is of paramount importance to realize the full potential of GaN power devices. Two major types of edge termination techniques have been reported for high voltage GaN devices; field plate based, and

junction termination by ion implantation [13], [34]. These edge termination studies were primarily reported using p-n diodes.

In this work, the field-plate based edge termination technique was adopted. Field plate studies were performed using GaN p-n diodes. We employed a spin-on-glass based field plate edge termination for p-n diodes [13]. Plasma enhanced chemical vapor deposition (PECVD) and atomic layer deposition (ALD) dielectrics were avoided due to the presence of hydrogen gas. Hydrogen can potentially passivate the p-GaN on the sidewall and can cause reverse leakage at higher voltages thus limiting the performance of field-plate based edge termination.

GaN p-n diode epitaxial structure was grown by MOCVD on bulk GaN substrates (Fig. 3.35). The growth of entire p-n stack on bulk GaN substrates was same as OG-FET epitaxial structure (until the p-GaN layer) except for one detail. The p-GaN layer was capped with a 15 nm thick, heavily doped p^{++}-GaN (Mg: 1 x 10^{20} cm^{-3}) cap layer to form good ohmic contact to the p-GaN (Fig. 3.35). The diode fabrication process started with depositing ohmic contact (Ni/Au) by electron beam deposition. This was done to prevent any surface damage to the p^{++}-GaN layer during subsequent processing steps [59]. Following the p-GaN contact, mesa isolation was performed. Mesa isolation employing two different mesa angles were performed on two samples to understand the impact of isolation etch profile on the breakdown voltage of GaN diodes. Low power 15 W BCl_3/Cl_2 etch was done in the RIE system to achieve vertical (15°) and angled isolation mesas (45°). Photo-resist thermal reflow technique was used to obtain angled mesa as discussed in previous sections. Thereafter, spin-on-glass was applied on the samples followed by SOG curing in N_2 at 425° C. An ICP etch was used to form the via and Ti/Au was used as the field plate metal. Finally, the diode fabrication process was

completed with the deposition of the backside contact. The cross-sectional schematics are shown in fig. 3.36.

p^{++}-GaN **15 nm, [Mg] = 1x10^{20} cm^{-3}**
p^{+}-GaN 0.3 μm, [Mg] = 3x10^{19} cm^{-3}
n^{-}-GaN 5 μm, [Si] = 8 x 10^{15} cm^{-3}
n^{+}-GaN 1 μm, [Si] = 3 x 10^{18} cm^{-3}
GaN Substrate

Figure 3.35: Epitaxial structure for p-n diode with p^{++}-GaN cap for ohmic contact.

In this experiment, devices were measured prior to the field-plate formation to allow comparison between the with-field plate and without-field plate results. The doping concentration was verified by C-V measurements on p-n diodes. The field-plate extended between 5-20μm beyond the isolation mesas.

The breakdown voltage observed prior to field–plate formation was between 600-700 V in both samples. Both repeatable (reverse leakage current limited) and non-repeatable (catastrophic) breakdown were observed in both samples as shown in fig. 3.37. No clear distinguishing features were observed between both samples prior to the field-plate process. After field-plate, no improvement in breakdown voltage was observed for both samples. However, for angled mesa sample, only catastrophic breakdown was suppressed. The absence of catastrophic breakdown indicated the effectiveness of angled mesa in reducing the peak electric field at the corners. However, the absence of improvement in the breakdown voltage with field-plate process was difficult to explain.

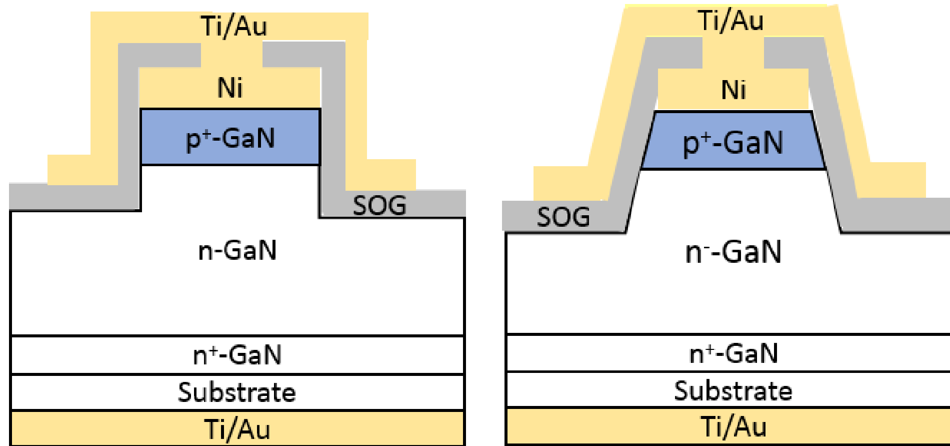


Figure 3.36: Cross sectional schematic of p-n diode with vertical (Left) and angled (Right) isolation mesa.

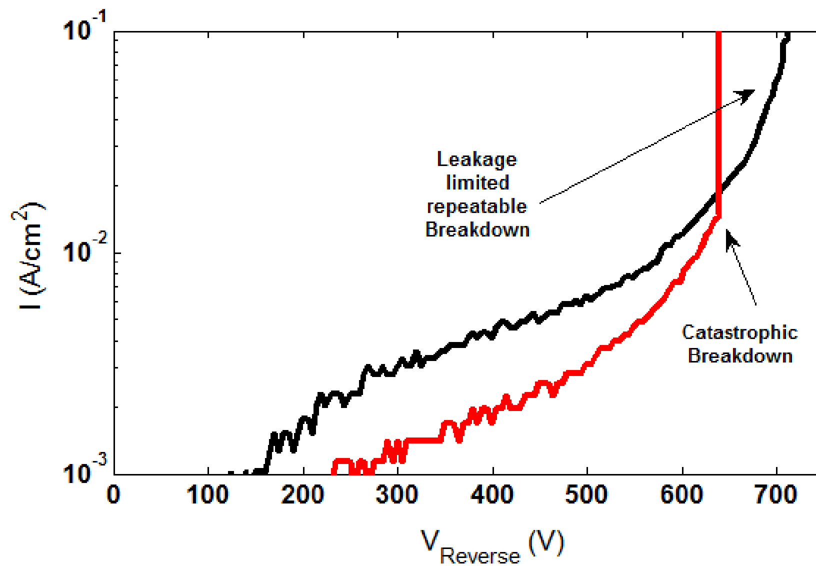


Figure 3.37: I-V characteristics of p-n diode without field-plate demonstrating catastrophic (non-repeatable) and leakage limited breakdown (repeatable).

The GaN drift region with 5 μm thickness and 8 x 10^{15} cm^{-3} carrier concentration gets fully depleted around 200 V reverse bias. Until a reverse bias of 200 V, the electric field in n^+-GaN was approximately zero. However, after that, the electric-field increases in n^+-GaN with

increased reverse bias. We hypothesized that electric field in n^+-GaN could result in electron-hole pair generation resulting in increased reverse leakage current near breakdown voltage.

Therefore, in the next experiment, thicker drift region (10μm) was grown with increased carrier concentration (1 x 10^{16} cm^{-3}) to reduce electric field in n^+-GaN. Here, the p-n diode was fabricated with a 45-degree angled mesa with the same fabrication process (SOG based field plate) as described in the last p-n diode experiment.

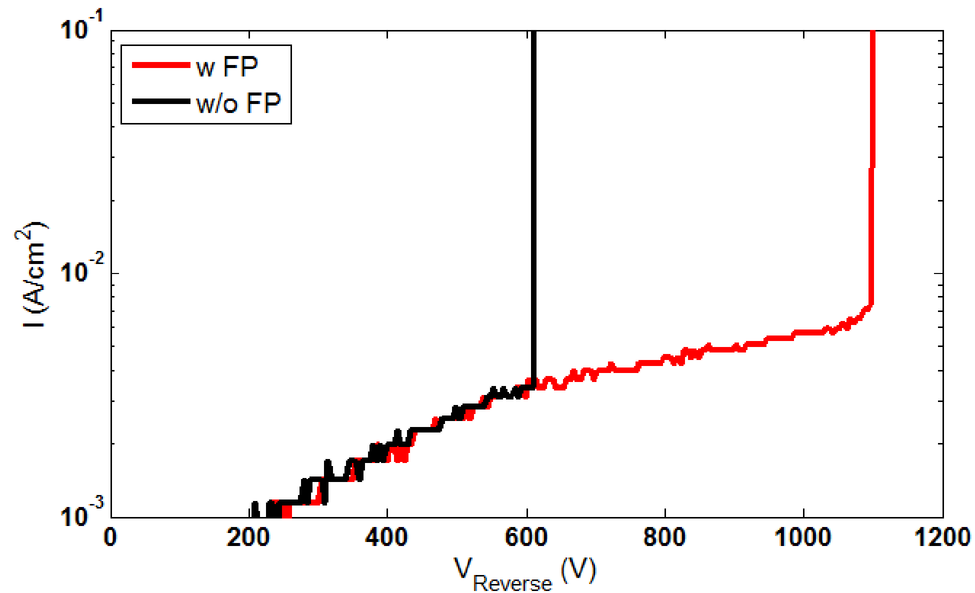


Figure 3.38: I-V characteristics for both with field plate and without field plate. Enhancement in breakdown voltage was observed with the SOG based field-plate process.

Here, the advantage of field plate was observed as the breakdown voltage improved from ~600 V to ~1100 V. The I-V characteristics are shown in fig 3.38. Catastrophic breakdown occurred at the p-n edge for both the with and without field-plate process (fig 3.39). This implies that the breakdown voltage could be further improved with improved field-plate design because with a near perfect edge termination avalanche breakdown would be observed [13]. It

should be noted that no clear dependence of breakdown voltage on field-plate extension on the isolated region was observed.

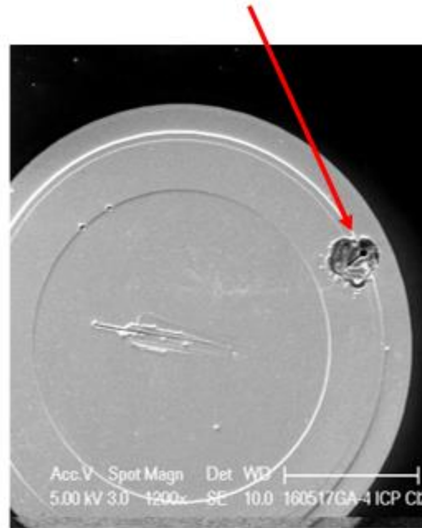


Figure 3.39: SEM image of a field-plated p-n diode after catastrophic breakdown.

These results illustrate the importance of edge termination in power devices. SOG based field-plate process was used in OG-FETs as well to enhance the breakdown voltage further. These results will be discussed in the next chapter.

3.3.4 Sidewall channel plane orientation

The trench MOSFET is a favorable device structure for reducing on-resistance owing to its high cell density and the absence of a JFET region. To obtain high cell density in vertical devices, devices are generally fabricated in a hexagonal grid structure [54]. The hexagonal crystal structure of GaN allows for the utilization of certain crystal planes as sidewalls upon which the MOS channel can be formed [60]. Understanding the impact of the planes on the channel characteristics is crucial to improving trench-gate device design and performance.

Therefore, trench-gate MOSFET and OG-FET devices with *a*- and *m*-plane-oriented sidewall channels were fabricated and characterized [60].

The cross-sectional schematics of the trench MOSFET and OG-FET are shown in fig. 3.40. The $n^+/p/n^+$ structure was used in this study to characterize the MOS channel properties without having resistance contributions from the drift region. It should be noted that the actual trench MOSFET device used for switching and sustaining high voltages has a thick n− drift region. Also, the MOS channel planes denoted in this study are not crystallographically accurate crystal planes since the MOS channel was formed on the trench sidewalls at a taper angle of 81°. The devices were hexagonal in shape and were oriented toward a- and m-plane sidewalls, as shown in fig 3.41. These devices were fabricated with low damage RIE trench-gate etch. Apart from the gate-trench etch, the entire fabrication process was same as described in previous sections.

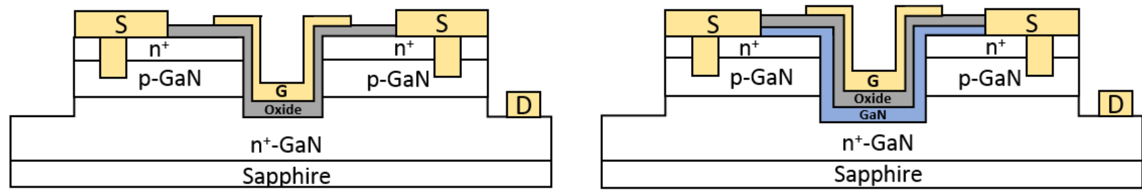


Figure 3.40: Cross-sectional schematic of trench MOSFET (left) and OG-FET (right) for sidewall channel comparison experiment.

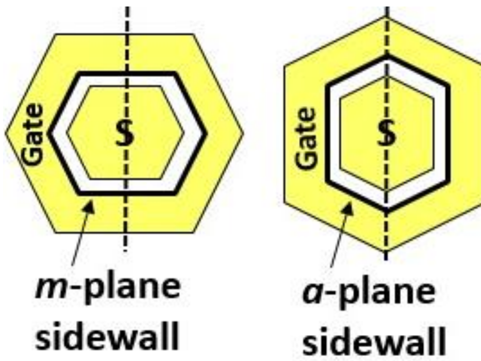


Figure 3.41: *m*-plane and *a*-plane oriented hexagonal shaped devices (Top view). Copyright, 2016, The Japan Society of Applied Physics.

The transfer I_{DS} –V_{GS} characteristics normalized by gate width for both *a*- and *m*-plane-oriented trench MOSFET devices at V_{DS} = 0.1 V is shown in fig 3.42. Both *a*- and *m*-plane-oriented devices demonstrated normally-off operation with threshold voltages of 6.1 and 6.3 V, respectively (calculated at I_{DS} = 1 μA/mm). Higher clockwise hysteresis (ΔV_{TH} ~ 0.4 and 0.2 V for *a*- and *m*-plane respectively) and higher sub-threshold slope (SS ~ 650 mV/dec and 480 mV/dec for *a*- and *m*-plane respectively) was observed for *a*-plane-oriented devices compared to *m*-plane-oriented devices.

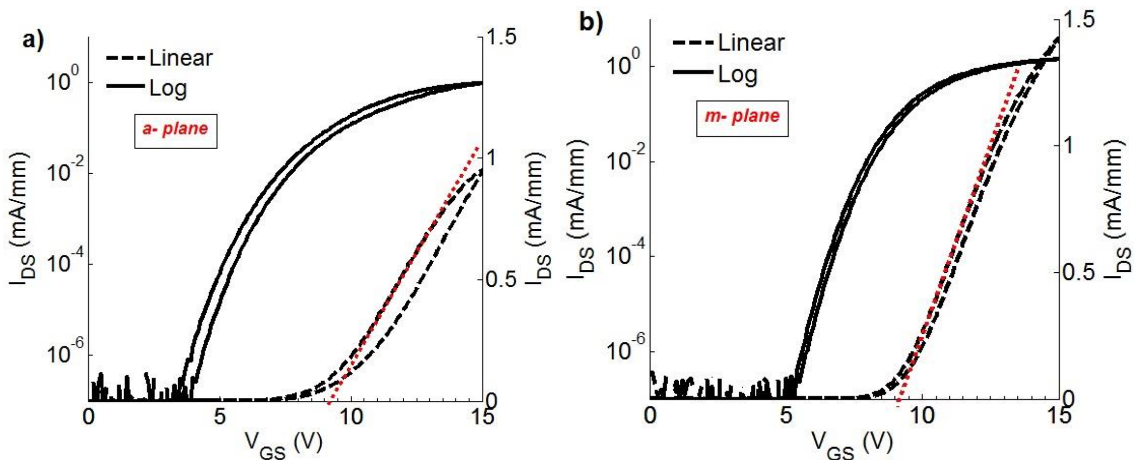


Figure 3.42: Transfer I-V charactertistics for trench MOSFET *a*-plane and *m*-plane sidewall channel devices at V_{DS} = 0.1 V. Copyright, 2016, The Japan Society of Applied Physics.

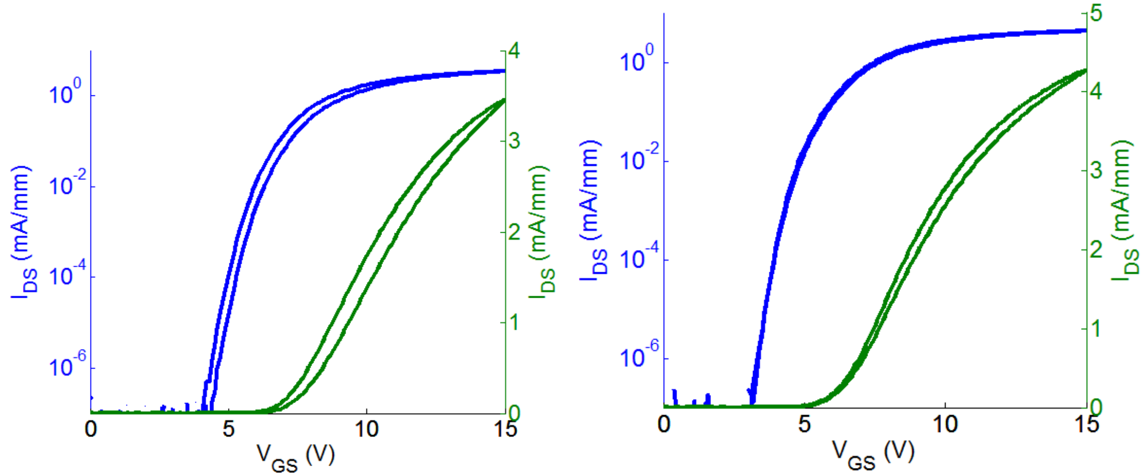


Figure 3.43: Transfer I-V charactertistics for OG-FET *a*-plane (left) and *m*-plane (right) sidewall channel devices at V_{DS} = 0.1 V.

The transfer I_{DS} –V_{GS} characteristics normalized by gate width for both *a*- and *m*-plane-oriented OG-FET devices at V_{DS} = 0.1 V is shown in fig 3.43. Both *a*- and *m*-plane-oriented devices demonstrated normally-off operation with threshold voltages of 5.4 and 4.3 V, respectively (calculated at I_{DS} = 1 μA/mm). Higher clockwise hysteresis (ΔV_{TH} ~ 0.3 and < 0.1 V for *a*- and *m*-plane respectively) and higher sub-threshold slope (SS ~ 330 mV/dec and 280 mV/dec for *a*- and *m*-plane respectively) was observed for *a*-plane-oriented devices compared to *m*-plane-oriented devices.

OG-FET devices show lower threshold voltage compared to trench MOSFET devices. This was expected as with GaN interlayer, conduction band will come closer to the fermi level. OG-FET devices also demonstrated improved channel properties compared with trench MOSFET devices such as lower SS, hysteresis etc.

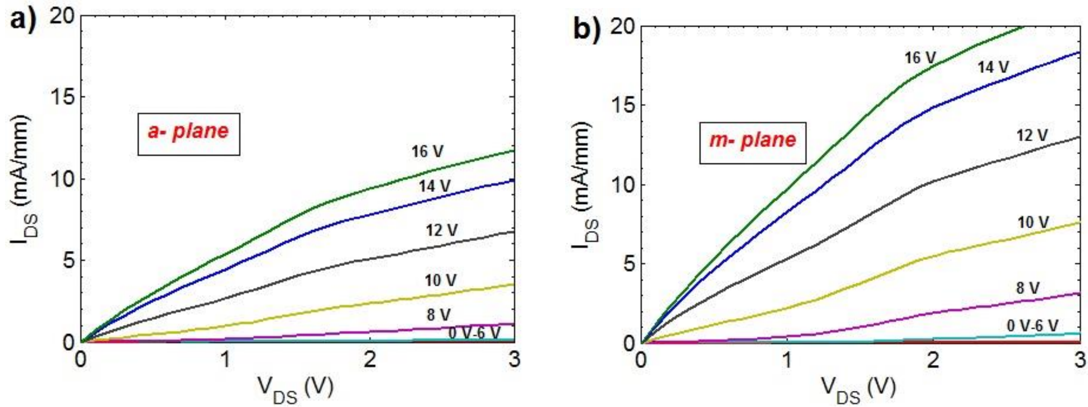


Figure 3.44: Output I–V characteristics ($I_{DS} – V_{DS}$) for (a) *a*-plane and (b) *m*-plane sidewall oriented trench-gate MOSFET at applied gate voltage range of 0 V-16 V in steps of 2 V. Copyright, 2016, The Japan Society of Applied Physics.

Figure 3.44 and figure 3.45 show the output DC characteristics ($I_{DS} –V_{DS}$) normalized by the gate width for both planes for both trench MOSFET and OG-FET respectively. The observed drain current density depended strongly on the MOS channel plane orientation. The drain current density was larger in *m*-plane-oriented devices than in the *a*-plane-oriented devices. The higher current density for *m*-plane-oriented devices indicates higher channel mobility for m-plane-oriented devices compared to *a*-plane-oriented devices.

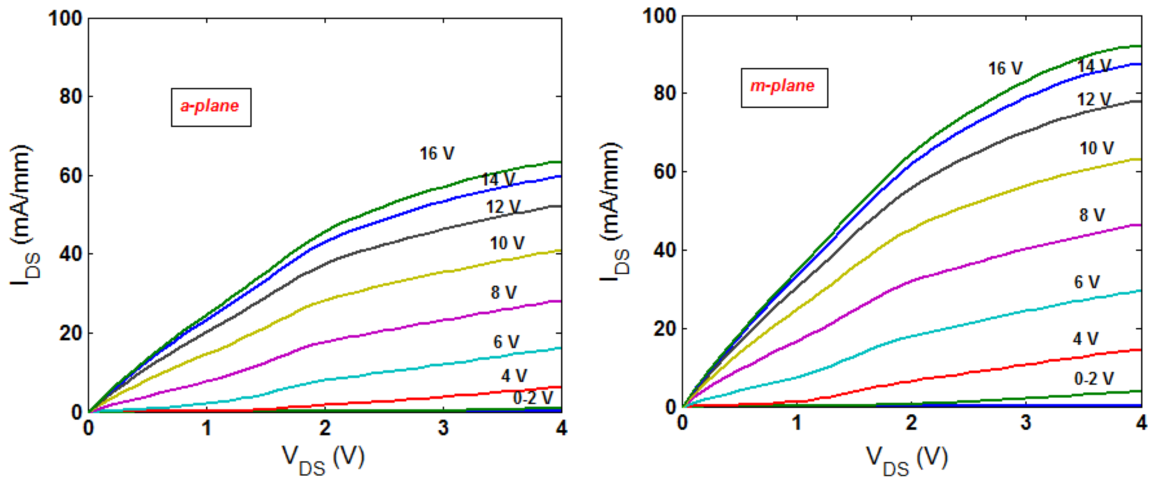


Figure 3.45: Output I–V characteristics ($I_{DS} – V_{DS}$) for *a*-plane (Left) and *m*-plane (Right) sidewall-oriented trench-gate MOSFET at applied gate voltage range of 0 V-16 V in steps of 2 V.

To confirm this, the field effect channel mobility as a function of gate voltage is shown in Fig. 3.46 for trench MOSFET and OG-FET. The channel mobility, μ_{CH}, was extracted from transfer I–V plots by using the following equation,

$$g_m = \left(\frac{dI_{DS}}{dV_{GS}}\right) = \frac{W}{L} C_{OX} \mu_{CH} V_{DS} \qquad 3.4$$

The maximum channel mobilities obtained in both devices were higher on *m*-plane sidewall channel. It should be noted that the impact of both drain lateral resistance and source resistance was negligible on the extraction of the channel mobility. Also, low hysteresis of the device is important in this analysis otherwise threshold shift needs to be considered.

These results suggest that, to achieve improved performance in GaN trench MOSFETs and OG-FETs, the devices should be oriented toward the crystallographic *m*-plane.

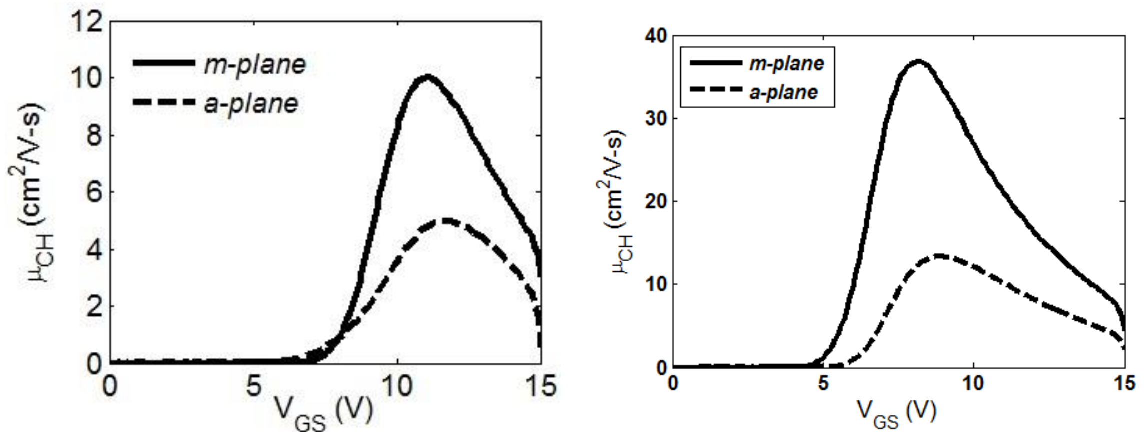


Figure 3.46: Field-effect channel mobility as a function of gate voltage for both *a*- and *m*-plane MOS channel for trench MOSFETs (Left) and OG-FETs (Right).

3.4 Summary

The OG-FET device design builds on the advantages offered by trench MOSFET. This chapter summarized the advantages and design considerations for OG-FET. To utilize potential advantages offered by OG-FET, multiple fabrication modules were identified and optimized. The fabrication process and techniques developed in this chapter were used to fabricate high voltage OG-FETs as described in the next chapter.

Chapter 4: High voltage OG-FETs

Vertical GaN devices are considered more suitable for high voltage applications which require breakdown voltage to be greater than (at least) 900 V. In this chapter, OG-FETs fabricated with re-growth and etch optimizations described in the previous chapter are discussed in detail.

4.1 GaN on sapphire OG-FETs

Regrowth, etch damage and sidewall plane optimizations were first explored with high voltage devices on GaN on sapphire.

4.1.1 Basic growth and fabrication

The epitaxial growth process was similar as described in chapter-3. On the semi insulating sapphire substrate, first, a heavily Si doped (3-5 x 10^{18} cm^{-3}) n^+-layer of 1 μm thickness followed by a lightly Si doped (5 x 10^{15} cm^{-3}) drift region of 6 μm thickness was grown. The drift region carrier concentration was calibrated on test samples with mercury capacitance-voltage (Hg C-V) measurements. Thereafter, 250 nm of p-GaN (Mg: 3 x 10^{19} cm^{-3}) was grown. After p-GaN regrowth, the sample went through a surface cleaning treatment (5 min 48% HF dip) to get rid of any magnesium on the surface. This was done to prevent surface riding of magnesium into the n^+-GaN layer. Finally, the p-n structure was capped with a heavily doped (5 x 10^{18} cm^{-3}) 200 nm n^+-GaN layer for source contact. The resultant epitaxial structure is shown in fig 4.1.

The device fabrication process also followed the basic fabrication process described in chapter-3. The device fabrication process started with the formation of vertical trench

structures. A low power 15 W Cl_2/BCl_3 gas combination etch (630 nm) was done in a RIE system to obtain vertical sidewalls as shown in fig 4.2.

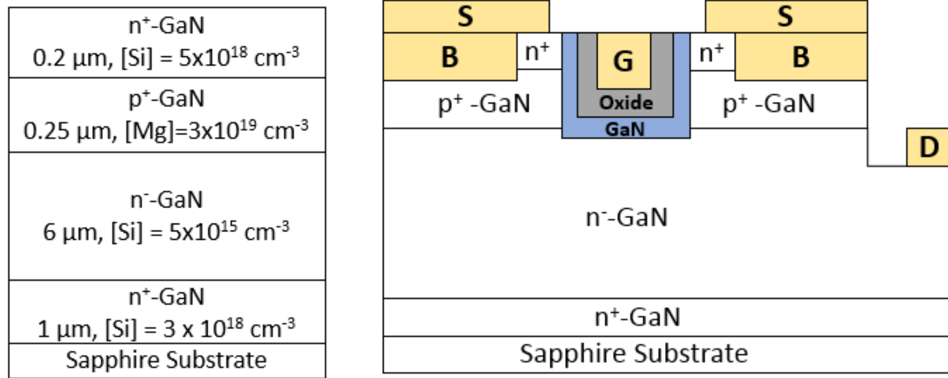


Figure 4.1: Epitaxial structure (Left) and cross-sectional schematic (Right).

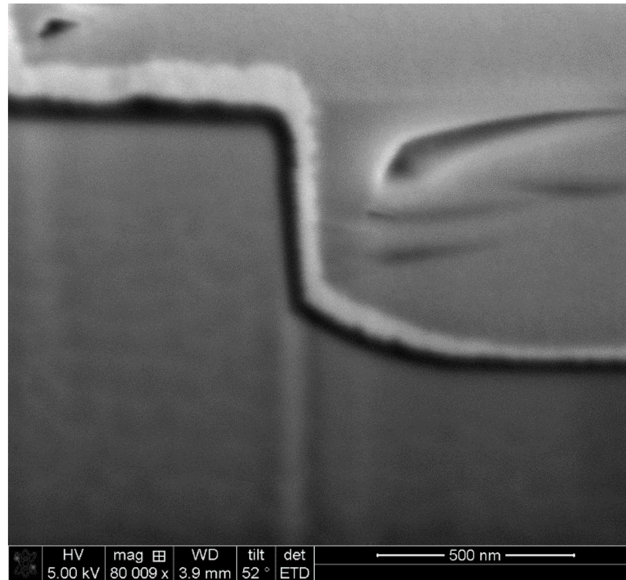


Figure 4.2: RIE vertical etch profile.

Figure 4.2 shows a focused ion beam-scanning electron microscopy (FIB-SEM) image of the trench. The RIE etch was vertical with a ‘shoe’ towards the bottom of the trench. This ‘shoe’ was characteristic of this low power RIE etch. Similar etch profiles have been observed with chemically assisted ion beam etch (CAIBE) of GaN. The sample underwent 3 cycles of UV ozone and HF treatment to remove residual Si at the regrowth interface. After cleaning,

the samples were immediately transferred to the MOCVD chamber. First, the sample was annealed in N_2/NH_3 at 930º C for 30 minutes to recover any etch damage. Then, a GaN interlayer of 5nm thickness on the sidewall (~10nm on c-plane) was grown followed by an in-situ 50 nm thick MOCVD Al_2O_3. Following the MOCVD regrowth process, source and body etches were performed as described in chapter-3. Prior to metallization, MOCVD recovery anneal and p-GaN activation anneal were performed as described in chapter-3. Ti/Au (30nm/200 nm) deposited by electron-beam deposition were used as electrodes for body, source, drain and gate. A large pad was deposited on the sample which acted as the drain contact as shown in the device schematic (Fig. 4.1). Finally, mesa isolation was performed to complete the device fabrication process.

4.1.2 Device details

The devices under test were circular in shape. The top view of these devices is in shown fig. 4.3. The devices with different L_{MOS} (2µm, 4µm, 8µm and 16µm) were measured and analyzed. The total area of the unit cell inclusive of gate and source pads was ~25,000 μm^2. The total area was large as it includes probe pads. This was an inefficient utilization of the chip area as the majority of chip area was inactive. In a commercial chip, the chip area is better utilized by joining multiple unit cells together such that the majority of chip area is active. Therefore, the on-resistance of the device in ohms was normalized by the active area to better represent the (specific) on-resistance of the device. Active area is generally considered to be the area which contributes to the current flow from drain to source electrode. The major active area contribution arises from the spreading area in the drift region. In this analysis, it was assumed that the current (electron) spreads at a 45° angle (isotropic drift region mobility) at the bottom of the trench into the drift region as shown in fig 4.4. Here, the active area was then

considered to be a circle with a diameter equal to the sum of trench diameter and drift region thickness. Even though the total spread is L_{MOS}+2W, the drift region thickness contribution was considered only once (L_{MOS}+W), because half of the area was still not utilized (due to a 45° angle spread). Therefore, a simple approximation was considering drift region thickness only once.

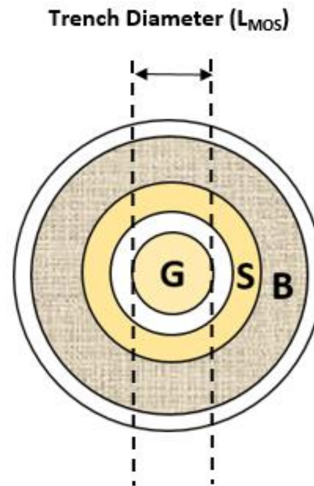


Figure 4.3: Top view of circular shape fabricated devices (Left).

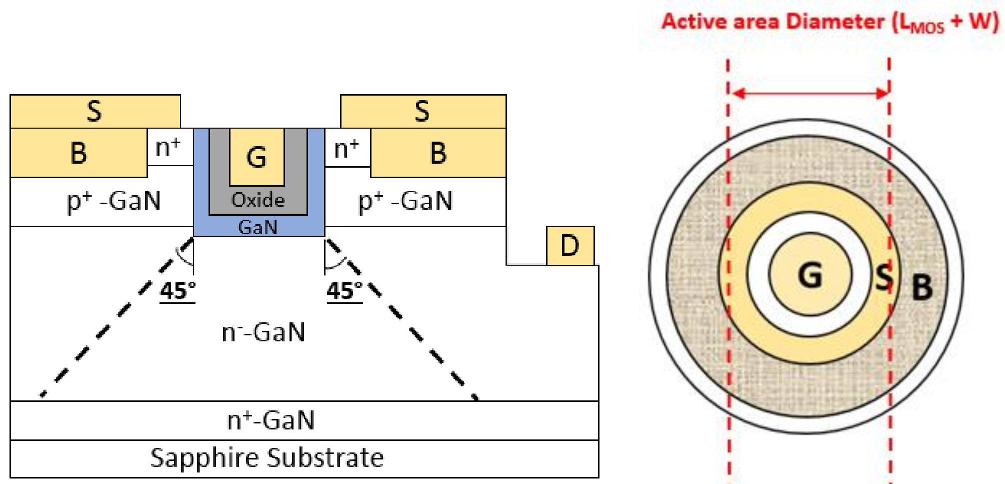


Figure 4.4: (Left) 45° spread of electrons into the drift region resulting in active area dependence on drift region thickness (W). Since, device area was large and inclusive of probe pads, active area was defined as shown in fig (Right).

4.1.3 Device results and analysis

The output I-V characteristics normalized by the gate-width (L_{MOS} =2 μm) are shown in fig 4.5. The device was normally-off as evident from the I-V plot. The on-resistance calculated at V_{GS} = 12 V, V_{DS} = 0.25 V was 5.8 mΩ.cm^2 considering active area definition as discussed above.

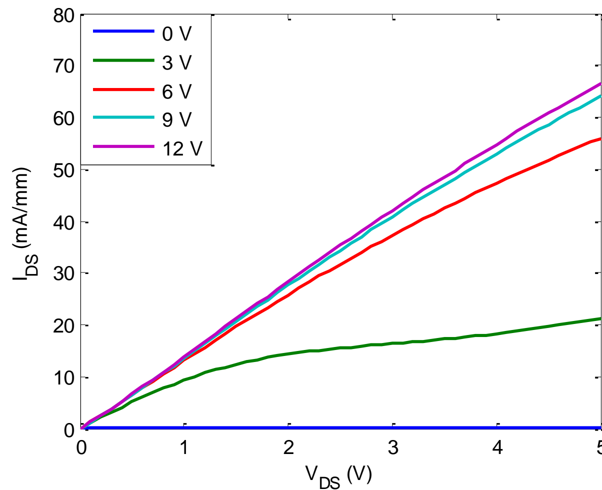


Figure 4.5: Output I_{DS}-V_{DS} plot normalized by the gate-width.

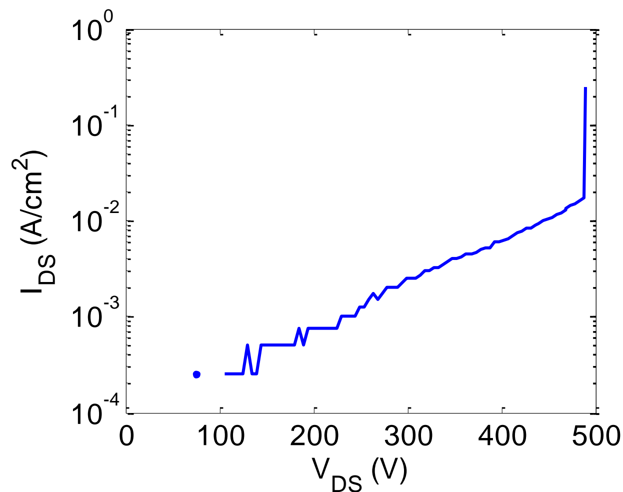


Figure 4.6: Off-state characteristics of the device measured at V_{GS} =-5 V. Hard breakdown was observed at 490 V.

The off-state I-V characteristics normalized by the total area and measured at V_{GS} = -5V is shown in fig. 4.6. Hard pinch-off was achieved with V_{GS}=-5V. Catastrophic gate-drain breakdown was observed at 490 V for L_{MOS}=2μm device. The p-n diode test structure on the same wafer broke down around ~600-700 V. Other devices with different L_{MOS} were also measured and average breakdown performance with L_{MOS} is shown in fig. 4.7.

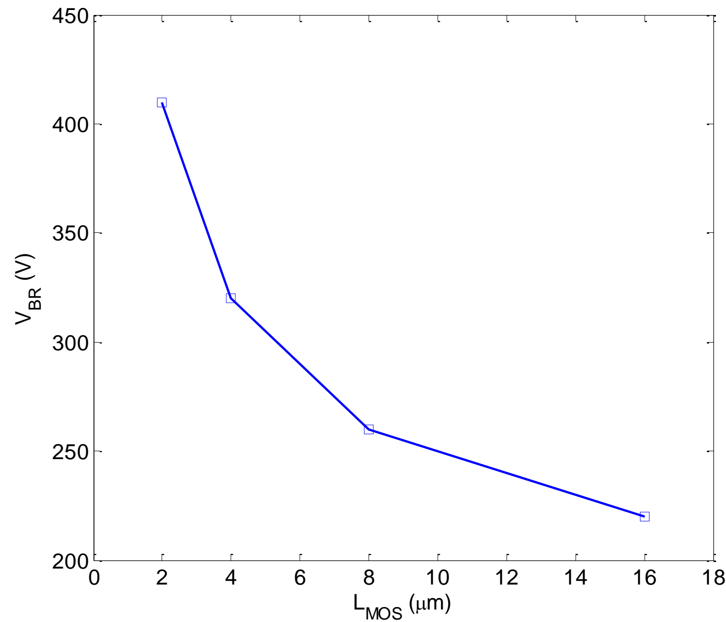


Figure 4.7: Average breakdown vs L_{MOS}

The average breakdown decreased with increasing L_{MOS}. This was difficult to comprehend as with increasing L_{MOS}, the electric field curvature would soften and result in almost equal or higher breakdown voltage [61]. Similar to our analysis of early breakdown of the gate-dielectric in MOSCAPs as discussed in chapter-2, this result could be explained by electron-hole pair generation due to dislocations. Holes generated in the depleted drift region are extracted out more efficiently by the p-GaN layer in devices with smaller L_{MOS} compared to larger L_{MOS}. This reasoning also explains the observed breakdown trend, $V_{BR,\ P\text{-}N} > V_{BR,\ 2\mu m} >$

$V_{BR,\ 16\mu m} > V_{BR,\ MOSCAP}$. This behavior reinforced that dislocations are affecting the breakdown of the device and needs to be reduced to obtain high breakdown.

The breakdown performance on this sample might be limited due to deep trench-gate etch than desired. The trench etch was ~ 200 nm deep beyond the p-GaN, this results in an increased field at the oxide corner resulting in early breakdown voltage. Even though improvements can be expected with optimized trench-gate etch and edge termination (if needed), due to dislocations, the overall performance would be affected. Henceforth, OG-FETs were fabricated on bulk GaN substrates.

4.2 Bulk GaN OG-FETs without edge termination

As described in chapter-2, vertical power devices require highest quality material to obtain high performance. The results from sapphire substrates obtained in the previous section further illustrated the importance of fabricating devices on higher quality bulk GaN substrates compared to sapphire. Therefore, first set of OG-FETs were fabricated on bulk GaN substrates. These devices were fabricated to observe/understand the impact of the underlying substrate on the device performance. Therefore, these OG-FETs were fabricated without edge termination.

4.2.1 Basic growth and fabrication

The epitaxial growth process was similar as described in chapter-3. The growths on bulk GaN samples were performed in MO5 (Nippon Sanso) reactor. It should be noted that all growths on sapphire substrate were performed in MO4 (Thomas Swann) reactor. On a half of 2-inch bulk GaN substrate (Hitachi), first, a heavily Si doped (3-5 x 10^{18} cm^{-3}) n^{+}-layer of 1 μm thickness followed by a lightly Si doped drift region (targeted: 1 x 10^{16} cm^{-3}) of 9 μm thickness was grown. The drift region carrier concentration was calibrated on a small bulk GaN sample (~1cm x 1 cm) with mercury capacitance-voltage (Hg C-V) measurements. The

epitaxial structure of the test sample is shown in fig 4.8. Thereafter, 300 nm of p-GaN (Mg: 3 x 10^{19} cm^{-3}) was grown. Following surface cleaning treatment as described in the previous section, a heavily doped (5 x 10^{18} cm^{-3}) 200 nm n^+-GaN was grown for the source. The resultant epitaxial structure is shown in fig. 4.9.

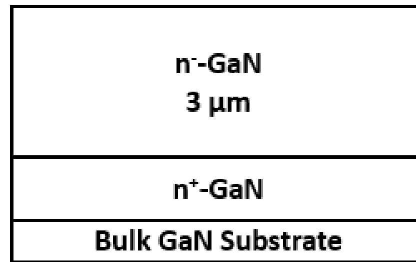


Figure 4.8: Test structure cross-sectional schematic. The drift region doping was extracted by mercury C-V measurements.

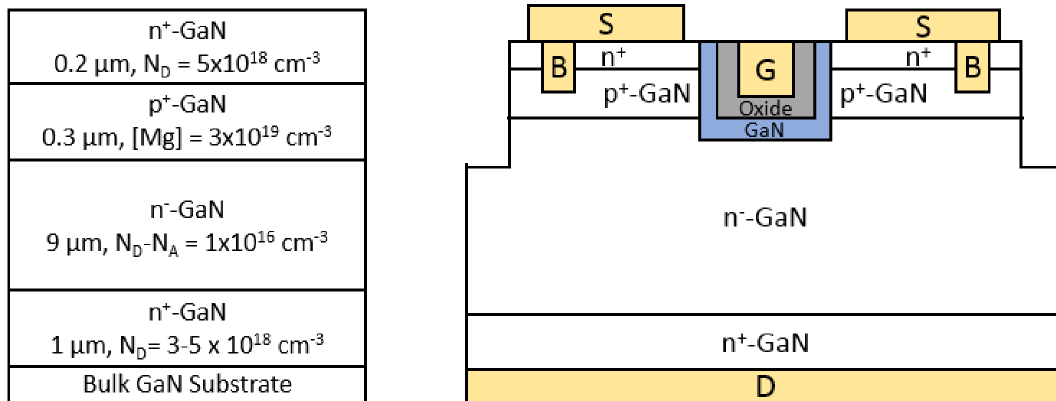


Figure 4.9: Epitaxial structure (Left) and cross-sectional schematic (Right). (Copyright © 2017, IEEE)

600 nm deep vertical trenches were made with a low power (15 W) BCl_3/Cl_2 dry etch in a RIE system. After UV-ozone and HF treatment as discussed earlier, the samples were then loaded into MOCVD chamber for regrowth process. After annealing for 30 min., UID GaN interlayer (10 nm c-plane, 5 nm sidewall) followed by Al_2O_3 (50 nm thick) was grown on the

sample. Thereafter, source and body etch were performed followed by MOCVD recovery and activation anneals as described in chapter-3. Ti/Au (300/2000 nm) was used as gate, body, source and drain (backside) electrode. Mesa isolation (vertical) was performed with RIE 15 W etch to complete the device process. The device schematic is shown in fig. 4.9.

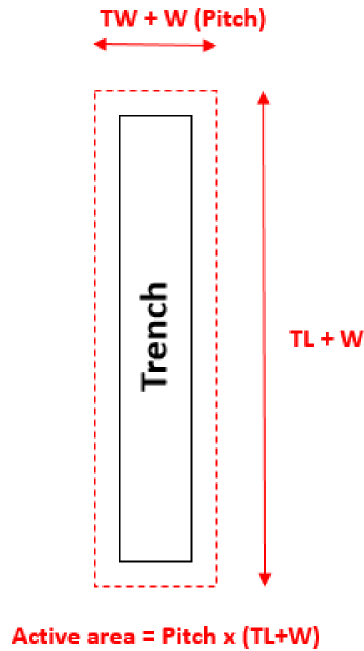


Figure 4.10: Active area definition for a rectangular device. Pitch was defined as the sum of trench width (TW) and drift region thickness (W). Active area was equal to pitch x (trench length (TL) + W).

4.2.2 Device details

The devices under test were rectangular with 3 µm trench-width and 80 µm trench length. Contrary to GaN on sapphire devices, rectangular geometry was preferred due to better utilization of active area. The total area of the unit cell inclusive of gate and source pads was ~25000 µm^2. The total area was large as it again included probe pads. Therefore, the on-resistance of the device in ohms was again normalized by the active area to better represent the (specific) on-resistance of the device. In this analysis as well, it was assumed that the electron

current spreads at 45° angle at the bottom of the trench into the drift region as shown in the previous section (Fig. 4.4). However, since half of the area was being utilized for current spreading, the device pitch was defined as trench width + drift region thickness. The active area of the device was then pitch x (trench-length + drift region thickness) (Fig. 4.10).

4.2.3 Device results and analysis

Capacitance-voltage (C-V) measurements were performed on the gate-drain MOSCAP test structure and p-n diode test structure as shown in fig**.** 4.11 to estimate the drift region doping. Huge variation in drift region doping was observed. A decrease in drift region doping was observed radially. This effect could be attributed to the inconsistent carbon incorporation in GaN drift regions due to radial temperature gradient. Varied carbon incorporation could explain variation in drift region doping as resultant doping was N_D-N_A.

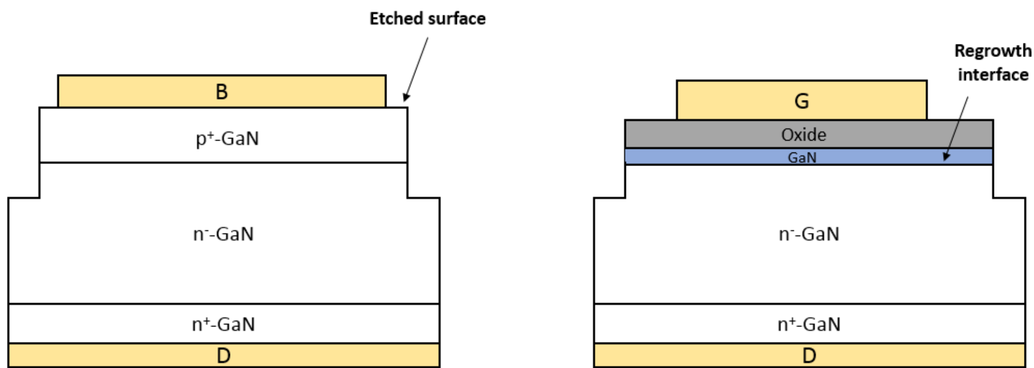


Figure 4.11: P-n diode (Left) and MOSCAP (Right) test structures to extract drift region doping.

Three dies with different doping were measured and analyzed. The measured carrier concentration for three dies were 1.4 x 10^{16} cm^{-3} (Die 1), 1 x 10^{16} cm^{-3} (Die 2) and 7 x 10^{15} cm^{-3} (Die 3).

Figure 4.12 shows the transfer I_{DS}-V_{GS} characteristics normalized by the gate width for all three dies at V_{DS} = 1 V. Low gate leakage (< 100pA/mm) and excellent on-off ratio of 10^9 was

obtained for all three dies. Normally-off operation with threshold voltage (calculated at I_{ON}/I_{OFF} = 1µA/mm) of 2.6 V, 3.2 V and 3 V was observed for the dies with a drift region doping of 1.4 x 10^{16} cm^{-3}, 1 x 10^{16} cm^{-3} and 7 x 10^{15} cm^{-3} respectively [46].

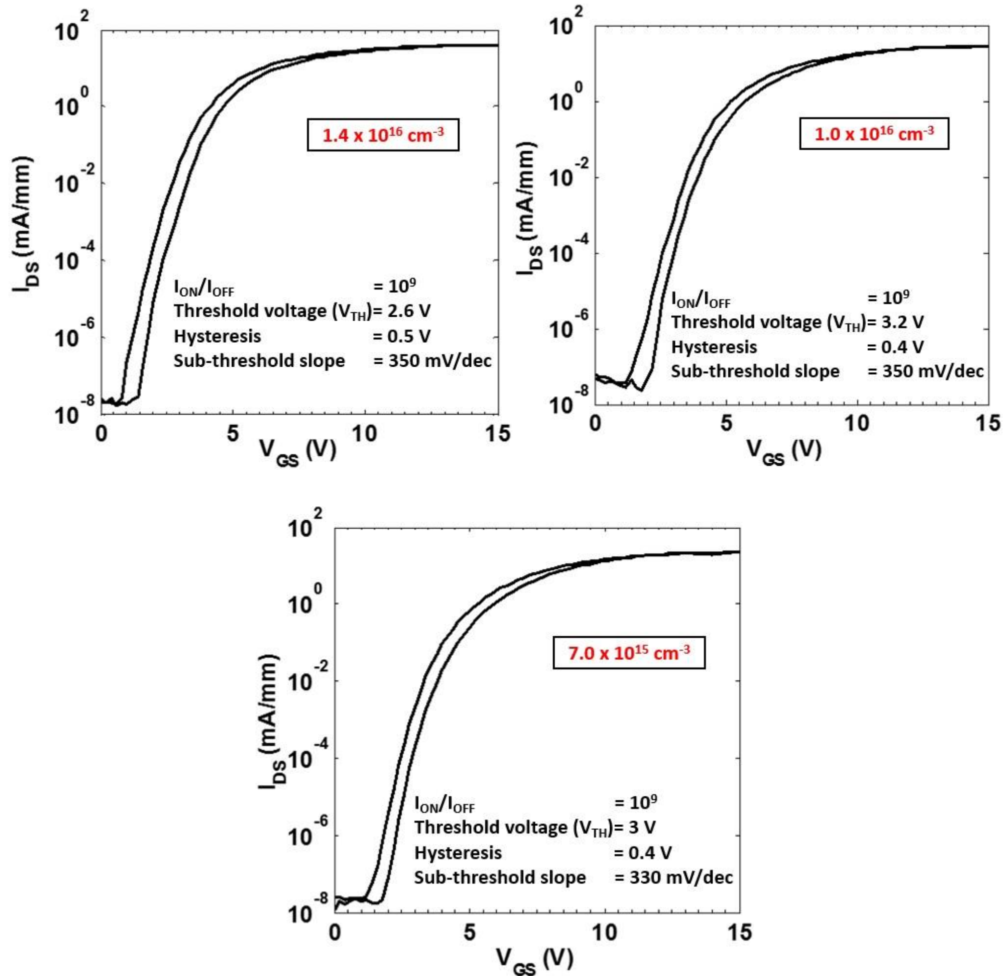
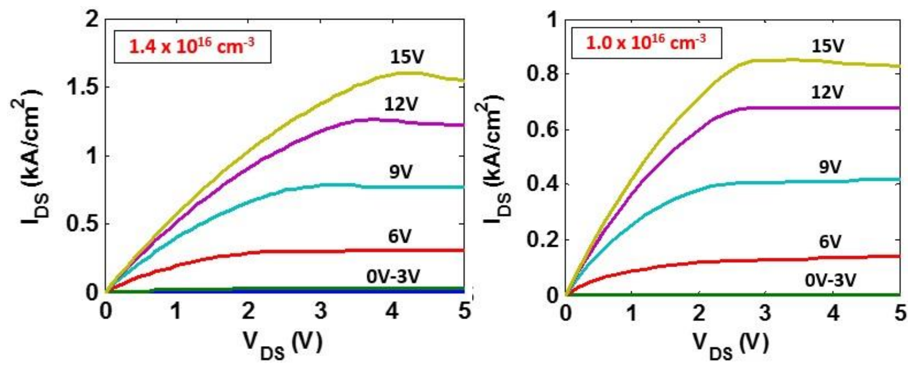


Figure 4.12: Transfer I-V characteristics normalized by the gate-width for all three dies at V_{DS} = 1V.

The threshold voltages for all three dies were considerably lower than the expected threshold voltage value of 18.4 V which was obtained from one dimensional self-consistent Schrödinger-Poisson solver or using MOSFET basics [46]. Lowered experimental threshold values compared with estimated values have been observed by other researchers as well and

were attributed to sidewall etch damage, which can cause nitrogen vacancies to form and act as donors [10]. The density of fixed charge obtained from the threshold voltage difference between experimental and estimated values was almost similar in all three dies and was approximately, 8 x 10^{12} cm^{-2}. A clockwise hysteresis of $\Delta V_{TH} \sim 0.5$ V was observed in all three dies. Sub-threshold slope varied between 300 mV/dec-350 mV/dec for all three dies.

The output DC characteristics of the drain current (I_{DS}-V_{DS}) normalized by the active area (as described above) for all three dies is shown in the figure 4.13. As expected, the drain current density increased with higher drift region doping or increased charge in the drift region. A similar trend was also observed in the on-resistance of these devices. The on-resistance was calculated here by considering the active area (as described above) and evaluated at V_{GS}=15 V and V_{DS}=0.25 V. The on-resistance values thus obtained for the dies with 1.4 x 10^{16} cm^{-3}, 1 x 10^{16} cm^{-3} and 7 x 10^{15} cm^{-3} doped drift region were 1.6 mΩ.cm^2, 2.1 mΩ.cm^2 and 2.6 mΩ.cm^2 respectively. A further reduction in the on-resistance could be obtained by optimizing active area utilization, which could be achieved by utilizing a hexagonal grid structure [14].



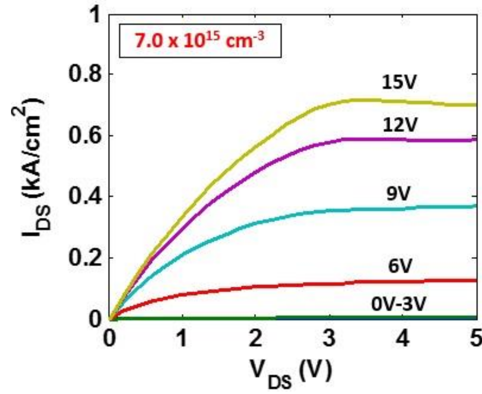


Figure 4.13: Output I-V characteristics for all three dies normalized by the active area at different gate voltages.

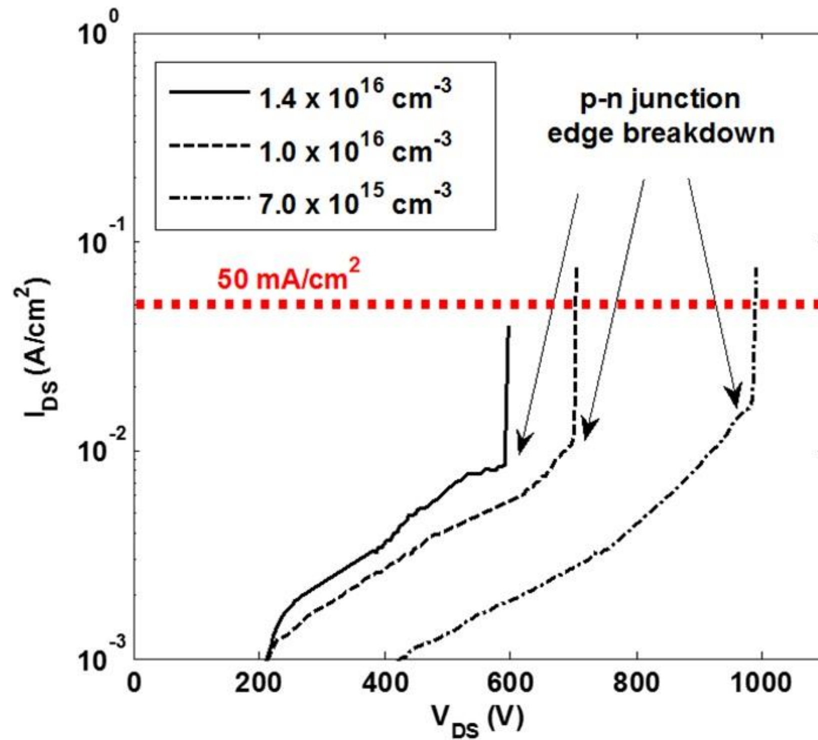


Figure 4.14: Off I-V characteristics for all three dies normalized by the total area at zero gate bias.

The off-state characteristics of all three dies measured at zero gate bias is shown in fig. 4.14. Hard pinch-off was achieved at zero gate bias. The leakage current was normalized by the total device area. This was done because the whole device area was “active” in the off-

state. The breakdown voltage was defined as the voltage, at which $I_{DS} > 50$ mA/cm^2. This breakdown definition was borrowed from ARPA-E SWITCHES program standards. As expected, the breakdown voltage increased with decreasing drift region doping. A high breakdown voltage of 990 V (E_{BR} ~ 1.75 MV/cm) was observed for the 7 x 10^{15} cm^{-3} die. The breakdown occurred at the edge of the p-n junction isolation mesa in the majority of devices in all three dies, possibly due to the potential crowding at the edge of the p-n junction. The breakdown at the p-n junction was identified either by optical microscopy and/or measuring gate leakage in the absence of gate breakdown and/or scanning electron microscopy (SEM) after breakdown. All three dies demonstrated high breakdown fields between 1.5 MV/cm-1.8 MV/cm. Similar breakdown fields were obtained with GaN trench MOSFETs and in GaN p-n diodes without edge termination [10], [59], [62]. The breakdown field was calculated by using the following equation,

$$BV = \frac{\varepsilon E_{BR}^2}{2q(N_D - N_A)} \qquad 4.1$$

where, BV is the breakdown voltage and E_{BR} is the breakdown field. It should be noted that the estimated breakdown field does not truly represent the breakdown field at the physical breakdown point. It represents the maximum field of GaN which could be achieved by this device design, which by definition is less than the critical field of GaN. For example, if we perform calculations for Die 2, and assume that the achievable critical field of GaN is 3 MV/cm, therefore, with a perfect design, the expected breakdown voltage will be approximately 1890 V by simple one-dimensional p-n junction calculations. Therefore, the above represented number can be used as a metric to determine how efficient the device design is in realizing the full potential offered by GaN.

Compared to GaN on sapphire breakdown results, these results demonstrate that bulk GaN substrates were instrumental in enhancing the breakdown voltage (and breakdown field) compared to GaN on sapphire devices (last section) which gave breakdown field of ~1-1.2 MV/cm. In bulk GaN, the device breakdown was limited by the p-n edge breakdown and the intrinsic or internal MOS device was protected (Fig. 4.15). This implies that by using proper edge termination, breakdown voltage can be further enhanced [10]. However, the nature of breakdown in GaN on sapphire was intrinsic and gate-drain or MOS was breaking down. Therefore, any edge termination would not help in increasing the breakdown voltage and it was difficult to improve breakdown voltage without any trade-offs in the on-state performance.

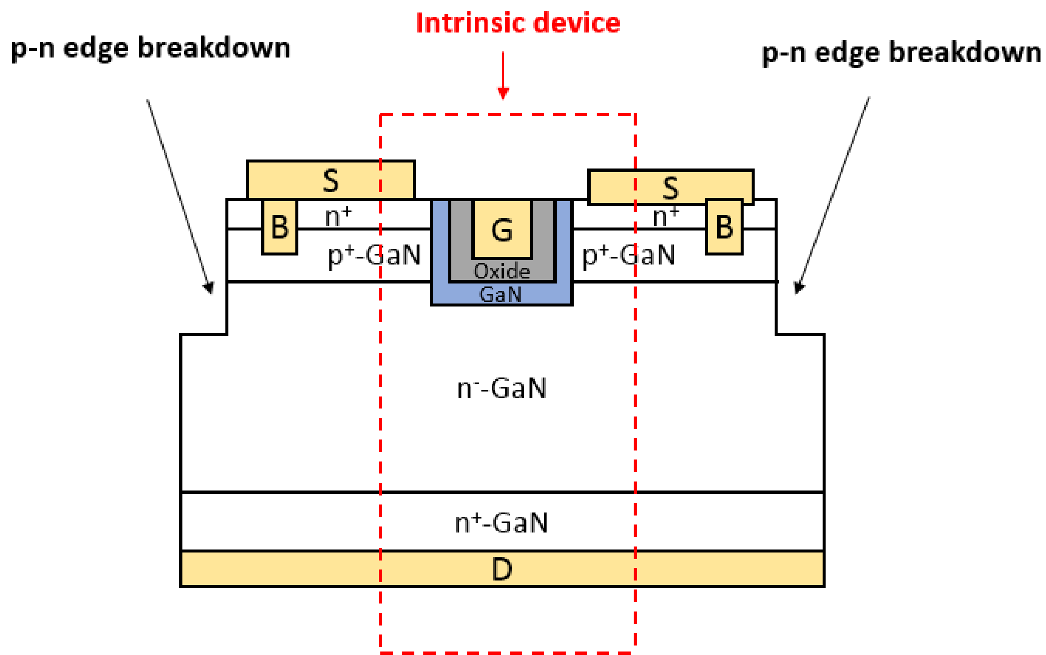


Figure 4.15: Cross-sectional schematic showing edge breakdown and un-affected intrinsic device.

Another key difference between bulk GaN and sapphire was the breakdown voltage dependence on the trench area. Contrary to GaN on sapphire devices, bulk GaN devices

showed no dependence on trench area (up to ~400 μm^2) [61]. This implies high current devices can be obtained with bulk GaN for same breakdown voltage.

These results demonstrated high performance OG-FETs on bulk GaN substrates for the first time. By utilizing bulk GaN substrates, a high breakdown field of 1.6-1.7 MV/cm (without edge termination) was achieved in OG-FETs. This breakdown performance was achieved alongside a low on-resistance (R_{ON} = 1.5-2.5 mΩ.cm^2) while maintaining excellent enhancement mode operation (V_{TH} ~ 3 V). Independent of the drift region doping, a high figure of merit (FOM) value (> 150 MW/cm^2) was observed for all three dies.

4.3 Field-plated bulk GaN OG-FETs

The results from the previous section illustrate that the p-n edge breakdown limited the breakdown voltage of the devices. The intrinsic device can potentially hold more voltage. Therefore, with edge termination, improved breakdown performance of the device can be expected. A spin-on-glass (SOG) based field-plate process was adopted for edge termination as described in chapter-3 for p-n diodes.

4.3.1 Basic growth and fabrication

The epitaxial growth process was similar as described in chapter-3 and previous section. Here, the drift region thickness and doping were targeted to be 10 µm and 1 x 10^{16} cm^{-3} respectively. The resultant epitaxial structure is shown in fig. 4.16 [17].

The device fabrication process was same as described in the previous section until vertical mesa isolation. After ~1 um deep mesa isolation, the photo-resist was stripped off and underwent standard solvent clean. Following the solvent clean, the sample was dipped in HCl:DI (1:1) solution prior to SOG application to reduce impurities at the interface. Hydrofluoric (HF) or TMAH was not used as they could potentially etch Al_2O_3 present as the

gate-dielectric. Thereafter, SOG was spun followed by a series of bakes as described in appendix A. Finally, SOG was cured in N_2 at 425° C for an hour with slow temperature ramp from 250° C (~2.5° C/min). The thickness of SOG was ~600 nm. Following SOG deposition, SOG was selectively etched to form via. The field-plate process was completed with the deposition of Ti/Au (30 nm/200 nm) as the field-plate metal. The cross-sectional schematic is shown in fig. 4.16.

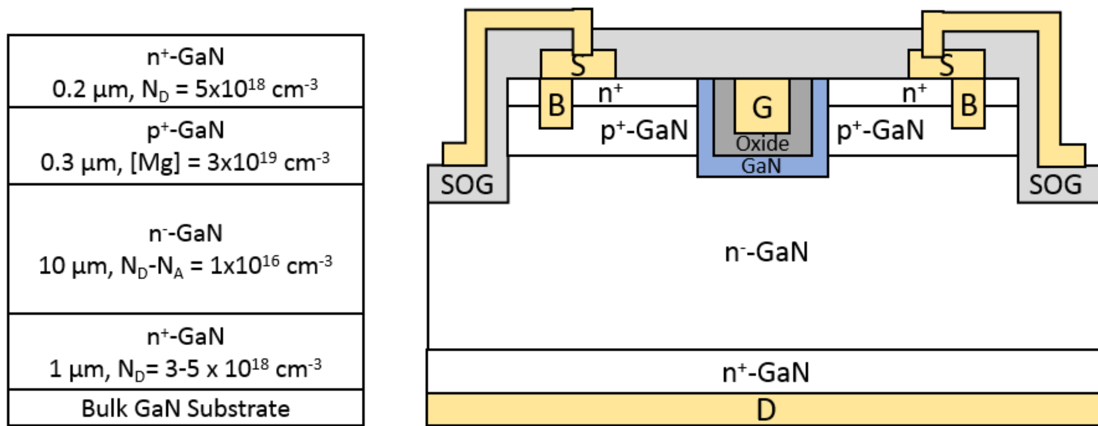


Figure 4.16: Epitaxial structure (Left) and cross-sectional schematic (Right). (Copyright © 2017, IEEE)

4.3.2 Device results and discussion

The active area was defined like the previous section. Radial variation in the drift region doping was observed on this sample as well. The devices were measured on die with 1 x 10^{16} cm^{-3} drift region doping.

The transfer I-V characteristics normalized by the gate width at V_{DS}=1 V is shown in fig. 4.17. The device exhibited normally-off operation with threshold voltage (calculated at I_{DS} = 1 µA/mm) of 3.2 V, an up-down sweep hysteresis of ΔV_{TH} = 0.4 V and sub-threshold slope of

340 mV. The density of fixed charge obtained from the threshold voltage difference between experimental and estimated values was 9 x 10^{12} cm^{-2}.

The output I-V characteristics of the sample normalized by the active area is shown in fig. 4.18. Here, the on-resistance was calculated at V_{GS} = 15 V and V_{DS} = 0.25 V. The on-resistance value, thus obtained was 3.6 mΩ.cm^2. The increase in on-resistance value compared to the last experiment could be attributed to growth and/or process variation. Potential causes could be lower source region doping or lower channel mobility due to relatively poor interface or lower drift region mobility or some combination of these factors [17].

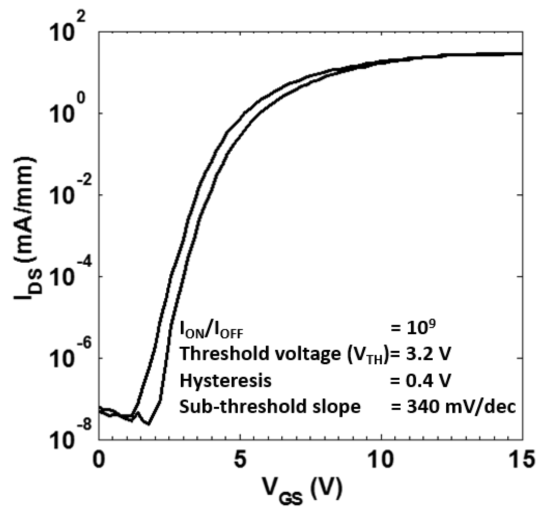


Figure 4.17: Transfer I-V characteristics normalized by gate-width measured at V_{DS} = 1V. (Copyright © 2017, IEEE)

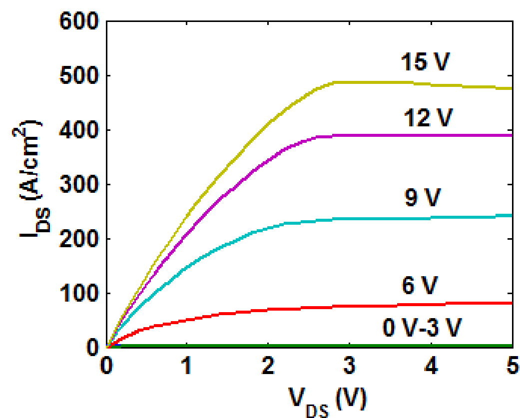


Figure 4.18: Output I-V characteristics of field plated OG-FET normalized by the active area. (Copyright © 2017, IEEE)

The off-state characteristics are shown in fig 4.19 normalized by the total area (~25000 μm^2) and measured at zero gate bias. Employing field-plate-based edge termination technique increased the breakdown voltage from ~600 to ~1000 V. The breakdown occurred at the p-n isolation mesa edge in both devices with a field plate and without field plate structures. The latter was catastrophic. This implies that an improvement in edge termination structure would further enhance the breakdown voltage of the OG-FET. Also, the intrinsic device can potentially hold higher voltage than 1000 V. The breakdown field estimated using equation 4.1 improved from ~1.6 MV/cm to ~2 MV/cm with field-plate based edge termination [17].

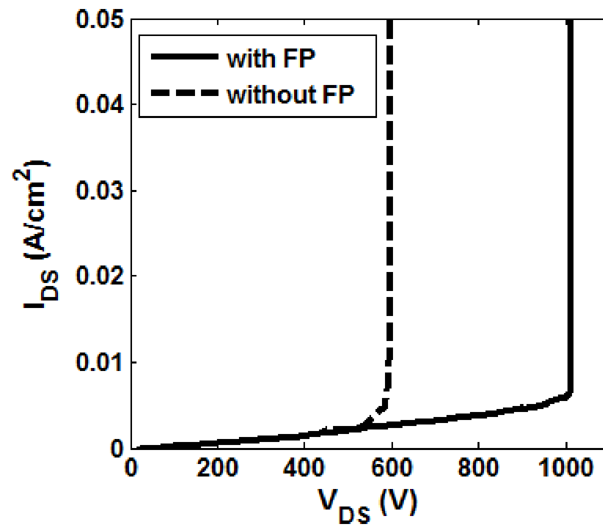


Figure 4.19: Off-state I-V characteristics of field plated OG-FET normalized by the total area at V_{GS} = 0V. (Copyright © 2017, IEEE)

Here, in this device fabrication process, the isolation mesa etch was vertical. It has been shown in previous chapter that an angled isolation etch allows better management of peak

electric field compared to a vertical one. Therefore, improvement in breakdown performance can be expected with angled isolation etch.

4.3.3 OG-FETs with angled isolation etch

As discussed above, OG-FETs were fabricated with angled etch on another piece of the same epi. Similar on-state performance was observed for the sample. As expected, the breakdown performance improved with angled etch. For same drift region doped die (1 x 10^{16} cm^{-3}), a high breakdown between 1100 V-1200 V was observed. On this device, the device broke down at the gate-drain junction rather than the p-n edge. Therefore, the intrinsic device needs to be improved to obtain a higher breakdown voltage.

4.4 Bulk GaN OG-FETs with Aluminum Silicon Oxide (AlSiO)

The gate-dielectric is an integral and important part of the module of a power MOSFET. Improvement in gate-dielectric quality can improve both on-state and off-state performance simultaneously. Oxide/semi-conductor interface quality affects channel properties such as channel mobility, hysteresis, and reliability as well. High breakdown field strength reduces gate-leakage and increases off-state breakdown voltage. Amongst dielectric metrics, high permittivity, high breakdown field strength and large conduction band offset are important requirements for a gate dielectric for wide band gap power devices. Both Al_2O_3 and SiO_2 are suitable candidates for gate-dielectrics to be used in wide band gap semiconductors. However, while Al_2O_3 has relatively lower band offsets and field strength compared to SiO_2, SiO_2 has lower permittivity than Al_2O_3. Addition of Si into Al_2O_3 allows the ability to tune these properties to meet application specific demands. Few groups have explored aluminum silicon

oxide (AlSiO) deposited by MOCVD and ALD [63], [64], [65]. With MOCVD, *in-situ* growth of III-N is an added advantage.

To improve device performance of OG-FETs, where *in-situ* deposition of gate dielectric plays an important role in improving channel mobility at the dielectric-semiconductor interface, MOCVD based AlSiO was explored as the gate dielectric.

To understand the impact of dielectric on device performance, detailed *in-situ* MOSCAP studies were performed with AlSiO by Chan *et al* [18]. The results obtained demonstrate the superiority of AlSiO over Al_2O_3 as the gate-dielectric in breakdown field, time-dependent dielectric breakdown, interface trap density, stress testing etc. Therefore, OG-FETs were fabricated with AlSiO as the gate-dielectric.

4.4.1 Basic growth and fabrication

The epitaxial growth process was similar to described in chapter-3 and the previous section. Here, the drift region thickness and doping were targeted to be 12 μm and 1 x 10^{16} cm^{-3} respectively. Also, the p-GaN layer was 400nm thick instead of usual 300 nm thickness. The p-GaN thickness was increased to allow more process tolerance with low power RIE source region etch to expose p-GaN. Damage caused by the body etch can result in increased source-drain leakage and early breakdown of the device. Therefore, thicker p-GaN was grown to increase fabrication process tolerance. The resultant epitaxial structure is shown in fig. 4.20.

The device fabrication process started with the formation of ~720 nm deep vertical trench structures with RIE 15 W BCl_3/Cl_2 low damage vertical etch. Prior to MOCVD regrowth, the samples underwent UV Ozone and HF cleaning process as described earlier. After annealing and GaN regrowth, 60 nm thick AlSiO was grown on the sample as the gate-dielectric. The precursors used for AlSiO growth were trimethylaluminum (TMA, 4.5 μmol/min), oxygen (O_2,

100sccm), and disilane (Si_2H_6, 1.9 µmol/min). The AlSiO composition (in Si/(Al+Si)) was approximately 24% Si (±4 %) [18]. AlSiO was etched in BHF to expose the source regions. The AlSiO underwent a short RIE etch to remove UID-GaN layer to expose the n^+-GaN region. Next, n^+-GaN was etched to expose the buried p-GaN layer followed by recovery anneal and activation. Here, first, nickel (Ni, 150 nm) was deposited as the body contact to the p-GaN followed by Ti/Au (30 nm/200 nm) deposition as source, gate and backside drain contact. Here, as discussed in previous section, angled isolation etch was performed using photoresist thermal reflow technique. After angled mesa isolation, the devices were edge terminated with SOG based field-plate process as described in the previous section. The cross-sectional schematic is shown in fig. 4.20 [18].

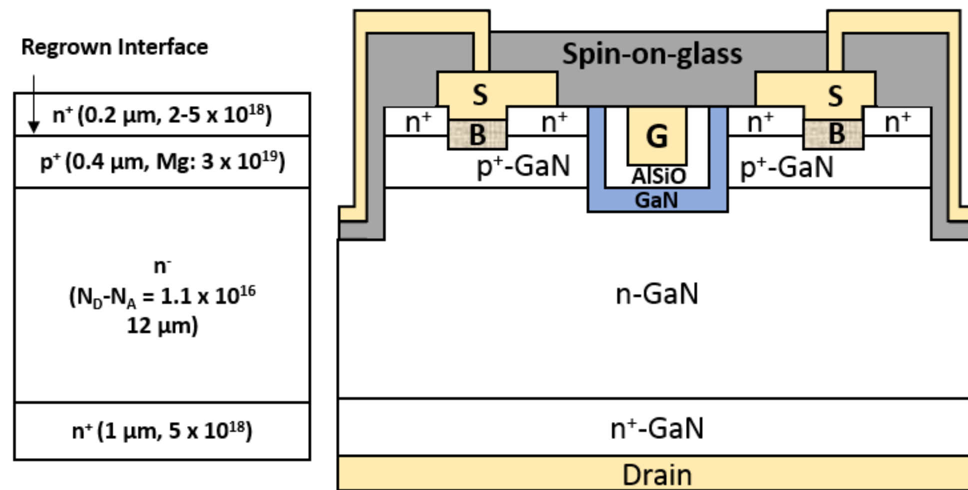


Figure 4.20: Epitaxial structure (Left) and cross-sectional schematic (Right). (Copyright © 2017, IEEE)

4.4.2 Device results and analysis: OG-FETs with AlSiO

The active area was defined like the previous section. Variation in the drift region doping was observed on this sample as well. The rectangular shaped devices (2µm x 100µm) were measured on die with 1.1 x 10^{16} cm^{-3} drift region doping.

The output DC characteristics of the drain current normalized by the active area (as defined in previous sections) is shown in figure 4.21 [18]. Here, the on-resistance values were calculated at V_{GS} = 12 V and V_{DS}=0.25 V. The on-resistance value thus obtained was 2 mΩ.cm^2. Figure 4.22 shows the transfer I_{DS}-V_{GS} characteristics normalized by the gate-width of the device at V_{DS} = 1V [18]. Normally-off operation was obtained for these devices with a threshold voltage of 1.5 V (defined at I_{DS} = 1 µA/mm). The lowering of threshold voltage with AlSiO compared to Al_2O_3 was difficult to explain. Multiple processing runs are needed to confirm this behavior. The device had a clockwise hysteresis (between up and down gate bias sweeps) of ΔV_{TH} < 0.1 V and a sub-threshold slope (SS) of 230 mV/dec. The hysteresis and SS values were the lowest amongst OG-FET results obtained so far. This also implies the improvement in interface properties with AlSiO compared with Al_2O_3.

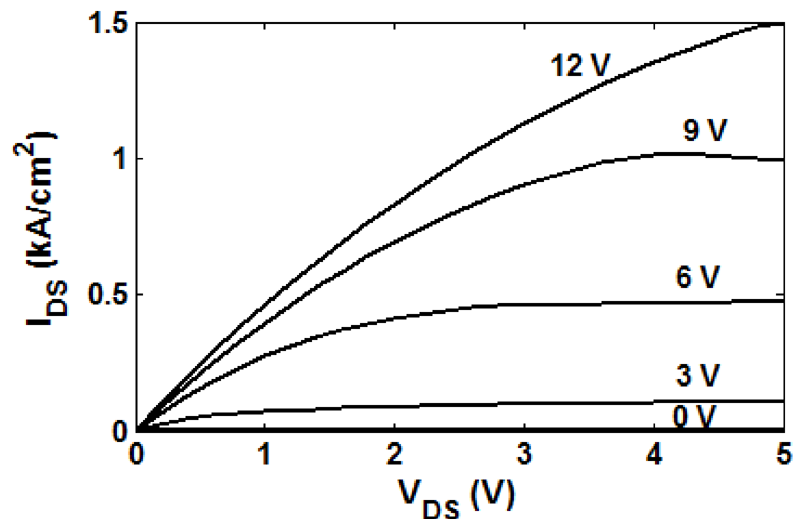


Figure 4.21: Output I-V characteristics normalized by the active area. (Copyright © 2017, IEEE)

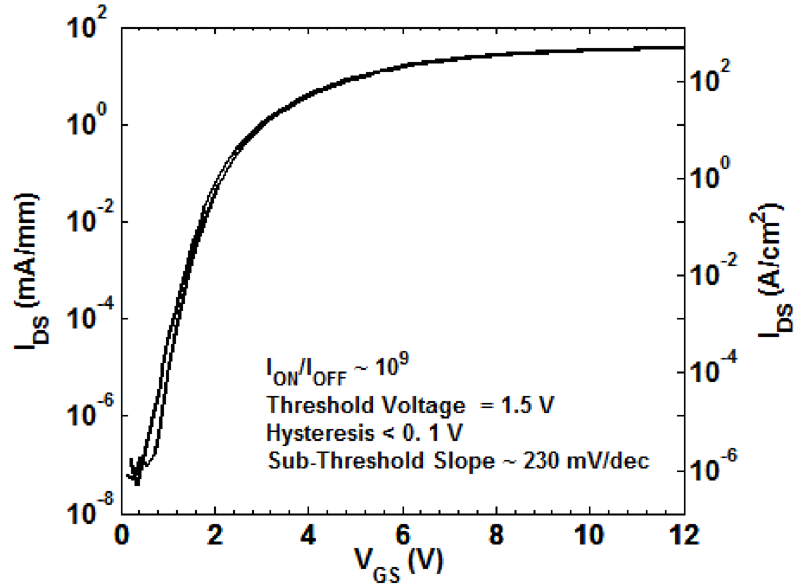


Figure 4.22: Transfer I-V characteristics normalized by both gate-wdith and active area at V_{DS} =1V. (Copyright © 2017, IEEE)

Figure 4.23 shows the off-state characteristics of OG-FET normalized by the total device area (~25000 μm^2) was measured at V_{GS} = -1 V [18]. The leakage current was normalized by the total device area. The device demonstrated a high breakdown voltage of 1200 V. The breakdown occurred at the trench corner (gate-drain junction) and was catastrophic in nature (confirmed by visual inspection/scanning electron microscopy). Using equation 4.1, the estimated breakdown field of GaN was ~2.3 MV/cm. This was an improvement over the results obtained in previous sections. Majority of devices demonstrated breakdown voltage between 1050-1300 V on the die.

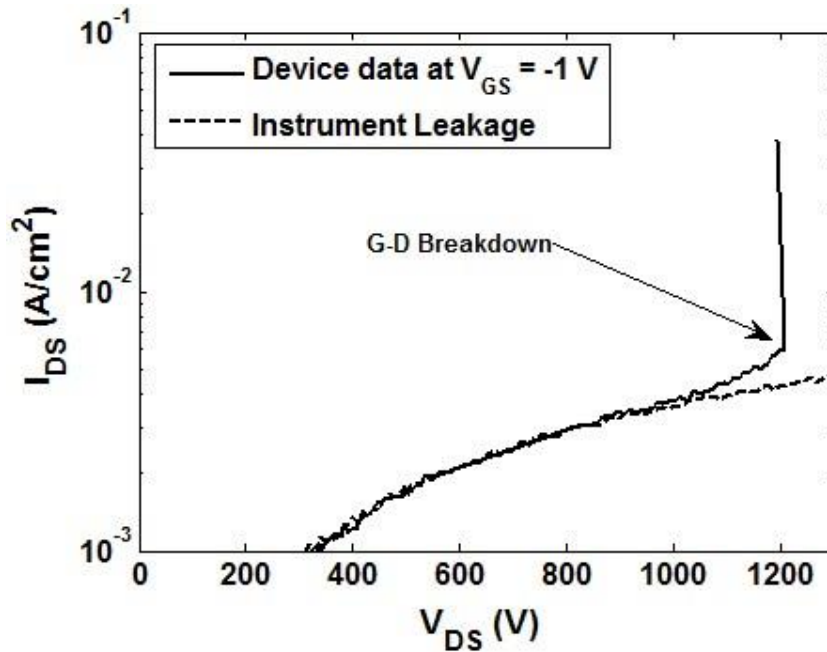


Figure 4:23: Off-state characteristics normalized by the total area at V_{GS}=-1V. (Copyright © 2017, IEEE)

The gate-drain breakdown indicates that the edge termination was successful in alleviating the peak electric-field near the p-n junction edge. The p-n test structure broke down catastrophically around 1600 V. The leakage current prior to breakdown voltage was at the instrument leakage. The breakdown field for the p-n diode was ~2.6-2.7 MV/cm. The breakdown field obtained is very high and avalanche breakdown has been observed by other researchers around these values [13]. With further improvement in edge-termination, avalanche breakdown can be expected in GaN p-n diodes. Shallower etch may be utilized to better manage the peak electric field [13].

It should be noted that the breakdown measurements were performed at V_{GS} = -1 V. Ideally, normally-off devices should allow breakdown voltage to be measured at zero gate bias. Here, the device demonstrated source-drain leakage current prior to breakdown at high drain bias

(~900 V-1100 V) in the off-state, with zero gate bias. Therefore, to obtain hard pinch-off, gate was biased more negative.

These were the best performing unit cell OG-FETs with low on-resistance, normally-off behavior, high breakdown voltage (and field) and good channel properties. Figure 4.24 shows the performance of OG-FET benchmarked with other vertical GaN FETs.

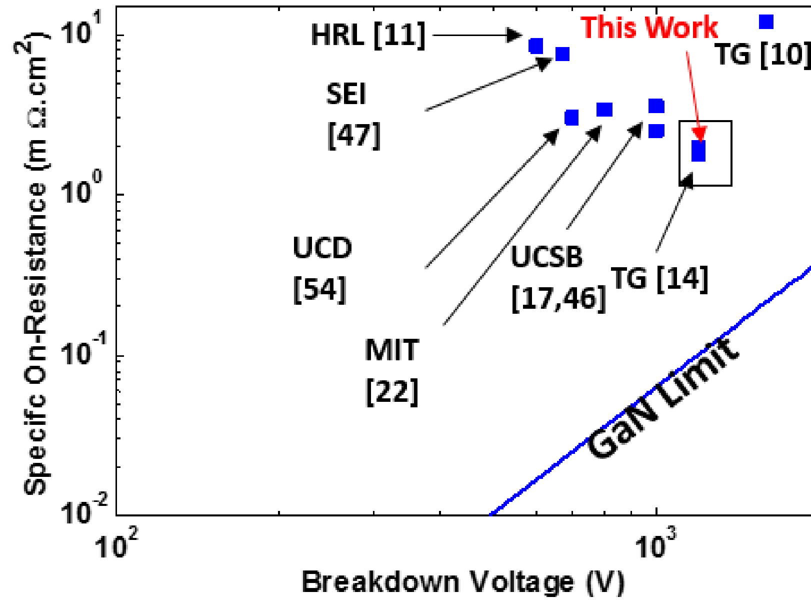


Figure 4.23: Bench-marking of OG-FET performance with vertical GaN FETs.

4.5 On-state analysis

Low on-resistance is one the basic requirements of power devices. The on-resistance of the device contribute to the conduction losses and reduces the over-all efficiency of the system. Therefore, the focus was on minimizing the on-state resistance. The on-resistance of OG-FET consists of components as show in the following equation (Fig. 4.24),

$$R = R_S + R_{CH} + R_{SUB} + R_{DRIFT} \quad 4.2$$

Where, R is the total on-resistance of the device, R_S is the source resistance, R_{CH} is the channel resistance, R_{SUB} is the resistance of the device from drift region end to the drain contact and R_{DRIFT} refers to the drift region resistance.

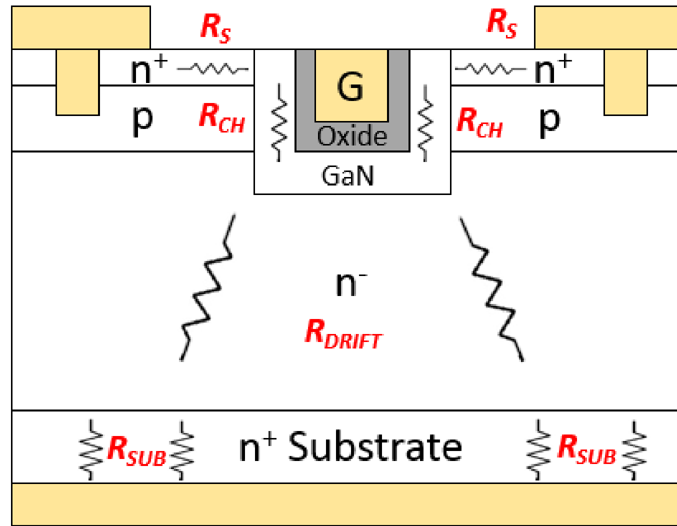


Figure 4.24: On-resistance components of an OG-FET.

4.5.1 Source resistance

Source resistance (R_S) consists of two components as described in the following equation,

$$R_S = R_{S,C} + R_{S,SHEET} \tag{4.3}$$

Where $R_{S,C}$ is the source contact resistance and $R_{S,SHEET}$ is the source sheet resistance. The source contact resistance depends on the doping of and the contact metal to the top source layer. In this dissertation work, Ti was used as the source contact metal. Al could be used as the source contact in future due to lower barrier to n^+-GaN. Here, in this work, the n^+-GaN doping was targeted to be 5 x 10^{18} cm^{-3}. TLM measurements were performed to extract contact resistance (R_C) and sheet resistance (R_{SH}). The TLM test structure is shown in fig 4.25. The typical R_C and R_{SH} were ~0.03-0.1 mΩ.cm^2 and ~400-600 Ω/sq. These numbers are reasonable and similar numbers were obtained for Ti contact with 3-5 x 10^{18} cm^{-3} doped source layer [30].

The source electrode to trench distance would affect the $R_{S, SHEET}$. In this work, the distance was 5µm. This should be reduced to minimize the source resistance. $R_{S,C}$ could be minimized by increasing the doping of the source region or increasing the source metal contact area. The source-metal/n^+-GaN overlap in this dissertation work was 1µm. This resulted in significant resistance contribution due to contact resistance. The total source resistance contribution (in ohms) to on-resistance (in ohms) in these devices varied between ~15-30 %.

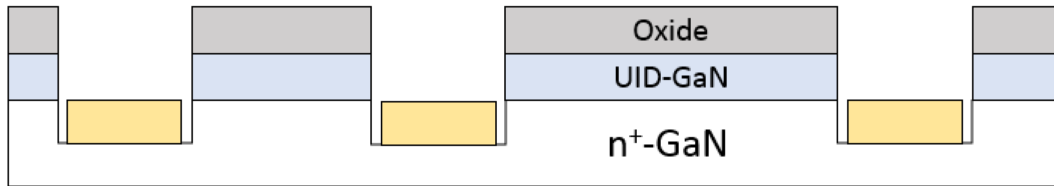


Figure 4.25: TLM test structure to extract source contact structure and sheet resistance. This structure was design to mimic the OG-FET source resistance. The gate-dielectric and UID-GaN were etched followed by an over–etch penetrating into n^+-GaN.

4.5.2 Channel resistance

The channel resistance can be obtained by using the following equation,

$$R_{CH} = \frac{L}{qn_s\mu_{CH}W} \quad 4.4$$

$$n_s = C_{OX}(V_{GS} - V_{TH}) \quad 4.5$$

Where, C_{OX} is the oxide capacitance, V_{GS} and V_{TH} are the gate and threshold voltage, L is the effective gate length (or the length of the tapered p-region), W is the trench perimeter or gate width. From the equation 4.4 above, it could be seen that to achieve lower channel resistance higher channel mobility is desired. The OG-FETs device design results in the improvement of channel mobility compared to conventional trench MOSFETs. Apart from

channel mobility, high k-dielectrics will also reduce the channel resistance by increasing the oxide capacitance.

Effective gate-length can be reduced to obtain lower channel resistance. However, the thickness and the doping concentration of the p-GaN layer needs to be sufficient to avoid punch-through and allow process tolerance. Therefore, optimizing the p-GaN layer can result in lower channel resistance for targeted breakdown voltage. A controlled vertical etch would reduce the length of the tapered p-GaN layer.

In this dissertation, initially, the p-GaN thickness was kept 0.3µm. However, to allow more tolerance in the OG-FET fabrication process, it was increased to 0.4µm. The channel resistance accounted for ~10-20 % of the total on-resistance (in ohms).

4.5.3 Drift and substrate resistance

The substrate resistance contribution for small-area or unit-cell devices can be considered negligible. However, for large area devices, substrate resistance becomes important.

The drift resistance of the device is given by the following equation,

$$R_{DRIFT} = \frac{L}{qN_D\mu_{Drift}A} \quad 4.6$$

Where, N_D is the free carrier concentration or doping, μ_{Drift} is the drift layer mobility, L is the drift region thickness and A is the area. The doping and the thickness of the drift region also determines the breakdown voltage of the device. The lowering of drift resistance for a desired breakdown voltage can only be achieved by high quality material growth resulting in increased drift mobility. A method to extract drift region mobility is given by Gupta *et al* [61]. In this dissertation work, the drift region accounted for ~60-70 % of the total on-resistance (in ohms). These results indicate that source resistance should be minimized as it is the easiest to engineer with minimum trade-offs. Source resistance can be minimized by increasing source layer

thickness, higher doping, increased source electrode and n^+-GaN overlap, reduced distance between source electrode and trench, and using Al instead of Ti.

4.5.4 Sub-threshold slope and hysteresis

Apart from on-resistance, the sub-threshold slope (SS) and hysteresis are other important on-state metrics. Low SS is imperative for power devices. For normally-off devices, since off-state characteristics are measured at zero gate bias, low SS results in lower leakage. In this dissertation, with OG-FETs, lower sub-threshold slope was achieved compared to conventional trench MOSFETs. Further improvement in SS was obtained with AlSiO as the gate-dielectric compared to Al_2O_3. An improved interface quality will result in a lower SS. The best SS result obtained in this dissertation was 230 mV/dec.

In the on-state, under forward bias, electrons gets injected into the gate-dielectric resulting in charge trapping and hysteresis [44]. This is detrimental to device performance especially under switching conditions. Hysteresis resulting in increased threshold voltage gives rise to dynamic on-resistance degradation. Therefore, lower hysteresis is highly desirable in power devices for reliable operation. In this dissertation, lower hysteresis was achieved with OG-FETs compared to conventional trench MOSFETs. This was due to improved semiconductor/dielectric interface quality. Further improvements were obtained with AlSiO as the gate dielectric.

4.6 Off-state analysis

A power device holds voltage in the off-state. In vertical devices, the voltage is generally held in the low doped and thick drift region. The breakdown voltage (V_{BR}) can be related to drift region thickness (L) and doping (N_D) by the following equation,

$$V_{BR} = \frac{qN_D W^2}{2\varepsilon_o \varepsilon_r} \qquad 4.7$$

where, W is the depletion width at the breakdown and W < L. An ideal power device design targets breakdown to be achieved when drift region gets almost fully depleted (W = L).

Good gate control is needed to turn-off the trench MOSFET to avoid drain induced barrier lowering (DIBL) at high drain biases. In GaN trench MOSFETs, the p-GaN is generally doped with Mg > 5 x 10^{18} cm^{-3}, this reduces DIBL, as the p-GaN depletion region is thin relative to the total thickness. For example, p-GaN depletes ~20nm for a drain bias of 1000 V with a 1 x 10^{16} cm^{-3} free carrier concentration and 10μm thick drift region. Also, high p-GaN doping would help under switching conditions as mobile carriers matter while switching.

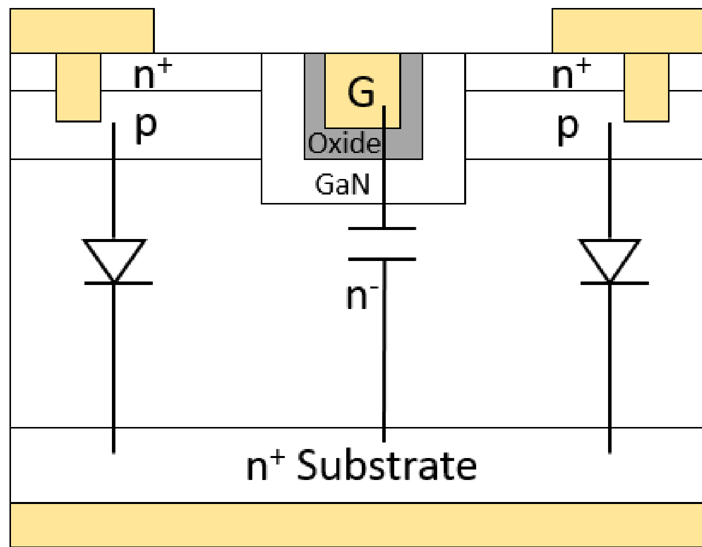


Figure 4.26: In the off-state, in OG-FET, voltage is held by the reverse biased p-n junction and reverse biased MOSCAP.

In trench MOSFET, the voltage is held by the reverse biased p-n junction (source-drain) and the reverse biased MOS capacitor (gate-drain junction) as shown in fig. 4.26. The gate-drain junction is usually etched in trench MOSFETs and since, high fields occur near the junction, it is imperative to obtain a low damage etch to sustain high fields in the off state. In

trench MOSFETs, the due to geometry, the peak electric field occurs at the trench corner in a well-designed edge terminated device. It is important to manage peak electric field at the trench corner to allow the full utilization of GaN's critical electric field. It has been shown that softening the trench corner by TMAH or chemical etch resulting in "shoe" (as described in the previous chapters) can result in lower peak electric field compared to a sharp trench corner [41]. Another way to reduce peak electric field is to fabricate trench MOSFETs with wider trenches, however, wider trenches result in increased pitch and increased gate capacitance.

Power devices require the highest material quality to allow high electric fields to be sustained reliably. In the next section, the impact of material quality on device breakdown is discussed.

4.6.1 Impact of material quality on device breakdown

To understand the impact of material quality of device breakdown, devices were fabricated on both bulk GaN and sapphire substrates and their breakdown performance was compared. As discussed in the earlier chapters, the MOS region is more susceptible to material quality issues compared to p-n diodes. Therefore, the OG-FET breakdown was studied as a function of trench area.

Circular trenches of radius 1μm, 2μm, 4μm and 8μm with total device size of 100μm radius were fabricated to study the breakdown voltage variation with increasing trench (MOS) area as shown in fig. 4.27. The area of the MOS region represents the dislocations existing in the MOS region. For example, with a threading dislocation density of ~2×10^{8} cm^{-2}, a circular trench of 16μm diameter would result in ~400 dislocations under the MOS area (Fig. 4.28). Here, it should be noted that the even though with increasing trench dimensions, the trench area was increasing, the source-drain (or equivalently p-n junction) area, however, was

approximately equal and sufficiently greater (~30000 μm^2) than the MOS area in these devices. Simulation studies were performed (in collaboration with Dong Ji) with Atlas Silvaco to obtain peak electric field in the device with increasing trench dimensions at V_{DS} = 600 V. Figure 4.29 shows the simulated electric field profile. It should be noted as discussed above, the peak electric field occurred at the trench corner and decreased with increasing trench dimension. However, the peak electric field difference between trench diameters (or widths) from 1μm to 8μm was not significant [61]. Therefore, almost similar peak electric field or breakdown voltage could be expected from OG-FETs.

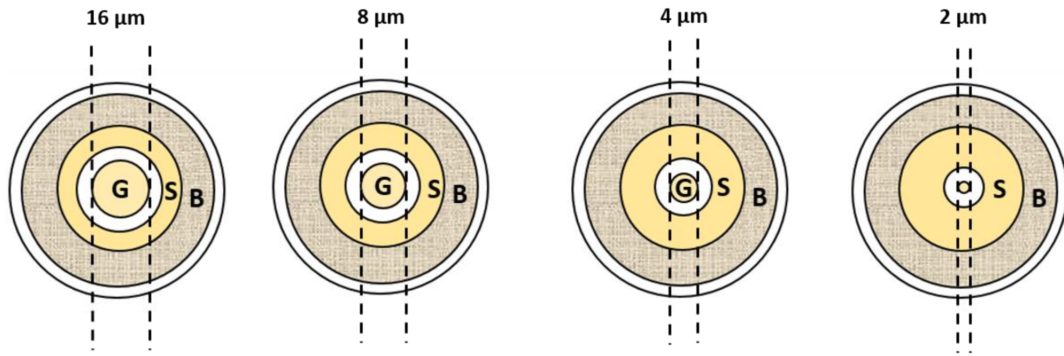


Figure 4.27: Circular devices with different radii (Top View). MOS area varied from ~200 μm^2 to ~3μm^2. The total device area was ~30000 μm^2 and was similar in all devices.

	16 μm	8 μm	4 μm	2 μm
Sapphire (2 x 10^8 cm^{-2})	~400	~100	~25	~6
Bulk (2 x 10^6 cm^{-2})	~4	~1	~0	~0

Figure 4.28: MOS area represents the dislocations under the MOS region.

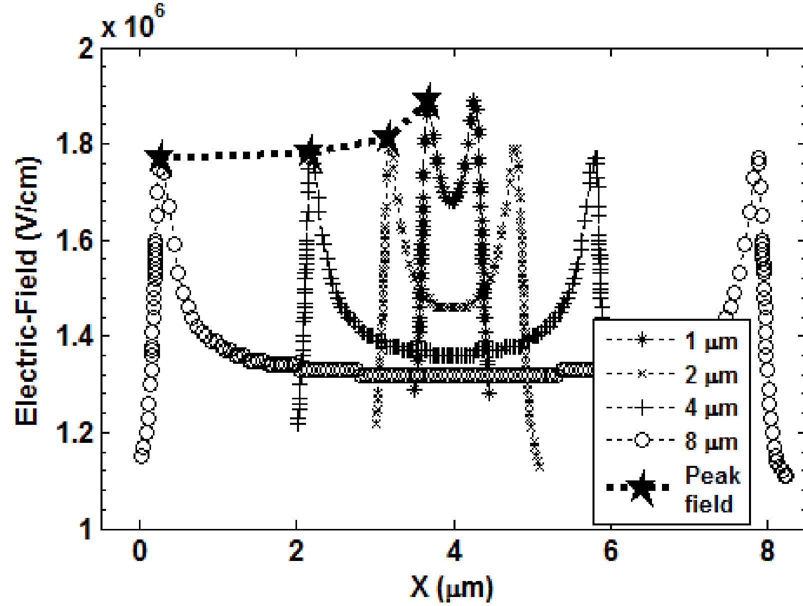


Figure 4.29: Simulated electric-field profile with different trench widths at V_{DS} = 600 V. (Copyright © 2017, IEEE)

It should be noted here that these results are only applicable in case of gate-drain breakdown. Catastrophic (hard) gate-drain breakdown was observed on both sapphire and bulk GaN devices in this experiment. This was confirmed by visual inspection and SEM.

Contrary to the simulation results, GaN on sapphire devices showed the opposite trend. The breakdown voltage decreased from 480 V to 290 V with an increase in the trench area from ~3 μm^2 (1μm radius) to ~200 μm^2 (8μm radius) as shown in fig. 4.30 [61]. However, the breakdown in devices fabricated on bulk GaN substrate was observed to be independent of the trench area (~3 μm^2-200 μm^2) for the same circular device designs. The results obtained on bulk GaN substrates corroborate simulation studies. These results strongly suggest that the increase in the breakdown voltage with narrower trenches in OG-FETs fabricated on sapphire substrates was related to the reduction in the number of dislocations (under the MOS area) [61]. Higher off-state leakage current was observed in devices fabricated on sapphire substrates

compared to bulk GaN devices (Fig. 4.31). This could be attributed to higher leakage in p-n diodes with dislocations.

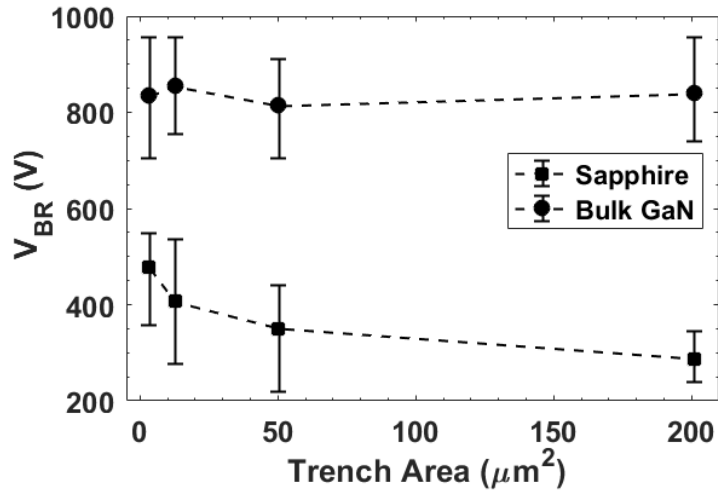


Figure 4.30: V_{BR} vs Trench area for both GaN on sapphire and bulk GaN devices. (Copyright © 2017, IEEE)

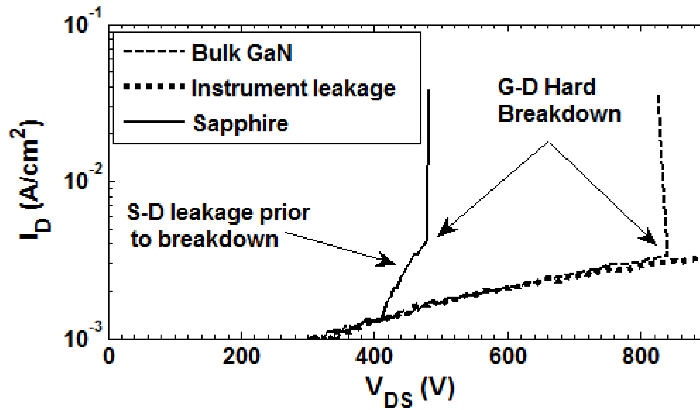


Figure 4.31: Off-state I-V characteristics for both sapphire and bulk GaN devices. (Copyright © 2017, IEEE)

These results demonstrate the impact of dislocations on the breakdown of trench MOSFETs. Commercially available bulk GaN wafers still contain a dislocation density of 10^4-10^7 cm^{-2} and may have dislocation clusters. The results of this study indicate that dislocations

are likely to have consequences on the lowering the yield of large-area devices required for high voltage/high current applications.

4.7 Dynamic performance of unit-cell OG-FETs

Dynamic performance analysis takes power devices one step closer to real switching conditions. So far, in this dissertation, DC performance was targeted, measured and analyzed. In this section, dynamic measurements on field plated OG-FETs are discussed. The OG-FETs demonstrated in section 4.3 were used to perform dynamic measurements.

A resistive single pulsed setup as shown in fig. 4.32 was used for dynamic on-resistance measurements. In this setup, the gate was pulsed while drain voltage (V_{DD}, as shown in fig. 4.32) was varied. The load resistor was chosen such that the device was expected to operate in the linear region in the on-state.

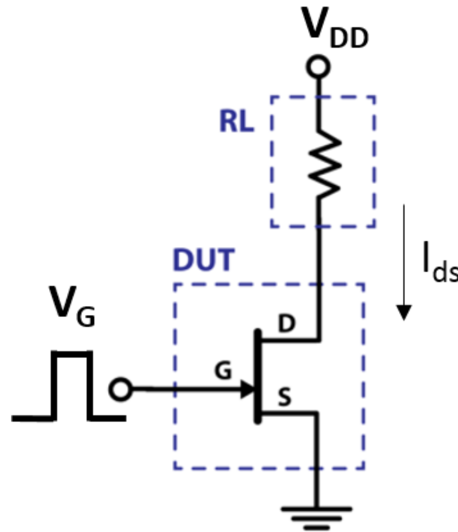


Figure 4.32: Dynamic performance measurement setup.

First, the impact of load resistor and device dimensions on response time was studied. The rise-time increased as the charging time constant increased with increasing resistor value.

However, fall-time was almost independent of the resistor value as the output capacitance discharges via FET (Fig. 4.33). The dependence of rise and fall times on load resistor is shown in fig. 4.34.

The device gate-width or absolute on-resistance affected the fall-time as the output capacitance discharges via FET resistance. Rise time was unaffected with variation in device dimensions (Fig. 4.34).

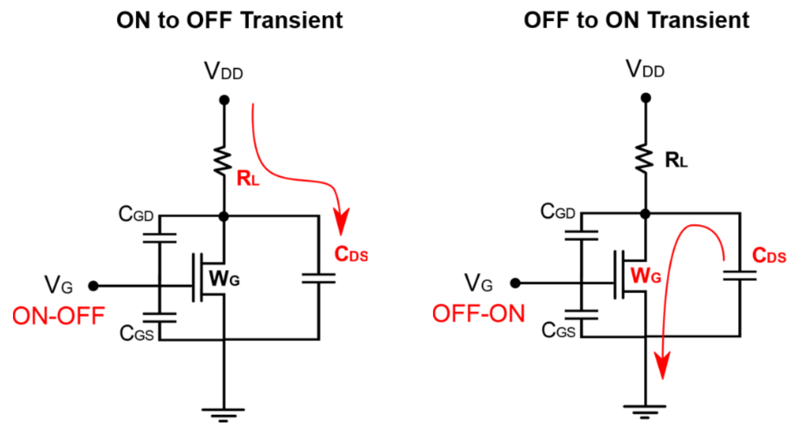


Figure 4.33: On-off and off-on transients in resistive gate pulse dynamic measurement setup.

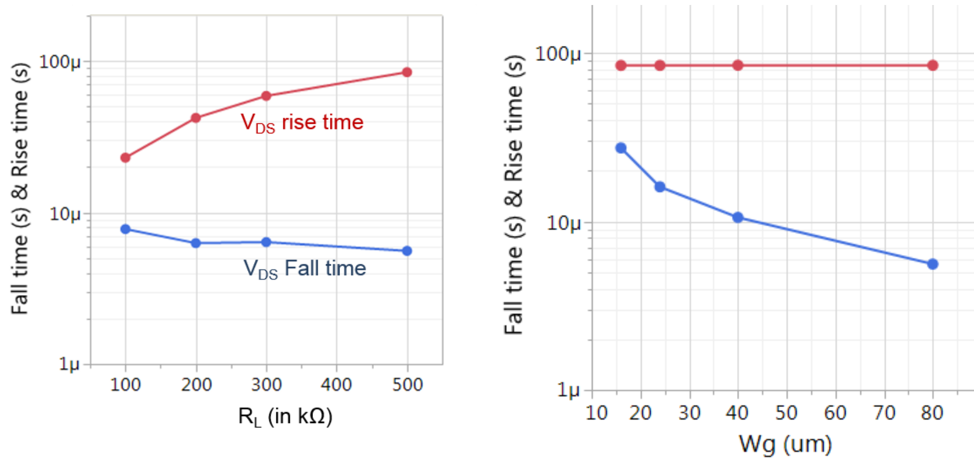


Figure 4.34: Impact of load resistor and gate-width on rise and fall times.

Therefore, dynamic on-resistance measurements were performed on the device with largest gate-width (~170µm). The gate was pulsed at V_{GS} = 12 V in the on-state and at V_{GS} = -8 V in the off-state. The total pulse time period was 20 ms, while the gate-pulse width was kept 100µs and 1000µs. For a pulse-width of 100µs, the device demonstrated a sharp increase in $R_{ON, DY}$ after 210 V. This was because device takes longer to discharge (increased fall-time) with increasing applied voltage. Hence, pulse-width was relaxed to measure fall-time suitably. With 1ms, the device exhibited 60% increase in $R_{ON, DY}$ at 500 V compared with on-resistance at V_{DD} = 50V (Fig 4.35).

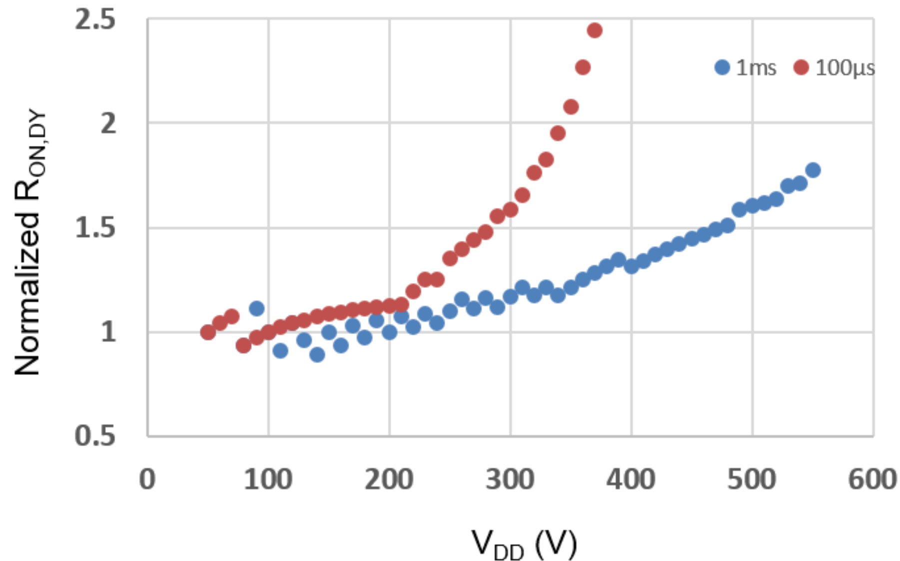


Figure 4.35: Dynamic on-resistance performance.

These devices demonstrated good dynamic performance with an 60% increase in $R_{ON, DY}$ at 500 V for 1ms pulse-width. To obtain such performance at shorter pulse-widths (few µs), large area OG-FETs resulting in low on-resistance need to be fabricated.

4.8 Large area OG-FETs

Large-area devices are a necessity to service high voltage/high current (1200 V/100 A) applications. Unit-cell OG-FETs provide currents upto few tens of mA. To obtain large currents, multiple unit-cells are connected in parallel. Large area OG-FETs were explored in collaboration with UC Davis.

Large area OG-FETs were fabricated on UCSB epi without edge termination [54]. The details of the experiment can be found in ref. 54. The maximum current obtained was ~0.65 A and the breakdown voltage was ~300 V. The unit-cell OG-FETs demonstrated a higher breakdown of 700 V. The lowering of breakdown with large area devices can be expected due to process and epitaxial variations across the wafer. Therefore, epitaxial and process control is important to fabricate large area high performing devices.

In the next processing run, OG-FETs were edge terminated and TMAH wet etch was employed [66]. Also, the epitaxy was obtained from IQE (p-n layer structure on bulk GaN substrates), which had uniform doping and thickness throughout the sample compared to UCSB epi. This resulted in improved large area performance with 0.5A current and 900 V breakdown voltage. Dynamic performance measurements on these OG-FETs were performed and will be published soon.

The large area OG-FET results are exciting and demonstrate OG-FET potential to be a competitive vertical GaN technology.

Chapter 5: Summary, conclusion, and future work

This dissertation was focused on the development of the in-situ Oxide, GaN interlayer based vertical trench MOSFET (OG-FET). In conventional GaN trench MOSFETs, the channel forms on the vertical etched p-GaN sidewall where sidewall roughness, ionized impurity scattering, and ex-situ gate-dielectric deposition can result in poor channel properties and can cause reliability issues. The OG-FET is a trench MOSFET variant targeted towards improving channel properties by re-growing a thin unintentionally doped (UID) GaN interlayer followed by the in-situ dielectric deposition on the trenched structure by MOCVD.

Since, this device was first of its kind, majority of the work was focused on the development of material growth and fabrication process to obtain high DC performance. Thus, material growth and fabrication process modules to achieve high performance vertical trench MOSFETs were identified and studied in detail. Major findings and device results are summarized in the subsequent section.

5.1 Summary

5.1.1 Material Quality

Vertical devices require the material of highest quality to operate reliably. Threading dislocations and carbon incorporation in drift layers are major concerns for vertical devices.

Studies performed to understand the impact of threading dislocations on device performance revealed that increased TD density results in increased reverse leakage current in GaN p-n diodes and causes lower breakdown of GaN MOSCAPs (with aluminum oxide as the gate-dielectric). The MOSCAP breakdown trend can be applied to other dielectrics which exhibit positive valence band offset with GaN.

The OG-FET devices fabricated on sapphire substrates demonstrated breakdown voltage dependence with trench MOSFET area while breakdown of devices fabricated on GaN substrates was independent of trench area. Also, lower leakage current was observed for bulk GaN devices compared to GaN on sapphire devices. This implies that fabricating large area devices or high current on sapphire substrates with high breakdown voltage is challenging.

Carbon incorporation can result in low free carrier concentrations or insulating layers and can significantly increase the resistance of the GaN layers. The epitaxial layers utilized in this work had non-uniform carbon incorporation resulting in non-uniform doping across the sample. However, majority of this dissertation work was targeted towards unit-cells, therefore, growths were not optimized.

To summarize, to fabricate high voltage and high current devices, uniform epitaxy with low threading dislocation density is needed.

5.1.2 Fabrication process

In the absence of wet etch of GaN, the trench-gate etch becomes a crucial step in the trench MOSFET fabrication process. Since, the peak fields at the trench bottom and corner, the damage to the underlying GaN crystal due to the dry etch needs to be minimized. In this dissertation work, a low damage 15 W BCl_3/Cl_2 etch was used to achieve >1 kV devices on bulk GaN substrates.

Alongside, low damage trench gate-etch, edge termination is also important to allow high breakdown voltage to be realized. Edge termination reduces the peak field at the device edge and results in higher breakdown. This dissertation work employed a field-plate based edge termination. This resulted in enhancing the useful breakdown field from ~1.5 MV/cm to ~2.3 MV/cm.

Vertical devices are generally fabricated in a hexagonal layout to reduce the on-resistance by utilizing the maximum chip area. In this regard, the hexagonal crystal structure of GaN allows the utilization of certain crystal planes as sidewalls upon which the MOS channel can be formed. Our studies revealed that fabricating GaN sidewall channel on *m*-plane results in improved on-state characteristics such as channel mobility, hysteresis, sub-threshold slope etc. compared to *a*-plane sidewall channel.

	Trench MOSFET (Toyoda Gosei)	Normalized data for comparison	OG-FET (UCSB)
V_{TH}	3.5 V		2 V – 4 V
V_{BR} (@ V_{GS})	1600 V (-10 V) 8 x 10^{15} cm^{-3}, 13μm	1200 V (-10 V) 1.1 x 10^{16} cm^{-3}, 12μm	1200 V (-1 V) 1.1 x 10^{16} cm^{-3}, 12μm
E_{BR}	~2.3 MV/cm		~2.3 MV/cm
R_{ON}	2.7 mΩ.cm^2	2.35 mΩ.cm^2 Active area & doping	**2 mΩ.cm^2**
V_{GS} @ R_{ON} (E_{OX})	40 V (~5 MV/cm)		**12-15 V (~2 MV/cm)**

Figure 5.1: Comparison of OG-FET data with best available unit-cell trench MOSFET data from T. Oka *et al* [48]. Here, the breakdown was normalized to the drift region doping and thickness to provide same breakdown field. Also, the on-resistance was also normalized according to active area defined in this work and accounted for drift region doping and thickness.

5.1.3 Device results and comparison with state-of-the art unit cell GaN trench MOSFETs

High DC performance was achieved in this dissertation work with devices fabricated on bulk GaN substrates. The devices exhibited 900-1200 V breakdown voltage, an on-resistance of 2-4 mohm.cm^2 alongside normally-off operation with threshold voltage between 1.5 V-3.5 V. A comparison of OG-FET performance with best available unit cell GaN trench MOSFET data (at the time of this dissertation work) is shown in figure 5.1.

To allow a fair comparison, the breakdown field was calculated for GaN trench MOSFET and breakdown voltage was calculated for 1.1 x 10^{16} cm^{-3} and 12 μm thick drift region doping and thickness respectively. Since, breakdown fields were similar, normalized data resulted in same breakdown voltage in both devices. For on-resistance, more conservative active area definition as defined in this work was utilized alongside the scaling of on-resistance with drift region doping ratio (11/8). Here, this is a conservative normalization as the drift region doping will only affect the drift region resistance and increased doping will potentially reduce mobility as well. However, we assumed same mobility and scaled total on-resistance for simplicity.

The results shown in fig. 5.1 clearly demonstrate the advantages offered by OG-FET device design compared to GaN trench MOSFETs.

5.2 Conclusion

To conclude, this dissertation work conceptualizes and demonstrates a novel device design (OG-FET) to improve the on-state characteristics and reliability of GaN trench MOSFETs while maintaining similar off-state performance and normally-off operation. The results obtained evidences the advantage gained from OG-FET device design over state-of-the-art trench MOSFETs.

5.3 Future Work

5.3.1 On-state characteristics

To improve on-resistance in both unit-cell and multi-cell OG-FETs, device dimensions such as source-electrode to trench distance etc. can be scaled to reduce device foot-print and resistances. In multi-cell OG-FETs, the pitch can be reduced to allow better utilization of the drift region and thus resulting in reduction of drift resistance [14].

Further improvement can be obtained by improving channel mobility. This can be accomplished by improving the quality of channel interface. TMAH based wet etching following dry etch can be performed to obtain smooth perfect vertical sidewalls on *m*-plane [11]. This will result in lower roughness at the regrowth interface.

Another possible way to enhance channel mobility is by using a AlGaN/GaN based hetero-junction as shown in fig. 5.2. Here, the channel will form at AlGaN/GaN interface instead of dielectric/GaN interface as in OG-FET. Here, the AlGaN/GaN regrowth needs to be optimized to provide high mobility and normally-off behavior simultaneously.

Gate dielectric annealing studies can be performed to improve robustness of the gate under forward bias.

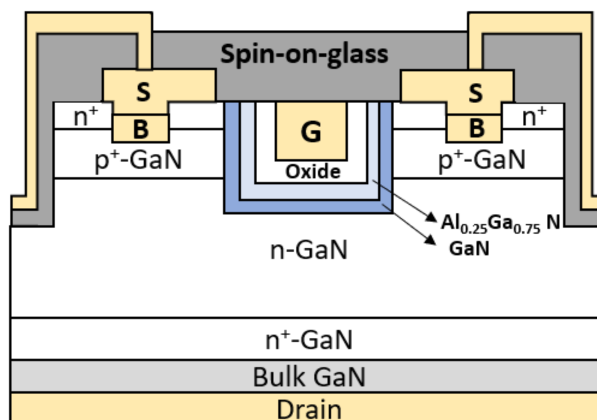


Figure 5.2: Regrown AlGaN/GaN channel based GaN trench MOSFET.

5.3.2 Off-state characteristics

The breakdown field available from OG-FET devices is around ~2.3 MV/cm. This is approximately 75% of the field that can be achieved before avalanche breakdown is observed. Therefore, off state characteristics needs to be improved to allow avalanche breakdown to be achieved in OG-FETs.

Since, the OG-FET device was breaking down at the trench bottom or trench corner, the electric field needs to be reduced. To reduce peak electric field at the trench corner, the corners can be rounded using TMAH as shown in fig 5.3.

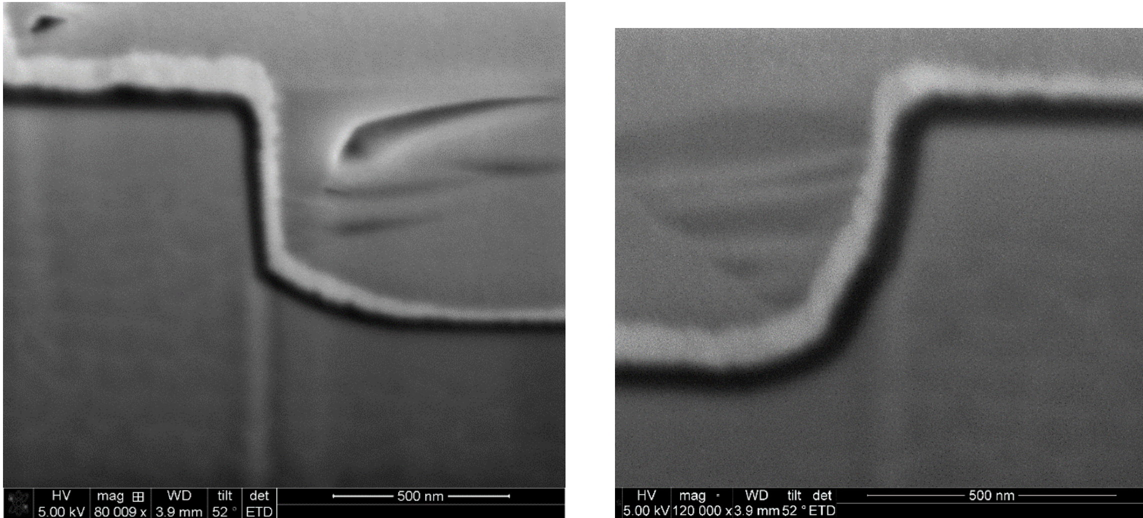


Figure 5.3: (Left) Trench profile after dry etch. (Right) Trench profile after dry etch + TMAH wet etch.

Another potential solution is to deposit selectively thicker gate-dielectric at the bottom to strengthen the gate-drain MOS region [22]. To ensure high trans-conductance, relatively thinner gate-dielectric will be desirable on the sidewall.

5.3.3 Switching and stress testing

This dissertation work was primarily focused on achieving high DC performance, therefore, switching and stress analysis was not performed in great detail. Since, this device design has achieved reasonable high DC performance as a result of this work, therefore, switching and stress testing of OG-FETs is imperative at this juncture. Early switching results indicate the need to improve gate- stack performance. Post-deposition annealing alongside TMAH process can result in highly reliable gate-stack for OG-FETs.

Additionally, good ohmic contacts to p-GaN needs to be achieved in this device design. The potential issue with a non-ohmic contact has been discussed in ref. [11]. The p-GaN ohmic contact can be achieved by a selective area p-GaN regrowth as performed in ref. [16].

Appendix A: Process Traveler

Field Plated OG-FET Traveler

Trench Etch				
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	SPR 220-3	Spin	2500 rpm	30 sec
	Bake		115°C	90 sec
	Cool			1 min
Expose				
	[10,36]		Trench Etch	
	Stepper 1	F/O = 0		2.4 sec
Post-Exposure				
	Bake		115°C	90 sec
Develop				
	AZ300MIF			70 sec
	DI Water	Running		2 min
Observe				
Etch				
	RIE 5	MAHR_LP2	~6 nm/min	As req.
Strip				
	AZNMP Rinse		80°C	~10 min.
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Measure Depth	AFM/Dektak			
Regrowth Clean				
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				

	Bake		115°C	3 min
Expose	UV-ozone			15 min.
Etch	HF (48%)			1 min.
	DI Water	Running		1 min
Expose	UV-ozone			15 min.
Etch	HF (48%)			1 min.
	DI Water	Running		1 min
Expose	UV-ozone			15 min.
Etch	HF (48%)			1 min.
	DI Water	Running		1 min
Regrowth	MOCVD			
Source etch				
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	SPR 220-3	Spin	2500 rpm	30 sec
	Bake		115°C	90 sec
	Cool			1 min
Expose				
	[10,36]		Source Etch	
	Stepper 1	F/O = 0		2.4 sec
Post-Exposure				
	Bake		115°C	90 sec
Develop				
	AZ300MIF			70 sec
	DI Water	Running		2 min
Observe				
Al_2O_3 Etch				
Conditioning	ICP 1	#134 (50 W)		5 min.
Etch	ICP 1	#134 (50 W)	~2-2.5 nm/min	As desired
Strip				
	AZNMP Rinse		80°C	~10 min.

	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Measure depth	AFM/Dektak			
Body Etch				
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	SPR 220-3	Spin	2500 rpm	30 sec
	Bake		115°C	90 sec
	Cool			1 min
Expose				
	[10,36]		Source Etch	
	Stepper 1	F/O = 0		2.4 sec
Post-Exposure				
	Bake		115°C	90 sec
Develop				
	AZ300MIF			70 sec
	DI Water	Running		2 min
Observe				
n^+-GaN Etch				
Calibration	RIE 5	GEET_LPE		10 min.
Etch	RIE 5	GEET_LPE	~6 nm/min	As desired
Strip				
	AZNMP Rinse		80°C	~10 min.
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Measure depth	AFM/Dektak			
p-GaN Activation				
	MOCVD Oven		700°C	20 min.

Body Metal				
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115^oC	3 min
PR Spin				
	OCG 825	Spin	5000 rpm	30 sec
	Bake		95^oC	1 min
	Cool			1 min
	SPR 955-0.9	Spin	3500 rpm	30 sec
	Bake		90-95^oC	1 min
	Cool			1 min
Expose				
	[10,36]	Body Metal		
	Stepper 1	F/O = 0		1.6 sec
Post-Exposure				
	Bake		100^oC	2 min
Develop				
	AZ300MIF: DI	2:1		90 sec
	DI Water	Running		2 min
Observe				
	HCl:DI	2:1		30 sec
Metal Deposition				
	E-Beam 1	Ni	1500 A	Flat
Liftoff				
	AZNMP-Rinse		80^oC	> 2 hrs
	Isopropyl	NO Ultrasonic		3 min
	DI Water	Running		1 min
Gate & Source				
Clean				
	Acetone			
	Isopropyl	NO Ultrasonic		3 min
	DI Water	Running		1 min

Dehydration				
	Bake		115°C	3 min
PR Spin				
	OCG 825	Spin	5000 rpm	30 sec
	Bake		95°C	1 min
	Cool			1 min
	SPR 955-0.9	Spin	3500 rpm	30 sec
	Bake		90-95°C	1 min
	Cool			1 min
Expose				
	[10,36]	Gate & Source		
	Stepper 1	F/O = 0		1.6 sec
Post-Exposure				
	Bake		100°C	2 min
Develop				
	AZ300MIF: DI	2:1		90 sec
	DI Water	Running		2 min
Observe				
	HCl:DI	2:1		30 sec.
Metal Deposition				
	E-Beam 1	Ti/Au	300/2000 A	Rotation
Liftoff				
	AZNMP-Rinse		80°C	> 2 hrs
	Isopropyl	NO Ultrasonic		3 min
	DI Water	Running		1 min
Isolation				
Clean				
	Acetone	No Ultrasonic		3 min
	Isopropyl	No Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	SPR 220-3	Spin	2500 rpm	30 sec
	Bake		115°C	90 sec

	Cool			1 min
Expose				
	[10,36]		Isolation Etch	
	Stepper 1	F/O = 0		2.4 sec
Post-Exposure				
	Bake		115°C	90 sec
Develop				
	AZ300MIF			70 sec
	DI Water	Running		2 min
PR Reflow	Bake		110°C	5 min
Observe				
Etch				
	RIE 5	MAHR_LP2	~6 nm/min	As req.
Strip				
	AZNMP Rinse		80°C	~10 min.
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Measure Depth	AFM/Dektak			
FP Dielectric				
SOG Spin		Spin	5000 rpm	40 sec
	Bake		90°C	1 min
			150°C	1 min
			210°C	1 min
	Curing	Furnace 1	SOG recipe	60 min (425°C)
Measure	Oxide thickness			
FP Dielectric Etch				
Clean				
	Acetone	NO Ultrasonic		3 min
	Isopropyl	NO Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	SPR 220-3	Spin	2500 rpm	30 sec
	Bake		115°C	90 sec

	Cool			1 min
Expose				
	[10,36]		FP Etch	
	Stepper 1	F/O = 0		2.4 sec
Post-Exposure				
	Bake		115°C	90 sec
Develop				
	AZ300MIF			70 sec
	DI Water	Running		2 min
Observe				
SiO_2 Etch				
Conditioning	ICP 1	#145		5 min.
Etch	ICP 1	#145	~80 nm/min	As desired
Strip				
	AZNMP Rinse		80°C	~10 min.
Liftoff				
	Isopropyl	No Ultrasonic		3 min
	DI Water	Running		1 min
Measure depth	AFM/Dektak			
FP Metal				
Clean				
	Acetone	NO Ultrasonic		3 min
	Isopropyl	NO Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	OCG 825	Spin	5000 rpm	30 sec
	Bake		95°C	1 min
	Cool			1 min
	SPR 955-0.9	Spin	3500 rpm	30 sec
	Bake		90-95°C	1 min
	Cool			1 min
Expose				
	[10,36]	FP Metal		

	Stepper 1	F/O = 0		1.6 sec
Post-Exposure				
	Bake		100°C	2 min
Develop				
	AZ300MIF: DI	2:1		90 sec
	DI Water	Running		2 min
Observe				
	HCl:DI	2:1		30 sec.
Metal Deposition				
	E-Beam 1	Ti/Au	300/2000 A	Rotation
Liftoff				
	AZNMP-Rinse		80°C	> 2 hrs
	Isopropyl	NO Ultrasonic		3 min
	DI Water	Running		1 min
Liftoff				
	NMP		80°C	> 2 hrs

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