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Publication Date 2017

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UNIVERSITY OF CALIFORNIA

Los Angeles

Design and Performance of Near-Infrared Nanowire Photodetectors

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of

Philosophy in Electrical Engineering.

by

Alan Cervantes Farrell

2017

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ABSTRACT OF THE DISSERTATION

Design and Performance of Near-Infrared Nanowire Photodetectors

by

Alan C. Farrell

Doctor of Philosophy in Electrical Engineering University of California, Los Angeles, 2017 Professor Diana L. Huffaker, Chair

The research in this dissertation attempts to take advantage of the nanowire platform in order to outperform state-of-the-art commercial detectors in one or more metrics. Nanowire photodetectors with increasing cutoff wavelength and device complexity will be presented, beginning with simple GaAs homojunction photodetectors. It is shown that through proper design, an ideality factor of n = 1.0 - 1.15 and dark current density as low as $J = 6 \times 10^{-7}$ A/cm² can be achieved, both equivalent to the best bulk GaAs diodes. The design principles learned from this study are applied to all of the nanowire photodetectors that follow. InGaAs-GaAs heterojunction photodetectors exhibit n = 1.06 and a responsivity of up to 30 A/W, indicating avalanche gain. InGaAs avalanche photodetectors are shown to have low excess noise with k = 0.15 and a bandwidth of 2.4 GHz. InGaAs-GaAs single photon avalanche diodes are operated in free-running mode with an ultra-low dark count rate of less than 60 Hz, a photon count rate of 8 MHz, and a

timing jitter less than 38 ps. Free-running mode operation is possible through the control of afterpulsing through single nanowire avalanche pulses, with a maximum afterpulsing probability less than 25%. Finally, InAsSb-InAs heterojunction photodetectors are presented with an absorption cutoff at 3.0 µm and a maximum quantum efficiency of 29%. This work shows that for most photodetectors operating in the near-infrared, the nanowire platform can either match or surpass conventional planar photodetector performance, and in the case of single photon detectors, provides a compelling case for the commercialization of nanowire-based photodetectors.

This dissertation of Alan C. Farrell is approved.

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Acknowledgements

This thesis was made possible through the support and contributions of several individuals and organizations. I would first like to thank my committee chair and advisor Diana L. Huffaker for taking a chance on me, and the remainder of my committee, whose guidance and suggestions contributed to the completion of this dissertation. Mariko Walton, for noticing my admissions application in a pile of almost certainly more impressive applications. The past and current staff of the UCLA Integrated Systems Nanofabrication Cleanroom: Lorna Tokunaga, Yuwei Fan, Tony Wright, Da Teng, and Krissy Do for always taking the time to help when I needed it. The staff at the Office of Graduate Student Affairs: Deeona Columbia and Mandy Smith, for taking care of everything behind the scenes. The National Science Foundation through the Clean Green IGERT Fellowship, the Eugene V. Cota Robles Fellowship, and the Dissertation Year Fellowship for the financial support during the five years of my Ph.D. studies.

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Ren, D., **Farrell, A. C.**, Williams, B. S., and Huffaker, D. L., "Seeding layer assisted selectivearea growth of As-rich InAsP nanowires on InP substrate", Nanoscale, *just accepted*, DOI: 10.1039/C7NR00948H.

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Patent disclosures

Plasmonically enhanced Nanopillar Separate Absorption Multiplication Diodes. Hufffaker, D. L., Senanayake, P., Hung, C.-H., Farrell, A. C., U.S. Provisional Patent Application No.:61/911,371

1. Introduction

1.1. Overview

Semiconductor photodetectors have become the technology of choice for applications that demand durability, high sensitivity, fast response times, and low cost. Commercially available photodetectors provide high detection efficiency at wavelengths from the visible spectrum to the long wavelength infrared (LWIR). The standard photodetector is the p-i-n diode. This structure allows operation at zero-bias for extremely high sensitivity, and can be biased for high speed operation. A p-i-n photodetector is characterized by three primary performance metrics: 1) responsivity, 2) dark current density, and 3) response time. Other performance metrics exist, such as noise-equivalent-power (NEP), but they are derived from the more fundamental performance metrics. The NEP provides a simple metric to compare photodetectors with different responsivities and dark current densities. The responsivity, $\mathcal{R}(\lambda)$, is defined as the photocurrent resulting from a given incident power at a given wavelength and has units of A/W. The responsivity is related to the quantum efficiency, η , by

$$\mathcal{R} = \eta \, \frac{q}{hf} \tag{1.1}$$

where q is the electron charge, h is Planck's constant, and f is the frequency of light. The dark current density, J, is calculated by normalizing the measured current by the photodetector junction area.

It can be difficult to compare two detectors if both the responsivity and dark current density are different. For example, consider photodetector 1 (PD1) whi ch has a responsivity \mathcal{R}_1 and dark

current density J_1 , and photodetector 2 (PD2) with a responsivity $\mathcal{R}_2 = 0.3\mathcal{R}_1$ and dark current density $J_2 = J_1/10^2$. It is not immediately apparent which photodetector is superior. This is where NEP is useful, as it is defined as the signal power that gives a signal-to-noise ratio (SNR) of one in a one hertz bandwidth and has units of W/ $\sqrt{\text{Hz}}$. For a photodetector dominated by shot noise and thermal noise, the SNR is given by

$$SNR = \frac{I_p^2}{\sigma_{shot}^2 + \sigma_{thermal}^2} = \frac{\mathcal{R}^2 P_{in}^2}{2q(\mathcal{R}P_{in} + I_d) + 4(k_b T/R_L)F_n} \cdot \frac{1}{\Delta f}$$
(1.2)

where P_{in} is the incident power, I_d is the dark current, k_b is the Boltzmann constant, T is the temperature, R_L is the load resistance, and F_n is the amplifier noise figure. Setting Eq. 1.2 equal to one and solving for $P_{in}/\Delta f$ gives the NEP. Note that the NEP depends on both the responsivity and dark current, and is therefore a useful metric for comparing different detectors. This is especially important for the nanowire photodetectors presented in this dissertation, as the responsivity can be much lower than for a planar photodetector, but at the same time the dark current is also much lower. Therefore, an accurate comparison should look at the SNR or NEP.

The response time is typically presented as either a bandwidth measurement or a pulse response measurement, and so the metric is either bandwidth (Hz) or rise(fall) time (s), defined as the time it takes the output signal to rise(fall) from 10%(90%) to 90%(10%) of the peak signal value. The response time is affected by three factors: 1) the transit time of carriers through the depletion region, 2) the RC response, determined by the capacitance of the photodetector, and 3) slow diffusion of carriers generated in the quasi-neutral regions. As a result, high-bandwidth photodetectors are typically very small area in order to minimize the capacitance. The transit time can be reduced by decreasing the depletion region width, however this also reduces the responsivity and increases the capacitance and so this is not a useful approach.

Avalanche photodetectors (APDs) are characterized by two additional performance metrics: 1) gain, and 2) excess noise factor, which by convention, is parameterized by the ratio of electron to hole ionization coefficients, k. The gain is simply the measured photocurrent normalized by the primary photocurrent,

$$M = \frac{I_{ph}}{I_{pr}} \tag{1.3}$$

For a simple p-i-n structure, determination of I_{pr} is straightforward, as essentially all of the photogenerated carriers are collected at zero bias. For more complex structures, such as the separate absorption, multiplication (SAM)-APD, the situation is more complex. At low bias, a barrier exists between the absorber and the avalanche region. This barrier prevents photogenerated carriers from being collected, and the responsivity is extremely low. As the bias is increased, the barrier is lowered, until eventually it is eliminated entirely and all of the carriers are collected, known as *punch-through*. In the simplest case, the photocurrent at punch-through is the primary photocurrent and the gain is easily calculated. However, complications can arise. For example, it is possible that the avalanche process begins before punch-through, leading to an overestimation of I_{pr} and an underestimation of M. In more complicated structures, there may be a second barrier that makes it difficult to determine when all of the primary photocurrent has been collected. Comparing I_{pr} to that of a p-i-n can support the estimate, but is not a direct measurement. The only way to *directly* confirm that the primary photocurrent is not mixed with avalanche current is to measure the noise.

The RMS noise current of unmultiplied current can be described by shot noise theory, and is given by

$$\sigma_{shot}^2 = 2q(I_{ph} + I_d)\Delta f = 2q(RP_{in} + I_d)\Delta f$$
(1.4)

The avalanche process adds additional noise on top of the shot noise, and is given by

$$\sigma_{excess}^2 = 2qM^2F(I_{ph} + I_d)\Delta f = 2qM^2F(RP_{in} + I_d)\Delta f$$
(1.5)

where F is the excess noise factor, and is related to k by

$$F(k,M) = kM + (1-k)(2-1/M)$$
(1.6)

Thus, by measuring the noise as a function of photocurrent (where the photocurrent is varied by increasing the reverse bias), a change in the slope of the noise indicates that the avalanche process has begun. This is a very complicated measurement and is only necessary when there are significant doubts about the primary photocurrent.

The SNR of an APD is described by an expression similar to a p-i-n, with σ_{shot}^2 replaced with σ_{excess}^2 :

$$SNR = \frac{I_p^2}{\sigma_{excess}^2 + \sigma_{thermal}^2} = \frac{(M\mathcal{R}P_{in})^2}{2qM^2F(\mathcal{R}P_{in} + I_d) + 4(k_bT/R_L)F_n} \cdot \frac{1}{\Delta f}$$

When $M\mathcal{R}P_{in}$ is small, i.e., low gain and/or low incident power, the noise is dominated by the thermal noise component and increasing M results in an increase in the SNR. Increasing M also increases F at a rate determined by k. Eventually, the shot noise will dominate and increasing M further results in a decrease in the SNR. Thus, there is an optimum value of M that maximizes the SNR. For silicon APDs, the low value of k leads to $M_{opt} \approx 100$, while for InGaAs APDs, the high value of k leads to $M_{opt} \approx 10$.

When an APD is operated as a single photon avalanche diode (SPAD), four additional performance metrics are required: 1) dark count rate (DCR), 2) photon count rate (PCR), 3) photon

detection efficiency (PDE), and 4) timing jitter. The DCR is due to pulses generated by the generation of carriers in the bulk of the absorber. These dark pulses are indistinguishable from pulses generated from the absorption of photons and are thus the background noise of the SPAD. The PCR is limited by several factors, including the response time of the SPAD, external electronics, and incident photon flux. The PDE is similar to the responsivity, but also takes into account the probability that the carrier generated by an absorbed photon initiates avalanche breakdown. Finally, the timing jitter is the variation in the delay between the arrival of the photon and the generation of the output pulse by the SPAD, and is important for sensitive timing applications.

1.2 Nanowire photodetectors

Commercial p-i-n photodetectors, APDs, and SPADs all suffer from certain unavoidable performance tradeoffs. The nanowire platform can circumvent many of these tradeoffs due to both the nanostructure of the devices as well as the ability to grow high quality lattice-mismatched materials. In some cases, the advantages may be small and not enough to justify the increased complexity. In other cases, nanowire photodetectors may provide unprecedented performance enhancements that suggest commercialization of nanowire photodetectors may be profitable. It is the goal of this dissertation to push the limits of nanowire photodetectors of each type, and determine what, if any, and to what extent the performance of commercial photodetectors can be surpassed.

1.3 Design considerations

Nanowire photodetectors fall into two main categories: 1) horizontal single nanowire photodetectors, and 2) vertical nanowires array photodetectors. While interesting from a scientific point of view, horizontal single nanowire photodetectors are not a practical design from the



Figure 1.1 Nanowire device fabrication (**a**) As-grown nanowire array are (**b**) planarized by spin-coating with BCB. (**c**) The nanowire tips are exposed by dry-etching in an Oxford 80 RIE. (d) Electrical contact to the nanowires is made by depositing metal with the samples mounted at an angle, resulting in a partially exposed nanowire surface.

commercialization point of view. Since the focus of this work is bringing nanowire photodetector performance up to commercial standards, we will focus on vertical nanowire array photodetectors. In this category of nanowire photodetectors, there are several subcategories defined by the growth technique: 1) catalyzed growth, 2) self-catalyzed growth, 3) selective-area catalyzed growth, and 4) selective-area catalyst-free growth. Once again, since the commercialization is a design goal in this work, catalyzed and self-catalyzed growth are immediately eliminated because they result in randomly located nanowires with random diameters and heights. Selective-area growth allows the location and diameter of the nanowires to be determined before growth by electron beam lithography (EBL), making the nanowire morphology a design parameter. In this work, catalyst-free growth is favored over catalyzed growth, as the catalyst, typically gold, is considered an unnecessary complication. I have little doubt that many, if not all, of the results of this work can be reproduced using gold-catalyzed growth, but with the added complication of additional



Figure 1.2 Schematic of nanowire photodetector fabricated structure. The Cyclotene acts as both structural support for the nanowires, as well as electrical isolation of the top contact from the substrate.

processing for sample preparation (gold deposition) and device fabrication (gold catalyst removal), as well as the added cost using gold.

Fabrication of photodetectors from as-grown nanowire arrays is shown schematically in Fig. 1.1. As-grown nanowire arrays are planarized by spin coating with a dielectric polymer, in this case Cyclotene 4000 series resin made by Dow Chemical Company. This polymer is photosensitive, allowing the polymer to be patterned by photolithography before curing. Following the curing of the polymer, the nanowire tips are exposed by RIE. Finally, electrical contact to the nanowires is made by depositing metal with the samples mounted at an angle, resulting in a partially exposed nanowire surface to allow light absorption.

The advantage of this fabrication technique is the simplicity. Nothing more than simple photolithography and lift-off techniques are required. Since the nanowire arrays are defined by



Figure 1.3 False-color SEM of fabricated nanowire device. The partial gold shell around each nanowire acts as a surface plasmon antenna. Scale bar is 500 nm.

EBL, each wafer piece in a growth contains 50-100 devices which are easily fabricated by photolithography. A schematic of the final fabricated structure is shown in Fig. 1.2.

1.4 Surface plasmon resonance enhanced absorption

Although a significant aspect of photodetector performance depends on absorption efficiency, this topic has been covered extensively in the literature and is not the focus of this work, which will focus on the equally important and often neglected electrical performance of the devices. Nonetheless, these are photodetectors after all, and so a brief discussion on the absorption of light in nanowires is necessary. Although semiconductor nanowires have proven to be a viable path towards nanoscale photodetectors, the dramatic reduction in semiconductor absorption volume can have a negative effect on responsivity (1). In order to overcome the reduced absorption volume, incident light must be focused within the nanopillar and surface reflections must be minimized. The ability to lithographically define the position and diameter of individual nanowires makes



Figure 1.4 (a) Plasmonic resonance can be shifted to longer wavelengths by increasing the nanopillar array pitch. (b) A minimum in the reflectance occurs at the same wavelength as a maximum in the photoresponse. (c) Photocurrent exhibits a clear polarization dependence.

surface plasmon polariton (SPP) resonances an attractive option, as regular metal scattering centers can overcome the momentum mismatch between the incident wavevector and the SPP mode and scattering center size can influence optical aborption enhancement (2).

Reflection spectrometry is a simple and effective tool for sensing surface plasmon resonances (3), and was used to characterize the 3-dimensional plasmonic antenna. The photodetector active area, consisting of exposed nanowires with a partial gold shell (Fig. 1.3) was



Figure 1.5 (**a**) Measured (blue circles) and simulated reflectance spectra (solid line). FDTD simulations of absorbed power within a nanopillar at a reflection (**b**) dip and (**c**) peak show enhanced absorption at resonance.

illuminated by a synchrotron white light source which was focused to a 10 µm spot using a continuum IR microscope and the reflectance spectra was captured and analyzed with an FTIR-spectrometer. Fig. 1.4a shows the measured reflectance spectra for devices with pitches varying from 750 nm to 900 nm in 50 nm increments. A clear shift in the reflectance minimum to longer wavelengths is observable for increasing array pitch. In order to verify this reflection minimum is due to a plasmonic resonance and not to increased scattering outside the collection area of the objective, wavelength dependent photocurrent measurements were carried out using a supercontinuum white light source coupled to an acousto-optic tunable filter for wavelength selection. Fig. 1.4b shows the spectral photoresponse (the sharp drop near 1200 nm is due to the bandgap of InGaAs) and the correspending relectance spectrum. A peak in the photoresponse is readily observed at wavelengths near the reflection minimum, with a 67% reduction in reflectance resulting in a 51% increase in the photocurrent. Thus, 76% of the reduced reflection can be attributed to enhanced optical absorption in the nanopillar. Ohmic loss in the metal contact or surface recombination in the semiconductor likely accounts for the loss. The 3-dimensional

plasmonic antenna is not symmetric, and thus it is not surprising that a polarization dependence is observed (Fig. 1.4c). The reflectance spectrum is simulated by finite-difference-time-domain (FDTD) simulations of a single nanopillar unit cell with periodic boundary conditions. Although reflectance measurments were performed with focused light (range of incident angles), simulations were limited to a plane-wave source. As a result, the simulated reflectance spectrum shows more narrow, well defined reflectance dips (Fig. 1.5a). FDTD simulations of the plasmonic modes indicate the absorbed power density is located almost exclusively within the exposed nanowire tips at resonance (Fig. 1.5b), while little power is absorbed in the nanowires off resonance (Fig. 1.5c).

This study shows that it is possible to adjust the SPP resonance to the target wavelength by choosing the nanowire array pitch accordingly. However, it is important to note that the exposed height of the nanowires is extremely important and effects the amount of light absorbed at the SPP resonance. For example, two devices with the same pitch but different exposed heights will have a resonance at the same wavelength, however, the photocurrent will be much larger in the device with the larger exposed height. If the exposed height is too small, e.g., less than 400 nm, the responsivity is extremely low as the absorption volume becomes too small to support the SPP mode. In this work, no attempt to maximize light absorption is made, as the focus of this work is on the electrical characteristics of nanowire photodetectors. There is little to gain by optimizing the electrical properties, then repeating the device growth and fabrication in order to improve the responsivity since the tuning of light absorption is well studied and understood. The reader is therefore asked to keep this in mind when evaluating the performance of the photodetectors presented in this work.

1.5 Approach

The focus of this dissertation is near-IR photodetectors. The study will begin with the simplest case: a GaAs homojunction p-n photodiode. Although this structure has been studied many times over in the literature, there still is a significant gap between nanowire photodetector performance and commercial photodetector performance. In Chapter 2, GaAs homojunction p-n photodiodes are presented that finally achieve bulk-equivalent performance in a nanowire photodetector. The lessons learned from this study are applied to every device studied in the remainder of the dissertation and results in bulk-equivalent or better performance from all devices. The subsequent photodetectors not only increase the cutoff wavelength, but increase the device complexity. Chapter 3 investigates InGaAs/GaAs heterojunction p-n photodetectors, including the first measurement of excess noise in a nanowire-based APD. Chapter 5 demonstrates an InGaAs/GaAs nanowire single photon detector, including the first measurements of dark count rate, photon count rate, afterpulsing probability, and timing jitter in a nanowire-based SPAD. Finally, Chapter 6 looks at InAsSb/InAs heterojunction photodetectors, and the prospects of MWIR nanowire photodetectors.
2.1. Overview

Semiconductor nanowires are frequently touted as promising building blocks for a variety of nanoscale electronic and optoelectronic devices. The primary criticism of nanowire devices is the large surface-to-volume ratio and the deleterious effect of surface states on electrical properties. Indeed, for thin film devices involving mesa etching, the etched surface presents a problem as the diameter of the mesa becomes small, eventually dominating the carrier transport in the device (4,5). As a result, *ex-situ* passivation of the etched sidewalls is necessary to minimize these effects (6,7). Nanowire growth and fabrication is intrinsically different in that there is no post-growth etching required, and therefore no ex-situ passivation is required; all sidewalls are passivated through in-situ growth of a high-bandgap shell. To date however, all demonstrations of nanowire devices have been inferior to their thin film counterparts in most performance metrics, including ideality factor and dark current density.

The dark current at room temperature in p-n diodes employing III-V semiconductors with a short carrier lifetime and/or small intrinsic carrier concentration is dominated by bulk generation current through recombination centers at the midgap in the depletion region (8–10). Hence, even the best thin film GaAs diodes have an ideality factor of n = 1.1 - 1.5 (8,11,12). However, the vast majority of nanowire-based p-n junctions reported to date have an ideality factor of n > 2, higher than expected for a GaAs diode dominated by bulk generation or surface leakage current. This is likely due to either improper device design, poor bulk material quality, or inadequate surface passivation (13,14). The best reported ideality factor of $n \approx 1.6$ and rectification ratio of 10^5 was achieved with a vertically-aligned array core-shell p-n junction diodes with an InGaP passivation shell (15,16). In both cases, nanowire arrays are embedded in benzocyclobutene (BCB), which has been shown to effectively passivate GaAs surfaces (17,18). It is difficult, however, to determine the effectiveness of the BCB passivation because for these core-shell structures a fraction of the junction area exists in air above the BCB.

In this chapter, we present a p-GaAs nanowire array on n-GaAs substrate operating as p-n diode with the junction at the nanowire-substrate interface. The purpose of this approach is to ensure the depletion region remains below the surface of the BCB in order to assess the effectiveness of InGaP + BCB passivation. The standard perimeter-to-area analysis is not suitable for this study as it is not easy to control or define the nanowire diameter due to unavoidable lateral overgrowth and the variation in nanowire height with mask-hole diameter. Therefore, the effectiveness of the passivation is inferred from ideality factor and dark current density. Fully 3-dimensional simulations are employed in order to analyze the electrical characteristics. The results are compared to the standard 1-dimensional analysis and the range of applicability is discussed.

2.2. Electrical characterization

2.2.1 Growth conditions

GaAs nanowires were grown on a n-doped GaAs (111)B substrate by selectrive area epitaxy using metal-organic chemical vapor deposition in an Emcore vertical-flow reactor at a pressure of 60 torr and temperature of 730°C. A passivation shell was subsequently grown *in situ* at 600°C. The primary precursers were trimethylindium (TMIn), trimethylgallium (TMGa), tertiarybutylarsine (TBAs), and tertiarybutylphosphorus (TBP); the p-dopant was diethylzinc (DEZn). The V/III ratio for the GaAs core and the InGaP shell were 40 and 25, respectively. The



Figure 2.1 (**a**) False-color SEM image of fabricated nanowire array p-n diode. Scale bar is 50 μm. (**b**) Close-up view of diode active area showing nanowire array. Scale bar is 500 nm. (**c**) Schematic of device structure.

ratio of DEZn to TMGa partial pressures was 0.02. The InGaP passivation shell thickness was 10 nm; the gas phase indium composition was 40%.

2.2.2 Dark current

Fig. 2.1a shows the device layout, including BCB, via, substrate, and nanowire electrical contacts. Note that the ground-signal-ground contacts are not necessary for this study, but are merely a convenience allowing the use of existing photolithography masks. The close-up view in Fig. 2.1b shows the partial gold shell and self-aligned hole resulting from tilted metal deposition. The purpose of this design is discussed in detail elsewhere (*19,2,20*), but for our purposes in this



Figure 2.2 Dark I-V for sets of nanowire array diodes of various array sizes.

study it simply serves as electrical contact to the nanowires. The schematic in Fig. 2.1c shows the nanowire device structure. A p-GaAs nanowire is surrounded by an InGaP shell acting as a passivation layer. Because the doping in the substrate ($\sim 3 \times 10^{18} \text{ cm}^{-3}$) is much higher than in the nanowire ($\sim 5 \times 10^{16} \text{ cm}^{-3}$), the result is a one-sided p-n diode, with the depletion region extending primarily through the nanowire. Therefore, the electrical characteristics reflect the structure and properties of the nanowire component of the device.

Nanowire array diodes are patterned with various array diameters. Five diodes of each diameter are patterned on the GaAs die. The measured I-V characteristics for each set are plotted



Figure 2.3 (**a**) Measured (symbols) I-V of a typical nanowire-array p-n diode at room temperature, and the calculated (line) I-V using the Shockley equation. (**b**) Temperature dependence of the ideality factor. Inset: Bias dependence of the ideality factor at room temperature. (**c**) Arrhenius plot of the saturation current.

in Fig. 2.2. Apart from some variation in the series resistance, the diode characteristics are fairly uniform, although it is not clear why the series resistance varies from device to device. It is possible that there is some residual BCB remaining on the exposed nanowire surface before electrical contact, resulting in random variations in the amount of surface area contacted directly with metal. Another possibility is that the thickness of the BCB varies with position, resulting in variation in exposed height of the nanowires contacted with metal. The reverse bias leakage current appears to



Figure 2.4 Dark current at room temperature for two sets of identical nanowire diodes composed of single nanowires and 3×3 arrays of nanowires. Inset: Close-up SEM of single nanowire diode. Scale bar is 500 nm.

become more uniform as the number of nanowires in the array increases (with the exception of the largest arrays), indicating that non-uniformities from nanowire to nanowire are averaged out. There is no correlation between the forward and reverse bias currents, i.e., a larger forward bias current does not correspond to a larger reverse bias current. There were a few "dead" devices (five out of thirty), i.e., no current flow through the device. These were not plotted as they contain no useful information. This is likely due to the nanowires becoming separated from the substrate during device processing.

The current-voltage (I-V) relationship of an 80 μ m × 80 μ m (6,400 nanowires) nanowire array p-n diode is shown in Fig. 2.3a along with the calculated I-V using the Shockley equation

$$I = I_0 \left\{ exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1 \right\}$$
(2.1)

with $I_0 = 4.8 \times 10^{-12}$ A, n = 1.15, and $R_s = 1.8 \Omega$. The ideality factor reaches the minimum of n = 1.15 above 250 K (Fig. 2.3b) and is independent of bias up to about 0.4 V, where series

resistance effects prevent accurate fitting (Fig. 2.3b, Inset). In Fig. 2.3c, an Arrhenius plot of the saturation current is used to extract the activation energy, assuming

$$I_0 \propto exp\left(\frac{E_a}{kT}\right) \tag{2.2}$$

giving $E_a = 690$ meV at room temperature and $E_a = 21$ meV at low temperature. At room temperature, the activation energy is roughly half the bandgap of GaAs, indicative of midgap states. The low temperature activation energy of 21 meV is likely due to zinc dopants (21), but carbon impurities may also contribute (22).

The maximum rectification ratio of this particular device is 2.1×10^9 (at 1 V_{fb}), the highest reported to date for a nanowire p-n diode of any material. The series resistance for a single nanowire diode can be calculated by dividing the total series resistance by the number of nanowires in the array, giving $R_s = 11 \text{ k}\Omega$. By calculating the area of the nanowire contacted with metal, the specific contact resistance is estimated to be $r_c = 1.3 \times 10^{-5} \Omega \cdot cm^2$. Similarly, the dark current per nanowire at 1 V_{rb} is estimated to be about 0.8 fA. Single nanowire diodes and 3×3 nanowire diodes were also fabricated and characterized (Fig. 2.4). The plot shows two representative I-V curves of each array size, with very little variation between devices. Note that it is not possible to determine the rectification ratio for these devices as the dark current is below the sensitivity of the measurement. However, for the single nanowire device it is at least 10^8 and for the 3 \times 3 nanowire diode it is at least 10⁹. The series resistance for a single nanowire diode was found by fitting to the Shockley equation and gave $R_s = 9.4 \text{ k}\Omega$, and for the 3 × 3 nanowire diode we find $R_s =$ 12.1 k Ω per nanowire. Interestingly, the ideality factor for these nanowire diodes is n = 1.0, as opposed to n = 1.15 for the larger nanowire array. The reason for this will be explained in section 2.3.3. The reverse bias current for both single and 3×3 nanowire diodes is less than the noise

floor of the measurement setup (~50 fA), supporting the 0.8 fA/nanowire estimate from the larger array.

For bulk photodetectors, the dark current density is given by $J = I/A_j$, where I is the measured current and A_j is the area of the etched mesa, i.e., the junction area. For nanowire photodetectors, the situation is not so clear. A nanowire photodetector is typically composed of a large number nanowires, N_{nw} , electrically contacted in parallel. There are two device areas to consider here: 1) the *effective* device area, A_{eff} , of the array, including the empty space between the nanowires, and 2) the total junction area, $N_{nw}A_j$, of the array of nanowires (or equivalently, the total device area multiplied by the junction fill factor, F_j , e.i., $A_j = F_j \cdot A_{eff}$). Let us define the *junction* dark current density as $J_j = I/A_j$, and the *effective* dark current density as $J_{eff} = I/A_{eff}$. In the literature, the dark current density of multi-nanowire devices is typically normalized using A_{eff}^{2-4} . This is likely due to the difficulty in estimating F_i for arrays grown by gold-catalyzed methods, which yield randomly distributed nanowires of varying diameters. The lack of an accurate estimate of F makes comparison of J_j difficult, if not impossible. Note that J_{eff} is not meaningful on its own. As an example, consider two nanowire photodetectors (labeled 1 and 2) with $A_{eff}^{(1)} = A_{eff}^{(2)}$, but with device 1 having a higher density of nanowires, i.e., $A_j^{(1)} > A_j^{(2)}$. Suppose now that $J_{eff}^{(1)} = J_{eff}^{(2)}$. If only A_{eff} and J_{eff} are given, we might incorrectly assume that these devices are equivalent, when in fact device 1 is superior since the same dark current is achieved with a greater number of nanowires. This simple example illustrates the importance of A_i for device comparison. Nanowire growth by selective-area epitaxy yields arrays with a predetermined number of nanowires of nearly identical diameter. In this case, estimating F_i is



Figure 2.5 Dark and photocurrent as a function of bias for a representative photodetector with 80 µm diameter active area.

trivial, and accurate comparison of nanowire to bulk J_j can be done with ease. For our photodetector, the effective dark current density is given by

$$J_{eff} = \frac{I_{dark}}{A_{eff}} = 8 \times 10^{-8} \,\mathrm{A} \,\mathrm{cm}^{-2}, \tag{2.3}$$

and the junction current density is given by

$$J_j = \frac{I_{dark}}{A_j} = 7 \times 10^{-6} \,\mathrm{A} \,\mathrm{cm}^{-2}, \tag{2.4}$$

Note that this calculation was done using the diameter of the hole patterned in the growth mask, *i.e.*, the true junction area, rather than the nanowire diameter, which is typically greater than the junction area.

2.2.3 Responsivity

Another important photodetector performance metric is responsivity, *R*. Nanowire diodes were illuminated with a 670 nm fiber-pigtailed laser diode. The total incident power of 100 μ W

was measured with a calibrated silicon detector. Under-filling of the active area was verified by observing a plateau of the photoresponse for nanowire array diodes with diameters \geq 80 µm. Fig. 2.5 shows the dark and photocurrent of an 80 µm diode at room temperature. As with the calculation of the dark current density, interpreting the meaning of *R* for a nanowire array photodetector requires special care. Recall that *F* < 1, and so most of the incident light does not fall directly on the nanowires, leading to a responsivity that is directly proportional to the density of nanowires. In the example above, suppose that $R^{(1)} > R^{(2)}$. Once again, without knowledge of A_j , we might conclude that device 1 is the better light absorber, although in reality the light absorption per nanowire may be higher in device 2. Increasing the density of nanowires to improve the responsivity, however, will result in a corresponding increase in J_{eff} (recall that J_j is the real

current density and thus is independent of nanowire density). Thus, while dark current density and responsivity are independent for bulk photodetectors, they are inexorably tied to each other for nanowire photodetectors. We define the effective responsivity, R_{eff} , as the total photocurrent normalized by the total incident laser power (assuming the active area is underfilled):

$$R_{eff} = \frac{I_{ph}}{P} = \frac{1 \times 10^{-5} A}{1 \times 10^{-4} W} = 0.1 A/W$$
(2.5)

Parameter	Value	Units
Number of nanowires in 80um array (1 um pitch)	5026	
Total incident laser power (P)	100	μW
Laser spot size diameter	50	μm
Photocurrent	10	μΑ

Table 2.1. Parameters used for calculation of responsivity.

This is the standard calculation for planar photodetectors. When we compare a nanowire array with the same area as a planar photodetector, we must consider the fact that the fill factor of 1% reduces both I_{dark} and I_{photo} . But unlike I_{dark} , I_{photo} is not reduced by a factor of 100, *i.e.*, without plasmonic enhancement, responsivity of the NW array would be 0.004 A/W. The measured value of R = 0.1 A/W indicates plasmonic enhancement increase the nanowire's ability to absorb light by a factor of 25.

We can also define the optical absorption-area responsivity, R_a , as the photocurrent density normalized by the laser power density:

$$R_a = \frac{J_{photo}}{P/A_{laser}}.$$
(2.6)

The photocurrent density, J_{photo} , is the measured photocurrent divided by the illuminated area area:

$$J_{photo} = \frac{I_{photo}}{A_{ill}} \tag{2.7}$$

For a planar photodetector, $A_{ill} = A_{laser}$ and $R_{eff} = R_a = R$, as expected. However, for a nanowire array photodetector,

$$A_{ill} = \frac{A_{laser}}{A_{eff}} N_{nw} A_{nw}$$
(2.8)

where A_{nw} is the cross-sectional area of a nanowire, and the area factor reduces this to the number of illuminated nanowires. Substituting Eqs. 2.7 and 2.8 into Eq. 2.6 gives

	Conditions	Min.	Typical	Max.	Units
J_j	-1 V, 300 K	6×10^{-7}	7×10^{-6}	1×10^{-5}	A/cm ²
J _{eff}	-1 V, 300 K	6×10^{-9}	8×10^{-8}	2×10^{-7}	A/cm ²
<i>R_{eff}</i>	-1 V, 633 nm		0.1		A/W
R_a	-1 V, 633 nm		8.2		A/W

 Table 2.2. Dark current density and responsivity calculated using both the total

 nanowireray area as well as by using a single nanowire.

$$R_a = \frac{A_{eff}}{N_{nw}A_{nw}} \cdot \frac{I_{photo}}{P} = \frac{R_{eff}}{F_a}.$$
(2.9)

where $F_a = N_{nw}A_{nw}/A_{eff}$ is the optical absorption fill factor (as opposed to the junction area fill factor, $F = N_{nw}A_j/A_{eff}$). It is important to use F_a rather than F_j because $F_a > F_j$ due to radial overgrowth. Using Eq. 2.9, and the measured nanowire diameter of 137 nm, we get $R_a = 8.2 A/W$. This is about 20 times higher than would be expected for a planar GaAs photodetector and is due to surface plasmon resonance enhanced absorption. Table 2.2 summarizes the dark current density and responsivity calculations for this device.

2.2.4 Ideality factor

Recombination current in the region where the junction space-charge region intersects with the surface is known to produce a current with n = 2 at a forward bias as high as 1V (23). Bulk current behaves similarly at low forward bias, where recombination in the junction space-charge region dominates, but drops to n = 1 at high forward bias where diffusion current becomes very large (24). The absence of an n = 2 region for the GaAs nanowire p-n diode at low forward bias is surprising, and merits discussion. For an n^+ -p junction at a forward bias greater than a few kT/q, the total current can be approximated by

$$J_{FB} = J_D + J_{re} \approx \frac{qD_n n_i^2}{L_n N_A} \exp\left(\frac{qV}{kT}\right) + \frac{qW_D n_i}{2\tau_n} \exp\left(\frac{qV}{2kT}\right)$$
(2.10)

where J_D and J_{re} are the diffusion and bulk recombination current components, D_n is the electron diffusion coefficient, τ_n is the electron lifetime, N_A is the acceptor doping level, and W_D is the depletion region width. The ratio of the diffusion to recombination current is thus

$$\frac{J_D}{J_{re}} = \frac{2n_i D_n \tau_n}{N_A L_n W_D} \exp\left(\frac{qV}{2kT}\right)$$
(2.11)

With the parameters for GaAs given in the Appendix, we get

$$\frac{J_D}{J_{re}} \approx \frac{10^{10} \text{ cm}^{-3}}{N_A}$$
 (2.12)

at 300 mV. It is clear that even at background doping levels (~10¹⁵ cm⁻³) the diffusion current in GaAs is several orders of magnitude smaller than the recombination current and we expect n = 2. At a bias greater than 1 V (with $N_A = 10^{16}$ cm⁻³), the diffusion current is greater than the recombination current and n = 1. To understand why this behavior is not observed in the GaAs nanowire diode, we note that since the nanowires are less than 1 µm long, then $L_n \approx 3 \mu m \gg W_{QN}$, where W_{QN} is the width of the quasi-neutral region in the nanowire. Thus, this is a narrow-base diode and the diffusion current component should be much larger than suggested by the previous analysis.

2.3. Electrical modeling

2.3.1 Electric field and depletion region

In order to quantify the increase in diffusion current and determine whether it can account for the absence of a recombination dominated current at low forward bias, we perform fully 3dimensional (no rotational symmetry) electrical simulations. The simulation domain is schematically shown in Fig. 2.6a. The simulations include the effects of Shockley-Read-Hall recombination, including surface recombination. The dimensions of the nanowire were defined based on SEM measurements of the actual nanowires. Every surface was treated as non-ideal with a surface recombination velocity. All dimensions and material/surface parameters can be found in the Supplementary Information. It is important to note that the contact to the nanowire is defined not only on the top facet, but on three of the sidewalls above the BCB, as in the actual device. As we will see shortly, this has a dramatic effect on the device characteristics.

At the top of Fig. 2.6b, 2-dimensional views of the electric field distribution are shown at 0 V and 5 V reverse bias, along with 1-dimensional cuts through the center of the nanowire below. It is immediately apparent that the electric field distribution within this nanowire device structure is markedly different than a thin film device. Initially, the electric field is confined within the BCB layer, and resembles the standard triangular profile of a 1-dimensional device. As the bias is increased, the depletion region edge approaches the portion of the electrical contact at the surface of the BCB. As the bias is increased further, the depletion region edge is pinned at the surface of the BCB and produces a second peak in the electric field. We next investigate the bias dependence of W_D . We define the edge of the depletion region as the location where the electric field drops below 10 kV/cm. Fig. 2.6c shows W_D as a function of $V_{rb} + \psi_{bi}$ for nanowire doping concentrations of 2×10^{16} cm⁻³ to 5×10^{17} cm⁻³. It is well known that for 1-dimensional



Figure 2.6 (a) Electric field distribution in 3-dimensional space. The segment of the nanowire exposed to air is kept fixed at 400 nm, while the portion buried in BCB is varied between 300 and 600 nm by adjusting the total height of the nanowire. (b) 2D cuts of the electric field distribution at 0 Vrb and 5 Vrb, and 1D cuts of the electric field through the center of the nanowire. (c) Simulated depletion region width for several p-doping concentrations (symbols) and calculated depletion region width with the exponential dependence on the bias voltage used as a fitting parameter.

devices with abrupt junctions, $W_D \propto (V_{rb} + \psi_{bi})^m$, with m = 0.5 and m = 1/3 for graded junctions. For the nanowire device, we find $m \approx 0.5$ for higher doping and gradually increases to



Figure 2.7 (a) Measured (symbols) capacitance per nanowire and calculated capacitance assuming the standard m = 0.5 bias dependence for an ideal diode (blue solid line) and the calculated capacitance using the simulated depletion region width (red solid line). (b) Simulated forward bias current (symbols) for a short (700 nm) and long (1000 nm) nanowire, and the calculated forward bias current using the Shockley equation using a single diode model for the short nanowire and a 2-diode model for the long nanowire. (c) Carrier concentration through the center of the p-GaAs nanowire. The position of the contact is marked for easy comparison.

 $m \approx 1$ as the doping decreases. When the depletion region edge is pinned to the BCB surface, we find m = 0.2, regardless of doping concentration.

2.3.2 Capacitance

In order to estimate the doping concentration in the nanowire diode, we measured the capacitance-voltage (C-V) characteristics and assume $C \propto W_D^{-1}$ to calculate the capacitance using he previous simulations. In Fig. 2.7a, the capacitance per nanowire (symbols) is plotted along with the capacitance of an ideal diode assuming $C = C_0/(\psi_{bi} + V)^{0.5}$ and the calculated capacitance using $C = C_0/W_D$, where C_0 is a proportionality factor adjusted to fit the data. The best fit to the data was achieved by using W_D calculated for a doping concentration of 5×10^{16} cm⁻³. The fact that the measured C-V exhibits an m = 0.2 region is clear evidence that the depletion region edge is pinned at the BCB surface for reverse bias greater than 1 V. This means that the depletion region edge is very close to the BCB surface at 0 V, and supports the narrow-base diode argument put forward earlier. It is worth noting the standard $1/C^2$ analysis of the measured C-V data gives ψ_{bi} = 4.1 V and $N_A = 1 \times 10^{23}$ cm⁻³, which is clearly nonsensical. This exemplifies the need for careful attention to the validity of the equations used to analyze nanowire devices. The question naturally arises as to whether the $1/C^2$ analysis yields accurate results if the measured capacitance is proportional to $(\psi_{bi} + V)^{-0.5}$. We found that some devices on the same sample do, in fact, have a capacitance bias dependence with m = 0.5. The $1/C^2$ analysis was performed on one of these devices, discussed below, and we found $\psi_{bi} = 1.74 \text{ V}$ and $N_A = 6 \times 10^{16} \text{ cm}^{-3}$. Although the built-in voltage does not agree well with the simulated built-in voltage, $\psi_{bi} = 1.33$ V, the doping concentration is very close to what was found through 3D simulations.

A few of the measured devices located closest to the outer edge of the substrate exhibit a bias-dependent capacitance with m = 0.5 beyond -1 V (Fig. 2.8, Inset). Based on the analysis just discussed, this is likely a result of the increase in thickness of the BCB near the edge of the substrate of about 200 nm—a natural byproduct of the spin-coating process—that moves the



Figure 2.8 Analysis of capacitance using 1D equations to extract doping concentration and built-in voltage. Inset: Measured C-V for a nanowire array diode showing an m = 0.5 dependence on the bias.

electrical contact a larger distance from the depletion region edge. If the depletion region width has a bias dependence with m = 0.5, the standard 1D analysis of the C-V data yields accurate results for the doping concentration. The built-in voltage, however, is not accurately found using this analysis, likely because the area-normalization of the capacitance is not well defined (area of the nanowire and area of the junction are not equivalent because of radial overgrowth). The slope of $1/C^2$ is not affected by a constant factor, and so the doping concentration should be accurate regardless of the uncertainty in the area. The plot of $1/C^2$ vs. bias is shown in Fig. 2.8. The equation of the linear fit is

$$\frac{1}{C^2} = (-1.69V + 2.86) \times 10^{14} F^{-2}$$
(2.13)

from which we find $N_A = 6.5 \times 10^{16} \text{ cm}^{-3}$ and $\psi_{bi} = 1.74 \text{ V}$. From the 3D simulations we concluded $N_A \approx 5 \times 10^{16} \text{ cm}^{-3}$ and $\psi_{bi} = 1.33 \text{ V}$.

2.3.3 Ideality factor

The forward bias current was simulated for nanowires with heights of 700 and 1000 nm, shown in Fig. 2.7b. The long nanowire exhibits a two-diode behavior with n = 2 region at low forward bias and an n = 1.15 region at high forward bias, typical of thin film GaAs diodes. The short nanowire, on the other hand, has a single diode ideality factor of n = 1.3. The fact that n = 1.15 for the experimental devices is irrelevant, as this analysis is simply intended to elucidate the factors that lead to non-standard characteristics in nanowire diodes, i.e., $m \neq 0.5$ and single diode behavior. To understand the difference between the long and short diodes, we look at the simulated electron concentration within the p-type nanowire at 0.3 V forward bias, shown in Fig. 2.7c. Since the excess electrons recombine at the contact, the electron concentration at the axial position of the contact is drawn with dotted lines for both long and short diodes. Note that the electron concentration at the contact is much higher in the short diode than in the long diode. This explains the increase in diffusion current responsible for eliminating the n = 2 region at low bias.

2.4. Discussion

We have demonstrated vertically-oriented nanowire array GaAs p-n junction diodes with ideality factors as low as n = 1, rectification ratios > 10⁸ (with a maximum of 2 × 10⁹), and dark current density comparable to bulk. It was shown through detailed 3-dimensional simulations that the ideality factor is affected by an increase in the diffusion current resulting from the narrow-base diode structure. The diffusion current thus exceeds the recombination current and eliminates the low-bias n = 2 region typical of GaAs thin film diodes. In addition, the capacitance of a nanowire diode was shown to exhibit atypical behavior in the rate at which the capacitance decreases as a function of reverse bias, initially increasing more rapidly, then less rapidly than expected for thin film diodes. This was attributed to depletion region pinning at the BCB surface as the electric field

approaches the electrical contact. This work demonstrates that it is entirely possible to achieve bulk-like performance from nanowire devices if proper design considerations are implemented. In addition, we showed that electrical characterization of nanowire devices must be done with care and the standard 1-dimensional $1/C^2$ analysis does not yield accurate results for the doping concentration unless m = 0.5.

3.1 Overview

Modern fiber optic communications relies on InGaAs p-i-n photodetectors because of their reliability, high detection efficiency at 1550 nm, high speed, and small package. Planar InGaAs photodetectors are restricted to a single indium composition, x = 0.53, due to lattice matching constraints on InP substrate. At this composition, InGaAs photodetectors have a cutoff at approximately 1700 nm at room temperature. For certain applications, it may not be necessary to detect light beyond a shorter wavelength, i.e., a more gallium rich InGaAs would suffice. The obvious benefit to a reduced indium composition is a decrease in generation-recombination current, which would increase the sensitivity of the photodetector. Nanowire growth does not suffer from the same strict lattice matching constraints, allowing a range of low indium compositions to be grown on GaAs substrate.

In this chapter, we explore the growth of gallium rich InGaAs on GaAs, and near-lattice matched growth on InP. We determine the composition mainly through photoluminescence, but verify the composition with EDX on occasion. Photodetectors are fabricated and characterized on both GaAs and InP substrates.

3.2 Gallium-rich InGaAs on GaAs

3.2.1 Growth

InGaAs nanowires are grown at 730° C using trimethylindium (TMIn), trimethylgallium (TMGa) and tertiarybutylarsine (TBAs) as source precoursors. The V/III ratio is 40, and the total



Figure 3.1 Tilted SEM of InGaAs nanowires grown on n+GaAs (111)B substrate.

Nanowires height is 1300 nm and diameter is 220 nm.



Figure 3.2 Room temperature photoluminescence of InGaAs nanowire array on GaAs substrate. The emission peak is at 1380 nm.

growth time is 13 minutes. Fig. 3.1 shows a tilted SEM of an InGaAs nanowire array with 100% yield and extremely high uniformity. From photoluminescence measurements, shown in Fig. 3.2, the composition is estimated to be about 40% indium. The weak emission at ~900 nm is from the n-GaAs substrate.

3.2.2 Electrical characterization

The forward bias current at room temperature is shown in Fig. 3.3. In the low forward bias regime, the ideality factor is approximately 2, while in the high forward bias regime, the ideality factor is approximately 1. Although this is typical behavior for generation-recombination dominated devices, it is unusual for the n = 1 regime to begin at such a low forward bias (0.2 V). From the analysis of GaAs photodetectors in Chapter 2, we can explain this by an increase in the diffusion current in a narrow-base diode. This is supported by the fact that the forward bias current reaches the compliance of 1 mA at only 0.75 V for a device of 80 µm diameter. Such a large current is evidence of a large diffusion current component. Once again, we achieve bulk-like characteristics in nanowire devices by simply ensuring the depletion region is contained entirely beneath the surface of the BCB in an axial structure.



Figure 3.3 Forward bias current of InGaAs NW-PD. The low forward bias regime has an ideality factor of about 2, and in the high bias regime the ideality factor is nearly 1.



Figure 3.4 Reverse bias dark current and current under illumination by a 1064 nm continuous-wave laser with a power of 41 μ W.

The reverse bias dark current and photocurrent is shown in Fig. 3.4. The illumination source is a 1064 nm continuous wave laser with a power of 41 μ W. It is difficult to determine the primary photocurrent, as there is clearly a bias-dependence even at low reverse bias. At low reverse bias, this is due to an increase in carrier collection efficiency caused by the expanding depletion region. At high bias, there is clearly avalanche gain, as the responsivity approaches R = 30 A/W, shown in Fig. 3.5. It is possible that the carrier collection efficiency continues to improve as avalanche gain begins to increase the responsivity, making it very difficult to accurately determine the gain.

Nanowire arrays with mask holes from 80 nm to 140 nm were grown on a single sample, allowing comparison of electrical characteristics on devices from the same growth. Fig. 3.6 shows the dark current and photocurrent for typical devices with each mask hole diameter. Although there is little change in the photoresponse (indicating a weak dependence of the surface plasmon resonance on the nanowire diameter), the dark current is strongly dependent on the mask hole



Figure 3.5 The photocurrent vs. incident optical power is measured at 0 V, -10 V, and -14 V. The response is linear, allowing a linear fit to be used to extract the responsivity.



Figure 3.6 Dark current and photocurrent for devices with increasing mask hole diameter on the same sample.

diameter. The dark current increases more rapidly than a simple surface or volume dependence would suggest. The likely cause is once again a result of the characteristics of narrow-base diodes. Note that as the diameter of the mask hole increases, not only does the dark current increase, but the bias dependence decreases, becoming more like a diffusion-limited device. The nanowire



Figure 3.7 Measured (symbols) and calculated (lines) dark current for devices with indium composition of 30% (open symbols) and 40% (filled symbols). The doping is a fitting parameter in the drift-diffusion equations.

height decreases for increasing mask hole diameter, which in turn increases the diffusion current in the device, since the base becomes more narrow.

Simple drift-diffusion modeling in Sentaurus TCAD accounts for most of the observed characteristics. Fig. 3.7 shows the measured leakage current (symbols) for devices with 30% (open symbols) and 40% (filled symbols) indium composition. The doping is used as a fitting parameter in the simulated leakage current (lines). Note that the zinc flux was not changed during the growth of the 30% and 40% indium samples, yet a small change in the doping appears to have occurred. This may be due to a change in the zinc incorporation for different indium flux. Increasing the zinc flux by a factor of five resulted in an increase in the doping concentration of a factor of three. The simple drift-diffusion model no longer accurately describes the observed leakage current, and is most likely due to the early onset of trap-assisted tunneling (TAT) resulting from the small bandgap and high doping level of the device.

3.3 InGaAs on InP

3.3.1 Growth

Heteroepitaxy of uniform arrays of InGaAs nanowires on InP substrate (Fig 3.8a,b) was achieved through a study of the effect of TMIn and TMGa partial pressures, V/III ratio, and growth temperature on nanowire morphology and composition. A temperature of 700° C and V/III ratio of 45 was used to grow the nanowires shown in Fig. 3.8a,b. Fig. 3.8c shows that the Ga composition in the gas phase (x_g) does not directly determine the composition in the solid phase (x_s), but is a function of both x_g and growth temperature (Fig. 3.8d). InGaAs with solid phase compositions from $x_s = 73\%$ to 39% were grown directly on InP substrate with no threading dislocations. The composition was determined by performing photoluminescence measurements on the nanowire arrays.

3.3.2 Electrical characterization

In order to determine the dominant component of the dark current at room temperature, temperature dependent current-voltage measurements were performed from 77° K to 350° K (Fig. 3.9a). Although there is only a weak bias dependence to the dark current above 2 V reverse bias, the dark current increases rapidly from 0 - 2 V reverse bias. This indicates a large saturation current, the source of which was determined using an Arrhenius plot to extract the activation energy (Fig. 3.9b). At 10 mV reverse bias, where the saturation current dominates, the activation energy is 284 meV. The likely source of this defect is phosphorus vacancies, which have been shown to have an activation energy of about 270 meV, and thermal degradation of the substrate. This is due to the high growth temperature (680° C) necessary for the verticle growth of InGaAs nanowires. The relatively low decomposition temperature of InP (380° C) makes high-temperature growth, even under TBP stabilization, unsuitable for high-performance electrical devices. This is



Figure 3.8 (a) Scanning electron micrograph (SEM) of uniform array of InGaAs nanowires grown on InP substrate. Scale bar: 15 μ m (b) Tilted SEM of as-grown InGaAs nanowires. Scale bar: 600 nm. Control of InGaAs composition is achieved through (c) TMGa and TMIn partial pressures and (d) growth temperature.

apparent when looking at the dark current characteristics for devices composed of nanowires grown with different mask hole diameters, as shown in Fig. 3.10. The leakage current increases dramatically as the junction area is increased, indicating the interface is severely degrading the device.



Figure 3.9 (a) Temperature dependent current measurements were performed from 77° K to 350° K. (b) The extracted activation energy of 284 meV suggests phosphorus vacancies in the substrate are likely the dominant source of dark current at room temperature.



Figure 3.10 Dark current measurements at room temperature for devices with different mask hole diameters (all grown on a single sample).

Light is focused within the nanopillar by coupling with surface plasmon resonances, resulting in a photocurrent peak at the resonant wavelength (Fig. 3.11a). The geometry of the self-aligned nanowire optical antenna (Fig. 3.11a Inset) can be controlled in order to shift the plasmonic resonance to the desired wavelength. A plasmonic resonance at the target wavelength of 1550 nm was achieved with an array pitch of 1.0 μ m, exposed height of 500 nm, and pillar diameter of 200 nm. The photocurrent was measured as a function of reverse bias (Fig. 3.11b). A peak responsivity >20 A/W is an indication of avalanche gain.



Figure 3.11 (**a**) Plasmonic resonances at 1500 nm and 1550 nm for pitches of 950 nm and 1000 nm, respectively, are responsible for the photocurrent peaks. Inset: self-aligned nanohole array acts as a plasmonic antenna. (**b**) Photocurrent and responsivity measurements clearly indicate avalanche gain.

3.4 Discussion

InGaAs NW-PDs on GaAs substrate displayed excellent electrical and optical characteristics, and can provide advantage over conventional planar photodetectors in certain regards, for example the ability to tune the indium composition to the desired target wavelength. Although not explored in

this work, another potential advantage is the reduced carrier transit time through the short nanowire devices, potentially allowing ultra-high speed operation. This would require a redesign of the device structure, most important of which is the need to grow nanowires on an undoped substrate. The InGaAs NW-PDs on InP substrate, on the other hand, have electrical characteristics that are far inferior to conventional InGaAs/InP photodetectors. The reason for this is simply that the amount of phosphoros-arsenic exchange at the substrate-nanowire interface is much larger than what occurs with planar epitaxy due to the much higher growth temperature required for nanowires. High temperature is an unavoidable consequence of nanowire growth, and renders the InGaAs/InP material system one of the few that show little to no promise for device applications. In addition to direct epitaxy on InP substrate, InP/InGaAs nanowire heteroepitaxy was also attempted, with little success, and is discussed in detail in the appendix.

4.1. Overview

The early theoretical work of McIntyre (25) and Emmons (26) showed that the excess noise and bandwidth of an avalanche photodiode is determined by the stochastic nature of the avalanche process and is a function of the ratio, k, of the electron, α , to hole, β , ionization coefficients. A key assumption of their work was that 1) a carrier experiences a spatially uniform electric field and 2) the multiplication region is much larger than the ionization path length, such that the excess noise at a given gain, M, is determined by bulk ionization coefficients. However, since their early work it has been shown that shrinking the volume of the avalanche region (27-31) and engineering sharp gradients in the electric field (32) lowers the effective ratio of the ionization coefficients, $k_{e\!f\!f}$, resulting in lower excess noise factors and higher gain-bandwidth products (33,34) beyond what is predicted by bulk values of the ionization coefficients. The improved statistics of the impact ionization process is attributed to the ionization path length of carriers having a narrower probability distribution due to dead space. The dead-space effect can dramatically reduce the excess noise (30), resulting in a k_{eff} that is much smaller than the intrinsic material k (28,35,36). Nanowires offer a path towards further miniaturizing the multiplication volume and exploiting the dead-space effect. Although nanowire-based APDs have been reported (37-41), all but one are single nanowire demonstrations having nanoscale active areas with extremely lossy free-space or optical fiber coupling, limiting their usefulness.

In this chapter, we provide the first excess noise measurements on nanowire (NW)-APDs at 1.06 μm with highly localized and physically separate optical absorption and multiplication



Figure 4.1 (a) Tilted SEM of as-grown InGaAs nanopillar array. Scale bar, 600 nm. **(b)**, Fabricated NOAAD with ground-signal-ground (GSG) contacts for high speed measurements. The signal contact is deposited directly on the BCB to electrically isolate it from the substrate. Scale bar, 80 μm. Inset: Tilted metal deposition results in a self-alligned nanohole array.

regions within a nanowire array. The noise measurement shows a significant reduction in excess noise compared to bulk and is the first exploitation of dead space effects utilizing a 3D electric field within a nanowire. We have also developed a novel modeling scheme for the analysis of avalanche multiplication process in the 3D electric field within a nanowire. Recursive dead-space multiplication theory has been generalized in 3D dimensions (3D-DSMT) to analyze our experimental data and has been found to be in good agreement.

4.2. Growth of InGaAs nanowires

InGaAs nanowires were grown on a n-doped GaAs (111)B substrate by selectrive area epitaxy using metal-organic chemical vapor deposition in an Emcore vertical-flow reactor at a pressure of 60 torr and temperature of 730°C. A passivation shell was subsequently grown *in situ* at 600°C. The primary precursers were trimethylindium, trimethylgallium, tertiarybutylarsine, and tertiarybutylphosphorus; the p-dopant was dimethylzinc. The V/III ratio for the InGaAs core and



Figure 4.2 (a), Measured dark current (black curve) and photocurrent (red curve) at room temperature of an APD with a 40 μ m X 40 μ m active area. The photocurrent was measured with a chopped light source and lock-in amplifier due to the high leakage current. **(b)**, Gain as a function of bias for increasing incident optical power. Gain saturation occurs at high optical power.

the InGaP shell were 43 and 26, respectively. The gas phase indium composition was 40% for the InGaAs and 70% for the InGaP. The InGaP passivation shell thickness was 10nm.

The lithographically defined patterned growth mask is systematically optimized in terms of array pitch in order to tune the enhanced optical absorption at a plasmonic resonance to the desired wavelength (19). The detector active area was 40 μ m × 40 μ m, corresponding to 1156 to 2809 nanopillars for a pitch of 1150 nm to 750 nm, respectively. Figure 4.1a shows a tilted (30°) scanning electron micrograph of the as-grown nanowire array. The fabricated device is shown in Figure 4.1b, and the inset shows the result of the tilted deposition: a self-aligned nanohole array which functions as a 3-dimensional plasmonic antenna. Ground-signal-ground (GSG) contacts were used for noise spectral density and high-speed measurements.

4.3. Electrical characterization

4.3.1 Photocurrent and gain

The room-temperature dark current and photocurrent as a function of bias measured from a typical device is shown in Figure 4.2a. A phase-sensitive measurement was used to distinguish photocurrent from dark current. It is important to accurately determine the primary photocurrent in order to avoid overestimating the gain, thereby underestimating the excess noise factor. In typical planar APDs the primary photocurrent is determined from the DC photocurrent vs. bias characteristics. There is a clear plateau of the photocurrent with increasing bias as a result of the electric field extending through the absorption region. This plateau, or punch-through, is usually identified as the primary photocurrent. However, in the NW-APD, with increasing bias the depletion region extends through a 3-dimensional spatial distribution of photogenerated carriers. As a result, it the primary photocurrent cannot be extracted from the DC photocurrent vs. bias



Figure 4.3 Gain as a function of incident optical power for increasing reverse bias. Gain saturation is clearly visible above 40 μ W incident power, with the effect becoming more prominent at higher bias.

characteristics. The primary photocurrent can be determined directly by measuring the photocurrent noise for increasing reverse bias until the measured noise begins to exceed the calculated shot noise. The photocurrent at a bias immediately before the photocurrent noise exceeds the calculated shot noise is taken as the primary photocurrent. The gain is calculated by normalizing the bias dependent photocurrent to the primary photocurrent, and reaches a peak value of M = 96, as shown in Fig. 4.2b. Also shown is the gain for increasing incident laser power (note that the laser source is a fs pulsed laser and the average power is given). As the incident laser power is increased, the NW-APD experiences gain saturation. In order to ensure gain saturation does not occur during the excess noise measurement, photocurrent measurements were performed at various incident optical powers. The gain is then plotted as a function of incident power at a bias of 4.7 V to 6.2 V (Fig. 4.3). As the bias is increased the gain saturation effect becomes more prominent at high optical power. Therefore, the optical power used for excess noise measurements was kept below 30 μ W.

4.3.2 Excess noise

In order to convert the measured power spectral density to current spectral density, the system impedance must be known. The impedance was measured as follows: The DC photocurrent, I_{DC} , of an InGaAs PIN photodiode was measured at a given incident laser power using a standard semiconductor parameter analyzer. The laser was then mechanically chopped at 5 kHz and the peak-to-peak power, P_{peak} , at 5 kHz was measured using the signal analyzer. Assuming the peak-to-peak current produced by the photodiode is equal to the DC photocurrent (which is reasonable, given the very low modulation frequency), then

$$I_{peak} = I_{DC} \tag{4.1}$$


Figure 4.4 Measured noise (symbols) of an InGaAs PIN photodiode along with the various noise sources: pre-amp, laser RIN, and shot noise (grey dashed lines). The total noise is shown in the red dashed line. Transimpedance gains of (**a**) 10^6 V/A and (**a**) 10^4 V/A were used to cover DC photocurrent noise measurements from 100 nA to 10 μ A.

and

$$P_{peak} = I_{peak}^2 R \tag{4.2}$$

where R includes the input impedance of the signal analyzer. Therefore,

$$R = P_{peak} / I_{peak}^2 \tag{4.3}$$

The noise measurement setup was then tested by measuring the noise power of an InGaAs PIN photodiode (at zero bias) by varying the incident laser power, shown in Fig. 4.4 for two different transimpedance gain settings (after 500 averages). The measured noise (symbols) was converted to current spectral density using the measured value of R. The theoretical bandwidth normalized shot noise is given by

$$i_{shot} = \left(2qI_{ph}\right)^{1/2} \tag{4.4}$$



Figure 4.5 Noise calculated by subtracting the pre-amp noise and the laser RIN from the total measured noise under illumination. The grey dashed line is the calculated shot noise.

where I_{ph} is the DC photocurrent. The laser RIN line is also plotted (calculated from manufacturer specifications). The pre-amp noise floor was measured. The red dashed line is the total noise calculated from the pre-amp noise floor, the shot noise, and the laser relative intensity noise (RIN). Subtracting the pre-amp noise and laser RIN from the measured noise gives the shot noise, shown in Fig. 4.5. By carefully accounting for all the noise sources in the measurement setup and measuring the system impedance, a very accurate measurement of shot noise can be performed. Since a PIN photodiode at zero bias was used for the calibration of the noise measurement setup, there is no uncertainty about the M = 1 reference point because there is no gain. The InGaAs PIN was then replaced by the nanowire APD to perform excess noise measurements.

To accurately determine unity gain photocurrent, noise spectral density measurements on the photocurrent were performed. Fig. 4.6 shows the noise measurement with increasing applied reverse bias. At low biases the noise of the NW-APD follows the expected shot noise up to $10 \,\mu$ A



Figure 4.6 Measured noise for increasing bias. The unity gain point is taken at the point immediately before the noise exceeds the calculated shot noise.

of photocurrent. Further increasing the bias results in an increase in the slope of the current dependence of the noise, indicating excess noise from the avalanche process has increased the noise above the shot noise level. The intersection of the fits to the shot noise and excess noise is then taken as the unity gain photocurrent, I_{pr} , as indicated in Fig. 4.6. The measured noise includes both noise from the dark current and photocurrent

$$i_{meas}^2 = i_{dark}^2 + i_{ph}^2 \tag{4.5}$$

The noise is measured under both dark and illuminated conditions to separate the two sources of noise. The photocurrent noise is given by

$$i_{ph}^2 = i_{meas}^2 - i_{dark}^2 = 2qI_{pr}FM^2$$
(4.6)

and thus, the measured excess noise factor is given by



Figure 4.7 Excess noise factor calculated from measured noise spectrum (symbols) along with theoretical predictions based on McIntyre's model (lines) for various values of k.

$$F = \frac{i_{ph}^2}{2qI_{pr}M^2} \tag{4.7}$$

A theoretical expression for the excess noise factor was derived by McIntyre (25), and is given by

$$F(M,k) = kM + \left(2 - \frac{1}{M}\right)(1-k)$$
(4.8)

The measured excess noise factor (symbols) and theoretical predictions based on Eq. 4.8 for various values of k are shown in Fig. 4.7. The best fit to the data occurs for k = 0.15, which is substantially lower than expected for bulk InGaAs. We investigate the source of this effect using 3-dimensional modeling in the next section.

4.5. 3D dead space multiplication theory

Although very large gain is achievable in the NW-APD, an APD's maximum *usable* gain is that which results in the optimum signal-to-noise ratio and is determined by the excess noise factor. Minimizing the excess noise is therefore of considerable interest and is an active area of research. A unique feature of NW-APD optical absorption is the localization of optical absorption to the exposed nanopillar volume, while the avalache region is located at the nanopillar-substrate interface. Since optical absorption near the multiplication region is dramatically reduced in the NW-APD, a reduction in the excess noise as compared to double-carrier multiplication in bulk InGaAs is expected. This effect was studied through detailed modeling and simulations. Although the recurrence theory for avalanche multiplication, including the statistics of gain and impulseresponse under non-uniform, static electric fields is well-known for 1D electric fields (30,42), both the magnitude and direction of the electric field in the NW-APD vary in space. This is in direct contrast to planar APDs, which assume an internal electric field that only varies along the axis of the device. Here, we introduce a generalization of the recurrence theory, 3D-DSMT, to account for a 3D electric field. The doping profile was calculated by fitting the modeled capacitancevoltage (CV) characteristics to the measured CV by adjusting the doping profile within the nanowire. The capacitance of a single nanowire was estimated by measuring the CV of the NW-APD as well as the CV of a dummy device (identical to the NW-APD, but without nanowires, fabricated on the same sample). The CV of the dummy device is independent of bias, since there is no contribution from junction capacitance from the nanowires. Since the voltage on the contact is equal to the voltage on the nanowires, we treat the system as two parallel capacitors and simply subtract the dummy capacitance from the capacitance of the NW-APD. Finally, we once again assume that the array of nanowires is connected in parallel and divide by the number of nanowires to get the capacitance of a single nanowire. The measured and simulated capacitance are shown in Fig. 4.8. Care has to be taken when extracting electric fields in nanostructures since the surrounding material plays a major role in fringing the electric field lines (43). A 3D electrostatic



Figure 4.8 Measured capacitance-voltage (CV) characteristics for unit cell of and the modeled CV used to extract the doping profile within a nanopillar. A 40 X 40 array of nanowires produced a capacitance well above the parasitic capacitance and the noise floor of the measurement system.

model of a single unit cell of the NW-APD is developed taking into account both the surrounding cyclotene dielectric polymer and a cathode geometry which accounts for the metal on top of the nanowire, on the sidewalls and on top of the cyclotene, shown in Fig. 4.9a. A 2D cut through the center of the nanowire, shown in Figure 4.9b, shows the electric field radiating out from the junction area. Note that the nanowire extends beyond the junction area due to radial overgrowth. The paths of electrons generated outside the multiplication region were numerically calculated to determine their position and energy upon entering the multiplication region (Figure 4.9c). The ionization parameters were taken from measured impact ionization rates (*44*).

The traditional recursive methods of studying the avalanche process within the multiplication region developed by Hayat et al., assume planar APDs where the direction of the internal electric field does not change spatially. That is, the derivations were performed under the



Figure 4.9 (a) Fitting and extraction of the experiment capacitance of the NW-APD with the 3D drift diffusion model allows the calculation of the electric field within a nanowire. The cyclotene polymer, included in the simulation, contributes to the fringing fields. (b) Electric field lines, drawn in black, show a field that radiates out from the junction area throughout the nanowire (the nanowire extends beyond the junction area due to radial overgrowth). (c) The electron trajectories through a nanowire are numerically calculated showing that electrons generated in the nanowire tip are funneled to the multiplication region by the 3D electric field.

assumption that the electric field was one-dimensional in nature. This theoretical model is known as dead space multiplication theory (DSMT). Since the electric field for a NW-APD has components in 3 orthogonal directions, it must be represented by a vector function that depends on the 3-dimensional position within the multiplication region: $\mathbf{E}(x, y, z)$. The 3D contact of the NW-APD and surrounding BCB dielectric was taken into account in the electrostatic model.

After determining all the possible paths of the carriers in the NW-APD 3-dimensional multiplication region, we apply a generalized 3D-DSMT to all the possible trajectories. Each of these potential paths has its own individual probability of occurring; that is, depending on the entrance position of a photocarrier to the multiplication region, an avalanche process occurs at a specific path. We calculated the mean gain and excess noise for each trajectory, triggered by an

Carrier	A (cm1)	B(V/cm)	m	Threshold Energy (eV)
Electrons	$1.80 imes 10^7$	$1.95 imes 10^6$	1	1.20
Holes	$2.56 imes10^7$	$2.20 imes10^6$	1	1.00

Table I: Ionization Parameters for InGaAs

electron injected at the beginning of the multiplication region. Since these electrons originate from photon absorption within the plasmonically enhanced nanowire, we can determine the entrance probability using photon absorption rates and the electric field within the absorption region. Then the average gain and overall excess noise factor are found by averaging over all possible paths.

The electron and hole saturation velocities are assumed as 6.7×10^6 cm/s. The ionization parameters for InGaAs are given in Table 1. Note that the ionization coefficients reported by Ng, et al., were tested as well but did not accurately predict the IV characteristics of our device and so the coefficients of Pearsall were used. Figure 4.10a shows the mean gain as a function of applied bias for the electron trajectories shown in Figure 4.9c. Since the gain reaches large values at a different bias voltage for each electron trajectory, it is not possible to calculate an average gain vs. bias curve. Nonetheless, by calculating the average *bias* at which the gain reaches 50, we find the calculated average bias of 6.9 V agrees very well with the measured bias of 6.8 V. The simulated excess noise factor is shown in Figure 4.10b (solid line), along with the measured excess noise factor (symbols) and the calculated excess noise factors using McIntyre's model (dotted lines). The excess noise calculated using 3D-DSMT is a weighted average based on the photogeneration profile. By modeling electron initiated multiplication and dead space effects, a good fit to the experimental data is achieved. The best fit to McIntyre's model occurs for $k_{\rm eff} = 0.15$, a significant reduction compared to bulk InGaAs, for which 0.33 < k < 0.65 for mixed carrier injection, while $0.19 < k_{\text{eff}} < 0.27$ has been reported for single carrier injection (45).



Figure 4.10 (a) The gain is calculated for each electron trajectory in Figure 3c and matches well with the measured gain (symbols). (b) Excess noise vs. Gain of the InGaAs NOAAD. The symbols show the measured excess noise factor and the solid line is calculated using 3D-DSMT. The dotted lines are calculated using McIntyre's theory for (from bottom to top) k = 0.05, 0.10, 0.15 and 0.20.

4.6. Temporal response

The ability to tightly confine optical absorption to the exposed nanopillar tips means that instead of following Beer's Law, there is a sharp cut-off in the optical absorption near the avalanche region, minimizing the transit time through the low-field drift region and potentially enabling ultra-high speed optoelectronics. Although the current device structure is not optimized for high speed operation (large contact capacitance, highly doped substrate), we nonetheless investigate the response time of the NW-APD. The temporal response was generated by illuminating the APD with a Coherent Ti-Sapphire laser with a 120-fs pulse width and 76-MHz repetition rate tuned to a 998-nm center wavelength. Transient pulse characteristics were measured with a microwave probe (Cascade ACP40-GSG-150) and a 50-GHz oscilloscope (Tektronix SD-32 sampling head). A microwave bias-T (Wiltron V250) was used to bias to the sample while



Figure 4.11 Temporal response of NW-APD measured with 50 GHz oscilloscope and coherent Ti-Saphire laser (998nm, 120 fs pulse, 76 MHz repetition rate). The incident *average* power was 70 μ W (peak power is 7.2 W).

passing the transient signal to the oscilloscope. The pulse response for a 70 μ W average power pulse is shown in Figure 4.11. Below 5 V reverse bias, the polarity of the pulse is actually reversed. This is likely due to an inability to collect the large number of carriers generated by the high power pulse before they recombine at the top contact at low bias, as this effect does not occur for lower power pulses.

In Figure 4.12a-d, the pulse response for average pulse powers of 7, 12, 42, and 70 μ W are shown. The rise time of 18 ps is unaffected by incident laser power or increasing bias, indicating the avalanche build-up time is not limiting the response time. On the other hand, the fall time decreases, ranging from 297 ps to 76 ps with increasing reverse bias, with a miniumum full width at half max of 51 ps. For the NW-APD, the capacitance monotonically decreases as the depletion region grows with increasing reverse bias until the parasitic contact capacitance of 250 fF is reached, resulting in a calculated RC-limited bandwidth of 2.8 GHz. The frequency response was



Figure 4.12 Temporal response of NW-APD for incident average powers of (a) 7 μ W, (b) 12 μ W, (c) 46 μ W, and (d) 70 μ W. The rise time of 18 ps is independent of incident laser power or bias. The fall time decreases from 297 ps to 76 ps with increasing reverse bias

calculated by taking the Fourier transform of the pulse response, using a fast Fourier transform (FFT) algorithm with zero padding and Hamming window to smooth the edges.

The frequency response is plotted in Figure 4.13a-d. The bandwidth increases with gain until a plateau is reached in the -3 dB bandwidth at 2.1 GHz. Note that this is a very high bandwidth given that this device was not designed for high speed operation. At the highest measured gain of M = 96, a gain-bandwidth product (GBP) is 201 GHz.



Figure 4.13 Frequency response of NW-APD for incident average powers of (a) 7 μ W, (b) 12 μ W, (c) 46 μ W, and (d) 70 μ W

4.7. Discussion

In summary, we have demonstrated a novel NW-APD architecture based on positioncontrolled arrays of III-V semiconductor nanopillars employing a self-aligned plasmonic optical antenna. The focusing of light near the exposed nanowire tip physically separates the absorption region from the multiplication region, favoring electron injection over hole injection and reducing the excess noise compared to bulk. The measured k_{eff} of 0.15 represents a substantial reduction in k_{eff} over bulk InGaAs and is the first reported excess noise measurement on a nanowire-based APD. The NW-APD reported here demonstrates it is possible to engineer optical absorption and electric fields within nanowires for favorable avalanche statistics. The NW-APD exhibit gain approaching 100 and a bandwidth of 2.1 GHz, for a gain-bandwidth product of over 200 GHz. We believe further optimization is possible by bringing the absorption region closer to the avalanche region, resulting in increased bandwidth with minimal effect on noise.

5.1. Overview

Avalanche photodetectors (APDs) have become the technology of choice for the most demanding photon detection applications, including time-resolved photoluminescence (46), laser rangefinders (47), time-of-flight 3D scanners (48), and light detection and ranging (LiDAR) (49). More recently, demand for high volume, low-cost LiDAR has seen a dramatic rise with the development and commercialization of autonomous vehicles (50). For many applications, silicon single photon avalanche diodes (SPADs) offer the best available performance in terms of dark count rate (DCR), photon detection efficiency (PDE), and timing jitter. However, in certain instances, e.g., quantum key distribution (51) and eye-safe LiDAR (52), it is advantageous to be able to detect light in the near-IR, where silicon SPADs fail to offer acceptable PDE (53). Initially, standard commercially available InGaAs-InP separate absorption-multiplication (SAM) APDs were tested in Geiger mode (54-56), but the DCR of these detectors was very high. Later, InGaAs-InP SPADs specifically designed for single photon detection emerged that took into account the much higher electric fields present in the avalanche region of a SPAD to reduce trap-assisted tunneling responsible for the high DCR (57,58). Although considerable progress has been made towards improving performance—it is now common to achieve 10-20% PDE with a DCR of only a few kHz (59,60) there still exists a fundamental limit to the maximum count rate.

As opposed to linear mode APDs, the count rate in a SPAD is not limited by avalanche build-up time, but rather by afterpulsing effects. During an avalanche event, a large current flows through the semiconductor and fills the empty traps. The avalanche is self-sustaining and must be quenched. The simplest approach is to passively quench the avalanche using a resistor in series with the SPAD. When a large current flows through the resistor, the increased potential drop across the resistor reduces the potential across the SPAD below the breakdown voltage and terminates the avalanche event. The trapped carriers are then released at a rate determined by the detrapping lifetime. The SPAD is then biased above the breakdown voltage while the number of trapped carriers being released is still significant, and an increase in the DCR is observed. The most obvious solution to this problem is to reduce the material defect density to a concentration equivalent to silicon. However the task of reducing the defect density in III-V semiconductors remains a difficult challenge. As a result, other techniques have been employed to mitigate the effects of afterpulsing.

The most commonly used approach to reducing afterpulsing is to *actively* quench the SPAD using external electronics. After an avalanche event, the bias is reduced below the breakdown voltage for a period of time, known as the *dead time*, in order to allow the detrapping of carriers without initiating an avalanche pulse. The time period required is determined experimentally by varying the dead time and measuring the DCR until a minimum is reached. Although this technique is very effective at eliminating afterpulsing effects, the dead time limits the counting rate to about 100 kHz. Another approach is to limit the current flow through the SPAD to reduce the number of traps filled by an avalanche event. This can be achieved by using ultra-short gated bias (e.g. overbias the SPAD for a period of less than 1 ns). However, sophisticated electronics for cancelling large transient pulses induced by fast gated bias, such as sinusoidal gating (*61*) and self-differencing techniques (*62*), are necessary. And this largely limits its usefulness in applications requiring compact SPAD arrays (e.g. 3D imaging using SPAD array). In addition, this fast gate approach requires very precise synchronization between the light source and gated bias in order to

maximise the detection efficiency. This makes it unsuitable for applications without a known photon arrival time (e.g. LiDAR and time-resolved fluorescence spectroscopy) in which free-running operation is needed.

The nanowire platform was used as an APD by Hayden *et al.* for the first time in 2006 (37). Crossed Si-CdS nanowires were used to form heterojunction p-n diodes. Later, nanowire APDs with different materials (Si (63-65), GaAs (38) and InP (39)) and structures (core-shell (38), p-n (39) and p-i-n (63-65)) were demonstrated with very high avalanche gain. However, these are all single nanowire photodetectors which leads to extremely low optical coupling efficiency. More recently, APDs with plasmonic antenna structures using nanowire arrays have been demonstrated with enhanced absorption (41,66). Linear mode photon detection was reported in a single InAsP quantum dot embedded in the avalanche region of a single InP nanowire (39), however the large bandgap absorber limits photon detection to the visible spectrum. Despite these advances, there are no reports on nanowire APDs operated above their breakdown voltage (i.e. Geiger mode-APD or SPAD) or near-IR photon detection.

In this chapter, we present a vertical nanowire array separate absorption-chargemultiplication APD operating in Geiger mode. We adopt an approach for reducing afterpulsing based on reducing the *volume* of semiconductor material exposed to the high current flow of an avalanche event. Vertical arrays of nanowires with an InGaAs absorption layer and GaAs avalanche layer comprise the active area of the nanowire (NW)-SPAD. The dark current of this device at 95% breakdown voltage is below the noise floor of 100 fA of the measurement electronics. Assuming that the dark current is 100 fA, then about 650,000 electrons travel through the SPAD per second. Since an avalanche event reduces the bias below the breakdown voltage in under 1 ns, in order for two unrelated carriers to simultaneously initiate an avalanche, they must be generated within a 1 ns window. Since only 6.5×10^{-4} electrons travel through the entire array of 4,444 nanowires per nanosecond, it is reasonable to assume that the majority of avalanche events are caused by single carriers, and hence completely contained within a single nanowire. Given that the ratio of the volume of a single nanowire to a bulk SPAD of equal effective volume is extremely small, a dramatic reduction in afterpulsing probability is expected.

5.2. Growth of nanowire SPADs

Although axial heterostructure formation in nanowires is routinely achieved with a variety of materials using catalyzed growth techniques, it remains a challenging problem for catalyst-free nanowire epitaxy. Several examples of core-shell InGaAs-GaAs heteroepitaxy exist in the literature (67–69), but reports on axial heteroepitaxy are limited to quantum dot formation (70), low indium composition (71), or thin InGaAs layers (72). The nanowire SPAD design requires at least a 500 nm InGaAs axial layer to maximize absorption, and thus a different approach was necessary. The commonly used gallium precursor, trimethylgallium, was replaced with triethylgallium in order to take advantage of the enhanced vertical growth rate observed in selective-area epitaxy using large-area openings (73).

Nanowires were grown on n-doped GaAs (111)B substrate by catalyst-free selectrive-area epitaxy using MOCVD in an Emcore vertical-flow reactor at a pressure of 60 torr. Source materials for indium, gallium, arsenic, phosphorus, and zinc were trimethylindium (TMIn), triethylgallium (TEGa), tertiarybutylarsine (TBAs), tertiarybutylphosphine (TBP), and diethylzinc (DEZn), respectively. Before loading the sample, it is etched in a H2O:HF (200:1) solution for 45 seconds, rinsed with deionized water, dried with N₂, then immediately transferred to the MOCVD. The temperature is ramped to 680° C and held for 10 minutes under TBAs overpressure to remove

native oxide from the substrate surface. A 400 nm nominally undoped GaAs avlanche layer was grown in 20 minutes at 680° C with V/III ratio of 40. A 300 nm p-GaAs layer was grown in 9 minutes with [DEZn]/[TEGa] = 0.1. A 400 nm nominally undoped InGaAs absorption layer was grown in 8 minutes with [TMIn]/([TMIn]+[TEGa]) = 0.4. A 100 nm p-InGaAs contact layer was grown in 2 minutes with [DEZn]/([TMIn]+[TEGa]) = 0.5. The temperature was ramped down to 590° C under TBAs overpressure and allowed to stabalize for 2 minutes. The TBAs is shut off, the growth chamber is cleared under H₂ for 15 seconds, followed by TBP flow for 15 seconds. Finally, a nominally undoped 15 nm InGaP shell was grown in 2 minutes with [TMIn]/([TMIn]+[TEGa]) = 0.4. The temperature is ramped down under TBP overpressure. The final nanowire diameter and height were 150 nm and 1.2 μ m, respectively.

The device structure, shown in Fig. 5.1A, was optimized using 3D simulations in Sentaurus TCAD to find the thinnest device layers that still gave acceptable device characteristics. The motivation behind this strategy was to avoid the increase in the InGaAs lateral growth rate that occurs as the height of the nanowires increases. Doping of the InGaP passivation shell resulted in a low series resistance electrical contact, but was found to create shunt paths that significantly increase the leakage current under reverse bias. Therefore, an undoped InGaP shell was used and a 100 nm zinc doped InGaAs layer was introduced.



Fig. 5.1 (**A**) SACM-APD structure in a nanowire with InGaP passivation shell, (**B**) Tilted SEM images of nanowire growth after each layer.



Figure 5.2 (A) Nanowires with a 500 nm InGaAs layer are vertical and have the same diameter as the GaAs layer underneath, indicating no radial overgrowth has occurred.
(B) Nanowires with a 700 nm InGaAs layer are mostly vertical (Box 2), but the final diameter is greater than the GaAs layer below, and several nanowires are curved due to strain on the sidewalls (Box 3).



Figure 5.3 (**A**) STEM and EDX of single nanowire before growth of InGaP passivation shell. (**B**) Room temperature photoluminescence of nanowire array with complete device structure.

Device layer thicknesses were calibrated by measuring the height of the nanowires after the addition of each layer using SEM, as shown in Fig. 5.1B. There was no increase in the diameter of the nanowires from the first GaAs layer to the final InGaAs layer, within the measurement error of the SEM (Fig. 5.2A). Growth of axial InGaAs on GaAs is sensitive to growth temperature, V/III ratio, indium composition, and layer thickness. No attempt at a complete study of the parameter space was performed. Instead, the maximum axial InGaAs layer thickness was found for a given set of growth conditions. Radial overgrowth of InGaAs on the GaAs layer was observed by SEM as an increase in the nanowire diameter and bending of the nanowires due to strain on the sidewalls caused by lattice-mismatched heterointerfaces, shown in Fig. 5.2B, for nanowires that do not grow a uniform shell.

Scanning transmission electron microscopy (STEM) imaging (Fig. 5.3A) clearly shows two distinct materials, with the bright region corresponding to the InGaAS. An energy dispersive x-ray (EDX) line scan along the length of the nanowire reveals a graded In:Ga interface which has also been observed during the growth of InGaAs-GaAs heterostructures using TMGa and is



Figure 5.4 Effect of contact layer on dark current of devices (**A**) without a contact layer and (**B**) with a contact layer.

attributed to indium segregation as the growth front progresses (72). Although this graded interface is not grown intentionally, it is in fact a useful feature for preventing carrier accumulation at the heterointerface and is an intentional design feature of modern SPADs. The indium fraction of 27% is supported by the peak photoluminescence emission at 1.16 μ m (Fig. 5.3B) which suggests an indium fraction of 24%. The discrepancy is likely due to the existence of wurtzite crystal phase within InGaAs nanowires, which is known to increase the bandgap by a few 10's of meV.

5.3. Electrical characterization

The effect of the p-InGaAs contact layer were investigating by comparing the electrical characteristics of devices without (device A) and with the contact layer (device B). The total thickness of the InGaAs layer was kept the same for both devices, i.e., 500 nm i-InGaAs = 400 nm i-InGaAs + 100 nm p-InGaAs. The dark current measured at 300 K is shown for device A in Fig. 5.4A and device B in Fig. 5.4B. Although the original intent was to create a low-resistance Ohmic contact, the result was a dramatic reduction in the leakage current by over three orders of magnitude. After annealing, there is a reduction of the series resistance in device A, while no



Figure 5.5 Device uniformity determined by looking at dark current for 10 randomly selected devices on the sample.



Figure 5.6 (**A**) Temperature dependent leakage current, and (**B**) Arrhenius plot of the activation energy for nanowire devices composed of GaAs p-n diodes, InGaAs p-n diodes, and InGaAs-GaAs SACM-APDs.

change is observed in device B. We see a large reduction in the leakage current in both devices after annealing, although it is not understood why this occurs.

There are 50 individual single-pixel SPADs fabricated on a single sample. All 50 devices were "active", and no significant variation in electrical characteristics were observed. Fig. 5.5



Fig. 5.7 Repeated DC voltage sweeps on a single NW-SPAD at 77 K. The breakdown voltage shifted randomly between -17 V and -22 V.

shows the dark current at room temperature for 10 devices selected at random. A single device showed a higher than expected leakage current.

The temperature dependence of the leakage current is shown in Fig. 5.6A. Below 175 K the leakage current is entirely below the system noise floor and is not shown, however, the forward bias current was above the noise floor and recorded. The activation energy of the NW-SPAD was compared to simple nanowire p-n junction diodes at low reverse bias in Fig. 5.6B. The activation energy of the NW-SPAD is identical to that of the GaAs nanowire p-n junction, indicating that the depletion region in the NW-SPAD is contained entirely within the GaAs avalanche layer, as designed. The saturation current at temperatures below the system noise floor was estimated by fitting the forward bias current with the Shockley equation.

Current-voltage characteristics were measured under vacuum at 77 K. Fig. 5.7 shows the result of several repeated measurements on a single NW-SPAD. Immediately apparent is the variation of the breakdown voltage from one measurement to the next. Two features of this



Figure 5.8. Repeated dark current measurements at 200 K. (**A**) The breakdown voltage based on the first measurement is 18.1 V. (**B**) The second measurement is taken within a few seconds of the first. (**C**) The third measurement is take five minutes after the second measurement. The breakdown voltage has shifted slightly to 17.8 V.

behavior are important to note: 1) the breakdown voltage is varying randomly (*i.e.*, it is not monotonically increasing or decreasing), and 2) the electrical characteristics of the NW-SPAD are not degrading, as has been observed after avalanche breakdown of nanowire APDs (*39*). The random variation in the breakdown voltage is a direct result of the extremely low dark current at the breakdown voltage. Although the dark current is below the noise floor of the measurement equipment, from the temperature dependence of the dark current we estimate a dark current of ~ 1 fA at breakdown. During the voltage sweep, about 6 electrons flow through the NW-SPAD during each voltage step lasting 1 ms. Of these 6 electrons, the majority are expected to originate from the surface of the nanowire—due to the very high surface-to-volume ratio—and do not initiate breakdown (*74*). Therefore, it is very likely that the probability of an electron originating from the bulk of the nanowire and initiating breakdown during a given voltage step is less than one, leading



Figure 5.9 The breakdown voltage is measured at 77 K and 200 K. A temperature coefficient of breakdown of 8.1 mV/K is calculated and used to estimate the breakdown voltage at any temperature. Circles are reported in (76), filled squares are measured NW-SPAD, empty squares are calculated.

to the observed random variation in the breakdown voltage. This effect has been reported in extremely small volume silicon APDs as well (75).

At high temperature (~200 K), the NW-SPADs become unstable. Fig. 5.8 shows the result of three consecutive measurements on the same device. The second measurement is taken within a few seconds of the first, and exhibits resistor-like characteristics. However, after five minutes, a third measurement reveals the device has regained its diode characteristics. This reversible process suggests this is due to overheating of the device. The failure of the device prohibited the characterization at higher temperatures, thus all SPAD characterization was performed form 77 – 125 K. This issue may be addressed in future work by replacing the BCB with a dielectric with higher thermal conductivity to allow better heat dissipation. For example, SiNx has a thermal conductivity of up to 33 $Wm^{-1}K^{-1}$, compared to BCB, which has a thermal conductivity of 0.29

Wm⁻¹K⁻¹. The factor of 100 increase in the thermal conductivity of the dielectric surrounding the nanowires should allow a significant increase in the maximum operating temperature.

The breakdown voltage at low temperature varies randomly due the extremely low dark current, making it difficult to accurately determine the breakdown voltage. At 77 K, the breakdown voltage was chosen at the lowest voltage where it occurred after multiple measurements. At 200 K, the breakdown voltage did not vary significantly. Using the breakdown voltage at these two temperatures, the temperature coefficient of breakdown voltage is calculated and used to estimate the breakdown voltage at 100 K and 125 K. Fig. 5.9 shows the measured (filled squares) and the calculated (empty squares) breakdown voltage. Also shown is the measured breakdown voltage for bulk GaAs APDs (circles) with 100nm and 1 µm wide avalanche layers taken from reference (76).

5.4. SPAD characterization

5.4.1 Dark count rate and photon count rate

The NW-SPAD is passively quenched with a 1 M Ω resistor and operated in free-running mode, *i.e.*, no gating or dead time is used, as shown in Fig. 5.10A. This is the simplest and most desirable configuration for photon counting as no active quenching electronics are required and photons can be detected as they arrive, rather than only during gated periods. Fig. 5.10B shows the



Fig. 5.10 (**A**) Configuration of free-running measurement setup for dark counts and photon counts. Passive quenching is accomplished with a 1 M Ω resistor in series with the SPAD. (**B**) Pulse shape of dark carrier initiated avalanche events for increasing DC bias.



Fig. 5.11 (**A**) Pulses under dark conditions arrive at a rate of 6 Hz. (**B**) Pulses under CW illumination arrive at a rate of 8 MHz. Note that the pulses occur much more frequently under illumination and thus the time scale is modified for clarity, (**C**) Close-up view of three consecutive pulses with 40 ns between pulses indicating a maximum count rate of 25 MHz.

pulse shapes at different applied biases for dark carrier initiated avalanche events. Note that both the pulse amplitude *and* the pulse width increase as the applied bias is increased. The increase in pulse width is due to a sustained avalanche caused by the high electric field (77), but does not negatively affect SPAD performance except for a slight decrease in the maximum count rate. A real-time sweep of the NW-SPAD at a reverse bias of 29 V is shown in Fig. 5.11A. A total of 28 pulses are measured during the entire 10 second sweep, corresponding to a DCR of 2.8 Hz. To place this in perspective, note that commercial InGaAs/InP SPADs typically achieve a DCR of 1-2 kHz at this temperature in *gated mode*, as opposed to the free-running mode used in this work.



Figure 5.12 Start table legends with a title (short description of the table). Format tables using the Word Table commands and structures. Do not use spaces or tabs to create tables.

Next, real-time sweep is measured with a continuous-wave 1060 nm incident light source on the NW-SPAD, shown in Fig. 5.11B. A total of 31 photon initiated pulses are measured during a 4 μ s sweep, corresponding to a photon count rate of 7.8 MHz. Close examination of the pulse separation, shown in Fig. 5.11C, reveals that photons can be detected a minimum of 40 ns apart, corresponding to a maximum photon count rate of 25 MHz. Commercial InGaAs/InP SPADs are limited to counting rates up to 100 kHz as a direct result of the dead time necessary to suppress after-pulsing.

The DCR is usually presented as a function of the *excess bias*, i.e., the bias above the breakdown voltage. However, in this case it is difficult to determine the breakdown voltage at 77 K due to the random location of the breakdown voltage after successive DC sweeps. We take the lowest voltage at which breakdown occurs, 17 V, as the breakdown voltage at 77 K. At 200 K, the generation current increases and as a result the breakdown voltage variation is much smaller. The



Figure 5.13 Real-time sweeps lasting 100 μ s after the primary dark pulse at increasing overbias. A total of fifty sweeps are included in each plot at each overbias. No afterpulsing is observed beyond 2 μ s after the primary pulse.

temperature coefficient of breakdown is estimated to be 8.1 mV/K and is used to estimate the breakdown voltage at 100 K and 125 K and compared to values reported for planar GaAs (76) to ensure reasonableness. Fig. 5.12 shows the DCR from 77 – 125 K as a function of excess bias, V_E . There is no clear temperature dependence in this temperature range, indicating the source of the dark current is likely due to trap-assisted tunneling. Given that the GaAs avalanche layer is only 400 nm wide, this is not surprising.

5.4.2 Afterpulsing probability

The effect of afterpulsing can be observed by using an actively quenched SPAD and measuring the dependence of the DCR on the dead time. Since we operate our NW-SPAD in freerunning mode, there is no active quenching and no means to control the dead time. However, afterpulsing occurs within the first few microseconds of a dark pulse. Therefore, by looking at the time spacing between pulses in free-running mode, we can determine whether a pulse was caused by a



Figure 5.14 (**A**) Real-time sweeps spanning 2 μ s at various applied overbiases. Afterpulsing begins to appear at 10 V overbias. (**B**) The maximum apfterpulse probability of 23% occurs at 12 V overbias.

standard Shockley-Read-Hall process, or by carrier detrapping. We assume that if two pulses are greater than 100 µs apart, then the second pulse is not correlated to the first pulse. Conversely, if two pulses are less than 100 µs apart, then the second pulse is assumed to be an afterpulse. Since the average time between dark pulses is greater than 50 ms, it is highly unlikely two uncorrelated pulses will be found within 100 µs of each other. We measured fifty dark pulses at each applied bias and found no secondary pulses occurred beyond 2 µs, up to 100 µs, shown in Fig. 5.13. Within a 2 µs time window, however, secondary pulses are observed as the excess bias is increased, shown in Fig. 5.14A, where the primary pulse is located at t = 0. At $V_{OB} = 9$ V, there are zero secondary pulses out of fifty measured primary pulses, at $V_E = 10$ V, there is one secondary pulse, at $V_E = 11$ V there are five secondary pulses, and at $V_E = 11$ V, there are 15 secondary pulses. Using simple frequentist statistics, we estimate the afterpulse probability, p, by

$$p = N/(N+50),$$
 (5.1)

where *N* is the number of secondary pulses (Fig. 5.14B). Note that a secondary pulse can cause its own afterpulse, and so must be counted as a new primary pulse and added to the fifty original primary pulses in the denominator. Two important conclusions are drawn from these data: 1) the afterpulse probability is significantly lower than bulk SPADs operating in free running mode, where the afterpulse probability is unity (78), and 2) even at the highest applied bias, the afterpulsing terminates after only 1.5 μ s. Furthermore, as the temperature is increased, the detrapping lifetime decreases (*52*), and so the afterpulsing will terminate after an even shorter time period. This opens the possibility of using sub-microsecond dead-times in an actively quenched operating mode, allowing megahertz count rates with a nearly zero afterpulse probability (at the expense of increased circuit complexity).

5.4.3 Timing jitter

The timing jitter of a SPAD is an important performance metric, especially for timing applications such as LiDAR. The measured timing jitter is a convolution of the timing jitter of each individual element in the measurement setup. Assuming the SPAD, laser, oscilloscope, and amplifier have Gaussian timing distributions, the total timing jitter is given by

$$\tau^{2} = \tau_{SPAD}^{2} + \tau_{laser}^{2} + \tau_{osc}^{2} + \tau_{amp}^{2}$$
(5.2)

The total timing jitter is measured, and the timing jitter of the oscilloscope is known from the equipment specifications, however the remaining terms in Eq. 1 are unknown. Therefore, we first



Figure 5.15 Experimental histograms obtained by measuring the timing distribution of a pulsed voltage source with a known timing jitter of 70 ps (top), and the NW-SPAD with unknown timing jitter (bottom).

replace the SPAD with a pulsed voltage source with a known timing jitter (from equipment specifications) such that

$$\tau^{2} = \tau_{pulse}^{2} + \tau_{osc}^{2} + \tau_{amp}^{2}$$
(5.3)

Fig. 5.15 shows the timing distribution measurements in each case. Using a pulsed voltage source, a timing jitter of 283 ps is measured. Since $\tau_{osc} = 50$ ps and $\tau_{pulse} = 20$ ps, we find $\tau_{amp} =$ 278 ps. Replacing the pulsed voltage source with the NW-SPAD illuminated by the pulsed laser, we measure a timing jitter of 285 ps, from which we estimate $\tau_{SPAD}^2 + \tau_{laser}^2 = 38^2$ ps. Although we don't know the timing jitter of the laser, we know it is non-zero and we conclude that the timing jitter of the SPAD is < 38 ps. We should note that because the timing jitter of the amplifier is large compared to the rest of the components, the estimate presented here should not be considered precise.

5.5. Discussion

The purpose of this work is to show that the nanowire platform can provide certain SPAD performance improvements, namely a reduction in DCR and after-pulsing probability. The reduction in DCR is accomplished through the use of a gallium rich absorber to increase the bandgap and through a reduction of the fill factor to reduce the bulk volume. Although this eliminates applications at telecom wavelengths, it still allows detection at the technologically relevant wavelength of 1064 nm. The reduction in after-pulsing probability is accomplished by confining the avalanche current to the volume of a single nanowire, limiting the number of traps filled by the large current flow. We showed both extremely low DCR < 10 Hz, and significantly reduced after-pulsing for a range of applied biases. The lack of any significant after-pulsing allows operation in free-running mode, which eliminates the dead time limiting counting rates in commercial InGaAs/InP SPADs. We measure a photon count rate of nearly 8 MHz, and estimate the maximum count rate to be 25 MHz based on pulse separation. Although this performance is impressive, there are several challenges that must be addressed in order to make this a viable commercial technology.

First, although the photon detection efficiency (PDE) was not measured, it is likely very low compared to commercial technology. There main reason for this is that the plasmonic structure was not optimized for maximum absorption at 1064 nm. It is a simple matter to address, as the tuning of the plasmonic resonance to a particular wavelength has already been demonstrated, with a peak responsivity of 0.28 A/W at 1100 nm (2). Although this is less than half the responsivity of

a planar InGaAs detector (~0.7 A/W), the signal-to-noise ratio (SNR) of a SPAD depends on both the PDE *and* the DCR, and is given by

$$SNR = \frac{S}{\sqrt{S+N}} = \frac{PDE \cdot \Phi_S \cdot t_{int}}{\sqrt{PDE \cdot \Phi_S \cdot t_{int} + DCR \cdot t_{int}}}$$
(5.4)

where Φ_S is the signal photon rate and t_{int} is the integration time. The PDE differs from the quantum efficiency in that a photo-generated carrier initiates an avalanche pulse with a probability less than unity, an so

$$PDE = \eta(\lambda)\varepsilon(V) \tag{5.5}$$

where $\eta(\lambda)$ is the quantum efficiency at a given wavelength and $\varepsilon(V)$ is the avalanche initiation probability, which increases for increasing excess bias. Consider, for example, a planar SPAD with DCR = 2 kHz, $\eta = 0.7$, and $\varepsilon = 0.3$. For a photon rate of $\Phi_S = 1$ kHz, we have SNR = 4.5 (for a 1 second integration time). In order to achieve equivalent SNR with the NW-SPAD with DCR = 10 Hz, we only need $\eta = 0.1$, a factor of seven lower than the bulk SPAD. Thus, it is likely that a overall *improvement* in SNR is easily achievable by proper tuning of the surface plasmon resonance to the target wavelength.

The second major issue that must be addressed is the maximum operating temperature, which was 150 K for the NW-SPADs in this work. Above this temperature the devices quickly degraded after several measurements. We believe this is due to an increase in the current flow originating from the surface of the nanowires. Although the NW-SPADs are passivated with an InGaP shell, a combination of InGaP and cyclotene (BCB) passivation provides the best results when the depletion region is entirely confined beneath the BCB (79). In the NW_SPAD, the

depletion region must extend past the surface of the BCB through the absorber that is exposed to air, leading to an increase in surface leakage current. A possible solution is to apply a second layer of BCB after device fabrication to passivate the exposed portion of the nanowires, or chemical passivation with ammonium sulfide followed by encapsulation with SiO_x (80).
6.1. Overview

Semiconductor nanowires have become an increasingly important class of materials for novel photonic and nano-electronic devices. The field has matured to a stage where the growth of most material systems has been demonstrated using either Au-catalyzed, self-catalyzed, or catalyst-free growth techniques. Among the semiconductor nanowire material systems, the antimonides are of particular interest because of properties such as high carrier mobility and narrow bandgaps. The ternary material $InAs_{1-x}Sb_x$, in fact, has the narrowest bandgap of all the III-V semiconductors, for roughly 60% antimony, making it an ideal material for mid- and long-wavelength infrared photodetectors.

Growth of InAsSb nanowires has been reported using Au-catalyzed, self-catalyzed, and catalyst-free growth techniques. Au-catalyzed growth of III-Sb nanowires has shown promise and is the most mature growth technique to date, with studies on antimony incorporation (*81*), crystal phase evolution(*82*), and hetero-structure formation (*82,83*) available in the literature. Furthermore, the first reported nanowire-based mid-wavelength infrared photodetector (*84*) is based on Au-catalyzed growth. For monolithic integration of InAsSb on silicon, a Au-free growth mode is desirable to ensure compatibility with standard CMOS processing. Both self-catalyzed (*85–88*) and catalyst-free (*89*) growth of InAsSb on silicon have been demonstrated using both molecular beam epitaxy and MOCVD. While highly uniform nanowires have been achieved for many of the III-V material systems using self-catalyzed growth (*90–92*), the same level of uniformity has not been shown for InAsSb nanowires.

In order to advance from proof-of-concept to competitive technology, substantial improvements in material quality are required. Catalyst-free selective-area metal-organic chemical vapor deposition (SA-MOCVD) has proven to be a robust technique for the growth of high quality nanowires, but to date no data on InAsSb SA-MOCVD nanowire growth has been published. In this chapter, we present InAsSb nanowires grown by catalyst-free SA-MOCVD. We achieve highly uniform arrays of InAsSb nanowires free of parasitic growth and obtain strong mid-infrared photoluminescence (PL) from the nanowires. The peak energy of the PL as a function of temperature is used to determine the bandgap of the nanowires, and the rate of the shift is examined to determine the type of transitions responsible for the emission. The results presented here lay the groundwork for developing high-performance InAsSb nanowire-based infrared photodetectors and nanoelectronic devices.

6.2. Growth of InAsSb nanowires

InAs_{1-x}Sb_x nanowires are grown on InAs (111)B substrates via SA-MOCVD. A 20 nm SiO₂ mask is patterned with nano-hole arrays using e-beam lithography followed by reactive ion etching, with the hole size and pitch varying from 100 to 160 nm and 600 to 900 nm, respectively. Nanopillar growth is carried out in a low-pressure vertical MOCVD reactor at 0.1 atm using trimethylindium (TMIn), tertiarybutylarsine (TBAs), and trisdimethylaminoantimony (TDMASb) as source materials. The temperature is ramped to 550° C under TBAs over-pressure and held for 8 minutes to remove native oxide from the substrate. The temperature is then ramped to the growth temperature and the TMIn and TDMASb are introduced to initiate InAsSb growth. The InAsSb growth temperature was varied from 590 to 515° C in 25° C increments. The V/III ratio was fixed at 2.05 and the gas phase TDMASb composition ($x_{\nu} = [TDMASb]/([TDMASb]+[TBAs])$) was varied from $x_{\nu} = 0.15$ to 0.6. Growth was terminated by shutting off the TMIn and ramping down

the temperature under TBAs and TDMASb over-pressure until the temperature dropped below 200° C. A reference InAs sample was grown at a temperature of 590° C and V/III ratio of 8.

Nanowire morphology, including diameter, height, and parasitic growth, was studied using a Hitachi S-4700 scanning electron microscope (SEM). Transmission electron microscopy (TEM) was performed using STEM Titan (FEI) operating at an accelerating voltage of 300 kV. Solid phase Sb composition, *x*, was estimated using energy dispersive x-ray spectroscopy (EDX) on the Titan. TEM samples were prepared by exfoliation of nanowires and deposition onto carbon film supported TEM grids. Low temperature (77K) PL measurements were performed using Fourier transform infrared spectroscopy. The nanowire arrays were pumped by a 671nm diode laser at 5 W/cm² of incident power and the emission was detected by an InSb photodetector cooled to 77K. All beam paths were nitrogen purged to eliminate atmospheric gas absorption.

Epitaxial growth of the III-Sb family of semiconductors is notoriously difficult. The low equilibrium vapor pressure of antimony (P_{Sb}) at growth temperatures can easily lead to condensation of antimony on the substrate if the thermodynamics are not carefully controlled. This is not a desirable property for a group V element as it imposes a strict restriction on the usable range of V/III ratios. In contrast, the equilibrium vapor pressure of arsenic and phosphorus is much higher than partial pressures used for the growth of III-As and III-P family of semiconductors. Thus, arsenic or phosphorus condensation is not encountered, even at V/III ratios exceeding 100. We find that InAsSb nanowires prefer to grow at a V/III ratio of 2 or greater; below that the vertical growth rate is reduced and there is significant lateral overgrowth and non-uniformity. However, at a V/III ratio of 2, the excess antimony tends to condense on the growth mask, negatively affecting nanowire growth. The solution to these seemingly mutually exclusive requirements is to maintain a very low antimony partial pressure, p_{sb}^p , either through appropriate choice of the precursor flow rates or growth chamber pressure For this study, the total pressure was fixed at 0.1 atm and the TDMASb flow rates were minimized. The limiting factor for our experiments is the minimum TBAs molar flow rate achievable with our MOCVD system, which determines the minimum TDMASb molar flow rates we can use to attain the desired antimony composition in the vapor phase, x_v . Thus, we keep the TBAs partial pressure fixed at the minimum value, $[TBAs]_{min} = 6.26 \times 10^{-5}$ atm, and use TDMASb partial pressures of $[TDMASb] = 1.10 \times 10^{-5}$, 2.65×10^{-5} , 5.18×10^{-5} , and 9.38×10^{-5} atm, to get $x_{Sb}^v = 0.15$, 0.30, 0.45, and 0.60, respectively. The TMIn partial pressure is adjusted to keep the V/III ratio fixed.

In order to determine the range of tolerable growth temperatures, we compare p_{Sb}^p used during nanowire growth to P_{Sb} . For growth conditions where $p_{Sb}^p < P_{Sb}$, a V/III ratio of 2 may be used without antimony condensation. From this simple analysis, it appears the growth temperature must approach 590° C in order to have $x_v = 0.60$ while simultaneously avoiding antimony condensation. Interestingly, we observe that within the nanowire array we can significantly exceed P_{Sb} , if the array pitch is sufficiently small, and observe no antimony condensation. This can be explained by a reduction in p_{Sb}^{p} in the vicinity of the nanowire arrays relative to the mask area caused by antimony adsorption in the nanowires. If we define the ratio $R = p_{Sb}^p / P_{sb}$, we find empirically that for a 600 nm array pitch, antimony condensation within the nanowire arrays begins for R > 8. For larger pitches, R is smaller. We therefore accepted antimony condensation (which appears as a bluish-grey film to the naked eye) on the mask away from the nanowire arrays and performed many growths with R reaching values up to 8. In addition to array pitch, the mask hole diameter also plays an important role in the growth. With increasing hole size, array uniformity decreases and "pancake"-like structures begin to replace nanowire growth. Thus, all characterization was performed on the nanowires grown on arrays with 100 nm holes and 600 nm



Figure 6.1 Tilted SEM (30°) of as-grown $InAs_{1-x}Sb_x$ nanowires at 590°C for x = 0.15 (a), 0.30 (b), 0.45 (c), and 0.6 (d). Keeping the gas phase composition fixed at x = 0.6, the temperature was varied from 590 °C (e), 565 °C (f), 540 °C (g), to 515 °C (h). To aid in comparison, image (e) shows the same nanowires as (d). The scale bar is identical for all images.

pitch free of parasitic growth or antimony condensation.

Fig. 6.1a-d shows $InAs_{1-x}Sb_x$ nanowires grown with $x_v = 0.15$, 0.30, 0.45, and 0.60. There is a clear transition in axial growth rate that occurs between $x_v = 0.15$ and 0.30, which then stays relatively constant up to $x_v = 0.60$. As discussed earlier, [*TBAs*] is kept fixed at the minimum value allowed by the MOCVD system and [*TMIn*] and [*TDMASb*] are adjusted to change the composition and V/III ratio. Thus, for larger x_v , both the TDMASb and TMIn are increased, raising the overall concentration of precursors in the reactor and initially enhancing the vertical growth rate. Subsequently, the growth rate is kinetically limited and remains relatively constant, despite increasing group III concentrations. This becomes more evident as the growth temperature is decreased from 590° C to 515° C, shown in Fig. 6.1e-h. It is worth noting that the vertical growth rate was improved at 515° C by slightly increasing the V/III ratio from 2.05 to 2.17 at the expense of reduced solid phase antimony composition.



Figure 6.2 Solid phase composition, *x*, as determined by EDX spot measurements, of $InAs_{1-x}Sb_x$ nanowires as a function of the vapor phase composition, *x_v*. The solid lines are calculated from a thermodynamic growth model.

6.3. Material characterization

6.3.1 Antimony composition

The solid phase composition, x, was determined using EDX point analysis at four points along the length of the nanowire. The analysis was carried out using the standardless ratio method using the L α emission lines of In, As, and Sb. Stoichiometry was verified to within $\pm 2.5\%$ and composition uniformity was verified with a line scan along the axial direction of the nanowire. No variation in composition in the axial direction was found. In Fig. 6.2, x is plotted as a function of x_v along with the theoretical solid phase composition based on a thermodynamic model developed for planar InAsSb growth under the constraint of high V/III ratio (93), then later generalized for any V/III ratio (94). The calculation assumes complete decomposition of the precursors and treats the non-ideality of the solid using the regular solution model. By enforcing conservation of mass constraints on the system, the solid phase composition can be calculated from the input partial pressures of the group III and group V precursors. Although the V/III ratio in the experiment was 2.05, the best fit to the data is achieved using a V/III ratio of 5 in the calculation. It is well known that nanowire growth is extremely sensitive to pattern geometry and diffusion of adatoms from the large area of the mask surrounding the pattern, known as the *skirt* (95). The increase in V/III ratio observed here is likely caused by parasitic growth on the skirt area. Photoluminescence from the parasitic growth has a peak emission at roughly the same wavelength as the nanowires, indicating the composition is similar to the nanowires. Thus, the parasitic InAsSb growth acts as an indium sink for adatoms diffusing towards the nanowires from the skirt area. Since V/III > 1, all of the indium is consumed (96) by the parasitic growth leaving behind excess group V precursors that diffuse along the mask towards the nanowire arrays, leading to an increase in the effective V/III ratio within the nanowire arrays.

For planar growth of InAsSb, the antimony composition is known to increase for increased x_v , decreased temperature, or decreased V/III ratio. Since V/III > 2 is necessary to achieve uniform nanowire morphology, in order to obtain antimony composition greater than 15%, antimony composition must be increased by increasing x_v rather than reducing the V/III ratio. From Fig. 6.2, we expect a rapid increase in the antimony composition for $x_v > 0.8$, however for this study we were unable to reach $x_v > 0.8$ while simultaneously ensuring R < 8 due to the lower limit of the TBAs flowrate imposed by the MOCVD system, $[TBAs]_{min} = 6.26 \times 10^{-5}$ atm. One possibility to overcome this limit is to use a smaller pitch for the nano-hole array in the mask since this allows for larger values of R to be used, allowing higher TDMASb flowrates to be used. Another method is to reduce the effective TBAs partial pressure (thereby increasing x_v) by modulation of the flow rate in an "on-off" fashion. The best solution, however, is simply to modify the MOCVD system to allow lower TBAs flow rates by a suitable mass-flow controller replacement or the installation



Figure 6.3 (a) Low-temperature (77 K) photoluminescence for as-grown InAsSb nanowires (blue) for increasing antimony composition. The peak at 0.4 eV is due to the InAs substrate (grey). (b) FWHM as a function of antimony composition for InAsSb nanowires and epitaxial film. (c) FWHM of InAsSb nanowires and the InAs substrate they were grown on as a function of temperature.

of a dilution line for the TBAs. Reducing the TBAs flow while keeping the TDMASb flow fixed accomplishes the same increase in x_v without increasing the antimony partial pressure.

6.3.2 Photoluminescence

Only one study of InAsSb nanowire PL has been reported in the literature. PL is presented for InAs and InAs_{0.96}Sb_{0.04} and is composed of several peaks, attributed to type II quantum-well emission, impurity emission, and band-to-band emission with peaks in the range of ~0.39 – 0.44 eV at 10 K (85). Despite this work, there still has been no mid-infrared (3 – 5 μ m) PL from InAsSb nanowires reported in literature. We performed low-temperature (77 K) PL measurements on the as-grown samples. Typical PL spectra of InAsSb nanowires are depicted in Fig. 6.3a. The two peaks correspond to the InAs substrate at ~0.4 eV and the InAsSb nanowires, shaded in blue. All fitting was done using only two Gaussian functions, suggesting type II quantum well or defect emission is not present in our nanowires (or is too weak to resolve). Furthermore, the intensity of the nanowire PL is comparable to that of the substrate, despite a fill-factor of only about 10%, indicating high-quality nanowire material. The emission from the nanowires with *x* < 0.068 is clearly blue-shifted compared to the InAs substrate PL. This phenomenon will be discussed in more detail later in the text.

In Fig. 6.3b, the full-width half-max (FWHM) of the InAsSb nanowires as a function of x is compared to epitaxially grown planar InAsSb on InAs substrate by MOCVD(97). As it does for planar InAsSb, the nanowire PL FWHM remains relatively constant for increasing x, however the nanowire FWHM is roughly 10 meV broader. The broad FWHM of the ternary alloys (with respect to the binaries) is typically attributed to random fluctuations in the composition (98), and nanowires appear to be no exception in this regard. Temperature-dependent PL measurements were performed on nanowires with x = 0.068. The FWHM as a function of temperature is shown in Fig. 6.3c for both the InAs substrate and the InAsSb nanowires. The FWHM of the InAs substrate increases linearly with temperature with a slope of $3.3k_B$, however the FWHM of the InAsSb nanowires remains relatively constant. Suppression of thermal broadening has been observed in AlGaAs/GaAs (99) and InSb/In_{1-x}Al_xSb (100) quantum wires, but the dimensions of the InAsSb nanowires are much too large for quantum effects to be observed. Therefore, the most

likely explanation is that a large inhomogeneous broadening component is responsible for the temperature-independent FWHM. There are many causes of inhomogeneous broadening, including ionized impurity scattering, hetero-boundary roughness, and inhomogeneities of alloy composition (*101*). Further study is necessary to determine the exact cause of the inhomogeneous broadening.

6.3.3 Bangap blueshift

The temperature dependence of binary semiconductors is described by (102)

$$E_g(T) = E_{g0} - \frac{\alpha T^2}{\beta + T} \tag{6.1}$$

where E_{g0} is the bandgap at 0 K, and α and β are empirically determined parameters. For InAsSb, the bandgap as a function of the composition at a given temperature is typically expressed as (103)

$$E_g(x) = xE_{InSb} + (1-x)E_{InAs} - Cx(1-x)$$
(6.2)

where E_{InAs} and E_{InSb} are the bandgaps at a temperature *T*, and *C* is the bowing parameter. By combining Eq. 1 with Eq. 2 and assuming the parameters α and β are linear functions of *x*, we can express the temperature dependence of InAs_{1-x}Sb_x as

$$E_g(x,T) = E_{g0}(x) - \frac{\alpha(x)T^2}{\beta(x) + T}$$
(6.3)

with

$$\alpha(x) = \alpha_{InAs} + (\alpha_{InSb} - \alpha_{InAs})x \tag{6.4}$$

and

$$\beta(x) = \beta_{InAs} + (\beta_{InSb} - \beta_{InAs})x \tag{6.5}$$



Figure 6.4 (a) Temperature dependence of the PL peak energy (black squares) and the corrected bandgap using correction of $k_BT/2$ (blue triangles) and $2k_BT$ (red circles). The solid line is calculated using x = 0.068 and a bowing parameter of C = 662 meV. (b) Estimated bandgap of InAsSb nanowires using a correction of $k_BT/2$ (symbols) and calculated bandgap using C = 662 meV. Inset: Difference between experimental and calculated bandgap as a function of antimony composition.

Using experimentally determined values of E_{go} , α , and β for InAs and InSb (97), we use *C* as a fitting parameter for the temperature dependent data. The peak energy, E_p , as a function of temperature for InAsSb nanowires with x = 0.068 is plotted in Fig. 6.4a. For the binary

semiconductors, E_g is $k_BT/2$ below E_p . The ternary InAsSb, however, typically exhibits a bandgap $2k_BT$ below E_p for x > 0.10. This has been attributed to transitions where the wave-vector k is not conserved (97) and is an indicator of poor material quality. Transitions that do not conserve k can occur if there is a high degree of disorder in the crystal due to the lattice mismatch, clustering due to a miscibility gap, or high impurity concentrations (104). The sold line in Fig. 6.4a is calculated with C = 662 meV, slightly lower than that reported by Fang, *et al.* (672 meV) and Yen, *et al.* (685 meV). There is no value of C that will give a good fit to the k-nonconserved model, and thus we conclude that k-conserving transitions are responsible for the PL observed from the InAsSb nanowires. Additional evidence for the k-conserving nature of the PL is the fact that the energy peak shift for the nanowires is about 23 meV for T = 77 to 200 K (higher temperatures were unfortunately not possible due to weak signal), about the same as for the binaries, InAs and InSb. For planar InAsSb with x > 0.10, k-nonconserving transitions result in smaller peak shift, roughly 7-15 meV for the same temperature range (97,98,105,106).

Having determined the appropriate correction to the peak energy, the bandgaps are calculated for the remaining samples and plotted in Fig. 6.4b, along with the calculated composition dependence given by Eq. 2 with C = 662 meV. As mentioned briefly earlier in the text, a significant blueshift is present in the expected bandgap of InAsSb nanowires for low antimony composition. There exists both theoretical (107,108) and experimental (109–111) evidence that the bandgap of wurtzite (WZ) InAs is blueshifted with respect to zinc-blende (ZB) InAs. In addition, it has been shown that there is significant structural evolution of InAsSb nanowires with increase of Sb incorporation. For Au-catalyzed grown nanowires, a transition from WZ/ZB polytypism to pure ZB crystal phase occurs at about x = 0.05 (82), while for indium droplet assisted growth the ZB crystal phase becomes dominant at about x = 0.10 (85). These two

facts suggest that we should expect to see this structural evolution mirrored by a similar evolution of the bandgap of InAsSb nanowires for increasing antimony composition. The inset of Fig. 6.4b plots the difference between the expected bandgap (for the ZB crystal phase) as a function of antimony composition. Somewhere between x = 0.05 and x = 0.068 the blueshift vanishes, suggesting the ZB crystal phase has become dominant.

6.3.4 Crystal structure

In order to validate the hypothesis that the bandgap is influenced by the crystal structure, a HR-TEM image of an InAsSb nanowire with x = 0.068 was analyzed to determine the crystal phase composition (Figure 6.5). The solid white line guides the eye along the crystal stacking

Figure 6.5 High resolution TEM image of an InAsSb nanowire with x = 0.068 showing two types of planar defects: rotational twins (RT) and extrinsic stacking faults (ESF). The solid white line helps guide the eye along the zinc-blende stacking sequence, ...ABCABC..., which is only interrupted by twin planes and the occasional stacking fault. At this composition, no evidence of wurtzite crystal structure was found.

sequence. We adopt the convention of requiring a minimum of four planes in a stacking sequence to avoid ambiguity between ZB and WZ crystal phases. Each HR-TEM images spans 33 nm, and

6 images taken along the length of the wire, for a total of 200 nm. The nanowires are about 2 μ m long, so this represents a 10% sampling of the nanowire. We find that the nanowire is composed entirely of ZB crystal phase with a rotational twin density of 269 μ m⁻¹ and a stacking fault density of 70 μ m⁻¹ (includes both extrinsic stacking faults and intrinsic stacking faults). Moreover, the maximum blueshift of about 60 meV is in good agreement with the theoretical prediction of about 55 meV. This is strong evidence for a crystal phase-induced blueshift of the PL at low antimony composition.

6.4. Device fabrication

Arrays of InAsSb nanowires with a diameter of 180 nm and a height of 1000 nm were grown on a p-doped InAs buffer layer with a doping concentration of 5×10^{18} cm⁻³ on GaAs (111)B substrate. A p-n heterojunction is formed between the p-doped InAs buffer layer and an n-doped InAsSb NP array with doping concentration of 3×10^{17} cm⁻³ to generate a built in field for extracting photo-generated carriers. The gas phase Sb composition, Sb / [Sb + As], during growth was 40% which resulted in a solid phase composition of 7% (*112*). The detector effective area was 50 µm × 50 µm, consisting of a square array of 3086 nanowires with a pitch of 900 nm. The bottom and top metals are Cr/Au (10 nm/150 nm). Figure 6.6a shows an SEM image of the fabricated nanowire photodetector (NW-PD). The NW-PDs were wire-bonded to a 68 pin leadless chip carrier (LCC), as depicted in Fig. 6.6b. The schematic of the NW-PD is shown in Fig. 6.6c.

6.5. Electrical characterization

The wire-bonded NP PDs were mounted in a lakeshore TTPX cryogenic probe station for dark current measurements. Figure 6.7a shows temperature dependent dark current characteristics of the NW-PD. At 77 K, dark currents as low as 40 pA were achieved at a reverse bias of 0.1 V, corresponding to a dark current density of 200 mA/cm² (normalized to the NP junction area). We

Figure 6.6 (a) SEMs of the fabricated NP PDs. Inset shows the diameter of NP. Scale bar indicates 100 nm in the inset. (b) Photograph of the wire-bonded device. (c) Schematic of proposed NP PD structure.

note that the diode behavior and the kinks in the low temperature IV curves under forward bias are a common feature of InAs diodes and has been attributed to tunneling current (*113,114*). The temperature dependence of the dark current of a PD is described by equation (6.6) below,

$$I = AT^{\frac{3}{2}}e^{-\frac{E_a}{kT}} \left(e^{\frac{qV_{bias}}{2kT}} - 1 \right)$$
(6.6)

Figure 6.7 (a) Semi-log plot of dark current voltage from 77 - 300 K. (b) Extraction of the activation energy of NP PD at reverse bias of 0.1 V and 0.3 V.

where A is proportionality constant, E_a is the activation energy, q is the elementary charge, k is Boltzmann constant, V_{bias} is the bias voltage, and T is the temperature. E_a can be extracted by fitting the slope of the semi-log plot of $I/V^{3/2}$ with 1/kT. Figure 6.7b shows the extracted activation energies at reverse biases of 0.1 V and 0.3 V. An activation energy of 0.17 eV is measured, which is approximately half the bandgap of InAs_{0.93}Sb_{0.07}. The dark current density is comparable to bulk InAsSb photodiodes that are limited by generation-recombination current.

In order to evaluate the electro-optic properties of the NW-PD, the LCC is mounted in a liquid nitrogen flow cryostat integrated with a Nicolet 8700 Fourier-transform infrared (FTIR) spectrometer. The NW-PDs were illuminated by an IR source passing through the FTIR and then focused by means of a reflective objective. The photocurrent spectra was recorded in the rapid scan mode with a spectral resolution of 4 cm⁻¹. To account for the spectral response of the IR source and system optics the photocurrent spectra was normalized to the flat response of a deuterated triglycine sulphate (DTGS) detector. The frequency response of the DTGS detector was also compensated by taking advantage of the variable mirror velocity of the FTIR, allowing the true spectral shape of the photocurrent spectrum to be recorded. The arbitrary units of the photocurrent spectra were converted to units of amperes per watt using a calibrated commercial InGaAs detector.

Figure 6.8 shows the measured spectral responsivity taken under unpolarized IR light at 77 K (blue, left axis) and 227 K (red, right axis). The cutoff wavelength (λ) of the NW-PDs is around 3000 nm. Evidence for plasmonically enhanced absorption is the occurrence of the enhanced responsivity peaks around 1040 nm, 1370 nm, 1950 nm, and 2390 nm with a corresponding zero bias responsivity of 0.189 A/W, 0.161 A/W, 0.149 A/W, and 0.194 A/W, respectively. The inset shows the quantum efficiency at 2390 nm as a function of reverse bias, where the quantum efficiency reaches ~29% at a reverse bias of 0.15 V. The quantum efficiency of the NW-PDs is comparable with planar PDs using 2.5- μ m-thick InAs_{0.88}Sb_{0.12} layer (*115*) which exhibit a quantum efficiency of 19% and 25% at wavelengths of 4000 nm and 2400 nm, respectively. Further increasing the bias results in a degradation of quantum efficiency as the photocurrent is degraded

Figure 6.8 Measured spectra responsivity of NP PDs at 77 K (blue, left axis) and at 227 K (red, right axis). The spectra are carefully normalized by a DGTS and a commercial InGaAs detector in amperes per watt. The inset shows the quantum efficiency (QE) in terms of the bias voltage.

by the increase in dark current. The bias dependence of the quantum efficiency can be explained by increased carrier collection efficiency of the plasmonically photogenerated carriers at the exposed portion of the nanowires as a result of the expanding depletion region. We confirmed that the spectral response disappears when light is incident on nanowires which are not covered by metal so that the InAs buffer layer does not contribute to the photocurrent.

The NW-PDs can be operated at a relatively high temperature, above 220 K, which does not require bulky cryogenic cooling but light weight thermoelectric coolers. It also clearly shows the peaks at similar wavelengths, indicating the LSP resonances, although the responsivity is much lower than that at 77 K. We should note that the operation temperature of NW-PD can be further increased by passivating the nanowire surface in order to reduce the surface recombination and by incorporating heterostructures which can provide electron or hole barriers.

6.6. Discussion

High quality InAsSb nanowires were grown using catalyst-free SA-MOCVD for the first time. Antimony composition as high as 15% is achieved, with strong PL at all compositions and a FWHM comparable to that of epitaxially grown thin films on InAs. We find a bowing parameter of C = 662 meV fits the data well and agrees with the majority of the literature on epitaxial films. We observed a blueshift in the photoluminescence for $x \le 0.068$ and a maximum blueshift of 60 meV, which is evidence for crystal-phase-dependent bandgap. HR-TEM analysis supports the crystal-phase-dependent bandgap hypothesis by showing that the crystal phase is composed entirely of ZB for a nanowire with no PL blueshift.

We demonstrated InAsSb NW-PDs with high quantum efficiency of ~ 29% at a reverse bias of 0.15 V, which is comparable to planar PDs. The spectral response has a cutoff wavelength of ~3000 nm. Several peaks (that is, strong absorption) in the response were observed and FDTD simulations confirmed that the strong absorption is caused by LSP resonances and showed a 37x absorption enhancement compared with bare nanowires at 2440 nm for the *x*-polarization. This work shows that NW-PDs can be used for detecting mid- and/or long-IR wavelength light. This has remained largely unexplored in nanowire photonics because the diameter of nanowires should be over 1000 nm in order to have significant absorption(*84*). Our plasmonic antenna structure can circumvent this problem and allow high performance infrared imaging systems, such as the focal plane array (FPA) camera, with reduced pixel size and pitch. It has been shown in this work that it is possible to fabricate nanowire devices with electrical characteristics that are equal to bulk detectors. That is, when comparing device characteristics such as dark current density, ideality factor, activation energy, etc., we have shown equivalent performance between bulk and nanowire material. This addresses perhaps the most scathing criticism of nanowire devices: the large surface-to-volume ratio. We achieved bulk-equivalent electrical characteristics through a combination of in-situ high-bandgap passivation, end ex-situ BCB passivation. The effectiveness of this scheme relies on a device design that keeps the depletion region contained entirely beneath the surface of the BCB. The one exception to this is the InGaAs/InP material system, where the high growth temperature results in rapid phosphorus desorption and damaging arsenic-phosphorus exchange.

Given that bulk-equivalent electrical characteristics can be achieved, the next question is whether there is any advantage to using the nanowire platform. For simple photodetectors, the answer is yes. The use of plasmonic antenna structures allows the decoupling of the semiconductor junction area from the optical absorption area. As a result, the total bulk volume can be reduced by some factor, while reducing the optical absorption by some smaller factor, leading to an increase in detector sensitivity, as was shown explicitly for the GaAs NW-PD. However, this improvement in sensitivity probably does not justify the increased cost of the nanowire platform. Another potential benefit of the nanowire platform is for ultra-high bandwidth photodetectors. The plasmonic antenna design means only a few hundred nanometers are required for efficient light absorption, compared to several microns for planar devices. The reduction in carrier transit time can result in much higher bandwidth devices. In order to realize such a device, nanowires need to be grown on an undoped substrate. Since electrical contact cannot be made to the bottom of the nanowires, this means that the surface of the substrate must be doped, either by ion implantation or epitaxial growth. Epitaxial growth is preferable, as the material quality is much improved over substrates, and in addition, device layers may be grown for more sophisticated device designs, such as a SAM-APD where the avalanche region consists of epitaxially grown planar layers and the absorber consists of small bandgap nanowires. Unfortunately, epitaxial growth on the (111)B surface is not well studied, and would require a significant effort to develop the growth techniques. Given the immense challenges for growth on undoped substrates, it is not clear at this stage whether ultra-high speed nanowire photodetectors are a practical application for the nanowire platform. For SPADs and MWIR photodetectors, on the other hand, the case for the nanowire platform is much more compelling.

The single biggest issue plaguing conventional InGaAs/InP SPADs is the afterpulsing dilemma. This is a problem that will only go away when growth techniques that produce material with a much lower defect density are developed. However, the demand for near-IR SPADs is outpacing the development of high purity III-V material, and so other approaches have been taken, mostly having to do with gating techniques. The problem with gating is that it introduces a significant level of complexity to the SPAD circuitry, reduces the maximum photon count rate, and results in "dead" times when the detector is blind to impinging photons. These consequences of gating make near-IR SPADs inappropriate for applications that require high count rates and arbitrary photon arrival times, such as LiDAR and QKD. It was shown in this work that the nanowire platform provides an elegant solution to the afterpulsing dilemma: by confining each avalanche pulse to a single nanowire, the volume of material exposed to the large flow of current

that causes the filling of traps is reduced by several orders of magnitude, resulting in a significant reduction in afterpulsing. The reduction in afterpulsing was so significant, that the NW-SPAD was operated in free-running mode with passive quenching and no dead time while maintaining a DCR < 10 Hz at 125 K. The limitation of the current device design is that one of the design rules must be broken: the depletion region must extend beyond the surface of the BCB. By breaking this design rule, the operating temperature of the NW-SPAD was limited to below 200 K. The large surface leakage current at higher temperatures resulted in unstable operation, i.e., large fluctuations in the DCR on time scales in the seconds. In order for the nanowire platform to be a commercially viable alternative to planar InGaAs/InP SPADs, an effective passivation scheme must be developed for the exposed surface of the nanowire. The simplest means of achieving this may simply be to apply a second layer of BCB after device fabrication to protect the exposed portion of the nanowires. In any case, the performance of the NW-SPAD at low temperature provides compelling motivation to further develop the design this device.

Finally, a strong case for MWIR-LWIR nanowire photodetectors can be made on the basis of the lack of lattice-matched substrates available for planar growth. In addition, the only commercially available semiconductor LWIR photodetector contains both mercury and cadmium, each of which are banned in the ROHS compliance guidelines. An InAsSb nanowire LWIR photodetector would quickly find large commercial demand, especially in the European Union. InAsSb nanowires in this work have a maximum wavelength cutoff at 5 μ m, and so much work remains to be done to extend this to the LWIR (14 μ m). Nonetheless, the demand for LWIR detectors is not going away any time soon, and the competition is thin, and so nanowire LWIR detectors should be a strong candidate in the years to come. One major change that will have to occur is the plasmonic antenna design, which is currently based on a simple tilted metal deposition

technique. Therefore, the dimensions of this plasmonic antenna are tied to the dimensions of the nanowires. Unfortunately, this will not do in the LWIR, as the nanowire dimensions are much to small, even for plasmonics. A new design will likely depend on EBL to pattern a larger antenna design on top of multiple nanowires to create surface plasmon resonances that engulf multiple nanowires at once. Work on such designs is already underway by students who remain in the group.

In conclusion, it is my contention that nanowire photodetectors do indeed have a place in commercial applications. The increased complexity, in terms of sample preparation, nanowire growth, and device design, must be justified by the promise of unmatched performance in some critical performance metric. I believe this was shown to be the case with NW-SPADs, where the reduction in afterpulsing is unprecedented for III-V SPADs and can revolutionize near-IR single photon detection.

A.1. Material parameters

In the main text, the ratio of the diffusion current to the recombination current at low forward bias is calculated using the following parameters for GaAs. Note that this calculation is an order of magnitude estimate, and so we are not concerned with the accuracy of these values, but rather that the values are reasonable for GaAs nanowires.

Parameter	Value	Units
n _i	2.1×10^{6}	cm ⁻³
D_n	100	$\mathrm{cm}^2\mathrm{s}^{-1}$
$ au_n$	1	ns
L_n	3	μm
W_p	300	nm

Table A1. Material parameters for GaAs nanowires used throughout the main text

A.2. Electrical modeling

The simulations are meant to incorporate all the elements of the actual device structure, shown schematically in Fig. A4. This includes modeling every interface as non-ideal, i.e., non-zero surface recombination velocity, *S*. In addition, we include the radial overgrowth since it is known that the GaAs/SiO₂ interface is very poor and can negatively influence electrical characteristics.

Figure A4. 2D schematic of simulation structure. The actual simulation structure is fully 3-dimensional.

The key simulation parameters are given in the table below.

Parameter	Value
τ _e	1 ns
μ_e	$1000 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$
S(GaAs/InGaP)	10 ³ cm/s
$S(GaAs/SiO_2)$	10 ⁷ cm/s
$S(InGaP/SiO_2)$	10 ⁷ cm/s
<i>S</i> (InGaP/BCB)	10 ⁵ cm/s
S(InGaP/air)	10 ⁷ cm/s

Table A2. Material parameters for GaAs nanowires used in the 3D simulations.

The experimental setup is shown in Fig. B1. The wire-bonded NW-PD sample was cooled with liquid nitrogen in a cryostat. The optical spectra were analyzed by a Fourier-transform infrared (FTIR) spectrometer (Thermo Scientific Nicolet 6700) equipped with an infrared microscope (Thermo Scientific Nicolet Continuµm). The NP PDs were illuminated by a thermal IR emitter passing through the FTIR and the light was focused in 150 µm × 150 µm area by a 15× Reflachromat Objective coupled with side port reflectance accessory. The photocurrent spectra were then collected in rapid scan mode with a spectral resolution of 4 cm⁻¹ in the spectral range 2000-10000 cm⁻¹ and averaging of 32 scans.

Figure B1. Experimental setup for measuring the responsivity of NP PDs. BS indicates beam splitter.

Figure B2. Responsivity measurement and unit conversion. (a) Measured frequency response of DTGS at various wavelengths in terms of the mirror velocity in the FTIR. (b) Comparison of the measured response with the compensated response of DTGS by taking advantage of a different magnitude at different mirror velocities. (c) Calibration of a commercial InGaAs detector response with the responsivity of 0.9 A/W at 1310 nm given by dividing by the compensated response of DTGS. (d) Calibration of InAsSb NP PDs response given by dividing by the compensated response of DTGS. The arbitrary units of the InAsSb NP PDs response (blue curve, left axis) are divided by the response and multiplied by the responsivity of the commercial InGaAs detector in order to convert to units of amperes per watt (red curve, right axis).

The responsivity can be obtained by taking advantage of the different responses of the DTGS detector with regards to various mirror velocities in the FTIR. We start by assuming that the DTGS detector shows a flat spectral response, which means the response proportional to the incident light power at each wavelength, as opposed to a semiconductor detector. However, the spectral response of the DTGS depends on optics in the FTIR, such as the interferometer mirror velocity. In order to compensate the spectral response of the DTGS, the responses of the DTGS at various mirror velocities and a few fixed wavelengths are measured as a function of wavenumber, as depicted in Fig. B2a. It is shown that there is a decrease of the response at shorter wavelengths (that is, large wavenumber) due to an underestimation of the light source by high frequency roll-off. We chose the response of the DTGS at 1.5 µm wavelength. The response at any arbitrary frequency can be extracted by fitting the measured response with a characteristic response equation and then the response of the DTGS is compensated as shown in Fig. B2b. The calibrated responses of a commercial InGaAs detector (Global Communication Semiconductor) and our NP PDs divided by the compensated response of the DTGS are plotted in Fig. B2c and d, respectively. Finally, the arbitrary responsivity is converted to units of amperes per watt by multiplying by a calibrated commercial InGaAs detector responsivity.

InP nanowires were grown on InP(111)A substrate at 650° C using a V/III ratio of 37 with no passivation shell. These conditions yielded vertical nanowires with little radial overgrowth (Fig. C1a). At lower temperatures the InP nanowires become tapered, resembling "nanoneedles." At higher III/V ratios, there is significant radial overgrowth. The dark current of devices fabricated from these nanopillars was several orders of magnitude lower than the InGaAs nanopillars (Fig C1b), with less than 15 pA at 15 V reverse bias at room temperature. Extraction of the activation energy from temperature dependent current-voltage measurements gives $E_a = 0.671$ (Fig. C1c). This implies that generation-recombination from mid-gap states dominates the dark current. This is a marked improvement over the InGaAs nanopillars and provides motivation for the separate absortion-multiplication (SAM) structure.

Figure C1 | **a**, Tilted SEM of InP nanopillars grown on InP substrate. Scale bar: 600 nm. **b**, Temperature dependent current-voltage measurements, **c**, Arrhenius plot of the leakage current at 100 mV reverse bias.

Figure C2 | Comparison of dark current characteristics of InP and GaAs homojunction diodes. The reverse leakage current of the devices is essentially identical. The forward bias current, on the other hand, is much different. This is simply due to the superior Ohmic contact on the p-GaAs nanowires.

Since the bandgaps of GaAs and InP are nearly identical, we expect very similar IV characteristics from equivalent nanowire devices. Fig. C2 compares the IV at room temperature of the GaAs diode described in Chapter 2 to the InP diode described in this Appendix. The leakage current is nearly identical for both devices, which is not surprising as the generation current due to midgap states is likely similar. The series resistance of the InP device is much higher than the GaAs device, simply due to superior Ohmic contact to the GaAs device. In both cases, the dark current density is as good or better than bulk detectors.

Appendix D: InGaAs-InP nanowire heteroepitaxy

Axial InGaAs/InP heteroepitaxy was attempted with limited success. The results of these attempts are presented below.

D.1 Direct heteroepitaxy

The most obvious way to growth the InGaAs/InP axial heterostructure is simply to grow the InGaAs layer after the InP layer. There are several ways to do this, as shown in growth sequences I-IV in Fig. D1. The gas phase indium fraction is 50% and V/III = 40 for all growths.

Figure D1. Growth sequences I-IV all have identical InP growth, but vary the parameters of the subsequent InGaAs growth.

Figure D2. Switching sequence when going from InP to InGaAs growth. The temperature is ramped to the InGaAs growth temperature under TBP overpressure.

Growth sequence I simply grows each layer at the optimum temperature for that material. Growth sequence II keeps the temperature fixed for both layers. Growth sequence III reduces the temperature for the InGaAs growth. Finally, growth sequence IV starts the InGaAs growth at a low temperature, then ramps up to a higher temperature for the remainder of the growth. The switching sequence between the InP and the InGaAs is shown in Fig. D2. When the temperature between layers is different, the temperature is ramped under TBP overpressure to prevent phosphoros desorption in the first InP layer.

The first layer, consisting of a single undoped InP layer, is shown in Fig. D3. This growth serves as a reference when analyzing the result of the InGaAs growth. The results of growth sequences I and II are shown in Fig. D4. Note that in both cases, there is significant phosphorus desorption due to the high temperature growth of InGaAs with no TBP overpressure to protect the InP layer beneath. This motivates growth sequence III, where the InGaAs growth temperature is significantly reduces to slow the rate of phosphorus desorption.

Figure D3. Growth of InP layer for comparison with later growths where the InGaAs layer is added.

Figure D4. For both growth sequences I and II the resulting nanowires are shorter than the original InP layer, indicating rapid phosphorus desorption occurs before InGaAs growth commences.

Figure D5. Result of growth sequence III for increasing InGaAs growth time. The reduced InGaAs growth temperature circumvents the phosphorus desorption problem, however the radial growth rate is quite high, resulting in a thick shell.

Fig. D5 shows a series of growths at a growth temperature of 500° C for increasing InGaAs growth times. The InGaAs growth begins on the sidewalls, as can be seen in the second image. The InGaAs forms a complete shell after an additional 30 seconds, and growths mostly laterally from that point on. From the peak wavelength of the photoluminescence at 2.8 μ m, shown in Fig. D6, the indium composition is estimated to be x = 0.88. The temperature of the InGaAs layer is increased from 500° C to 550, 565, and 580° C, shown in Fig. D7. The nanowires appear to get shorter, indicating an increase in phosphorus desorption, as expected. No obvious improvement in axial growth rate is observed in this temperature range.

Figure D6. Photoluminescence of the sample from growth sequence III with 4 minutes of InGaAs growth. The peak at about 2.8 μ m suggests an indium composition of x = 0.88.

Figure D7. Growth sequence III with various temperatures for the InGaAs growth. All InGaAs growth times are 4 minutes.

Figure D8. The indium composition of the InGaAs layer is affected by the growth temperature, increasing as the temperature is reduced. This makes it difficult, or perhaps impossible, to grow InGaAs with roughly equal group III compositions at low temperature.

Fig. D8 shows close-up SEMs of the nanowires with the InGaAs layer grown at 500° C and 550° C. From the PL peaks, the indium compositions are estimated to be 88% and 80%, respectively. Clearly, the growth temperature plays a major role in indium incorporation and axial growth rate. With this in mind, growth sequence IV attempts to increase the InGaAs growth temperature by first protecting the underlying InP layer with a thin indium-rich shell, then ramping the temperature up to grow axial InGaAs. The result of growth sequence IV is shown in Fig. D9, with SEMs taken after each growth step, labeled A, B, and C. Although it appears that an InGaAs shell was successfully grown in step B, the nanowires have nonetheless become smaller after step C, indicating that significant desorption took place.


Figure D9. Growth sequence IV attempts to growth a thin InGaAs shell around the InP layer to prevent phosphorus desorption, then ramp to a higher temperature to allow increased gallium incorporation in the InGaAs. The labels A, B, and C, correspond to the growth after the layers labeled in the schematic.

It is not clear at this time why this is the case. Presumably, with an InGaAs shell surrounding the InP, phosphorus overpressure should no longer be necessary. No further study of this issue was performed.

D.2 Regrowth mask

As is apparent from the previous section, the major issue with axial growth of InGaAs on InP is the inability to suppress phosphorus desorption when growing the InGaAs layer. This likely means



Figure D11. Regrowth method. a, SiO2 is deposited on pre-grown InP nanowires and the top 200 nm are etched with B.O.E. using photoresist as a mask. The top 200 nm of exposed InP are then etched, leaving a tube-like structu. **b**, The InP nanowires before the regrowth mask is deposited. After the InP is etched to make the tubes, the regrowth mask is removed in B.O.E. to verify the height of the remaining InP. **c**, Growth of InGaAs in the regrowth tube mask after removal of the mask in B.O.E. The notch is present in every nanowire, and is located at the heterointerface.

axial growth of InGaAs on InP is in fact impossible since the sidewalls of the InP would be exposed to a phosphorus-free environment. A possible solution to this is to deposit a second growth mask after the growth of the InP layer (Fig. D11a) to protect the sidewalls during InGaAs growth. This was accomplished by depositing an isotropic 100 nm thick SiO₂ mask deposited by PECVD after the growth of the InP layer (Fig. D11b). The sample is then planarized with AZ5214 photoresist, which is then etched using RIE to expose about 200 nm of the SiO₂ covered nanowires (Fig. D11c). The SiO₂ is then removed from the exposed area using B.O.E. (Fig. D11d). Finally, about 200 nm of the InP nanowire is etched in a HCl/H₃PO₄/CH₃COOH/H₂O (1:1:2:1) solution (800 nm/min etch rate) to produce a tube-like mask structure, exposing only the (111)A surface of the InP nanowires during growth (Fig. D11e). Fig. D11f shows the result of the growth of InGaAs at 680°C in the tube-mask after the removal of the regrowth mask (close-up shown in Fig. D11g). For the first time, we have all-axial growth of InGaAs in InP, however there is a "notch" on the side of every nanowire. This may be due to uneven filling of the holes during growth, and might be eliminated by reducing the growth rate of the InGaAs. No further study of this growth technique was performed.

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