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Performance Evaluation and Improvement of

Ferroelectric Field-Effect Transistor Memory

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Hyung Suk Yu

2015

ABSTRACT OF THE DISSERTATION

Performance Evaluation and Improvement of

Ferroelectric Field-Effect Transistor Memory

By

Hyung Suk Yu

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2015

Professor Chi On Chui, Chair

Flash memory is reaching scaling limitations rapidly due to reduction of charge in floating gates, charge leakage and capacitive coupling between cells which cause threshold voltage fluctuations, short retention times, and interference. Many new memory technologies are being considered as alternatives to flash memory in an effort to overcome these limitations. Ferroelectric Field-Effect Transistor (FeFET) is one of the main emerging candidates because of its structural similarity to conventional FETs and fast switching speed. Nevertheless, the performance of FeFETs have not been

systematically compared and analyzed against other competing technologies.

In this work, we first benchmark the intrinsic performance of FeFETs and other memories by simulations in order to identify the strengths and weaknesses of FeFETs. To simulate realistic memory applications, we compare memories on an array structure. For the comparisons, we construct an accurate delay model and verify it by benchmarking against exact HSPICE simulations. Second, we propose an accurate model for FeFET memory window since the existing model has limitations. The existing model assumes symmetric operation voltages but it is not valid for the practical asymmetric operation voltages. In this modeling, we consider practical operation voltages and device dimensions. Also, we investigate realistic changes of memory window over time and retention time of FeFETs. Last, to improve memory window and subthreshold swing, we suggest nonplanar junctionless structures for FeFETs. Using the suggested structures, we study the dimensional dependences of crucial parameters like memory window and subthreshold swing and also analyze key interference mechanisms.

The dissertation of Hyung Suk Yu is approved.

Puneet Gupta

Yong Chen

Chi On Chui, Committee Chair

University of California, Los Angeles

2015

This dissertation is dedicated to

my family

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Hyung Suk Yu and Chi On Chui, "Performance Benefits of Ferroelectric Field-Effect Transistor with non-planar structure," *submitted to IEEE Trans. Electron Dev.*

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Augustin J. Hong, Emil B. Song, **Hyung Suk Yu**, *et al.*, "Graphene Flash Memory," *ACS Nano*, vol. 5, pp. 7812-7817, 2011.

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Chapter 1

Introduction

1.1.   Non-volatile Memory

Memory is a data storage device that is widely used for electronic devices. Memory can be categorized into two groups by volatility. Volatile memory is requires a constant power supply to retain data; static random-access memory (SRAM) and dynamic random-access memory (DRAM) are in this category. When power is not supplied to the volatile memory, data is lost immediately. On the other hand, non-volatile memory (NVM) can retain data without a power supply once it is programmed. Read only memories (ROMs), magnetic storage devices such as a hard disk and a tape, optical discs, and flash memory are NVMs. From among these, flash memory is the most important NVM technology due to its great scalability, fast operation time, and simple structure.

1.2.   Operation Principle and Limitations of Flash Memory
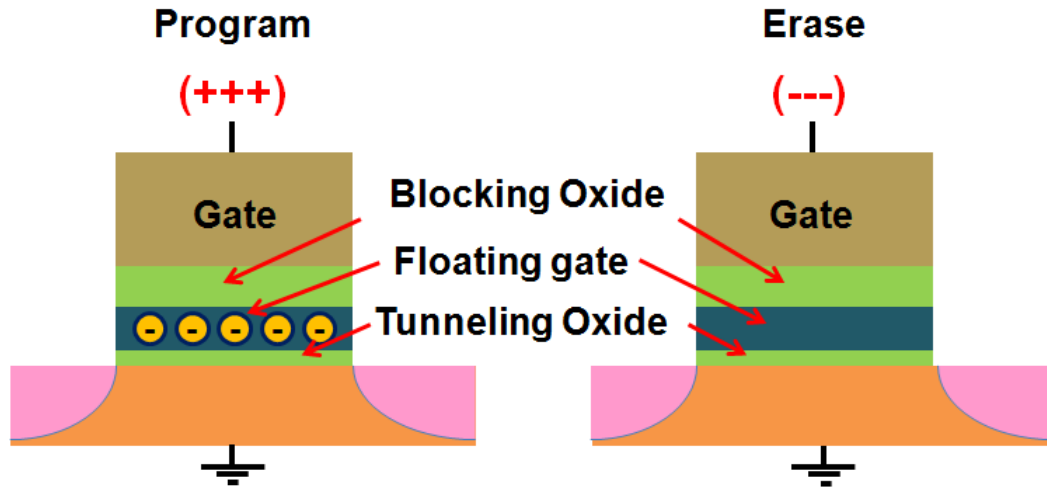
Figure 1.1 Flash memory structure and operations for (a) program and (b) erase.

Flash memory is transistor-based. It consists of one transistor, but the gate oxide is replaced with a floating gate. The floating gate is sandwiched by a blocking oxide (top) and a tunneling oxide (bottom), as shown in Figure 1.1. For programming, a large positive bias is applied to the gate. With a large positive voltage, electrons tunnel though the thin tunneling oxide from the silicon substrate to the floating gate. Although a large voltage is applied, electrons in the floating gate cannot reach the gate because of the thick blocking oxide. After the electrons tunnel into the floating gate, they are trapped because the floating gate is not connected to any electrode (hence, 'floating'). The erase process is simply the opposite to the programming process. Instead of the positive bias, a large negative bias is applied to the gate. Consequently, trapped electrons in the floating gate can pass through the tunneling oxide, and the floating gate is emptied. Without external bias, the electrons inside the floating gate cannot leave the floating gate, and

electrons in the substrate cannot tunnel into the floating gate. The presence of the electrons inside the floating gate results in threshold voltage (V_{th}) shift, which makes a memory window.

If scaled down, the conventional floating gate flash memory shows several problems. First, capacitive coupling of floating gates between neighboring memory cells becomes significant. Due to capacitive coupling, V_{th} is shifted by the neighboring cells, causing reliability issues as shown in Figure 1.2(a) [1]. Second, the number of electrons trapped in the floating gate is limited. It is very obvious that a smaller floating gate holds

(a)

Cell to Cell Interface vs. Technology Node

(b)
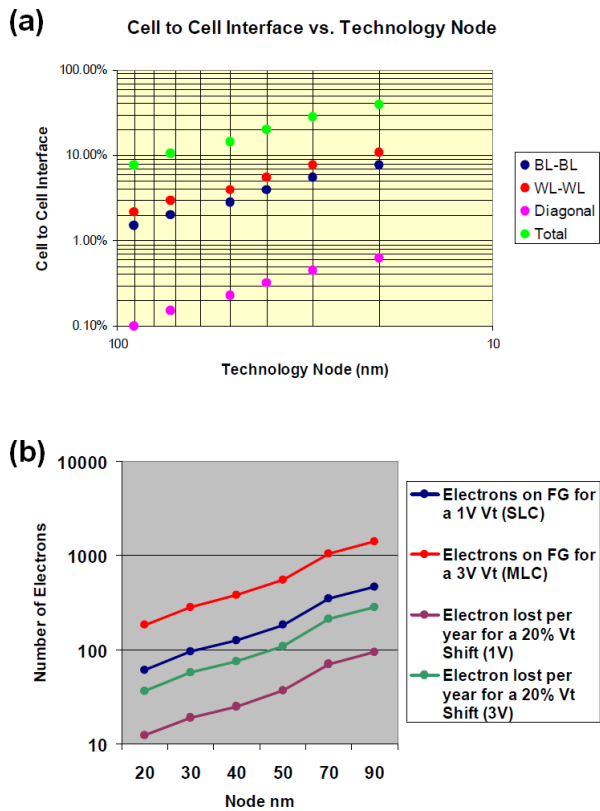
Figure 1.2 Problems of flash memory caused by scaling. (a) V_{th} shift due to capacitive coupling between memory cells and (b) limited number of stored electrons. [1]

fewer electrons, as shown in Figure 1.2(b). Third, as scaled down, the tunneling oxide becomes thinner as well, resulting in stored charge leakage. To relieve these issues, the floating gate is replaced with a charge trapping layer, and Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) is one of the charge trapping memories [2]. Since the trapping layer is not polysilicon, the SONOS can reduce capacitive coupling between memory cells. In addition, the SONOS is more immune to stored charge leakage because the charge trapping layer is an insulator. Although one electron leaks from the charge trapping layer, it just leaves one empty trap, and it does not form a short circuit, unlike the floating gate.

Alternative materials (e.g., CNT or graphene) for better I_{on}/I_{off} ratio and lower capacitive coupling [3], [4] or structures (e.g., TiN-Al$_2$O$_3$-Si$_3$N$_4$-SiO$_2$-Si, TANOS) for lower charge leakaging [5] are proposed to improve performance or to solve the problems mentioned above. However, none of those approaches fundamentally solves the problems. Therefore, to solve the issues, novel memory devices with completely different concepts are emerging.

1.3.   Emerging Memory Technologies

As current flash memory technology faces physical limitations mentioned in the previous section, alternative memory technologies are emerging. Those memory technologies can be categorized into two groups by the intrinsic storage mechanisms; capacitance-based and resistance-based. This section discusses classification of the

memory technologies and operation principles.

1.3.1. Capacitance-based memory

A capacitance-based memory device has three terminals. The memory state is switched by the capacitance changes of the third terminal, which are caused by electric field from the control terminals, like the gates of transistors. The capacitance changes conductivity of the memory. . Ferroelectric field-effect transistor (FeFET) are in this category.

(i) Ferroelectric Field-Effect Transistor

FeFET is a one-transistor (1T) type NVM with a ferroelectric (FE) material. It is receiving attention because of its structural similarity to a conventional FET and fast switching speed. The representative FE materials are perovskite oxides such as $SrBi_2Ta_2O_9$ (SBT) and $Pb[Zr_xTi_{1-x}]O_3$ ($0 \leq x \leq 1$) (PZT). The FE material is polarized by electric field. In Figure 1.3, when an electric field greater than a coercive field (E_C) is applied to the FE material, the FE material is polarized. Once it is polarized, it retains the polarization (remanent polarization, P_R) without an external electric field. It changes the direction of the polarization with the electric field with opposite polarity. As shown in Figure 1.4, the FeFET structure is basically the same as conventional MOSFETs except for the gate oxide. The gate oxide is replaced with an FE material and an optional insulator below it. The optional insulator is inserted between the FE and the semiconductor to prevent unwanted chemical reaction at the interface and charge leakage
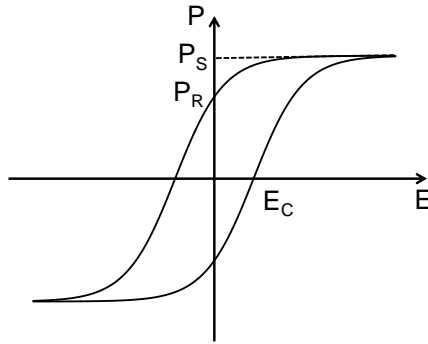
Figure 1.3 Polarization-Electric field (*P-E*) hysteresis of a general ferroelectric material. E_C, P_S, and P_R are coercive field, saturation polarization, and remanent polarization, respectively.
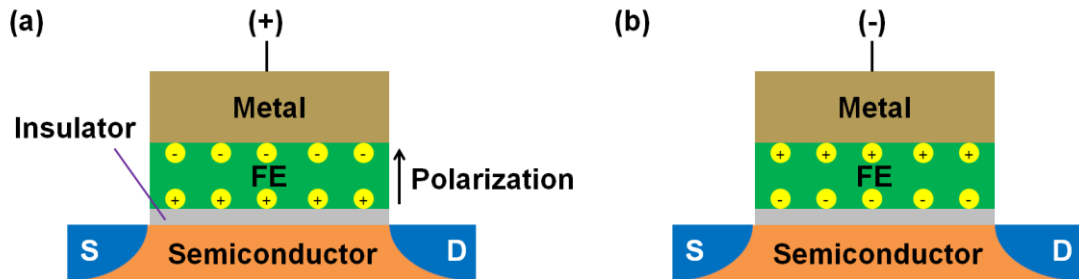
Figure 1.4 FeFET structure (a) with a positive gate bias and (b) with a negative bias. The gate oxide is replaced with an FE layer and an insulator stack. The polarization direction is determined by the gate bias.

from the semiconductor to the FE. When operation voltages are applied to the gate, the FE layer is polarized. Two different polarities of polarization in FE cause V_{th} shift, which makes the FeFET work as a memory device, as pictured in Figure 1.5 [6].

The FeFET has advantages over a 1T1C type Ferroelectric Random Access Memory (FeRAM). The footprint of the FeFET is smaller than that of the FeRAM. In
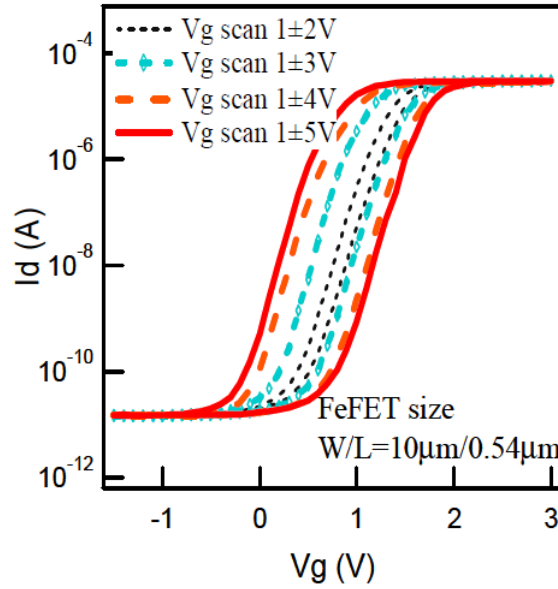
Figure 1.5 I-V characteristics of FeFETs [6].

addition, the read process is non-destructive because the electric field in FE layer caused by read voltage is smaller than E_C, so it does not change the memory state [7]. The memory states are directly distinguished by the transistor current. The FeFET has general advantages over other emerging memory technologies. First, the structure of the FeFET is very similar to the NAND flash memory, so it can immediately replace the flash memory. Second, it does not suffer from sneak current that will be explained in the next section; thus, it does not need additional selection devices.

Although the FeFET has advantages over other memory technologies, it is not commercialized yet due to its short retention time [8]. The Metal-Ferroelectric-insulator-semiconductor (MFIS) structure intrinsically has a depolarization field inside the FE layer and it continuously diminishes P_R of the FE layer, resulting in short retention time.
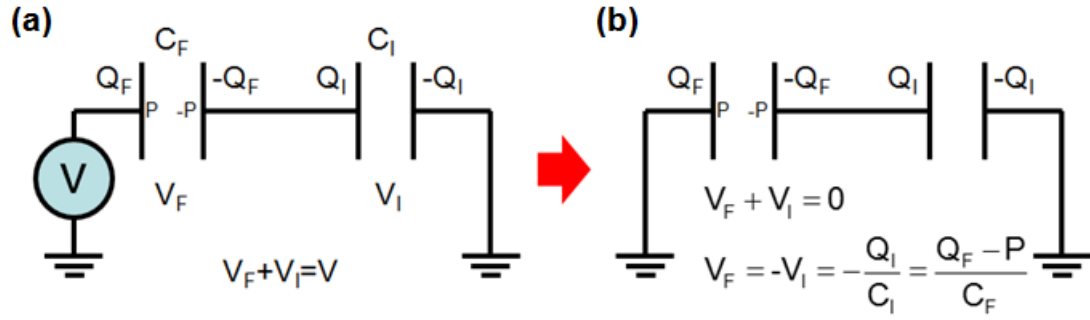
Figure 1.6 Equivalent circuits (a) with external voltage and (b) without external voltage after writing. There exists electric field inside the FE without external voltage.

The origin of the depolarization field is described using equivalent circuits in Figure 1.6. In the figure, C_F, C_I, Q_F, Q_I, and P are ferroelectric capacitance, insulator and semiconductor capacitance, charge of the ferroelectric capacitor, charge of the insulator, and polarization charge in the FE, respectively. When the external voltage V is applied, the voltage across the MFIS stack is

$$V = V_F + V_I. \tag{1}$$

After removing the external voltage, the voltage across the MFIS stack becomes

$$0 = V_F + V_I = \frac{Q_F - P}{C_F} - \frac{Q_I}{C_I}. \tag{2}$$

Without any external voltage, there exists voltage drop across each capacitor. Due to the

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voltage in the FE, there is a depolarization field, E_{dep}. The direction of E_{dep} in FE is the opposite to the electric field for programming, and it is given by

$$E_{dep} = -P \times \frac{1}{\epsilon_F \left(\frac{C_I}{C_F} + 1 \right)}, \qquad (3)$$

where ε_F is dielectric constant of the FE, and minus sign means the opposite direction. To decrease E_{dep}, the denominator of (3) must be large. Therefore, increasing C_I helps to decrease E_{dep}, resulting in longer retention time. One of the ways to increase C_I is using a Metal-Ferroelectric-Semiconductor (MFS) structure instead of MFIS. However, if there is no insulator between the FE and the semiconductor substrate, there might be chemical reaction and charge diffusion at the interface. In order to prevent these problems, low process temperature is essential, but it is not possible for SBT or PZT. Therefore, a new FE material with low process temperature, such as poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)), is necessary.

Another issue for FeFET is power consumption. Since FeFET is programmed by electric field, it requires a strong electric field, unlike resistance-based memories. If the thickness of the FE layer is small, required voltage can be lowered and power consumption can be reduced. However, the organic material cannot be very thin (<50 nm) because of the non-ferroelectric layer formed near the interfaces [9]-[10]. If the organic FE is too thin, it loses ferroelectricity [9]. Silicon doped hafnium dioxide (Si:HfO$_2$) is a promising FE material because a thin FE layer can be achieved (~10 nm).

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Poly(vinylidene fluoride-trifluoroethylene)

Polyvinylidene fluoride (PVDF) is an organic ferroelectric material that consists of carbon, hydrogen, and fluoride atoms, as shown in Figure 1.7. There are four phases of the PVDF, but the β phase (all trans) FE is the most important as an FE material since it has the maximum polarization [11]. To serve as an FE material, it must be crystallized. PVDF, however, is crystallized only up to 50 %. By substituting some H atoms with trifluoroethylene (TrFE) [12], the β phase becomes more stable and it can be crystallized up to 90 % [11]. The composition of the P(VDF-TrFE) determines the
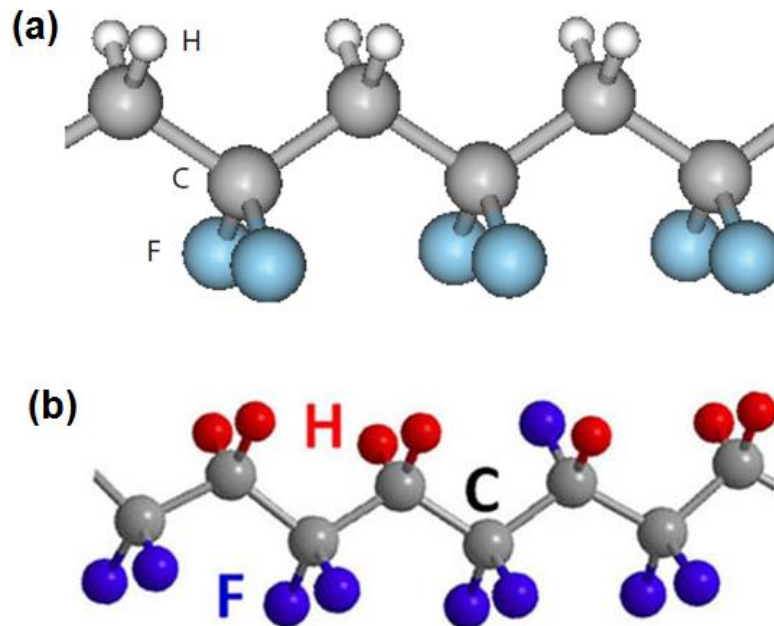
Figure 1.7 The chemical structure of (a) polyvinylidene fluoride (PVDF) and (b) poly(Vinylidene fluoride-trifluoroethylene). [11], [12].

material properties such as melting point, Curie temperature, dielectric constant, P_R, and E_C. The material parameters are listed in Table 1.1 [11].

Table 1.1 Material parameters of PVDF and P(VDF-TrFE) with various compositions [11].

Property	PVDF	VDF:TrFE 80:20	VDF:TrFE 70:30	VDF:TrFE 70:30, LB
Melting Temperature (℃)	180	148	152	>150
Curie Temperature (℃)		145	116	80-110
Dielectric Constant	16	12	10	>8
P_R (µC/cm^2)	12	10	8	8
E_C (MV/cm)	0.75	0.38	0.05–0.6	0.5–5

Silicon Doped Hafnium Dioxide

Silicon doped Hafnium Dioxide (Si:HfO$_2$) is a promising candidate for FE memory technologies due to its compatibility with a CMOS process and scalability. HfO$_2$ has various crystal structures with process environments. A bulk HfO$_2$ is monoclinic, and a transition occurs from monoclinic to tetragonal at 1973 K. Then it transforms from tetragonal to cubic at 2773 K [13], [14]. All the crystal structures are determined by process temperature and pressure. Si in HfO$_2$ layer reduces stability of the monoclinic phase, and helps transition from tetragonal to orthorhombic, which is polar-phase, as shown in Figure 1.8.

Since a thin Si:HfO$_2$ layer (~10nm) relative to other FE materials is experimentally achieved [15], [16], it is more suitable for scaling of the FeFET.
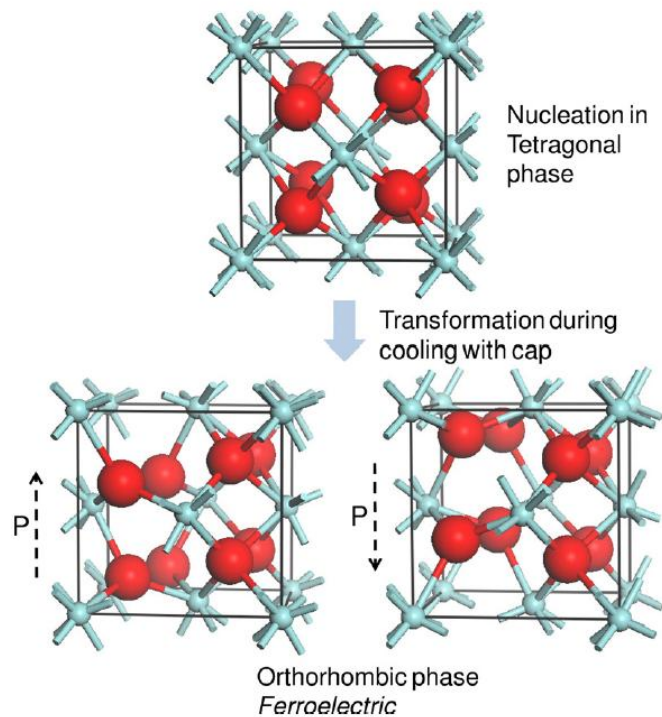
Figure 1.8. Transformation from tetragonal phase to orthorhombic phase. The two orthorhombic phases are for two polarization states. (Red: oxide atom, blue: hafnium atom) [13].

1.3.2. Resistance-based memory

Resistance-based memory is a memory device with two terminals. Unlike capacitance-based memories, the memory state is directly switched by the resistance changes caused by applied voltage or current. In general, resistance-based memories have cross-point architectures. Resistive Random Access Memory (ReRAM), Phase Change Random Access Memory (PCRAM), and Spin Transfer Torque Random Access Memory (STTRAM) are in this category.

Resistive Random Access Memory

ReRAM is one of the emerging candidates to replace flash memory technology due to its simple structure, compatibility with CMOS process, and small footprint. It has top and bottom electrodes and resistive switching material between them. The resistive changing material is either metal oxides such as $SrTiO_2$, $SrZrO_3$, TiO_2, or NiO [17]–[22] or organic materials such as 2-amino-4, 50 imidazoledicarbonitrile (AIDCN) with Al [23] and CuTCNQ [24], [25]. The resistive switching material has a high resistance state (HRS) or a low resistance state (LRS), and it is switched by the appropriate voltages, as shown in Figure 1.9. The resistive switching can be explained by a conductive filament or an interface switching.

The conductive filament model is that the resistive switching is due to forming and rupturing of the conductive filaments in the resistive switching materials. Figure 1.10
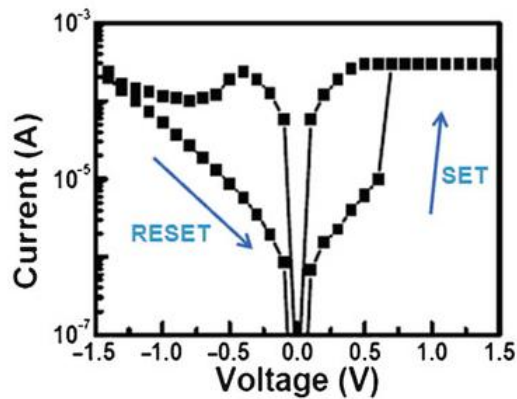
Figure 1.9 *I-V* characteristics of ReRAM. ReRAM is in LRS with high voltage (set process), and it is in HRS with voltage of opposite polarity (reset process) [20]
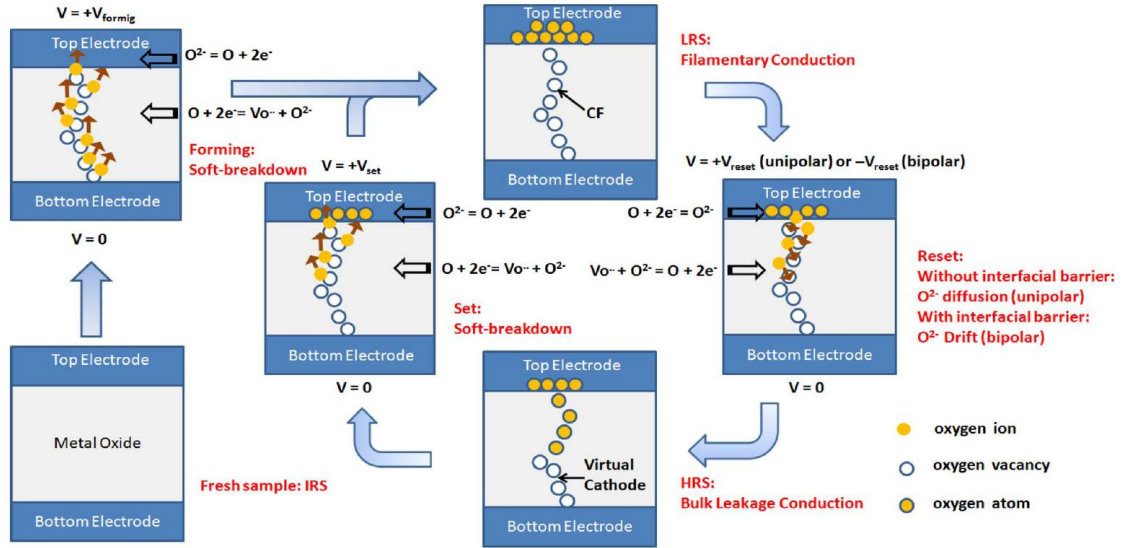
Figure 1.10 Forming and switching process of conductive filament model [21].

shows the conductive filament in the resistive switching material. An as-fabricated resistive layer does not have a conductive path in it. With a high voltage, a conductive filament is formed by dielectric breakdown. The oxide vacancies take place during this process, and they form a conductive path. During the forming process, an HRS is switched to an LRS. The rupturing process is opposite to the forming process. With a certain voltage, oxide vacancies are filled with oxide ions and the conductive filaments are ruptured, resulting in a higher resistance.

In the interface switching model, resistance switching occurs through the entire interface of the electrode and the resistive switching material. Figure 1.11 shows the schematic and energy band for the interface switching. Unlike the conductive filament model, oxide vacancies do not form a conductive path. Instead, the oxide vacancies are
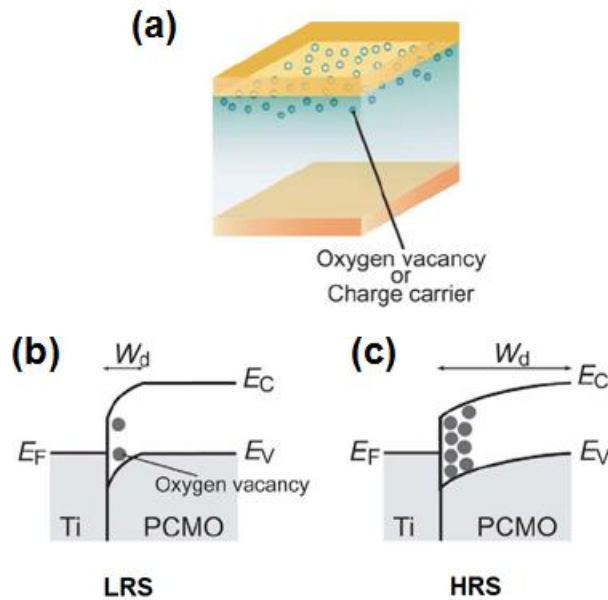
Figure 1.11 (a) Schematic of the interface switching model and energy band of (b) an LRS and (c) an HRS. Wider depletion width causes lower current (higher resistance) [22].

stacked up near the interface of the electrode and the resistive switching material. Once the oxide vacancies take place near the interface, the depletion width increases, resulting in a higher resistance. With a voltage with an opposite polarity, the oxide vacancies are filled with the oxide ions from the electrode. Thus, the depletion width decreases, resulting in a lower resistance.

The major difference between the two mechanisms is area dependency [22]. The conductive filament is independent of the device area since it is formed in a random place and the thickness of the filament is determined only by the magnitude and the pulse width of the applied voltage. However, as mentioned above, the interface switching takes

place across the entire area of the device; thus, the resistance is area-dependent. Therefore, resistance values of HRS and LRS vary with the area for the interface switching model, while resistance values of HRS and LRS are constant for the conductive filament model.

ReRAM exhibits fast operation speed and low switching energy, but it has limitations. The resistive switching mechanism is still not very clear, although there are many hypotheses, as mentioned above. In addition, ReRAM essentially requires selection devices because ReRAM is basically a resistor. Without the selection device, there would be huge leakage current through unselected memory cells called sneak current, as shown in Figure 1.12. As a consequence, data readout might be incorrect. Additionally, even with the selection devices, the leakage current through the unselected memory cells cannot be neglected because the selection device is just a nonlinear device and it does not block leakage current completely. Thus, there must be voltage drop along the wire, and the effective voltage that reaches the selected memory cell is, therefore, lower than the
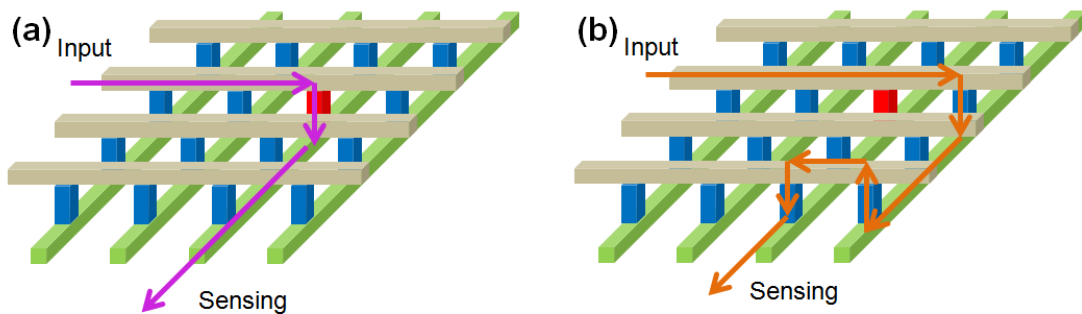
Figure 1.12 (a) access of the selected memory cell (red) and (b) an example of the sneak current through unselected memory cells (blue). Current is supposed to flow through the selected cell only, but there exist many current paths through unselected cells.

nominal input voltage. The voltage margin must be considered, including the voltage drop.

Phase Change Random Access Memory

PCRAM is another emerging memory technology using phase-change materials. Like ReRAM, it has two electrodes and a phase-change material between them. PCRAM is receiving attention owing to its simple structure, small footprint, and fast switching time [26]. The phase-change materials have either an amorphous phase or a crystalline phase, and it is switched by application of heat [27]. The amorphous phase has high resistivity, while the crystalline phase has low resistivity. A chalcogenide material such as $Ge_2Sb_2Te_5$ (GST) or an Sb-rich SbTe alloy such as Ag- and In-doped Sb_2Te (AIST) is generally used as phase-change materials [27], [28]. GST is a very reliable material since it is already widely used for rewritable CDs or DVDs.

The phase-change material becomes amorphous phase by the melting and quenching process. On the other hand, by applying current to generate heat above a crystallization temperature, the phase-change material becomes crystalline phase and the process is like annealing. The amorphous phase is considered as a RESET state and the crystalline phase is considered as a SET state. The structure and operations are depicted in Figure 1.13. Since it requires heat to change the phase, it needs a heater (which is generally made of TiN) right below the phase-change material. When external pulse is applied, the heater starts generating heat, changing the phase of the mushroom-shaped region near the contact of the heater to the phase-change material.

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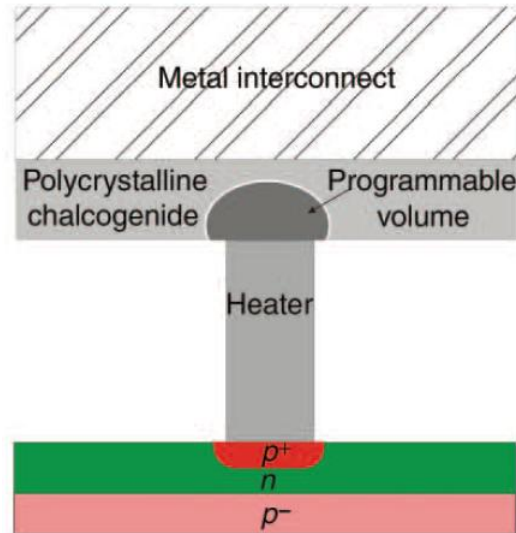
Figure 1.13 PCRAM structure and operations. The PCRAM consists of electrodes, a phase-change material (polycrystalline chalcogenide), a heater (TiN), and a selection device (diode). By means of a current through the device, the heater generates heat to change the phase of the polycrystalline chalcogenide [28].

One key property of the phase-change material is threshold voltage switching [27], [28]. Threshold voltage switching is change of conductivity of the phase-change material with an external voltage exceeding threshold voltage. With a high electric-field ($>10^5$ V/cm) inside the phase-change material, conductivity of the phase-change material increases drastically, as shown in Figure 1.14. When the phase-change material is amorphous and has high resistance, supply power is supposed to be extremely high to provide sufficient current to generate enough heat. However, due to threshold voltage switching, the heater can generate enough heat with relatively low power. With a certain
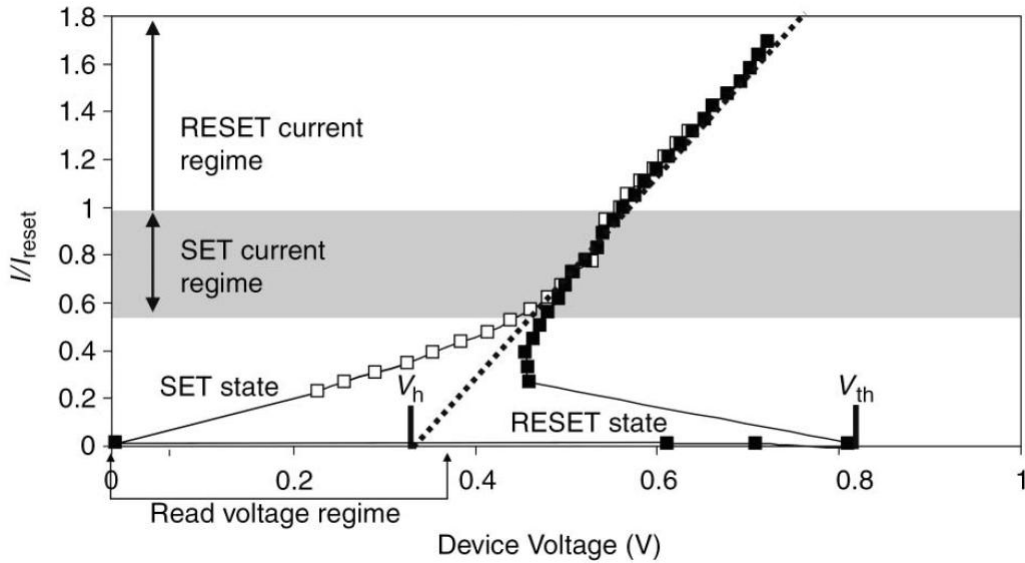
Figure 1.14 I-V characteristics of PCRAM. V_{th} and V_h are the switching threshold voltage and the holding voltage, respectively. When a high voltage ($\sim V_{th}$) is applied to the PCRAM, conductivity of the phase-change material decreases drastically [28].

voltage pulse for a relatively long time, amorphous phase turns into crystalline phase. However, if the heat is supplied for a short time, it retains its phase. When higher temperature is applied for a short time, the phase turns into amorphous phase.

Although the phase change occurs very quickly, heat generation usually takes much longer. Therefore, the actual operation for phase-change takes longer than the phase-change of the material itself.

Like ReRAM, it also needs a selection device, as shown in Figure 1.13, to prevent sneak current. The requirement of the selection device is a sufficiently high on-current to generate enough heat in the heater, and a sufficiently high nonlinearity to prevent sneak current effectively.
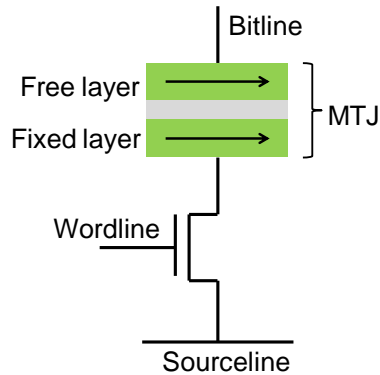
Figure 1.15 STTRAM structure. MTJ consists of an FM fixed layer, an FM free layer, and an insulator layer between the two FM layers.

Spin-Transfer Torque Random Access Memory

Spin-Transfer Torque Random Access Memory (STTRAM) is a memory that utilizes magnetic spins. STTRAM has one transistor and one magnetic tunnel junction (MTJ), as shown in Figure 1.15. The MTJ consists of two parallel ferromagnetic (FM) layers, and an oxide insulator, such as MgO and Al_2O_3, between them.

When a current is applied to the sandwiched structure, electrons move from one side to another. When the electrons pass through one FM layer, the electrons have aligned spin direction with the FM layer, as if the FM layer is a spin filter [29]–[32]. The electrons move into the insulator with the spin, and they reach another FM layer.

The MTJ has two distinguished resistance states by the giant magnetoresistance effect (GMR). The GMR is the resistance of the FM-insulator-FM structure. In the sandwiched structure, each FM layer works as a spin filter. As depicted in Figure 1.16, two FM layers are either parallel or anti-parallel. When magnetizations of the FM layers

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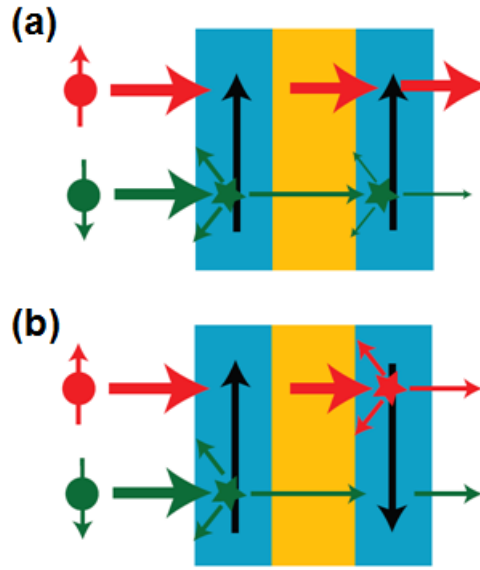
Figure 1.16 Schematic of the GMR effect. (a) Parallel magnetization of FM layers results in low resistance and (b) anti-parallel magnetization of FM layers results in high resistance [29].

are parallel, either up-spin electrons or down-spin electrons can pass through the entire structure. Thus, it shows low resistance (Figure 1.16(a)). When the magnetizations of the FM layers are anti-parallel, both up-spin electrons and down-spin electrons are blocked by either of the two FM layers. Thus, it shows high resistance (Figure 1.16(b)). The *I-V* characteristics and resistances of STTRAM are shown in Figure 1.17.

While the GMR is used for read processes, spin transfer torque (STT) effect is used for write processes. Electrons move from the left FM layer to the right FM layer, as shown in Figure 1.18(a). The electrons passing through the left FM layer are polarized, and the spin direction becomes the same as that of the left FM layer. When the electrons
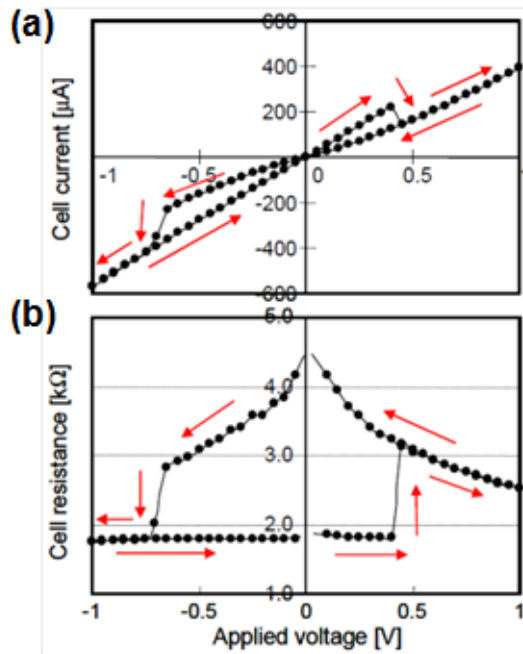
Figure 1.17 (a) *I-V* characteristics and (b) resistance of STTRAM [32].

reach the right FM layer, the magnetization of the right FM layer follows the spin direction of the electrons. In this process, some of the electrons are reflected at the interface of the insulator and the right FM layer with the anti-parallel spin of the right FM layer. When there is a pinning layer consisting of anti-ferromagnetic material on the left FM layer, the magnetization of the left FM layer is fixed, as shown in Figure 1.18(b). Negative current (from the fixed layer to the free layer) transfers spin of the left FM layer, resulting in parallel alignment, while positive current (from the free layer to the fixed layer) results in an anti-parallel alignment.
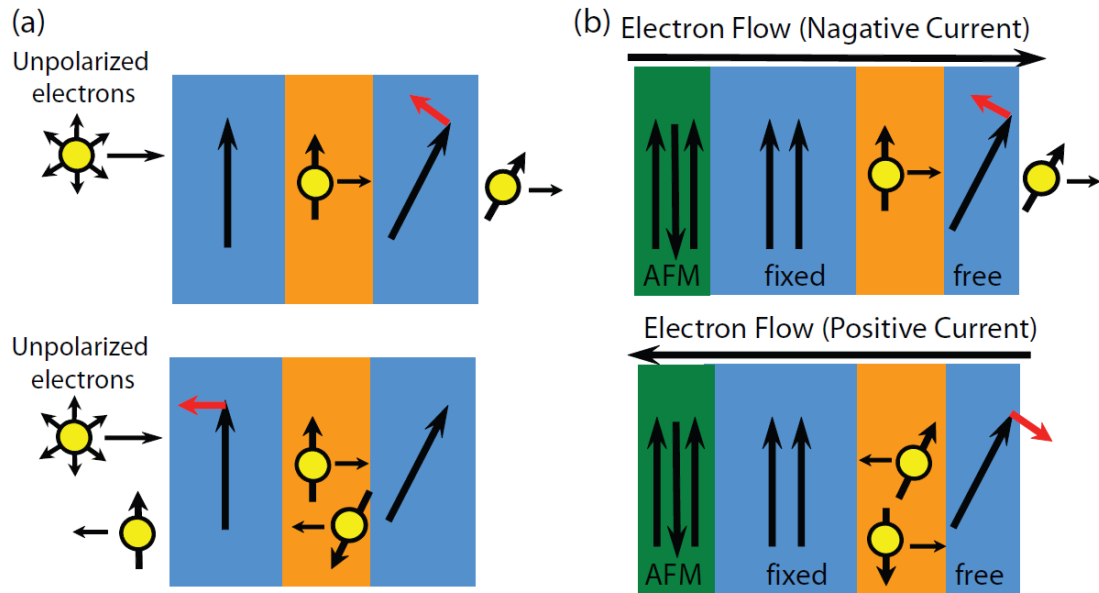
Figure 1.18 Schematic of the STT effects. (a) Spin transfer process. The left FM layer works as a spin filter and it allows one spin direction. The electron with the spin causes spin torque in the right FM layer. (b) Spin transfer process in MTJ with current. Negative current (from the fixed FM layer to the free FM layer) makes the magnetization parallel and positive current (from the free FM layer to the fixed FM layer) makes the magnetization anti-parallel [29].

1.4. Demand for Assessment and Cross-comparison of Emerging Memory Technologies

The emerging memory technologies are being widely studied to overcome the limitations of the current memory technologies and replace them. However, the studies are mainly focused on the performance of the individual memory cell [8], [27], [33]–[44];

cross comparisons between emerging memory technologies have not been done yet. Since each technology has its own advantages and disadvantages, it is very important to understand them for exploring uses in different applications. Nevertheless, different architectures of emerging memories make the cross comparisons more difficult, and lack of a proper delay model for architectures of emerging memory technologies is another major obstacle for evaluations. Thus, an accurate delay model must be constructed before any comparison, and the delay model should be applicable to any type of emerging memory.

1.5.   Ferroelectric Field-Effect Transistor as a Replacement of Flash Memory

Our delay modeling and cross comparison study shows the advantage of FeFETs over other memory technologies. Owing to the fast switching speed and NAND architecture, FeFETs have advantages over other memories in terms of operation speed especially when the array size is large. In addition to the specific advantage, FeFETs also have general advantages. The structure of FeFETs is very similar to the structure of flash memories, as mentioned in the previous section. However, the operation voltage of FeFETs is smaller than that of flash memories, since polarization takes place at lower electric field compared to the tunneling process. In addition, the ferroelectric layer in the gate stacks of FeFETs is scalable without charge leakage problems, unlike the blocking

layer of the flash memory. Therefore, FeFETs are considered as promising replacement of flash memories.

In spite of those advantages, FeFETs are not widely used because of the retention time issue [8]. In general, retention time is very critical for memory operations because it is directly related to reliability. As scaled down, FeFETs also face reliability issues faced by other memory technologies such as smaller memory window and greater interference. In order to relieve the problems, FeFETs should be studied in various aspects, including structures and dimensions.

1.6. Thesis Organization

This thesis consists of 5 chapters. Chapter 2 discusses performance comparisons between emerging memory technologies. In order to identify strengths and weaknesses of FeFET, the fundamental performances of FE and other memories are benchmarked by simulations. To simulate realistic memory applications, the comparisons are performed on an array structure. An accurate delay model is constructed and verified by benchmarking against exact HSPICE simulations.

Chapter 3 discusses an accurate model for the memory window of FeFET. Based on *P-E* hysteresis and operation voltages, a new model to calculate the memory window is introduced. Considering the real FeFET operations, memory window over time and retention time of FeFET are also investigated.

Chapter 4 discusses non-planar junctionless structures for FeFET to improve memory window and subthreshold swing. Using the suggested structures, the dimensional dependences of crucial parameters, like memory window and subthreshold swing, are studied, and key interference mechanisms are also analyzed.

Chapter 5 summarizes the thesis and its contributions, and then recommends possible future research.

Chapter 2

Array-Level Modeling and Assessment of

Emerging Memories

2.1. Introduction

As flash memory approaches its scaling limits, various novel storage class memory (SCM) technologies have emerged as possible replacements. Nevertheless, cross-comparisons between emerging memory technologies including their own architecture have not done yet. Comparative performance evaluations of these alternative technologies are needed to determine the most suitable choice(s) for different future applications. Most previous studies examine performance at the individual memory cell level [1]–[14], but in practical systems it is more important to perform array-level energy-delay assessments including wordline and bitline resistances and capacitances. Cross-comparisons of resistance and capacitance-based SCMs are particularly challenging due to their different array architectures. To our knowledge, an array-level comparison between the two has never been performed.

Although models for the array-level estimation of delay in capacitance-based

memories exist, their counterparts for resistance-based technologies do not. In this work, we build for the first time an analytical RC delay model initially for resistance-based memories which includes the contributions of all bitlines, wordlines, and individual memory cells within the array. We verify the model accuracy against HSPICE simulations and extend its applicability to both SCM categories. To complete our assessment, we also estimate and compare the energy consumption of selected SCM in both categories.

2.2. Modeling Methodology

Our ultimate goal is a generic array model suitable for an arbitrary memory technology; for specificity we initially develop our model for the case of the crosspoint architecture. We first introduce a model for interconnect delay, which we will then use to calculate energy consumption.

The overall evaluation procedure for our model is outlined in Figure 2.1. We input the resistances (R) and capacitances (C) of all relevant circuit elements in the array, including wires, memory cells, and load resistors. We illustrate the equivalent circuit model for a crosspoint memory array in Figure 2.2 without losing generality. The input parameters R_{BL}, R_{WL}, C_{BL}, C_{WL}, R_L and R_B are the bitline resistance, wordline resistance, bitline capacitance, wordline capacitance, load resistance connected to the bitline, and output resistance of the previous stage, respectively. Z_{cell} is the memory cell complex
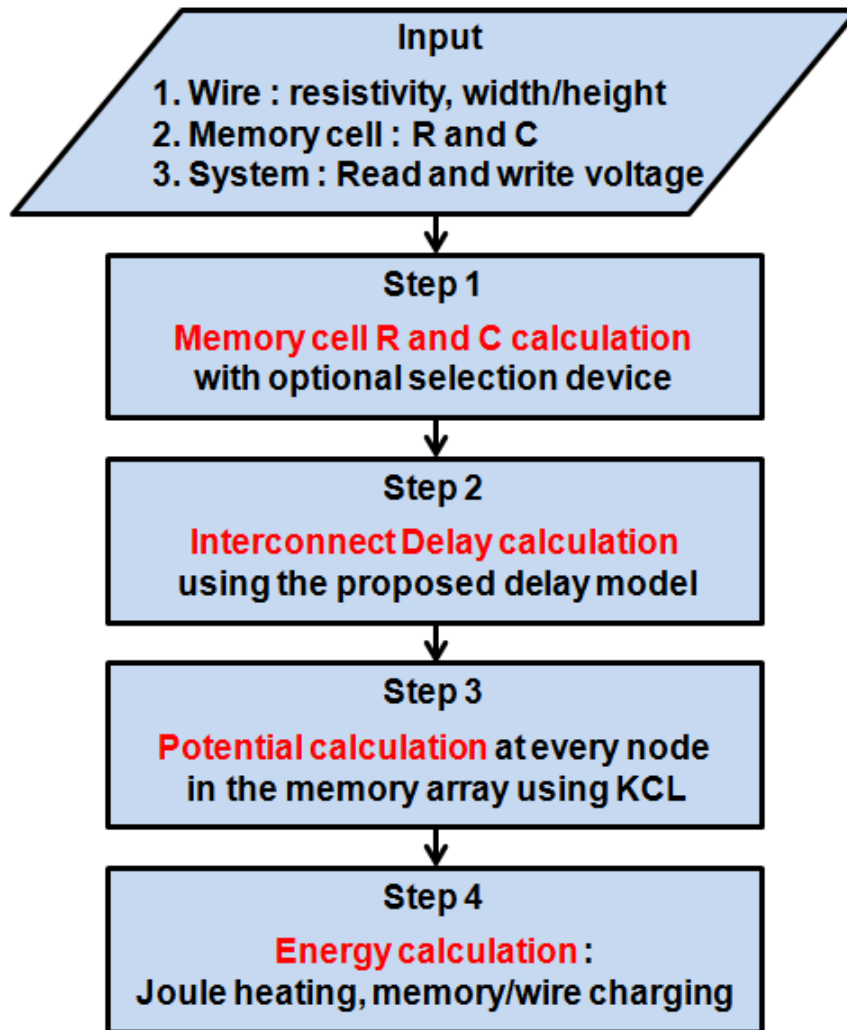
Figure 2.1 Flowchart for delay and energy consumption estimations
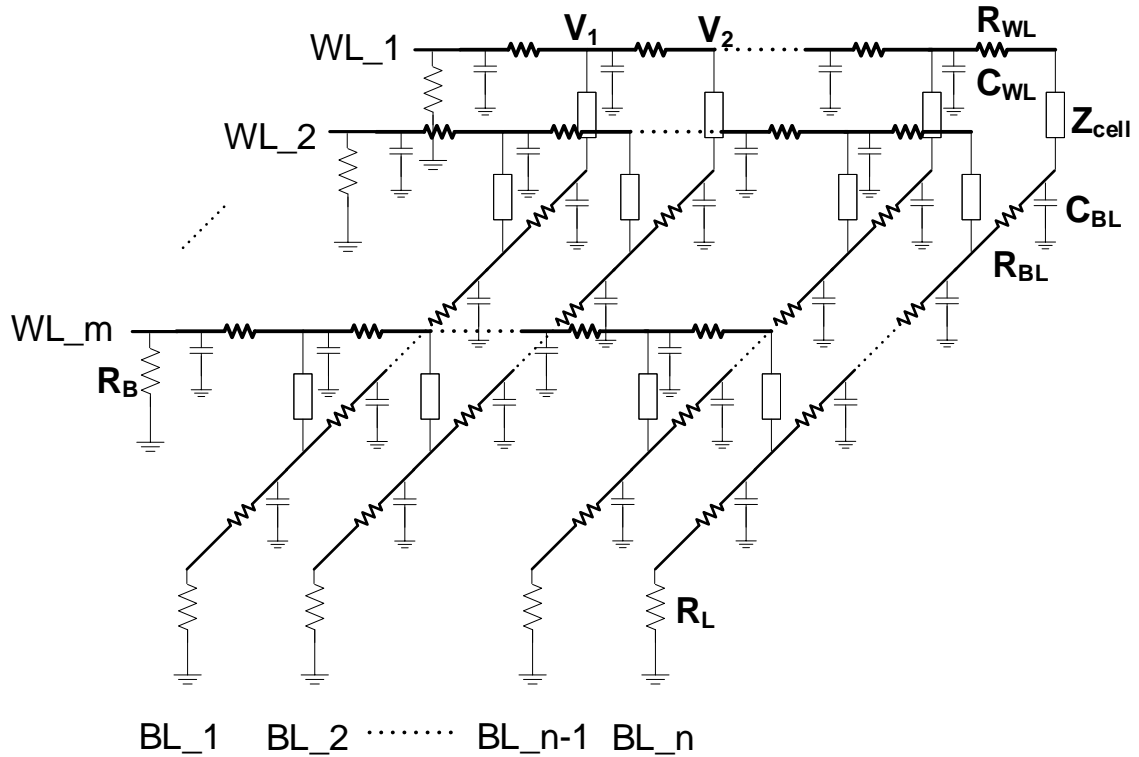
Figure 2.2 Equivalent circuit of crosspoint memory architecture. Notation is explained in the text.

impedance, which is usually some effective RC model for the specific device, such as a conductive filament switching cell or an interface switching device [15]. The effective impedance may be a function of cell area, depending on the particular device mechanism. For instance, for resistive memory cells utilizing conductive filament switching, the cell resistance R_{cell} is nearly independent of area because the width of the conductive filament is insensitive to device area. If interface switching dominates, however, R_{cell} will be area dependent since current flows through the entire memory cell area. Since the cell is an active device, in general Z_{cell} may be voltage dependent; thus, a memory device with a

nonlinear *I-V* characteristic will have a variable resistance depending on the read or write voltage. When evaluating R_{cell} for our delay calculations, we use the average resistance for the operating voltage range under consideration. In other words, for a given voltage range between V_1 and V_2 with corresponding device currents I_1 and I_2, we define $R_{cell} = (V_2 - V_1) / (I_2 - I_1)$.

It is noteworthy that practical crosspoint memories also have selection devices which are connected in series to the memory cell in order to reduce sneak currents. These selection devices are also active components such as diodes or metal-insulator transition switches with nonlinear *I-V* characteristics. As long as complete *I-V* models for both the memory and the selection devices are known, we can use them to calculate the potential at every node of the array using Kirchhoff's laws [16] and obtain the corresponding effective cell resistance which includes both the memory and selection device. For simplicity, however, we do not include selection devices in the specific calculations we present here.

2.2.1. Delay Modeling

Having obtained the effective circuit component values for the array, we can proceed to evaluate the delay. The basic equations are presented here; though they are nominally presented for one memory cell resistor (1R) crosspoint arrays as shown in the Figure 2.3, they are easily modified for other architectures as discussed below. Based on the delay of an interconnect for linear ramp signal as shown in Figure 2.4 [18]–[20], we derive the generic expression for the interconnect delay of the crosspoint architecture
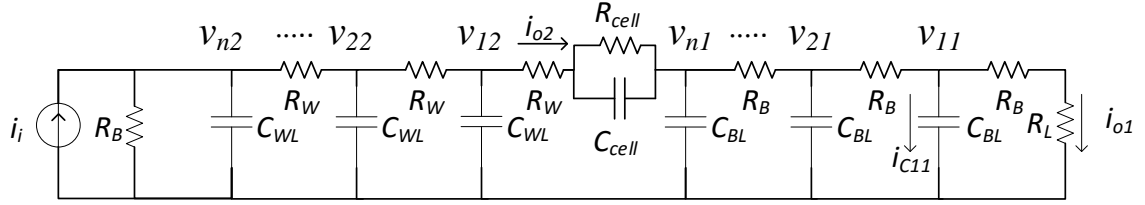
Figure 2.3 Equivalent circuit of the the selected wordline and bitline through the memory cell. R_W and R_B are the resistance of wordline and bitline per unit.
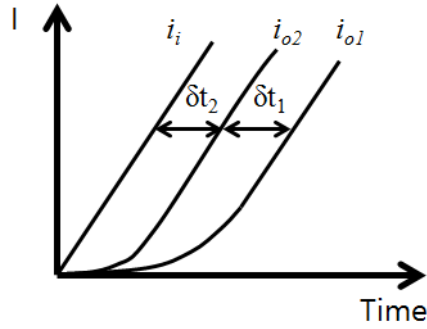
Figure 2.4 Linear ramp input signal (i_i) and the output signal through wordline (i_{o2}) and bitline (i_{o1}).

including sneak current paths. In Figure 2.3, the output signal i_{o1} is expressed as

$$i_{o1} = p_{o1}(t_2 - \delta t_1) \tag{1}$$

where t_2 and p_{o1} are the time when the signal reaches the memory cell through the wordline and the slope of the output signal, respectively. Thus, the potentials v_{11} and v_{12} are expressed as

$$v_{11} = i_{o1}(R_B + R_L) \tag{2}$$

$$v_{21} = v_{11} + (i_{o1} + i_{C11}) \times R_B \tag{3}$$

By repeating the procedures for the rest of the nodes on bitlines, v_{n1} and i_{n1} are expressed as

$$v_{n1} = i_{o1}R_{BL} + i_{o1}R_L + p_{o1} \cdot \frac{C_{BL}R_{BL}}{2} \cdot \frac{R_{BL}}{3} + p_{o1} \cdot \frac{C_{BL}R_{BL}}{2} \cdot R_L \tag{4}$$

$$i_{n1} = i_{o1} + p_{o1} \cdot \frac{C_{BL}R_{BL}}{2} + p_{o1} \cdot C_{BL}R_L \tag{5}$$

With the results, we can continue the same procedures for the wordline delay, and the total interconnect delay through the wordline and bitline is expressed as

$$\text{Interconne ct delay} = \frac{\left[\frac{C_{BL}R_{BL}}{2}\left(1 + \frac{R_{WL} + R_{eff}}{R_B{'}} + \frac{\frac{R_{BL}}{3} + R_L}{R_B{'}}\right) + C_{BL}R_L\left(1 + \frac{R_{WL} + R_{eff}}{R_B{'}}\right) \\ + \frac{(C_{WL} + C_{cell}) \cdot R_{WL}}{2} \frac{R_{BL} + R_L}{R_B{'}} + (C_{WL} + C_{cell}) \cdot (R_{BL} + R_L) \right]}{1 + \frac{R_{WL} + R_{eff}}{R_B{'}} + \frac{R_{BL} + R_L}{R_B{'}}}$$

$$+ \frac{\left[\frac{(C_{WL} + C_{cell}) \cdot R_{WL}}{2}\left(1 + \frac{\frac{R_{WL}}{3} + R_{eff}}{R_B{'}}\right) + (C_{WL} + C_{cell}) \cdot R_{eff} \right]}{1 + \frac{R_{WL} + R_{eff}}{R_B{'}} + \frac{R_{BL} + R_L}{R_B{'}}} \tag{6}$$

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where R_{eff} is the effective resistance of the element at the crosspoint. For crosspoint architecture with one selection diode and one memory resistor (1D1R) in each cell, R_{eff} in (6) is given by the combined resistance of R_{cell} and diode resistance in series. $R_B{}'$ is the parallel resistance of R_B and total resistance of the unselected memory cells, and it is

$$R_B{}' = R_B \parallel \frac{R_{cell} + \dfrac{n(n-1)}{2} \cdot R_{WL}}{n + \dfrac{R_{WL}}{R_{cell}} \cdot \left(\dfrac{1}{2} \cdot \dfrac{n(n+1)(2n+1)}{2} - \dfrac{1}{2} \cdot \dfrac{n(n+1)}{2} \right)} \tag{7}$$

where n is the number of columns.

Our model of the interconnect delay utilizes several approximations which we outline here. First, the array delay is calculated using the "worst case scenario" when the accessed target cell is the one farthest away from the wordline voltage source and the bitline sensing amplifier. Unselected memory cells are also assumed to be in the high resistance state (HRS) as the delay is longest in this scenario. Second, we used the distributed RC model for the interconnect delay. There are two possible ways for calculating the interconnect time constant, based on lumped and distributed RC models. As technologies scale down, the parasitic effects of the wires become greater and interconnect delay estimations using single lumped RC components become inaccurate [17]. Our calculation builds on an infinite number of distributed RC components rather than a single lumped RC component, and it accounts for the effects of sneak current paths,

which were previously neglected for the single wire.

For the assessment in the next section, the read time is defined as the sum of the interconnect delay and evaluation time, and the write time is defined as the sum of the interconnect delay and memory switching time. The operation delay and energy consumption of other circuitries such as multiplexers and amplifiers are not considered because our assessment purpose is to compare the interconnect delay of various types of SCM cells and architectures at the array-level.

2.2.2. Energy Consumption Modeling

Based on the results from the delay model, the energy consumption in the memory array is calculated from the voltage and current at each node. The energy consumption in the array is expressed as

$$\text{Energy Consumptio n} = I \times V \times t + 0.5 \times C \times V_{wire}^{2} + 0.5 \times C \times V_{cell}^{2} \tag{8}$$

where the first term is Joule heating energy which is the product of current, voltage and time for the entire wordlines and bitlines. The second and the third terms are the wire charging energy and the memory cell charging energy where V_{wire}, V_{cell} and C are the voltage difference between V_1 and V_2 in Figure 2.2, the voltage applied to the memory cell, and the wordline or bitline capacitance, respectively. To estimate the charging energies of the wire and memory cell capacitor, an infinite number of distributed wire

capacitors and resistors are assumed rather than simple lumped capacitances and resistances. With a distributed model for the unit wordline or bitline, the second term of (8) becomes

$$\text{Wire charging energy} = \frac{1}{2} \cdot C \cdot V_1^2 + \frac{1}{6} \cdot C \cdot (V_1 - V_2)^2 - \frac{1}{2} \cdot C \cdot V_1 (V_1 - V_2) \qquad (9)$$

The charging energy of the memory cell is simply calculated, but the voltage at each node is not identical because of the wire resistance. Since voltages at all nodes and the wire resistances and capacitances are known, Joule heating energy and the charging energy can be calculated. By adding the energy consumed in every unit wire and every unit memory cell in the array, the model includes dissipation from all sneak current paths.

2.2.3. Model Verification

We have verified the interconnect delay model with HSPICE simulations. Figure 2.5(a) compares the computed and simulated delays as a function of the number of bitlines and Figure 2.5(b) compares those for different feature sizes, showing good agreement between the two. As expected, the interconnect delay increases with the number of bitlines or feature size due to larger wire resistance and capacitance.

Although the delay model originates from the crosspoint architecture, it could be applied to other memory architectures by adding a proper term. For NAND architecture, the memory cell itself is replaced with a transistor. When the access
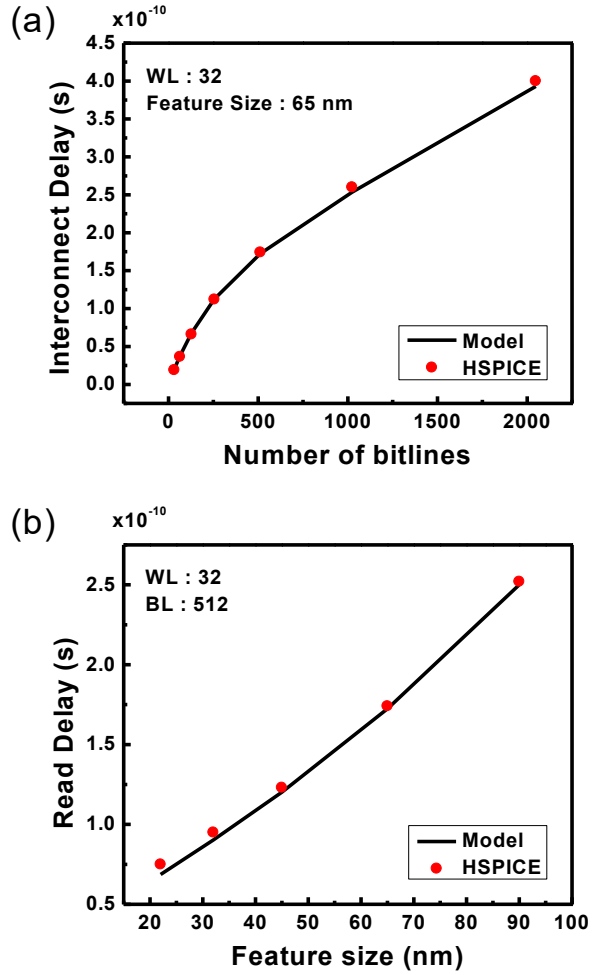
Figure 2.5 Model verification against HSPICE as a function of (a) the number of bitlines and (b) a feature size with crosspoint architecture.

transistor gate leakage is assumed to be negligible, R_{eff} becomes infinite. To extend (6) for a 1T1R architecture, the memory cell is also replaced with a transistor which output resistance is modeled as R_{tr}, and $C_{BL}(R_{BL} + R_{cell}' + R_L + R_{tr})$ is added where R_{cell}' accounts for the resistance of the memory cell which is connected to the access transistor. In the same manner as NAND, R_{eff} is also infinite since there is no current from the gate to the
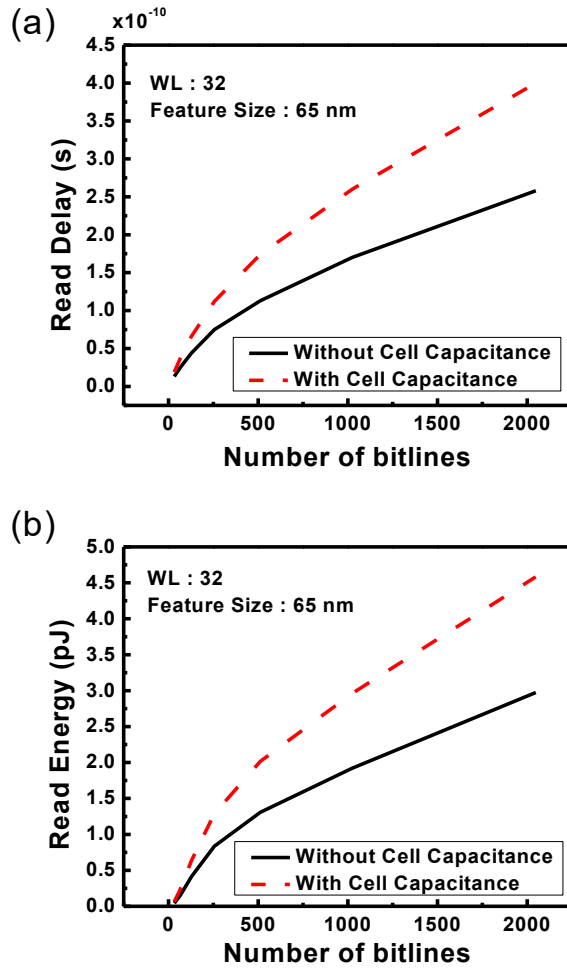
Figure 2.6   (a) The read delay and (b) the energy consumption of crosspoint architecture with and without cell capacitances. With the number of bitlines, the impact of the cell capacitance increases.

substrate.

As mentioned previously, our model accounts for the capacitance of the memory cell in the crosspoint architecture; this capacitance is relatively unimportant for individual cells, but becomes significant for delay and energy consumption at the array level. Such impact on the delay and energy estimations for resistance-based memories is

evaluated using the derived model in Figures 2.6(a) and (b). When the array size is small, the discrepancies of delays and energy consumptions with and without the memory cell capacitance are not notable. As the array size increases, however, the delay and energy consumption due to the cell capacitance increase. As the total cell capacitance becomes comparable to the total wire capacitance, the delay considering the cell capacitance is greater than the delay neglecting that.

2.3. Delay Estimation

Using our delay model, we have estimated the read and write time for three different types of memories: a FeFET capacitance-based memory with the NAND architecture, and ReRAM and PCRAM resistance-based memories using the crosspoint architecture. We lifted the parameters, as listed in Table 2.1, for the assessments from experimental data [9], [14] and simulations. If the memory cell resistance is not much greater than the wordline and bitline resistances, the voltage drop along the wire is significant especially in a large array size so the effective voltage applied to each memory cell becomes smaller than the supply voltage [16]. Therefore, one important criterion for a resistance-based memory is that the cell resistance must be at least several megaohms to avoid the voltage margin issue. We emphasize that the results of our delay estimation and comparison do not conclude if one memory type or architecture is superior in general to the others because the assessment results are specific to the sets of input memory

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Table 2.1 Memory parameters

Memory /Architecture	Parameters	Numerical Values
PCRAM [14] /1R crosspoint	Resistance (LRS)	$6.6 \times 10^5 \ \Omega$
	Resistance (HRS)	$6.6 \times 10^6 \ \Omega$
	Read Voltage	0.65 V
	Write Voltage	1.3 V
	Switching Time	200 ns
	Switching Energy	1×10^{-15} J
ReRAM [9] /1R crosspoint	Resistance (LRS)	$2.5 \times 10^7 \ \Omega$
	Resistance (HRS)	$7.2 \times 10^8 \ \Omega$
	Read Voltage	2 V
	Write Voltage	6 V
	Switching Time	1 ns
	Switching Energy	5×10^{-18} J
FeFET /NAND	Read Voltage	0.7 V
	Write Voltage	10 V
	Precharge Voltage	2 V
	Evaluation Voltage	1.5 V
	Pass Voltage	2 V
	Threshold Voltage	0.7 V
	Switching Time	1 ns
	Switching Energy	5×10^{-16} J

parameters.

Figure 2.7(a) and (b) show the read and write times as a function of the feature size and number of bitlines, respectively. For Figure 2.7(a), the numbers of wordlines and bitlines are fixed to 32 and 512, respectively. The capacitance-based memory and the resistance-based memory have opposite read time trends as the feature size decreases. FeFET with NAND architecture needs an evaluation time CV/I for the read operation with. As feature size decreases, the cell current is reduced, resulting in longer evaluation time. The read time of the resistance-based memory, however, is purely determined by
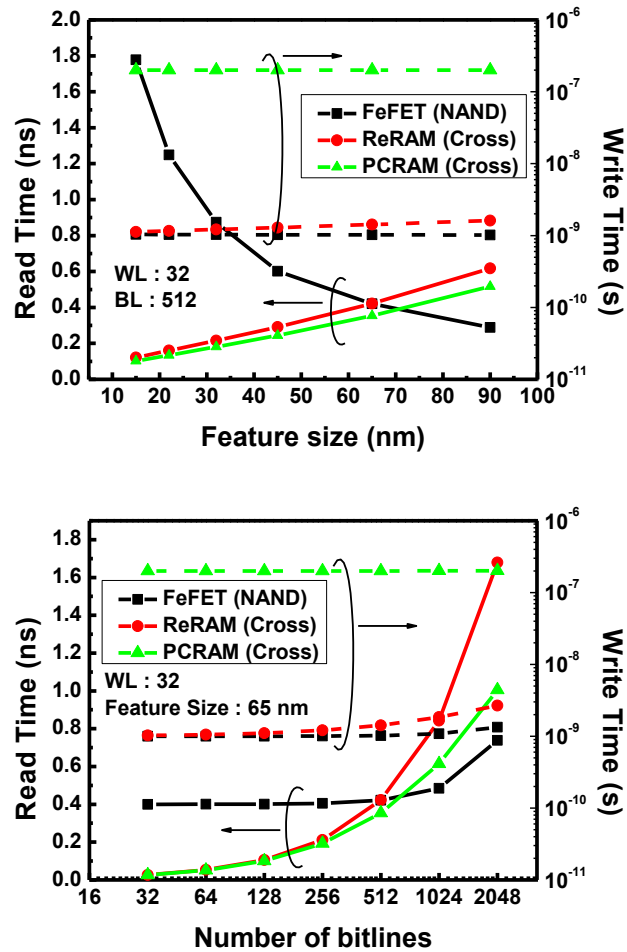
Figure 2.7 Write and read time as a function of (a) the feature size and (b) the number of bitlines.

the RC time constant, so it decreases as the feature size decreases. The write time is also evaluated in the same manner. For FeFET, the write time is relatively flat compared to the read time as shown in Figure 2.7(a). The main factor that determines the write time is switching time. For PCRAM, the switching time is a few hundred nanoseconds, so it is much greater than the wire delay and dominates write time. In ReRAM and FeFETs, the

switching time is also greater than the interconnect delay but is on the order of nanoseconds, leading to significantly shorter write times than PCRAM. However, the ReRAM shows slightly greater write time than the FeFET. This is because the resistance-based memory must allow a current from the wordline to the bitline in any state, while current does not flow from the wordline to bitline in capacitance-based memories. Therefore, the wordline delay of the capacitance-based memory is shorter than sum of the wordline and bitline delay of the resistance-based memory.

For Figure 2.7(b), the feature size is 65 nm and the number of wordlines is 32. In general, the read time of a smaller array is shorter because of the smaller RC constant. However, for the FeFET, the read time is almost constant below 512 bitlines because the evaluation time is greater than the interconnect delay and independent of the number of bitlines, becoming the limiting factor. Comparing PCRAM with ReRAM, the read time of PCRAM is slightly shorter because the memory cell resistance of PCRAM is lower in this assessment. However, as mentioned at the beginning of this section, this does not necessarily mean that PCRAM will always be faster than ReRAM because it depends on the input parameters. The write time as a function of the number of bitlines is also in Figure 2.7(b). As the number of the bitlines increases, the total write time increases due to the greater resistance and capacitance of the array. In short, the write time of capacitance-based memory and the resistance-based memory are dominated by the switching time.
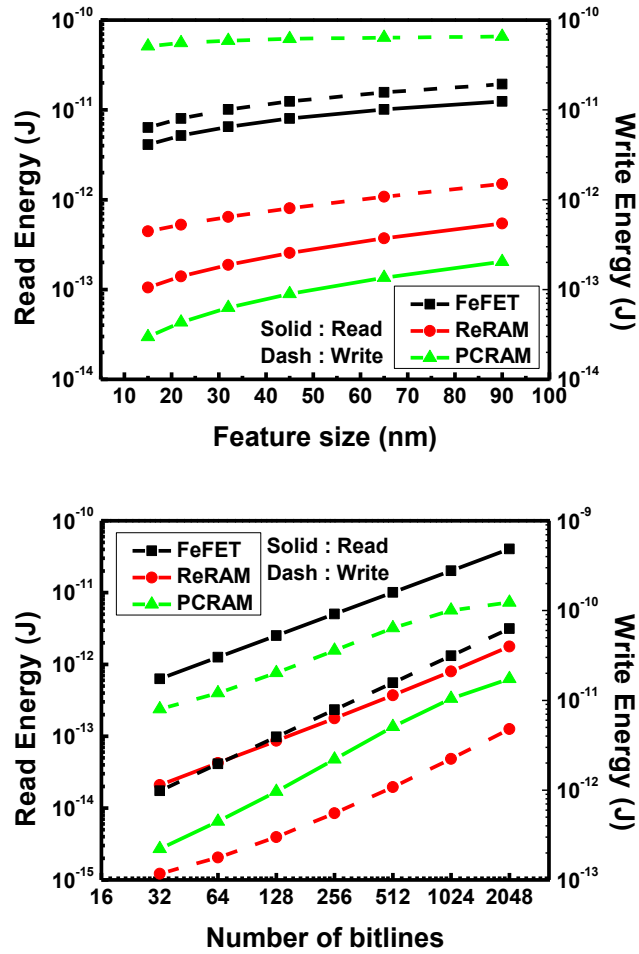
Figure 2.8 Write and read time as a function of (a) the feature size and (b) the number of bitlines.

2.4. Energy Consumption Estimation

Figure 2.8(a) and (b) show the read and write energy as a function of the feature size and the number of bitlines. As discussed in the modeling section, the read

energy and write energy consist of Joule heating, wire charging and memory cell charging energy. The read and write time obtained by the proposed model are used to calculate Joule heating energy. In read operation, FeFET has much greater energy consumption compared with the two other memories because the capacitance-based memory has a NAND architecture and pass voltage must be applied to all unselected wordlines during evaluation, unlike the resistance-based memory. Due to the charging energy of the unselected memory cells and unselected wordlines, the read operation energy consumption of the capacitance-based memory is much greater than that of the resistance-based memories. As the feature size decreases, the read operation energy consumption also decreases as shown in Figure 2.8(a) owing to smaller wire capacitances and memory cell capacitances.

The write energy is also pictured in Figure 2.8(a) and it shows that PCRAM has the largest energy consumption. The dominant factor of the total energy consumption for the resistance-based memory and the capacitance-based memory is different though. PCRAM requires very long write times to generate enough heat to switch states, so Joule heating energy is dominant. Since such write times barely change with the feature size, the write energy is not changed much accordingly. The capacitance-based memory such as FeFET and flash memory generally require high write voltage, so the cell charging energy is dominant and it is much greater than that of the resistance-based memory. On the other hand, Joule heating energy of FeFET is smaller than that of the resistance-based memory because the capacitance-based memory does not have current flowing from the wordline to the bitline. In read and write operations, Joule heating energy is much smaller

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than the cell charging energy if the operation time is short, so the total energy consumption is mainly determined by the operation voltages.

Also, it is obvious that the larger memory array consumes more energy, as seen in Figure 2.8(b). In this assessment, the read voltage of PCRAM is smaller than that of ReRAM. Also, the cell resistances of ReRAM is greater than that of PCRAM, thus the reading time is greater resulting in greater Joule heating energy. Therefore, PCRAM consumes less energy than ReRAM in this assessment with given experimental parameters.

2.5. Summary

We develop a general analytical RC delay model taking into account the sneak current paths and verify it against HSPICE simulations; we extend our framework to calculate energy consumption as well. In order to assess the advantages and disadvantages of the emerging memories within a given architecture, memory delay performance and energy consumption are cross-compared. From our comparison results, we see the advantage of FeFETs in operation delay. In addition, we can identify the advantages and disadvantages of each memory category. Within this comparison study, we also analyze the general scaling trends of capacitance-based and resistance-based memories.

Chapter 3

Modeling Memory Window of Ferroelectric

Field-Effect Transistor

3.1. Introduction

Memory window is an important feature that determines the stability and reliability of memory states, which also in turn affects the memory retention time. The memory window of a FeFET has been defined as the flat band voltage difference (ΔV_{FB}) or threshold voltage difference (ΔV_{th}) between the program and erase states. Under large gate bias, it has been expressed as $2E_C \times t_F$, where E_C and t_F are the coercive field and thickness of the ferroelectric layer, respectively [1]–[5]. However, this formulation computes the widest possible memory window which occurs only under large external bias. In many applications, the supply voltage ceiling prevents a FeFET from attaining such maximum. Thus, the memory window expression under small external bias is developed [6]. However, this memory window expression has several limitations. First, ΔV_{FB} does not mean the actual memory window because the difference of the required external bias to form strong inversion might be different from ΔV_{FB}. As the capacitance

of ferroelectric varies with external bias, ΔV_{th} is more accurate definition for memory window. Second, the *P-E* expressions under small external bias are not suitable for program and erase voltages of different absolute values which are common in the real operations.

In this chapter, we propose a new memory window model for FeFET with much better accuracy. Our model takes into account the FeFET's ferroelectric hysteresis, device dimensions, and ferroelectric material properties and the symmetric/asymmetric operation voltages. Also, by applying time-varying remanent polarization (P_R), the proposed model estimates retention property of FeFETs precisely. We verify the model via both simulations and experiments, showing very good agreement.

3.2.   Model Development

Without losing generality, we develop our memory window model based on an *n*-channel metal-ferroelectric-insulator-semiconductor (MFIS) FET as shown in Figure 3.1. Note that the resultant model equations would also be applicable to *p*-channel FeFET with appropriate sign changes.

When an external gate voltage (V_g) is applied, the corresponding potential drops across the MFIS stack are expressed as

$$V_g - V_{FB} = V_F + V_I + \phi_S \tag{1}$$
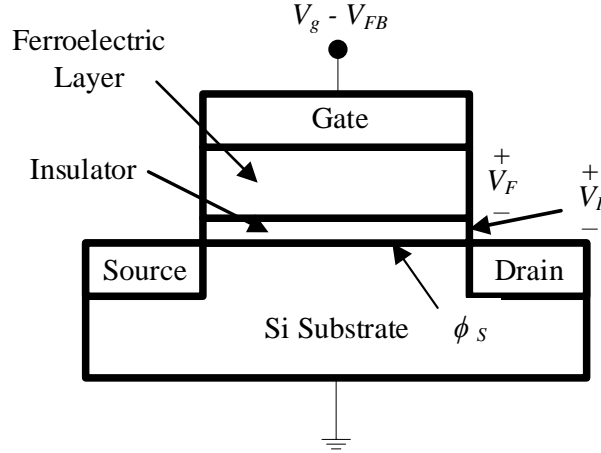
Figure 3.1 The metal-ferroelectric-insulator-semiconductor (MFIS) structure. ϕ_S, V_F, and V_I are surface potential, voltage drop across ferroelectric and voltage drop across insulator, respectively.

where V_{FB}, V_F, V_I, and ϕ_S are respectively the flat band voltage, ferroelectric voltage, insulator voltage and semiconductor surface potential as labeled in Figure 3.1. Based on Gauss's law, the electric displacement fields of different layers are inter-related as

$$\varepsilon_F \varepsilon_0 E_F + P(E_F) = \varepsilon_I \varepsilon_0 E_I = \varepsilon_S \varepsilon_0 E_S \tag{2}$$

where ε's, E's, and $P(E_F)$ are the respective dielectric permittivities, electric fields, and nonlinear polarization of the ferroelectric layer. From (1) and (2), we can define memory window as the voltage difference between *I-V* characteristics of the program and erase states. Therefore, it is generally calculated from ΔV_{FB} or ΔV_{th}. Under strong inversion conditions, V_{th} for two states are expressed as

$$V_{th1} = V_{FB1} + \frac{\sqrt{4\varepsilon_S\varepsilon_0\phi_B qN} - P(E_{F1})}{C_{F1}} + V_I + \phi_S$$

$$= \phi_{ms} - \frac{P_{R1}}{C_{F1}} + \frac{\sqrt{4\varepsilon_S\varepsilon_0\phi_B qN} - P(E_{F1})}{C_{F1}} + V_I + \phi_S$$

$$V_{th2} = V_{FB2} + \frac{\sqrt{4\varepsilon_S\varepsilon_0\phi_B qN} - P(E_{F2})}{C_{F2}} + V_I + \phi_S$$

$$= \phi_{ms} - \frac{P_{R2}}{C_{F2}} + \frac{\sqrt{4\varepsilon_S\varepsilon_0\phi_B qN} - P(E_{F2})}{C_{F2}} + V_I + \phi_S$$

(3)

where C_F is ferroelectric capacitance. The numbers in subscript denote two memory states. Thus, ΔV_{th} is given as

$$\Delta V_{th} = \Delta V_{FB} + \left(\frac{\sqrt{4\varepsilon_S\varepsilon_0\phi_B qN} - P(E_{F1})}{C_{F1}} - \frac{\sqrt{4\varepsilon_S\varepsilon_0\phi_B qN} - P(E_{F2})}{C_{F2}} \right)$$

(4)

The ferroelectric capacitance varies with external gate bias. In addition, polarizations under threshold condition ($P(E_{F1})$ and $P(E_{F2})$) also vary with external gate bias. Therefore, the parenthesis term in (4) is nonzero unlike conventional MOSFETs. As memory window, ΔV_{th} include variable ferroelectric capacitances, while ΔV_{FB} assumes the ferroelectric capacitance to be constant. Therefore, thus ΔV_{th} gives more accurate memory window results than ΔV_{FB}.

From (1) and (2), we obtain a general form of the voltage equation as

$$V_g - V_{FB} = \left(\frac{\varepsilon_F}{\varepsilon_I} t_I + t_F\right) E_F + \frac{t_I}{\varepsilon_I \varepsilon_0} P(E_F) + 2\phi_B \tag{5}$$

where t_F and t_I are the ferroelectric and insulator thickness, respectively. In general, the applied programming voltage is larger than the FeFET threshold voltage (V_{th}) such that ϕ_S becomes slightly larger than $2\phi_B$, where ϕ_B is the potential offset between the Fermi level and intrinsic energy level. Without losing accuracy, we approximate ϕ_S to be pinned at $2\phi_B$ when the channel is strongly inverted. Alternatively, the erasing voltage brings about channel surface accumulation and causes slight energy band bending; we similarly approximate here a channel flat band condition under this usually large negative gate bias.

From (5), we can obtain E_F and $P(E_F)$ at the applied gate bias for either programming or erasing. The basic form of $P(E_F)$ is given [7]–[9] as

$$P(E_F) = \pm P_S \tanh\left(\frac{\pm E_F - E_C}{2\delta}\right) \tag{6}$$

and

$$\delta = \frac{E_C}{\ln\left(\dfrac{1 + \dfrac{P_R}{P_S}}{1 - \dfrac{P_R}{P_S}}\right)} \tag{7}$$
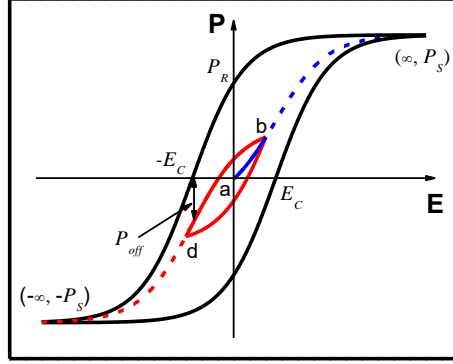
Figure 3.2 Polarization-Electric field (*P-E*) hysteresis for saturated case (black line) and minor loop (red line). The first sweep is following a blue line. For the minor loop, the starting point is origin (a) and the curve passes through b, d and goes back to b. The turning point b and d is corresponding to the maximum and minimum applied voltage.

where P_S is the saturation polarization of the ferroelectric layer, and E_C is the coercive field. When $|E_F|$ is much larger than $|E_C|$, the saturated *P-E* hysteresis is obtained (i.e. solid loop in Figure 3.2), and in which case $P(E_F)$ is simply P_S.

Nevertheless, if $|E_F|$ corresponding to the applied V_g for programming (or erasing) is not much larger or even less than $|E_C|$, the *P-E* hysteresis no longer saturates and instead manifests itself as a minor loop inside as illustrated in Figure 3.2. In this case, (6) is inadequate and we need to modify it to accommodate the minor loop as

$$P(E_F) = \pm c \cdot P_S \tanh\left(\frac{\pm E_F - E_C}{2\delta}\right) + P_{off} \tag{8}$$

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where c and P_{off} are scaling factor and polarization offset, respectively, which are dynamically determined by the 2 recent turning points of the minor loop as illustrated below.

Starting from the origin (i.e. point a in Figure 3.2), the P-E trace follows the blue dashed trajectory of a fresh device toward (∞, P_S) for programming, allowing us to obtain the respective set of c and P_{off} values for (8). By substituting (8) into (5), we can compute the E_F value corresponding to the applied programming V_g (i.e. point b). When an erasing V_g of opposite polarity is then applied, the P-E trace moves away from point b and toward (-∞, -P_S) along the red dashed trajectory which is again modeled using (8) with a new set of c and P_{off} values. Similarly, we can get the corresponding E_F value for erasing (i.e. point d) via substituting the new (8) into (5). Once this minor loop in solid red is defined, we can use it to obtain all subsequent P-E hysteresis loops. Since the minor loop is defined by the two latest turning points, this P-E relation can define minor loops for both symmetric and asymmetric V_g.

With the obtained $P(E_F)$ expressions from either the saturated P-E hysteresis or the minor loop, (4) becomes

$$\sqrt{4\varepsilon_S\varepsilon_0\varphi_B qN} = \varepsilon_F\varepsilon_0 E_{F1,2} + P(E_{F1,2}) \qquad (9)$$

with V_{th}. N is substrate doping concentration and

$$MW = \Delta V_{th} = \left(E_{F1} - E_{F2} \right) \times t_F \tag{10}$$

where E_{F1} and E_{F2} are electric field inside the ferroelectric layer corresponding to gate

bias of two different V_{th} due to hysteresis.

3.3. Memory Window Calculation Results

3.3.1. Memory Window Estimation and Verification

Simulation is done with Sentaurus TCAD [10] and the simulated structure is a

basic MFIS structure with the gate length of 32 nm as shown in Figure 3.1. The

simulation parameters for P(VDF-TrFE) is shown in Table 3.1 [11]. To mimic the

Table 3.1   Simulation parameters

Symbol	P(VDF-TrFE)	Si:HfO$_2$	Description
P_s (μC/cm^2)	12	9.5	Saturation polarization
P_r (μC/cm^2)	8	6	Remanent polarization
E_c (MV/cm)	1.3	1.1	Coercive field
Q_f (cm^{-3})	2.5×10^{18}	1×10^{17}	Fixed charge of FE
D_{it} (cm^{-2})	1.0×10^{11}	1.0×10^{11}	Si/SiO$_2$ interface trap density
ε_f	10	32	FE dielectric constant
A	2.11	2.11	Surface roughness scattering coefficient
B	1×10^7	1×10^7	Acoustic phonon scattering coefficient
C	400	400	Acoustic phonon scattering coefficient
ν	2	2	Coulomb scattering coefficient
γ	1	1	Coulomb scattering coefficient

realistic P(VDF-TrFE) layer from spin coating, non-ferroelectric layers of 2.5 nm with the same dielectric constant as P(VDF-TrFE) are added at the top and the bottom of the ferroelectric material. For the simulation, t_F and t_I are are 10 nm and 2 nm, respectively. Figure 3.3(a) shows memory window from simulation, the proposed model in this paper using ΔV_{th}, and ΔV_{FB}. For the simulations, memory window is extracted using constant current of 10^{-7} A/µm. For the saturated $P\text{-}E$ case, write and erase voltages are 100 V and -100 V, respectively. Both ΔV_{th} and ΔV_{FB} show good agreement (error ~10 %), because the device operates in saturated $P\text{-}E$ region. In this case, the parenthesis term in (4) is negligibly small. For the minor loop case, write and erase voltages are 15 V and -15 V, respectively. Unlike the saturated $P\text{-}E$ case, the proposed model shows better result since the minor loop is not symmetric with respect to origin so that the C_F and $P(E)$ in (4) are not identical.

Figure 3.3(b) is memory window comparison with experimental data. For FeFET with silicon doped hafnium dioxide (Si:HfO$_2$), t_F and t_I are 9 nm and 1.2 nm, respectively [12]. The simulation parameters for Si:HfO$_2$ are shown in Table 3.1. Write and erase voltages are 5 V and -5 V, respectively. With the given parameters, the proposed model shows good agreement. Since the $P\text{-}E$ is not completely saturated, ΔV_{FB} has greater error. For FeFET with P(VDF-TrFE), t_F and t_I are are 40 nm and 10 nm, respectively [11]. Write and erase voltages are 12.5 V and -7.5 V, respectively. Since t_I is thicker than that of the Si:HfO$_2$ case, E_F is not high enough to form saturated $P\text{-}E$. Consequently, the device operates with minor $P\text{-}E$ loop and ΔV_{FB} becomes inaccurate. However, as the proposed model can take any $P\text{-}E$ shape into account, it can estimate
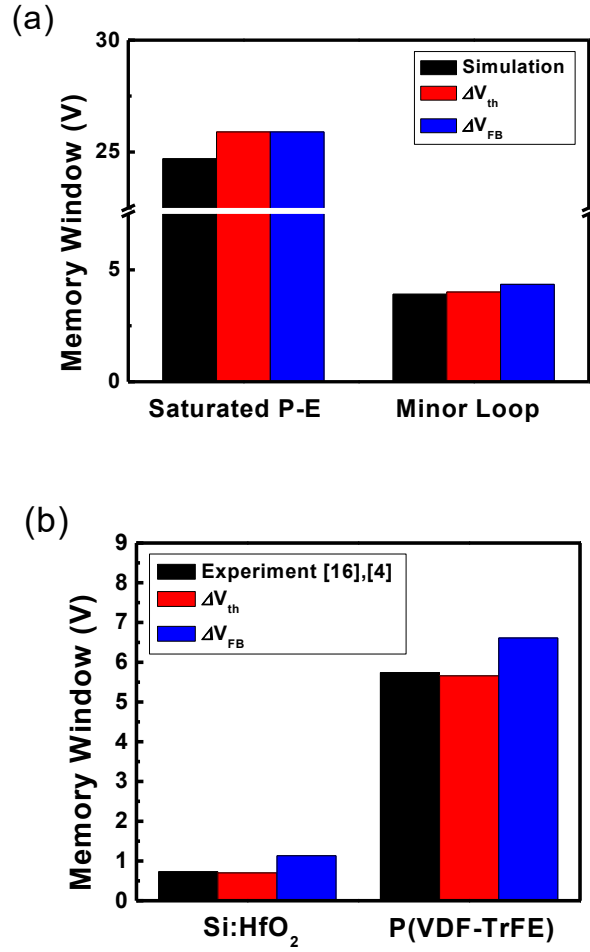
Figure 3.3 The MW comparisons with (a) simulation and (b) experiment. The device has either Si:HfO$_2$ gate oxide [12] or P(VDF-TrFE) [11]. The proposed model using ΔV_{th} predicts MW precisely. MW from ΔV_{FB} has larger error especially when the hysteresis forms the minor loop with asymmetric turning points.

memory window accurately.

In this modeling, fixed charge inside the ferroelectric layer is not included. If fixed charge is included, *P-E* hysteresis is shifted horizontally. It can be considered in *P-E* extractions from (6) to (10) and the model does not lose generality.

3.3.2. Polarization Retention and Memory Window

The proposed memory window is calculated right after program or erase operation. However, due to depolarization field in FeFETs, remanent polarization P_R diminishes [13], thus memory window is reduced over time. Lou developed a polarization retention model [14], and the model predicts P_R in ferroelectric thin films. In Lou's model, the ferroelectric material is divided into several hundred parts, and time required to switch the polarity of the half of the parts under depolarization field is calculated. Lou's model is based on the switching of the P_R. Since we confirmed that memory window is determined not only by P_R but also by operation voltages and *P-E* hysteresis, we utilized the time varying P_R from Lou's model and also considered *P-E* hysteresis to calculate memory window over time.

We can obtain P_R as a function of time using Lou's model as shown in Figure 3.4. Although P_R affects memory window, it is not directly interpreted as memory window. To calculate memory window, we should obtain the latest P-E hysteresis using the given P_R with time. The hysteresis is determined by the same procedures as a minor loop calculation in (8). With time, P_R decreases and the P-E hysteresis is calculated again using (8). The reduced P_R decreases depolarization field, and due to the decreased depolarization field, the decrease rate of P_R is varying. This process continues until the depolarization field is removed. During this process, P_R, depolarization field and memory window are self-consistently calculated.
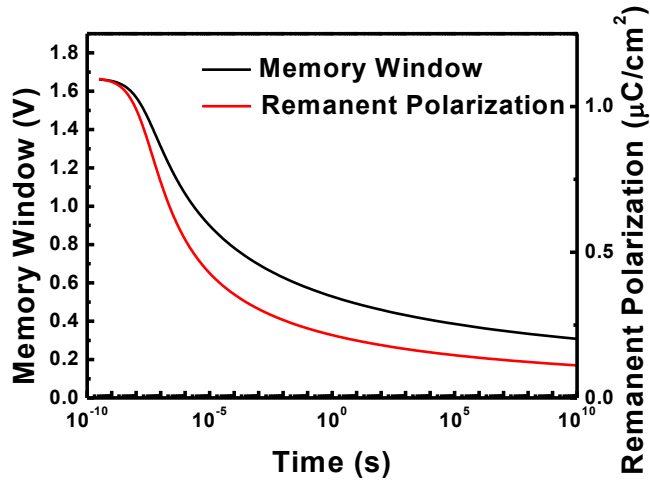
Figure 3.4 Memory window and remanent polarization as a function of time. They are decreasing with different rate with time.

Lou's model requires some physical quantities and device parameters to calculate P_R. It needs activation field of ferroelectric materials, switching time under infinite field, dielectric constants and device dimensions. Activation field is temperature and thickness dependent parameter and it is the field for generation of anti-parallel nuclei. Activation field is obtained by experiments [15] or calculation [16], and switching time is obtained by experiments [15]. Using the proposed memory window model with time-varying P_R from Lou's model, memory window as a function of time can be calculated as shown in Figure 3.4. For the calculations, E_C, P_S, P_R, dielectric constant, switching time and activation field are 84 kV/cm, 6.5 μC/cm^2, 4.8 μC/cm^2, 155, 1 ns and 200 kV/cm, respectively. Although both memory window and P_R decrease over time, the decrease
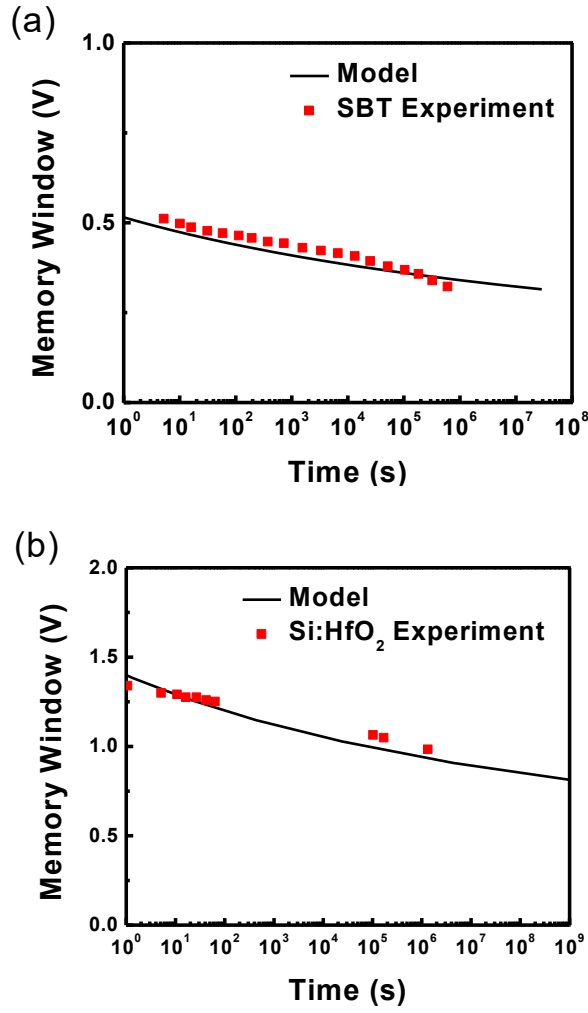
Figure 3.5 The MW as a function of time with (a) SBT [17] and (b) Si:HfO$_2$ [12].

rate is different because memory window is determined by ΔV_{th} not by P_R as shown in

(10).

The memory window is also verified with experiment data of strontium

bismuth tantalite (SrBi$_2$Ta$_2$O$_9$, SBT) [17] and Si:HfO$_2$ [12] in Figure 3.5. For memory

window calculation for SBT, E_C, P_S, P_R, dielectric constant, switching time and activation

field are 84 kV/cm, 6.5 µC/cm^2, 4.8 µC/cm^2, 155, 1 ns and 200 kV/cm, respectively. The write and erase voltages are 6 V and -4 V, respectively. For Si:HfO$_2$, those parameters are 1.1 MV/cm, 9.5 µC/cm^2, 6 µC/cm^2, 32, 1 ns and 630 kV/cm, respectively. The write and erase voltages are 4 V and -6 V. The calculations of memory window are based on the time scale of experiments. Both SBT and Si:HfO$_2$ results show good agreement on time scale from experiments.

3.4. Summary

A new model to calculate memory window for FeFETs is proposed. The proposed model can estimate memory window precisely regardless of the magnitude of external gate bias while the existing model is applicable for symmetric operation voltages only. The retention property of FeFETs can be calculated using the proposed model by applying time-varying P_R. The calculation results are compared with both simulation and experimental data, and it show good agreement.

Chapter 4

Performance Benefits of Ferroelectric Field-Effect Transistor with non-planar structure

4.1.   Introduction

Retention time is one of the most important features for memory technologies. Although FeFETs have several advantages such as non-destructive readout, high speed operation, and low power consumption [1]–[3], their short retention time is the major obstacle to their replacing current memory technologies. To increase retention time, one transistor-two capacitors (1T2C) structure is proposed for reduced depolarization field in the ferroelectric (FE) layer [4]. However, this leads to a larger footprint problem and is hence not suitable for high density. Alternatively, wider memory window devices can be a solution to extend retention time provided a small footprint can be maintained. In order to increase memory window without increasing cell area, new device structures must be used. Wider memory windows can be also achieved by using FE materials with smaller dielectric constants. In conventional inorganic materials such as lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT), the electric field in the FE layers is low due

to their high dielectric constants, causing smaller memory windows. Thus, the organic FE copolymer vinylidene fluoride and trifluoroethlene (P(VDF-TrFE)) is considered as a candidate owing to its low dielectric constant [5]–[12]. Alternatively, the recently discovered ferroelectric properties of Si-doped HfO_2 (Si:HfO_2) [13] are also promising because of its relatively low dielectric constant and its CMOS compatibility. If higher electric fields can be applied to FE layers with the same operation voltage by changing the FE materials, we can expect wider memory window and longer retention time.

In this chapter, we propose non-planar channel Metal-Ferroelectric-Insulator-Semiconductor (MFIS) FeFET and Metal-Ferroelectric-Semiconductor (MFS) FeFET memory structures using either P(VDF-TrFE) or Si:HfO_2. A junctionless (JL) transistor structure is used to enable low-thermal budget processing, because ion implantation steps for the source and the drain can be omitted; this is particularly advantageous for organic materials like P(VDF-TrFE) as well as future post-metallization 3D integration. In addition, by applying the shared FE top dielectric, the process for $4F^2$ cell size can be achieved. Using the proposed devices, we design 3x3 memory arrays and analyze array-level memory performance for the first time via technology computer-aided design (TCAD) simulations. We evaluate the impact of device dimensions on FET memory metrics such as threshold voltage shift (ΔV_{th}), subthreshold swing (SS), and interference.

4.2.   Device Structure and Operating Principle
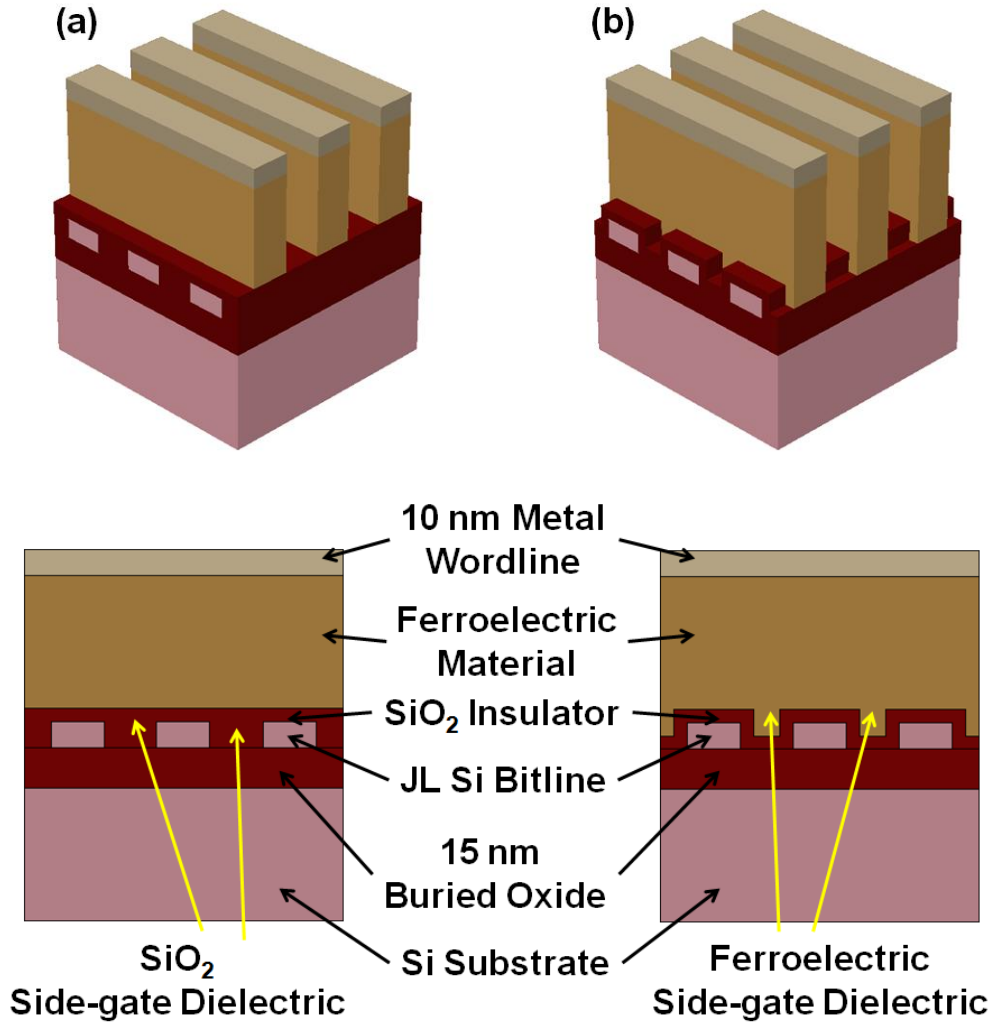
Figure 4.1 Proposed and simulated $4F^2$ FeFET memory structures organized in a 9-cell array. Both structures have non-planar junctionless (JL) channel, ferroelectric polymer top-gate dielectric, SiO_2 insulator and either (a) an oxide or (b) ferroelectric polymer side-gate dielectric.

The two proposed MFIS FeFET memory structures and their structural dimensions are shown in Figure 4.1, which have non-planar SiO_2-coated silicon JL channels to utilize the extra storage area and a FE top-gate dielectric with $4F^2$ cell size.

We consider the cases where the FE is either organic (P(VDF-TrFE)) or inorganic (Si:HfO$_2$) . The chosen side-gate dielectric is either SiO$_2$ for pure gate-to-channel electrostatic coupling (Figure 4.1(a)) or FE for simultaneous coupling and storage (Figure 4.1(b)) to verify a tradeoff between device performances (memory window and *SS*) and interference. The structures can be implemented on JL channel bitline arrays patterned on an SOI substrate followed by slight oxidation or oxide deposition. To realize the structure in Figure 4.1(a), an optional inter-channel oxide deposition and planarization step can be performed. A conformal SiO$_2$ is deposited and a FE layer can be formed by spin-coating for P(VDF-TrFE) or deposition for Si:HfO$_2$. The metal wordline arrays are defined followed by self-aligned etching of the FE material to minimize wordline interference.

The devices we study have silicon channels with 5×10^{18} cm^{-3} *n*-type doping for depletion mode operation, and the metal work function is 4.1 eV for P(VDF-TrFE) and 4.4 eV for Si:HfO$_2$. The FE top-gate dielectric is chosen to be 50 nm since a thinner organic FE layer would degrade the remanent polarization (P_r) and shorten the retention time [14]. P(VDF-TrFE) layers with 50 nm thickness have been experimentally achieved and devices have been demonstrated with sufficient memory windows [8], [10]. To make a fair comparison, the FE thickness is kept the same for Si:HfO$_2$. For all cases, a SiO$_2$ layer of 5 nm is inserted between the substrate and the FE in order to prevent charge injection from the substrate to the FE layer. In our structures, using SiO$_2$ layers thicker than 5 nm results in increased off-state leakage because the JL channel is not fully controlled by the gate. This effect will become more significant as the silicon channel height increases.

4.3. Simulation Models and Calibrations

We use Sentaurus TCAD [15] to simulate the foregoing 9-cell FeFET arrays. Since most simulation models for FE devices are not well characterized, we perform detailed calibration of P(VDF-TrFE) and Si:HfO$_2$ against experimental MFIS and MFS data [8], [13], [16]. In our calibration, we emphasize memory window, *SS*, and on-current level fittings because those metrics are of primary interest in this paper. Memory window and *SS* are fitted by FE material parameters, while the on-current level is matched by adjusting device transport coefficients. In order to mimic the actual phenomena in FE films formed by spin coating, amorphous non-ferroelectric layers with the same dielectric constant and fixed charge density as P(VDF-TrFE) has been added at both top and bottom interfaces of the FE material [17], [18]. The thickness of each non-ferroelectric layer is 2.5 nm.

Firstly, a MFIS structure with P(VDF-TrFE) is simulated using the same specifications as its experimental counterpart [8]. The dielectric constant and E_c are chosen from experimental values. From the transfer curves shown in Figure 4.2(a), V_{th} is fitted using Q_f, and *SS* is then matched by adjusting the interface trap density (D_{it}) of Si/SiO$_2$ interface. The on-current as a function of drain voltage is tuned by altering the mobility model parameters. For all simulations, the Lombardi mobility model [19], [20]
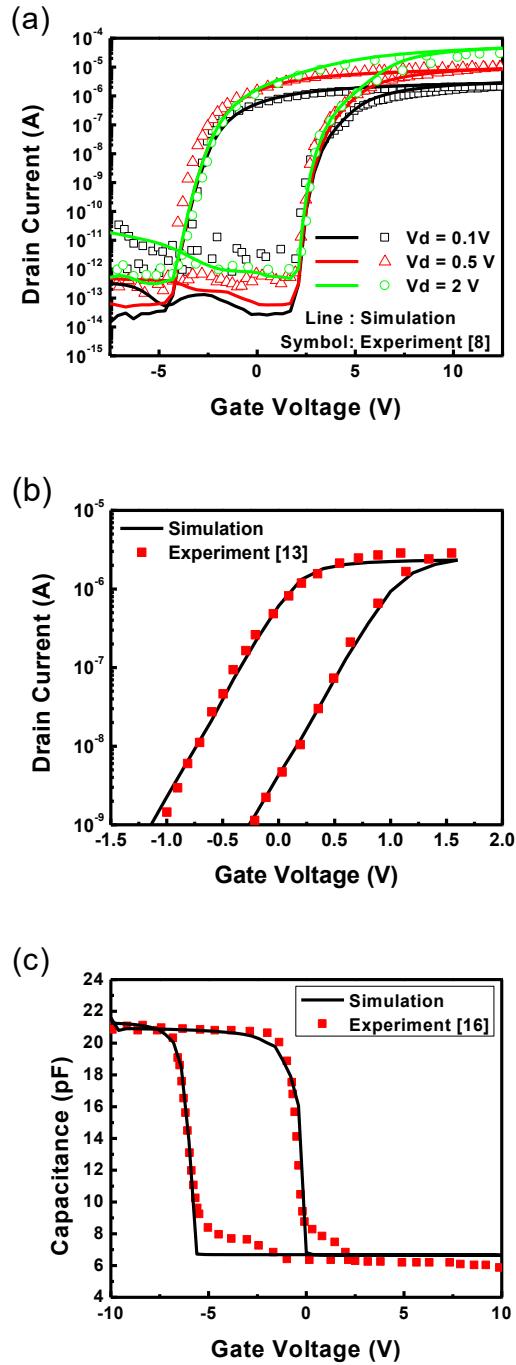
Figure 4.2 Comparison of calibrated simulation and experimental data. I_d-V_g for MFIS FeFET with (a) P(VDF-TrFE) [8], (b) Si:HfO$_2$ [13], and (c) C-V for MFS FeFET with P(VDF-TrFE) [16].

for phonon and surface roughness scattering is used, along with models accounting for impurity and Coulomb scattering. The resulting fitting parameters different from default simulator values are listed in Table 4.1. The hydrodynamic and density gradient models are included to account for nonstationary transport and carrier quantization, respectively. The Si:HfO$_2$ device parameters are also calibrated against experiment [13] in a similar manner. The resulting *I-V* fits are shown in Figure 4.2(a)-(b).

Table 4.1   Simulation parameters

Symbol	P(VDF-TrFE)	Si:HfO$_2$	Description
P_s (μC/cm^2)	10	9.5	Saturation polarization
P_r (μC/cm^2)	8	6	Remanent polarization
E_c (MV/cm)	1.3	1.1	Coercive field
Q_f (cm^{-3})	2.5×10^{18}	1×10^{17}	Fixed charge of FE
D_{it} (cm^{-2})	1.0×10^{11}	1.0×10^{11}	Si/SiO$_2$ interface trap density
$D_{it,ferro}$ (cm^{-2})	1.2×10^{13}	-	Si/P(VDF-TrFE) interface trap
ε_f	10	32	FE dielectric constant
A	2.11	2.11	Surface roughness scattering coefficient
B	1×10^7	1×10^7	Acoustic phonon scattering coefficient
C	400	400	Acoustic phonon scattering coefficient
ν	2	2	Coulomb scattering coefficient
γ	1	1	Coulomb scattering coefficient

Secondly, based on the parameters fitted for the MFIS device, a MFS P(VDF-TrFE) capacitor [16] is also calibrated. Most of the material parameters are the same as those for the MFIS device except for D_{it}, which changes because of the different interface. The memory window is mainly determined by E_c and Q_f of the P(VDF-TrFE), and those parameters are identical for both MFIS and MFS. By fitting the curvature of the *C-V* curve shown in Figure 4.2(c), $D_{it,ferro}$ of the P(VDF-TrFE)/Si interface is determined as

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listed in Table 4.1.

As Figure 4.2 shows, our simulation results agree well with experimental results in terms of memory window and *SS*. As the band-to-band tunneling model is not included, tunneling current is not captured here and may account for some deviation in the leakage current, which however does not compromise the validity of our simulations for memory window and *SS*.

4.4. Dimension Dependence

To evaluate the operational feasibility of our proposed non-planar FeFET memory structures, we perform 3D simulations using a +/- 10 V set/reset voltage. Shown in Figure 4.3 are simulated bi-directional transfer curves with both side-gate dielectrics.
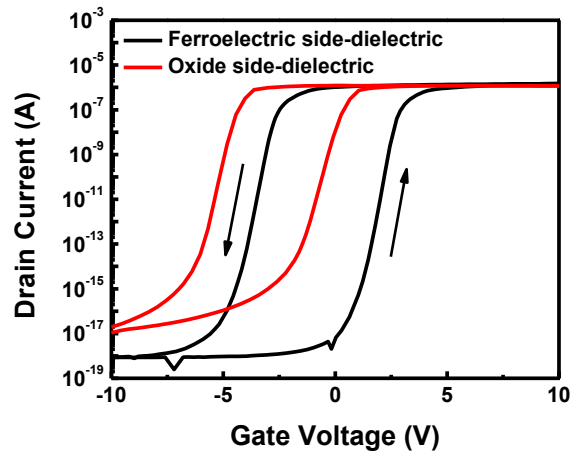
Figure 4.3 Representative simulated hysteretic transfer characteristics of the FeFET with either an SiO_2 or P(VDF-TrFE) side-gate dielectric.

The FE side-gate FeFET offers a slightly steeper *SS* yielding a wider memory window. These findings indicate that the side-gate FE enhances the wordline-to-bitline (gate to channel) electrostatic coupling due to the larger dielectric constant of FE compared to SiO_2, and slightly enhances storage.

The set/reset voltage is chosen by considering a gate stack voltage divider consisting of the oxide and FE capacitances. It requires the electric field inside the FE to be larger than E_c to switch polarization. Although the polarization does not reach the saturation value P_s under the given set voltage, achieving the remanent value P_r is enough to switch polarization. The required external voltage can be lowered by reducing the thickness of the FE layer. Alternatively, increasing the set voltage can help the polarization attain P_s and thus increase the memory window, but is technologically undesirable due to the increased power consumption. From our simulation results, it is clear that 10 V is enough to make wide memory windows for FE thicknesses of 50 nm.

4.4.1.   Dimension Dependence on Memory Window

The dependences of the memory window on the bitline channel dimensions for a baseline structure and both side-gate dielectrics are extracted in Figure 4.4. Figure 4.4(a) and (b) are for P(VDF-TrFE) and $Si:HfO_2$, respectively.

First, as shown in Figure 4(a), a wider FeFET with FE side-gate dielectric generally possesses a wider memory window since the corresponding volume of FE side-gate dielectric is proportional to the channel width to keep the cell size $4F^2$. The oxide

(a)

(b)
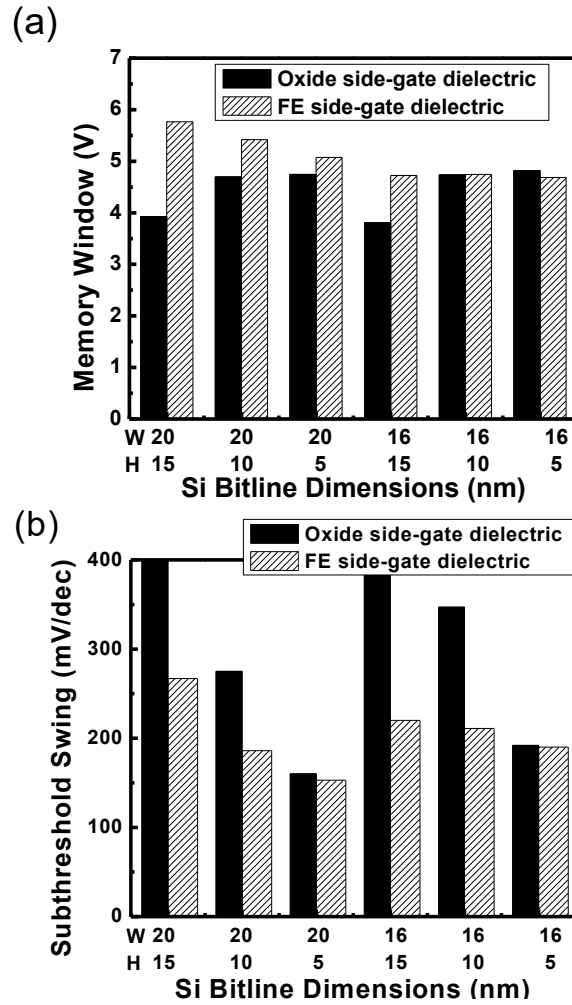
Figure 4.4 Extracted (a) memory window and (b) *SS* for different channel dimensions (W: width, H: height) with P(VDF-TrFE).

side-gate dielectric counterparts on the other hand exhibit no clear width dependence over the range examined. Second, for 20 nm wide FeFETs with FE side-gate dielectric, a thicker channel shows wider memory window because of greater FE volume (due to height increase) in between the channels and hence an increased voltage drop across the FE. This trend should continue unless the gate control of the channel degrades at large

heights. No height dependence is, on the other hand, observed for the 16 nm wide counterparts because their rather narrow FE side-gate dielectrics reduce gate field penetration and polarization of themselves. Moreover, since the SiO_2 side-gate dielectric is unable to provide storage, so increasing channel thickness of the respective FeFETs only weakens the gate coupling to the channel through SiO_2 and degrades off-current as well as memory window.

Figure 4.4(b) is the dependences of the memory window of Si:HfO$_2$ MFIS on the bitline channel dimensions for both side-gate dielectrics. Since the material parameters of Si:HfO$_2$ are different from those of P(VDF-TrFE), the memory window is different. However, the trends and the advantages which come from the FE side-gate dielectric are the same.

4.4.2. Dimension Dependence on Subthreshold Swing

The dependences of *SS* on the bitline channel dimensions for a baseline structure and both side-gate dielectrics are extracted in Figure 4.5. Figure 4.5(a) and (b) are for P(VDF-TrFE) and Si:HfO$_2$, respectively.

First, for thinner channel FeFETs, the *SS* generally decreases with increasing channel width as shown in Figure 4.5(a) owing to improved gate-to-channel electrostatic control through the top rather than side-gate dielectric. For the same reason, *SS* decreases as channel height shrinks. However, when the channel gets thicker, a narrower channel yields a smaller *SS* because the center of the channel is controlled through both the top

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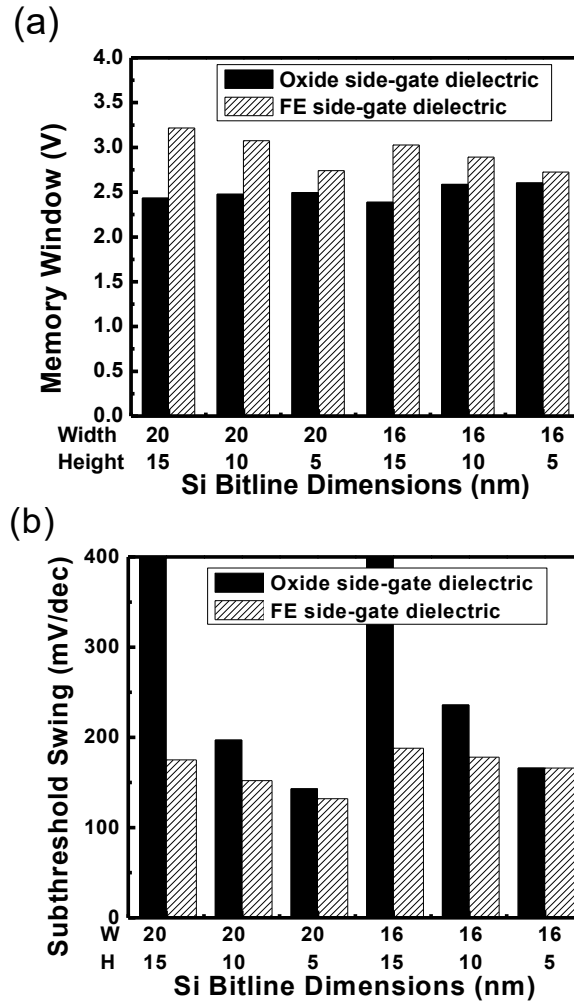
Figure 4.5 Extracted (a) memory window and (b) *SS* from set operation for different channel dimensions (W: width, H: height) with Si:HfO$_2$. At the height of 15 nm for oxide side-gate dielectric, the device is not turned off resulting in much greater *SS* than any other case.

and side-gate dielectrics. For instance, 20 nm wide devices have larger *SS* than 16 nm wide devices with fixed 15 nm channel thickness. Second, the higher permittivity side-gate FE provides additional coupling compared to SiO$_2$ and hence reduces *SS*, an effect which is more pronounced with taller channel due to the increased proportion of side-

coupling.

Figure 4.5(b) shows the dependences of *SS* of Si:HfO$_2$ MFIS on the bitline channel dimensions for both side-gate dielectrics. Although the values are different from those of P(VDF-TrFE), the trends with the channel dimensions are the same.

4.5. Interference

Interference of the current memory technologies is one of the big concerns for scaling. In this section, cell-to-cell interference and half-setting interference of the proposed structures are examined.

4.5.1. Cell-to-Cell Interference

Since FeFET is a capacitance-based memory, the fringing fields and interference between cells affect device performance significantly. We examine wordline and bitline interference separately using the same 9-cell arrays shown in Figure 4.1, where we choose channel thickness of 5 nm and pitch size of 20 nm.

For wordline interference evaluations, the middle target cell and two nearest adjacent cells sharing the same bitline are first reset by applying -10 V to all three wordlines and 0 V to the common bitline. These adjacent cells are then set by applying 10 V to their respective wordlines while grounding the wordline above the middle target cell. During the adjacent cell setting, the common bitline is kept grounded. Consequently, the potential difference between the adjacent wordlines and the bitline reaches the set
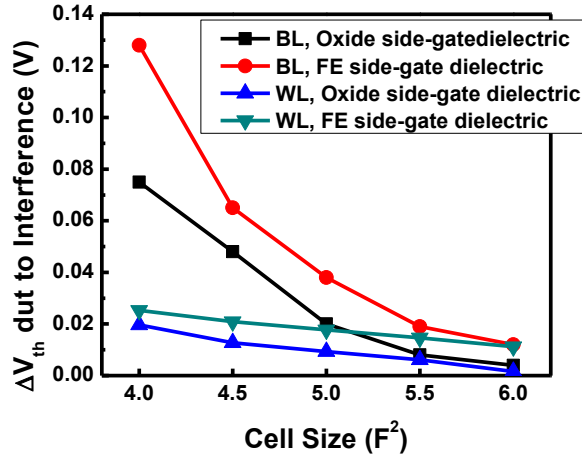
Figure 4.6 Wordline and bitline interference as a function of inter-line pitch, or equivalently cell size, extracted from the 9-cell arrays with different side-dielectric shown in Figure 4.1.

voltage, while the nominal potential difference between the middle target wordline and the bitline is kept zero and the middle target cell retains the state. However, due to interference caused by electric fields between the wordlines of the adjacent cells and the bitline of the middle target cell, the polarization of the FE layer right above the middle target cell can be affected and is reflected by V_{th}. The resultant ΔV_{th} on the target cell due to interference [21] is examined as a function of inter-wordline pitch, or equivalently the cell size, keeping inter-bitline pitch the same. As shown in Figure 4.6, the wordline interference marginally decreases with increasing pitch due to weaker coupling between the adjacent aggressor wordlines and the victimized middle target bitline. Also, the side-gate dielectric material affects wordline interference, but the effect is narrow and they are all below 0.03 V.

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For the bitline interference examination, the middle target cell and two nearest adjacent cells sharing the same wordline are first reset by applying -10 V to the common wordline and 0 V to all three bitlines for reset. With 10 V applied to the common wordline, the adjacent cells are then set by grounding the corresponding bitlines. The voltage on the target cell bitline is changed to half the set voltage to prevent an unintentional set. It is assumed that the electric field from the potential difference of half-set voltage between the wordline and the bitline of the target cell does not exceed E_c. Therefore, the middle target cell keeps the reset state and two adjacent cells have the set states. The simulated ΔV_{th} of the target cell due to bitline interference as a function of inter-bitline pitch are also shown in Figure 4.6. The extracted bitline interference also decreases inversely with the inter-line pitch but is more substantial (≤ 0.14 V) than wordline interference at the same pitches. This is attributed to the FE material overlapping adjacent cells along the same wordline, in contrast to the air or dielectric gap between adjacent cells sharing the same bitline for wordline interference.

Another general trend observed from Figure 4.6 is that the FE side-gate dielectric FET shows higher wordline and bitline interference than its SiO_2 counterpart due to the polarization of the FE in between channels. In other words, bitline interference with the FE side dielectric is the largest. However, we note that the maximum bitline interference in $4F^2$ cells constitutes less than 2.6 % of the ~5.06 V memory window (Figure 4.4(a)); this suggests that that highly selective setting of physically connected, individual FeFET bits is feasible.

4.5.2. Half-setting Interference

Figure 4.7 shows the voltage matrix for write operation of selected cells. During set/reset operations of a memory array, the proper voltage set must be applied not only on the target memory cell but also on the neighboring memory cells. The set voltage is applied on the wordline and 0 V is applied on the bitline of the target cell. To avoid unintentional setting of the adjacent cells, half of the set voltage is applied on the bitlines of adjacent cells. For the ideal case, the polarization must be preserved even if half-set voltage is applied because vertical electric fields due to half-set voltages do not exceed E_c. In reality, however, it is affected even at fields smaller than E_c. This phenomenon is prominent when the previously programmed cell is under half-set voltage with opposite sign over cycles [22]. This interference must be distinguished from cell-to-cell interference caused by fringing fields between the target cell and the adjacent cell,
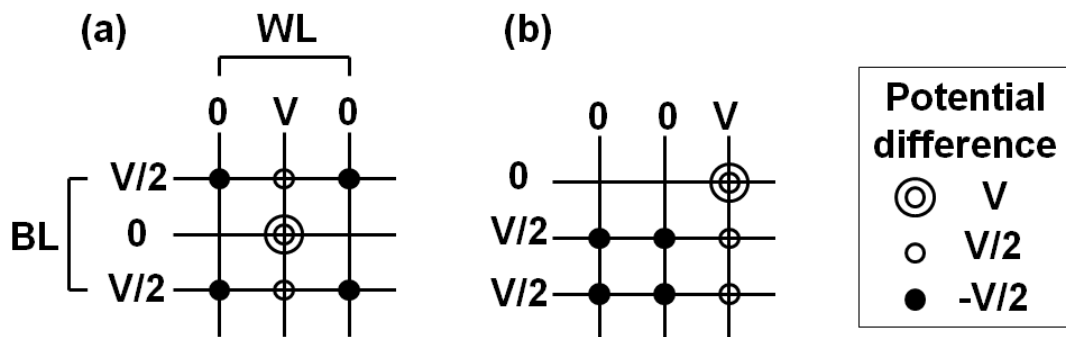
Figure 4.7 Write operation voltage sets. (a) The only center cell is set and (b) the written cell is under unintentional half-set voltage during write operation for other cells.
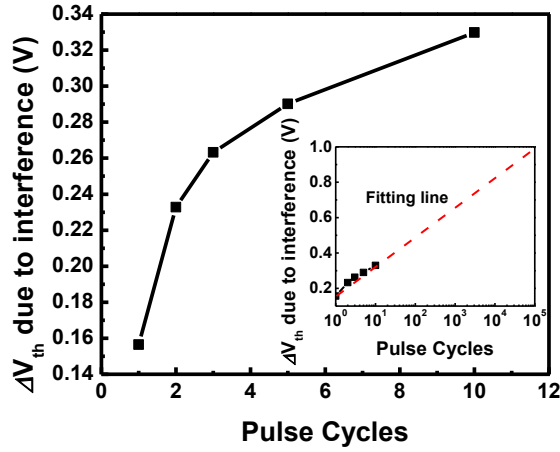
Figure 4.8 Programming interference as a function of the pulse cycles extracted from the 9-cell arrays with ferroelectric side-gate dielectric. (Inset) Trend line over pulse cycles in log scale.

because, in contrast with the latter, this effect is directly caused by the voltage of the cell's own gate.

The unintentional half-setting interference is plotted in Figure 4.8. As described, with increasing number of cycles, V_{th} of the memory cell shifts more due to continuous accumulation of partial polarization switching. After the first pulse cycle of the half-set voltage application on the programmed memory cell, ΔV_{th} is 0.15 V. As a half-set voltage pulse is continuously applied, the amount of ΔV_{th} per cycle is decreased, but total ΔV_{th} increases because the state of the victimized memory cell is changed to the "half-programmed state." This result is in line with previous reports [22]. According to the logarithmic relationship between the interference and pulse cycles, ΔV_{th} will reach approximately 1 V after 10^5 cycles, which is the minimum industry roadmap (ITRS)

requirement as shown in the inset of Figure 4.8. When the programmed memory cell is affected by the half-set/reset voltage over cycles, the V_{th} of the memory cell can be changed, reducing memory window; fortunately this reduction will not affect the state since it is much smaller than the memory window margin of ~4 V.

4.6.   Metal-Ferroelectric-Semiconductor Structure

As discussed above, one critical problem of the FeFET is charge diffusion at the substrate and FE interface. An insulating layer is normally placed between the substrate and the FE material to prevent the inter-diffusion, at the cost of reduced electric field. Thus, if the diffusion issue can be solved without the insulating layer, unnecessary voltage drop across the insulating layer can be removed. P(VDF-TrFE) does not need high temperatures for annealing, so the process temperature can be lower than that of inorganic materials. Consequently, the diffusion problem can be reduced without the insulating layer. Therefore, the MFS structure can be achieved [16].

Figure 4.9 shows memory windows and *SS* for MFS structures for SiO_2 and FE side-gate dielectrics. The applied voltage is the same as the voltage on MFIS. It is obvious that MFS structures have a wider memory window than MFIS shown in Figure 4.4(a) because there is no potential drop across the insulating layer. Therefore, we need less voltage to achieve the same memory window using the MFS design. In the same manner as MFIS performance evaluations, the dependences of the memory window and
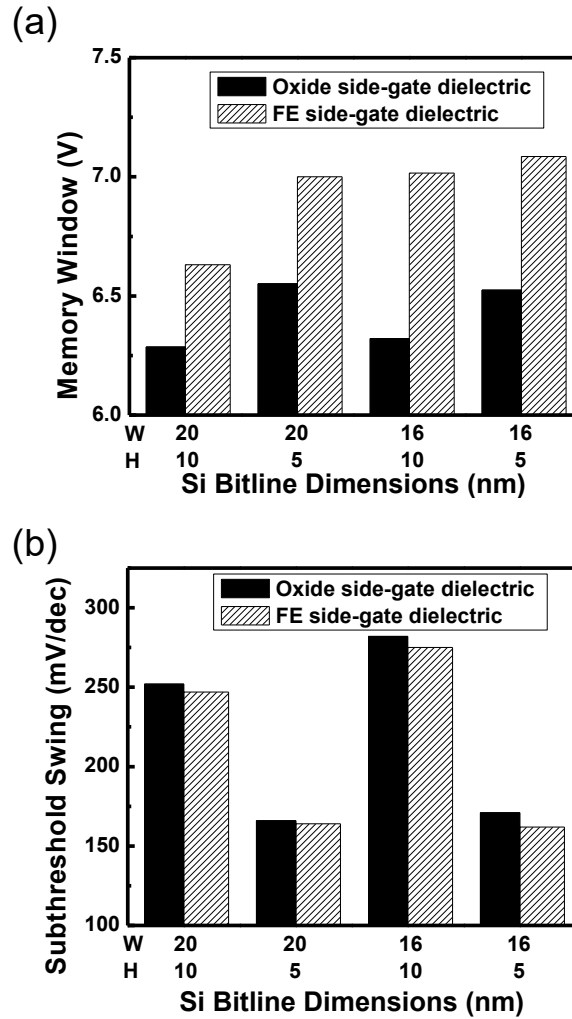
Figure 4.9 Extracted (a) memory window and (b) *SS* for MFS FeFET structures with P(VDF-TrFE).

SS on the bitline channel dimensions for both side-gate dielectrics are extracted. With a shorter or narrower channel, the portion of the FE region affected by enhanced field crowding near the channel corners is increased. It results in a greater polarization per unit area, and a wider memory window is attained. Unlike MFIS structures, the field crowding

effect near the channel corners is strong. Thus, it affects more on a memory window than the total ferroelectric volume. Also, smaller *SS* of the thin channel is one cause of a wider memory window, as discussed for the MFIS device.

The *SS* exhibits similar trends to the MFIS cases. Interestingly, the *SS* improvement from the side-gate dielectric is insignificant for MFS. Since there is no insulator, there is no voltage drop across the insulator resulting in a strong vertical coupling between the gate and the channel. Therefore, the side coupling effect is less important for MFS FeFETs.

4.7. Summary

Non-planar FeFETs with JL channel and either a SiO_2 or a ferroelectric side-gate dielectric are proposed to solve the thermal budget issue and to improve memory performance. Dimension dependences on memory window and *SS* and interference are examined. Our results indicate that the FE side-gate option delivers large enough memory windows. The better *SS* and memory windows offered by the FE side-gate device must be balanced against slightly worse bitline interference. However, the performance benefit from the FE side-gate is much larger than the increased interference. Our interference study affirms the feasibility of the novel structure of FeFET memory with $4F^2$ cell size. We also find that unintentional half-set interference does not confuse the cell states. Finally, MFS structures with either a SiO_2 or a FE side-gate dielectric were examined as

counterparts of MFIS, and they show wider memory windows than MFIS. In this work, we focus on P(VDF-TrFE) and Si:HfO$_2$, but our results can be generalized to other materials.

Chapter 5

Conclusion

5.1. Summary

As the current flash memory technology faces scaling limitations, alternative memory technologies are emerging to overcome the limitations and continue scaling. Although individual memory cells have been studied, the performance of memory technologies on array structures has not yet been studied extensively. Considering the practical applications, memory performance on array structures is more important to identify the properties of memory technologies. In order to find proper applications, we need to know the advantages and disadvantages of memory technologies. Comparisons of performance, such as delay and energy consumption, between memory technologies are necessary, but they have not yet been conducted, since there is no proper delay model for crosspoint architecture. Thus, we developed an accurate delay model for crosspoint architecture. Using the delay model, we benchmarked the delay and energy consumption of memory technologies. The results show that FeFETs have advantages over other memory technologies in terms of operation delay, especially when the array size is large.

Although FeFETs have such an advantage, the important features of memory,

such as memory window, have not been well established. Since the hysteresis and capacitance of ferroelectric materials vary with applied voltages, all material properties and device parameters must be considered for accurate memory window calculations. In this work, we developed an accurate memory window model including material parameters, device dimensions, and practical symmetric/asymmetric operation voltages. The results of the proposed model are more precise than those of the existing memory window model. In addition, this model can be used to estimate the retention properties of FeFETs. All the calculation results show good agreement with the experiments.

Despite their several advantages, FeFETs are not widely used because of their short retention time. One of the ways of increasing retention time is by increasing memory window. To increase the memory window while maintaining the cell size, we proposed non-planar structures with either SiO_2 side-gate dielectrics or FE side-gate dielectrics and continuous FE regions along the wordlines. Due to the extra storage volume and the improved electrostatic coupling between the channel and the gate, the proposed structures showed wider memory windows and smaller *SS*. The proposed structures were examined with various device dimensions. In addition, wordline interference and bitline interference were separately examined. In spite of the continuous FE below the gate, the proposed structures showed reasonably low interference. While maintaining the cell size of $4F^2$, the maximum interference was 2.6 % of the memory window of 5.06 V under the write voltage of 10 V. Therefore, interference did not confuse memory cell states.

5.2. Contributions of This Work

The important contributions of this work are as follows:

(1) The first development of an array-level delay model for crosspoint architecture

(2) Performance comparisons between memory technologies on array structures in order to identify the advantages and disadvantages of various memory technologies

(3) Development of an accurate memory window model for FeFETs with practical conditions without simulation

(4) Design of novel non-planar FeFET structures with the smallest cell size of $4F^2$ for a wider memory window and better subthreshold swing

(5) Dimensional dependence and interference study of the non-planar FeFETs to optimize the proposed FeFETs

5.3. Recommendations for Future Work

To build upon the work performed in this thesis, we recommend further research in the following areas:

(1) Evaluation of delay and energy consumption with peripheral circuitry: Delay and energy consumption evaluation is based on a memory array structure. For more general performance evaluations, peripheral circuitry such as drivers, sensors, or multiplexors can be included in benchmarking.

(2) Depolarization field of FeFETs with various device structures: In general, different device dimensions of FeFETs provide different depolarization fields, because they are affected by the capacitance ratio between the FE and the insulator. In order to optimize the depolarization field for FeFETs, further research is required with various structures and dimensions.

(3) Experimental demonstration of non-planar FeFETs: The proposed non-planar structures were studied based on the TCAD tool. To confirm the feasibility of the proposed structures, an experimental study is required.

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