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Fixed On-time Series Resonant Converter for Maximum Power Point Tracking Application

THESIS

submitted in partial satisfaction of the requirements
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MASTER OF SCIENCE

in Electrical Engineering

by

Yi-Shao Liao

Thesis Committee:
Professor Keyue Smedley, Chair
Professor Hung Cao
Professor Quoc Viet Dang

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ABSTRACT OF THE THESIS

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by

Yi-Shao Liao

Master of Science in Electrical Engineering

University of California, Irvine, 2023

Professor Keyue Smedley, Chair

This dissertation explores the feasibility of using resonant converters for maximum power point tracking (MPPT) of solar power. Resonant converters are known for their high efficiency, compact size, low EMI, and high power density. However, one crucial factor of resonant converters hindered their applications in many areas, i.e., lack of full regulation capability. Recently, the fixed on-time modulation method was reported to series resonant converters (SRCs), enabling them with full range regulation. This advantage is adopted in this thesis for maximum power point tracking (MPPT) applications. A precise and responsive perturb and observe algorithm is employed as the MPPT method to achieve maximum power output from the solar system. Chapter 1 provides a comprehensive literature review on MPPT applications with SRCs. It examines the characteristics of PV arrays, explores soft-switching techniques and resonant converters for high-efficiency topologies, and investigates various MPPT techniques to achieve fast and accurate tracking of the maximum power point. Chapter 2 focuses on analyzing the fixed on-time control method for half-bridge SRCs. This analysis enables half-bridge SRCs to perform full-range regulation within a limited frequency range, making them viable candidate for MPPT applications. In

Chapter 3, experimental results are presented. A prototype of a half-bridge SRC is built with a nominal input voltage of 36V to utilize with a PV panel. The prototype demonstrates a peak efficiency of 95.4% in a 180W application, validating the high efficiency of the prototype. Moreover, the MPPT experiment is conducted using the half-bridge SRC prototype, demonstrating its ability to track the MPP of the PV array with a deviation of only ±2W from the actual maximum power. The prototype exhibits a good efficiency of 92.6% during this process. Chapter 4 compares the half-bridge SRC with a conventional buck converter, highlighting the differences between their hard-switching and soft-switching characteristics. The results demonstrate that the half-bridge SRC displays efficiency enhancements ranging from 2% to 5%. Chapter 5 presents the conclusions drawn from this study, along with a discussion on the future directions and potential areas for further investigation.

INTRODUCTION

The potential for sustainable energy generation is driven by the increasing interest in photovoltaic (PV) arrays to convert solar energy into electricity. It is crucial to efficiently track and maintain the PV panel at its maximum power point (MPP) to generate the highest power output. Numerous maximum power point tracking (MPPT) algorithms and techniques have been developed to extract the maximum power from PV arrays. One commonly used approach is the perturb and observe algorithm (P&O), which determines the MPP by analyzing the power-voltage characteristic curve of the PV array.

Series resonant converters (SRCs) have gained popularity in various industries due to their high efficiency and reliability. They operate at high frequencies and possess desirable soft-switching capabilities, such as zero voltage switching (ZVS) and zero current switching (ZCS), which enhance system power density by maintaining high efficiency. However, conventional SRCs theoretically achieve full-range voltage regulation only with an infinite frequency range. Consequently, they are inappropriate for solar system applications requiring adjustable voltage gain within a limited frequency range.

To address this limitation, a method for achieving full-range voltage regulation in series resonant converters has been proposed. This method, known as fixed on-time modulation, enables voltage gain adjustment within a limited frequency range while retaining the advantages of zero voltage switching of SRCs. In this research, an MPPT application is proposed based on a half-bridge SRC configuration designed to identify a PV array's maximum power point automatically. The proposed method incorporates

ZVS turn-on for transistors and ZCS turn-off for diodes, thereby enhancing system efficiency. Moreover, the proposed approach goes beyond implementing an advanced P&O algorithm, ensuring fast response and high stability in MPPT operations. This improvement facilitates accurate and efficient tracking of the maximum power point, leading to enhanced performance compared to traditional P&O algorithms.

Chapter 1 comprehensively reviews essential aspects of MPPT applications in PV systems. It begins by examining the characteristics of PV arrays and previous approaches used for MPPT. Furthermore, the chapter discusses different DC-DC converters commonly employed in MPPT applications. It explores their features, advantages, and methods to improve efficiency. The chapter also delves into the control method used for SRC to achieve full-range voltage regulation, making them qualified for MPPT applications.

Chapter 2 presents a detailed system analysis, focusing on the half-bridge SRC. The analysis includes an in-depth examination of the converter's operation, characteristics, and performance. Furthermore, Chapter 2 covers the implementation of maximum power point tracking in the PV system. It explains the techniques and advanced P&O algorithms used to track and maintain the optimal operating point of the PV system, ensuring maximum power extraction from the solar panels.

Chapter 3 presents the experimental results of the proposed half-bridge SRC-based MPPT approach. The chapter validates the proposed method by evaluating the transistors' ZVS turn-on and the diodes' ZCS turn-off. Additionally, the chapter illustrates the efficiency of the half-bridge SRC prototype when executing the MPPT algorithm for battery charging. The chapter also demonstrates the effective tracking of

the PV system's maximum power point with the FTM-based P&O method. The experimental results prove the capability of the proposed method to achieve accurate and efficient MPPT.

Chapter 4 implements a buck converter to compare with the half-bridge SRC. The hard-switching operations of the buck converter are contrasted with the soft-switching operations of the half-bridge SRC. Additionally, a comparison is made regarding the buck converter's efficiency, emphasizing the half-bridge SRC's excellent efficiency.

The paper's main contributions are summarized in Chapter 5, including the proposed half-bridge SRC-based MPPT approach and the FTM-based P&O method. Finally, suggestions for future research directions are provided.

CHAPTER 1: Literature Review

Photovoltaic Arrays Characteristics

The PV arrays were modeled for analysis and simulation in [1]. Fig. 1.1 shows the model of a theoretical PV cell and equivalent circuit of a practical PV device, including the series and parallel resistances. The performance of PV arrays depends on its current-voltage (I-V) characteristic curve, which can be derived using the model in Fig. 1.1.

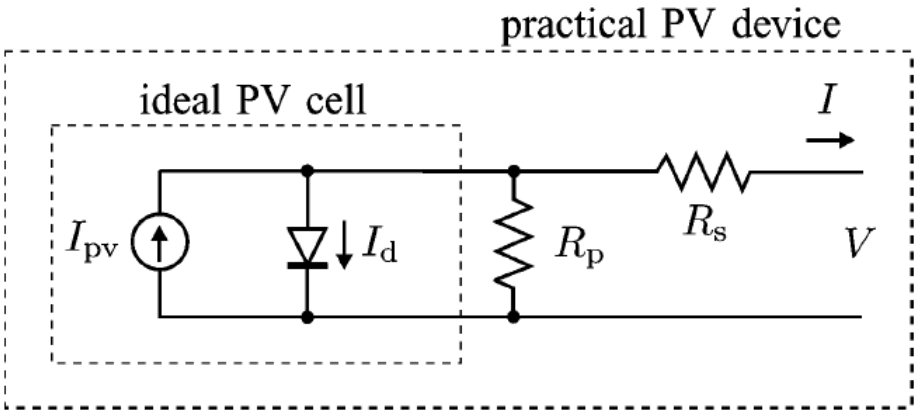


Fig. 1.1: Single-diode model of PV cell in practical devices. Figure from [1].

Fig. 1.2 shows the I-V curve of PV arrays based on the model in Fig. 1.1, where three remarkable points are highlighted: maximum power point, short-circuit current (I_{sc}), and open-circuit voltage (V_{oc}). The MPP, located at the knee of the I-V curve, represents the point at which the PV array operates at its maximum power output. Similarly, the V_{oc} and I_{sc} on the I-V curve represent the array's maximum voltage and current output.

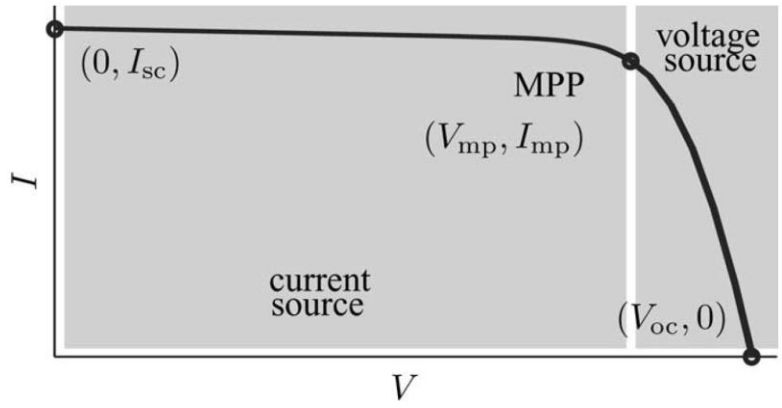
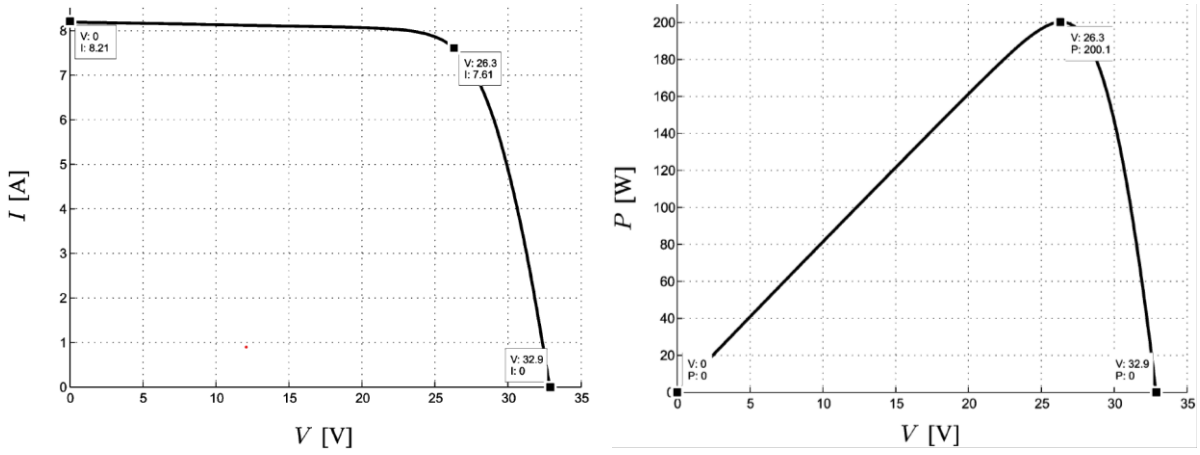


Fig. 1.2: An example I–V curve of PV arrays. Figure from [1].

Fig. 1.3 displays the Power-Voltage (P-V) and I-V curves under experimental conditions. The most effective way to enhance the efficiency and performance of the PV array is to regulate the operating point around the MPP to generate the maximum output power. The P-V and I-V curves demonstrate the fundamental characteristics of PV arrays, including Maximum Power, Voltage at MPP (V_{mp}), Current at MPP (I_{mp}), I_{sc}, and V_{oc}.

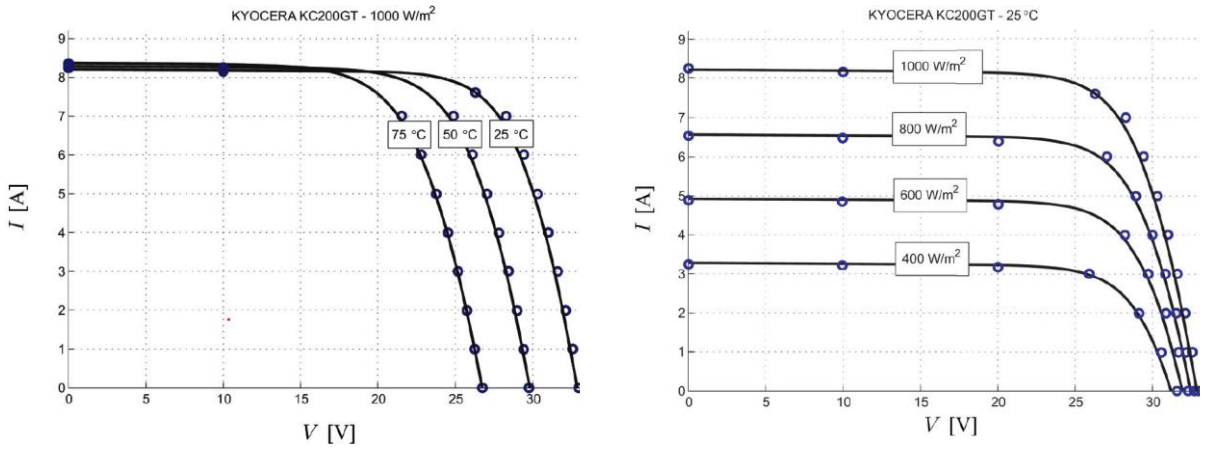


(a) (b)

Fig. 1.3: (a) Characteristic I–V curve of PV arrays. (b) Characteristic P-V curve of PV arrays. Figure from [1].

Both temperature and irradiation levels impact the functioning of PV arrays. Fig. 1.4a illustrates that with an increase in the ambient temperature, the PV voltage

decreases, reducing maximum power. Additionally, Fig. 1.4b demonstrates that varied irradiation levels affect maximum power, with higher irradiation resulting in higher maximum power.



(a) (b)

Fig. 1.4: (a) I-V curves with different temperature levels. (b) I-V curves with different irradiation levels. Figure from [1].

To ensure PV systems operate optimally, designers and operators must regularly monitor their performance and adjust as necessary. One method for optimizing the performance of PV arrays is maximum power point tracking.

Maximum Power Point Tracking Techniques

Various maximum power point tracking techniques have been previously proposed to find the MPP of PV arrays:

Constant reference voltage method [2]:

Fig. 1.5 illustrates the error amplifier and comparator with a reference voltage. This technique involves comparing the PV array voltage with a predetermined reference voltage that corresponds to the PV voltage at the MPP under specific atmospheric conditions. The resultant difference signal drives a power conditioning unit that links the PV array to the load. However, this approach is limited to specific solar radiation intensity and solar cell temperature conditions, neglecting the variations in these environmental factors. A more inclusive design should be proposed to accommodate applications where these factors change.

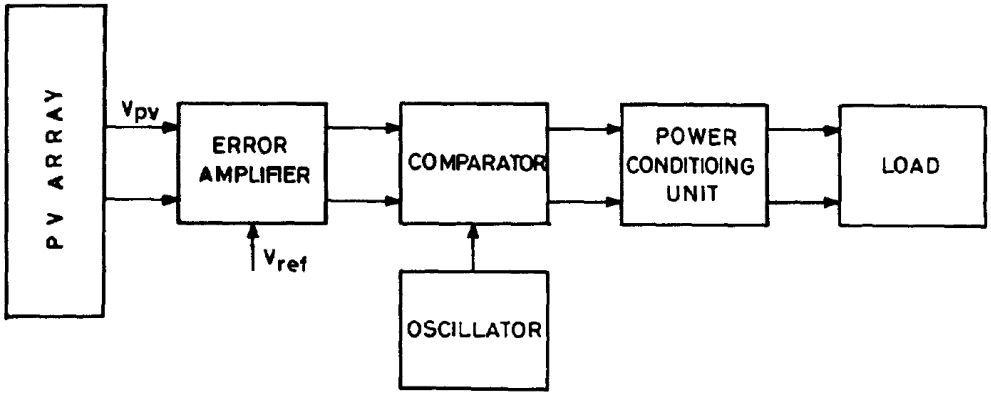


Fig. 1.5: Block diagram of constant reference voltage method. Figure from [2].

Zero-slope regulation [3]:

As depicted in Fig. 1.3, the power derivative concerning voltage (dP/dV) equals zero at the MPP. The PV power can be calculated by sampling the current and voltage of the PV array at regular intervals. A PI controller regulates the PWM control signal of the dc/dc converter until dP/dV = 0 is satisfied.

Digital signal processor or microcontroller based [4] [5]:

Technological advancements have led to the adoption of digital signal processors (DSPs) and microcontrollers in the power electronics area, compared to traditional PWM devices and PI control methods. The increased computing power of these devices has enabled the utilization of two popular MPPT techniques: the Incremental Conductance (INC) method and the Perturb and Observe method.

Incremental conductance method [6] [7]:

The INC algorithm controls the operating point toward the MPP by comparing the incremental conductance (ΔI/ΔV) with the actual conductance (I/V). Fig. 1.6 shows the operational principle, which is:

$$\begin{cases} \frac{dI}{dV} = -\frac{I}{V}, & At\ the\ MPP \\ \frac{dI}{dV} > -\frac{I}{V}, & Left\ side\ of\ the\ MPP \\ \frac{dI}{dV} < -\frac{I}{V}, & Right\ side\ of\ the\ MPP \end{cases}$$

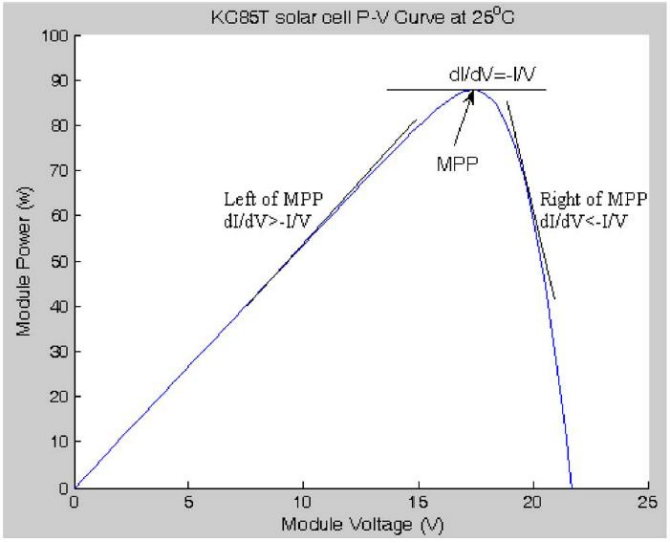


Fig. 1.6: The operational principle of the INC method. Figure from [6].

The control of the operating point continues until ΔI/ΔV = I/V, indicating that the MPP has been achieved. The controller subsequently maintains this voltage until there is a change in the atmosphere condition, and the process is repeated.

Perturb and Observe method [4] [5] [7]:

The P&O method introduces small variations in the converter's duty ratio and then observes the resulting change in the output power after each perturbation. Fig. 1.7 illustrates the P&O operating principle. If the operating point is on the left-hand side of the curve (where ΔP/ΔV is positive), then the operating voltage should be increased toward the MPP by adjusting the duty ratio. Conversely, the operating voltage should decrease if the operating point is on the right-hand side of the curve (where ΔP/ΔV is negative).

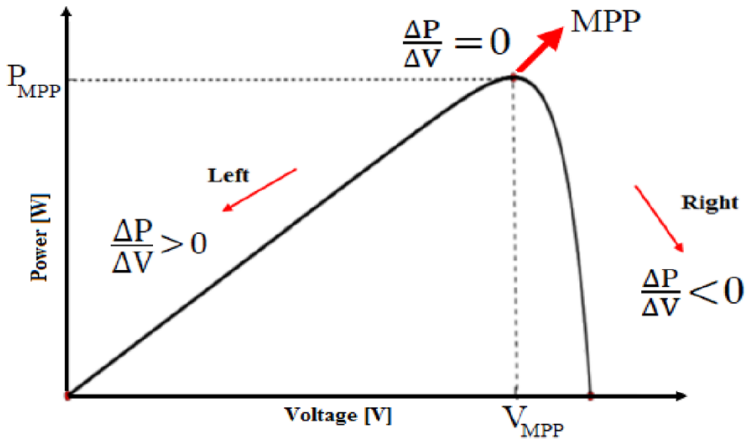


Fig. 1.7: The operational principle of the P&O method. Figure from [7].

INC method vs. P&O method [7]-[10]:

There is a debate about which of the two techniques is superior. Regarding accuracy, the INC technique is considered more reliable in maintaining the MPP than the P&O technique. The latter employs perturbations that cause the operating point to oscillate around the MPP, resulting in steady-state oscillations [8]. Moreover, the INC

technique has a faster speed in achieving the MPP, making it more adaptive to rapidly changing conditions. However, from an implementation standpoint, the INC method necessitates more complex computations, which may result in higher DSP costs and make it more difficult for the user to implement. The summary of the comparison between the two techniques is presented in Table 1.1.

Table 1.1: Comparison of MPPT techniques [9] [10]

Technique	Accuracy	Speed	Implementation Complexity	Sensors Needed
P&O	Good	Good	Simple	V, I
INC	Better	Better	Medium	V, I

Advanced P&O methods:

One drawback of the P&O method is the presence of steady-state 3-level oscillation, as depicted in Fig. 1.8. This oscillation causes the duty ratio to alternate between the duty ratio at MPP, the duty ratio at MPP + Δd, and the duty ratio at MPP - Δd. Such oscillation can lead to inefficient tracking and instability in specific scenarios.

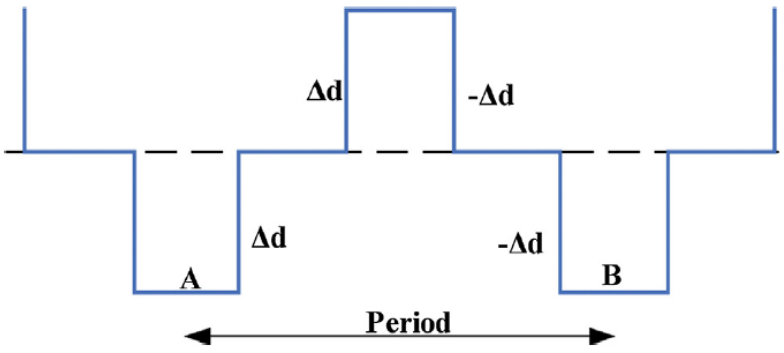


Fig. 1.8: Steady-state 3-level oscillation in the P&O method. Figure from [11].

To address the issue of 3-level oscillation in the P&O method, a method has been introduced in [11]. This method tracks whether the system has reached the steady-

state oscillation. Once this condition is satisfied, the system operates at a fixed duty ratio equal to the average of the duty cycle values recorded during one period of the 3-level oscillation.

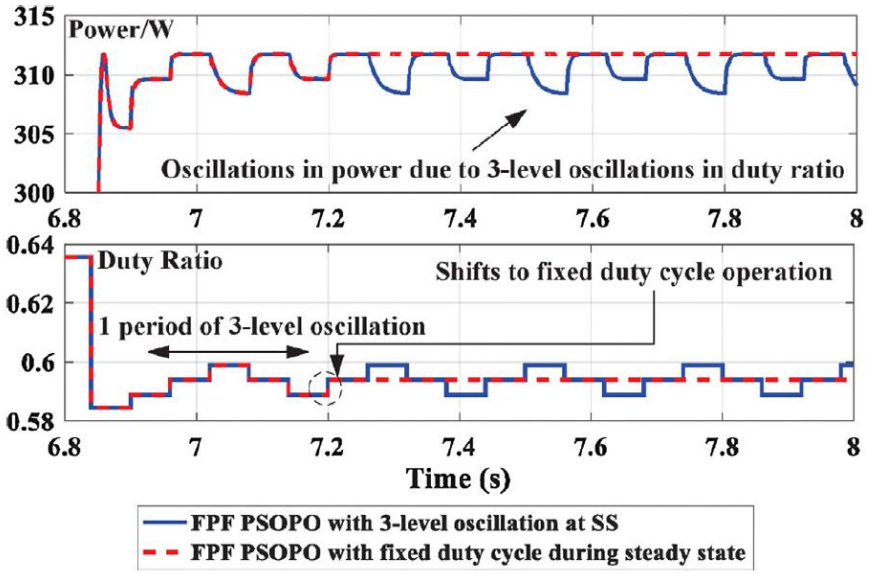


Fig. 1.9: Comparison of 3-level and fixed-duty-cycle methods. Figure from [11].

Fig. 1.9 illustrates the waveform results aimed at addressing the 3-level oscillation. In the presence of this oscillation, the output power experiences fluctuations during the steady state due to the oscillation in the duty ratio. However, by employing the proposed fix-duty-ratio method, the duty ratio is fixed at the average duty ratio value, eliminating power oscillation. The waveform results demonstrate the effectiveness of this approach in stabilizing the output power and enhancing the stability and efficiency of the MPPT system.

Various parameters, including the perturbation step (ΔD) and frequency, can be adjusted to improve MPP tracking speed. However, using a large, fixed perturbation step can increase the tracking speed, but it often leads to significant oscillations in the

steady state. Similarly, employing a large constant perturbation frequency can also result in similar oscillation issues.

To address this challenge and achieve improvements in the speed, accuracy, and efficiency of MPPT, a variable step-size algorithm is proposed in [12].

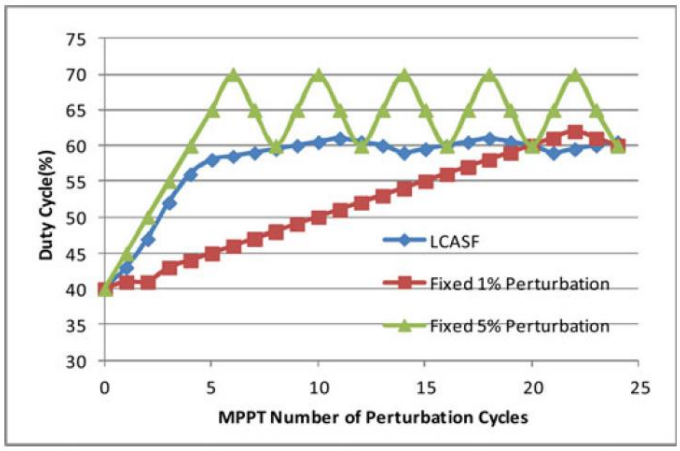


Fig. 1.10: Comparisons of adaptive-step method and fixed-step methods. Figure from [12].

In Fig. 1.10, different perturbation step sizes are compared. The fixed 1% duty step exhibits the slowest tracking speed, while the fixed 5% duty step demonstrates a faster approach to reach the MPP but results in more significant oscillations. However, with the variable step-size algorithm, the method achieves a quick control speed to reach the MPP while maintaining a similar oscillation level as the fixed 1% duty ratio.

In [11], an adaptive perturbation frequency algorithm is utilized. The results depicted in Fig. 1.11 highlight the faster speed (red line) at which the MPP is reached compared to using a fixed perturbation frequency (blue line).

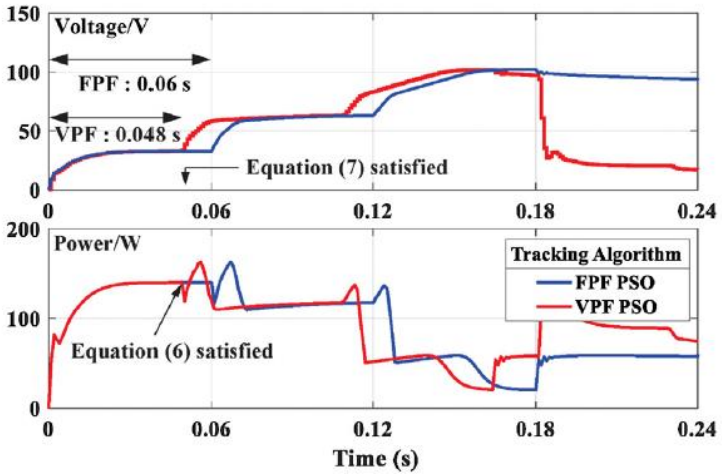


Fig. 1.11: Comparisons of adaptive and fixed perturbation frequency methods. Figure from [11].

In conclusion, implementing the adaptive perturbation step and frequency methods has proven effective in achieving improved tracking speed while maintaining stability. These adaptive algorithms adjust the perturbation step and frequency based on system conditions, enhancing performance and accurate maximum power point tracking.

DC-DC Converters for MPPT Applications

DC-DC converters are commonly used in MPPT systems to efficiently convert the output voltage of a PV array to the voltage required by the load or the battery. The MPPT controller monitors the output voltage and current of the PV array and then adjusts the duty cycle of the DC-DC converter to maintain the operating point at the MPP. By operating at the MPP, the MPPT system ensures that the PV panel operates at its highest efficiency and generates the maximum possible output power.

The DC-DC converter used in an MPPT system can be either a buck [4] [5], boost [13], buck-boost, or other topology, depending on the voltage and current requirements of the load or the battery. The converter selection also hinges on the application's specific needs, such as input and output voltage range, efficiency, and cost.

Buck converter [4] [5] and Boost converter [13]:

Buck converters, also known as step-down converters, are commonly utilized when the output voltage of the PV panel is higher than the voltage required by the load. Fig. 1.12 depicts an equivalent circuit of a buck-converter-based PV array system, where a buck converter is connected between a PV array and loads. By adjusting the duty cycle of the $V_{control}$, the voltage gain can be modified according to the voltage gain vs. duty cycle curve of buck converters (which can be seen in Fig. 1.13).

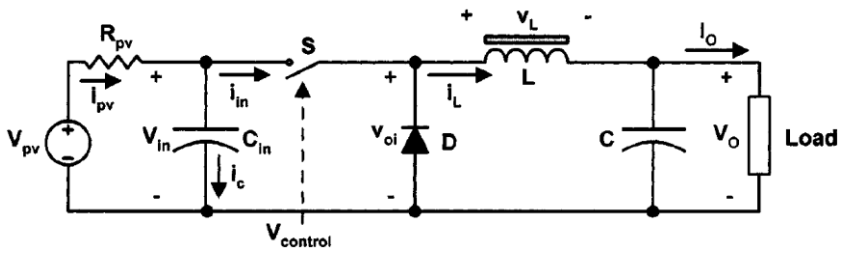


Fig. 1.12: Equivalent circuit of a buck-converter-based PV system. Figure from [5].

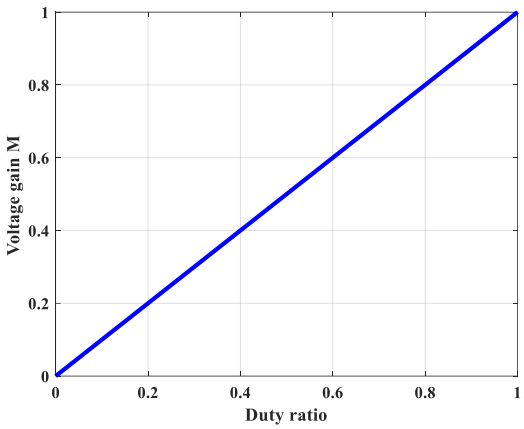


Fig. 1.13: Voltage gain vs. duty ratio curve of buck converters.

Boost converters, or step-up converters, are employed when the output voltage of the PV panel is lower than the load voltage. The voltage gain vs. duty cycle curve is plotted in Fig. 1.14.

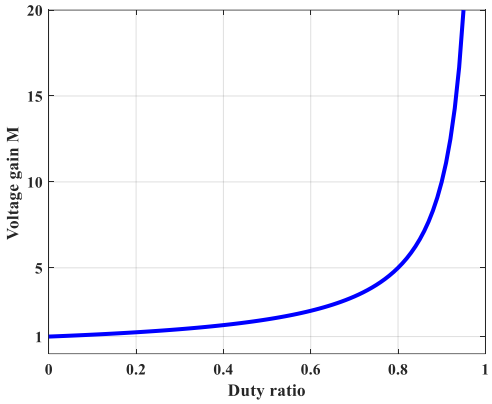


Fig. 1.14: Voltage gain vs. duty cycle curve of boost converters.

When the MPPT algorithm is utilized, the PV array operates at the MPP. However, the actual power delivered to the load still relies on the converter's efficiency, even when operating at the MPP. As a result, the choice of converter and design method significantly impacts the output power. In addition to efficiency, other factors such as the converter's size, voltage stress of components, and electromagnetic interference (EMI) performance should also be considered.

Soft-switching techniques:

Conventional buck and boost converters have been widely used in power electronics but suffer significant switching losses due to the large voltage and current transients during each switching cycle. This drawback can lead to reduced overall efficiency, especially in high-frequency applications.

Several studies have been proposed to discuss the challenges of switching losses and EMI that arise with higher switching frequencies in pulse-width modulated (PWM) switching converters. Passive soft-switching techniques [14] are presented as a solution to reducing these losses, as they do not require an extra switch or additional control circuitry. The article describes the necessary components, such as a small inductor and capacitor, to achieve passive zero voltage and zero current switching operations. Fig. 1.15a shows an example of passive soft-switching topology with a boost converter.

[15] compares a group of active soft-switching converters that utilize an auxiliary switch with an inductor and aims to identify the losses in the auxiliary circuit that may affect the overall efficiency of the converter. The paper concludes that soft-switching techniques can significantly improve efficiency in high-frequency power conversion. However, carefully considering circuit design and component selection is necessary to achieve the best results. An illustration of an active soft-switching topology with a boost converter is presented in Fig 1.15b.

[16] discusses lossless soft-switching methods for converters, which can be active or passive. While active methods can significantly reduce losses in the main switch, they transfer some losses to the auxiliary circuit and require extra switches or control

circuitry. Passive methods only provide ZVS and ZCS operation of the main switch, but the method features simplicity, lower cost, and higher reliability compared to active approaches.

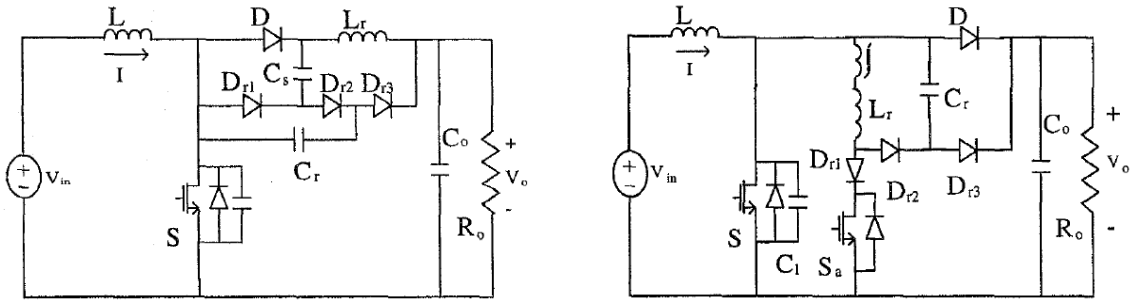


Fig. 1.15: Example of soft-switching methods with boost topologies. (a) Passive soft-switching method. (b) Active soft-switching method. Figure from [16].

Resonant converters:

Resonant converters utilize resonant components, like capacitors and inductors, to reduce switching losses, making them a soft-switching technique [17]. The switching element, typically a transistor or MOSFET, is controlled to switch around the resonant frequency of the resonant circuit. This allows the switching elements to operate in ZVS and ZCS operations. By adjusting the resonant frequency of the circuit, the converter can adapt to changes in load and input voltage [18]. Moreover, resonant converters can operate at higher frequencies than conventional converters, reducing the size and cost of passive components.

There are various types of resonant converters [17] [19], including series-resonant, parallel-resonant, and series-parallel resonant converters, each with distinct advantages and disadvantages depending on the application requirements. Among

them, the series resonant converter has a step-down voltage conversion ratio and is the focus of this article.

Several comprehensive analyses for series resonant converters have been published [17] [19] [20]. The SRC's voltage gain–switching frequency curve has been derived in the literature. An example plot of voltage gain vs. normalized frequency is depicted in Fig. 1.16.

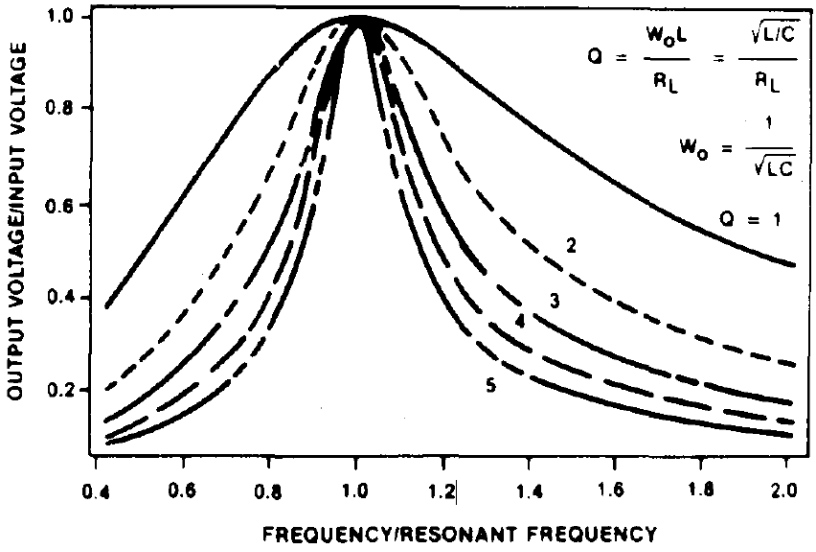


Fig. 1.16: Example of resonant converter's voltage gain vs. normalized frequency. Figure from [19].

Traditional resonant converters typically use the frequency modulation (FM) method to maintain resonant operation under changing load conditions or input voltage by varying the frequency of the switching signal. However, as shown in Fig. 1.16, the switching frequency range goes infinite to achieve full range (0 to 1) voltage gain regulation, especially within light load conditions (low quality factor Q). However, voltage regulation ability is essential for applications like PV systems and MPPT since the system needs to shift between different voltage ranges to achieve power tracking and needs this ability to deal with different environmental conditions.

To address this issue, the method proposed in [21] introduces a fixed on-time modulation (FTM) method for resonant switched-capacitor converters. The FTM method is further utilized in [22], [23], and [24] for half-bridge SRCs to achieve full-range voltage regulation within a limited switching frequency range.

Full-Range Regulation Method for Series Resonant Converter [22]

Article [22] presents a fixed on-time modulation approach for the half-bridge SRC. The aim is to enable full-range voltage regulation within a restricted switching frequency range. This FTM method also allows for zero voltage turn-on for transistors and zero current turn-off for diodes. The following section discusses the operation principle, control scheme, and voltage regulation performances.

Fig. 1.17 depicts the structure of the half-bridge SRC, wherein S_1 and S_2 are the MOSFETs that come with antiparallel diodes, while D_1-D_4 are the power diodes. The resonant tank consists of an inductor L_r and a capacitor C_r. The resonant frequency f_r of an SRC is defined by the resonant tank, which is

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

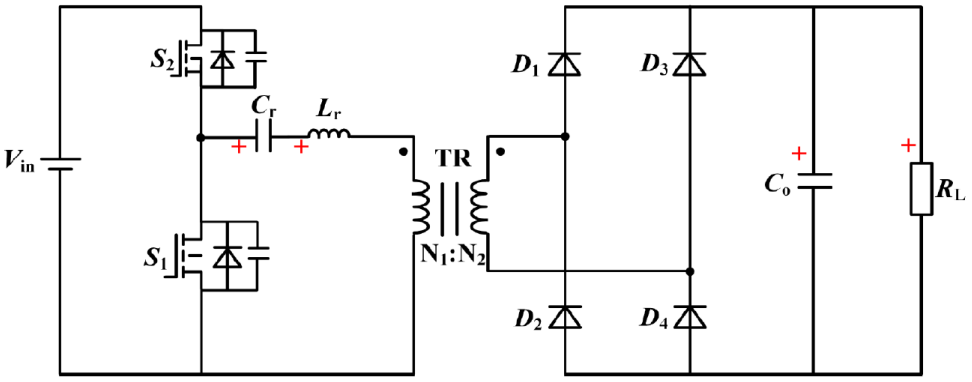


Fig. 1.17: Scheme diagram of the half-bridge SRC. Figure from [22].

The FTM method employs a constant turn-on time for the transistor S_1, expressed as

$$t_{on} = \frac{1}{2f_r} \tag{2}$$

Fig. 1.18 illustrates the control scheme employed by the FTM method. Using equation (2), the duty cycle of transistor S_1, denoted by d_1, can be calculated as

$$d_1 = \frac{F}{2} \tag{3}$$

where F is the normalized frequency given by

$$F = \frac{f_s}{f_r} \tag{4}$$

with f_s representing the switching frequency of the SRC. The duty cycle d_2 of transistor S_2 is defined as

$$d_2 = 1 - d_1 \tag{5}$$

which varies from 0.5 to 0 as the normalized frequency F increases from 1 to 2.

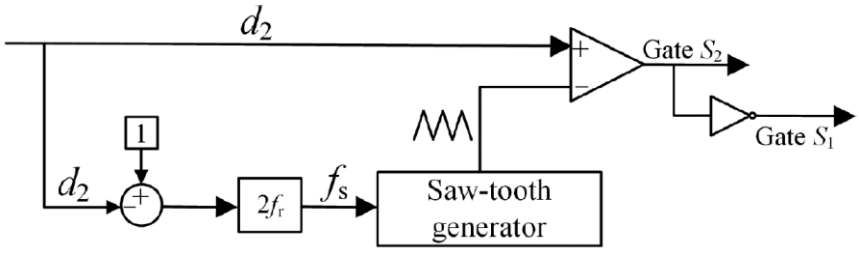


Fig. 1.18: Control scheme employed by the FTM method. Figure from [22].

The four switching states of the half-bridge SRC can be seen in Fig. 1.19, along with their corresponding operating waveforms shown in Fig. 1.20. The first switching state, shown in Fig. 1.19a, occurs between t_0 and t_1 with transistor S_2 still turned on and diodes D_1 and D_4 conducting. At t_0, the resonant current i_{Lr} increases until t_1, when transistor S_2 turns off. The second switching state, shown in Fig. 1.19b, occurs from t_1 to t_3, with transistor S_1 turning on at t_2. During this period, the resonant current decreases from t_1 to zero at t_3. From t_3 to t_4, depicted in Fig. 1.19c, the resonant current reverses and swings

until transistor S_1 turns off. Finally, during t_4 to t_6, shown in Fig. 1.19d, the resonant current value gradually decreases and reaches zero at t_6, and the same cycle repeats.

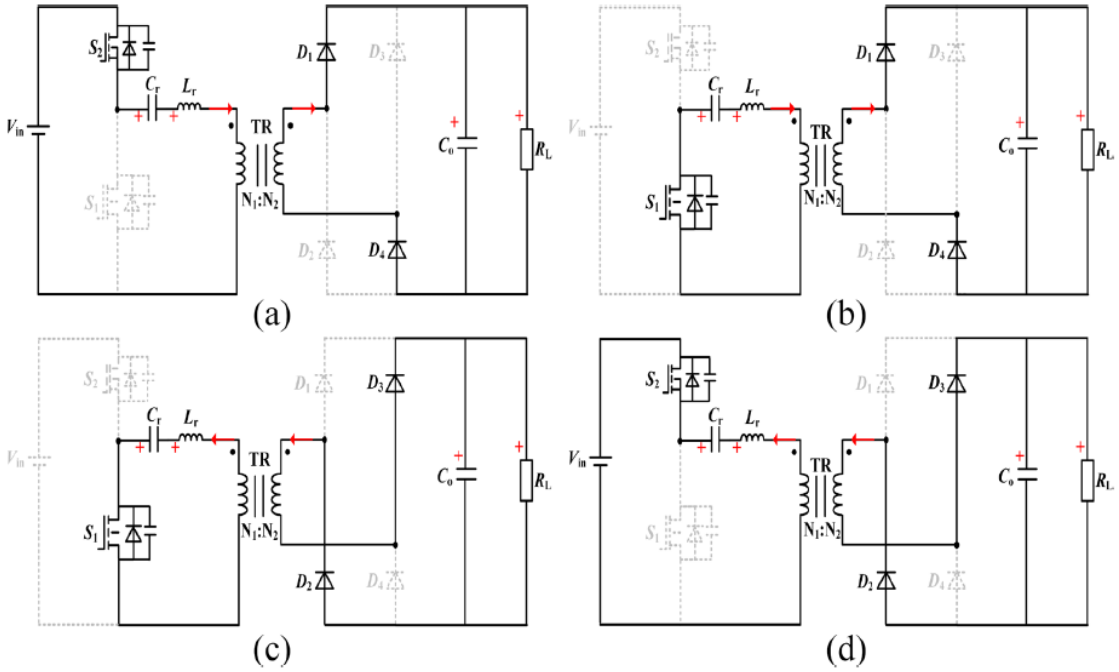


Fig. 1.19: Switching states of the half-bridge SRC. (a) State 1 [t_0, t_1]. (b) State 2 [t_1, t_3]. (c) State 3 [t_3, t_4]. (d) State 4 [t_4, t_6]. Figure from [22].

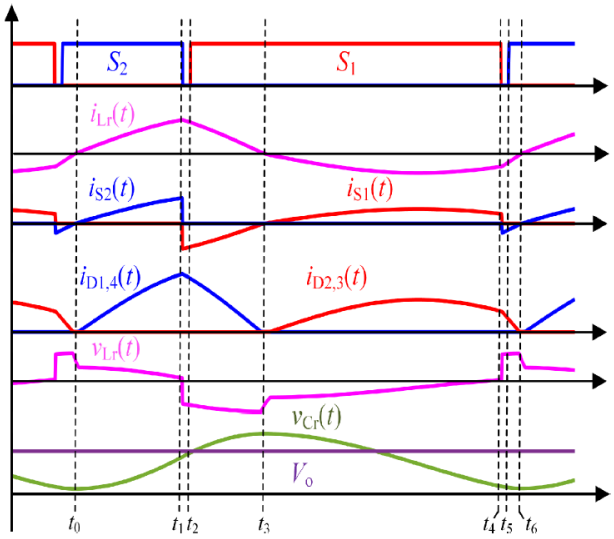


Fig. 1.20: Theoretical operating waveforms of the half-bridge SRC. Figure from [22].

Fig. 1.21a depicts the voltage gain curves of the SRC as a function of duty ratio d_2, and Fig. 1.21b describes the voltage gain curve with normalized frequency F for various load resistances R_L and with components specified in [22]. It can be observed from the plots that the SRC is capable of achieving full-range voltage regulation over the normalized frequency range of F = 1 to 2 by varying the duty ratio d_2 from 0.5 to 0.

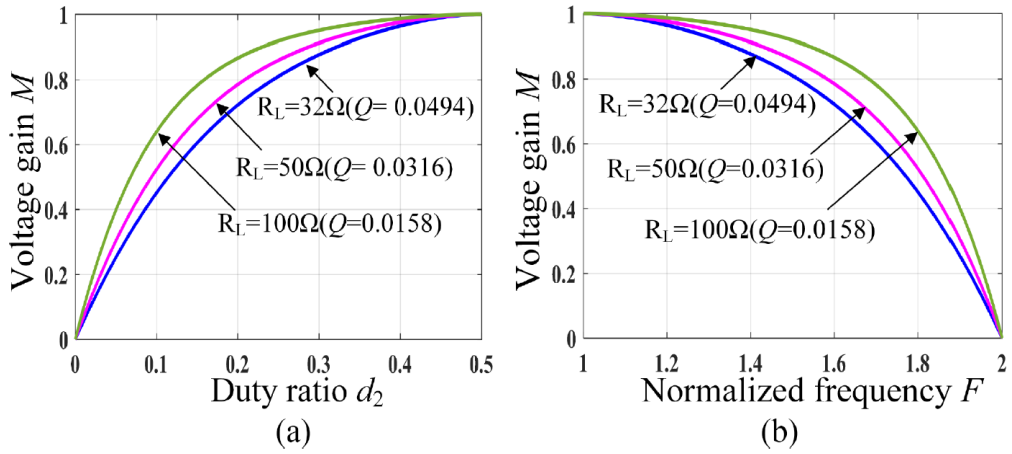


Fig. 1.21: Voltage gain curves of the FTM method. (a) Voltage gain vs. duty ratio d_2. (b) Voltage gain vs. normalized frequency. Figure from [22].

Article [22] compared the Frequency Modulation (FM) and FTM methods by presenting the voltage gain-normalized frequency curves in Fig. 1.22. The FM method can theoretically achieve complete regulation across the full range of operations with an infinite switching frequency. Fig. 1.22 demonstrates that the FM method's voltage gain is limited to a range of 0.6 to 1, which decreases even further with lower Q values. In contrast, the FTM method can achieve complete regulation across the full range of operations with a smaller range of switching frequencies.

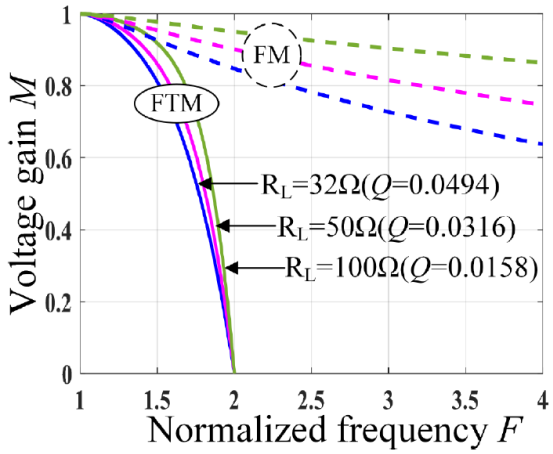


Fig. 1.22: Voltage regulation range with the FM and the FTM methods.

Figure from [22].

CHAPTER 2: Fixed On-time Series Resonant Converter for MPPT Application

System Overview

The proposed system block diagram in Fig. 2.1 illustrates a PV power system with MPPT control using a half-bridge SRC. This system comprises a PV panel and battery set with load interfaced through a half-bridge SRC. Voltage and current sensors are incorporated to measure the V_{PV} and I_{PV}. These measurements are then used by the microcontroller and generate the duty signal for the half-bridge SRC to implement the MPPT algorithm. The MPPT algorithm ensures the PV panel operates at its maximum power point, which is achieved by continuously adjusting the duty cycle of the SRC's switching signals to maintain the highest output power of the PV panel.

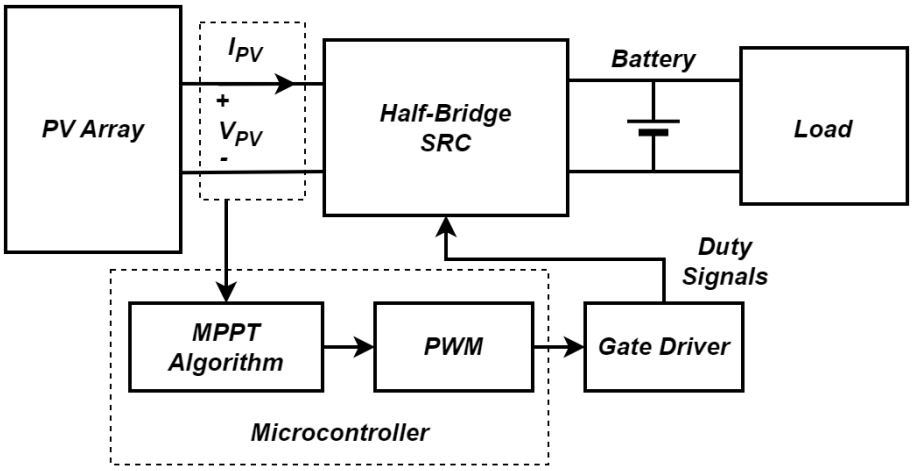


Fig. 2.1: Block diagram of the proposed PV power system.

The half-bridge SRC implemented in the PV power system is illustrated in Fig. 2.2. This SRC is responsible for converting the input power from the PV array port, denoted as V_{in}, into a usable form that can be delivered to the load. The SRC comprises two MOSFETs, S_1 and S_2, each with internal antiparallel diodes. The MOSFETs operate

complementary, allowing the SRC to achieve a more efficient operation than other converter topologies. The parasitic capacitances are also modeled, which significantly impact the switching performance in the practical use of MOSFETs and are addressed by the soft-switching techniques.

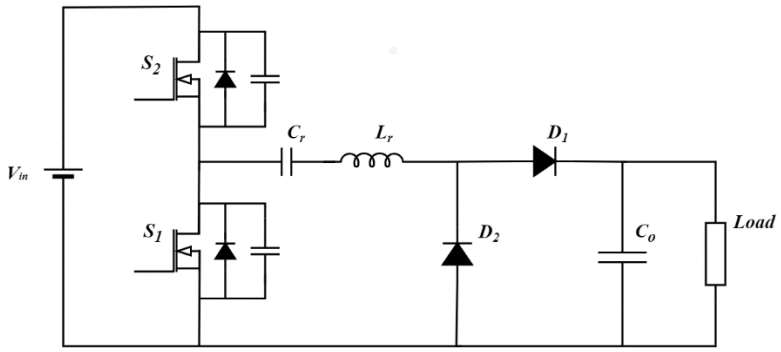


Fig. 2.2: Topology of the half-bridge SRC.

The resonant tank of the SRC is composed of an inductor, L_r, and a capacitor, C_r. The resonant tank stores energy when the S_2 is switched on then releases the stored energy to the output capacitor and loads when the S_2 is switched off. During the operation of the SRC, the MOSFETs switch on and off at a specific frequency, causing the resonant tank to store and release energy in a resonant manner.

Furthermore, the SRC also consists of power diodes D_1 and D_2. These diodes provide a path for the energy to flow when the MOSFETs switch alternately. The output capacitor C_o is expected to be sufficiently large, ensuring the output voltage remains stable with minimal fluctuation.

The FTM control method for the SRC is similar to [22] and the same as the one proposed in [24], described in Fig. 1.14. To simplify the description of the control scheme and the equations from (1) to (5), Table 2.1 shows the critical parameters for the FTM control method used in this system.

Table 2.1: Parameters for FTM control topology

Symbol	Description	Formula
f_s	Switching frequency of S_1 and S_2	
f_r	Resonant frequency	$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$
F	Normalized frequency	$F = \frac{f_s}{f_r}$
d_1	Duty cycle of S_1	$d_1 = \frac{F}{2}$
d_2	Duty cycle of S_2	$d_2 = 1 - d_1$
t_{on}	Turn-on time of S_1	$t_{on} = \frac{1}{2f_r}$

Detailed Analysis [24]

This section examines how the half-bridge SRC operates with the FTM control method. Additionally, the calculations for the voltage and current of the resonant tank and derivation of the voltage gain equation are performed.

The equivalent circuits of the four switching states of the half-bridge SRC are illustrated in Fig. 2.3, with the operation waveforms for each state shown in Fig. 2.4. Fig. 2.4 illustrates that the switching signals for transistors S_1 and S_2 are conducted complementarily. The turn-on time for S_1 is set as described in equation (2) to satisfy the FTM control method. The detailed analysis for each state is illustrated as follows.

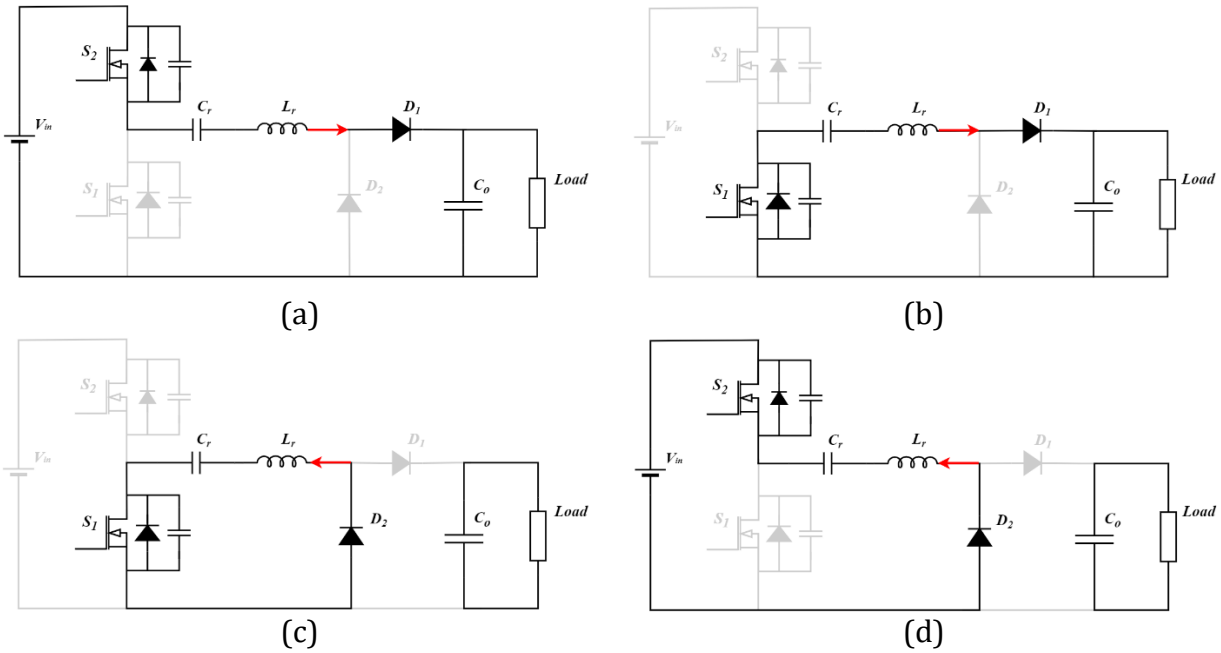


Fig. 2.3: Switching states of the half-bridge SRC. (a) State 1 [t_0 to t_1]. (b) State 2 [t_1 to t_3]. (c) State 3 [t_3 to t_4]. (d) State 4 [t_4 to t_6].

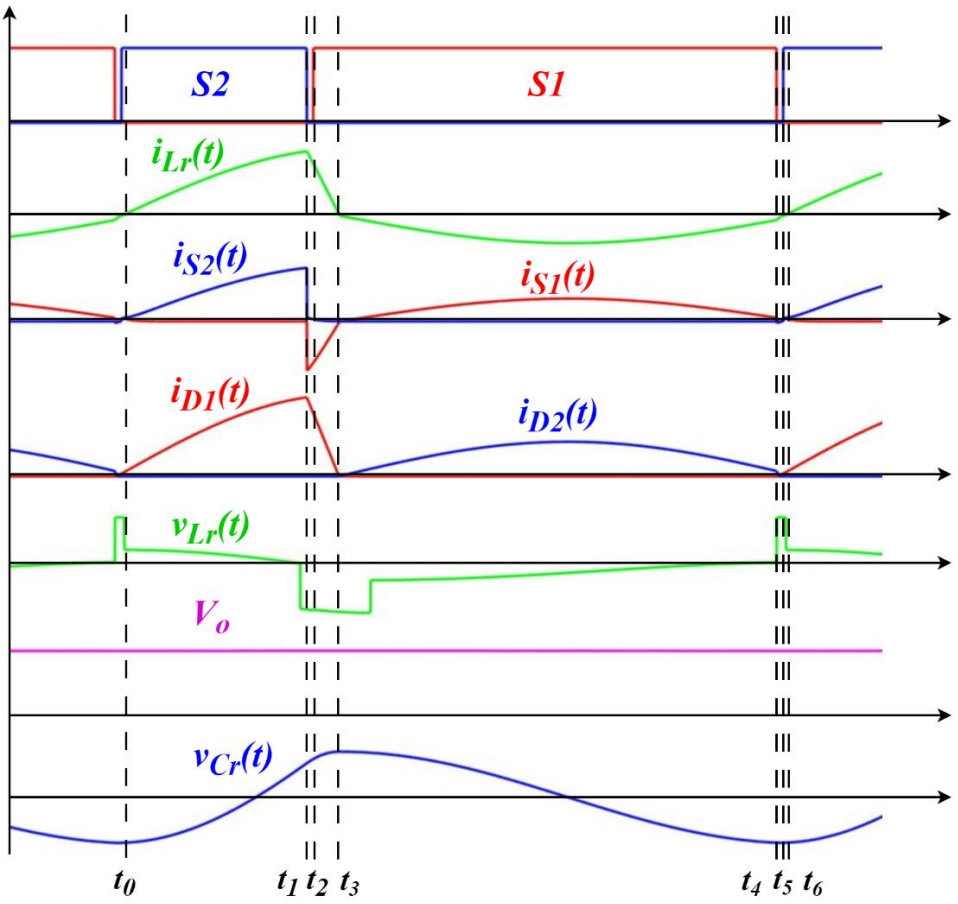


Fig. 2.4: Operation waveforms for the half-bridge SRC.

State 1 [t_0-t_1]: As shown in Fig. 2.4, the half-bridge SRC undergoes several changes from t_0 to t_1. Before t_0, the transistor S_2 is turned on, and the current flowing through the resonant inductor, $i_{Lr}(t)$, is negative. However, at t_0, the current $i_{Lr}(t)$ decreases and eventually reaches zero. At the same time, the voltage across the resonant capacitor, $v_{Cr}(t)$, decreases to its minimum value, V_{Cr_min}.

At t_0, power diode D_1 begins to conduct, while power diode D_2 turns off with diode current i_{D2} closed to zero, which performs ZCS operation. As a result, the resonant inductor current $i_{Lr}(t)$ begins to increase and continues until t_1. At t_1, transistor S_2 turns off, marking the end of this period.

By applying Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) for Fig. 2.3a, the following equations are obtained:

$$V_{in} - v_{Cr}(t) - V_o = L_r \frac{di_{Lr}(t)}{dt} \tag{6}$$

$$i_{Lr}(t) = C_r \frac{dv_{Cr}(t)}{dt} \tag{7}$$

As observed from Fig. 2.4, the boundary conditions for this period are

$$i_{Lr}(t_0) = 0 \tag{8}$$

$$v_{Cr}(t_0) = V_{\text{Cr\_min}} \tag{9}$$

In equation (6), by substituting $i_{Lr}(t)$ with equation (7), the second-order differential equations for $v_{Cr}(t)$ can be derived as

$$\frac{d^2 v_{Cr}(t)}{dt^2} - \frac{v_{Cr}(t)}{L_r C_r} = \frac{V_{in} - V_o}{L_r C_r} \tag{10}$$

In the same way, by substituting $v_{Cr}(t)$ in equation (7), the second-order differential equations for $i_{Lr}(t)$ can be derived as

$$\frac{d^2 i_{Lr}(t)}{dt^2} + \frac{i_{Lr}(t)}{L_r C_r} = 0 \tag{11}$$

From equations (10) and (11), the resonant voltage can be derived as

$$v_{Cr}(t) = V_{in} - V_o - (V_{in} - V_o - V_{\text{Cr\_min}}) \cos[\frac{1}{\sqrt{L_r C_r}}(t - t_0)] \tag{12}$$

To introduce resonant frequency f_r from equation (1), the resonant inductance and capacitance can be substituted f_r by

$$\frac{1}{\sqrt{L_r C_r}} = 2\pi f_r \tag{13}$$

The equation (12) can be rewritten as

$$v_{Cr}(t) = V_{in} - V_o - (V_{in} - V_{\text{Cr\_min}} - V_o)\cos[2\pi f_r(t - t_0)] \quad (14)$$

Similarly, from equations (10) and (11), the resonant current can be derived as

$$i_{Lr}(t) = (V_{in} - V_o - V_{\text{Cr\_min}})\sqrt{\frac{C_r}{L_r}}\sin[2\pi f_r(t - t_0)] \quad (15)$$

State 2 [t_1-t_3]: At t_1, transistor S_2 is turned off, causing the internal antiparallel diode of S_1 to conduct. After a small amount of dead time between the two switching signals, S_1 is turned on at t_2 with zero voltage across the drain-to-source of the transistor, which fulfills ZVS operation.

Within this period, the resonant tank's energy consistently decreases, reflecting on the resonant inductor current $i_{Lr}(t)$, and the slope of the resonant capacitor voltage $v_{Cr}(t)$ gradually decreases.

By the end of this period at t_3, the resonant inductor current $i_{Lr}(t)$ has decreased to zero, and the resonant capacitor voltage $v_{Cr}(t)$ reaches its maximum value V_{Cr_max}.

The KVL and KCL equations obtain from Fig. 2.3c are

$$-v_{Cr}(t) - V_o = L_r\frac{di_{Lr}(t)}{dt} \quad (16)$$

$$i_{Lr}(t) = C_r\frac{dv_{Cr}(t)}{dt} \quad (17)$$

By examining Fig. 2.4, the boundary conditions are

$$i_{Lr}(t_3) = 0 \quad (18)$$

$$v_{Cr}(t_3) = V_{\text{Cr\_max}} \quad (19)$$

With the same derivation process above, the resonant voltage and current are:

$$v_{Cr}(t) = -V_o + (V_{\text{Cr\_max}} + V_o)\cos[2\pi f_r(t - t_3)] \tag{20}$$

$$i_{Lr}(t) = -(V_o + V_{\text{Cr\_max}})\sqrt{\frac{C_r}{L_r}}\sin[2\pi f_r(t - t_3)] \tag{21}$$

State 3 [t_3-t_4]: At t_3, the resonant inductor current $i_{Lr}(t)$ reaches zero and begins to swing in to reverse direction. Power diode D_2 turns on while diode D_1 turns off with ZCS operation. At t_4, transistor S_1 switches off, and the internal antiparallel diode of the transistor S_2 starts conducting. The resonant capacitor voltage $v_{Cr}(t)$ decreases within the whole period.

The KVL and KCL equations derived from Fig. 2.3c are

$$-v_{Cr}(t) = L_r\frac{di_{Lr}(t)}{dt} \tag{22}$$

$$i_{Lr}(t) = C_r\frac{dv_{Cr}(t)}{dt} \tag{23}$$

Similarly, from Fig. 2.4, the boundary conditions are

$$i_{Lr}(t_3) = 0 \tag{24}$$

$$v_{Cr}(t_3) = V_{\text{Cr\_max}} \tag{25}$$

With equations (22)(23)(24)(25), the resonant voltage and current for the period can be expressed as

$$v_{Cr}(t) = V_{\text{Cr\_max}}\cos[2\pi f_r(t - t_3)] \tag{26}$$

$$i_{Lr}(t) = -V_{\text{Cr\_max}}\sqrt{\frac{C_r}{L_r}}\sin[2\pi f_r(t - t_3)] \tag{27}$$

State 4 [t_4-t_6]: At t_4, the switching process continues as transistor S_1 turns off, and the internal antiparallel diode of transistor S_2 begins to conduct current. With a small amount of dead time, transistor S_2 turns on at t_5 with ZVS operation. During this state,

the capacitor voltage, $v_{Cr}(t)$, continues to decrease until t_6, where the period ends, and a new cycle begins.

The KVL and KCL equations from Fig. 2.3c can be found as

$$V_{in} - v_{Cr}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{28}$$

$$i_{Lr}(t) = C_r \frac{dv_{Cr}(t)}{dt} \tag{29}$$

In Fig. 2.4, the boundary conditions for this period are

$$i_{Lr}(t_6) = 0 \tag{30}$$

$$v_{Cr}(t_6) = V_{\text{Cr\_min}} \tag{31}$$

With equations (28)(29)(30)(31), the resonant voltage and current can be acquired as below.

$$v_{Cr}(t) = V_{in} - (V_{in} - V_{\text{Cr\_min}}) \cos[2\pi f_r (t - t_6)] \tag{32}$$

$$i_{Lr}(t) = (V_{in} - V_{\text{Cr\_min}}) \sqrt{\frac{C_r}{L_r}} \sin[2\pi f_r (t - t_6)] \tag{33}$$

Full-range Voltage Gain

The steps outlined in [21] and [24] can be followed to derive the voltage gain. A control variable, h, is defined as

$$h = cos\left(\frac{2\pi d_2}{F}\right) \tag{34}$$

to derive the voltage gain, comprised of the duty cycle d_2 and the normalized switching frequency F. The characteristic impedance is described as

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{35}$$

which consist of the resonant inductor and capacitor. The quality factor, which composes of the ratio of impedance to the load, is defined as

$$Q = \frac{Z_r}{R_L} \tag{36}$$

Another variable defined to simplify the derivation of voltage gain is

$$m = C_r R_L f_s = \frac{F}{2\pi Q} \tag{37}$$

From the switching state 1 (t_0-t_1) to stage 2 (t_1-t_3), the resonant capacitor is charged from v_{Cr_min} to v_{Cr_max}. The average dc voltage across C_r in state 1 and state 2 are defined as V_{Cr_T1} and V_{Cr_T2}, respectively.

$$V_{C_{r\_T1}} = \frac{1}{T_1}\int_{t_0}^{t_1} v_{Cr}(t)dt \tag{38}$$

$$V_{C_{r\_T2}} = \frac{1}{T_2}\int_{t_1}^{t_3} v_{Cr}(t)dt \tag{39}$$

where $T_1 = t_1$-t_0 and $T_2 = t_3$-t_1.

The following equation can be derived by applying the principles of voltage-

second balance to L_r during the time from state 1 to state 2.

$$T_1\left(V_{in} - V_o - V_{C_{r\_T1}}\right) + T_2\left(-V_o - V_{C_{r\_T2}}\right) = 0 \tag{40}$$

By manipulating the equations (14), (20), (38) ~ (40), the following equation can be derived.

$$\left(V_{in} - V_{\text{Cr\_min}} - V_o\right)\sin[2\pi f_r(T_1)] - \left(V_{\text{Cr\_max}} + V_o\right)\sin[2\pi f_r(T_2)] = 0 \tag{41}$$

By applying the equations

$$\sin[2\pi f_r(T_1)] = \sqrt{1 - \cos[2\pi f_r(T_1)]^2} \tag{42}$$

and

$$\cos[2\pi f_r(T_1)] = cos\left[2\pi f_r\left(\frac{d_2}{f_s}\right)\right] = h \tag{43}$$

to equation (41), the following equation can be derived.

$$\sin[2\pi f_r(T_2)] = \frac{\left(V_{in} - V_{\text{Cr\_min}} - V_o\right)}{\left(V_{\text{Cr\_max}} + V_o\right)}\sqrt{1 - h^2} \tag{44}$$

The application of the charge balance principle to C_r during a single switching cycle results in the following:

$$\int_{t_0}^{t_1} i_{Lr}(t)dt + \int_{t_1}^{t_3} i_{Lr}(t)dt + \int_{t_3}^{t_4} i_{Lr}(t)dt + \int_{t_4}^{t_6} i_{Lr}(t)dt = 0 \tag{45}$$

Reorganizing equations (15), (21), (27), (33), (43), and (45) leads to the following equation:

$$\cos[2\pi f_r(T_2)] = \frac{\left(V_{in} + V_{\text{Cr\_max}} - V_{\text{Cr\_min}}\right)}{\left(V_{\text{Cr\_max}} + V_o\right)} - \frac{\left(V_{in} - V_{\text{Cr\_min}} - V_o\right)}{\left(V_{\text{Cr\_max}} + V_o\right)}h \tag{46}$$

Performing the principle of charge balance to the output capacitor C_o during one switching cycle yields

$$C_r\left(V_{\text{Cr\_max}} - V_{\text{Cr\_min}}\right) = \frac{V_o}{R_L}\frac{1}{f_s} \tag{47}$$

Applying equations (37) and (47) yields the equation for output voltage:

$$V_o = m\left(V_{\text{Cr\_max}} - V_{\text{Cr\_min}}\right) \tag{48}$$

Also, from Fig. 2.4 and equation (14), the equation for input voltage can be derived as:

$$V_{in} = 2\left(V_{\text{Cr\_max}} + V_{\text{Cr\_min}}\right) + V_o \tag{49}$$

By solving the set of equations (44), (46), (48), and (49), the following expression can be obtained:

$$M = \frac{V_o}{V_{in}} = \frac{4m(h-1) - 2h + \sqrt{[4m(h-1) - 2h]^2 - 32m(h-1)}}{4} \tag{50}$$

Fig. 2.5 shows the voltage gain curves for the half-bridge SRC with the FTM control method. These curves are calculated using equation (50), with three load resistances: 69 Ω, 14.5 Ω, and 7.3 Ω, corresponding to quality factor Q values of 0.0229, 0.1087, and 0.2176, respectively. These particular load resistance values were chosen to meet the experiment specifications related to the chosen PV array for the MPPT method.

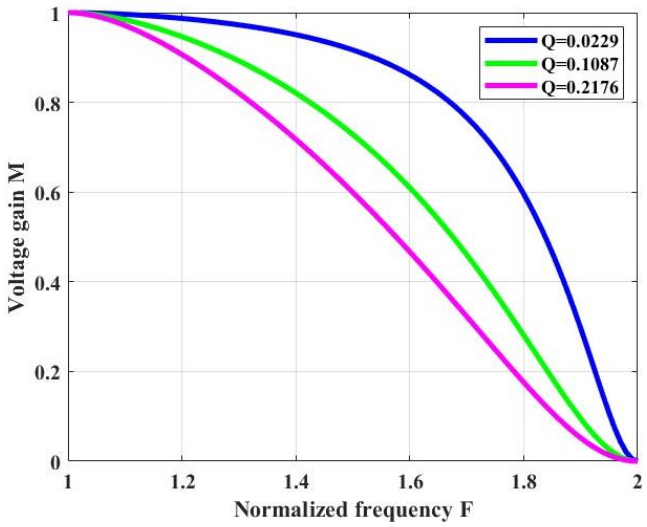
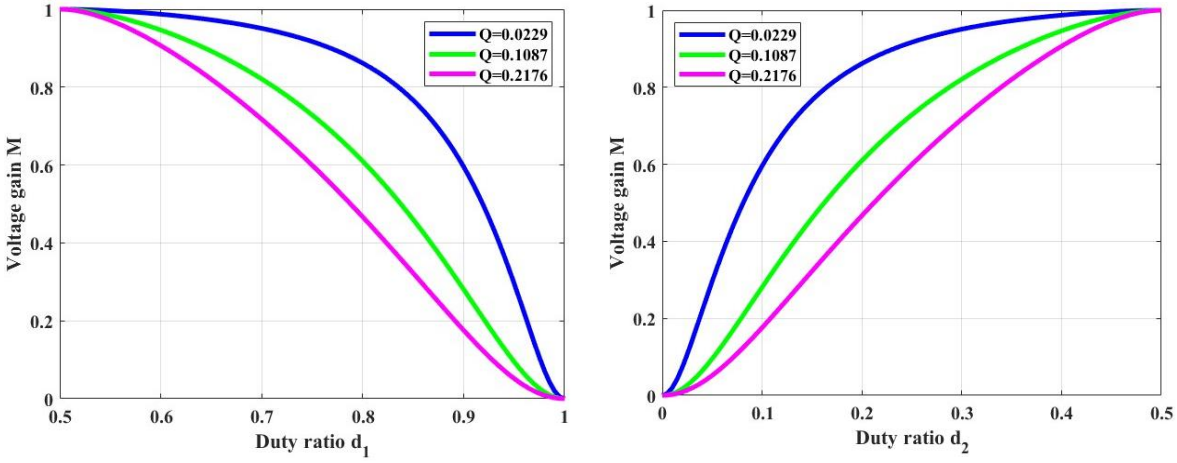


Fig. 2. 5: Voltage gain curves of the half-bridge SRC.

The voltage gain curves shown in Fig. 2.5 demonstrate the ability to regulate in full voltage range within the normalized frequency range of F = 1~2. Fig. 2.6 displays the voltage gain vs. duty ratio curve for the switching signals d_1 and d_2, respectively. It should be clear that the half-bridge SRC utilizing the fixed on-time modulation method achieves full range regulation within a limited frequency range.



(a) (b)

Fig. 2.6: (a) Voltage gain vs. duty ratio d_1. (b) Voltage gain vs. duty ratio d_2.

MPPT Implementation

While there have been some concerns regarding the shortcomings of the P&O algorithm [2], it remains a widely used and effective method for implementing maximum power point tracking applications.

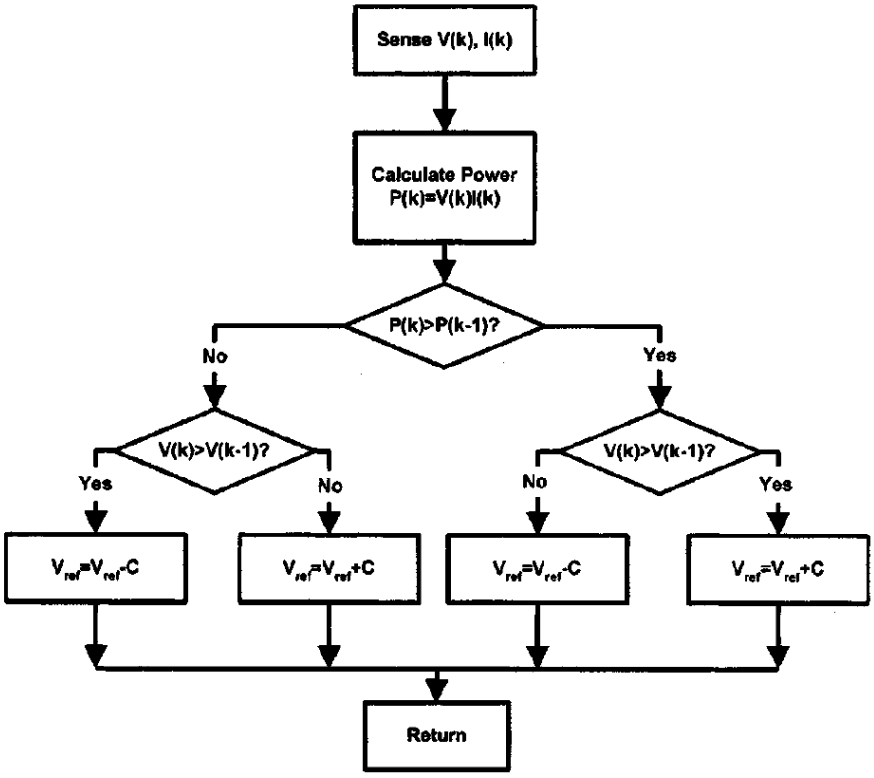


Fig. 2.7: The flowchart of perturbation and observation algorithm. Figure from [5].

The fundamental approach of the P&O algorithm involves perturbing the operating voltage to reach the maximum power operating point. These perturbations can be either in the direction of increasing or decreasing the voltage. If the power generated by the PV array increases in response to a given perturbation, it means that the operating point has moved closer to the MPP. In this case, the operating voltage should be moved further in the same direction. Conversely, if the power of the PV array is reduced, the direction of the operating voltage movement should be reversed.

Implementing the P&O algorithm involves several steps, as illustrated in the flowchart depicted in Fig. 2.7. The voltage sensing and current sensing circuits are initially used to sense the voltage V(k) and current I(k) generated from the PV array. These values are then used to calculate the power P(k) the PV array generates. Next, the PV power P(k) is compared with the P(k-1) obtained during the previous iteration.

If the equation P(k)>P(k-1) is true, it indicates that the present operating point can be one of the two possible situations, as shown in Fig. 2.8. One possible situation is that the operation point is on the left-hand side of the MPP, with the perturbation increasing the PV array's voltage toward the MPP. The other possible situation is that the operation point is on the right-hand side of the MPP, with the PV array's voltage decreasing toward the MPP.

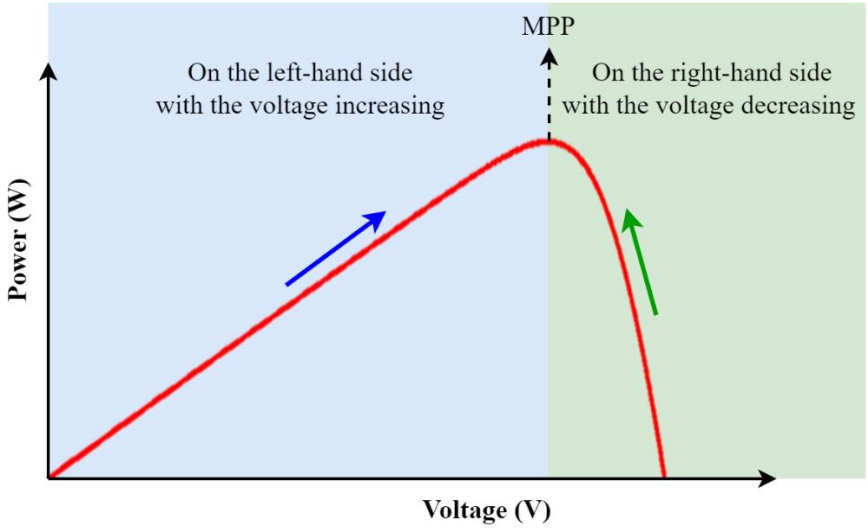


Fig. 2.8: Operation principles of P&O algorithm.

The present PV array voltage V(k) is compared with the previous voltage V(k-1) to determine which operation point it is in the current operation status. If the present voltage is higher than the previous voltage, it suggests that the operating point is on

the left-hand side of the MPP. In such a scenario, the reference voltage of the saw-tooth signal generating the duty signal is adjusted to increase the operating voltage further and enhance the power output. The decision logic employed in this situation can be applied to different scenarios shown in Fig. 2.7.

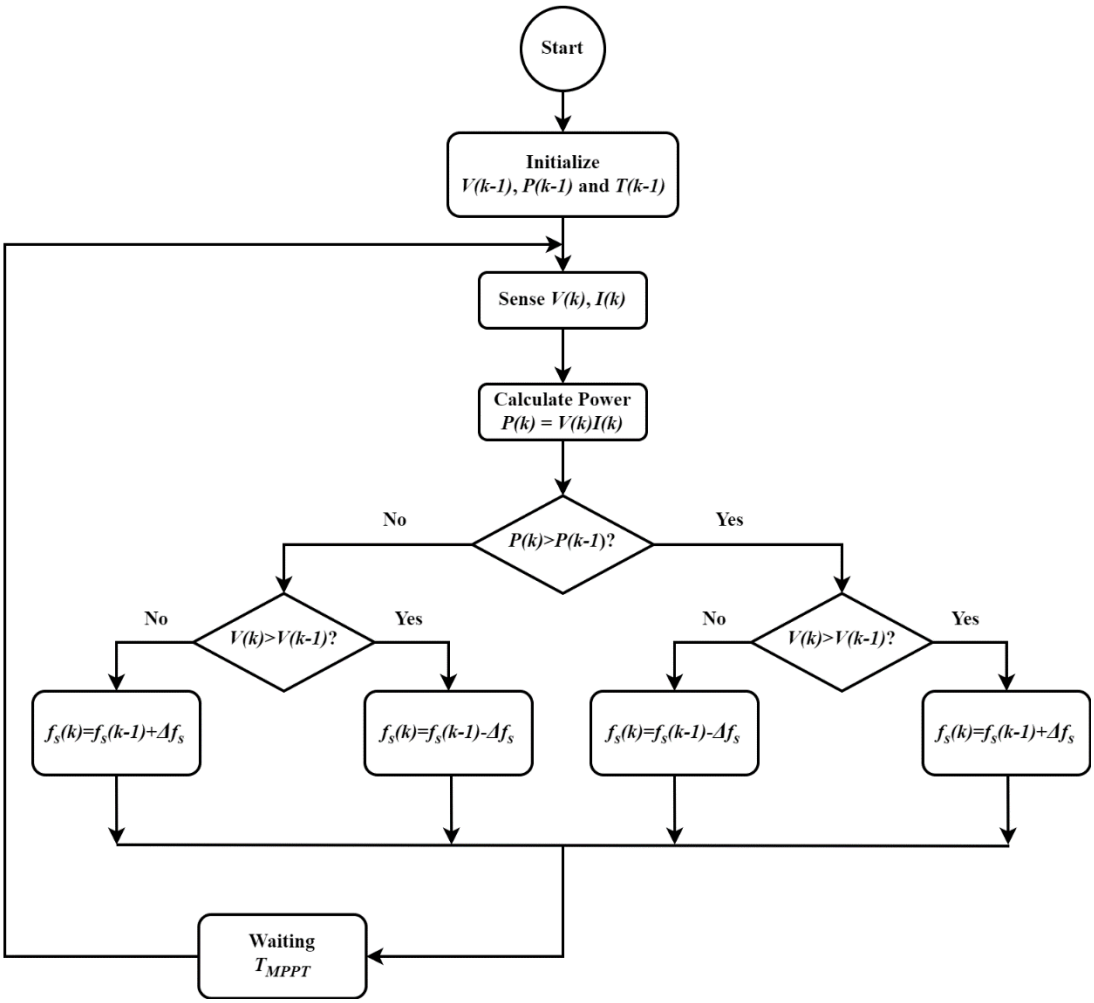


Fig. 2.9: The flowchart of the FTM-based P&O algorithm.

In the fixed on-time topology, the switching frequency is adjusted to regulate the voltage gain while maintaining a constant turn-on time determined by the resonant frequency. This feature enables the half-bridge SRC to achieve full-range voltage gain modulation. Fig. 2.9 depicts the flowchart of the FTM-based P&O algorithm.

In contrast to the conventional P&O topology, which modifies the duty ratio by perturbing the reference voltage compared with the saw-tooth signal, the fixed on-time topology modifies the switching frequency of the saw-tooth signal to impact the voltage gain. The parameter $f_s(k)$ shown in Fig. 2.9 represents the switching frequency of the current iteration.

The perturbation step size of switching frequency, defined as Δf_s, added or deducted from the frequency $f_s(k)$ after each MPPT iteration, is used to execute the perturbation to alter the operating point. According to equation (4), Δf_s can be expressed as a percentage of resonant frequency f_r since the switching frequency f_s range between f_r to $2f_r$.

The trigger frequency of the MPPT algorithm, denoted as f_{MPPT}, has the potential to impact the speed of reaching the MPP. The parameter T_{MPPT}, which indicates the waiting time between each trigger of the MPPT algorithm, is defined as

$$T_{MPPT} = \frac{1}{f_{MPPT}} \tag{51}$$

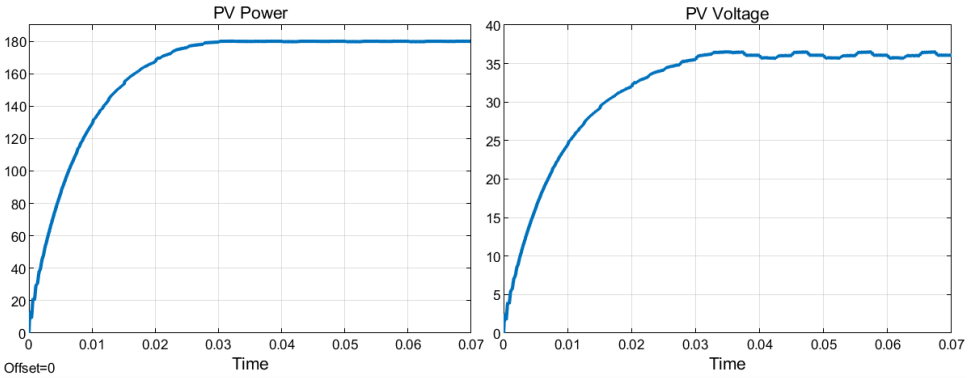
The speed of reaching the maximum power point and the steady-state performance of the PV system can be significantly impacted by the parameter settings of f_{MPPT} and Δf_s. High values of these parameters can help the system overcome rapid environmental changes. However, they can also result in significant steady-state oscillations, leading to a large output voltage and power ripple.

After reaching the maximum power point, the P&O algorithm experiences steady-state oscillations due to the algorithm feature, where the switching period oscillations

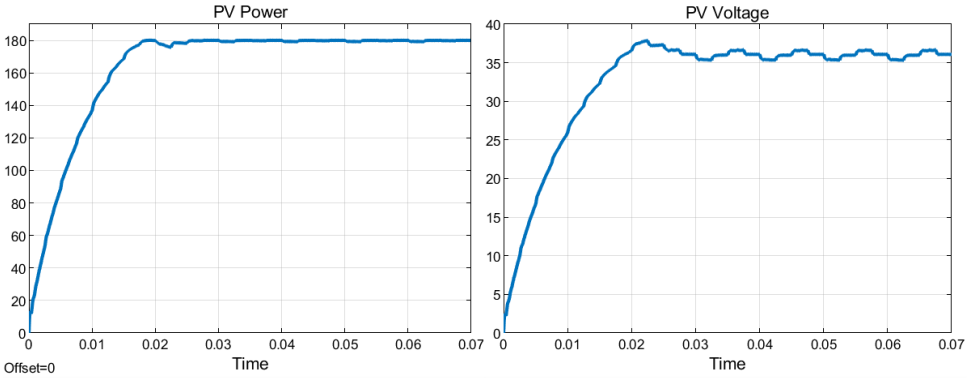
between $f_s(k_{MPP})$-Δf_s, $f_s(k_{MPP})$, and $f_s(k_{MPP})$+Δf_s (3-level oscillations in [11]). With a large Δf_s, the oscillation can be significant, leading to high voltage and power ripple.

Simulation waveforms for different Δf_s settings with a 180W, 36V at MPP PV array are presented in Fig. 2.10. The resonant frequency f_r is 100kHz with trigger frequency f_{MPPT} = 0.4kHz. The power and voltage of the PV array are compared to evaluate the rise time to reach the MPP and the voltage ripple after reaching the MPP.

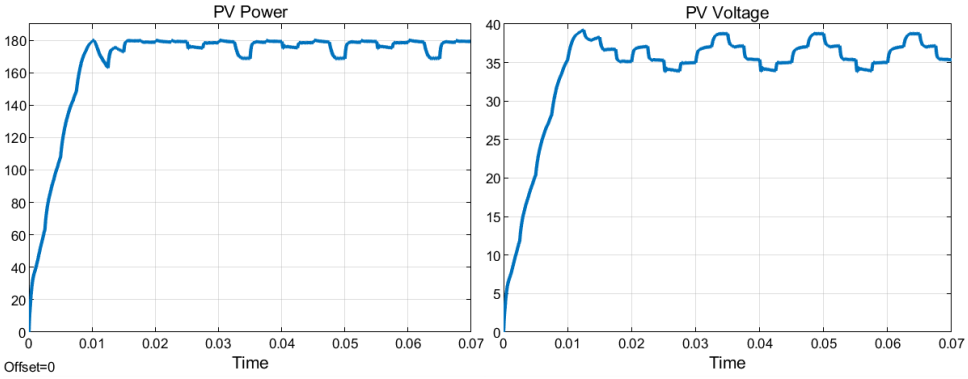
In Fig. 2.10a, a Δf_s value of $0.01f_r$ is simulated, with a rise time of 31ms to 180W and a PV array ripple voltage of 1.01%. In Fig. 2.10b, a Δf_s value of $0.02f_r$ is simulated, with a rise time of 28ms and a ripple voltage of 1.76%. In Fig. 2.10c, a Δf_s value of $0.05f_r$ is simulated, with a rise time of 16ms and a ripple voltage of 6.42%. The simulations demonstrate that a high perturbation step reduces the rise time but increases the steady state's voltage ripple.



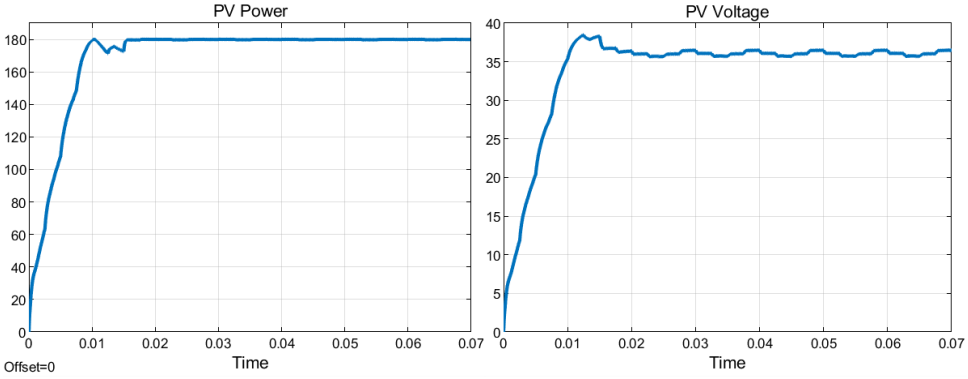
(a) $\Delta f_s = 0.01 f_r$



(b) $\Delta f_s = 0.02 f_r$



(c) $\Delta f_s = 0.05 f_r$



(d) Adaptive Δf_s

Fig. 2.10: Simulation waveforms for different Δf_s.

An adaptive perturbation step method introduced in reference [12] was applied to the FTM-based P&O algorithm, which sets the Δf_s value based on the $\Delta P/\Delta V$ slope. If the $\Delta P/\Delta V$ slope is large, the operating point is still far from the MPP, and the perturbation step Δf_s can be set with a high value to accelerate the tracking process (shown in the rise time in Fig. 2.10c). Conversely, suppose the $\Delta P/\Delta V$ slope is small, indicating that the operating point is close to the MPP. In that case, a minor perturbation step can avoid huge oscillations and result in a minor voltage ripple (as shown in the ripple voltage in Fig. 2.10a). Fig. 2.10d presents the simulation results of the adaptive perturbation step, with the $\Delta P/\Delta V$ threshold set as

$$\begin{cases} \Delta f_s = 0.01 f_r, & if \quad \left|\frac{dP}{dV}\right| \leq 2 \\ \Delta f_s = 0.02 f_r, & if \ 2 < \left|\frac{dP}{dV}\right| \leq 5 \\ \Delta f_s = 0.05 f_r, & if \ 5 < \left|\frac{dP}{dV}\right| \end{cases} \tag{52}$$

The simulation results for various Δf_s values are presented in Table 2.2, displaying the rise time and voltage ripple. The rise time indicates the time required to achieve 99% of 180W. While applying the adaptive perturbation step, the rise time remains the same for $\Delta f_s = 0.05 f_r$. However, in the steady-state feature, the PV voltage ripple is at the same level as $\Delta f_s = 0.01 f_r$, resulting in a quick speed with minimal voltage disturbance.

Table 2.2: Simulation results with different perturbation steps

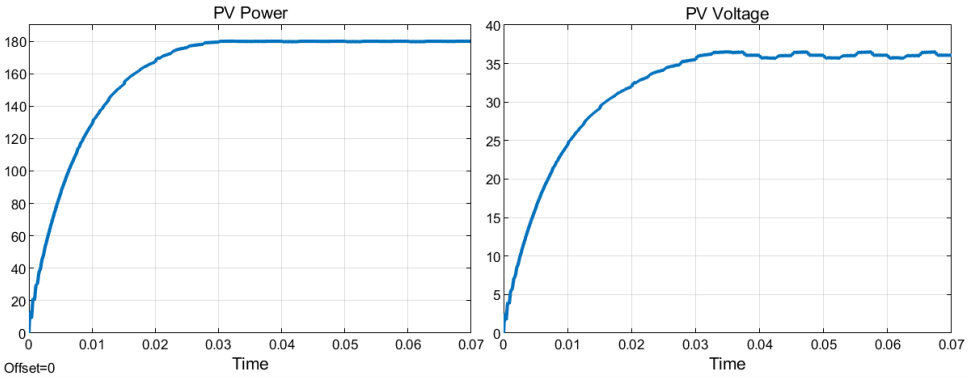
Δf_s	**Rise Time**	**PV voltage ripple**
$0.01 f_r$	31ms	0.88%
$0.02 f_r$	28ms	1.76%
$0.05 f_r$	16ms	6.42%
Adaptive	16ms	0.88%

Likewise, when the trigger frequency f_{MPPT} is set at a high value, the voltage and current transient may fail to reach a stable state after each perturbation, resulting in inaccurate perturbation direction estimates for subsequent iterations. If the trigger frequency is not adjusted appropriately, the static-state oscillations may be more pronounced.

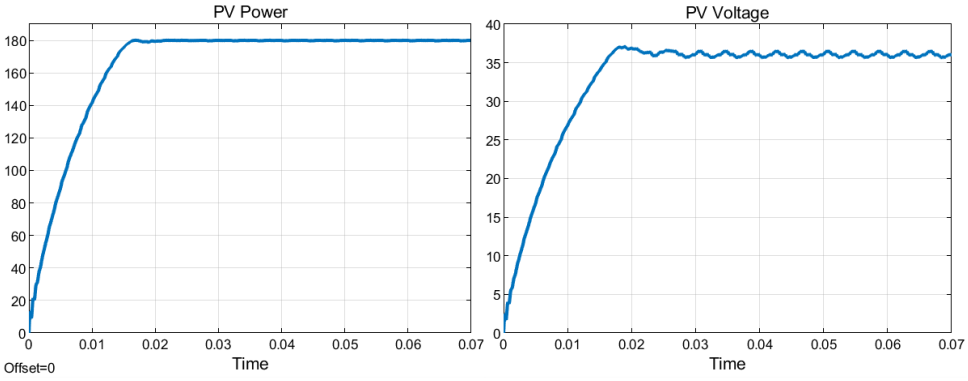
The simulation waveforms for different trigger frequencies are presented in Fig. 2.11, with the same simulation condition in Fig. 2.10 and $\Delta f_s = 0.01 f_r$. In Fig. 2.11a, with a trigger frequency of 0.4kHz, the system's rise time is 30ms, and the ripple voltage is 0.88%. In Fig. 2.11b, with a trigger frequency of 1kHz, the rise time decreases to 21ms, and the ripple voltage slightly increases to 0.96%. Finally, in Fig. 2.11c, with a trigger frequency of 4kHz, the rise time significantly decreases to 10ms, but the ripple voltage increases to 1.14%. These results indicate that a higher trigger frequency can result in faster tracking of the MPP and lower rise times. However, a higher trigger frequency can also increase ripple voltage in the steady state.

In order to overcome the varying environmental conditions, an adaptive trigger frequency method was employed. The simulation results for this method are depicted in Fig. 2.11d, with the $\Delta P/\Delta V$ threshold being set as

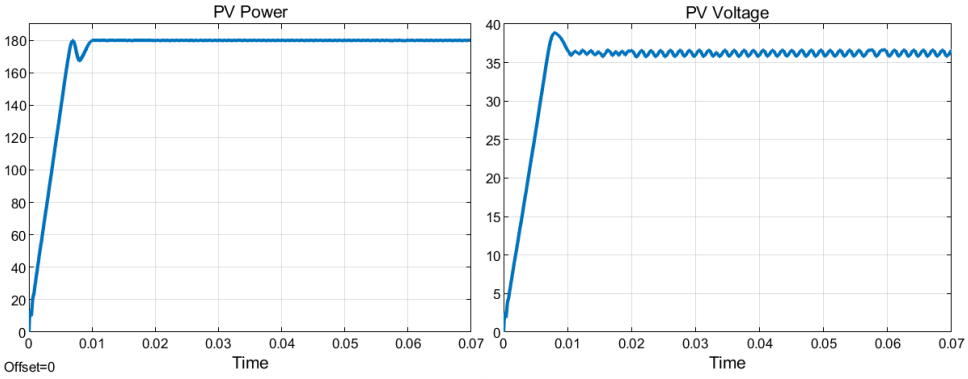
$$\begin{cases} f_{\mathrm{MPPT}} = 0.4kHz, & if \quad \left|\frac{dP}{dV}\right| \leq 2 \\ f_{\mathrm{MPPT}} = 1kHz, & if\ 2 < \left|\frac{dP}{dV}\right| \leq 5 \\ f_{\mathrm{MPPT}} = 4kHz, & if\ 5 < \left|\frac{dP}{dV}\right| \end{cases} \tag{53}$$



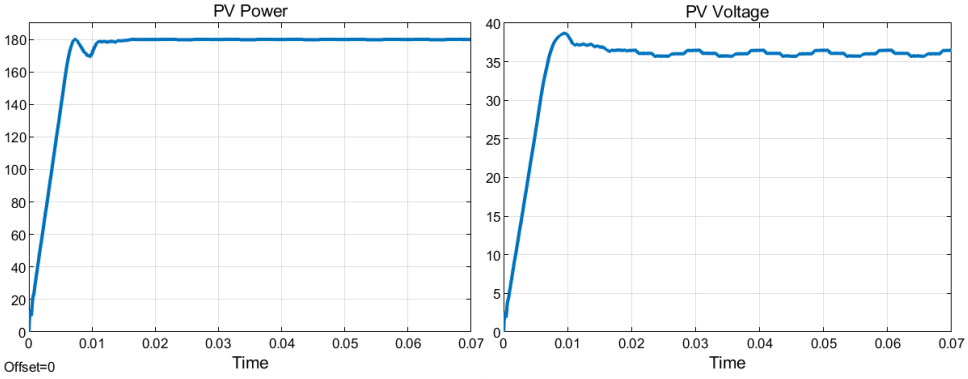
(a) f_{MPPT} = 0.4kHz



(b) f_{MPPT} = 1kHz



(c) f_{MPPT} = 4kHz



(d) Adaptive f_{MPPT}

Fig. 2.11: Simulation waveforms for different f_{MPPT}.

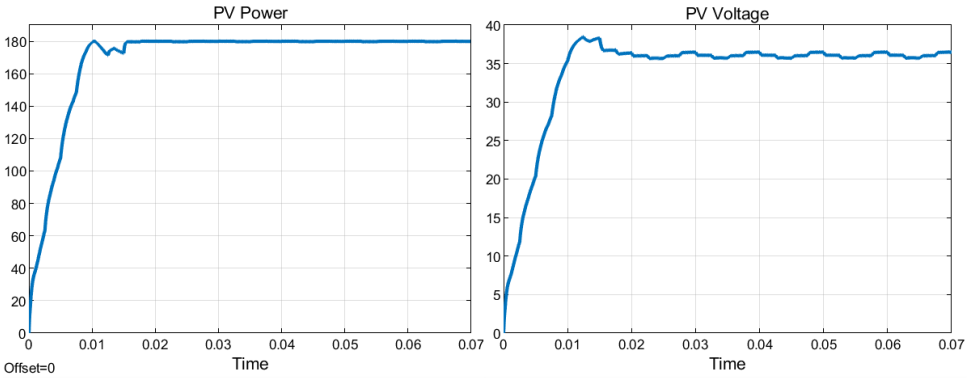
The simulation results for different trigger frequencies are presented in Table 2.3, which includes the rise time and voltage ripple. With the adaptive trigger frequency method, the rise time is equivalent to the trigger frequency of 4kHz, while the voltage ripple is at the same level as the trigger frequency of 0.4kHz. Therefore, the adaptive trigger frequency approach effectively achieves rapid tracking without causing significant voltage frustration.

Table 2.3: Simulation results with different MPPT trigger frequency

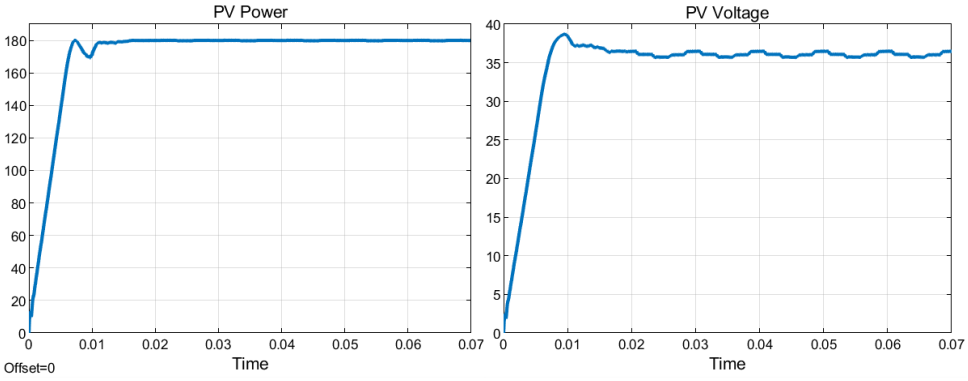
f_{MPPT}	Rise Time	PV voltage ripple
0.4kHz	30ms	0.88%
1kHz	21ms	0.96%
4kHz	11ms	1.14%
Adaptive	11ms	0.88%

An approach to improve tracking speed and reach the MPP faster is proposed by integrating the adaptive perturbation step and adaptive MPPT trigger frequency methods. The simulation waveforms of the three cases are depicted in Fig. 2.12, where the first and second cases use either an adaptive perturbation step or an adaptive MPPT trigger frequency, respectively. In contrast, the last case employs both methods, with the adaptive rule set as

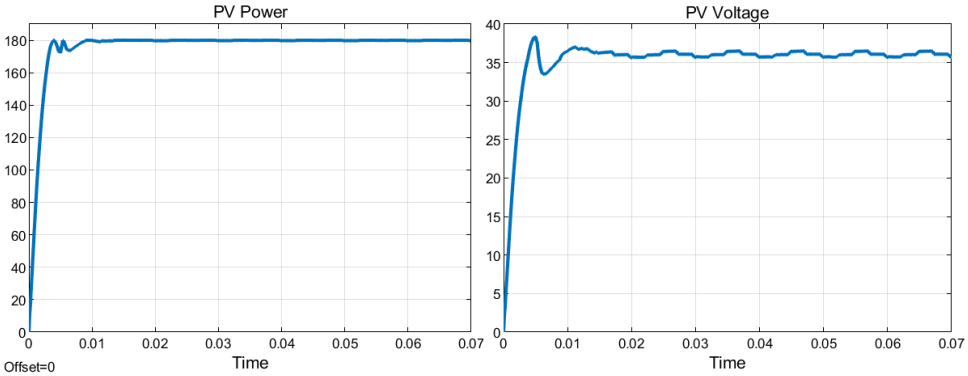
$$\begin{cases} \Delta f_s = 0.01 f_r \; and \; f_{\mathrm{MPPT}} = 0.4kHz, & if \quad \left|\frac{dP}{dV}\right| < 1 \\ \Delta f_s = 0.01 f_r \; and \; f_{\mathrm{MPPT}} = 1kHz, & if \; 1 \le \left|\frac{dP}{dV}\right| < 3 \\ \Delta f_s = 0.02 f_r \; and \; f_{\mathrm{MPPT}} = 1kHz, & if \; 3 \le \left|\frac{dP}{dV}\right| < 5 \\ \Delta f_s = 0.05 f_r \; and \; f_{\mathrm{MPPT}} = 4kHz, & if \; 5 \le \left|\frac{dP}{dV}\right| \end{cases} \tag{54}$$



(a) Adaptive Δf_s with constant f_{MPPT}



(b) Constant Δf_s with adaptive f_{MPPT}



(c) Adaptive Δf_s with adaptive f_{MPPT}

Fig. 2.12: Simulation waveforms for different adaptive methods.

As presented in Table 2.4, the combined method significantly reduces rise time compared to the other two methods while maintaining a low voltage ripple level. Therefore, the benefits of utilizing the adaptive perturbation step and adaptive MPPT trigger frequency are evident. The flowchart of the FTM-based P&O algorithm with adaptive perturbation step and adaptive MPPT trigger frequency is shown in Fig. 2. 13.

Table 2.4: Simulation results of different combinations of adaptive methods

Method	Rise Time	PV voltage ripple
Adaptive Δf_s	16ms	0.88%
Adaptive f_{MPPT}	11ms	0.88%
Adaptive Δf_s + Adaptive f_{MPPT}	8ms	0.88%

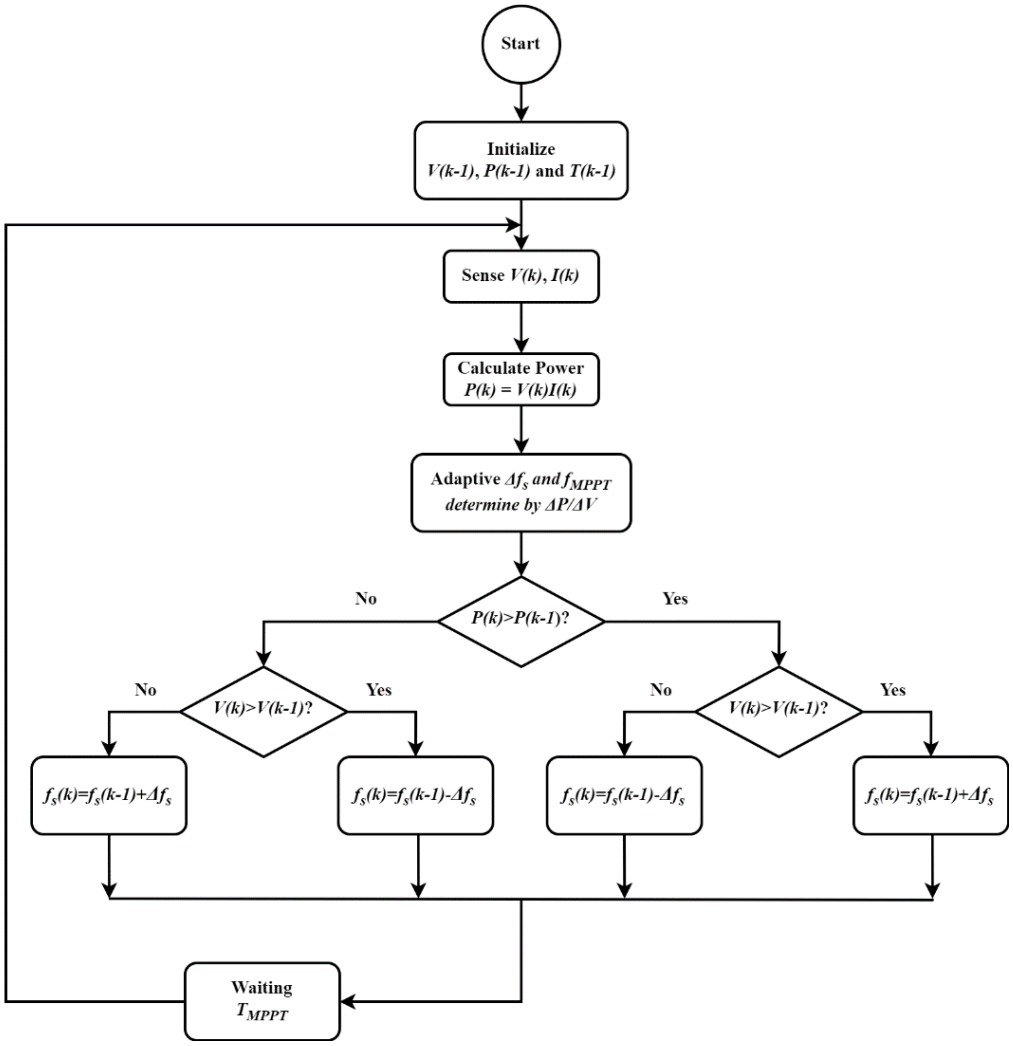


Fig. 2.13: The flowchart of the FTM-based P&O algorithm with adaptive strategy.

CHAPTER 3: Experimental Results

Prototype Details

PV Array:

To verify the proposed application, a 180W PV array was utilized. The specifications of this PV array are presented in Table 3.1, and a photo of the PV panel is shown in Fig. 3.1.

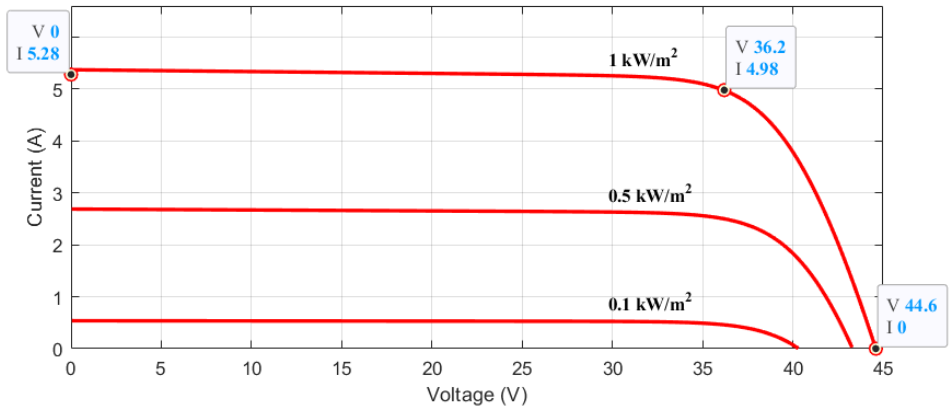
Table 3.1: PV array specifications in the experiment

Parameter	Symbol	Value
Maximum power	P_{mp}	180 W
Voltage at maximum power	V_{mp}	36.2 V
Current at maximum power	I_{mp}	4.98 A
Open circuit voltage	V_{oc}	44.6 V
Short circuit current	I_{sc}	5.28 A

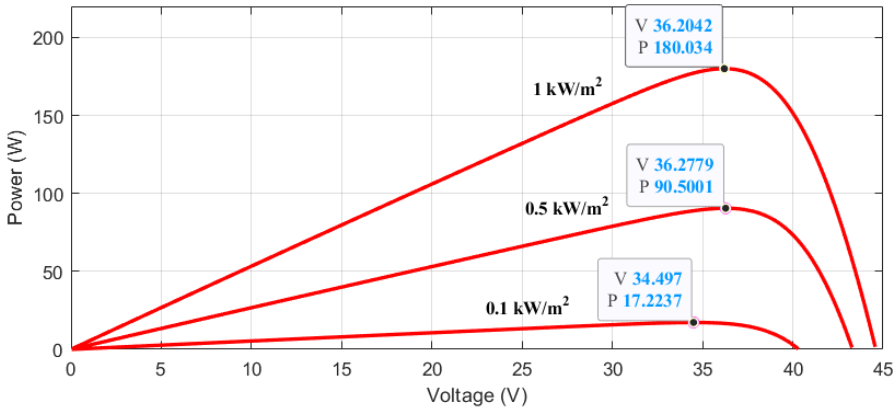
Fig. 3.1: A photograph of the PV panel used in the experiments.

Based on the given specifications, obtaining the characteristic curves of the PV array is possible. As depicted in Fig 3.2a, the PV panel's I-V curves are shown at 25°C and irradiance levels of 1000, 500, and 100 W/m^2. The I-V curve displays the maximum

input voltage, V_{oc}, which can be applied to the half-bridge SRC. Conversely, the short-circuit current, I_{sc}, is the highest current that the half-bridge SRC can utilize. In Fig 3.2b, the P-V curves of the PV panel indicate that the output power decreases with lower irradiance levels. However, the PV voltage at the MPP remains within a small range at each irradiance level.



(a)



(b)

Fig. 3.2: (a) The I-V curves of the PV array in the experiments. (b) The P-V curves of the PV array in the experiments.

Half-bridge SRC:

A half-bridge SRC is connected to the PV array to implement the MPPT system based on the analysis and design procedure in Chapter 2. In the experiment, the input voltage range is defined by the PV array, in which the maximum input voltage is 44.6V,

while the maximum input current is 5.28A. The SRC's resonant frequency is 100kHz, which defined the turn-on time of the transistor S_1 to be 5μs, according to equation (2). The resonant inductor is implemented as 2.5μL with 1μF resonant capacitor to meet the resonant frequency based on equation (1). The switching frequency ranges from 100kHz to 200kHz to fulfill full-range regulation, resulting in a normalized frequency range from 1 to 2. The output voltage of the half-bridge SRC prototype spans a range from 12V to 36V. The system's efficiency determines the output power, which is below 180W. Various resistors are employed as loads to assess the prototype's performance under different conditions. Additionally, a 24V battery load is implemented to simulate the scenario where the output load is capacitive. This diverse range of load configurations allows for comprehensive testing and evaluation of the prototype's functionality.

The value of each parameter for the prototype is listed in Table 3.2. The components selected for the prototype, according to Fig. 2.2, are listed in Table 3.3. The photograph of the half-bridge SRC is shown in Fig. 3.3.

Table 3.2: Defined parameters for half-bridge SRC prototype

Parameter	**Symbol**	**Value**
Resonant frequency	f_r	100 kHz
Switching frequency of S_1 and S_2	f_s	100~200 kHz
Normalized frequency	F	1~2
Turn-on time of S_1	t_{on}	5 μs
PV array's voltage	V_{PV}	0~44.6 V
PV array's current	I_{PV}	0~5.28 A
Output voltage	V_o	12~36 V
Output power	P_o	<180 W

Table 3.3: Selected components for prototype

Component	Value	Part No.	Voltage Rating	Current Rating
L_r	2.5 µH	-	-	-
C_r	1 µF	F17725102030	630Vdc	-
$S_{1\text{-}2}$	-	IRF200P223	200V	100A
$D_{1\text{-}2}$	-	FERD15S50SB-TR	50V	15A
C_o	82 µF	-	-	-

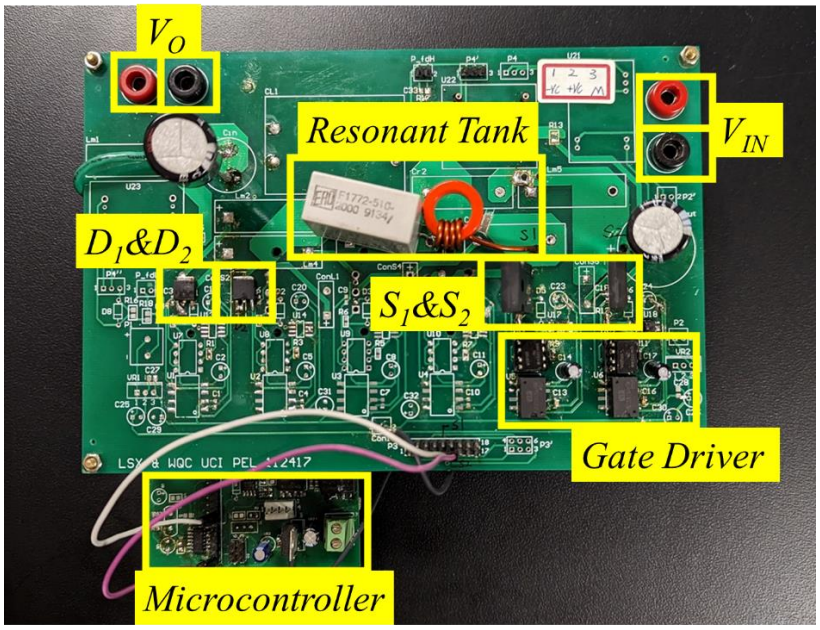


Fig. 3.3: A photograph of the half-bridge SRC prototype.

MPPT Controller:

The MPPT algorithm is implemented using a microcontroller (ATtiny24a). This 8-bit microcontroller is equipped with PWM and ADC functions that operate on low power, making it a suitable choice for MPPT applications. The microcontroller obtains analog voltage and current signals from the PV array, which it then converts into a digital signal through its ADC function. The microcontroller utilizes a voltage divider

for voltage sensing, while a current sensor consisting of an operational amplifier and a current sense resistor is employed for current sensing.

The MPPT is implemented based on the algorithm described in Fig 2.13, with the adaptive frequency step and adaptive MPPT trigger frequency depicted in equation (54) and summarized in Table 3.4.

Table 3.4: Defined parameters for the MPPT algorithm

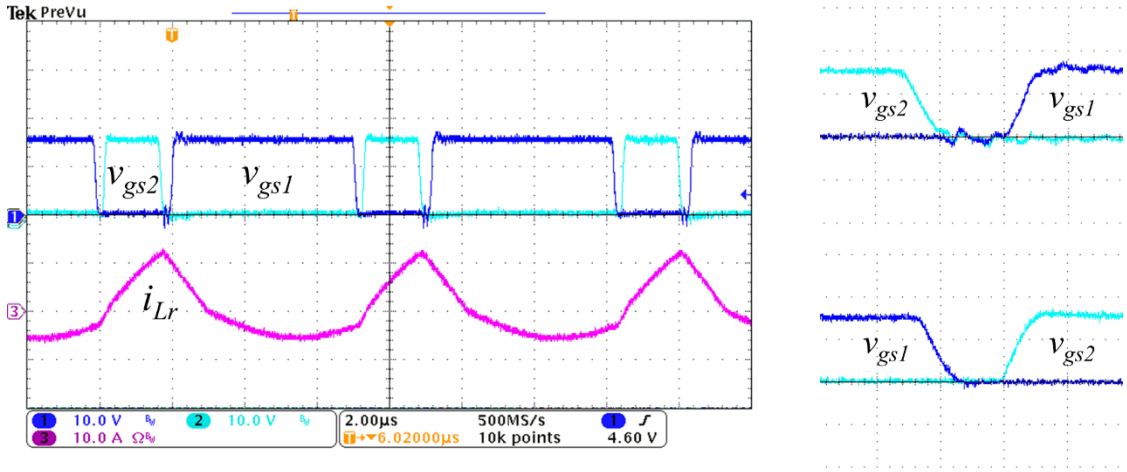
Parameter	**Symbol**	**Value**
MPPT trigger frequency	f_{MPPT}	400, 1000, 4000 Hz
Perturbation step size	Δf_s	1%, 2%, 5% of f_r

Experimental Waveforms

This section presents the experimental waveforms of the half-bridge SRC prototype, including illustrations of the current and voltage oscillations in the resonant tank and the switching actions of the transistors and diodes during the switching cycle.

Switching signals investigation:

Fig. 3.4a displays the switching signals of transistors S_1 and S_2, with a duty ratio of S_1 = 70% and an output power of 120W. The waveforms demonstrate complementary switching signals, separated by a short dead time. Additionally, Fig. 3.4b presents zoomed-in waveforms of the switching signals, where the dead time is approximately 300ns. During this period, the antiparallel diode in the MOSFET conducts, allowing the parasitic capacitance in the MOSFET to reach zero voltage, thus enabling the zero-voltage turn-on operation.



(a) (b)

Fig. 3.4: (a) Complemental switching signals of the transistors. (b) Zoom-in waveforms of switching signals. v_{gs1} and v_{gs2}: 10V/div, i_{Lr}: 10A/div.

Voltage regulation ability:

Fig. 3.5 displays the output voltage and resonant inductor current for various duty ratios while maintaining a constant input voltage of 36V. The output terminal is connected to a 7.3Ω resistor as output load (Q = 0.2176). The input voltage of 36V is chosen to simulate the practical scenario with the PV array used in the experiment. Fig. 3.5a depicts the switching waveform for a duty ratio of S_1 = 50%, resulting in an output voltage of 35.0V and a voltage gain of 0.97. The resonant inductor current exhibits an approximately sinusoidal waveform due to the matching of the switching frequency f_s and the resonant frequency f_r.

Fig. 3.5b, Fig. 3.5c, and Fig. 3.5d show the switching waveforms with duty ratios of S_1 = 60%, S_1 = 70%, and S_1 = 80%, respectively. The corresponding output voltages are 29.9V, 22.1V, and 14.1V, which indicate voltage gains of 0.83, 0.61, and 0.39, respectively.

These results demonstrate the voltage regulation capability of the half-bridge SRC prototype across different duty ratios, which indicates that the half-bridge SRC can achieve full-range voltage regulation across a limited range of frequencies, demonstrating its potential as an effective solution for MPPT applications.

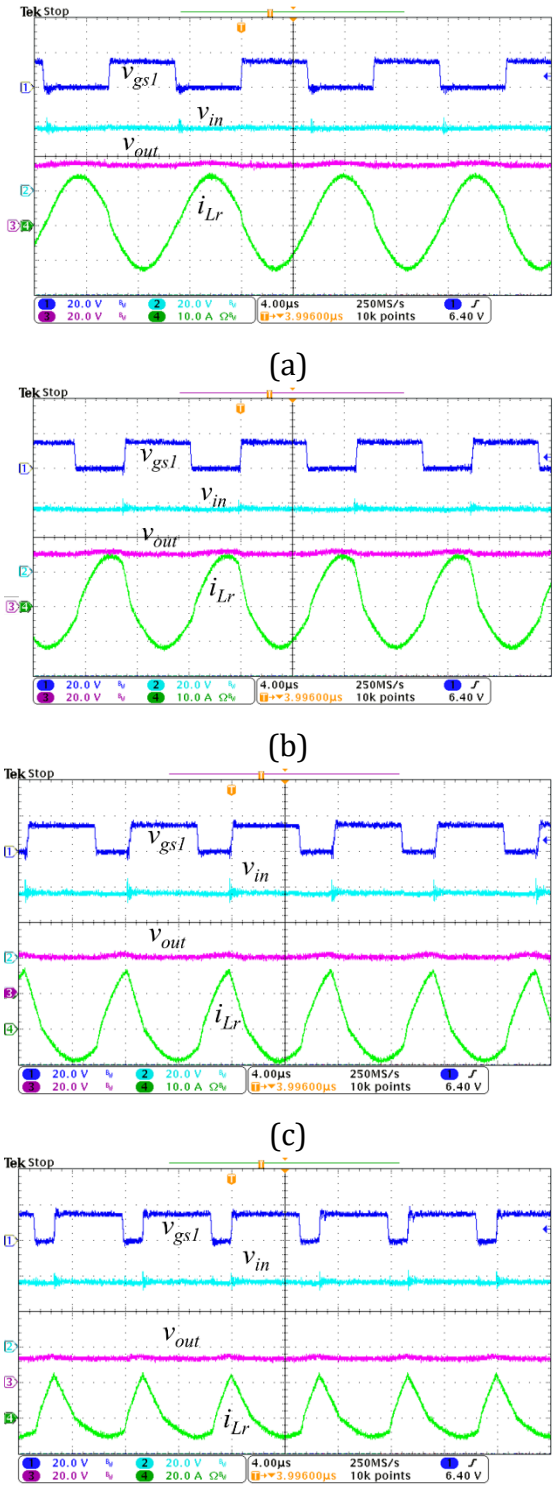
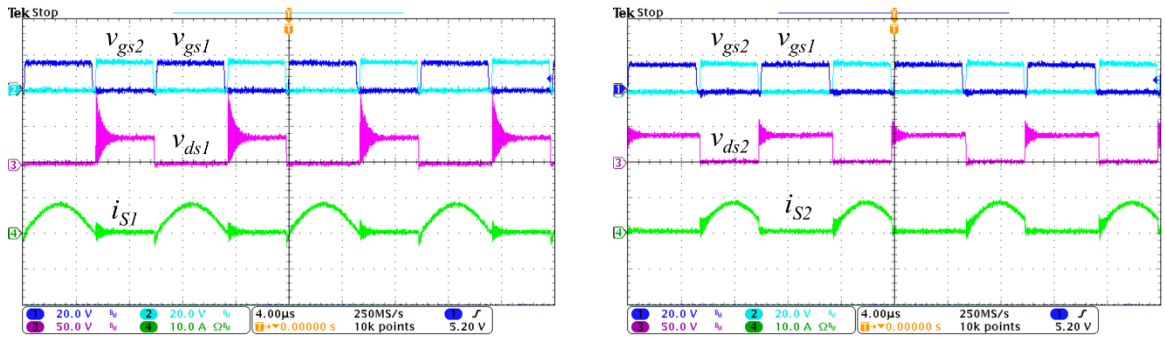


Fig. 3.5: Switching waveforms and output voltage with (a) Duty ratio of S_1 = 50%, (b) Duty ratio of S_1 = 60%, (c) Duty ratio of S_1 = 70%, (d) Duty ratio of S_1 = 80%. v_{gs1}: 20V/div, v_{in} and v_{out}: 20V/div, i_{Lr}: 10A/div or 20A/div.

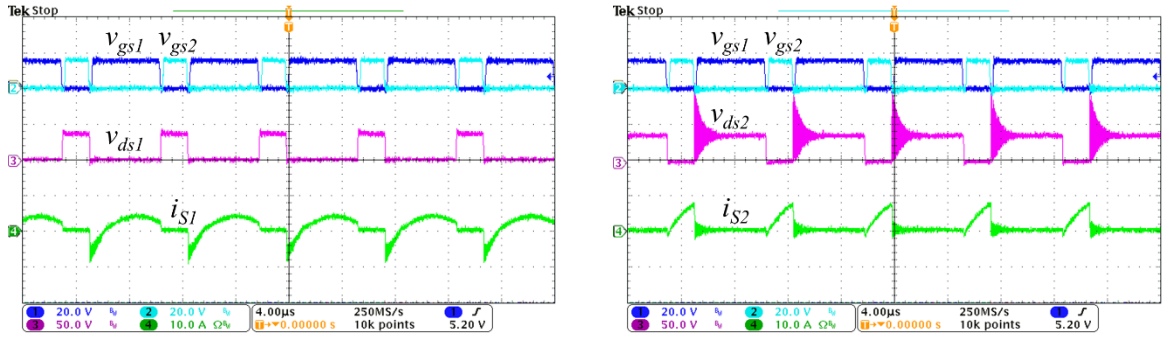
Zero voltage turn-on:

In Fig. 3.6, the zero voltage turn-on of transistors S_1 and S_2 is demonstrated with a duty ratio of S_1 = 50%. Fig. 3.6a displays the drain-to-source voltage and current of transistor S_1, while Fig. 3.6b shows the drain-to-source voltage and current of transistor S_2. The results show that the MOSFETs conduct complementary based on the switching signals.



(a) (b)

Fig. 3.6: Switching waveforms of transistors S_1 and S_2 at a duty ratio of S_1 = 50%. v_{gs1} and v_{gs2}: 20V/div, v_{ds1} and v_{ds2}: 50V/div, i_{ds1} and i_{ds2}: 10A/div.



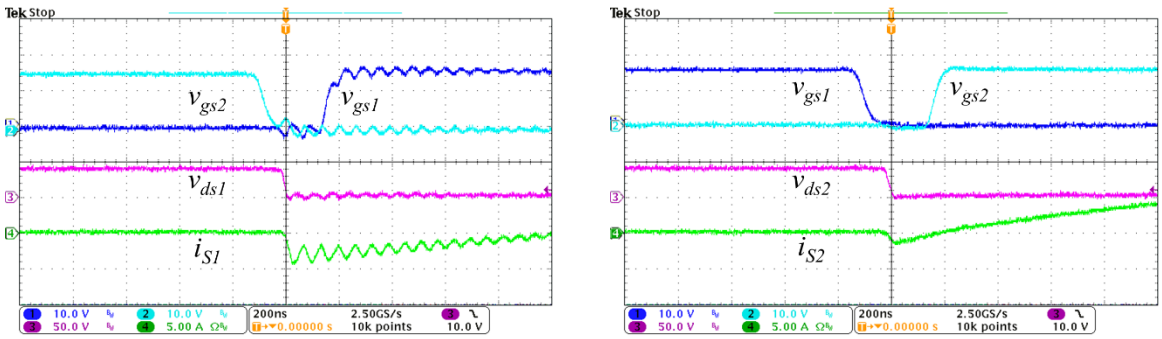
(a) (b)

Fig. 3.7: Switching waveforms of transistors S_1 and S_2 at a duty ratio of S_1 = 70%. v_{gs1} and v_{gs2}: 20V/div, v_{ds1} and v_{ds2}: 50V/div, i_{ds1} and i_{ds2}: 10A/div.

Fig. 3.7 extends this analysis by showing the ZVS of transistors S_1 and S_2 with a duty ratio of S_1 = 70%. Fig. 3.7a and Fig. 3.7b show the drain-to-source voltage across

the MOSFETs and their conducting currents. Once again, the results indicate that the transistors conduct complementary corresponding to the switching signals.

To further investigate the transistors' ZVS operations, Fig. 3.8 provides a zoomed-in view of the switching waveforms for transistors S_1 and S_2. Fig. 3.8a shows the drain-to-source voltage across transistor S_1 drops before the gate-to-source signal switches on. The waveform shows that the voltage across the transistor, v_{ds1}, reaches zero before the transistor switches on. Likewise, Fig. 3.8b shows the drain-to-source voltage across transistor S_2 dropping to zero before the gate-to-source signal switches on.



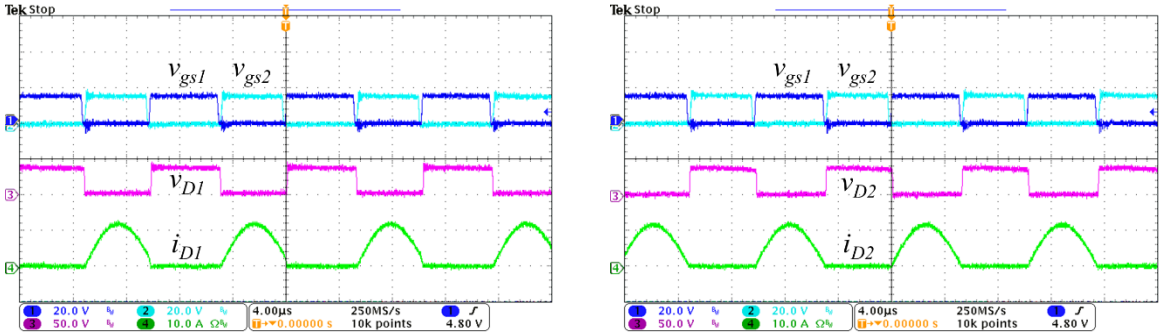
(a) (b)

Fig. 3.8: Zoom-in switching waveforms of transistors S_1 and S_2. v_{gs1} and v_{gs2}: 20V/div, v_{ds1} and v_{ds2}: 50V/div, i_{ds1} and i_{ds2}: 10A/div.

The results from Fig. 3.6 to Fig. 3.8 suggest that the half-bridge SRC's transistors are capable of ZVS operation across the limited range of switching frequencies. The conventional converter sustains higher switching losses as frequency increases, which this half-bridge SRC overcomes, making it well-suited for high-frequency, high-efficiency applications.

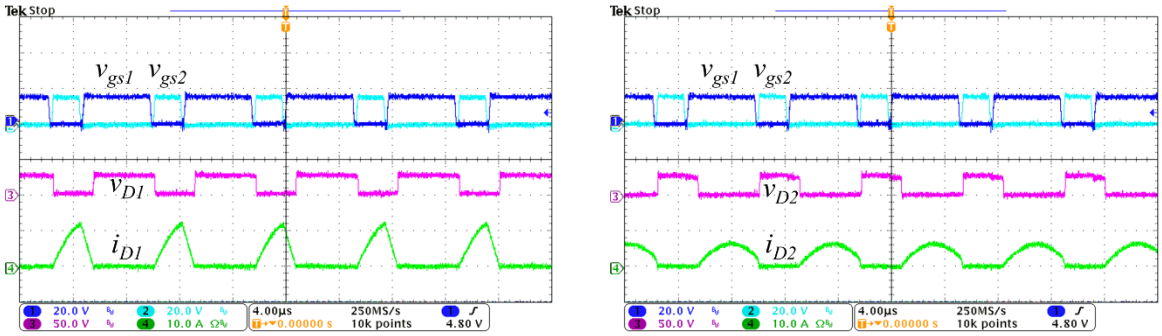
Zero current turn-off:

Fig. 3.9 and Fig. 3.10 depict the zero current turn-offs of power diodes D_1 and D_2, respectively, with different duty ratios. Fig. 3.9a and Fig. 3.9b show the voltage across each diode and their corresponding conducting current at a duty ratio of S_1 = 50%. These results demonstrate that the power diodes conduct alternately according to the switching signals. Similarly, Fig. 3.10a and Fig. 3.10b show the voltage across the power diodes and their respective conducting currents at a duty ratio of S_1 = 70%, again showing alternating conduction.



(a) (b)

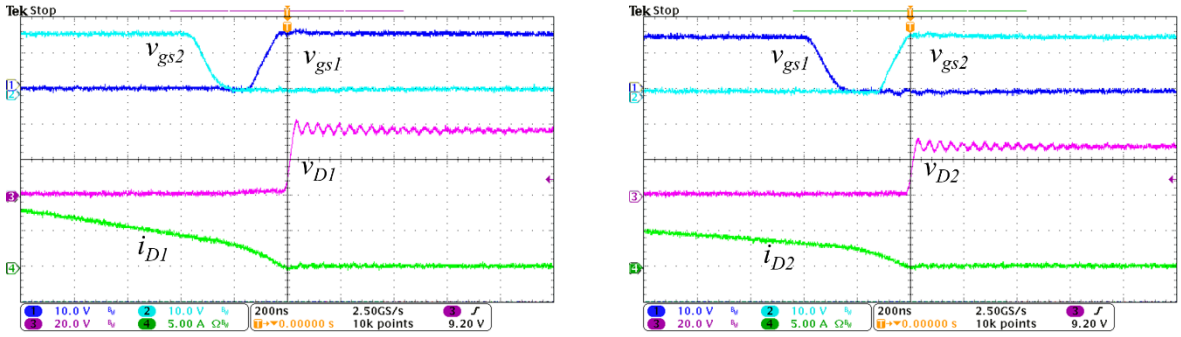
Fig. 3.9: Switching waveforms of power diode D_1 and D_2 at a duty ratio of S_1 = 50%. v_{gs1} and v_{gs2}: 20V/div, v_{D1} and v_{D2}: 50V/div, i_{D1} and i_{D2}: 10A/div.



(a) (b)

Fig. 3.10: Switching waveforms of power diode D_1 and D_2 at a duty ratio of S_1 = 70%. v_{gs1} and v_{gs2}: 20V/div, v_{D1} and v_{D2}: 50V/div, i_{D1} and i_{D2}: 10A/div.

To investigate the ZCS operations more closely, Fig. 3.11 provides zoom-in switching waveforms for the power diodes D_1 and D_2. In Fig. 3.11a, the power diode D_1 turns off after transistor S_1 turns on, and the waveform clearly shows that the power diode current i_{D1} reaches zero before the diode turns off. Similarly, in Fig. 3.11b, the power diode D_2 turns off after transistor S_2 turns on. The waveform again indicates that the power diode current i_{D2} reaches zero before the voltage across the diode rises.



(a) (b)

Fig. 3.11: Zoom-in switching waveforms of power diode D_1 and D_2. v_{gs1} and v_{gs2}: 10V/div, v_{D1} and v_{D2}: 20V/div, i_{D1} and i_{D2}: 5A/div.

From Fig. 3.9 to Fig. 3.11, it is clear that the half-bridge SRC's power diodes can operate in ZCS within the entire frequency range while the duty ratio changes. These results demonstrate the SRC's ability to achieve high-frequency operation with low switching losses, enhancing its overall efficiency.

Voltage Gain and Efficiency

Fig. 3.12 illustrates voltage gain curves for the prototype with different Q values, along with the theoretical voltage gain for comparison. The selection of resistor load values is based on the chosen PV array for the experiment. By examining the P-V curves in Fig. 3.2b, it becomes evident that different irradiation levels lead to varying maximum power points, corresponding to different equivalent resistance values at each irradiation level. These equivalent resistance values are determined by considering each irradiation level's power level and operating voltage. The resulting equivalent resistances at 100W/m^2, 500W/m^2, and 1000W/ m^2 are calculated as 69.1Ω, 14.5Ω, and 7.3Ω, respectively.

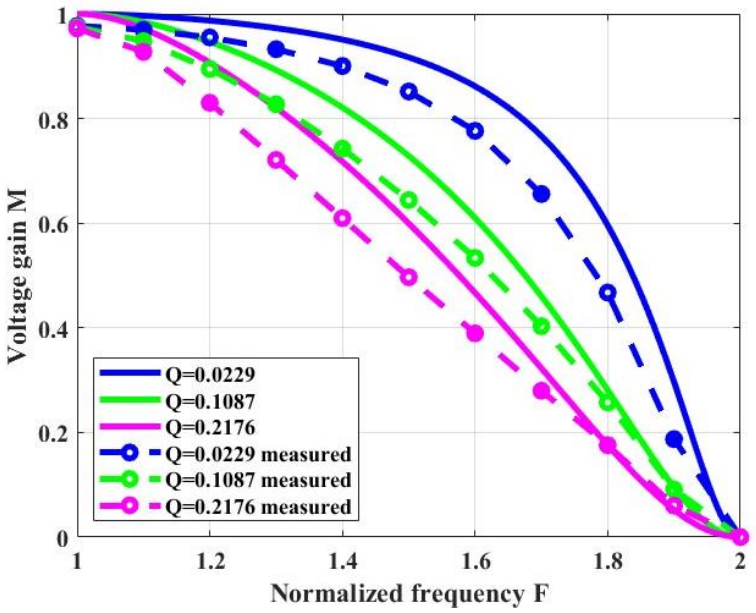


Fig. 3.12: Experimental and theoretical voltage gain curves.

Upon observing Fig. 3.12, it can be noticed that the voltage gain curves exhibit a slight deviation from the theoretical voltage gain curves. This deviation can be attributed to the forward voltage drop of the power diode in the prototype, which has

been optimized by selecting power diodes with an approximate forward voltage drop of 0.4V. Additionally, parasitic inductance within the circuit might influence the offset, resulting in a higher impedance value and quality factor. Despite these offsets, the experimental voltage gain curves obtained from the prototype demonstrate its ability to achieve full-range voltage regulation, and the results are in close agreement with the theoretical calculations.

Fig. 3.13 provides an overview of the efficiency performance of the half-bridge SRC prototype. The measurements are performed under the specific conditions of an input voltage of 36V, precisely matching the nominal voltage of the PV array. Three different load values are employed to cover the range of irradiation levels in a practical scenario, allowing for a thorough assessment of the prototype's efficiency under varying conditions.

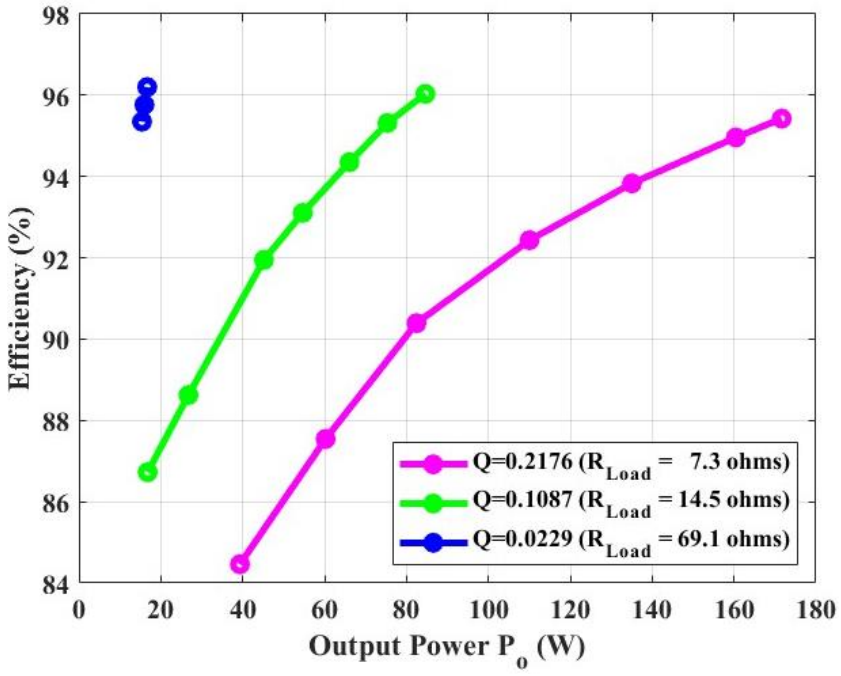


Fig. 3.13: Efficiency curves of the half-bridge SRC.

Each curve on the graph consists of multiple data points, each representing a measurement taken at incremental intervals of 0.1 of normalized frequency (as shown in Fig. 3.12) within each curve. The highest efficiency point on each curve corresponds to a normalized frequency value of F=1.

In the case of R_{Load} = 7.3Ω, the best efficiency is 95.4% at F=1, with an input power of 180W. This load value represents the high irradiation level, with the prototype delivering the highest power. Similarly, with R_{Load} = 14.5Ω, the prototype attains a peak efficiency of 96% at F=1, accompanied by an input power of 90.5W. Finally, the highest efficiency of 96.3% at F=1 is achieved when utilizing R_{Load} = 69.1Ω, resulting in an input power of 17.2W. This load value demonstrates the prototype's capability to maintain high efficiency when operating with lower power levels. Overall, the results in Fig. 3.13 illustrate the impressive efficiency performance of the half-bridge SRC prototype across various load values and normalized frequencies.

MPPT Results

In the MPPT experiment, the primary objective is to evaluate the performance of the half-bridge-SRC-based MPPT system. An important step is to determine the actual maximum power of the PV array within specific environmental conditions. This is achieved by directly connecting a variable resistor to the PV array, as illustrated in Fig. 3.14. By adjusting the value of the variable resistor, it becomes possible to record the PV array's I-V and P-V curves.

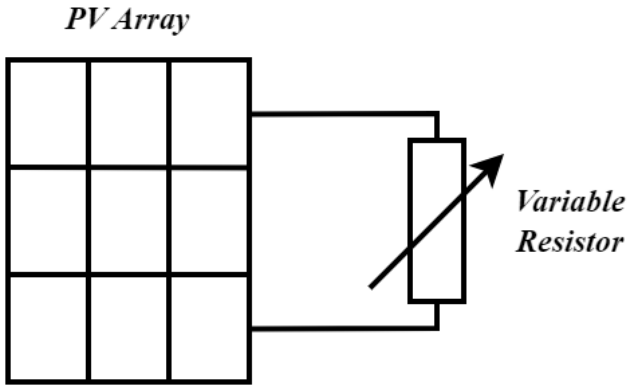
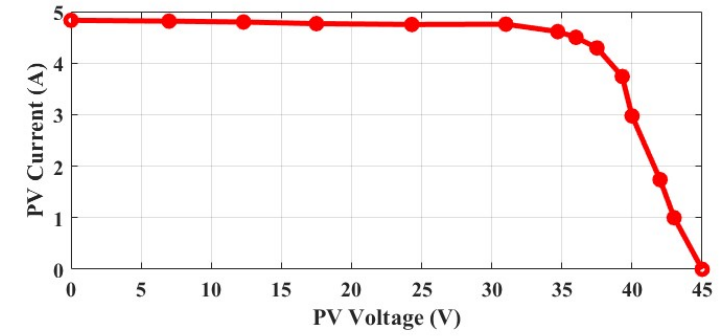
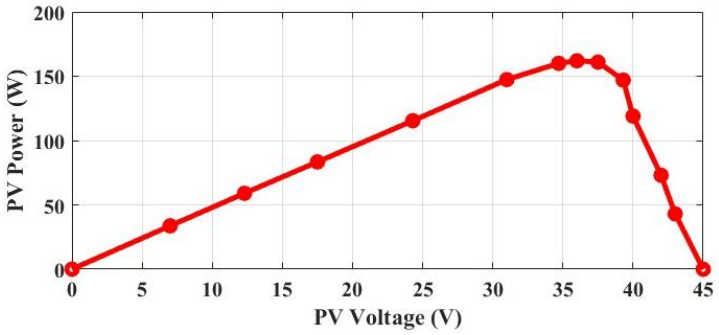


Fig. 3.14: Method to measure I-V and P-V curves.

Fig. 3.15a showcases the I-V curve, representing the relationship between current and voltage across the PV array. On the other hand, Fig. 3.15b presents the P-V curve, which illustrates the variation in power output at different voltage levels. During the experiment, the maximum power is 162W, with a corresponding PV voltage of 36V and PV current of 4.5A at the MPP. The characteristics of the PV array under experimental conditions are written in Table 3.5.



(a)



(b)

Fig. 3.15: (a) I-V curve of the PV array under experimental conditions. (b) P-V curve of the PV array under experimental conditions.

Table 3.5: PV array characteristics under experimental conditions

Parameter	**Symbol**	**Value**
Maximum power	P_{mp}	162 W
Voltage at maximum power	V_{mp}	36 V
Current at maximum power	I_{mp}	4.5 A
Open circuit voltage	V_{oc}	44.6 V
Short circuit current	I_{sc}	4.83 A

The efficiency of the half-bridge-SRC-based MPPT system is presented in Fig. 3.16. This efficiency evaluation focuses on different output voltage levels during the execution of the MPPT algorithm, where the system aims to reach the MPP. The experiment is conducted under the specific conditions described in Table 3.5.

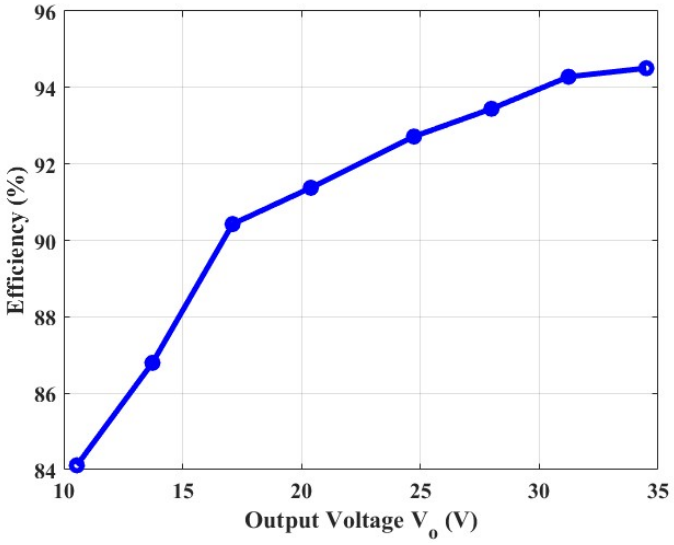


Fig. 3.16: Efficiency curves with different output voltages.

To assess the efficiency, the output voltage is adjusted by employing various load resistors while keeping the maximum power fixed at 162W and the PV voltage at 36V. Upon analysis, it is observed that the highest efficiency of 94.5% is achieved when the output voltage is adjusted at 34.5V, which indicates that the system operates with optimal efficiency when the output voltage is close to the PV voltage. Conversely, the lowest efficiency of 84.3% is recorded when the output voltage is 10.55V. These results emphasize the system's ability to sustain high efficiency, especially when the output voltage is near the PV voltage.

To thoroughly assess the performance of the half-bridge SRC-based MPPT system, an experiment from 9 am to 4 pm is performed. This extended duration allows for evaluating the system's capabilities over an entire day. In order to simulate practical usage scenarios, a 24V battery is connected as a load, reflecting the system's application in charging batteries.

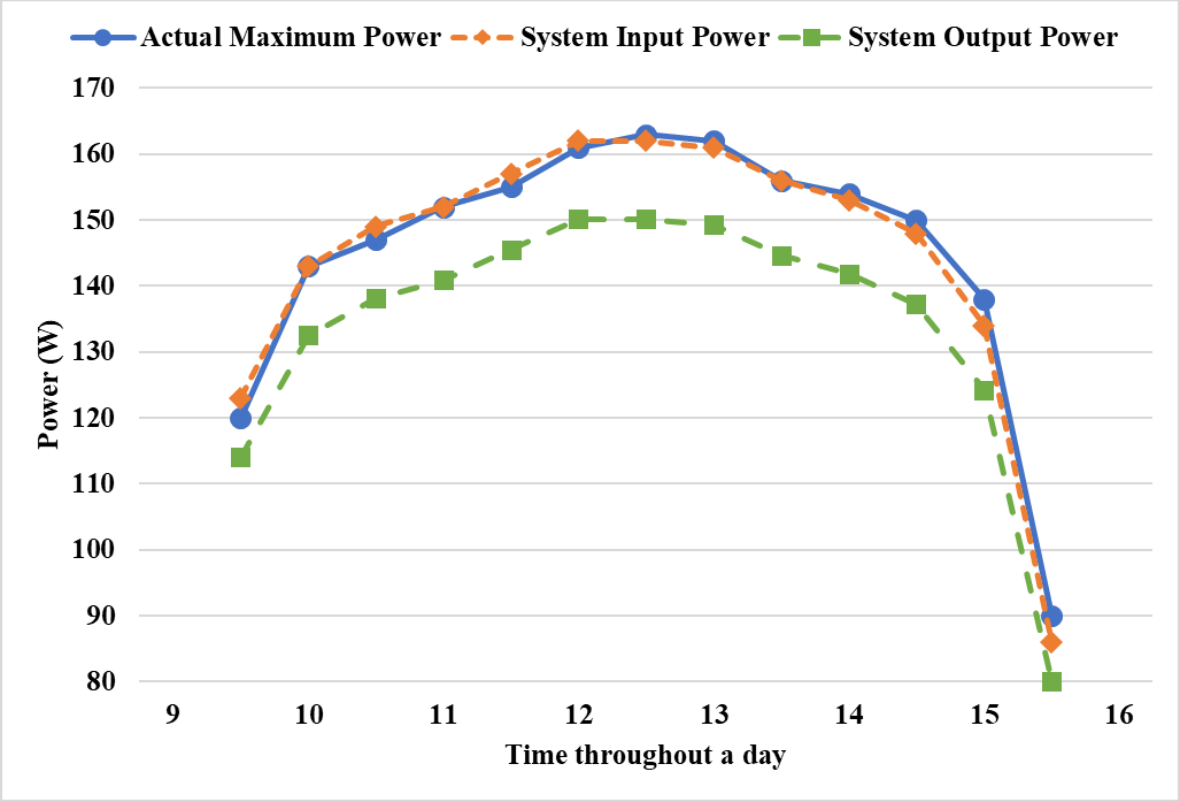


Fig. 3.17: MPPT experiment results throughout a day.

The actual maximum powers are measured using the method illustrated in Fig. 3.14 to determine the system's effectiveness in achieving the maximum power point. The system's input power corresponds to the measured power from the PV array when the MPP is reached, which is a validation check to verify whether the MPPT algorithm successfully identifies and maintains the MPP. On the other hand, the system's output power represents the measured power from the load when the MPP is attained. The output power is influenced by the system's input power and the efficiency of the half-bridge SRC.

From the observations presented in Fig. 3.17, it is evident that the system's input powers closely align with the actual maximum powers, which indicates the successful

implementation of an accurate MPPT algorithm. The greatest discrepancy between the actual maximum power and the system's input power is 4W. This difference occurs after 3 pm, where rapid changes in irradiation levels lead to more significant variability. It is worth noting that, on average, the difference between the actual maximum power and the system's input power remains within ±2W. Furthermore, the efficiency achieved during the experiment is approximately 92.6%. This value represents the proportion of real power utilized for battery charging, demonstrating the system's ability to convert power to energy storage.

CHAPTER 4: Topology Comparison

This chapter explores a comparative analysis between the half-bridge SRC and a conventional buck converter. A buck converter is built without soft-switching techniques, and its switching waveforms are examined. These waveforms are then compared with the switching waveforms of the half-bridge SRC to discuss the distinctions. The voltage gain curve of the buck converter is presented, allowing for a direct comparison with the half-bridge SRC prototype. Additionally, the efficiency of the buck converter is evaluated and presented alongside the efficiency of the half-bridge SRC prototype.

Buck Converter Details

Fig. 4.1 presents a schematic diagram of a buck converter used in this comparison. A continuous conduction mode (CCM) buck converter is designed to be compatible with the PV array described in Table 3.1.

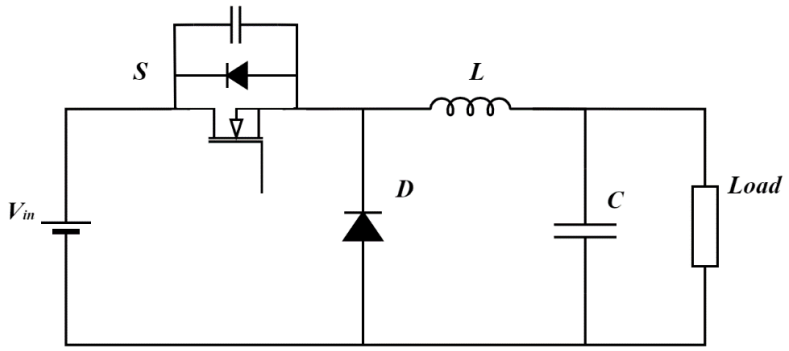


Fig. 4.1: Schematic diagram of a buck converter.

To ensure a fair comparison with the half-bridge SRC, the buck converter utilizes the same components for the transistor and diode used in the half-bridge SRC. The inductor L is designed to operate in CCM for all operating conditions in the experiments.

Under the worst-case condition, with a switching frequency of 100kHz and a duty cycle of 35%, the ripple current is 10% of the output current. The output capacitor C is designed to maintain a relatively constant output voltage, with a maximum voltage ripple of 1% under worst-case conditions.

Two switching frequencies, 100kHz and 200kHz, have been chosen for efficiency compared with the half-bridge SRC. In order to achieve a comprehensive assessment, a range of output voltages, from 11V to 32V, is selected. These output voltage values correspond to duty cycle ranges from 35% to 90%. By investigating these different operating points, a thorough evaluation of the buck converter's performance can be compared with the half-bridge SRC's performance. The operating conditions for the buck converter are shown in Table 4.1. Details of the components used in the buck converter can be found in Table 4.2.

Table 4.1: Operating conditions for the buck converter

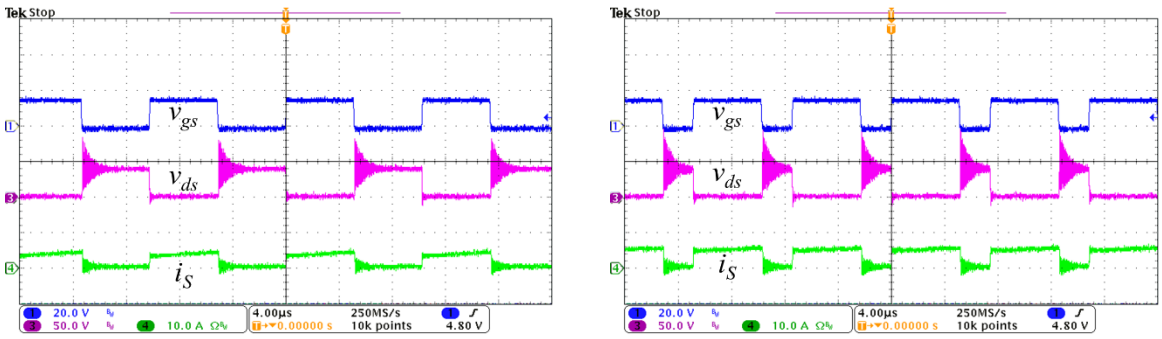
Parameter	**Value**
Switching frequency	100~200 kHz
Duty cycle	35%~90%
Output voltage	11~32 V
Input voltage	0~44.6 V
Output power	<180 W

Table 4.2: Selected components for the buck converter

Component	**Value**	**Part No.**	**Voltage Rating**	**Current Rating**
S	-	IRF200P223	200V	100A
D	-	FERD15S50SB-TR	50V	15A
C	82 μF	-	-	-
L	200 μH	-	-	-

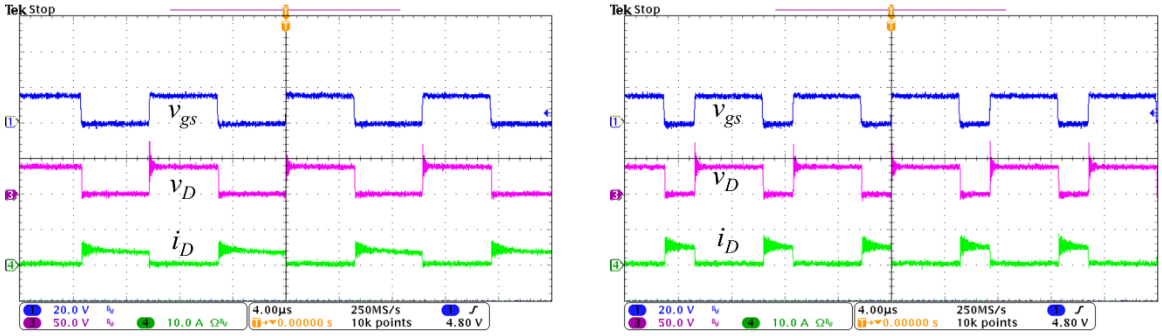
Experimental Waveforms

This section presents the experimental waveforms of the buck converter. Fig. 4.2 illustrates the gate signal v_{gs}, drain-to-source voltage v_{ds}, and drain current i_s of transistor S for two different duty ratios: 50% in Fig. 4.2a and 70% in Fig. 4.2b. To effectively compare the buck converter and the half-bridge SRC, the switching frequencies are adjusted to be the same in both topologies. The buck converter operates at a switching frequency of 100kHz for a duty ratio of 50% and 140kHz for a duty ratio of 70%.



(a) (b)

Fig. 4.2: (a) Switching waveforms of transistor S at a duty ratio of S = 50%. (b) Switching waveforms for transistor S at a duty ratio of S = 70%. v_{gs}: 20V/div, v_{ds}: 50V/div, i_S: 10A/div.

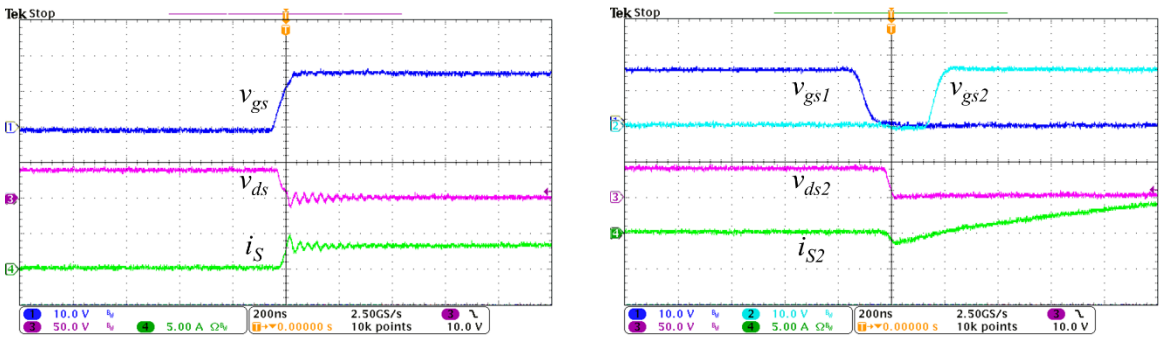


(a) (b)

Fig. 4.3: (a) Switching waveforms of diode D at a duty ratio of S = 50%. (b) Switching waveforms for diode D at a duty ratio of S = 70%. v_{gs}: 20V/div, v_D: 50V/div, i_D: 10A/div.

The switching waveforms of the power diode D are shown in Fig. 4.3, which displays the voltage across the diode v_D and the current flowing through the diode i_D regarding the switching signal. Fig. 4.3a represents a duty ratio of 50%, while Fig. 4.3b represents a duty ratio of 70%.

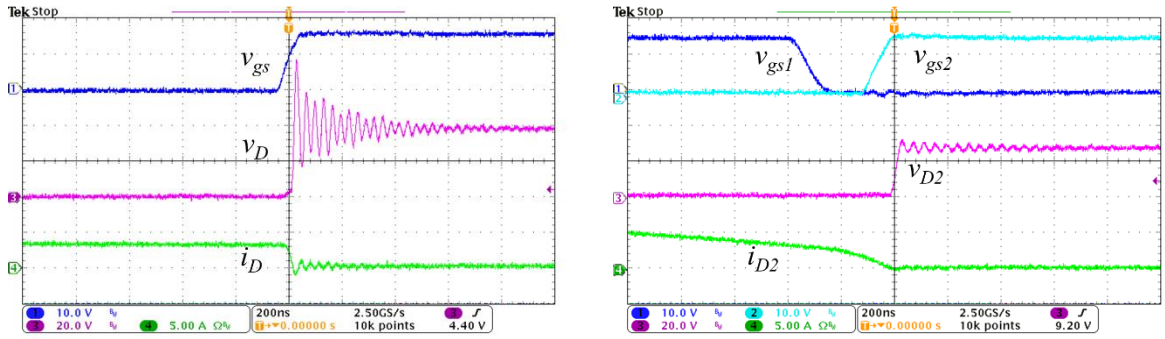
The switching waveforms in Fig. 4.2 and Fig. 4.3 are zoomed in to investigate the difference between hard-switching and soft-switching operations. Fig. 4.4a shows the switching waveforms of the buck converter's transistor, while Fig. 4.4b exhibits the soft-switching waveform of the half-bridge SRC as depicted in Fig. 3.8b. Similarly, Fig. 4.5a displays the switching waveform of the buck converter's diode, while Fig. 4.5b showcases the soft-switching waveform of the half-bridge SRC from Fig. 3.11b.



(a) (b)

Fig. 4.4: (a) Hard switching of the transistor in the buck converter. (b) Soft switching of the transistor in the half-bridge SRC. v_{gs}, v_{gs1} and v_{gs2}: 10V/div, v_{ds} and v_{ds2}: 50V/div, i_S and i_{S2}: 5A/div.

In Fig. 4.4a, the transistor gate signal turns on while the drain-to-source voltage is still high, resulting in a hard-switching operation. In contrast, the self-contained soft-switching capability of the half-bridge SRC, illustrated in Fig. 4.4b, enables the transistor to turn on when the drain-to-source voltage is zero, thanks to the negative drain current of the transistor.



(a) (b)

Fig. 4.5: (a) Hard switching of the diode in the buck converter. (b) Soft switching of the diode in the half-bridge SRC. v_{gs}, v_{gs1} and v_{gs2}: 10V/div, v_D and v_{D2}: 20V/div, i_D and i_{D2}: 5A/div.

In Fig. 4.5a, the buck converter's diode turns off while the transistor's gate signal is on, leading to a hard switching turn-off with the diode current still above zero. Comparatively, the soft-switching capability of the half-bridge SRC, demonstrated in Fig. 4.5b, allows the diode to turn off when the diode current reaches zero, exemplifying the advantages of soft-switching.

Voltage Gain and Efficiency Comparison

The voltage gain curve of the buck converter is illustrated in Fig. 4.6. The experimental voltage gain curve is plotted within the duty cycle range of 35% to 90%. Additionally, a theoretical voltage gain curve is included for comparison purposes.

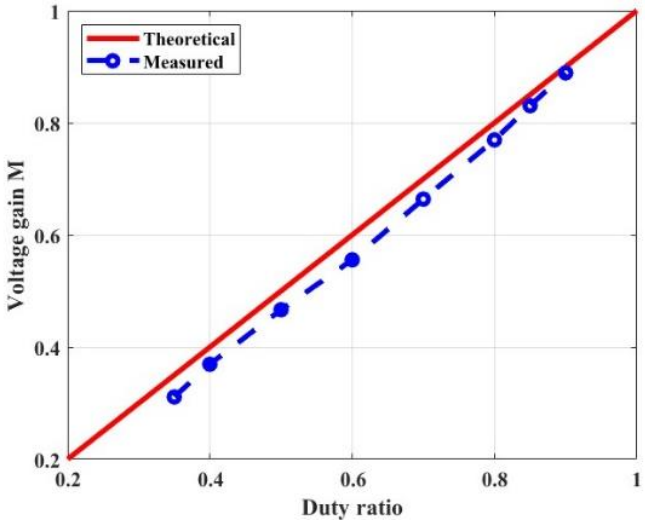


Fig. 4.6: Voltage gain curve of the buck converter.

To evaluate the efficiency of the buck converter and compare it with the half-bridge SRC, two different switching frequencies, i.e., 100kHz and 200kHz, are performed. The experimental conditions align with those depicted for the experiment in Fig. 3.16, where the input power is 160W, and the input voltage is 36V. The efficiency of the buck converter under both switching frequencies is presented in Fig. 4.7. Furthermore, the efficiency of the half-bridge SRC is included in the comparison.

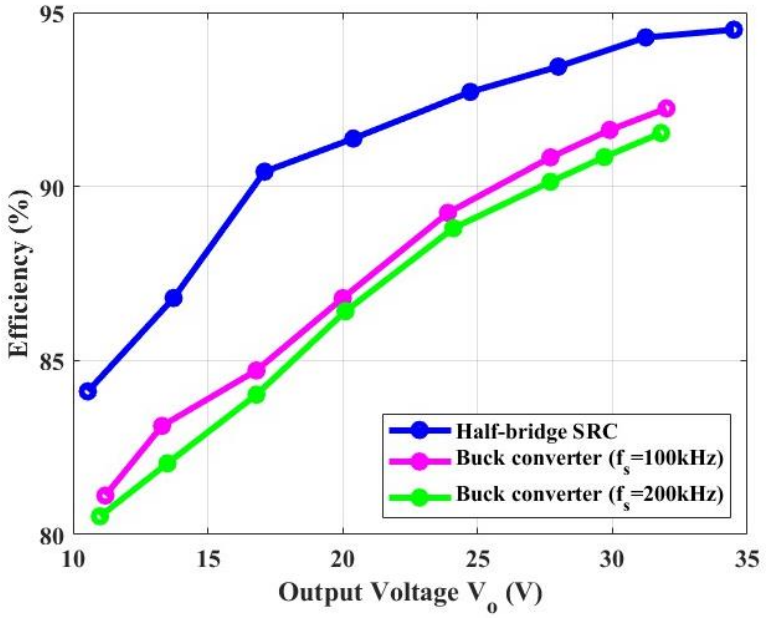


Fig. 4.7: Efficiency comparison of two topologies.

The buck converter achieves its highest efficiency when operated with a duty ratio of 90% and a switching frequency of 100kHz, reaching 92.2%. As the duty ratio decreases, the efficiency of the buck converter diminishes. Notably, as demonstrated in Fig. 4.7, the efficiency of the buck converter with a switching frequency of 200kHz is lower than that with a switching frequency of 100kHz under the same duty ratio. This decline in efficiency is attributed to increased switching losses associated with higher switching frequencies.

Overall, the half-bridge SRC exhibits much higher efficiency using the same circuit parameters, consistently outperforming the buck converter's efficiency. The half-bridge SRC achieves a minimum of 2.1% and a maximum of 5.3% higher efficiency than the buck converter.

CHAPTER 5: Summary and Discussion

In this research, a comprehensive review of the development of MPPT applications is provided, covering PV array characteristics [1], previous MPPT techniques [2]-[12], and commonly used DC-DC converter topologies [4][5][13]. Due to its superior efficiency, this study focuses on the soft-switching topology [14]-[20]. Ultimately, the half-bridge series resonant converter topology was selected due to its inherent soft-switching capability and high power density. The limitation of conventional SRCs, namely poor voltage regulation, was overcome by employing the fixed on-time control method [21]-[24].

To validate the feasibility of using a resonant converter for MPPT applications, a half-bridge SRC-based MPPT system was proposed. A detailed system analysis of the half-bridge SRC, examining its operation, characteristics, and performance, is given in the thesis. Additionally, techniques and advanced perturb and observe algorithms were selected for optimal power extraction from solar panels.

Experimental results demonstrate the effectiveness of the half-bridge SRC-based MPPT approach. ZVS turn-on and ZCS turn-off were achieved, achieving an efficiency of 95.4% in the laboratory environment with a voltage gain close to 1. In the MPPT experiment for 24V battery charging, the system achieves 92.6% efficiency and effectively tracks the PV system's maximum power point using the proposed algorithm.

Moreover, a comparison between the half-bridge SRC and a conventional buck converter explicitly examines their hard-switching and soft-switching operations. The

comparison demonstrated a much higher efficiency of the half-bridge SRC, showing an efficiency improvement in the range of 2% to 5% compared to the buck converter.

Although the proposed system exhibits excellent efficiency compared to the conventional buck converter, certain disadvantages still need to be addressed and can be explored in future research. For instance, in the proposed system, the RMS current can reach up to twice the value of a conventional buck converter operating under the same output voltage condition. This higher current stress in the resonant circuits may require higher rating components for the system. Additionally, this study does not cover the resonant inductor and capacitor design. The choice of the resonant tank can significantly impact overall efficiency by affecting the Q value. According to equations (36) and (37), the impedance change will affect the Q value under the same load resistor. The smaller the Q value, the higher the efficiency, but at the same time, the RMS current of the resonant tank will also increase. Optimizing the design of the resonant tank is a potential avenue for future research.

It is important to note a limitation that affected the experiments. Theoretically, the resonant converter can operate at a higher switching frequency (several megahertz) with a small size and high efficiency. However, the microcontroller used in the experiments restricts the half-bridge SRC's switching frequency, preventing the proposed circuit from leveraging the resonant converter's soft-switching capabilities at higher frequencies. With higher switching frequency, the resolution of the duty ratio will decrease, which increases the minimum duty step and results in inaccurate MPPT outcomes. Consequently, the proposed MPPT system operates at a switching frequency

of 100 kHz to 200 kHz. If a microcontroller with a higher frequency were utilized, the benefits of soft-switching operation would become more pronounced. By operating at a switching frequency in the megahertz level, a more significant efficiency advantage over the buck converter could be achieved, surpassing the 2% improvement observed in this study.

The proposed PV charging system offers a feasible solution for integrating into standalone solar systems, demonstrating an improvement in efficiency compared to conventional converters. The system's high-frequency operation capability offers several benefits, including reduced size and weight of passive components, allowing for easier installation and integration into space-constrained environments. Additionally, the proposed PV charging system excels in reducing EMI emissions, which allows for a simplified filtering mechanisms design with reduced size and cost. These combined advantages establish the proposed PV charging system as an efficient, reliable, and compact solution for standalone solar applications.

In conclusion, the half-bridge series resonant converter-based MPPT system effectively fulfills the objective of power extraction from the PV array, demonstrating outstanding efficiency and soft-switching operation. Future research may concentrate on exploring higher switching frequencies and optimizing the design of the resonant tank to enhance system performance further.

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