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Deposition of High-K dielectrics on 2D-semiconductors via low temperature ALD

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy

in

Materials Science and Engineering

by

Iljo Kwak

Committee in Charge:

Professor Andrew C. Kummel, Chair
Professor Prabhakar R. Bandaru
Professor Yu-hwa Lo
Professor Wei Xiong
Professor Paul K. Yu

2018

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The dissertation of Iljo Kwak is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California San Diego

2018

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LIST OF SYMBOLS AND ABBREVIATIONS

Å	angstrom
AFM	atomic force microscopy
ALD	atomic layer deposition
BE	binding energy
CB	conduction band
C_{max}	maximum capacitance
CV	capacitance voltage
CVD	chemical vapor deposition
DFT	density functional theory
DMA	dimethylaluminum
DOS	density of states
e	electron
EF	Fermi level
EOT	equivalent oxide thickness
h	Planck's constant
I	electric current
KE	kinetic energy
L	Langmuir
LDOS	local density of states
MBE	molecular beam epitaxy

MMA	monomethylaluminum
MOSCAP	metal oxide semiconductor capacitor
MOSFET	metal oxide semiconductor field effect transistor
nA	nanoamps
nm	nanometer
pA	picoamps
PBE	Perdew-Burke-Emzerhof
PBN	pyrolitic boron nitride
PDA	post deposition anneal
SPM s	canning probe microscopy
SRC	Semiconductor Research Corporation
STM	Scanning tunneling microscopy
TMA	trimethylaluminum
UHV	ultra high vacuum
V	volts
VASP	Vienna ab-initio simulation package
VB	valence band
Vth	threshold voltage
XPS	x-ray photoelectron spectroscopy
υ	frequency
Φ_{spec}	spectrometer work function

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ACKNOWLEDGEMENTS

Foremost, I would like to acknowledge Prof. Andrew Kummel, my advisor, for his continuous support, encouragement and patience. I sincerely appreciate his guidance and intellectual inputs on my Ph.D. research and career plans. I'm also grateful to the opportunities to participate in various projects that helped me to gain hands-on experience for my career and resume.

I would also like to acknowledge both former and current members of Prof. Kummel's lab. Jun Hong Park (Professor Park, as of now) taught me what I know about vacuum science and importance of being patient. Scott Ueda has been a great and smart colleague; he made a take-over and training process very easy. I would also thank all other labmates: Jongyeon Choi, Steven Wolf, Chris Ahles, Mike Breeden, Mahmut Sami Kavrik, James Wang and Emily Thomson for the experimental support and insightful suggestions. Special thanks go to Dr. Bernd Fruhberger, Larry Grissom and other staffs in Nano3 cleanroom facilities for the support developing Nanofog ALD technique.

A lot of the work performed in my Ph.D. was not possible without our collaborators. Professor Sanjay Banerjee group always provided quality 2D materials samples and Professor Alan Seabaugh group put lots of effort in fabricating FET devices with our gate oxide. I could have not published a paper without their helps. I would also thank my committee members, Professor Paul Yu, Professor Yuhwa Lo,

Professor Bandaru Prabhakar and Professor Wei Xiong for their precious time to attend my senate exam and defense also for the insightful comments and question.

The work in this dissertation was supported in part by the National Science Foundation Grant DMR 1207213, by the Center for Low Energy Systems Technology (LEAST) and Applications and Systems driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT). STARnet and JUMP sponsored by Semiconductor Research Corporation (SRC) programs and DARPA, and by the SRC Nanoelectronic Research initiated through the South West Academy of Nanoelecronics (SWAN).

Last but not least, I would like to acknowledge my parents, my wife and my son about to be born. I appreciate the endless and selfless support they have given me throughout Ph.D. years. I know it would not have been possible to start this thesis without them.

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VITA

EDUCATION

2007 Bachelor of Materials Science and Engineering, Seoul National University, Seoul, Korea

2009 Master of Materials Science and Engineering, Seoul National Universty, Seoul, Korea

2018 Doctor of Philosophy in Materials Science and Engineering, University of California San Diego

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FIELD OF STUDY

Major Field: Materials Science and Engineering

Studies in Surface Science and Physical Chemistry

Professor Andrew C. Kummel

ABSTRACT OF THE DISSERTATION

Deposition of High-K dielectrics on 2D-semiconductors via low temperature ALD

by

Iljo Kwak

Doctor of Philosophy in Materials Science and Engineering

University of California San Diego, 2018

Professor Andrew C. Kummel, Chair

2D materials such as graphene and TMDCs (Transition Metal Dichalcogenides) have increased interest in the research of future electronic devices due to their excellent

electronic properties. These materials can be easily exfoliated to make a monolayer which enables us to study the 2D properties of the materials such as the quantum confinement effect. In case of TMDCs, intrinsic bandgaps of the materials provide possible applications in digital logic devices. TMDCs also have ideal material properties for TFETs (Tunnel Field Effect Transistors). Having no dangling bond at the materials' surface, defects at the heterojunction interface can be minimized enabling to obtain steep TFETs with lower subthreshold swing. To realize these properties in the devices, preparation of insulating and uniform gate oxide with low EOT (Equivlaent Oxide Thickness) is required. However, due to the inert surface nature of 2D materials, various functionalization techniques have been used to initiate nucleation of the gate oxide. However, these functionalization methods inevitably induce damage to 2D materials, changing the electronic properties of 2D materials. Therefore, for successful fabrication of 2D materials electronic devices, a more facile gate oxide deposition method with low surface defects is needed.

This thesis consists of three parts. In the first part(Chapter 2), deposition of Al_2O_3/ HfO_2 bilayer nanolaminate structures on $Si_{0.7}Ge_{0.3}$(100) by thermal ALD was studied to develop high-K oxide with lower interface defects for 2D materials. It is shown that Al_2O_3/ HfO_2 bilayer or nanolaminate structures effectively reduced the density of interface traps more than 30% at the expense of a small capacitance drop in the accumulation. In addition, 3 orders of magnitude lower leakage currents were achieved compared to pure HfO_2 layer. Second part (Chapter 3) introduces mechanism

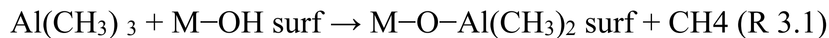
of low temperature ALD of Al_2O_3 on graphene. This study shows that a uniform and defect free Al_2O_3 film can be grown on graphene by ALD at low temperature without any functionalization techniques. The Capacitance-Voltage measurements of the 50 cycles of ALD Al_2O_3 films growth at 50°C showed 1.17 μF/cm^2 with very low leakage current of the Al_2O_3 was in order of $10^{-}5$ A/cm^2 which is consistent with the absence of pinholes. In the last part (Chapter 4), deposition of high quality Al_2O_3 and HfO_2/Al_2O_3 films on 2D materials using low temperature ALD/CVD was demonstrated. C_{max} and leakage current values of 50 cycles of low temperature ALD Al_2O_3 on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}(001)$ were comparable indicating uniform and pinhole free Al_2O_3 films across the entire surface. To obtain lower EOT, Al_2O_3 (7 cycles at 50 °C)/HfO_2(40 cycles at 300 °C) bilayer gate oxide was prepared on 2D materials substrates. C_{max} was increased by 2x compared to 50 cycles Al_2O_3 MOSCAPs. In addition, Pd/Ti/TiN gate was employed to scavenge the oxygen from the oxide. C_{max} of ~2.7 μF/cm^2 was achieved with MoS_2 and HOPG without loss of leakage current density. All 2D materials MOSCAPs in this study had lower interfacial defect density (D_{it}) compared to the same gate stacks on $Si_{0.7}Ge_{0.3}(001)$ indicating Van der Waals interactions between the oxide and the 2D material surfaces is dominant instead of chemical bondings.

Chapter 1. Introduction

1.1 ALD

ALD is a method of depositing various thin films on substrates with atomic scale precision. Chemistry of ALD is Similar to chemical vapor deposition (CVD) but it consists of two half-CVD reactions; first, the precursor is released in to a reactor and the precursor molecules adsorb on a substrate, excess layers of the reactant are purged from the reactor. Afterward, second precursor, which is typically oxidizer, is introduced to react with the first reactant, ideally, resulting in a monolayer of the film. [1]

ALD enables atomic scale thickness control by self-limited process based on the surface reactions. The reactions can be simply explained with deposition of Al_2O_3 on a substrate by ALD using trimethylaluminum (TMA, $Al(CH_3)_3$) and water(H_2O).



$$Al(CH_3)_3 + M{-}OH\ surf \rightarrow M{-}O{-}Al(CH_3)_2\ surf + CH4\ (R\ 3.1)$$

$$M{-}O{-}Al(CH_3)_2\ surf + 2\ H2O \rightarrow M{-}O{-}Al(OH)_2\ surf + 2\ CH4\ (R\ 3.2)$$

In this process, first, TMA molecules adsorb on the substrate reacting with the hydrogen terminated substrate surface to form a bond between Aluminum and oxygen atoms releasing a molecule of methane as a byproduct (Figure 1.1). Purging process is employed to remove excess TMA molecules on the surface. In the second step, H_2O

molecules are delivered on the surface and react with TMA molecules releasing methane CH_4 gas as a product and leaving with hydroxyl groups (-OH) (Figure 1.2). Excess H_2O and methane gas are also removed by another purge process. Being the surface is terminated with the hydroxyl groups which provide nucleation sites for TMA, the whole process cycle can be repeated until the desired thickness is achieved. As shown in this case, only surface reactions are involved while gas phase nucleation and interaction dominate in CVD process, therefore, the growth of the film by ALD can be controlled by the self-limiting mode.[1] When all the nucleation sites on the surface are occupied by one of precursor molecules, the reaction can no longer proceed because the precursors do not react with themselves. Since additional precursors are physiosorbed on the surface, they can be pumped away with a inert purge gas such as nitrogen (N_2) or argon (Ar) flowing through the reactor.

Growth rate and uniformity of a ALD process can be controlled by a number of factors, such as temperature, pulse time of the precursors and purge time between the precursor doses. In case of the reactor temperature, it should be higher to initiate the surface reactions and should be lower than the decomposition temperate of the precursor. For ALD, available precursors for a specific film deposition is limited compared to CVD because the precursors must not react with themselves to enable the self-limiting mechanism to work.

1.2 MOS (Metal Oxide Semiconductor) Capacitor

The MOS capacitor refers to a Metal-Oxide-Semiconductor structure as shown in Figure 1.3. The structure shown has a p-type substrate. The oxide layer can be prepared by various techniques such as thermal oxidation, CVD, ALD. Metal gates applying bias to the semiconductor substrate are typically deposited using sputtering or E-beam evaporation. In addition, another metal gate is formed on the back side of the semiconductor to make an ohmic contact. MOS capacitors are important devices in solid-state electronics. Due to the presence of an oxide layer and two surface-charge regions, MOS physics is wildly used to investigate interface properties or defect density of the devices.

1.2.1 Energy-band diagram of a MOS Capacitor

The Energy-band diagram of a p-type MOSCAP is shown in Fig.1.4. In case of zero applied bias (at equilibrium), due to the metal (ϕm) and semiconductor (ϕs) work-function difference (ϕm-ϕs), the band is bent down in the semiconductor side. In order to make the band flat (flatband condition), positive voltage should be applied to the capacitor. This voltage refers to "flatband voltage". Electrical charges (holes or electrons) can accumulate at the semiconductor interface and the equal but opposite sign at the interface between the metal and to the oxide layer under any biasing conditions. In ideal case, there is no carrier transport through the oxide layer under dc bias conditions and the resistivity of the oxide is assumed infinite.

1.2.2 Biasing the MOS Capacitor

By applying bias to a MOSCAP, it is possible to accumulate or deplete charges at the semiconductor surface. Depending on the bias and the doping type of the semiconductor, operation mode of the device can be divided as accumulation, Depletion and inversion regimes. Figure 1.5 shows the different bias modes of an MOS capacitor.

1.2.2.1 Accumulation

Accumulation occurs when one applies a voltage, which is less than the flatband voltage. The minority carriers on the gate attract majority carriers from the substrate to the oxide semiconductor interface. Only a small amount of band bending is needed to build up the accumulation charge so that almost all of the potential variation is within the oxide.

1.2.2.2 Depletion

As a more positive voltage than the flatband voltage is applied, a negative charge builds up in the semiconductor. Initially this charge is due to the depletion of the semiconductor starting from the oxide-semiconductor interface. The depletion layer width further increases with increasing gate voltage.

1.2.2.3 Inversion

As the potential across the semiconductor increases beyond twice the bulk potential, another type of negative charge emerges at the oxide-semiconductor interface: this charge is due to minority carriers, which form a so-called inversion layer. As one further increases the gate voltage, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential.

1.3 Interface state of MOSCAP and extraction methods

Defects and impurities can be incorporated into the oxide layer during oxide growth or device making processing steps. This results in the oxide being contaminated with various types of charges and traps. In general, four different types of charges can be detected in oxide layer on a semiconductor. These charges are shown schematically in Fig. 1.6.[5] They are interface-trapped charges Qit, fixed-oxide charges Qf, oxide-trapped charges Qot, and mobile ionic charges Qm. All of these charges are very dependent on the device fabrication process. Figure 1.7 is the energy band-diagram of a metal-oxide-semiconductor.[5] The periodic nature of the semiconductor is abruptly terminated at the interface allowing electronic energy levels to exist within the forbidden band gap. These allowed energy states are referred to as interface states. Charge can be transported between the semiconductor and interface-states, in contrast to

the fixed-oxide charge. The net charge in these interface-states is a function of the position of the Fermi level in the band-gap. In general, acceptor states exist in the upper half of the band-gap, and donor states exist in the lower half of the band-gap. An acceptor state is neutral if the Fermi level is below the state and becomes negatively charged if the Fermi level is above the state. A donor state is neutral if the Fermi level is above the state and becomes positively charged if the Fermi level is below the state. The charge of the interface-states is then a function of the gate voltage applied across the MOS capacitor.

1.3.1 Extraction of Interface state density from C-V and G-V plot

Performance and reliability of semiconductor devices depend on the electrical properties of oxide layer and semiconductor interfaces. Therefore, the interface state density (Dit) of semiconductor surfaces is an important issue for device performance. Interface state density can be extracted using measured C-V and G-V characteristics when realistic, bias-dependent trap time constants are assumed. Applying either Terman method or the conductance method to the model data then plays the interface-state densities back.

1.3.1.1 C-V Stretchout (Terman-Berglund) Method

Extraction of interface-state density by the stretchout of high frequency C-V curve was first proposed by L.M. Terman in 1962, hence also known as Terman method.[6] It is assumed that the small signal frequency is high enough that the total measured capacitance at that frequency has no interface-state component. The only effect of the interface states is then to cause a stretchout of the CV curve along the gate voltage (Vg) axis given by where ψ_s is the surface potential, C_{ox} is the gate oxide capacitance, C_s is the intrinsic semiconductor capacitance, and $C_{it} = qD_{it}$ is the interface-state capacitance. At high frequency, the surface states are unable to follow the AC signal component of bias voltage.

Berglund used the method for low-frequency CV and theoretical curve. The low-frequency approach extracts C_{it} through the increase of capacitance at each gate bias value, especially in depletion where the effect is most pronounced. [7]

$$C_{it}(V_G) = \left(\frac{1}{C(\psi)} - \frac{1}{C_{ox}}\right)^{-1} - C_S(\psi)$$

where C(ψ) is the measured total low-frequency MOS capacitance as a function of band bending.

Another approach developed by Castagn´e and Vapaille is to use $C_S(V_G)$ with the stretching caused by D_{it}, but without the added capacitance by the combination of

low and high frequency measurements.[8] A theoretical curve is not required for this case. C_{it} then can be extracted by the equation below.

$$C_{it}(V_G) = \left(\frac{1}{C_{lf}(V_G)} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{hf}(V_G)} - \frac{1}{C_{ox}}\right)^{-1}.$$

1.3.1.2 D_{it} extraction using Conductance Method

The conductance method was proposed by Nicollian and Goetzberger in 1967 and interface trap densities of 10^9 cm^{-2} eV^{-1} and lower can be measured [9]. The conductance method is to measure the equivalent parallel conductance Gp of an MOS-C as a function of bias voltage and frequency. Conductance Gp represents the loss mechanism caused by interface trap capture and emission of carriers, which is a measure of interface state density.

Figure 1S(a) shows the simplified equivalent circuit of an MOS-C. Cox is the oxide capacitance, C_S is the semiconductor capacitance, Cit is the interface trap capacitance and R_{it} is the lossy process caused by the capture-emission of carriers due to interface state density.

Cp and Gp are represented by Eq. 1 and 2.

$$C_p = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2} \quad \text{(Eq. 1)}, \qquad \frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \quad \text{(Eq. 2)}$$

where $C_{it}=q^2 D_{it}$, $\omega=2\pi f$ (f=measurement frequency) and $\tau_{it}=R_{it}C_{it}$, the interface trap time constant, given by $\tau_{it}=[v_{th}\sigma_p N_A \exp(-q\varphi s/kT]^{-1}$. Dividing Gp by ω makes Eq. 1 symmetrical in terms of $\omega\tau_{it}$. Eq 1 and 2 are single energy level interface traps in the band gap. Interface traps at the MOSCAPs interface, however, are continuously distributed in energy. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as Eq 3.

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1+(\omega\tau_{it})^2]$$

(Eq. 3)

The conductance is measured as a function of frequency and plotted as Gp/ω versus ω. Gp/ω has a maximum at $\omega=1/\tau_{it}$ and at that maximum D_{it} =2 Gp/qω. For Eq. 3, maximum D_{it}=2.5 Gp/qω can be obtained where $\omega \approx 2/\tau$. Hence, D_{it} can be extracted from the maximum Gp/ω on the ω-axis.

1.4 2D Semiconductor materials

2D materials are defined as materials which have strong in-plane bonds but weak out of-plane bonds with van der waals force so that the individual planes can be readily exfoliated. For example, graphene has strong covalent bonds between each of carbon atoms, but has weak bonding between the layers. Due to this property,

monolayer of graphene can be easily prepared with a mechanical exfoliation method using an adhesive tape. Other materials of interest are transition metal dichalcogenides [10],[11] (TMDCs), transition metal oxides[12], topological insulators[13], hexagonal boron nitride[14]. These materials have long been studied due to their extensive optical, electrical, chemical, thermal properties and the quantum confiemant effects in these materials. These 2D materials have large surface areas, providing improved surface sensor study. Unlike graphene, TMDC 2D semiconductors offer controllable band gaps which lead to applications in logic devices [10]. As the carriers are confined to this sub-nanometer thickness, they offer excellent gate electrostatics with reduced short channel effects [15].

1.4.1 Graphene

Graphene was the first material that raised interest in layered materials. It was initially studied in 2004 by researchers Andre Geim and Konstantin Novoselov in Manchester, UK, and the study of the physics[16] related to single-layer graphene eventually led them to win the Nobel Prize in 2010. It is a single sheet of closely knitted sp2 carbon atoms in a hexagonal pattern where all the carbon atoms are well saturated, resulting in no dangling bonds on the surface. This characteristic result of graphene having no interface traps made it the most suitable material for high frequency electronics [17], and RF applications [18]. Graphene can be easily exfoliated from a single crystal of highly ordered pyrolytic graphite using scotch tape. Figure 1.9 (a)

shows the honeycomb lattice of graphene and fig. 1.9 (b) shows the linear E-k diagram of graphene and the dirac cone where the electrons and hole act like mass-less particles. It is an excellent conductor, with sheet resistance of less than 30 Ω/sq, and nearly transparent [19]. This high degree of optical transmission makes it a viable competitor in the race to replace Indium tin oxide (ITO) as a transparent conductor. Other advantages of graphene which make it a better replacement for ITO include its low cost of fabrication when using a chemical vapor deposition (CVD) process, high electron mobility (>3000 cm2/Vs for CVD graphene), and high thermal and mechanical flexibility [20]. Researchers have also used graphene electrodes in touch panels, displays, solar cells, and bio-sensors.

1.4.2 Molybdenum disulfide (MoS_2)

Graphene has been investigated for ultrahigh speed transistors or RF devices, due to zero band gap nature resulting in insufficient current on-off ratio and voltage gain. However, the semiconducting MoS_2 has recently attracted considerable interest for overcoming these disadvantages of graphene with high on-off ratio and intrinsic voltage gain [21], [22]. A single layer of MoS_2 consists of a layer of Mo atoms sandwiched between two layers of S atoms. As a 2D material, it shares many interesting characteristics of the graphene such as atomically thin thickness (0.7 nm), excellent electronic properties, mechanical flexibility, and optical transparency, 2D electronics based on single or few-layer MoS_2 could be a promising candidate for future electronic

devices. With a larger band gap than silicon, MoS_2 can suppress the source-to-drain tunnelling current in transistors at the scaling limit [22]. Moreover, MoS_2 and other TMDC materials are attractive as a low-cost flexible electronics that has been intensively with amorphous silicon and organic semiconductors with low mobilities around 1 cm^2 /V·s or less [23]. A key step to realize the electronic application using 2DLMs is the demonstration of integrated circuits functioning in the gigahertz frequency regime. However, the 2DLMs circuits reported to date can only function in a few megahertz or even lower frequency regime [21]. The difficulties in integrating high quality dielectrics and conducting subtractive lithography on atomically thin materials have prevented achieving 2DLMs transistors with optimized device geometry and performance. It is a well-known challenge to integrate dielectrics with graphene because of the intrinsic incompatibility of graphene with typical oxide dielectrics or their deposition approaches24. Despite several attempts to date, the integration of high quality high-k dielectrics on TMDs such as MoS2 remains elusive [24]. Furthermore, another significant challenge to achieve high performance devices based on these atomically thin materials is their intrinsic incompatibility with the conventional subtractive lithography processes (e.g. various plasma etching) that can severely damage the atomic structure and degrade the electronic properties.

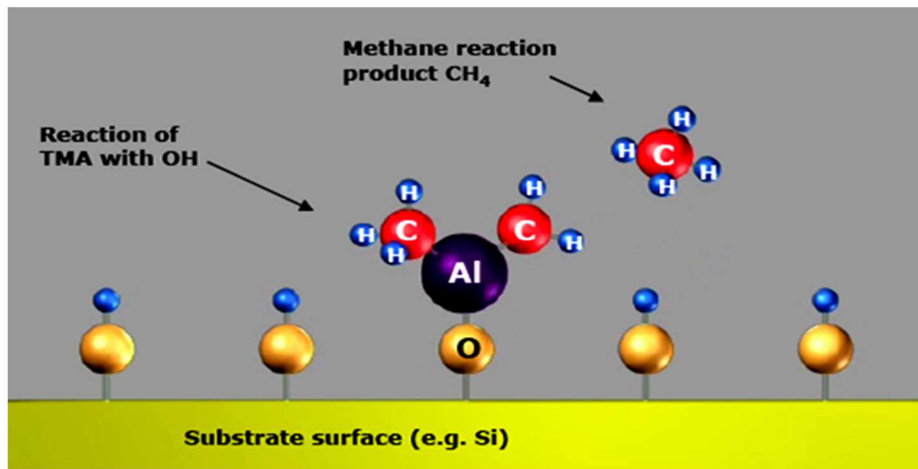


Figure 1.1 Al_2O_3 ALD cycle (a) – TMA reacts with the hydroxyl groups producing methane as the byproduct. [2]

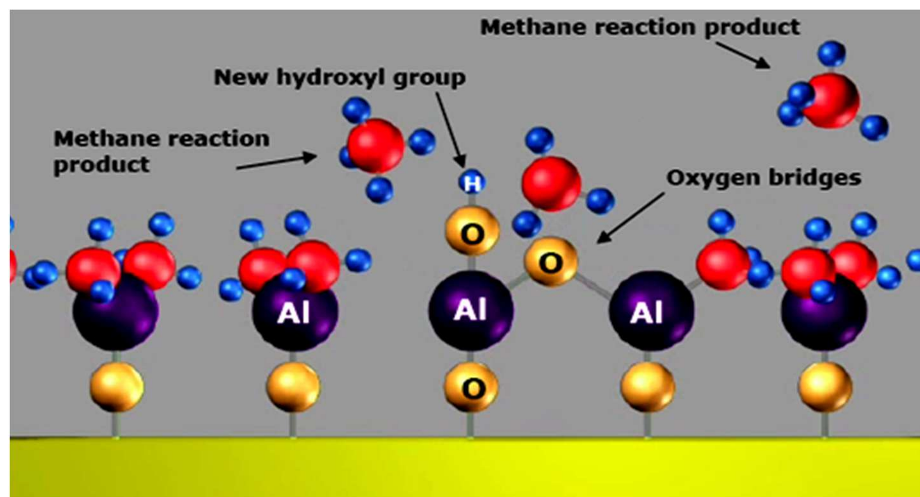


Figure 1.2 Al_2O_3 ALD cycle (b) – The methyl groups and H_2O reacts and form Al-O bonds and hydroxyl surface groups. Methane is produces as the byproduct. [2]

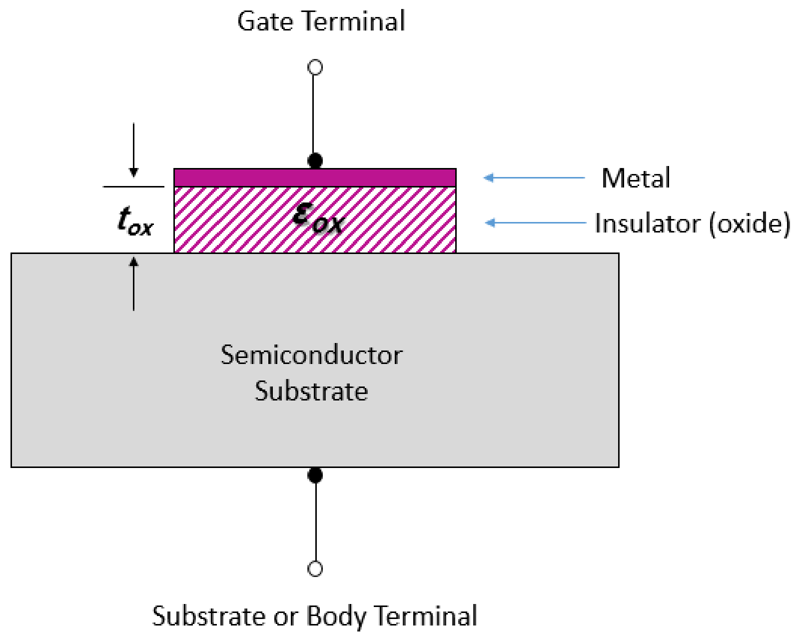


Figure 1.3 Schematic diagram of a MOSCAP [3]

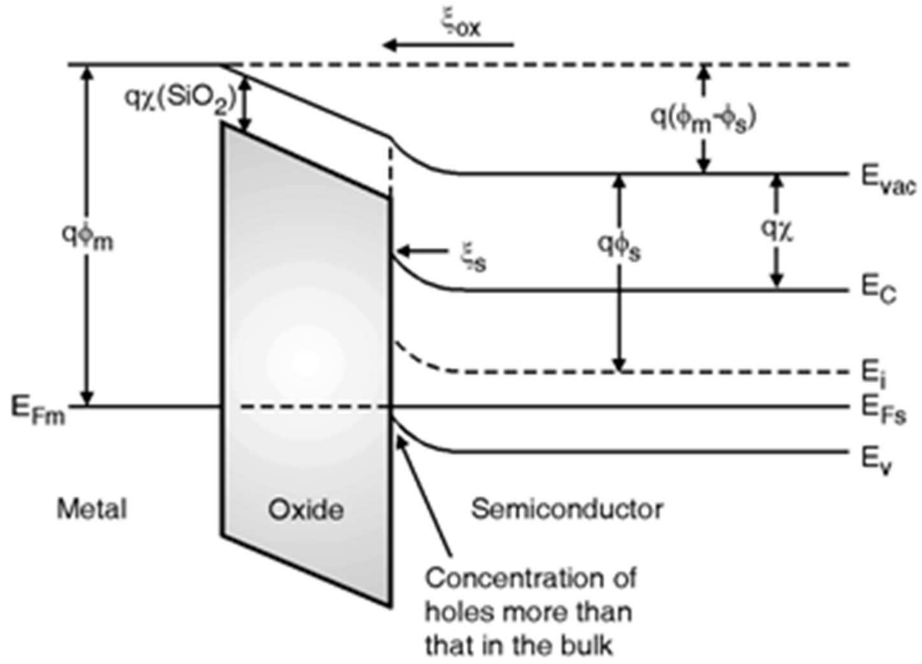


Figure 1.4 Band diagram of MOS structure at equilibrium [4]

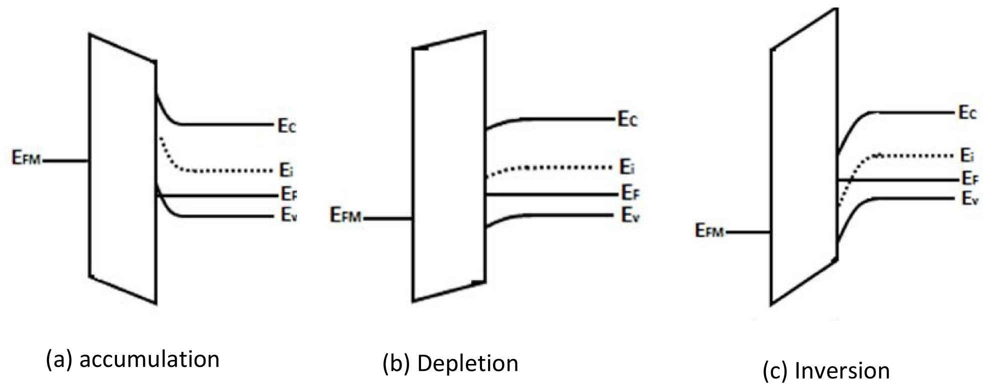


Figure 1.5 Different modes of a p-type MOS biasing

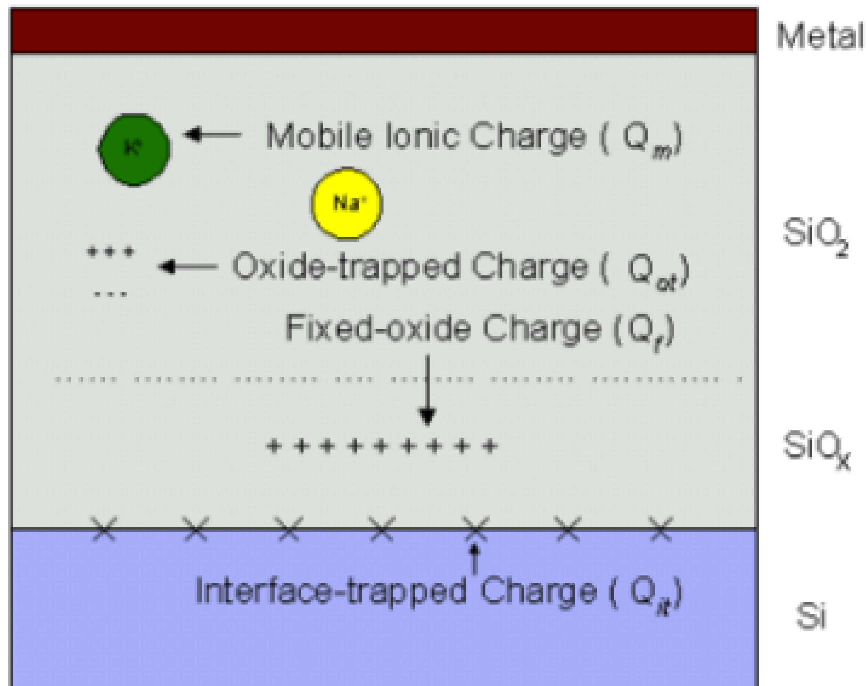


Figure 1.6 Defect charges in MOSCAP device [5]

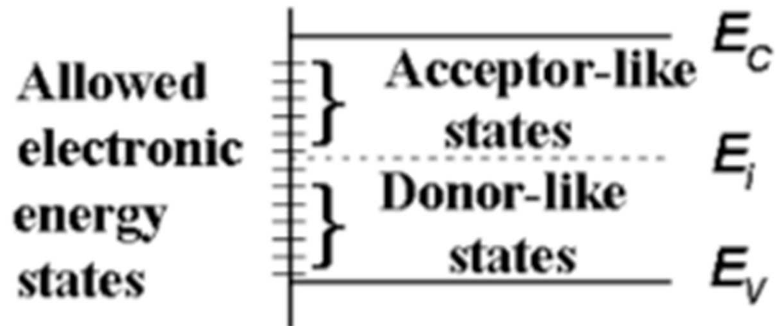


Figure 1.7 Diagram of interface states at the oxide-semiconductor interface [5]

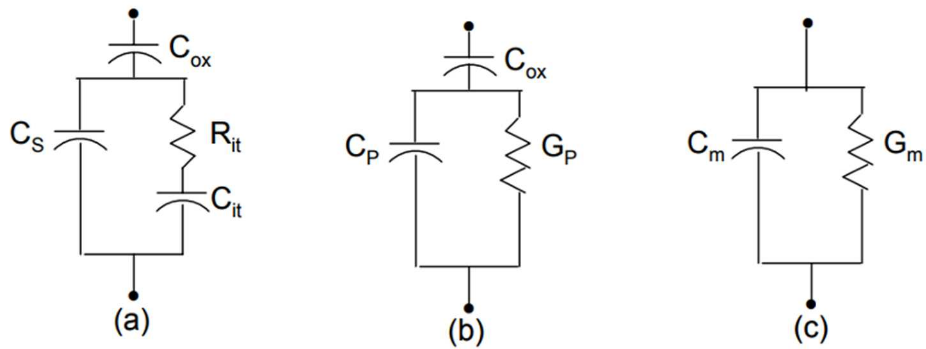


Figure 1.8 Equivalent circuits for conductance measurement. (a) MOS-C with interface trap time constant, (b) simplified circuit, (c) measured circuit. The circuit of Figure (a) can be simplified by the circuit of Figure (b).

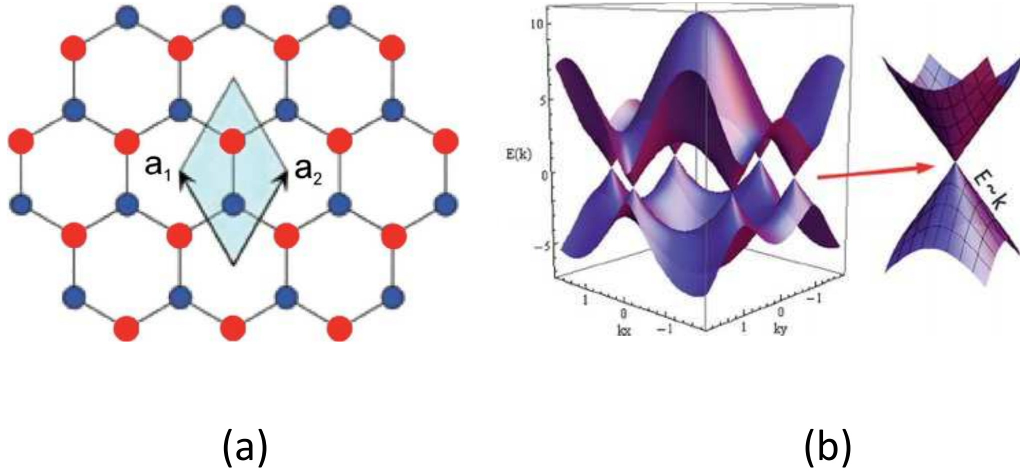


Figure 1.9 Intrinsic Properties of Graphene (a) Honeycomb lattice of graphene (b) E vs. k plot of graphene showing the conduction band and the valence band meeting at the K points. [19]

Chapter 2. Development and optimization of HfO_2/Al_2O_3 structure on $Si_{0.7}Ge_{0.3}$ (100) Surface by Thermal Atomic Layer Deposition for 2D materials

2.1 Abstract

To fabricate future 2D materials based devices, it is essential to deposit very thin high-k dielectrics on 2D materials surfaces with low density interfacial defects. In this chapter, development and optimization process of Al_2O_3/HfO_2 nanolaminate (HfO_2 layers incorporated with Al_2O_3 monolayers) gate stacks by atomic layer deposition (ALD) using $HfCl_4$ and H_2O precursors was introduced. Electrical properties of the interfaces were quantified by capacitance-voltage (C–V) spectroscopy. Interfaces of nanolaminate stacks were found to have 2x smaller density of interface traps (D_{it}) than pure HfO_2 gate stacks. Cross sectional TEM with Energy-dispersive X-ray spectroscopy (EDS) showed that an SiOx rich interlayer was formed between the nanolaminate and the $Si_{0.7}Ge_{0.3}$(001) substrate. The SiOx interlayer contains almost no Ge indicating that the $HfCl_4$/TMA nanolaminate deposition reduced the GeOx in the interface. Furthermore, the SiGe surface was enriched in Ge from 30% to ~70% consistent with the $HfCl_4$/TMA nanolaminate process reducing and redepositing Ge on the SiGe surface.

2.2 Introduction

In this study, $Si_{0.7}Ge_{0.3}(100)$ was used as a substrate to develop high-K gate oxide for 2D materials devices. Due to the inert nature of the materials, deposition of uniform oxide layer is difficult to achieve. To accelerate the development process, Silicon-Germanium surface was investigated first. In addition, Silicon-Germanium (SiGe) alloys have shown a great promise as the channel material for fin field effect transistors (FinFETs) and nanowire field effect transistors (NW-FETs) due to tunability of their carrier mobilities and band gaps by variation in Ge content and tensile/compressive stresses [25],[26],[27],[28]. SiGe alloys are expected to be more easily integrated into the existing Si CMOS fabrication technologies than III-V semiconductor or pure Ge due to rather facile growth of SiGe alloys on Si substrates [29], [30],[31],[32]. However, to ensure full integration of SiGe into the future CMOS technology, it is imperative to develop robust methods to deposit thin high-k dielectrics on SiGe surfaces with low leakage and high interface quality [33], [34],[35],[36].

One of the challenges in realizing low-defect interfaces between high-k dielectrics and SiGe is to control the Ge reactions during the oxide deposition and post deposition annealing steps [37],[38]. The presence of Ge at the high-k/SiGe interface could lead to Ge sub-oxide (GeO_x) formation which can readily diffuse within the high-k oxides [39]. In addition, since GeO and GeO_2 are volatile and unstable in the presence of Ge, they can pose reliability issues for devices [40]. Therefore, it is essential to

chemically passivate the interfaces to minimize Ge concentration at the high-k/SiGe interfaces.

Various approaches have been tested for limiting the Ge–O bond formation at the interface including sulfur passivation [37] and plasma nitridation [41]. However, these approaches were only successful for pure Al_2O_3 or Al_2O_3/HfO_2 bilayers with a 1-2 nm thick Al_2O_3 interfacial layer. Additionally, $Al_2O_3/HfO_2/Al_2O_3$ tri-layers (or sandwich) have been deposited on strained p-SiGe by ALD at 300°C, where a 0.7nm thick layer of mixed Al_2O_3-SiOx was observed at the interface [42] In that report, Al_2O_3 was employed as a spacer between HfO_2 and SiGe to prevent interfacial reactions (i.e. Ge out-diffusion) during the routine post deposition annealing of the devices. However, despite low gate leakage as a function of gate bias, the C-V curves showed high fixed and interface trap charges as well as false inversion [42].

In this chapter, electrical characteristics of the Al_2O_3–HfO_2 bilayer, nanolaminates and laminates/SiGe interfaces were compared by capacitance-voltage (C-V) and current-voltage (I-V) spectroscopy measurements on MOS capacitors (MOSCAPs). Al_2O_3–HfO_2 nanolaminates were prepared by periodic incorporation of Al_2O_3 monolayers in between HfO_2 multilayers from $HfCl_4$ based ALD. For comparison, Al_2O_3–HfO_2 laminates were prepared by deposition of single monolayers or multilayer of Al_2O_3 on the bottom and the top of the HfO_2. The nanolaminate gate oxides enabled formation of low-defect oxide/SiGe interfaces. High resolution TEM-

EDS (transmission electron microscopy-energy dispersive x-ray spectroscopy) shows that the nanolaminates form a nearly pure SiOx interlayer between the oxide and SiGe substrate.

2.3 Experimental Details

A 12nm thick p-type $Si_{0.7}Ge_{0.3}$(100) with doping level of $2x10^{18}$ cm^{-3} (Applied Materials) was grown epitaxial on p-type Si(100) by molecular beam epitaxy (MBE). Prior to ALD, SiGe native oxides were removed by cyclic HF clean using 2% HF solution and DI water at 25°C, ending with HF dip [43]. For surface passivation, HF-treated samples were immersed in 25% $(NH_4)_2S$ solution at 25 ^{o}C for 15 min followed by 30 s of DI H_2O rinse. After surface clean, the samples were transferred to the ALD chamber with less than 2 min of air exposure. HfO_2 ALD was performed at 300 °C in a commercial continuous cross-flow reactor (Beneq TFS-200) with Ar as the carrier gas. The chamber base pressure during the ALD process was about 1.7 torr. HfO_2 was deposited by consecutive cycles of 500 ms of $HfCl_4$ and 500 ms of H_2O. After each $HfCl_4$ and H_2O pulse, a 6 s long Ar purge was employed. For Al_2O_3 deposition in the cross-flow reactor, 20 cycles of 45 ms TMA pre-pulses were followed by consecutive cycles of 200 ms of TMA and 50 ms of H_2O. Similar to the HfO_2 recipe, after each TMA and H_2O pulse, a 6s Ar purge was employed. Al_2O_3 – HfO_2 nanolaminate structures were prepared by applying the above-mentioned HfO_2 and Al_2O_3 recipes in two different orders: i) 4 x [9 cycles of HfO_2 + 1 cycle of Al_2O_3]. ii) 12 x [3 cycles of

HfO_2 + 1 cycle of Al_2O_3]. Note for the nanolaminates, no TMA prepulsing was employed for each Al_2O_3 cycle. After ALD, 50 nm thick Ni gates were deposited by thermal evaporation. 100nm thick Al back gate electrode deposition was followed by DC magnetron sputtering on the back sides of the SiGe substrates. After completion of fabrication, MOSCAPs were annealed in forming gas (5% H_2, 95% N_2) at 300 °C for 15 min.

Capacitance-Voltage (C-V) spectroscopy of the MOSCAPs was performed using an Agilent B-1500 semiconductor analyzer, with AC modulation amplitude of 30 mV, and with a gate bias range of -2 to 2 V, at multiple frequencies from 2 KHz to 1 MHz. Current-voltage (I-V) spectroscopy measurements was also carried out in the bias range from -2V to 2V. Gate leakage vs. gate bias was measured in the same bias range.

2.4 Results and Discussion

The effects of the Al_2O_3/HfO_2 nanolaminate on the electrical properties of HfO_2/SiGe interfaces were determined by variable frequency C-V spectroscopy. Figure 2.1a-c displays the C–V results measured from 2 KHz to 1 MHz for HfO_2/SiGe and Al_2O_3/HfO_2 nanolaminate MOSCAPs. Densities of interface traps (D_{it}) were calculated using the conductance method [44]. Figure 2.1a displays the C-V characteristics of a MOSCAP with 50 cycles of HfO_2 deposited using $HfCl_4$ and H_2O as the precursors. As shown in Fig 2.1b and 2.1c, use of nanolaminate structures resulted in 29%

(Nanolaminate with 12 cycles of 3:1) and 39% (Nanolaminate with 5 cycles of 9:1 HfO_2: Al_2O_3) reduction in the density of interface traps relative to the pure HfO_2, at the expense of less than 0.2 μF/cm^2 drop in the accumulation capacitance. Note these nanolaminates have no direct Al_2O_3 deposition on the SiGe interface but instead have only HfO_2 deposition on SiGe. This improvement of D_{it} is hypothesized to be due to incorporated Al_2O_3 as a Ge diffusion barrier, a H_2O diffusion barrier or Ni gate metal protection layer; however, as shown by Kavrik et al, it is possible that the TMA may diffuse to the interface during deposition [45]. To better quantify the effect of TMA dosing, the values of C_{ox}/D_{it} were compared; the unit of this approximate metric was defined as $\mu F \times eV \times 10^{-12}$. For the 9:1 and 3:1 HfO_2: Al_2O_3 nanolaminates, the C_{ox}/D_{it} values were increased by 17% and 48% respectively compared to the pure HfO_2 device. Figure 2.1d-F displays the I-V spectroscopy of the pure HfO_2/SiGe and Al_2O_3/HfO_2 nanolaminate MOSCAPs. Compared to 50 cycles of HfO_2, nanolaminate samples resulted in more than 3 orders of magnitude lower leakage current which is consistent with less Ge diffusion into the nanolaminate or less diffusion of Ni during gate metallization.

In addition to being incorporated into the nanolaminate structure, Al_2O_3 can be used as an interlayer or a cap. The Al_2O_3 interlayer is hypothesized to prevent Ge out-diffusion by forming a Si-O-Al interface, while Al_2O_3 cap layer is used to protect top surface of the oxide from damage induced by the gate electrode deposition process (this includes ambient oxidation prior to gate metal deposition and Ni diffusion during gate

metal deposition) [37]. For thin HfO_2 layers, the chemistry of the Al_2O_3 cap may be more complicated since TMA might diffuse through the nanolaminate to the interface as shown by Kavrik et al. [45]. Al_2O_3 directly deposited on SiGe may reduce native GeOx to Ge [46]. Figure 2.2 displays the C-V characteristics of HfO_2/SiGe MOSCAPs with Al_2O_3 cap/interlayer. To determine the effect of the cap/interlayer layers, 3 different structures were studied: i) bilayer with Al_2O_3 interlayer: 1 or 5 cycles Al_2O_3 followed by 49 or 45 cycles of HfO_2 (Fig. 2.2a and 2.2d); ii) bilayer with Al_2O_3 cap layer: 49 or 45 cycles of HfO_2 followed by 1 or 5 cycles Al_2O_3 (Fig. 2.2b and 2.2e); iii) Al_2O_3/HfO_2/Al_2O_3 trilayer: 1 or 5 cycles Al_2O_3 followed by 48 or 40 cycles of HfO_2 and 1 or 5 cycles Al_2O_3 (Fig. 2.2c and 2.2f).

A thicker Al_2O_3 layer both as a cap and interlayer resulted in lower D_{it}. The trilayer structure with 5 cycles of Al_2O_3 has D_{it} levels even below the nanolaminates but with reduced Cmax compared to the nanolaminate; the EOT of the trilayer structure with 5 cycles of Al_2O_3 estimated by curve fitting of CV is about 1.9 nm. Compared to the pure HfO_2/SiGe (Fig 2.1a), adding a single monolayer of Al_2O_3 either on top (Fig 2.2a), on the bottom (Fig 2.2b), or both on the top and bottom (Fig 2.2c) had no significant effect on the D_{it}. However, adding 5 cycles of Al_2O_3 either on the bottom (Fig 2.2d), on the top (Fig 2.2e) or both on the top and bottom caused a significant drop in D_{it} but also C_{ox}. C_{ox}/D_{it} values were also improved by adding 5 layers of Al_2O_3 either on the bottom of HfO_2 to the top of HfO_2 consistent with Al_2O_3 acting either as a diffusion barrier or for GeOx reduction.

Effect of Al_2O_3 cap and interlayer on the nanolaminate structures was also evaluated by adding 5 cycles of Al_2O_3 to the top or bottom of 9:1 and 3:1 HfO_2 : Al_2O_3 structures. Figure 2.3 shows the C-V characteristics of nanolaminates with and without Al_2O_3 caps/interlayers. For the 9:1 HfO_2 : Al_2O_3 nanolaminate (Fig. 2.3a), addition of 5 cycles of Al_2O_3 either as an interlayer (Fig. 2.3b) or a cap (Fig 2.3c) resulted in lower D_{it} levels and lower C_{ox}. Comparing the C_{ox}/D_{it} values of the 9:1 HfO_2 : Al_2O_3 nanolaminates (C_{ox}/D_{it} = 0.89 (Fig 2.3a) with 5 cycles Al_2O_3 interlayers or caps, both the Al_2O_3 interlayer and cap showed an improvement (C_{ox}/D_{it} = 0.94 (Fig. 2.3b) and 0.98 (Fig. 2.3c)). The data is consistent with the Al_2O_3 in the nanolaminate lowering D_{it} by reducing diffusion of H_2O (from the ALD process) through the gate oxide or reduction of GeOx at the interface; since the Al_2O_3 at the interface is most efficient in reducing the D_{it}, the GeOx reduction by TMA probably plays a role in the D_{it} reduction.

The role of Al_2O_3 acting as a diffusion barrier or TMA acting as a reducing agent instead of Al_2O_3 directly passivating SiGe is consistent with the study on the 3:1 HfO_2 : Al_2O_3 nanolaminate. For the 3:1 HfO_2 : Al_2O_3 nanolaminate (Fig 2.3d), addition of 5 cycles of Al_2O_3 as a capping layer (Fig 2.3f) only modestly changed the D_{it} and the C_{ox}/D_{it} value only slightly increased (C_{ox}/D_{it} = 0.70 (fig 2.3d) vs 0.72 (fig 2.3f)). However, the device with 5 cycles of Al_2O_3 interlayer (Fig 2.3e) had a very low D_{it} of 1.43×10^{12} $eV^{-1}.cm^{-2}$, which is remarkably low for nanolaminate structures with EOT of less than 2nm. Furthermore, the C_{ox}/D_{it} value of the device (C_{ox}/D_{it} = 1.12 (Fig 2.3e)

was increased by nearly 60% compared to the nanolaminate only device (C_{ox}/D_{it} = 0.70 (Fig 2.3d).

Cross sectional scanning TEM with energy-dispersive x-ray spectroscopy (STEM-EDX) was performed (Fig. 2.4a-d) on a 5 cycles of 9:1 HfO_2: Al_2O_3 nanolaminate sample to determine the thickness of the interlayer between nanolaminate and SiGe. The TEM clearly shows an ~0.8nm thick interlayer of low atomic number between the AlHfOx and the SiGe (Fig 2.4a) meaning the nanolaminate does not directly bond to SiGe. EDS composition analysis (Fig. 2.4b and 2.4c) of the sub 1 nm interlayer shows that it consists of SiO_2 and contains almost no Ge nor Hf. The interlayer could be formed during the ALD or FGA process. Figure 2.4d is an EDX lines can across the interface of 9:1 Hf:Al nanolaminate after FGA. The oxygen signal (green line) in the SiGe region was attributed to the thin substrate having surface oxidation when it was exposed to the air between FIB cross sectioning and TEM analysis. The 5 nm thick nanolaminate layer consisting of HfAlOx was formed on SiOx. The annealing process which creates the pure SiO_2 layer also induces Ge enrichment of the SiGe substrate surface (blue arrow in Fig 2.4d). The Ge/Si atomic weight percent ratio next to the interlayer is 2 times greater than in the bulk SiGe. The data is consistent that in the presence of the NL, the annealing of SiGeOx results in formation of a SiO_2 interlayer and reabsorption of Ge into the SiGe substrate: $Si_xGe_yO_z \rightarrow SiO_2 + Ge$. This is consistent with an ALD cleanup process in which TMA reduces GeOx to Ge and the

Al_2O_3 in the nanolaminate reduces Ge and GeOx diffusion, so Ge is concentrated on the SiGe substrate [47], [48].

2.5 Summary

Al_2O_3/ HfO_2 nanolaminate by thermal ALD has been applied to $Si_{0.7}Ge_{0.3}$(100) surface at 300 ºC. Compared to pure HfO_2, use of the nanolaminate structures effectively reduced the density of interface traps more than 30% at the expense of a small drop in the accumulation capacitance. In addition, at least 3 orders of magnitude lower leakage currents were achieved compared to pure HfO_2 layer. Effects of Al_2O_3 layer as an interlayer and a capping layer were also studied. Comparison of deposition of Al_2O_3 between HfO_2 and SiGe (interlayer) vs on top of HfO_2 (cap) shows the lower D_{it} was achieved when the Al_2O_3 is in the interlayer instead of the capping layer. The data is consistent with Al_2O_3 acting as a diffusion barrier to Ge diffusion for the substrate or TMA clean-up effect reducing Ge oxides. While the nanolaminates do not have a distinct Al_2O_3 layer, the data is consistent with the incorporation of Al into HfO_2 improving the diffusion barrier properties thereby lowering the D_{it}. Cross sectional scanning TEM showed formation of SiOx interlayer between the AlHfOx and the SiGe. EDX spectra of the interlayer revealed that the SiOx layer contains almost no Ge showing the nanolaminate effectively prevents interfacial GeOx formation.

2.6 Acknowledgment

The authors would like to thank Larry Grissom, Ivan Harris, and Sean Park of UCSD Calit2 for their assistance with ALD and metal deposition at the UCSD Nano3 cleanroom facility. SiGe wafers were provided by Applied Materials Inc. This work is partially supported by a gift from Applied Materials Inc and Taiwan Semiconductor Manufacturing Co. In addition, this work was performed in part at the San Diego Nanotechnology Infrastructure (SDNI) of UCSD, a member of the National Nanotechnology Coordinated Infra-structure (NNCI), which is supported by the National Science Foundation (Grant ECCS-1542148).

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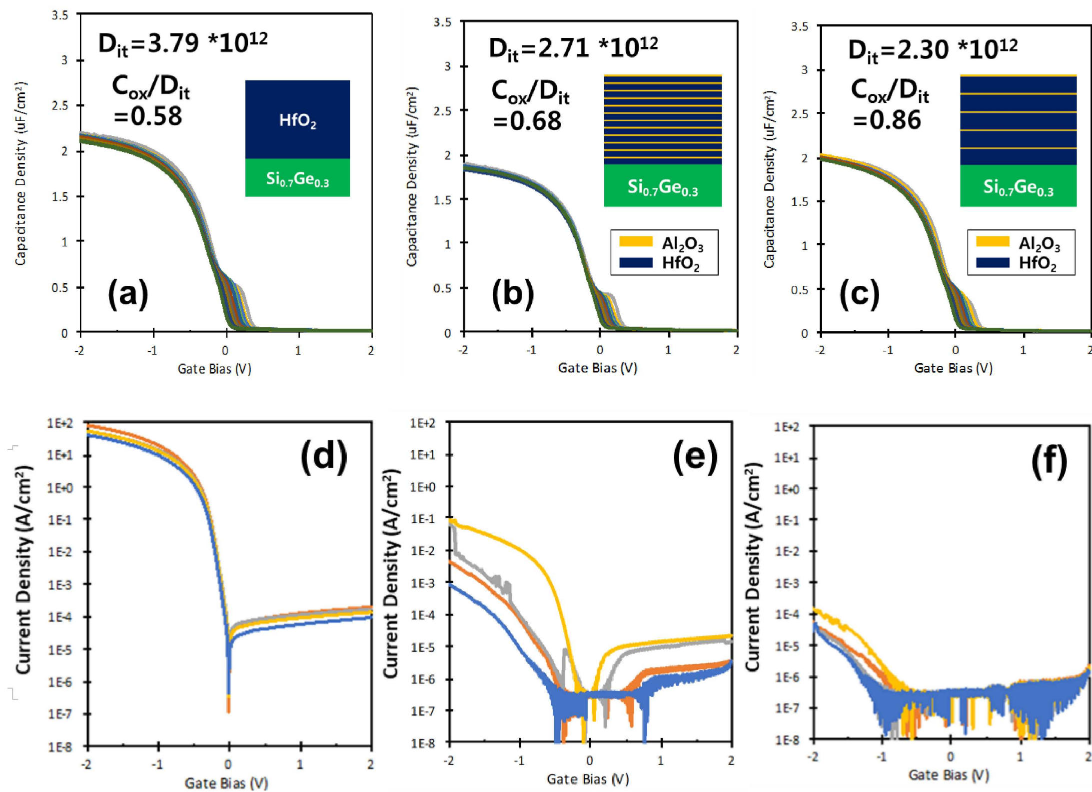


Figure 2.1 Capacitance – voltage characteristics for high-k/SiGe MOSCAPs with HfCl4 precursor: (a) 50 cycles of pure HfO_2 ALD (b) Nanolaminate with 12 cycles of 3:1 HfO_2:Al_2O_3; (c) Nanolaminate with 5 cycles of 9:1 HfO_2:Al_2O_3. D_{it} values in eV-1.cm-2 were calculated by the conductance method. Current – voltage spectroscopy for high-k/SiGe MOSCAPs with HfCl4 precursor: (d) 50 cycles of pure HfO_2 ALD (e) Nanolaminate with 12 cycles of 3:1 HfO_2:Al_2O_3; (f) Nanolaminate with 5 cycles of 9:1 HfO_2:Al_2O_3

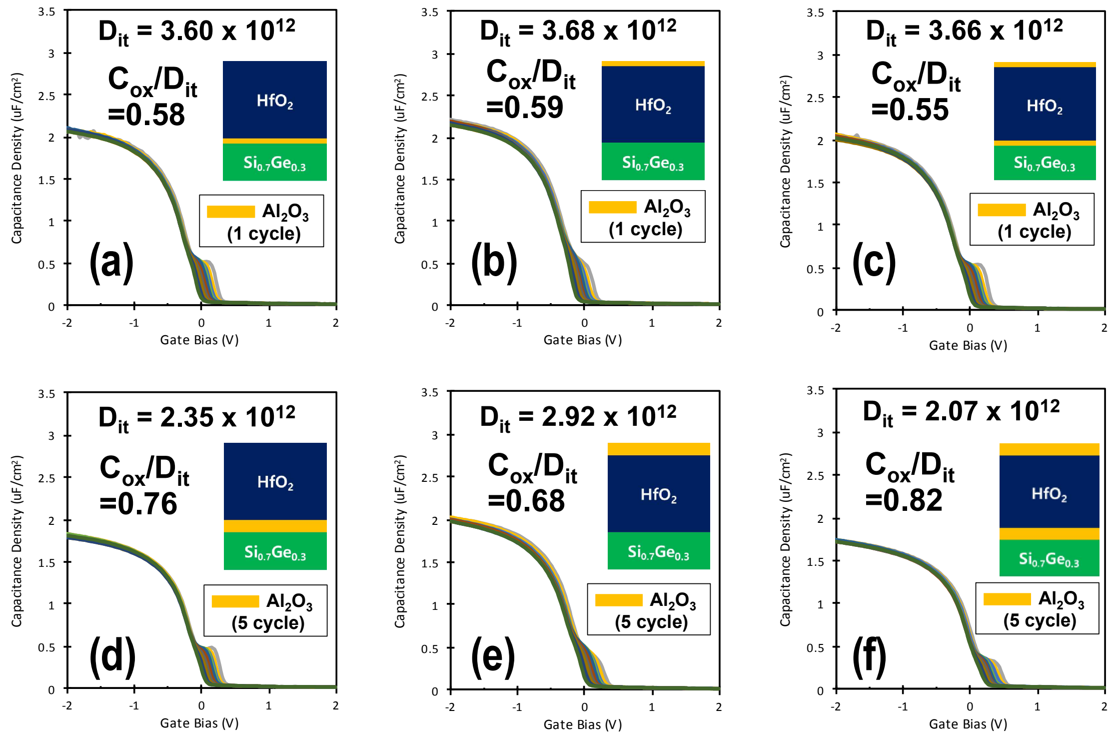


Figure 2.2 Capacitance – voltage characteristics for bilayer and trilayer oxides on deposited SiGe using HfCl4 precursor: (a) Bilayer with 1 cycle of Al_2O_3 followed by 49 cycles of HfO_2; (b) Bilayer with 49 cycles of HfO_2 followed by 1 cycle of Al_2O_3; (c) Trilayer with 1 cycle of Al_2O_3 followed by 49 cycles of HfO_2 and 1 cycle of Al_2O_3; (d) Bilayer with 5 cycle of Al_2O_3 followed by 45 cycles of HfO_2; (e) Bilayer with 45 cycles of HfO_2 followed by 5 cycles of Al_2O_3; (f) Trilayer with 5 cycle of Al_2O_3 followed by 40 cycles of HfO_2 and 5 cycle of Al_2O_3. All samples were passivated by wet sulfur clean prior to ALD. D_{it} values in $eV^{-1}.cm^{-2}$ were calculated by conductance method.

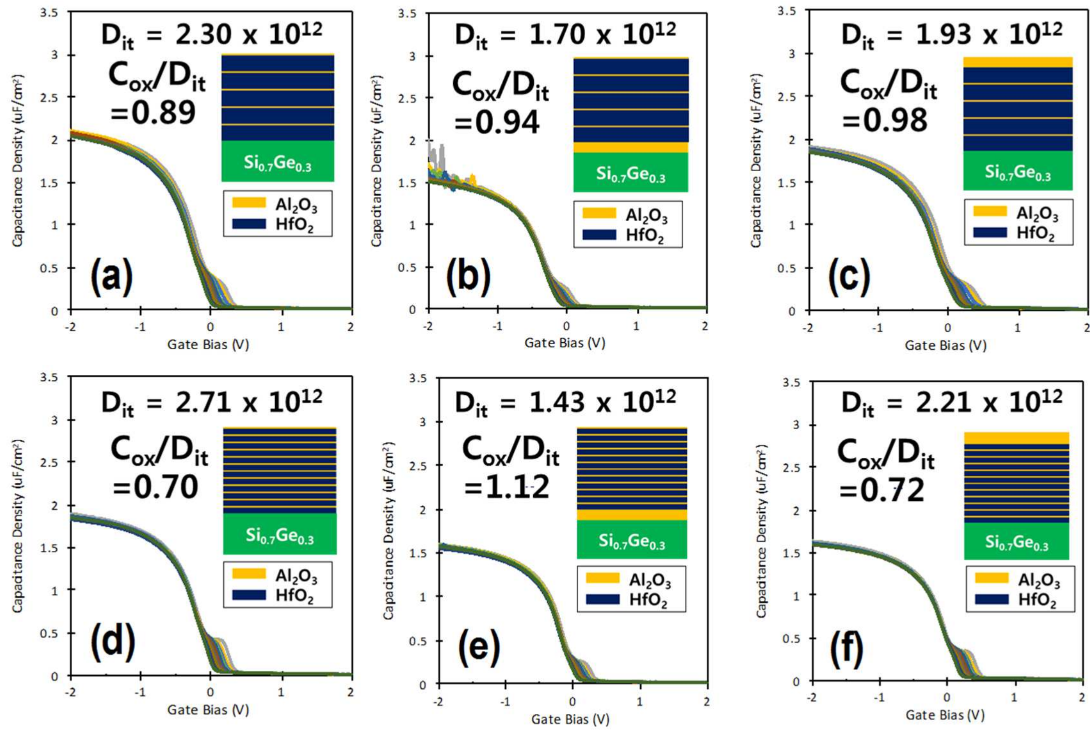
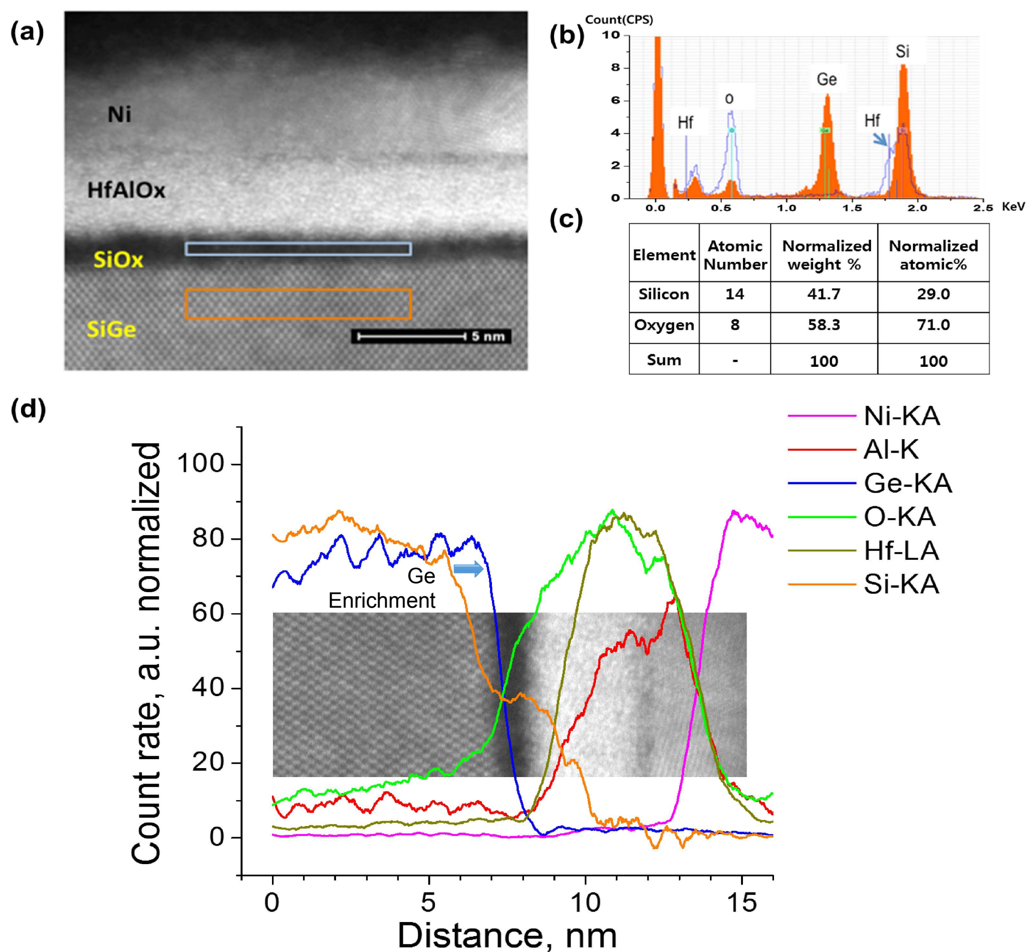


Figure 2.3 MOSCAPs Capacitance – voltage characteristics for Nanolamnate with Al_2O_3 Caps and Interlayers with $HfCl_4$ precursor: (a) Nanolaminate with 5 cycles of 9:1 HfO_2:Al_2O_3; (b) 5 cycles of Al_2O_3 interlayer followed by nanolaminate with 5 cycles of 9:1 HfO_2:Al_2O_3 followed by (IL); (c) Nanolaminate with 5 cycles of 9:1 HfO_2:Al_2O_3 followed by 5 cycles of Al_2O_3 cap; (d) Nanolaminate with 12 cycles of 3:1 HfO_2:Al_2O_3; (e) 5 cycles of Al_2O_3 interlayer followed by nanolaminate with 12 cycles of 3:1 HfO_2:Al_2O_3 plus 5 cycles of Al2O3 interlayer (IL); (f) Nanolaminate with 12 cycles of 3:1 HfO_2:Al_2O_3 followed by 5 cycles of Al_2O_3 cap;. D_{it} values in $eV^{-1}.cm^{-2}$ were calculated by conductance method.



Element	Atomic Number	Normalized weight %	Normalized atomic%
Silicon	14	41.7	29.0
Oxygen	8	58.3	71.0
Sum	-	100	100

Figure 2.4 STEM-EDX of 5 cycles of 9:1 HfO_2: Al_2O_3 nanolaminate (a) STEM-EDX characterization of ~10% Al_2O_3 and ~90% HfO_2/ $Si_{0.7}Ge_{0.3}$(001). Blue box shows a region of interlayer for EDX analysis revealing a Ge-free SiOx interlayer. The orange box is a control region in the SiGe. (b) The EDX spectra of the interlayer is in blue while the spectra on the SiGe control region is in orange. Note the absence of Ge in the interlayer. (c) EDX analysis of SiOx layer region (blue box). Note that the oxide composition is SiO_2. (d) EDX line scan across the interface of 9:1 Hf:Al nanolaminate.

Chapter 3. Mechanism of Low Temperature ALD of Al_2O_3 on 2D materials

3.1 Abstract

In this chapter, mechanism of low temperature ALD for graphene and MoS_2 surface and the optimization process is introduced. Al_2O_3 and Al_2O_3/HfO_2 bilayer gate stacks were directly deposited on the surface of 2D materials via low temperature ALD/CVD of Al_2O_3 and high temperature ALD of HfO_2 without any surface functionalization. The process is self-nucleating even on inert surfaces because a chemical vapor deposition (CVD) component was intentionally produced in the Al_2O_3 deposition by controlling the purge time between TMA and H_2O precursor pulses at 50 ^oC. The CVD growth component induces formation of sub-1 nm AlOx particles (nanofog) on the surface, providing uniform nucleation centers. The ALD process is consistent with the generation of sub-1 nm gas phase particles which stick to all surfaces and is thus denoted as nanofog ALD. To prove the ALD/CVD Al_2O_3 nucleation layer has the conformality of a self-limiting process, the nanofog was deposited on a high aspect ratio $Si_3N_4/SiO_2/Si$ pattern surface; conformality of >90% was observed for a sub 2nm film consistent with a self-limiting process.

3.2 Introduction

2D materials such as graphene, MoS_2 and WSe_2 have attracted attention as future electronic devices due to their excellent electronic properties [15], [49]–[57]. To switch on and off electric transistors, a few nanometer thick and defect-free gate oxide layers are integrated into the device fabrication for electrostatic gate control. However, due to the inert nature of the 2D material surfaces, the dielectric layers deposited by the conventional atomic layer deposition (ALD) processes preferentially nucleate at the defect sites or step edges. Such non-uniform oxides result in large leakage currents in the dielectrics of devices, consistent with the poor gate control.[58]–[60] Therefore, for successful integration of the 2D material devices, uniform and insulating gate oxides should be prepared. In order to deposit insulating gate oxides on 2D materials, various functionalization techniques have been studied such as surface treatment by using chemical solutions or O_3(g), deposition of reactive metal or polymer-based seeding layers.[59], [61]–[66] However, these chemical functionalization methods frequently induce damage to 2D materials, change the electronic properties of 2D materials, or the seeding techniques require complicated vacuum processes and thick dielectric layers. Therefore, a more facile low defect gate oxide deposition method is required for successful fabrication of 2D material-based devices.

In this work, aluminum oxide (Al_2O_3) was deposited on 2D material surfaces by low temperature ALD without any seeding layers or surface treatments. By controlling precursor pulse and purge times, a chemical vapor deposition (CVD) component was intentionally induced to form nucleation sites on the surface. The CVD growth

component generated subnanometer AlOx particles on the 2D material surfaces forming uniformly deposited pinhole-free dielectrics; the substrate independent deposition is consistent with a gas phase formation of the subnanometer AlOx particles and thus is denoted as "nanofog". As a means to demonstrate the self-limiting process of the ALD/CVD Al_2O_3 nucleation layer, the 20 cycles of nanofog ALD was deposited on a high aspect ratio $Si_3N_4/SiO_2/Si$ fin surface; 2nm thick film with conformality (step coverage) of >90% was achieved.

3.3 Experimental Details

Bulk MoS_2 and highly oriented pyrolytic graphite (HOPG) samples (SPI supplies) were mechanically exfoliated by an adhesive tape. The samples were transferred into a commercial ALD reactor (Beneq TFS 200 ALD system) which has a hot wall, crossflow reaction chamber. The base pressure of the reaction chamber was 1 mTorr. For Al_2O_3 ALD, TMA and H_2O were employed as precursor gases. The Ar carrier gas was continuously flowed at 300 sccm (standard cubic centimeter). 50 cycles of ALD were deposited and each cycle consisted of a sequence of a TMA pulse, an Ar purge, a H_2O pulse, and an Ar purge in the temperature range of 50 ^oC to 200 ^oC. In order to study the growth rate and the conformality of the Al_2O_3 film, 13 cycles and 50 cycles of ALD were deposited at 50 ^oC on a hydrogenated silicon oxycarbide (H:SiOC) substrate and 20 cycles of the ALD were prepared on a high aspect ratio patterned

sample with $Si_3N_4/SiO_2/Si$ fins; both samples were supplied by Applied Materials. Prior to ALD, the hydrogenated silicon oxycarbide (H:SiOC) and the high aspect ratio patterned samples were degreased by dipping sequentially in acetone, isopropyl alcohol, and DI water for 30 s followed by high purity N_2 drying. The cross section of each samples was investigated by TEM (Tunneling Electron Microscopy).

3.4 Results and discussion

3.4.1 Nucleation of Al_2O_3 on 2D materials

The effects of ALD temperature on nucleation of Al_2O_3 on HOPG were investigated. AFM images of Al_2O_3 ALD on HOPG using 50 cycles of ALD dielectrics in the temperature range of 50 ~ 200 ^{o}C are shown in Figure 3.1. For the samples in Fig. 3.1(a), (b), and (c), a 600 ms TMA and a 50 ms H_2O pulses were used with a 500 ms Ar purge time between the two precursor pulses. The nucleation of Al_2O_3 on HOPG was strongly dependent on the sample temperature. Typically, Al_2O_3 ALD is performed above 150 ^{o}C to reduce fixed charges in the oxide and interface defect density.[67] When the ALD was performed on HOPG at 200 ^{o}C and 150 ^{o}C (Fig. 3.1(a) and (b)), Al_2O_3 was only deposited at the step edges of the HOPG and not on the terraces because of a lack of dangling bonds on the HOPG surface. However, when the ALD temperature

was decreased to 50 ^{o}C (Fig. 3.1(c)), the Al_2O_3 film was continuously grown on both the step edges and the terrace without formation of any visible pinholes. Round Al_2O_3 particles were observed across the entire surfaces at this temperature.

The height and diameter of the particles (Fig 3.1c) was about 2 ± 0.4 nm and 20 ± 9.5 nm as quantified by line profiles in multiple AFM images. These particles are attributed to a CVD growth component. The short purge times for this study could induce the CVD reaction because of excess ALD precursors remaining in the gas distribution system. Under these conditions, TMA and H_2O can react with each other before reaching the substrate, and gas phase nucleation could occur to generate AlOx nuclei. It is hypothesized that the nuclei can be uniformly deposited on the surface by a reversible adsorption – desorption process due to the surface aluminum hydroxyl group (Al-O-H) of the nuclei. Once the surface covered with the nuclei, they eventually grow together and form a continuous Al_2O_3 film unlike the preferential nucleation in the case of Fig. 3.1(a) and 3.1(b). The asymmetric shape of the particles in Fig. 3.1(c) is consistent with agglomeration of weak bound, mobile sub 2nm nuclei on the surface.

This proposed reversible adsorption–desorption nucleation mechanism would suggest that the nucleation behavior should depend on the substrate in the temperature range where the conformal AlOx nuclei deposition the surface can occur. To validate this hypothesis, identical 50 cycles of Al_2O_3 were deposited on a HOPG and a bulk MoS_2 substrates at different temperatures. Figure 3.2 shows the AFM images of the

surfaces of two different substrates After ALD. As shown in Fig. 3.2(a) and 3.2(d), similar Al_2O_3 nuclei were observed on the HOPG and the MoS_2 surfaces at 50 ^oC. However, at 80 ^oC, while Al_2O_3 was nucleated preferentially on the step edges and the defect sites on HOPG surface (Fig. 3.2(b)), a continuous film was grown only on the MoS_2 substrate (Fig. 3.2(e)). For an ALD temperature of 100°C, Al_2O_3 film was discontinuous on both substrates (Figs. 3.2(c) and 3.2(f)). The different cut-off ALD temperatures on two substrates can be explained by the greater polarizability of the MoS_2 substrate compared to the HOPG substrate. The adsorption energy is expected to be higher with stronger surface polarizability providing strong dipolar interaction between the 2D semiconductors and the nuclei.[24] Graphene surface has weak polarization[60]; therefore, a lower ALD temperature is required for the nuclei to be deposited uniformly on a HOPG surface compared to the MoS_2 surface. There are two simple mechanisms to explain the formation of the Al_2O_3 particle layers on inert surfaces. (a) The TMA and the H_2O physisorb on the inert surfaces and form particles on the surface via reaction; (b) The TMA and the H_2O react in the gas phase and the particles reversibly deposit on the surface. Both processes are expected to be sensitive to pulse and purge times. The cutoff temperature for ALD being close to 100C is inconsistent with the physisorption mechanism of a purely surface based reaction; therefore, the temperature dependence is most consistent with gas phase nucleation in the ALD chamber[68]; therefore the technique is denoted as “nanofog” ALD.

Figure 3.3 (a) – (c) shows the AFM images of 50 cycles of Al_2O_3 ALD at 50 °C with different pulse lengths of TMA and H_2O with a fixed purge time of 500 ms. For the sample with 200 ms of TMA pulse and 50 ms of H_2O (Fig. 3.3a), Al_2O_3 was mainly deposited on the step edges. Although some Al_2O_3 was nucleated on the terraces, it was discontinuous and many visible pinholes were observed. The number densities of the Al_2O_3 particles (number of particles per 4 μm^2 image area) with the three different ALD conditions are shown in Table I. For this reaction condition, (200 ms of TMA pulse and 50 ms of H_2O), the density of the Al_2O_3 particles (15/ μm^2) was significantly lower than the other two conditions (Fig. 3.3b, 3.3c). The observation of a low density Al_2O_3 particles precludes formation of a continuous Al_2O_3 is consistent with the critical role of the particles in conformal ALD growth on HOPG.

When the TMA pulse time was increased to 600 ms while fixing the H_2O pulse length (Fig. 3.3b), the density of the Al_2O_3 particles was markedly increased (123/ μm^2) and continuous Al_2O_3 films were deposited on both terraces and step edges without pinholes. AFM line traces show that the particles are 2 ± 0.6 nm in diameter (Fig 3.3e).

When H_2O pulse was increased to 150 ms with a fixed TMA pulse time of 200 ms (Fig. 3.3c), similar morphology as the growth with a long TMA pulse (Fig. 3.3b) was observed. The Al_2O_3 film was continuous with high density of Al_2O_3 particles (44/ μm^2). AFM lines traces (Fig. 3.3f) show the particles increased in size to 4 ± 0.7 nm. This indicates that the Al_2O_3 particles which were induced by CVD component can be

controlled by TMA and H_2O pulse times consistent with both the island formation mechanism and the gas phase formation mechanism.

The size of the ALD nuclei can be controlled by the ALD parameters enabling sub-1 nm RMS roughness oxides. Figure 3.4(a) and 3.4(b) show the same 50 cycles of Al_2O_3 ALD on a HOPG and a bulk MoS_2 substrate with a 3sec purge. Compared to Fig. 3.2(a) and Fig 3.2(d), the surface became significantly smoother with smaller AlOx particles by increasing the purge time. This indicates that surface roughness can be controlled by purge times at this temperature.

Cross sectional TEM study was performed to investigate the conformality and the growth rate of Al_2O_3 ALD at 50C. Normally, a self-limiting process is documented in ALD by measuring the growth rate per cycle versus purge time. However, for the ALD/CVD process, this is not possible because changing the purge time changes the particle size as shown in Fig 3.3. Instead, conformal deposition in a high aspect ratio sample with features below 50 nm was employed. Figure 3.5(a) and 3.5(b) shows the TEM image of 50 cycles and 13 cycles of Al_2O_3 ALD on hydrogenated silicon oxycarbide (H:SiOC) substrates using a 200 ms of TMA pulse and a 50 ms of H_2O with 10s of Ar purges between the pulses. As shown in Figs. 3.5(a) and 3.5(b), the Al_2O_3 films were uniformly deposited on the substrate. Average thickness of the 50 cycles and 13 cycles Al_2O_3 layers was 6.6 nm and 2.0 nm, therefore, the growth rates were 1.32 Å/cycle and 1.53 Å/cycle respectively. This growth rate is slightly high growth rates

compared to typical "pure" ALD growth rates (~1.1 Å/cycle) at high temperature and is attributed to the CVD component of the process.[69],[70] Fig. 3.5(c) shows 20 cycles of Al_2O_3 ALD with the identical recipe as in Fig. 3.5(a), 3.5(b) on high aspect ratio $Si_3N_4/SiO_2/Si$ fin structures (250 nm height × 50 nm width, aspect ratio of 5:1) . Conformality was quantity from the film thickness at the top of the sample compared to the bottom of the trench. Conformal 2nm thick Al_2O_3 layer was deposited on the patterned structures without any visible pinholes. The growth rate was about 1 Å/cycle which is slightly lower than the ALD on a H:SiOC substrate due to the different material surfaces and structures. The conformality was determined to be 91% This result indicates ALD/CVD reaction was self-limiting consistent with the model of reversible adsorption/desorption of sub 1nm Al_2O_3 particles formed in the gas phase. Similar conformality was also observed for nanofog deposition on 13 nm tall MoS_2 nanoribbons (Alessandri et al, IEEE Trans Elect Dev. 64(12), p 5217 (2017)) consistent with conformality on a sub 10 nm scale.

3.5 Summary

In this study, deposition of high quality Al_2O_3 and HfO_2/Al_2O_3 films on 2D materials using low temperature ALD/CVD was demonstrated without organic seeding layers or chemical treatments. During ALD/CVD, AlO_x particles of below 1 nm diameter were formed on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}(001)$ consistent with a gas phase

reaction of the ALD precursors to form sub 1nm particles (denoted as nanofog) which reversible adsorb onto the substrates. The particles provided nucleation centers for further ALD on the inert 2D material surfaces. To document the nanofog process was conformal even on inert surfaces, a high aspect ratio $Si_3N_4/SiO_2/Si$ structure was coated with sub 2nm thick nanofog Al_2O_3 and was found to be 91% conformal.

3.6 Acknowedgments

This work is supported in part by the National Science Foundation Grant DMR 1207213, by the Center for Low Energy Systems Technology (LEAST), a STARnet Semiconductor Research Corporation (SRC) program sponsored by MARCO and DARPA, and by the SRC Nanoelectronic Research initiated through the South West Academy of Nanoelecronics (SWAN). Experiments were performed in the UCSD Nano3 facility supported by the NNCI.

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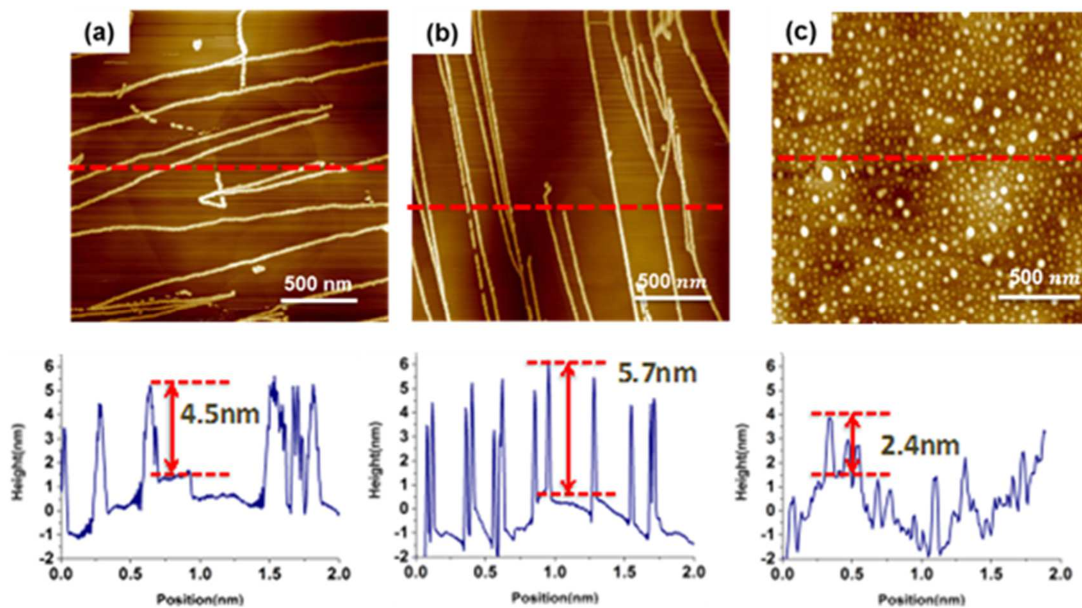

Figure 3.1 AFM images of 50 cycles of Al_2O_3 films on HOPG with different ALD temperatures. (a) 200 ^oC; the ridges along the step edges are 4.5 nm tall; (b) 150 ^oC; the ridges along the step edges are 5.7 nm tall; (c) 50 ^oC; the height and diameter of the particles are 2 ± 0.4 nm and 20 ± 9.5. Each ALD cycle consisted of a 600 ms TMA pulse, a 500 ms Ar purge, a 50 ms H_2O pulse, and a 500 ms Ar purge.

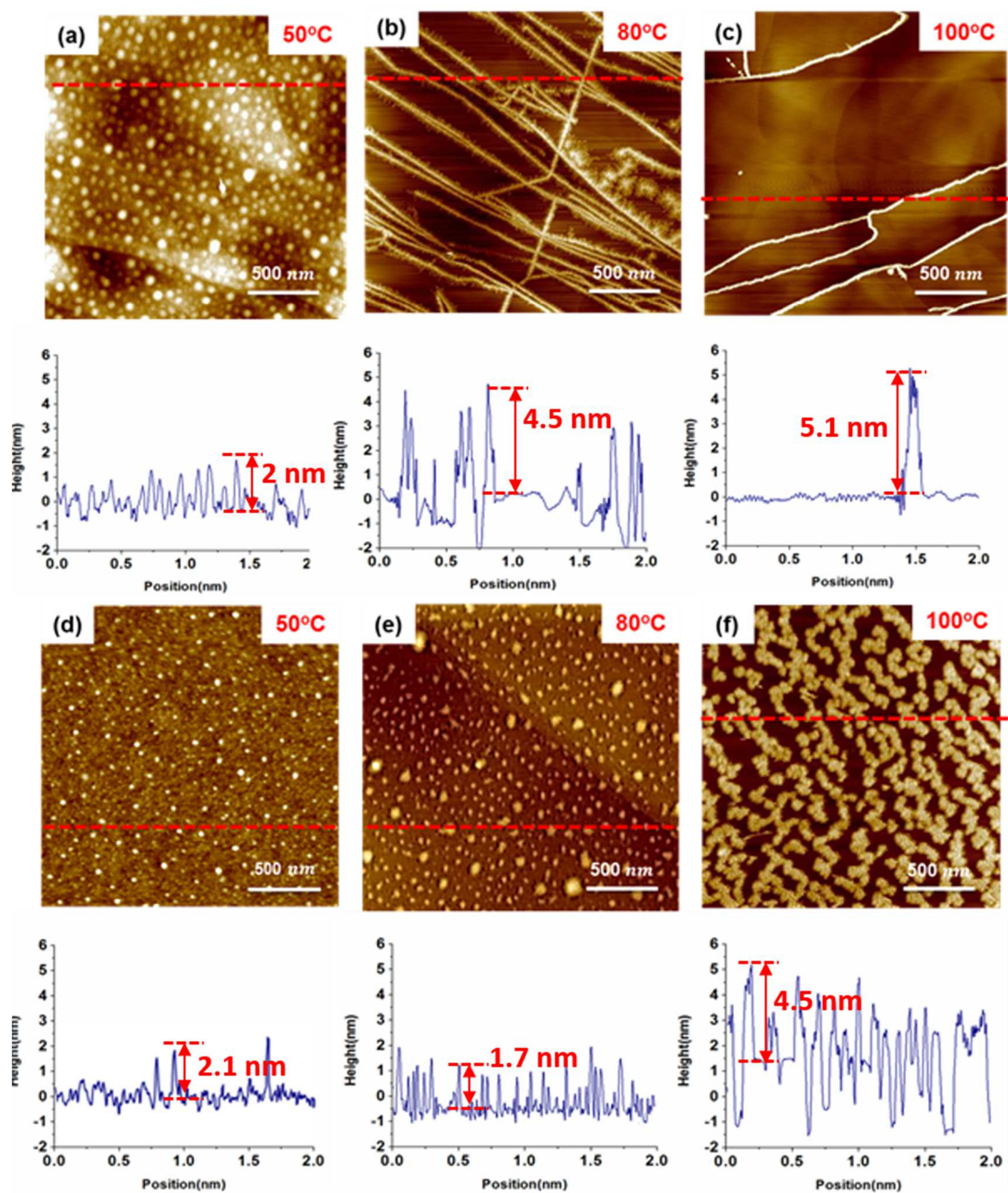

Figure 3.2 AFM images and line profiles of 50 cycles of Al_2O_3 films on HOPG vs MoS_2. (a) HOPG 50 °C, (b) HOPG 80 °C, (c) HOPG 100 °C, (d) bulk MoS_2 50 °C, (e) bulk MoS_2 80 °C, (f) bulk MoS_2 100 °C. The size of the images is 2 x 2 um^2. and purge times as in Figure 1 samples were employed.

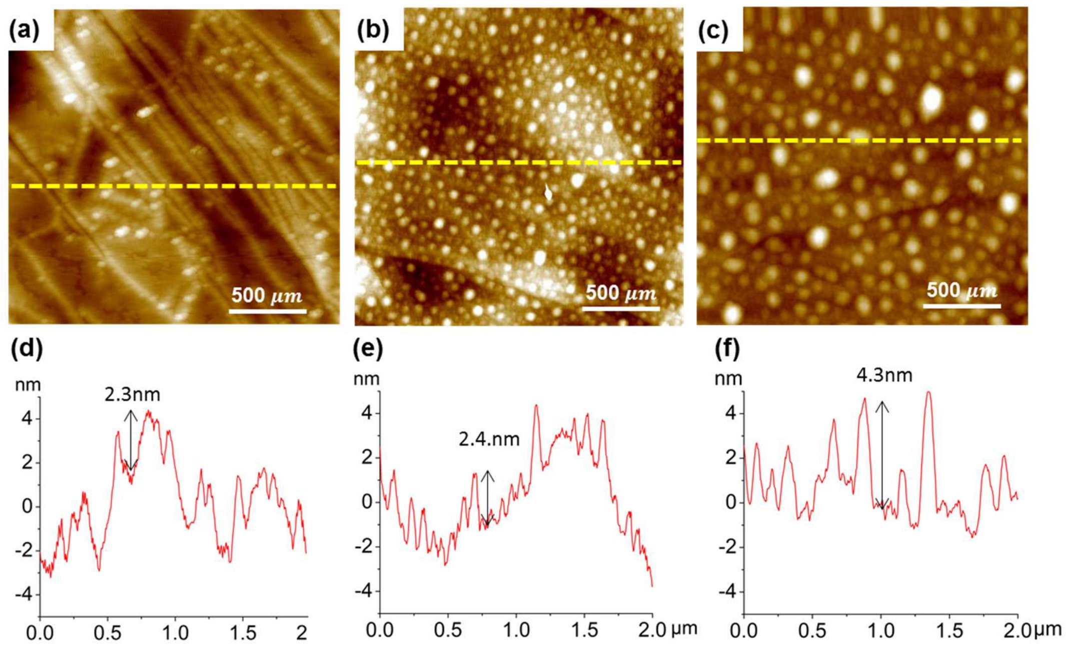

Figure 3.3 AFM images of Al_2O_3 film (50cycles) on HOPG (a) 200ms of TMA and 50 ms of H_2O. (b) 600ms of TMA of 50ms of H_2O and (c) 600ms of TMA and 150 ms of H_2O. (d), (e), and (f) are AFM height profiles along the yellow lines in the Fig. 3.3 (a), (b) and (c) respectively. For the ALD with short pulses (a/d), few condensation nuclei are observed, and the ALD primary occurs on the step edges. For the two growths with longer TMA pulses (b/e and c/f), white condensation nuclei are distributed across the terraces, and ALD is observed on the terraces.

Table 3.1 Number density of Al_2O_3 particles with different ALD conditions (Particle numbers / 4 μm^2)

200ms of TMA &50ms of H_2O	600ms of TMA &50ms of H_2O	200ms of TMA &150ms of H_2O
59	692	176

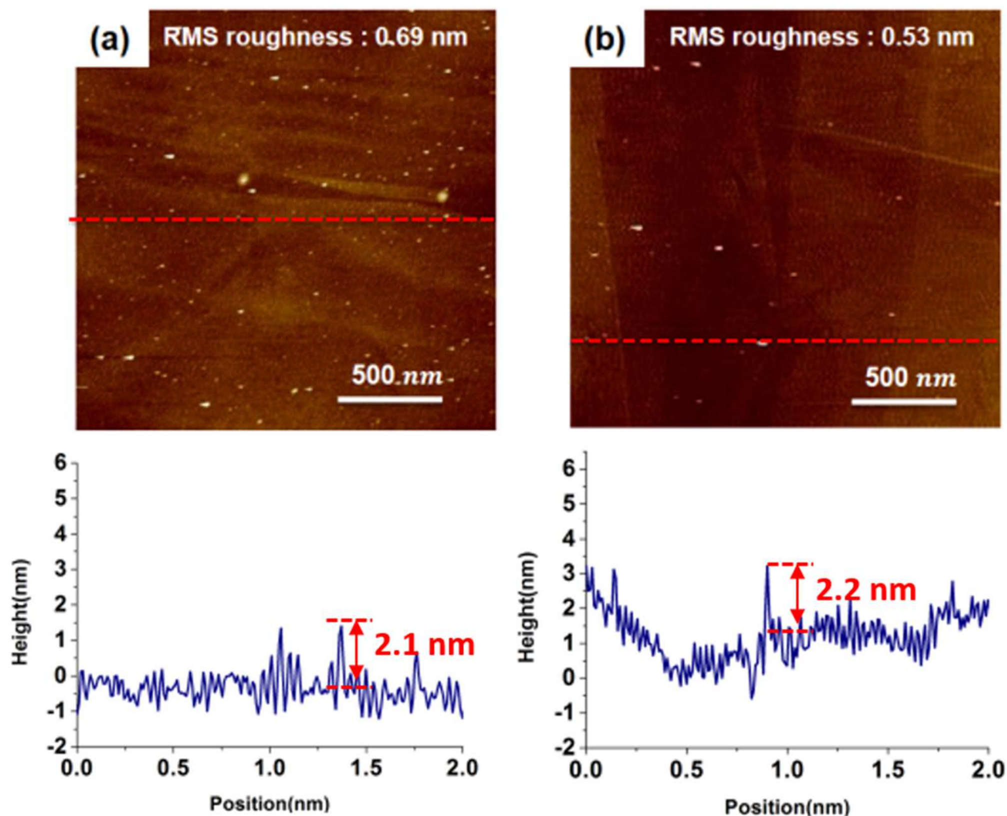

Figure 3.4 AFM images and line profiles of 50 cycles of Al_2O_3 films with long (3sec) purge times on (a) HOPG and (b) bulk MoS_2. The size of the images is 2 x 2 um^2. The line profiles were taken along red lines in each AFM images. The 50 ALD cycles consisted of a 600 ms TMA pulse, a 3s Ar purge, a 50 ms H_2O pulse, and a 3s Ar purge at 50 ^oC. The height and diameter of the largest AlOx particles was 2.1 ± 0.2 nm and 2.2 ± 0.3 nm but note that the surface has a roughness below 1 nm consistent with most particles being sub 1nm diameter.

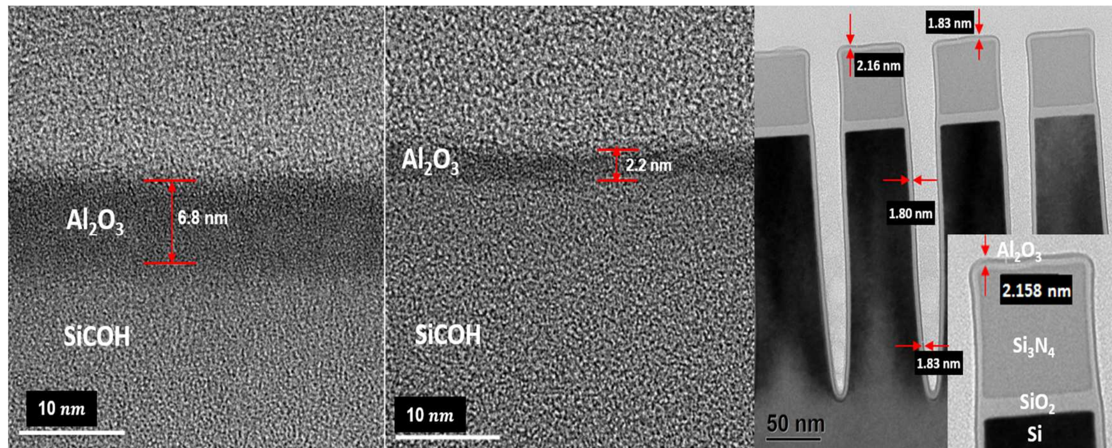

Figure 3.5 (a), (b) TEM images of 50 cycles and 13 cycles of Al_2O_3 ALD on hydrogenated silicon oxycarbide (H:SiOC) substrates. (c) TEM image of 20 cycles of Al_2O_3 ALD on high aspect ratio $Si_3N_4/SiO_2/Si$ fin structures. The black outmost layer is Al_2O_3. The ALD cycles consisted of a 200 ms TMA pulse, a 10s Ar purge, a 50 ms H2O pulse, and a 10s Ar purge at 50 ^oC.

Chapter 4. Electrical Properties of Low Temperature ALD oxide on 2D materials

4.1 Abstract

MoS_2 and HOPG (highly oriented pyrolytic graphite) metal oxide semiconductor capacitors (MOSCAPs) were fabricated with single layer Al_2O_3 ALD at 50 ºC and with the bilayer Al_2O_3/HfO_2 stacks having C_{max} of ~ 1.1 μF/cm^2 and 2.2 μF/cm^2 respectively. In addition, Pd/Ti/TiN gates were used to increase C_{max} by scavenging oxygen from the oxide layer which demonstrated C_{max} of ~2.7 μF/cm^2. This is the highest reported C_{max} and C_{max}/Leakage of any top gated 2D semiconductor MOSCAP or MOSFET. The gate oxide prepared on a MoS_2 substrate results in more than an 80 % reduction in D_{it} compared to a $Si_{0.7}Ge_{0.3}$(001) substrate. This is attributed to a Van der Waals interaction between the oxide layer and MoS_2 surface instead of a covalent bonding allowing gate oxide deposition without the generation of dangling bonds.

4.2 Introduction

To obtain higher capacitance and lower equivalent oxide thickness (EOT) gate stacks, Al_2O_3/HfO_2 bilayer gate oxides were deposited on the 2D materials with both non-reactive and reactive gate metals. To study the surface morphology, atomic force microscopy (AFM) was employed. The electrical properties of the oxides were

evaluated by measurements of capacitance-voltage and leakage current of metal oxide semiconductor capacitor (MOSCAP). The density of interface states (D_{it}) for MoS_2 MOSCAPs was approximately one order of magnitude lower compared to the D_{it} for $Si_{0.7}Ge_{0.3}$(001) MOSCAPs. This is attributed to a Van der Waals interaction between the oxide layer and MoS_2 surface instead of a covalent bonding allowing gate oxide deposition without generation of dangling bonds.

4.3 Experimental Details

MoS_2, HOPG and p-type $Si_{0.7}Ge_{0.3}$(001) MOSCAPs were fabricated to analyze the electrical properties of the oxide. $Si_{0.7}Ge_{0.3}$(001) samples were cleaned by dipping sequentially in acetone, isopropyl alcohol, and DI water for 30 s. The native oxide of $Si_{0.7}Ge_{0.3}$(001) was removed by cyclic HF cleaning by a 2% HF solution and DI water at 25 ^{o}C for 1 min in each solution for 2.5 cycles and finished with 2% HF clean. [71] After 50 cycles of Al_2O_3 ALD process at 50 ^{o}C, 30 nm thick Ni top contacts were deposited on top of the oxide using thermal evaporation. A stainless-steel shadow mask was used to prepare the circular Ni contact patterns to avoid possible contamination from lithography and lift-off techniques. The diameter of contacts for MoS_2 and HOPG deviceswas 50 μm and 150 μm for $Si_{0.7}Ge_{0.3}$(001) devices.

In addition, to achieve high capacitance, Al_2O_3/HfO_2 bilayer gate oxide stacks were deposited on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}$(001) substrates. 7 or 10 cycles of Al_2O_3 were deposited at 50 ^oC as a seeding layer. Afterward, 40 cycles of HfO_2 were grown on top of the Al_2O_3 layer at 300 ^oC using hafnium tetrachloride ($HfCl_4$) and H_2O as precursors. Note that between the Al_2O_3 and HfO_2 growth, the samples were stored in the load lock to avoid background oxidant exposure at high temperature. For HfO_2 ALD, each cycle consisted of a $HfCl_4$ and a H_2O pulse with Ar purges after each precursor dose. AFM was used in non-contact mode to characterize the surface topography after the ALD deposition.

Pd/Ti/TiN top contacts were also deposited on ALD dielectric to study the oxygen scavenging effects on the deposited oxides. The Pd/Ti/TiN contacts were deposited by DC sputtering and the thicknesses of Pd/Ti/TiN layers were 30 nm, 30 nm and 5 nm respectively. The sizes of Pd/Ti/TiN were identical as Ni contacts. Using Agilent B1500A semiconductor Device Analyzer, the capacitance of the oxides was measured as a function of voltage in the frequency range of 2 kHz to 1 MHz at room temperature. Leakage current densities were also obtained in the range of -2V to 2V. The conductance method was applied to extract density of interface states (D_{it}) of MoS_2 and $Si_{0.7}Ge_{0.3}$ MOSCAPs.[44]

4.4 Results and Discussion

Capacitance-voltage (C-V) and leakage current-voltage (I-V) of MOSCAPs with 50 cycles of Al_2O_3 at 50 ^oC were measured to evaluate the electrical properties of the oxide layer. Figure 5(a), (b). and (c) show the capacitance-voltage curves of MoS_2, HOPG and $Si_{0.7}Ge_{0.3}$(001) MOSCAPs. In case of the HOPG in Fig. 5(b), the capacitance of the oxide was not dependent on the voltage. For a single layer of graphene, capacitance can be modulated near the Fermi level due to the linear dispersion of the density of states; conversely, due to the high charge carrier density of HOPG near the Fermi level, the modulation cannot be observed. MoS_2 (Fig. 5(a)) and $Si_{0.7}Ge_{0.3}$(001) (Fig. 5(c)) samples showed n-type and p-type doping of the substrates. The negative flat band shift of MoS_2 sample was attributed to the charged defects on the surface, and the capacitance frequency dispersion in the accumulation region was due to the high series resistance of the bulk substrate. Note that the C_{max} of the three different samples was nearly identical (~1.1 μF/cm^2) which is consistent with the reported values for 50 cycles of Al_2O_3. This indicates that growth rate of the oxide on the three substrates was nearly identical without an induction period.

The D_{it} was evaluated via the conductance method from the G-V data which is shown in Fig. 5(e) and (f); note the conductance method provides the peak of the D_{it} distribution. As shown in Fig. 5(a) and (c), D_{it} of MoS_2 MOSCAPs (9.84×10^{11} eV^{-1}cm^{-2}) is approximately one order of magnitude lower compared to the D_{it} of $Si_{0.7}Ge_{0.3}$(001)

MOSCAPs (6.89×10^{12} $eV^{-1}cm^{-2}$). This is attributed to a Van der Waals bonding between the oxide layer and the MoS_2 surface instead of a covalent bonding between the oxide layer and the $Si_{0.7}Ge_{0.3}$(001) surface. Fig. 5(d) shows the leakage current of the three samples. The leakage current densities of MoS_2, HOPG and $Si_{0.7}Ge_{0.3}$(001) samples were 2.2×10^{-5} A/cm^2, 3.01×10^{-5} A/cm^2 and 2.2×10^{-6} A/cm^2 at -1 V. The slightly lower leakage of the $Si_{0.7}Ge_{0.3}$ MOSCAPs is consistent with dangling bonds on the surface providing better nucleation of Al_2O_3. The low leakage current of the HOPG and MoS_2 devices indicates that the deposited oxides are uniform and pinhole free on the 2D materials.

To obtain higher capacitance with lower EOT, HfO_2/Al_2O_3 bilayer gate stacks were prepared using a two-step ALD method. First, 7 cycles of Al_2O_3 were deposited at 50 ^oC as a seed layer. Afterwards, the ALD reactor temperature was increased to 300 ^oC and, using $HfCl_4$ and H_2O as precursors, 40 cycles of HfO_2 ALD were deposited on top of the Al_2O_3. Note that the samples were stored in the load lock during the ALD reactor temperature change to avoid substrate damage. For comparison, identical oxides were deposited on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}$(001). The identical device fabrication process that was used for the pure Al_2O_3 MOSCAPs was employed.

Figure 6 shows the electrical properties of MOSCAPs of MoS_2, HOPG and $Si_{0.7}Ge_{0.3}$(001) substrates with the Al_2O_3/HfO_2 bilayer stacks. As shown in Fig. 6(a), (b), and (c), the C_{max} value was increased by factor of two (~2 μF/cm^2), compared to that of

50 cycles of Al_2O_3 due to the higher dielectric constant of HfO_2 as compared to Al_2O_3. The identical C_{max} value for the different substrates is consistent with identical growth rates and no significant induction period during the ALD. Fig. 6(d) is the leakage current measurement of the MOSCAPs. The leakage currents of the three samples indicates the oxides are insulating and uniform on both 2D materials and $Si_{0.7}Ge_{0.3}$(001) substrate. However, the leakage current of MoS_2 MOSCAP was about 2 orders of magnitude higher at -1V compared to the other substrates. This is due to the high density of tall step edges (~10nm tall) of bulk MoS_2 substrates. Due to the high aspect of the step edges, conformality of the oxide on the MoS2 could be less than an HOPG and a $Si_{0.7}Ge_{0.3}$(001) substrate resulting in the higher leakage. The D_{it} was evaluated using the conductance method from the G-V data in Fig. 6(e) and (f). The extracted D_{it} value of the MoS_2 MOSCAP was 8.9×10^{11} $eV^{-1}cm^{-2}$, which is about an 85% reduction compared to the D_{it} value of $Si_{0.7}Ge_{0.3}$(001) (5.89×10^{12} $eV^{-1}cm^{-2}$) consistent with the result in Fig. 5. Employing low temperature ALD of Al_2O_3 as a seed layer, HfO_2 can be readily deposited on the inert surfaces of MoS_2 and HOPG while maintaining low leakage current.

It is known that titanium and titanium nitride (TiN) gates can be used to reduce the thickness of interface oxide layer in the Si, SiGe, and InGaAs MOSCAPs by gettering oxygen from the interface. The effect of the oxygen scavenging by Ti/TiN metal contacts on the HfO_2/ Al_2O_3 bilayer gate oxide was investigated using Pd/Ti/TiN, as shown in Figure 7. Pd/Ti/TiN top contacts were deposited on the HfO_2/ Al_2O_3 bilayer oxide (40 cycles of HfO_2 at 300 ^oC/10 cycles of Al_2O_3 at 50 ^oC) by DC sputtering.

Identical oxides and gates were deposited on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}(001)$ and capacitors were fabricated using the same process except the top contacts.

Fig. 7 (a), (b) and (c) present the capacitance-voltage measurements. The C_{max} of the three capacitors was increased to ~2.7 μF/cm^2 which was about 30% higher compared to the HfO_2/Al_2O_3 bilayer stack with Ni Gate in Fig. 6. This improvement suggests that Pd/Ti/TiN gates scavenge oxygen from the gate oxide resulting in an increase of dielectric constant of the layer or thinner interface oxide layer (for SiGe). The C_{max} of the $Si_{0.7}Ge_{0.3}(001)$ MOSCAPs was higher (~3.0 μF/cm^2) compared to MoS_2 and HOPG. This indicates that the oxygen scavenging is more effective on $Si_{0.7}Ge_{0.3}(001)$ than MoS_2 and HOPG since there is an $SiGeO_x$ interlayer. The D_{it} values from the MoS_2 and $Si_{0.7}Ge_{0.3}(001)$ MOSCAPs are shown in Fig. 7 (a) and (c). The D_{it} value of MoS_2 MOSCAPs was 1.12×10^{12} eV^{-1}cm^{-2} which is 88 % lower than that of $Si_{0.7}Ge_{0.3}(001)$ MOSCAPs (9.12×10^{12} eV^{-1}cm^{-2}) consistent with the results in Fig. 5 and 6. Fig. 7 (d) shows the leakage current measurement of three MOSCAPS. The leakage current densities of the three samples were similar to the results in Fig. 6 indicating lower EOT was achieved without degradation of the oxide layers.

4.5 Summary

In this study, deposition of high quality Al_2O_3 and HfO_2/Al_2O_3 films on 2D materials using low temperature ALD/CVD was demonstrated without organic seeding layers or chemical treatments. During ALD/CVD, AlO_x particles of below 1 nm

diameter were formed on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}(001)$ consistent with a gas phase reaction of the ALD precursors to form sub 1nm particles (denoted as nanofog) which reversible adsorb onto the substrates. The particles provided nucleation centers for further ALD on the inert 2D material surfaces. To document the nanofog process was conformal even on inert surfaces, a high aspect ratio $Si_3N_4/SiO_2/Si$ structure was coated with sub 2nm thick nanofog Al_2O_3 and was found to be 91% conformal. C_{max} and leakage current values of 50 cycles of low temperature ALD Al_2O_3 on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}(001)$ were comparable indicating uniform and pinhole free Al_2O_3 films across the entire surface. In order to obtain lower EOT, Al_2O_3 (7 cycles at 50 ^oC)/HfO_2(40 cycles at 300 ^oC) bilayer gate stack was prepared on 2D materials substrates. C_{max} was increased by 2x compared to 50 cycles Al_2O_3 MOSCAPs. Pd/Ti/TiN gate was employed to scavenge the oxygen from the oxide. C_{max} of ~2.7 $\mu F/cm^2$ was achieved with MoS_2 and HOPG without loss of leakage current density. All MoS_2 MOSCAPs in this study had lower interfacial defect density (D_{it}) compared to the same gate stacks on $Si_{0.7}Ge_{0.3}(001)$ indicating Van der Waals interactions between the oxide and the 2D material surfaces was dominant instead of direct formation of covalent bonding. This study can provide a way to prepare superior interface of 2D semiconductor oxide gate stacks with low EOT and leakage current.

4.6 Acknowedgments

This work is supported in part by the National Science Foundation Grant DMR 1207213, by the Center for Low Energy Systems Technology (LEAST) and Applications and Systems driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT). STARnet and JUMP sponsored by Semiconductor Research Corporation (SRC) programs and DARPA, and by the SRC Nanoelectronic Research initiated through the South West Academy of Nanoelecronics (SWAN), and Experiments were performed in the UCSD Nano3 facility supported by the NNCI (ECCS-1542148).

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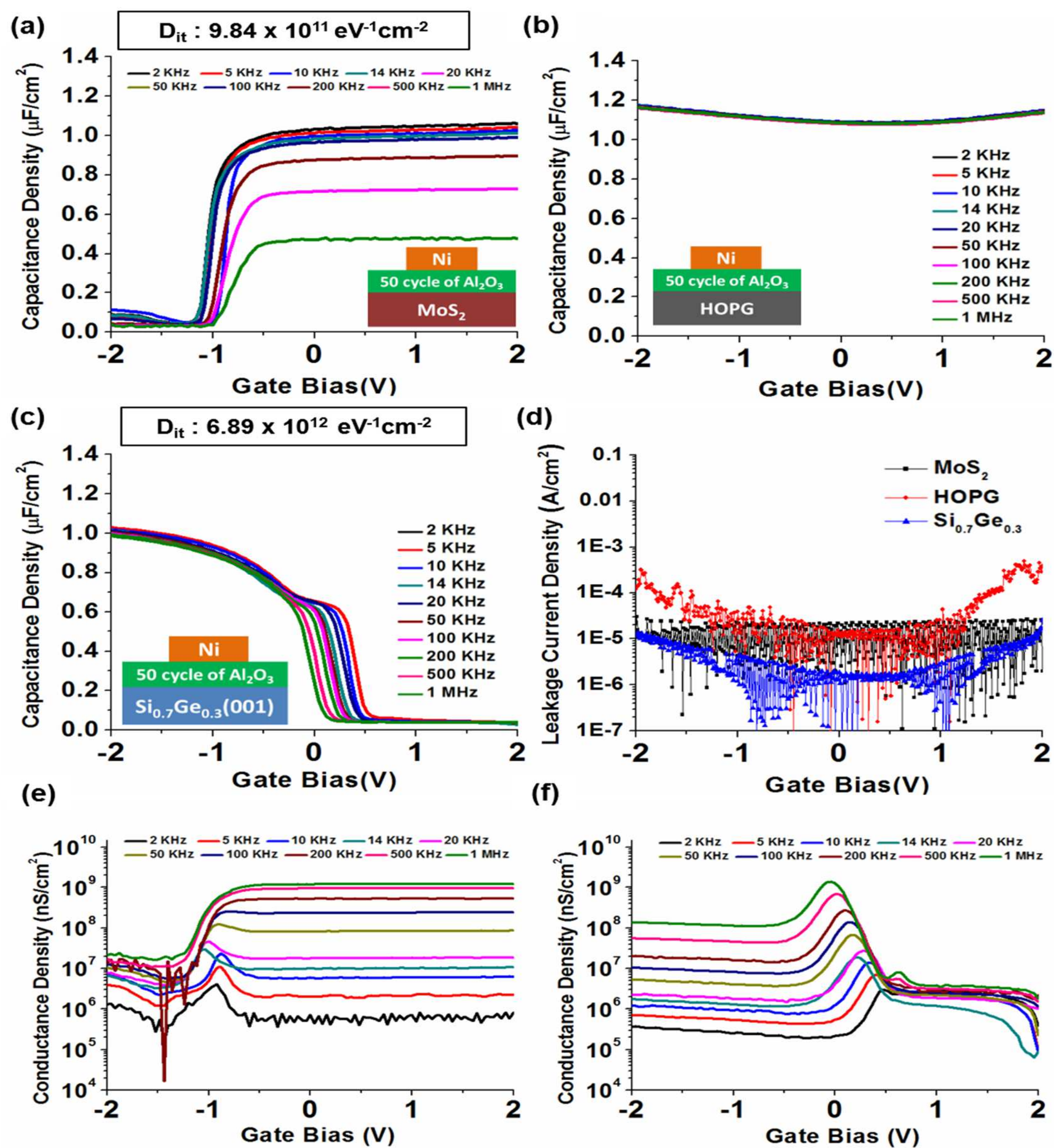

Figure 4.1 Capacitance vs. Voltage Curve of Ni/Low temperature Al_2O_3 50 ALD cycles on (a) MoS_2, (b) HOPG, (c) $Si_{0.7}Ge_{0.3}$(001) substrates. (d) Leakage current density of Ni/Low temperature Al_2O_3 50 ALD cycles on MoS_2, HOPG, $Si_{0.7}Ge_{0.3}$(001) substrates. (e), (f) Conductance density vs gate bias of MoS_2 and $Si_{0.7}Ge_{0.3}$(001) gate stacks respectively.

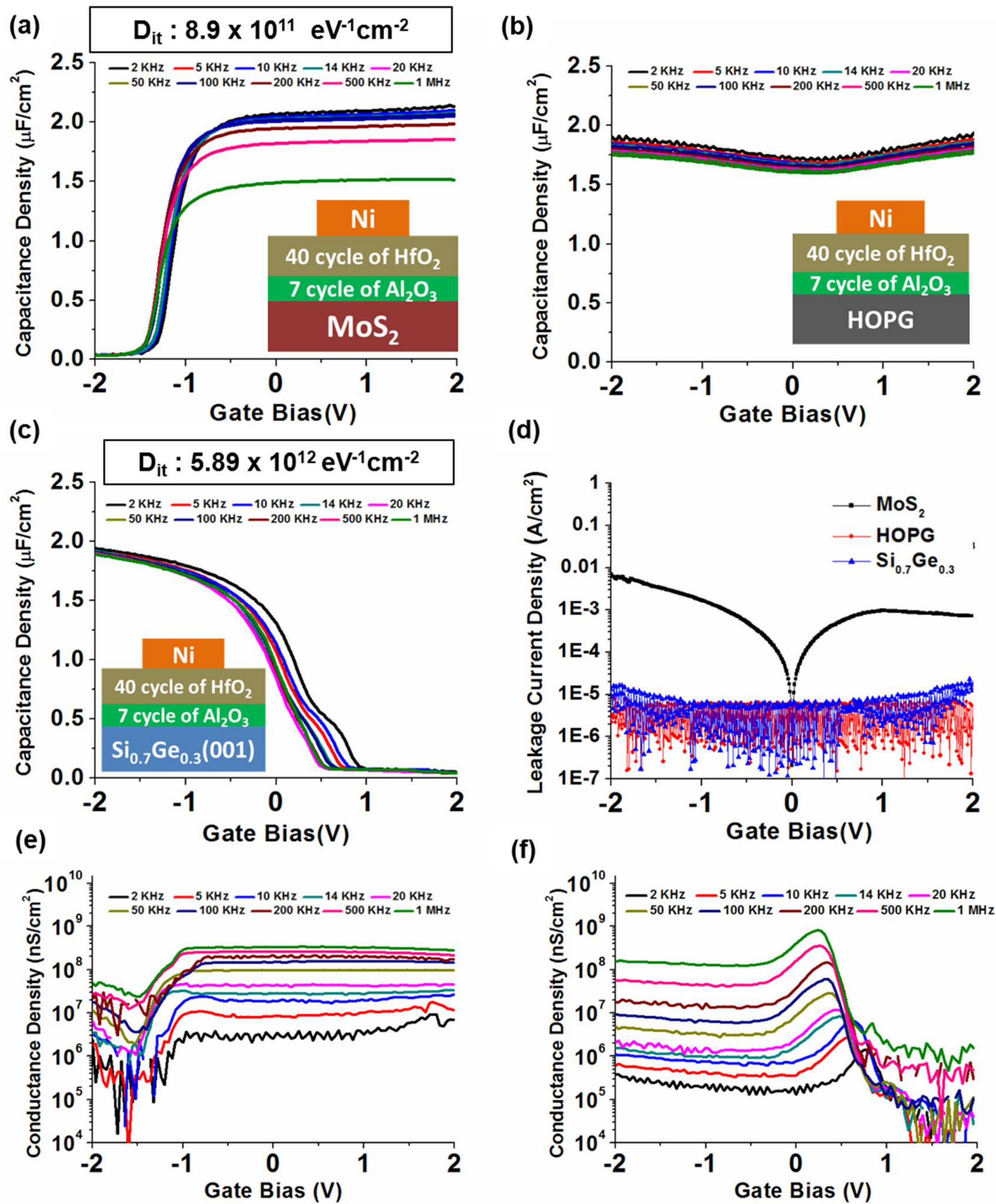

Figure 4.2 Capacitance vs. Voltage Curve of Ni/HfO$_2$ (40 ALD cycles)/Low temperature Al$_2$O$_3$ (7 ALD cycles) on (a) MoS$_2$, (b) HOPG, (c) Si$_{0.7}$Ge$_{0.3}$(001) substrates. (d) Leakage current density of Ni/HfO$_2$ (40 ALD cycles)/Low temperature Al$_2$O$_3$ (7 ALD cycles) on MoS$_2$, HOPG, Si$_{0.7}$Ge$_{0.3}$(001) substrates. (e), (f) Conductance density vs gate bias of MoS$_2$ and Si$_{0.7}$Ge$_{0.3}$(001) gate stacks respectively.

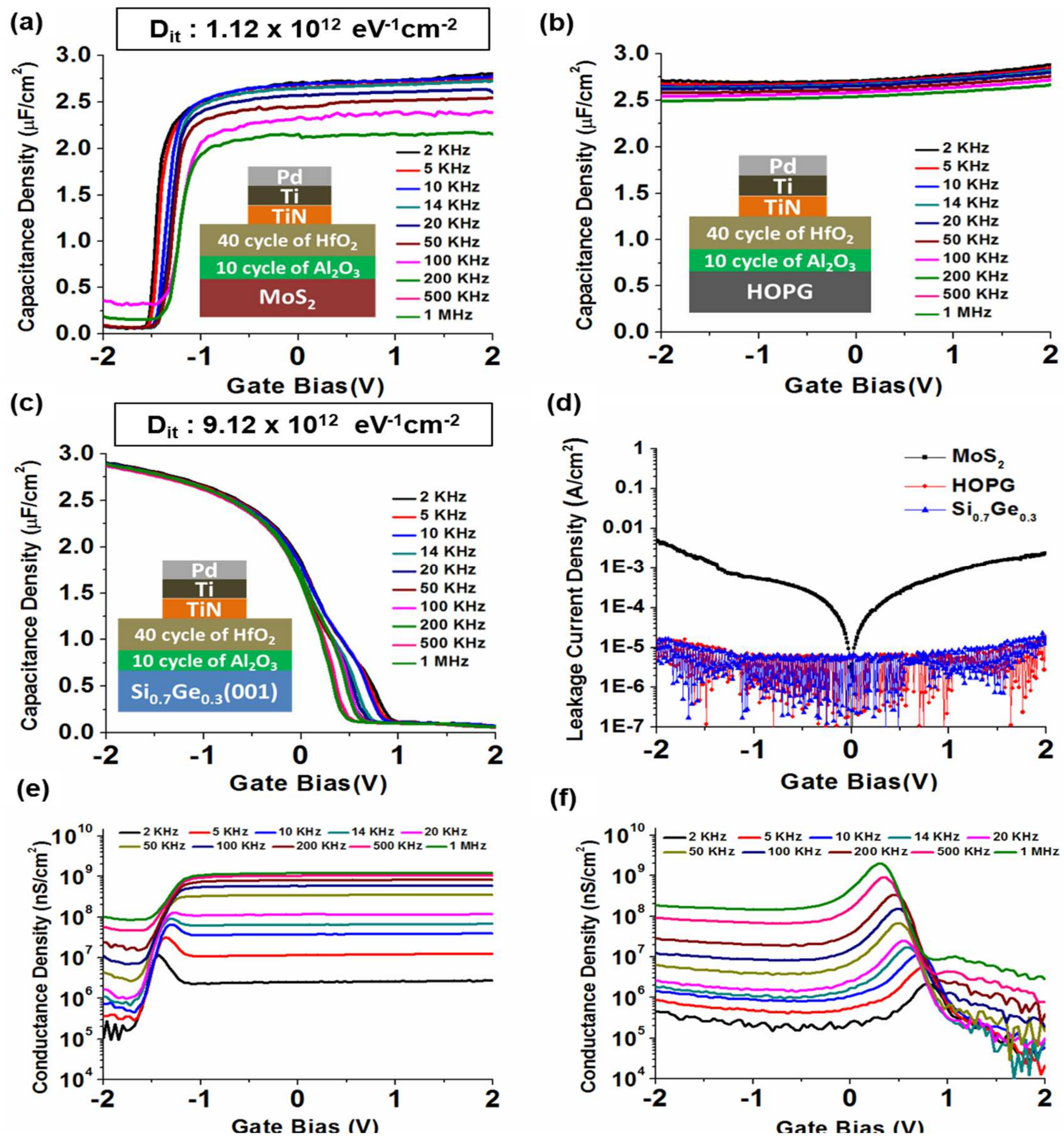

Figure 4.3 Capacitance vs. Voltage Curve of HfO_2 (40 ALD cycles)/Low temperature Al_2O_3 (10 ALD cycles) with Pd/Ti/TiN contact of (a) MoS_2, (b) HOPG, (c) $Si_{0.7}Ge_{0.3}$(001) substrates. (d) Leakage current density of Pd/Ti/TiN/Low temperature Al_2O_3(10 ALD cycles) + HfO_2 (40 ALD cycles) on MoS_2, HOPG and $Si_{0.7}Ge_{0.3}$(001) substrates. (e), (f) Conductance density vs gate bias of MoS_2 and $Si_{0.7}Ge_{0.3}$(001) gate stacks respectively.

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