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An Analog Phase Interpolation Based Fractional-N PLL

A Thesis submitted in partial satisfaction of the
requirements for the degree Master of Science
in Electrical and Computer Engineering

by

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The thesis of Aaron James Bluestone is approved.

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James Buckwalter

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ABSTRACT

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A novel phase-locked loop topology is presented. Compared to conventional designs, this architecture aims to increase frequency resolution and reduce quantization noise while maintaining the fractional-N benefits of high bandwidth and low phase noise up-conversion. This is achieved utilizing a feedforward mechanism for offset cancellation from the integer-N frequency. The design is implemented in a 0.13μm CMOS process technology. A frequency resolution of 1.16Hz is achieved on a 5GHz differential delay cell VCO with a 100MHz reference oscillator. A ping-pong swallow counter topology alleviates pipeline latency to achieve 1-64 divide ratios. A digital pulse generator and nested phase-frequency detector provide tunable offset cancellation. A 5-bit current-steering DAC capable of 200ps pulses reduces output spurs. Theoretical calculations and Simulink modeling provides insight to the effects of non-idealities in the system. Test structures and loop configurability are programmed via SPI interface through a custom GUI and prototype PCB.

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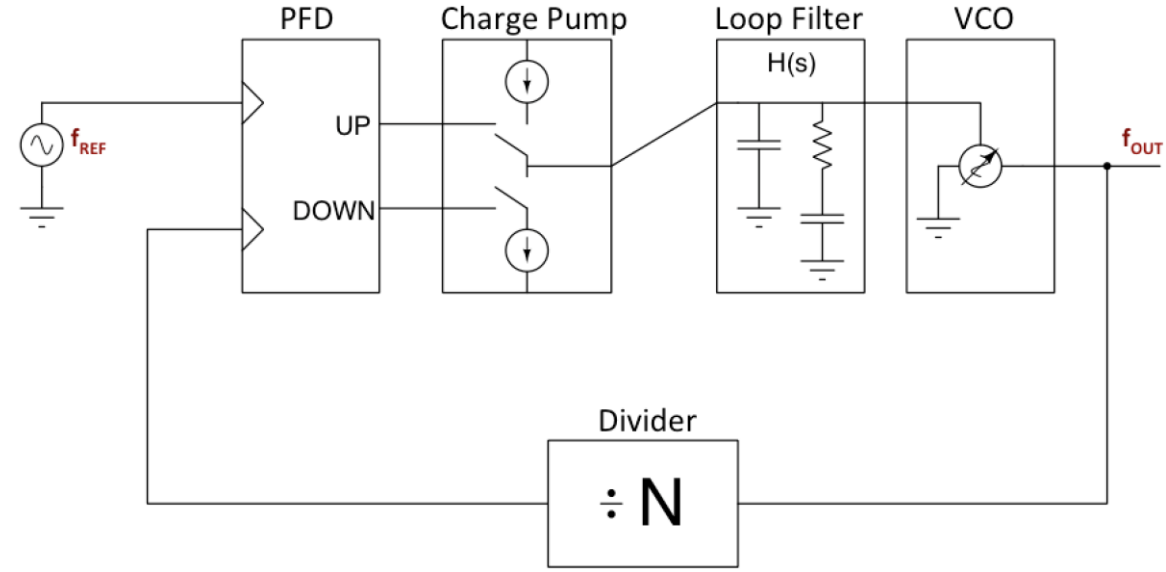
I. Introduction

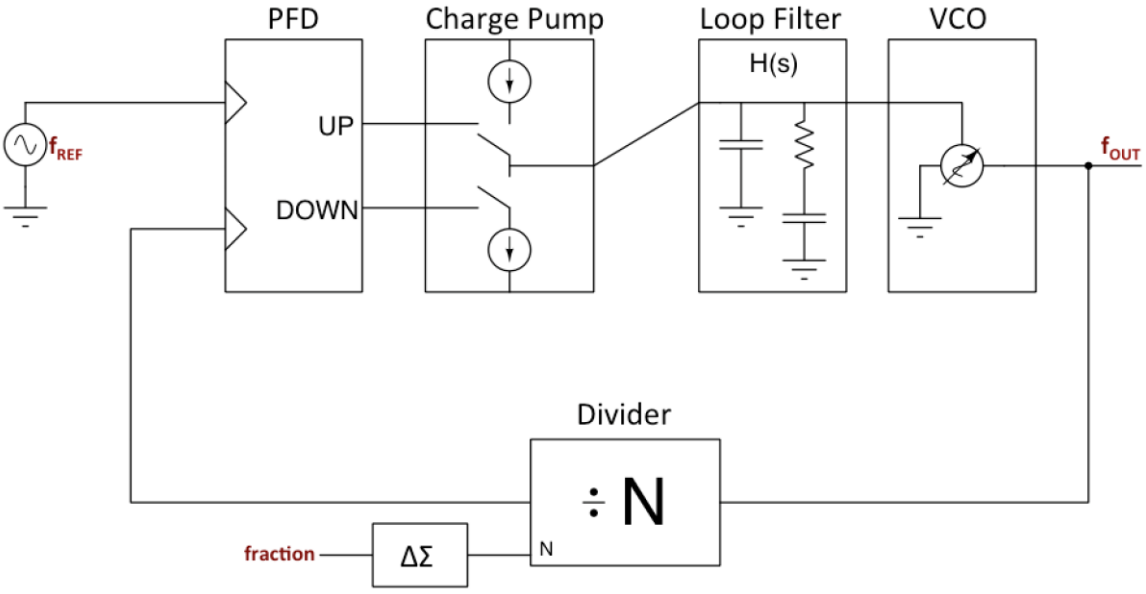
On-chip frequency synthesis is a demanding research topic for a growing number of applications. Microprocessors, communications systems, and metrology all require low-noise clocks at frequencies that cannot be supplied from off-chip references. A phase-locked loop (PLL) employs a negative feedback loop that relies on a stable reference to lock the phase and frequency of a variable oscillator, typically a voltage-controlled oscillator (VCO) for analog PLLs. A feedback signal from this VCO is typically passed through a frequency divider and then its phase is compared to the phase of the reference. A common method converts the output of a phase-frequency detector (PFD) to a current through a charge pump, which forms an error voltage that is passed through a loop filter and used to adjust the VCO's frequency.

An Integer-N PLL utilizes a feedback divider of set value "N" which locks the output frequency to N times the reference frequency ($f_{OUT} = N \times f_{REF}$). Because the PFD operates on making comparisons at the rate of the reference, the feedback loop can only be stabilized for a bandwidth < $1/10^{th}$ f_{REF}. High loop bandwidths are desirable to suppress VCO phase noise and keep the 20log(N) up-conversion of reference phase noise low, though modern systems often require a synthesizer that can resolve closely spaced channels[1]. For example, the Wi-Fi 802.11 b/g/n standard has 14 channels near 2.4GHz, spaced 5MHz apart [2]. An Integer-N synthesizer for Wi-Fi applications would require f_{REF} <= 5MHz, and could at most suppress phase noise out to 500KHz offset. To mitigate this frequency resolution / bandwidth & phase noise trade-off, designers typically implement a Fractional-N architecture which toggles between

multiple divide values to give an average output frequency resolution independent of PFD speed.



(a)



(b)

Figure 1: Conventional integer-N (a) and fractional-N (b) charge pump based PLLs

The earliest form of a fractional-N toggled the divide value between N and N+1 to give a frequency between the two values. Because the divided frequency will never perfectly match f_{REF}, this leads to a deterministic error signal at the PFD output, which in turn translates to a large spur in the output phase noise. Spur reduction in

Fractional-N topologies has been extensively investigated and many solutions involve feed-forward PFD error cancellation or shaping the quantization noise into high frequencies with a Δ-Σ modulator [3, 4]. This thesis will introduce a novel method for achieving the high frequency resolution of a fractional-N that removes dithering of the divider and its associated noise.

II. System Overview

The general concept arose from a goal to move the fractional resolution from the feedback divider to the feedforward path. Assuming a frequency offset from an integer-N could be achieved at the output, Figure 2 shows the expected signals at the inputs (a,b) and output (c) of the PFD. For a divided frequency slightly higher than f_{REF}, the PFD will output DOWN pulses with increasing width, as the phase offset grows larger. This signal will repeat itself at the rate of the beat frequency, $f_{OUT}/N - f_{REF}$. Due to the integrating loop filter, the output frequency will hold steady when the overall error signal settles to an average of 0. Therefore, a complementary signal can be generated that cancels the DOWN pulses (d) and the output will be forced to sit at this frequency offset. A second PFD then compares the expected pulse and first PFD output to generate a new error signal. The challenge became designing a high-resolution pulse generator with programmable beat frequency that can be used to set the output fractional-N frequency.

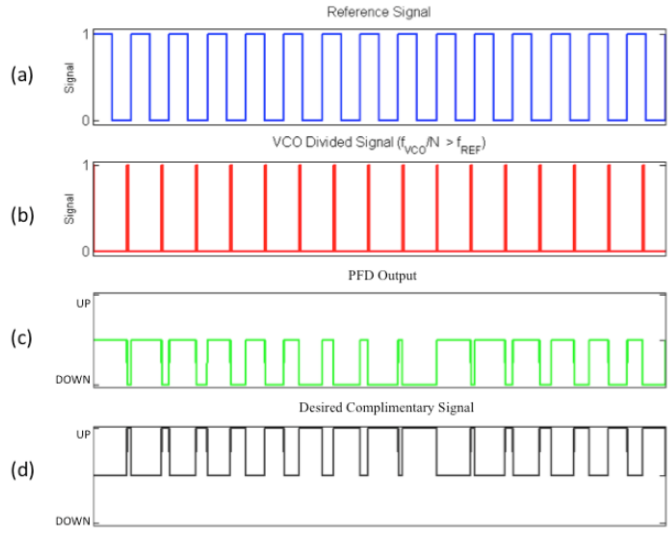


Figure 2: Transient simulation showing the output of an ideal PFD (c) when the reference signal (a) is slower than the feedback signal (b). The desired complimentary signal (d) would cancel the output error signal.

The analog comparator topology shown in Figure 3a was first explored for the pulse generator. A fast ramp would be generated off of the same reference oscillator, while the slow ramp would be a tunable current source charging a capacitor, and the beat frequency of that signal sets the fractional-N offset described above. Fabrication non-idealities affecting the capacitors, current source, and comparator voltage offset could all be accounted for in a calibration loop, however the accuracy on a cycle-to-cycle scale would be limited by the input noise of the comparator. This constraint eventually led to the digital pulse generator (DPG) shown in Figure 3b, which maintains a precision dictated by the reference oscillator.

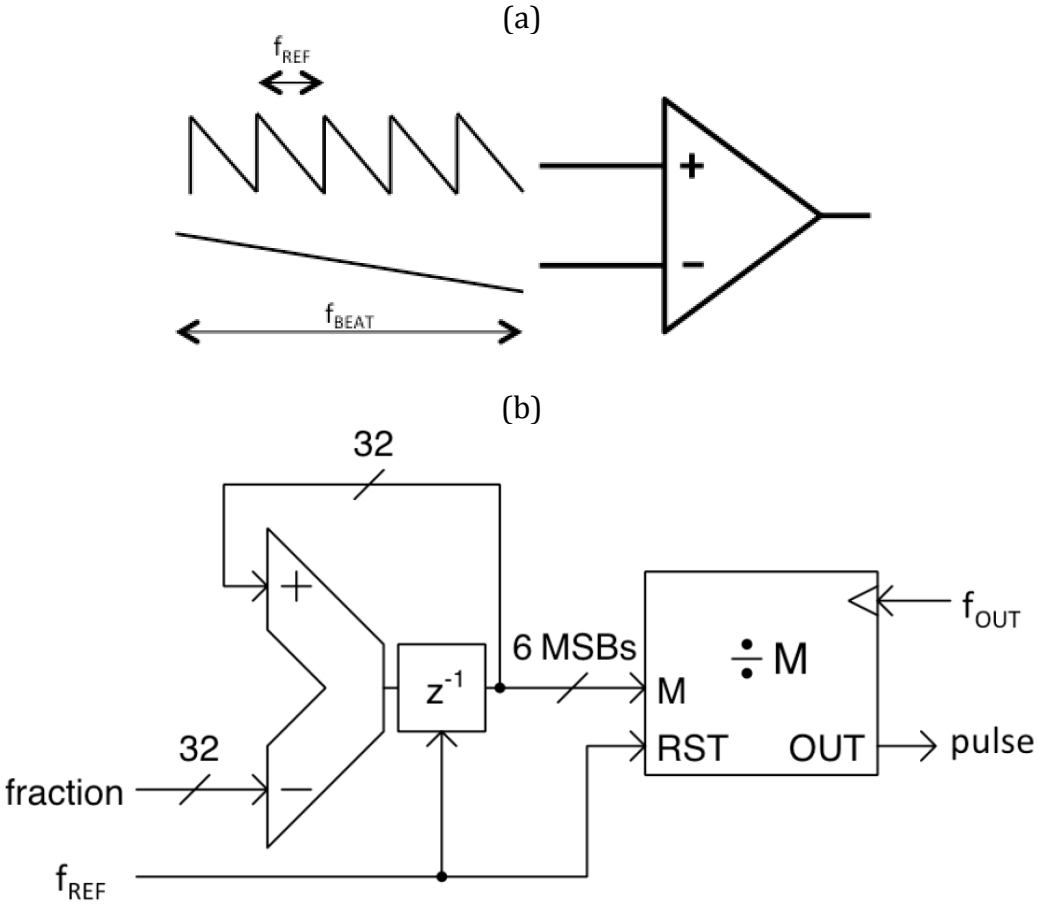


Figure 3: Analog (a) and digital (b) pulse generators for cancellation of beat frequency signal.

When the divider M value is close to the integer-N value, there will be a short pulse before the reference signal resets the output. Analogously when M is relatively close to 0, the pulse will be held high for a majority of the period and still reset on f_{REF}, as the system desires. The DPG takes in a 32-bit word that sets the speed of a decumulator whose output MSBs are used to set the M divide word. By resetting to N every time the decumulator reaches 0, this creates the required signal pattern with a beat frequency controlled by the fraction word. The design of a 32-bit decumulator at reference clock speeds is relatively straight forward, while the added benefit is frequency resolution of $f_{REF} / 2^{32}$. For the target design of f_{OUT} = 5GHz and f_{REF} = 100MHz, this translates to 1.16Hz resolution at the output.

While the beat frequency can achieve high resolution, the pulse width resolution is limited by the clock period of the output. Consider when the above design aims to take advantage of a 1kHz beat frequency, the PFD output pulse width would slowly increase over 100,000 cycles, increasing 0.1ps each time. For a 5GHz output clock, this counter based DPG can only achieve 200ps resolution, leading to maximum quantization errors of +/- 100ps. In a charge-pump PLL, these error signals are converted to current pulses that are then integrated on a capacitor to form the tune voltage for a voltage-controlled oscillator (VCO). This quantization error can be cancelled each cycle by adding an opposing current for an amount of time such that the net charge is zero.

$$\Delta V = \frac{I_{CP} \times t_{Quan.Error} - I_{opposing} \times t_{min}(200ps)}{C}$$

In the target design, a 5-bit DAC referenced to the charge pump current for the minimum pulse width (1 f_{OUT} cycle) yields an effective resolution of $200ps/2^5$ and a

maximum quantization error of +/- 3.1ps. Figure 4 shows the full PLL schematic with the addition of the DAC. Notably, the next 5 MSBs from the decumulator inherently form the perfect word for cancellation because of the linear ramp in pulse width quantization error.

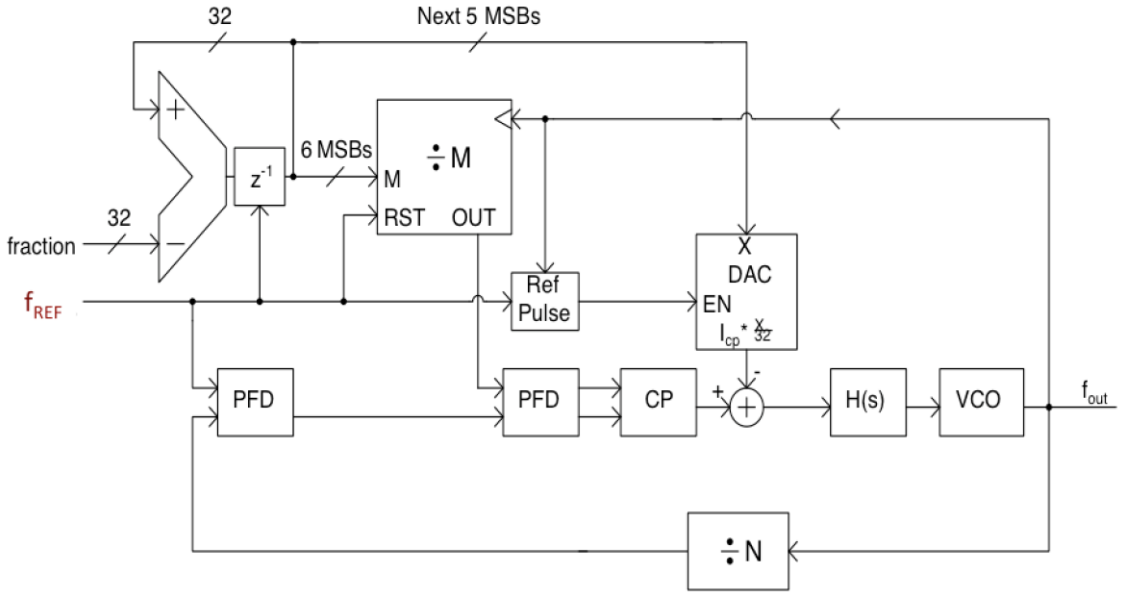


Figure 4: Analog phase interpolation based fractional-N system model.

III. Simulink Model

The entire feedback loop was modeled in MATLAB Simulink to initially prove the concept. The model helped gain intuition into the design challenges and provided several solutions to previously unforeseen issues. The pulse generator portion is shown in Figure 5.

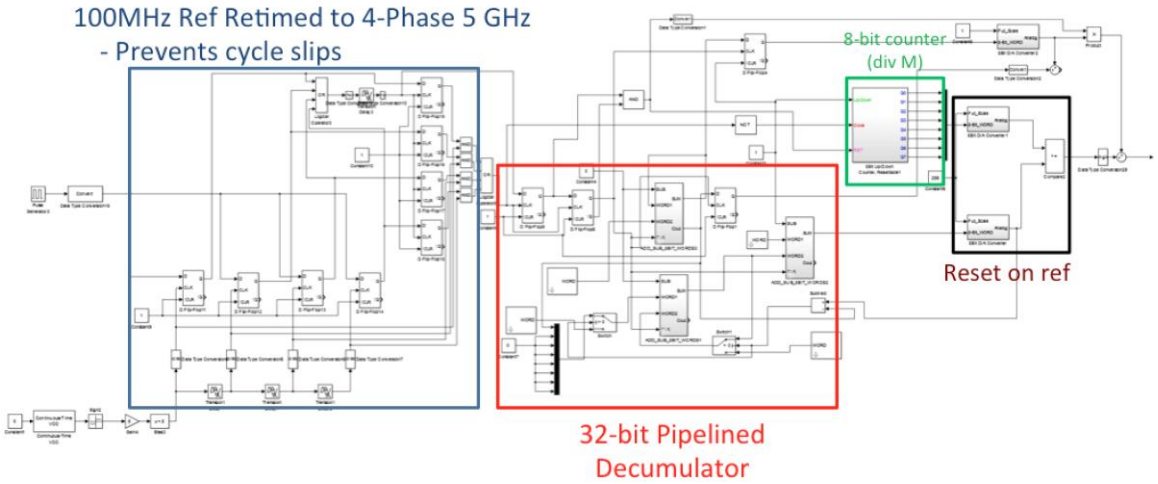


Figure 5: Simulink model of digital pulse generator (DPG).

Because the reference oscillator and output oscillator are unsynchronized, there's no certainty when the reset signal will arrive at the divide-by-M with respect to the counting clock, f_{OUT}. The simulation showed this could lead to race conditions that caused periodic errors in the output. To fix this, each rising edge of the reference is retimed to 1 of 4 output clock phases (90° apart). The selected output phase and synchronized edge are used for the next cycle.

The simulation also showed that a drastic glitch can occur when the system is not fully settled or operates with a static phase offset. If either the pulse generator or PFD output resets from a very high pulse width to minimal pulse width on a cycle while the other remains high one more cycle, the second PFD assumes a large error and

outputs a current pulse for nearly one full cycle. While an error-handling scheme could catch this in future designs, the straightforward solution was to disable the charge pump for several cycles before and after the expected reset point.

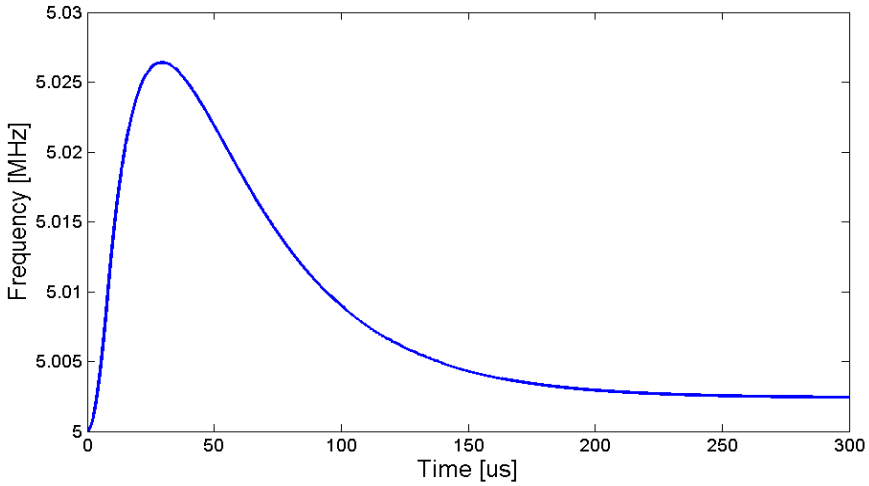


Figure 6: Simulink transient simulation showing the VCO settling in fractional-N mode.

The result above shows the VCO frequency from start-up to lock for a 100kHz reference and 50.025 divide ratio. The orders of magnitude difference between output frequency and loop bandwidth cause the simulator to record data files too large for processing. For this reason, the loop was slowed by 1000x and the output VCO runs at 5MHz. The same issue eventually manifested itself in Cadence transient simulations for the system-level verification.

IV. Theoretical Model

This chapter will provide theoretical error values the PLL output may experience based off non-idealities in the system. Specifically, the finite resolution of the DPG or a current mismatch between the charge pump and DAC could both result in a periodic jitter, invoking a spur in the output phase noise. The calculations below assume $f_{BEAT} << f_{REF}$, a worst-case scenario where the phase evolution of the first PFD can be considered analog as opposed to the discrete pulse width steps of the DPG.

A. Quantization Error without DAC

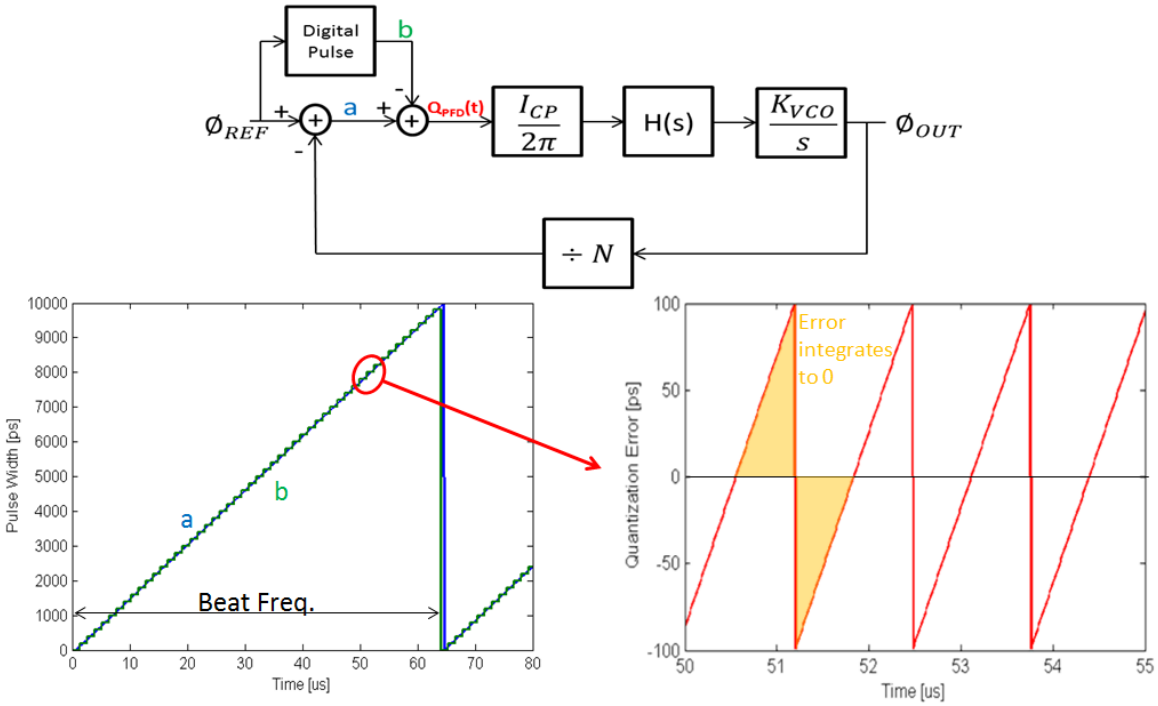


Figure 7: Phase domain model without the DAC enabled. The left plot shows the two signals entering the second PFD. Plot on the right shows the resulting quantization error.

Figure 7 first analyzes the quantization error of the pulse comparison when the DAC is disabled (Q_{PFD}). For low frequency spurs, the transfer function is approximately a gain of 1 and the spur will be convolved with the output spectrum[5]:

$$S_{OUT}(f) = \left|\frac{A(f)}{1+A(f)}\right|^2 \times S_{E_{spur}}(f) \; ; \; A(f) = \frac{I_{CP}}{2\pi} H(jf) \frac{K_{VCO}}{jf} \frac{1}{N}$$

The saw tooth error signal can be represented by its Fourier series equivalent:

$$\sum_{n=1}^{\infty} \frac{1}{n\pi} \sin\left(\frac{n\pi t}{T}\right)$$

Similar to measuring phase noise by taking the FFT of a tune voltage, the magnitude of the spurs are measured by comparing the saw tooth strength relative to an unlocked beat note on the tune voltage. For the given 5GHz VCO and 100MHz reference, the closest spur is -37.9dBc at N x f_{BEAT} offset. Figure 7 also shows that the system locks with a static phase offset between the two signals entering the PFD. Comparable to the effects of non-idealities in a traditional PLL, this occurs so the integration over time yields a DC value of 0 and the tune voltage doesn't drift. With the DAC disabled, the phase offset is π/N, 3.6° in this design.

B. Quantization Error with DAC

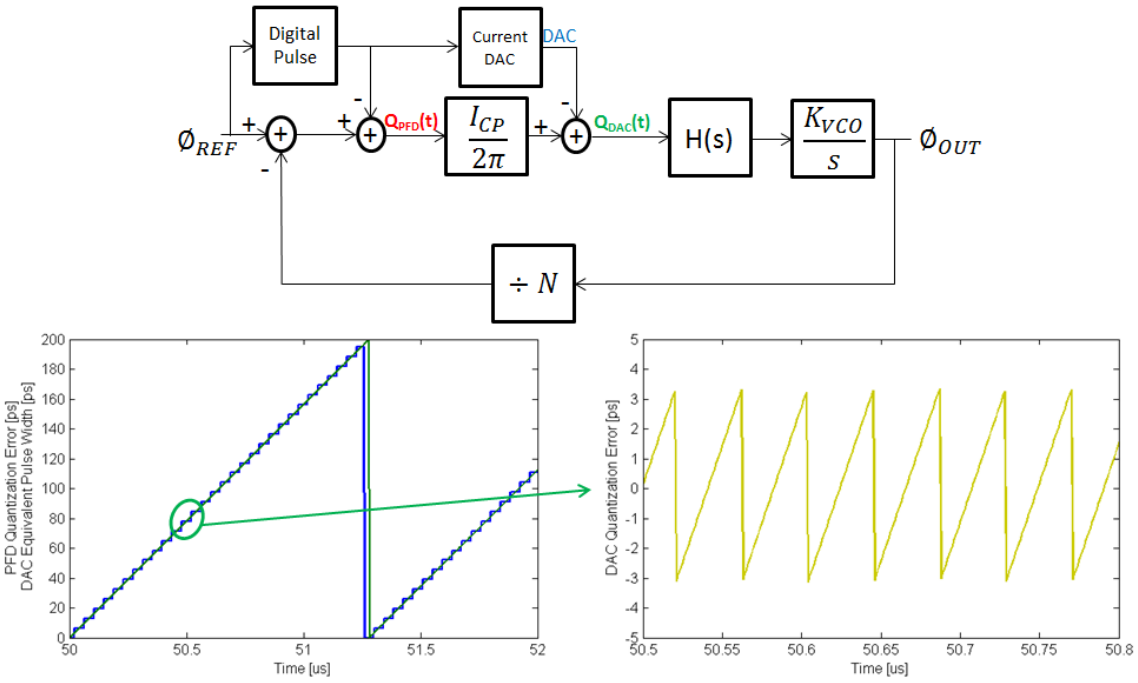


Figure 8: Phase domain model with the DAC enabled. Plot on the right shows PFD error and equivalent pulse width of the DAC current. The left plot shows resulting quantization error.

The periodic quantization noise of Q_{DAC} takes the same saw tooth shape as Q_{PFD} with the amplitude reduced by a factor of 2^5 for a 5-bit DAC. The repetition rate also increases by the same factor of 32 since the DAC operates on the next 5 bits ramping faster in the decumulator. This leads to a closest spur of -68dBc at 32 x N x f_{BEAT} offset. The static phase offset required to reach a DC error of 0 is also reduced to 0.1125°.

C. Effect of Current Mismatch

The spur reduction above made an assumption that the DAC current reference was perfectly matched to the charge pump, $I_{DAC,LSB} \times 32 = I_{CP}$. Using matched layout techniques, operating both designs off the same bias network, and spatial locality on-chip all help minimize mismatch, but some deviation is inevitable. Figure 9 looks at a worst-case scenario of 1 LSB full-scale range offset,

$$I_{DAC,LSB} \times 32 = \frac{31}{32} I_{CP}.$$

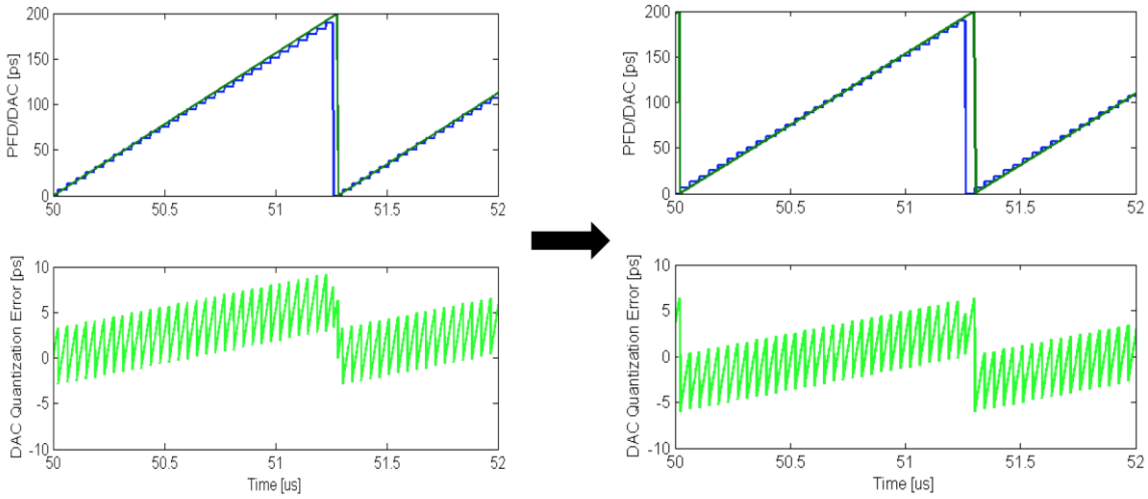


Figure 9: Initial quantization error for current mismatch (left) in the system, and resulting quantization error after the loop settles (right).

The difference in amplitude yields another saw tooth ramp at the slower rate of f_{BEAT} x N. This offset was shown to be the dominant spur when the DAC is turned off,

but the amplitude for this worst-case mismatch is significantly lower at -66dBc. The left set of plots in Figure 9 shows that the quantization error from ramp mismatch leads to a positive integration that would ramp up the VCO tune voltage. As shown in the plots on the right, a larger static phase offset once again returns the DC value to 0.

These examples show that despite non-idealities and limited pulse width resolution, the frequency resolution set by the 32-bit counter is maintained and the periodic jitter translates to close-in spurs in the output spectrum.

V. Integrated Circuit Design

The following section details the critical analog / mixed-signal circuit designs for fabrication of this fractional-N architecture in 0.13µm CMOS technology. The goal in aiming for a 5GHz VCO was to push the capabilities of this technology to the limit. This forced every component (dynamic flip-flops, ping-pong swallow counter, current-steering DAC / charge pump, etc.) to implore a high-performance and novel design.

A. Voltage Controlled Oscillator

A VCO with a low K_{VCO} (Hz/V) was essential to obtain and measure the frequency resolution this architecture can achieve, without being limited by the expected voltage noise on V_{TUNE}. The differential delay cell design shown in Figure 10 offers a frequency fine-tuning bias that can reduce the amount of current available for switching the inverters[6]. The design also gives 3 differential sets of outputs, ideal for the reference re-timing circuitry needed to avoid race conditions in the digital pulse generator. Assuming 20fF load from the interconnect and the typical process corner:

VCO Performance Summary

Frequency	4.7~5.1GHz
K_{VCO}	266MHz/V
Phase Noise	-94dBc/Hz @ 1MHz offset
	-120dBc/Hz @ 10MHz offset
Power Consumption	16mA @ 2.5V

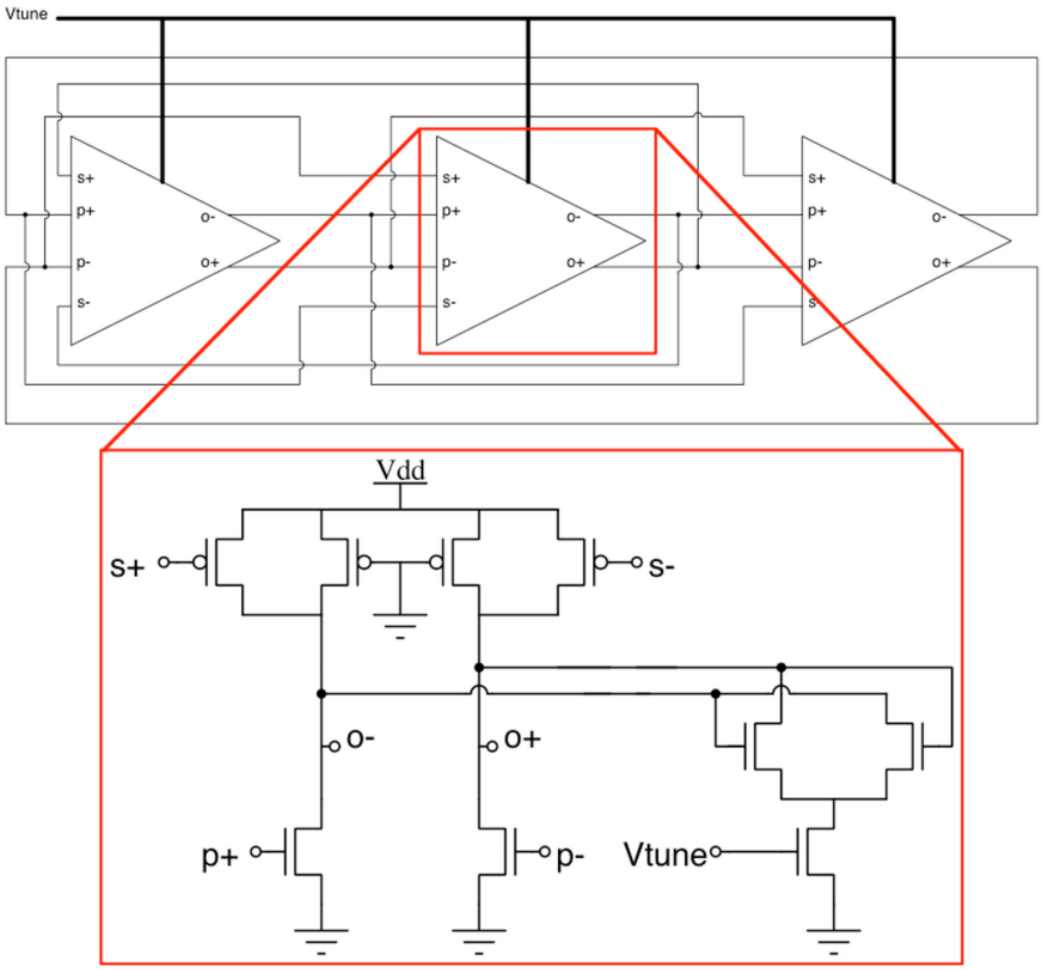


Figure 10: Differential Delay Cell VCO.

B. Frequency Dividers

A swallow counter was chosen for the frequency divider to minimize the number of gates switching at the clock frequency[7]. At high-speeds the combinational logic following the clock dividers presents a significant propagation delay, which unfortunately is divide-word dependent. To maintain a synchronized system, the entire swallow counter was pipelined, with flip-flops following each divide-by-2 and binary comparison. A True Single Phase Clock (TSPC) Master-Slave Flip-Flop was utilized to handle the 5GHz timing requirements in this technology.

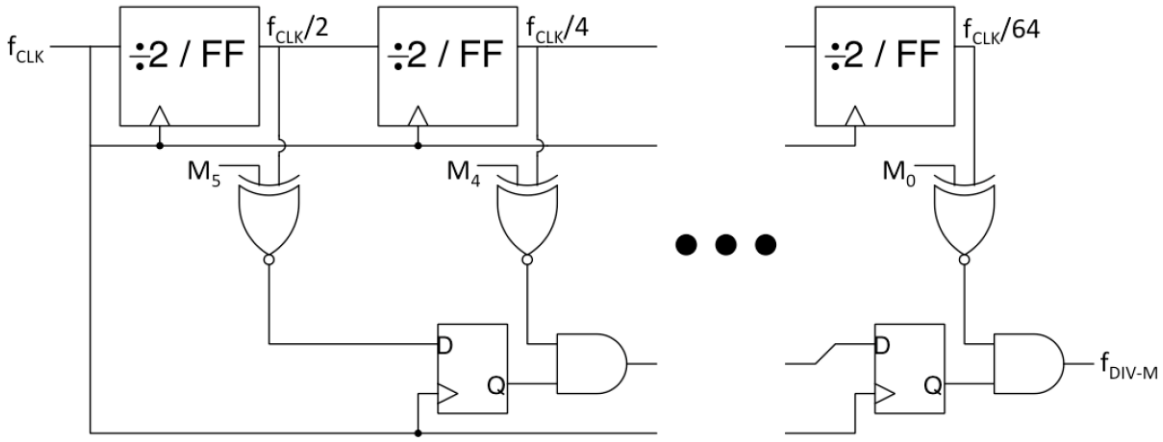


Figure 11: Pipelined Swallow Counter architecture for frequency division.

While the pipelined swallow counter is synchronized, it presents a minimum delay path of 9 input clock cycles. For the divide-by-N feedback route, this doesn't present a problem; the input word is just given N+9, with a minimum division of 10. The divide-by-M in the pulse generator however must be able to cover its full range for minimum to maximum duty cycle generation. The novel solution is a ping-pong swallow counter, shown in Figure 12. Delaying the reset signal by 9 cycles through shift registers allowed the minimum divide ratio to return to 1, but next division would need to start while the pipeline is resetting itself. To solve this, a second copy of the swallow counter was added to begin the a second division while the first is completing. Toggle logic handles switching between the two dividers at the input and output.

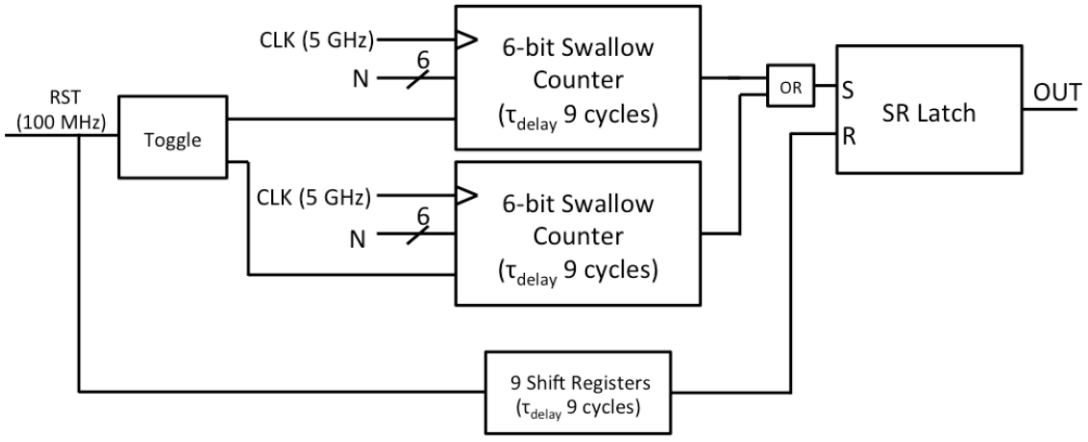


Figure 12: Ping-Pong Swallow Counter for full frequency division range (1-64).

C. Nested Phase-Frequency Detector

Because the pulse generator rising edge is compared to the output of the traditional reference-feedback PFD, the design calls for a PFD within a PFD. It is trivial to prove that the system can limit the beat frequency to less than $0.5f_{REF}$ by operating the above integer-N for $f_{beat} < 0.5f_{REF}$ and below integer-N for $f_{beat} > 0.5f_{REF}$. In order to allow the system to lock to fractional frequencies both above and below the integer-N value, the second PFD must be able to toggle between the UP and DOWN output of the first PFD. In addition, when locking below integer-N the reference becomes the leading edge so the SR latch output of the swallow counter must be inverted. A detail of the multiplexing required for real-time configurability is shown in Figure 13.

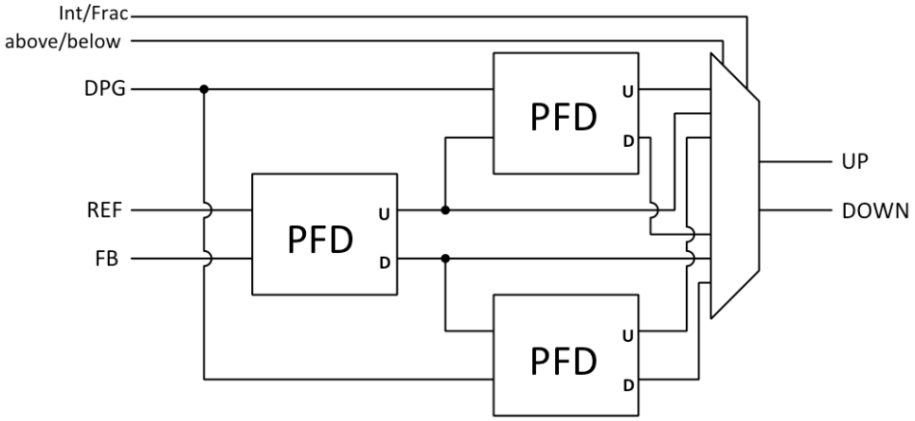


Figure 13: Phase comparison topology with digital multiplexing for integer mode and above and below fractional modes.

D. Bias Network

A robust feedback loop is used to generate the bias voltages for the voltage buffers, charge pump, and DAC. The bias network shown in Figure 14 provides 59dB PSRR and < 1% current variation for all process corners across 2.25-2.75V supply. The two middle branches invoke a threshold voltage dependency to fix the current in both paths based off the resistor value. The left three branches provide the internal cascode

biases, and the diodes are used as a start-up circuit to prevent the network reaching another stability point where no current flows. The two branches on the right mirror that current in a Sooch topology to achieve the maximum swing:

$$(V_{gs,n}-V_{th,n})<V_{out}< V_{DD}-2(V_{sg,p}-V_{th,p}).$$

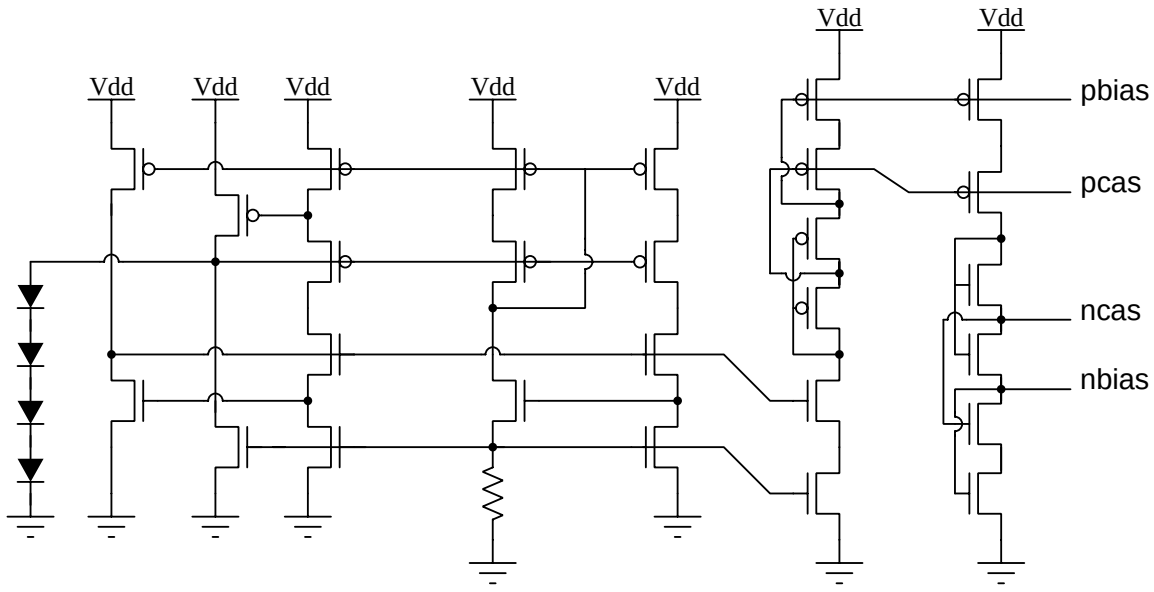


Figure 14: Constant g_m bias network with start-up circuitry and Sooch mirror for maximum voltage swing.

E. Current-Steering DAC and Charge Pump

Designing for 200ps current pulses requires sources with minimal rise / fall times. A current-steering scheme keeps the bias transistors operating at all times for quicker turn-on at the cost of static power dissipation[8]. A voltage buffer is used to provide a mimic of the output voltage, preventing current variation between the two paths. A servo-loop matches the sink and source currents across 0.5-2V output by adjusting the pbias voltage. The DAC is a replica design of the charge pump but with magnitude tuning implemented by switching the cascode node between cut-off and the bias voltage.

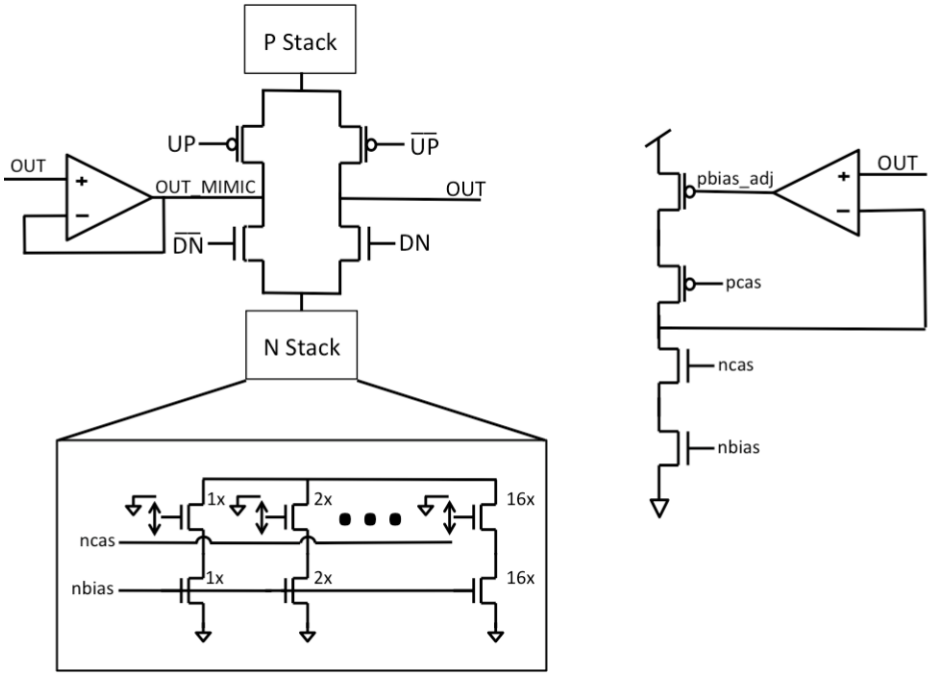


Figure 15: Current-Steering Topology for Charge Pump and DAC.

F. Loop Stability

The passive loop filter shown in Figure 13 gives a transfer function of:

$$V_{tune}(s) = I_{CP} \times \left[\frac{1}{sC_1} \middle\| \left(\frac{1}{sC_2} + R\right)\right]$$

$$= I_{CP} \times \left[\frac{\frac{1}{sC_1} \times \left(\frac{1+sRC_2}{sC_2}\right)}{\frac{1}{sC_1} + \left(\frac{1+sRC_2}{sC_2}\right)}\right]$$

$$= I_{CP} \times \left[\frac{1+sRC_2}{sC_2 + sC_1 + s^2RC_1C_2}\right]$$

$$= I_{CP} \times \left[\frac{sRC_2 + 1}{s(C_2 + C_1) \times \left(1 + sR\frac{C_1C_2}{C_1 + C_2}\right)}\right]$$

for $C_2 >> C_1$:

$$V_{tune}(s) \cong I_{CP} \times \left[\left(\frac{1}{sC_2}\right) \times \frac{1+sRC_2}{1+sRC_1}\right]$$

C_2 serves as the dominant integrating filter while the choice of R and C_1 sets a pole-zero pair for lead-lag compensation. With the loop filter given as H(s), the closed-loop transfer function in the phase domain is:

$$\frac{\theta_{OUT}(s)}{\theta_{IN}(s)} = \frac{\frac{K_{VCO}}{s}\frac{I_{CP}}{2\pi}H(s)}{1 + \frac{K_{VCO}}{s}\frac{I_{CP}}{2\pi}H(s)\frac{1}{N}}$$

The table and open-loop bode plot below demonstrate values chosen to stabilize the PLL with a 1MHz bandwidth.

Loop Parameters		
K_{VCO}	1.67	Grad/s
I_{CP}	50	µA
N	50	
C_1	40	pF
C_2	2	pF
R	19.7	kΩ

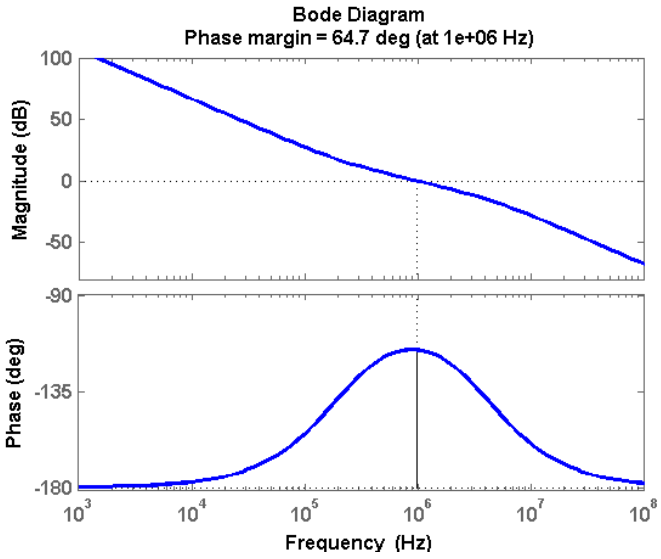


Figure 16: Open-loop bode plot stability analysis.

G. Synthesized Logic: Pipelined Decumulator and SPI Bus

Compared to the rest of the architecture, the pipelined decumulator and SPI bus were relatively straightforward and low-speed designs. Digital standard cells were utilized to convert RTL to gate level schematics that met critical timing. A place and route tool was then used to generate and auto-route a compact layout of each design.

The pipelined decumulator consists of four 8-bit decumulators, with the last decumulator in the chain serving as the MSBs. Because only the next 5 MSBs are wired out for the DAC, only one set of 5 flip-flops is needed for data realignment of the second to last decumulator operating one cycle early. Look-ahead logic resets each stage in 4 consecutive cycles.

The SPI bus is the single channel for real time configurability. Divider words, the fractional word, and several test bench modes for the DAC and reference retiming are all shifted in the standard SPI format. The MISO signal shifts out the word latched on the previous SPI write for verification.

H. System Level Results

Transient simulations confirmed functionality and loop stability for integer and fractional modes of operation. Similar to the Simulink model, the 3 orders of magnitude difference between clock frequency and loop bandwidth make this a lengthy simulation. Creating equivalent Verilog-AMS models for the pulse generator, PFD, charge pump, and dividers gave a 6x improvement in simulation speed. Figure 17 shows a plot for the system started in Integer-N and switched to Fractional-N.

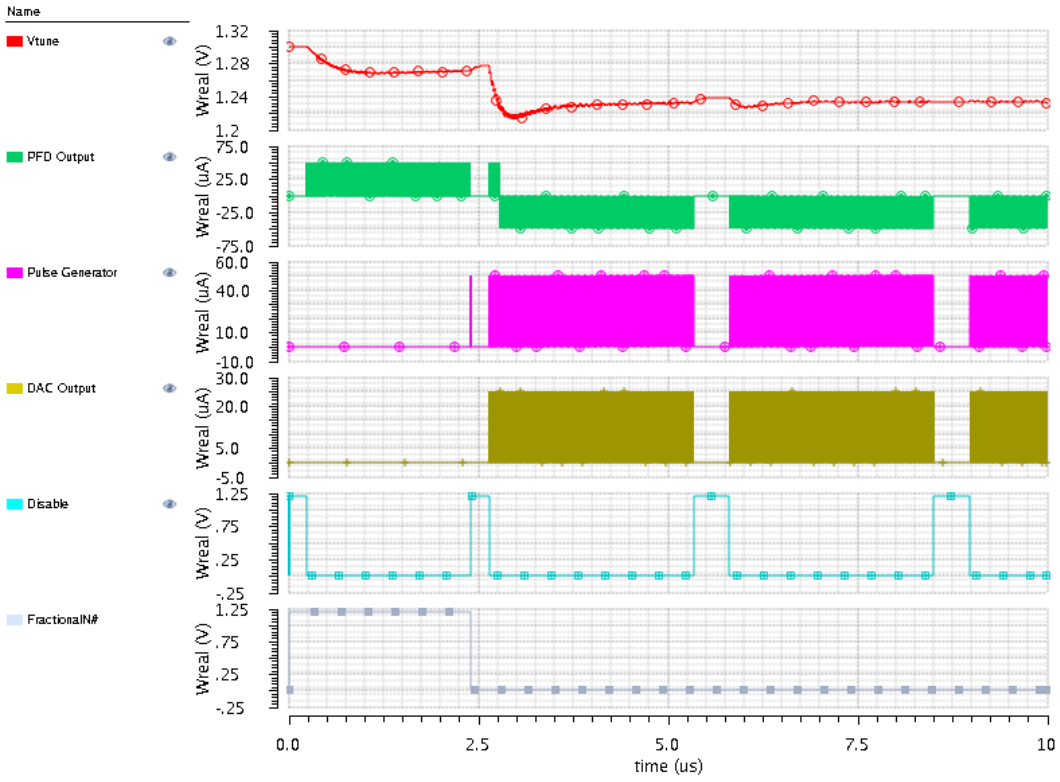


Figure 17: System-level transient results.

System lock is most easily seen in the VCO tune voltage, which first settles to 1.27V in integer mode. The Fractional# signal goes low at 2.4µs, which turns on the pulse generator. As expected, the VCO tune voltage adjusts so the PFD output creates current pulses of opposing the pulse generator. The disable signal puts all sources in tri-state while the beat frequency goes from high-to-low pulse width.

I. Layout

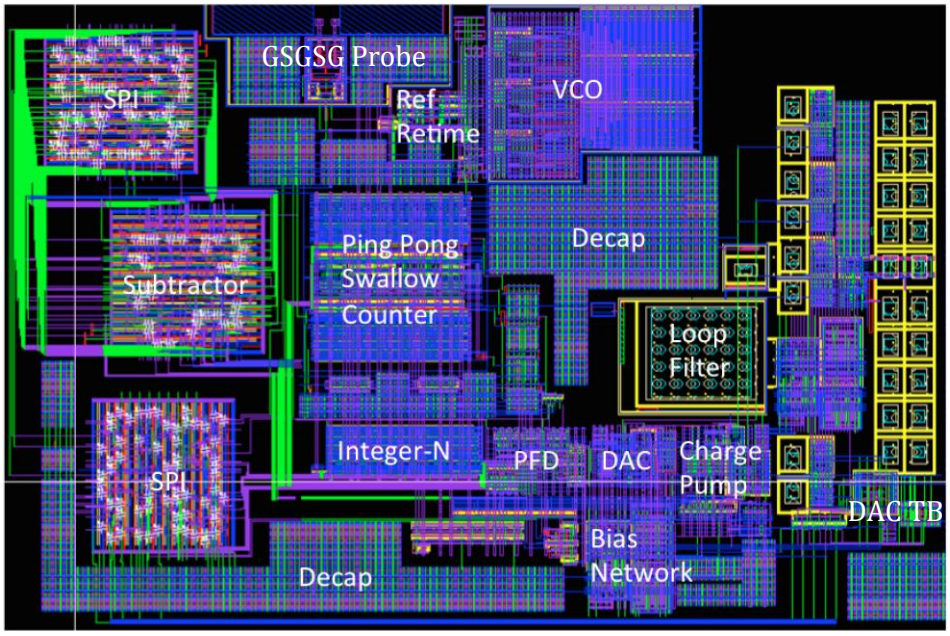


Figure 18: Completed IC layout.

Layout of M1-M4 of the entire chip is shown in Figure 18. M5-M8 were all used for a power grid that covered the entire chip. A unit size 1pF MOS decoupling capacitor was arrayed in any open space to provide over 200pF of on-chip supply noise suppression. To isolate the digital switching noise from the analog current sources, the pad ring is split so separate AV_{DD} and DV_{DD} can be brought in. A separate pad is also dedicated to the $VCOV_{DD}$ for the same purpose.

The VCO output is available through an exposed-metal GSGSG probe with 100Ω differential output drivers. The VCO signal is also routed through 10 flip-flops to a standard I/O pad to view $f_{OUT}/1024$. A full parasitic extraction (PEX) was performed on the VCO and the interconnect capacitance was reported on the order 100fF as opposed to the 20fF initially anticipated. This significantly reduced the frequency range to 1.9-2.3GHz. All components and the loop dynamics are still capable of operating in this range, but the design could have been optimized had the PEX been performed sooner.

VI. Post-Fabrication

A. Testing Setup

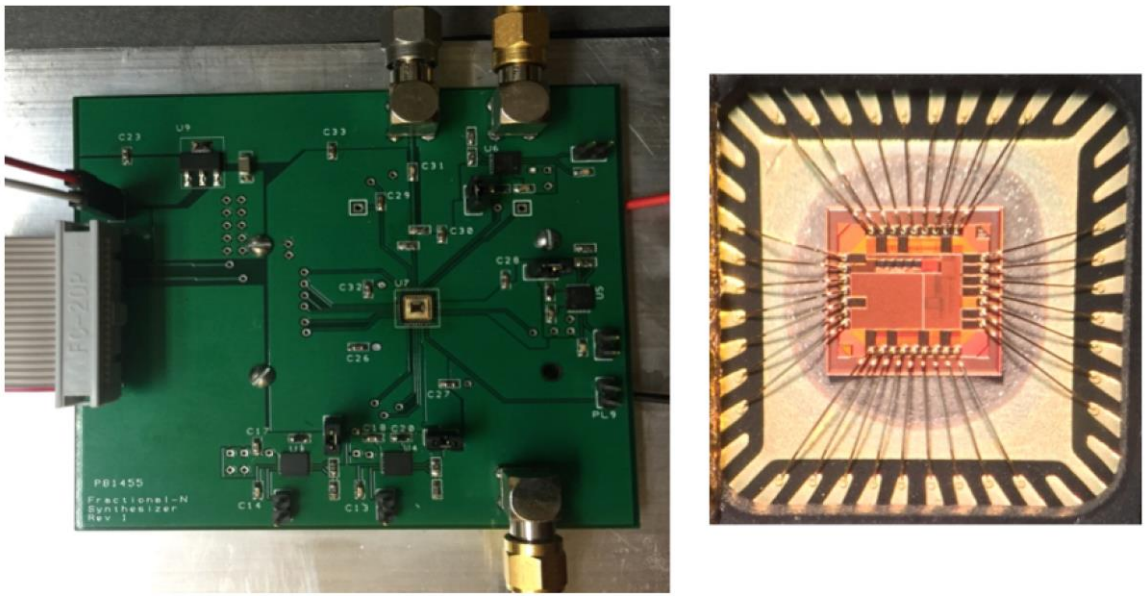


Figure 19: Prototype PCB (left) for testing the fractional-N integrated circuit (right).

The custom PCB shown in Figure 19 was designed to house the integrated circuit for testing. Several identical regulators are used to isolate noise on AV_{DD}, DV_{DD}, and $VCOV_{DD}$. The SMAs carry in the reference oscillator and carry out V_{TUNE} and the $f_{OUT}/1024$ signal. The source and sink currents of the test bench DAC are attached to their own transimpedance amplifiers on the PCB, and the voltages are read through an ADC. The ceramic package also has a removal lid for probing f_{OUT} directly on the GSGSG probe. SPI communications are handled over the 0.1" pitch header.

A LabVIEW program allows configurability of all frequency synthesizer controls and sets the test bench DAC through a graphical user interface. Shown in Figure 20, this software connects to a National Instruments data acquisition device to supply MISO, SCLK, and CS, and verify the correct word was previously written on the MOSI line.

Figure 20: LabVIEW graphical user interface for loop configurability and component testing.

B. Results

Functionality of several key components and integer-N locking were achieved, however a critical mistake was discovered after fabrication that prevented locking in fractional-N mode. The feedback divider's reset was left floating instead of being tied to the global reset signal. Because DVDD lines shielded the local reset, any supply noise couples directly to develop a voltage. Integer-N mode occasionally locks as planned but when the nearby ping-pong swallow counters are turned on for fractional-N mode, the supply noise triples and the feedback divider resets every cycle. The divider never outputs a rising edge and the VCO sits at its highest operating frequency. The DAC test bench performed as designed, and locking integer-N confirmed the loop stability, charge pump, PFD, and VCO blocks.

VII. Conclusion and Future Work

A. Summary

The implementation of the proposed analog phase interpolation based PLL was demonstrated in this thesis. This research was motivated by the growing necessity for integrated low-noise frequency synthesizers. The digital pulse generator and current-steering DAC in this novel topology achieve fractional-N resolution without the traditional divider dithering in the feedback path. Simulink modeling influenced the additional of reference retiming and the feedback disable signal to prevent output glitches. The theoretical calculations offer insight to the fractional spurs that might occur from non-idealities and prove the frequency resolution of the 32-bit tune word is preserved. High performance mixed-signal circuits were designed to achieve a 5GHz synthesizer in a 0.13μm CMOS process. Ultimately the tape-out featured an unrecoverable error, but system-level simulations validated the architecture.

B. Future Direction

The phase evolution concept could be further improved without deterministic jitter for low offset frequencies. Similar to a conventional fractional-N, the accumulator could be replaced with a delta sigma that randomizes the LSBs for DAC current pulses. The strength of the output spurs would be converted to high frequency noise that is better filtered by the feedback loop. A similar work has shown the benefits of this in a digital approach that utilizes a time-to-digital converter[9]. The ultimate topology would combine these concepts with an analog loop filter and VCO, to achieve frequency resolution and linearity that a digital controlled oscillator can't achieve.

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