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Carbon Nanotube Based Spike Neuromorphic Devices and Circuits

Author
Shen, Alex

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Carbon Nanotube Based

Spike Neuromorphic Devices and Circuits

A dissertation submitted in partial satisfaction of the

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in Mechanical Engineering

by

Alex Ming Shen

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ABSTRACT OF THE DISSERTATION

Carbon Nanotube Based

Spike Neuromorphic Devices and Circuits

by

Alex Ming Shen

Doctor of Philosophy in Mechanical Engineering

University of California, Los Angeles, 2014

Professor Yong Chen, Chair

Fabrication and operation of carbon nanotube (CNT) based electronic devices called "synapstors," with the goal of emulating the functions of biological synapses, are reported. These synapstors have a structure akin to field-effect transistors, utilizing a random network of single-wall semiconducting CNTs as its conducting channel. Analog spike signal processing with low power consumption was demonstrated. These synaptic devices are capable of carrying out logic, learning, and memory functions, all in a single element. Analog spike neuromorphic circuits, composed of CNT synapstors and integrate-and-fire (I&F) circuits, are also reported. A positive voltage spike, applied on the gate electrode of a synapstor, could generate a postsynaptic current (PSC) via the CNT channel of the device. Multiple input spikes could be applied on individual CNT synapstors, which could be either excitatory or inhibitory and be connected in a neuromorphic circuit, inducing excitatory or inhibitory PSCs, respectively. These PSCs flow

collectively to an I&F circuit, triggering output spikes. Such neuromorphic circuits are capable of emulating biological neural networks, enabling parallel signal processing, dynamic learning, and memory functions with low power consumption.

The dissertation of Alex Ming Shen is approved.

Chih-Ming Ho

Pei-Yu Chiou

Yu Huang

Yong Chen, Committee Chair

University of California, Los Angeles

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VITA

Alex Ming Shen graduated from Marin Academy High School, San Rafael, California, in June 2004. He enrolled at the University of California, Los Angeles later in 2004. He received a Bachelor of Science with a major in Mechanical Engineering from the University of California, Los Angeles in June 2009. Later that year, in September 2009, Alex entered the Graduate School in the Department of Mechanical Engineering at the University of California, Los Angeles. In December 2011, Alex received a Master's of Science degree in Mechanical Engineering from the University of California, Los Angeles. He received a Certificate of Leadership in the Business of Science from the University of California, Los Angeles in June 2013.

Alex participated in the Center for Scalable and Integrated Nanomanufacturing (SINAM) Summer Research Program at the University of California, Los Angeles and the University of California, Berkeley during the summers from 2005 through 2008. In 2010, he worked as a Research Associate in the Information & Quantum Systems Research Lab (Dr. Zhiyong Li's group) at Hewlett-Packard Labs. Alex has done some work as a Global Scholar and Consultant with PreScouter, Inc. He became involved with the nonprofit organization, World Possible, in September 2013, working on Business Development and Product Innovation. Alex was a core member of the Business of Science Center at the University of California, Los Angeles from September 2012 until June 2014. One of his contributions to the Business of Science Center was acting as a coordinator for the Venture Team Program. In this capacity, Alex mentored the winning teams of the 2013 and 2014 Venture Team Competition.

PUBLICATIONS AND POSTERS

A. M. Shen, C-L Chen, K. Kim, B. Cho, A. Tudor, Y. Chen, Analog Neuromorphic Module Based on Carbon Nanotube Synapses, *ACS Nano*, 6117-6122 (2013)

B. Cho, K. Kim, C-L Chen, A. M. Shen, Q. Truong, Y. Chen, Nonvolatile Analog Memory Transistor Based on Carbon Nanotubes and C60 Molecules, *Small*, 1-5 (2013)

K. Kim, C-L Chen, Q. Truong, A. M. Shen, Y. Chen, A Carbon Nanotube Synapse with Dynamic Logic and Learning, *Advanced Materials,* 1693-1698 (2013)

C-L Chen, K. Kim, Q. Truong, A. M. Shen, Y. Chen, A Spiking Neuron Circuit Based on a Carbon Nanotube Transistor, *Nanotechnology*, 1-6 (2012)

C-L Chen, K. Kim, Q. Truong, A. M. Shen, Z. Li, Y. Chen, Hydrogen Doped Carbon Nanotube Transistor for Biological Neuron Circuit Applications, *MRS Fall Meeting*, Poster in *Carbon Nanomaterials session* (2012)

CHAPTER 1: INTRODUCTION

1.1. Neuromorphic Devices and Circuits

The human brain is capable of processing massive amounts of information, all while consuming less than 100 W of power. The brain's neural network is composed of billions of neurons, each connected to up to 10,000 other neurons. Millisecond-long potential pulse input signals are passed from neuron to neuron, through trillions of synaptic connections. These input spikes trigger dynamic analog postsynaptic currents (PSC) in the neurons, with duration from a few milliseconds to seconds. When the resulting PSC drives the neural potential above a threshold value, output spikes will be emitted by the neuron.[1,2] There have been many attempts to emulate the brain's parallel processing architecture, utilizing various methods. Supercomputers have been used to perform simulations of the neural network, but were not able to match the signal processing speed or the low power consumption of the biological model.[1,3,4] Silicon (Si)-based circuits have been used to emulate the neural network, but consumed considerably more energy and were unable to be scaled up to a size comparable with the biological model.[5,6,7,8,9] There have been numerous attempts to emulate the functions of neurons and synapses through the use of various electronic devices, such as floating gate silicon transistors,[10] nanoparticle organic transistors,[11] resistive switches,[12,13] memristors,[14,15] phase change memory, and CNT transistors.[2,16,17,18] While these devices consume less power than the supercomputers or Si-based circuits, it is still substantially higher than that of the biological neural network.[5,11,19,20] In recent years, CNTs have become a popular alternative to Si in nanoscale electronic devices due to their nanoscale size and desirable electronic properties. CNT

transistors are the most promising amongst the electronic devices due to their scalability, lower power consumption, and compatibility with complementary metal-oxide-semiconductor (CMOS) technology.

We have developed an analog spike neuromorphic circuit, which is comprised of CNT based synaptic devices and a silicon based integrate-and-fire (I&F) circuit, to emulate the biological neural network. The CNT based synaptic devices have a structure similar to that of a field-effect transistor, with a random network of single-wall semiconducting CNTs as its conductive channel. Applying a voltage spike on the gate electrode of the CNT based synaptic device generates a PSC via the CNT channel. This PSC flows to an I&F circuit, triggering output spikes. Such neuromorphic circuits could be scaled up to emulate the biological neural network, in which neurons are connected to one another through synapses (**Figure 1.1a** and **b**). As described in this dissertation, the CNT based synaptic devices emulate biological synapses (**Figure 1.1c**), based on a random CNT network (**Figure 1.1d**), and silicon (Si) based I&F circuits, analogous to axons, emulate the biological synapses fairly well.[21]

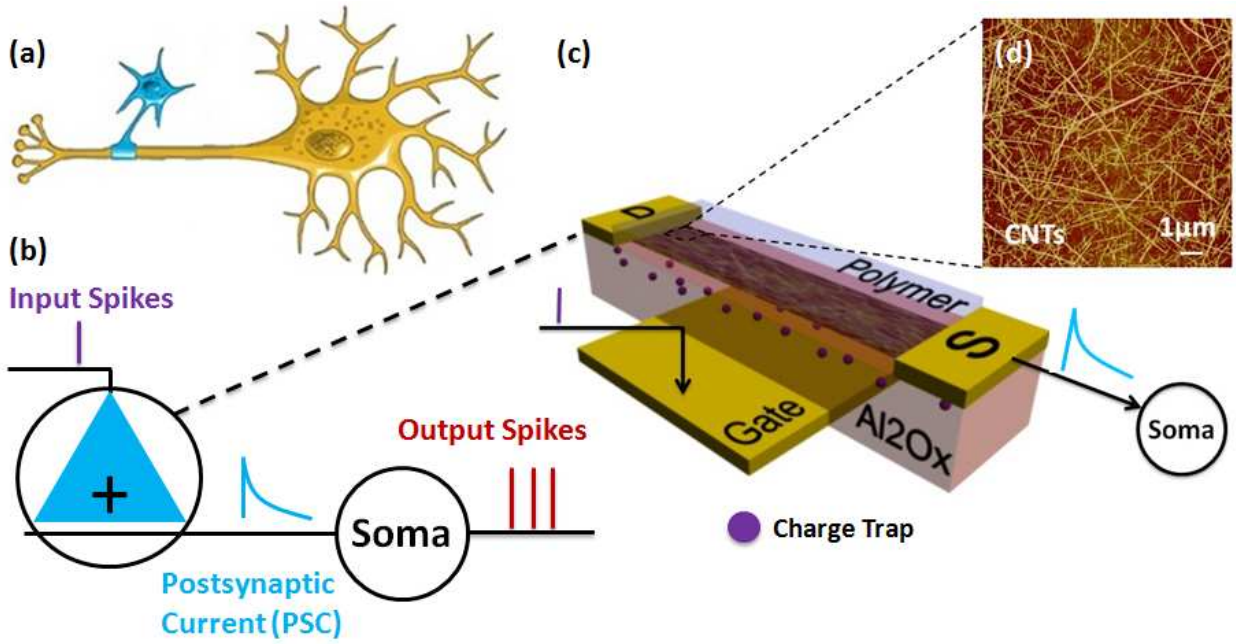

Figure 1.1. (a) A schematic of a simple biological network, showing one neuron (blue) connected to another neuron (yellow) through a synapse. (b) A schematic of a neuromorphic circuit, composed of a carbon nanotube (CNT) based synaptic device and an integrate-and-fire (I&F) circuit. In this case, the CNT synaptic device is excitatory (blue "+" triangle). Applying an input spike on the CNT synaptic device will generate an excitatory postsynaptic current (EPSC). The dynamic postsynaptic current (PSC) flows to the I&F circuit, triggering output spikes. (c) A schematic of a CNT synaptic device, with a channel composed of a random network of CNTs, bookended by source (S) and drain (D) electrodes. An aluminum oxide layer, with charge traps, acts as the device's dielectric layer. Applying an input spike on the gate electrode generates a dynamic PSC, via the transistor channel, which flows to the I&F circuit. (d) An atomic force microscope (AFM) image of a random CNT network, comprising the transistor channel.

1.2. Carbon Nanotube Field-Effect Transistor

A field-effect transistor (FET) allows for modification of the conductivity via a gate electric field. This channel is comprised of a either electrons (n-type) or holes (p-type) in a semiconducting material, meaning that the current through the device is due to either electrons or holes. The channel is bookended by ohmic-contacted source and drain electrodes, and biased at the middle by a gate electrode. Varying the gate potential varies the channel conductivity.[22]

In the case of a FET with an n-type channel, electrons are the charge carriers. Applying a negative voltage bias on the device's gate electrode repels electrons away from the conductive channel, creating a depletion region, narrowing the path through which carriers can flow. If this depletion region becomes large enough, it can block the path of the charge carriers, essentially turning off the device. Applying a positive voltage bias on the device's gate electrode increases the electron concentration in the conductive channel, widening the path through which charge carriers can flow, increasing the device current. In FETs with p-type channels, holes are the charge carriers. Applying a negative voltage bias on the device's gate electrode will increase the hole concentration in the conductive channel, widening the path through which charge carriers can flow, increasing the device current. Applying a positive voltage bias on the device's gate electrode will push holes away from the conductive channel, decreasing the carrier concentration, narrowing the path through which charge carriers can flow, decreasing the device current, with the potential to turn the device off entirely.

The use of carbon nanotubes as the conductive material in FETs, instead of the bulk silicon that is traditionally used in metal-oxide-semiconductor field-effect transistor (MOSFET) structures, has become popular due to their superior electrical characteristics. CNT FETs have

near-ballistic transport properties, allowing for the fabrication of high-speed devices.[23] In our work, a random network of single-wall semiconducting CNTs is used as the conductive channel.

1.3. Integrate-and-Fire Circuits

The integrate-and-fire (I&F) circuit is made up of about twenty silicon (Si) transistors and a capacitor.[21] The circuit can be subdivided into three main elements: a capacitor, a comparator, and a reset transistor. A schematic of the I&F circuit is shown in **Figure 1.2**. Postsynaptic currents (PSC) are triggered by input pulses applied on synaptic transistors and sent to the I&F circuit. These PSCs are accumulated on the capacitor, and potential on the capacitor gradually increases with the charge on the capacitor, which is proportional to the integration of the PSC against time. When the potential on the capacitor is increased to a preset reference threshold value, V_{th}, the output potential of the comparator is switched from low (0 V) to high (5 V) potential. The high output potential turns on the reset transistor, which releases the charge stored on the capacitor and resets the output potential back to low potential. When this happens, an output spike is generated, and the integration of the PSC on the capacitor also restarts from zero again. Two invertors, with positive feedback and adjustable slew-rate, are included in the comparator for setting the width and refractory period of the output spikes. The average power consumption of the I&F circuit is ~1 μW.

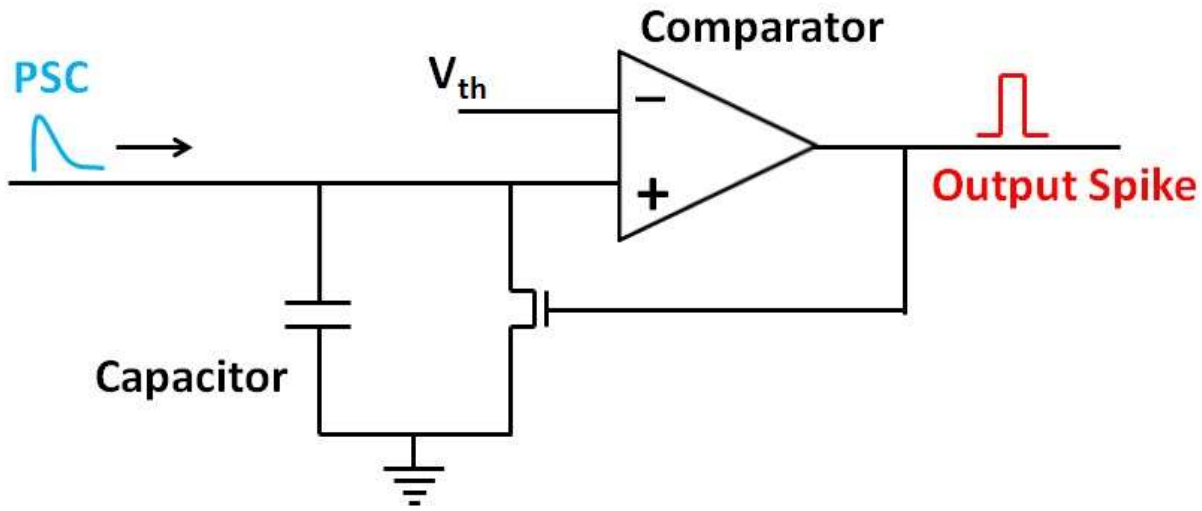

Figure 1.2. A schematic showing the structure of the integrate-and-fire circuit.

1.4. Measurement Setup of the Neuromorphic Module

A custom circuit measurement setup was developed to test the neuromorphic modules. A schematic of this measurement setup is shown in **Figure 1.3**. A field programmable gate array (FPGA) is used to apply input spikes on the gate electrodes of carbon nanotube (CNT) synapstors. Positive source-drain electrode voltages, V_{ds}, were applied on excitatory CNT synapstors, inducing excitatory postsynaptic currents (EPSC). Negative source-drain electrode voltages were applied on inhibitory CNT synapstors, inducing inhibitory postsynaptic currents (IPSC). The postsynaptic currents (PSC) generated by the CNT synapstors flow to an integrate-and-fire (I&F) soma circuit composed of silicon (Si) transistors and a capacitor.[18] When there are multiple CNT synapstors connected together in the neuromorphic module, the EPSCs and IPSCs generated by excitatory and inhibitory CNT synapstors flow collectively to the I&F soma circuit. The PSCs, induced by the input spikes applied on the CNT synapstors, were measured by

analog-to-digital converters (ADC). The total PSC is amplified and integrated, with respect to time, by a capacitor in the I&F circuit. When the PSC integration reaches a preset threshold value, an output spike is triggered and the PSC integration starts over again from zero. The output spike frequency increases monotonically with increasing PSC. The input spikes and output spikes were also measured using ADCs.

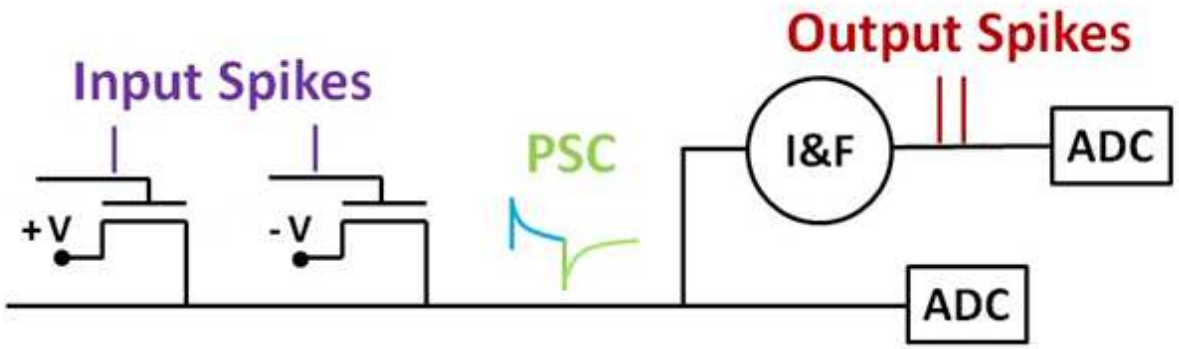

Figure 1.3. A schematic showing the measurement system of a neuromorphic circuit. Input spikes are applied to the CNT synaptic devices, which can be excitatory (+V source-drain voltage) or inhibitory (-V source-drain voltage). Dynamic postsynaptic currents (PSC) are generated via the devices' conductive channels. The excitatory PSCs, from the excitatory CNT synaptic devices, and the inhibitory PSCs, from the inhibitory CNT synaptic devices, are measured by an analog-to-digital converter (ADC) and flow collectively to an integrate-and-fire (I&F) circuit. The I&F circuit generates output spikes, which are also measured by an ADC.

1.5. Roadmap of Thesis

In the following chapters, I present two different carbon nanotube (CNT) based synaptic devices, called “synapstors,” with the goal of emulating the biological synapse. These synapstors have a structure similar to that of a field-effect transistor. The device channel is comprised of a random network of single-wall p-type semiconducting CNTs, and the dielectric layer is made of aluminum oxide (Al_2O_3), deposited by atomic layer deposition (ALD) at 250 C. These synapstors are integrated, with silicon (Si) based integrate-and-fire (I&F) circuits, into neuromorphic circuits in order to emulate the biological neural network. Chapter 2 discusses a CNT/In+ synapstor, in which Indium (In) ions are implanted into the dielectric layer. Chapter 3 presents a doping modulated CNT synapstor, in which half of the device channel has been converted from p-type to n-type, creating a p-n junction in the CNT channel. Finally, Chapter 4 summarizes the findings.

References:

1. Koch, C., Computation and the Single Neuron. *Nature* 1997, *385*, 207-210.
2. Byrne, J.; Byrne, J. H.; Roberts, J. L., *From Molecules to Networks: an Introduction to Cellular and Molecular Neuroscience*. Academic Press: 2009, pp. 470, 478, 544-545.
3. Fischetti, M., Graphic Science: Computers *vs*. Brains. *Scientific American Magazine* **2011**, *305*, 104-104.
4. Watson, A., Why Can't a Computer be More Like a Brain? *Science* **1997**, *277*, 1934-1936.
5. Indiveri, G.; Chicca, E.; Douglas, R., A VLSI Array of Low-Power Spiking Neurons and Bistable Synapses with Spike-Timing Dependent Plasticity. *IEEE Trans. Neural Netw.* **2006**, *17*, 211-221.
6. Arthur, J. V.; Boahen, K. A., Silicon-Neuron Design: A Dynamical Systems Approach. *IEEE Trans. Circuits Syst. I* **2011**, *58*, 1034-1043.
7. Mahowald, M.; Douglas, R., A Silicon Neuron. *Nature* **1991**, *354*, 515-518.
8. Poon, C. S., Neuromorphic silicon neurons and large-scale neural networks: challenges and opportunities. *Frontiers in neuroscience* **2011**, *5*.
9. Pickett, M. D.; Medeiros-Ribeiro, G.; Williams, R. S., A Scalable Neuristor Built with Mott Memristors. *Nature Mater.* **2013**, 12, 114-117.
10. Ramakrishnan, S.; Hasler, P. E.; Gordon, C., Floating Gate Synapses with Spike-Time-Dependent Plasticity. *IEEE Trans. Biomed. Circuits and Systems* **2011**, *5*, 244-252.
11. Alibart, F.; Pleutin, S.; Guérin, D.; Novembre, C.; Lenfant, S.; Lmimouni, K.; Gamrat, C.; Vuillaume, D., An Organic Nanoparticle Transistor Behaving as a Biological Spiking Synapse. *Adv. Funct. Mater.* **2010**, *20*, 330-337.

12. Kuzum, D.; Jeyasingh, R. G.; Lee, B.; Wong, H.-S. P., Nanoelectronic Programmable Synapses Based on Phase Change Materials for Brain-Inspired Computing. *Nano Lett.* **2011**, *12*, 2179-2186.
13. Hasegawa, T.; Ohno, T.; Terabe, K.; Tsuruoka, T.; Nakayama, T.; Gimzewski, J. K.; Aono, M., Learning Abilities Achieved by a Single Solid□State Atomic Switch. *Adv. Mater.* **2010**, *22*, 1831-1834.
14. Park, H.; Afzali, A.; Han, S.-J.; Tulevski, G. S.; Franklin, A. D.; Tersoff, J.; Hannon, J. B.; Haensch, W., High-Density Integration of Carbon Nanotubes *via* Chemical Self-Assembly. *Nat. Nanotechnol.* **2012**, *7*, 787-791.
15. Erokhin, V.; Berzina, T.; Camorani, P.; Smerieri, A.; Vavoulis, D.; Feng, J.; Fontana, M. P., Material Memristive Device Circuits with Synaptic Plasticity: Learning and Memory. *J. Bionanosci.* **2011**, *1*, 24-30.
16. Kim, K.; Chen, C. L.; Truong, Q.; Shen, A. M.; Chen, Y., A Carbon Nanotube Synapse with Dynamic Logic and Learning. *Adv. Mater.* **2013**, 25, 1693-1698.
17. Chen, C.; Kim, K.; Truong, Q.; Shen, A.; Li, Z.; Chen, Y., A Spiking Neuron Circuit Based on a Carbon Nanotube Transistor. *Nanotechnology* **2012**, *23*, 275202.
18. Joshi, J.; Zhang, J.; Wang, C.; Hsu, C.-C.; Parker, A. C.; Zhou, C.; Ravishankar, U., A Biomimetic Fabricated Carbon Nanotube Synapse for Prosthetic Applications. *IEEE LiSSA Workshop* **2011**, pp. 139-142.
19. Nayak, A.; Ohno, T.; Tsuruoka, T.; Terabe, K.; Hasegawa, T.; Gimzewski, J. K.; Aono, M., Controlling the Synaptic Plasticity of a Cu2S Gap□Type Atomic Switch. *Adv. Funct. Mater.* **2012**, *22*, 3606-3613.

20. Chen, Y.; McDaid, L.; Hall, S.; Kelly, P., A Programmable Facilitating Synapse Device. *IEEE Int. Joint Conf. on Neural Netw.* **2008**, pp. 1615-1620.
21. Indiveri, G., In A Low-Power Adaptive Integrate-and-Fire Neuron Circuit. *IEEE Int. Symp. Circuits Syst.* **2003**, pp. IV-820-IV-823 vol. 4.
22. Millman, J., *Electronic devices and circuits*. Singapore: McGraw-Hill: 1985. pp. 384-385.
23. Dai, H., Electrical Properties and Field-Effect Transistors of Carbon Nanotubes. *Nano: Brief Reports and Reviews* **2006**, *1*, 1.

CHAPTER 2: CNT/IN+ SYNAPSTORS

2.1. Introduction

We report a carbon nanotube (CNT) based synapstor, which can be incorporated into an analog neuromorphic module. The CNT/In+ synapse has a structure similar to a field-effect transistor. The device channel is composed of a random network of p-type CNTs. Indium (In) ions are implanted into the aluminum oxide (Al_2O_3) dielectric layer. Electrons move from the CNT channel into the Al_2O_3 dielectric layer when a positive voltage spike is applied on the gate electrode of the CNT/In+ synapstor. These electrons become trapped in the defect sites created by the implanted In ions, and the concentration of hole carriers in the CNT channel increases. After the spike, the electrons gradually move back to their original locations, decreasing the hole concentration in the CNT channel. This interaction induces a dynamic postsynaptic current (PSC) in the CNT channel. These CNT/In+ synapstors can be either excitatory or inhibitory, and can generate excitatory PSCs or inhibitory PSCs, respectively. PSCs generated by CNT/In+ synapstors flow to an integrate-and-fire (I&F) circuit, which generates output spikes. We analyze the relationship between the input and output spikes of the neuromorphic module. The neuromorphic module could be scaled up to emulate the biological neural network, capable of parallel signal processing with low power consumption.

2.2. CNT/In+ Synapstor Fabrication

A schematic of the CNT/In+ synapstor is shown in **Figure 2.1**. The synapstor is fabricated on a silicon (Si) wafer with a 300-nm-thick layer of thermally grown silicon dioxide

(SiO_2) on top. The back gate is composed of a 15-nm-thick layer of titanium (Ti) and a 100-nm-thick layer of aluminum (Al), both deposited via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. The device's dielectric layer is comprised of a 20-nm-thick layer of aluminum oxide (Al_2O_3), deposited by atomic layer deposition (ALD) at 250C. This layer of Al_2O_3 is patterned using polyimide (PI) and AZ 5214 photoresist, then etched using a solution of 4% phosphoric acid mixed with 96% deionized water. Indium (In) ions are implanted into the Al_2O_3 layer by INNOViON Corporation. Once this is done, ALD is used to deposit a layer of 5-nm-thick Al_2O_3 onto the sample at 250C, which is then patterned and etched in similar fashion. Following the deposition of a monolayer of (3-Aminopropyl)triethoxysilane (APTES) onto the surface of the Al_2O_3 layer, a random network of single-wall p-type semiconducting CNTs is deposited onto the surface of the APTES-coated Al_2O_3 via spin coating. This CNT network is patterned, using AZ 5214 photoresist and oxygen plasma etching, to form a 15-µm-wide and 20-µm-long transistor channel. The CNT transistor channel is connected with source and drain electrodes, composed of a 10-nm-thick layer of Ti and an 80-nm-thick layer of gold (Au), deposited via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. Finally, a 2-µm-thick layer of SU-8 polymer was deposited and patterned to cap the entire CNT channel area.

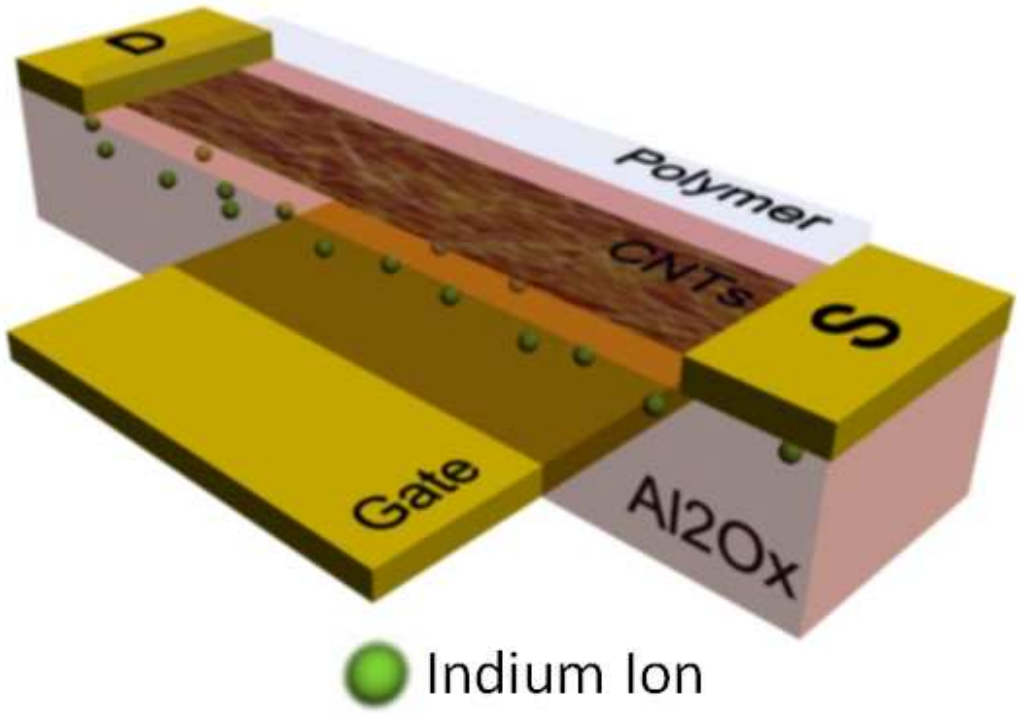

Figure 2.1. A schematic of a CNT/In+ synapstor, with a channel composed of a random carbon nanotube (CNT) network, bookended by source (S) and drain (D) electrodes. Indium ions are implanted into an aluminum oxide (Al_2O_3) dielectric layer.

2.3. Device Physics

When a positive voltage spike is applied on the aluminum (Al) back gate of the CNT/In+ synapstor, electrons are attracted away from the carbon nanotube (CNT) channel and into the aluminum dioxide (Al_2O_3) dielectric layer. These electrons become trapped locally near the defects in the Al_2O_3 dielectric layer, created by the implanted indium (In) ions. When this

happens, the hole concentration in the p-type CNT channel increases, thereby increasing the current through the CNT channel. After the spike is removed, the electrons are gradually released from the dielectric layer. As electrons return from the Al_2O_3 dielectric layer to their original locations near the CNT channel, the concentration of holes in the CNT channel decreases. As this happens, the current through the CNT channel will gradually decrease, returning to its initial baseline value. This is what generates a dynamic postsynaptic current (PSC) through the CNT channel. When a positive source-drain electrode voltage, V_{ds} = 0.2 V, is applied to the CNT/In+ synapstor, a positive voltage spike applied on the gate electrode induces an excitatory PSC (EPSC), and the CNT transistor functions as an excitatory synapse. When a negative source-drain electrode voltage, V_{ds} = -0.2 V, is applied to the CNT/In+ synapstor, a positive voltage spike induces an inhibitory PSC (IPSC), and the CNT transistor functions as an inhibitory synapse.

The PSC, generated from the CNT/In+ synapstor, flows toward an integrate-and-fire (I&F) circuit. The PSC is amplified and integrated with respect to time by a capacitor in the I&F circuit. When the PSC is below a preset threshold current, no output spikes are generated by the I&F circuit. When the PSC is increased above the preset threshold current, an output spike is triggered, and the PSC integration starts over again from zero.[1] The output spike rate increases nonlinearly with increasing PSC. The input spike, PSC, and output spikes of the neuromorphic module can be measured by analog-to-digital converters (ADC). The operation of a typical excitatory CNT/In+ synapstor, inducing an EPSC can be seen in **Figure 2.2**.

When multiple spikes with amplitude of 5 V and duration of 1 ms were applied on the gate electrodes of multiple CNT/In+ synapstors, connected in a neuromorphic module, the EPSCs and IPSCs generated by sets of excitatory and inhibitory synapses flow jointly toward an

I&F circuit in parallel. The total PSC is amplified and integrated with respect to time by a capacitor in the I&F circuit. When the total PSC is below a preset threshold current, no output spikes are generated by the I&F circuit. When the total PSC is increased above the preset threshold current, an output spike is triggered, and the PSC integration starts over again from zero. The output spike rate increases nonlinearly with increasing PSC. The input spikes, PSC, and output spikes of the neuromorphic module can be measured by ADC.

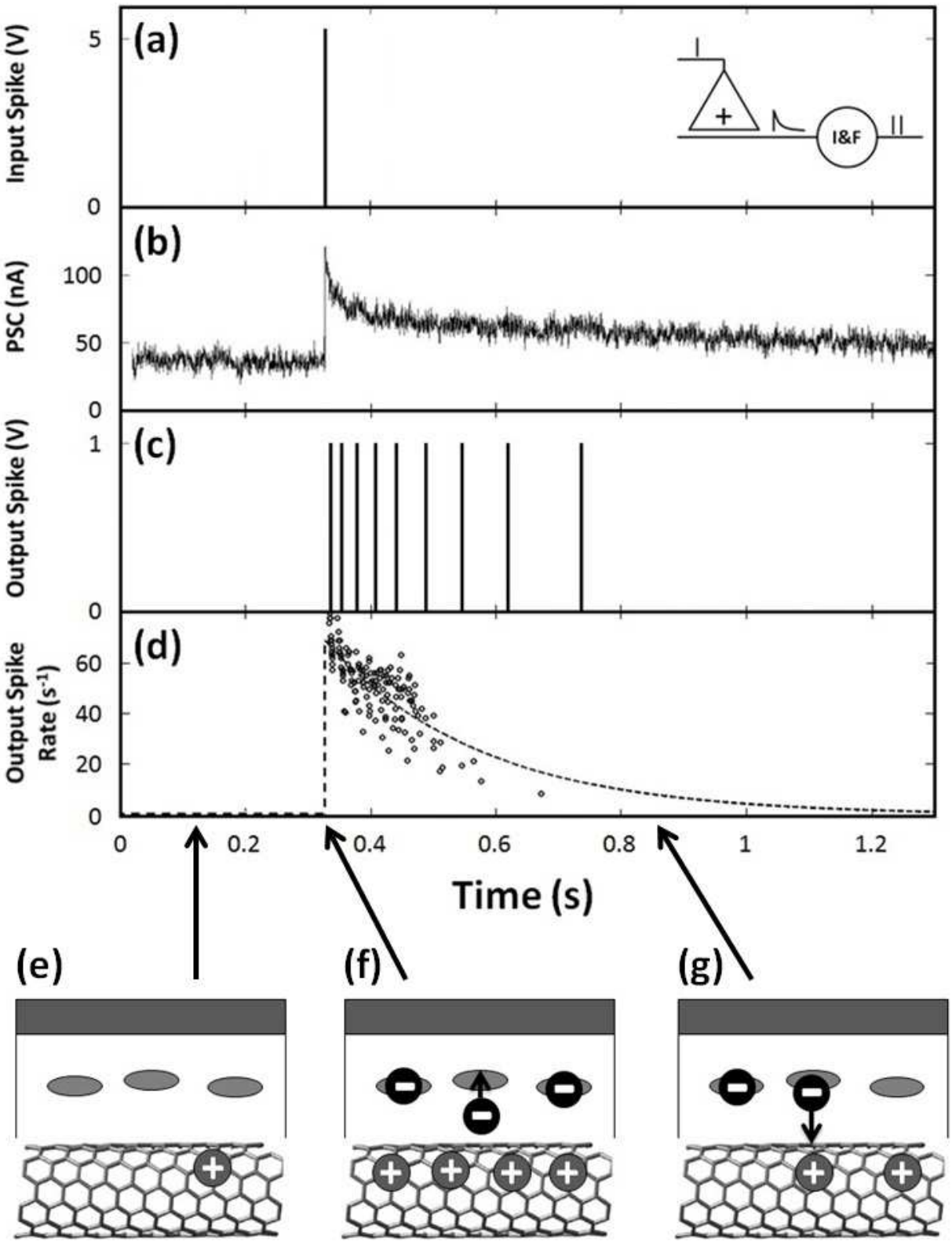
(a)
Input Spike (V)
5
0
I
+
I&F
II
(b)
PSC (nA)
100
50
0
(c)
Output Spike (V)
1
0
(d)
Output Spike Rate (s-1)
60
40
20
0
0
0.2
0.4
0.6
0.8
1
1.2
Time (s)
(e)
(f)
(g)

Figure 2.2. (a) A single input spike is applied on an excitatory CNT/In+ synapstor. The inset is a schematic showing a neuromorphic circuit, where an input spike, applied on an excitatory CNT/In+ synapstor ("+" triangle), generates an excitatory postsynaptic current (EPSC), triggering output spikes via the integrate-and-fire (I&F) circuit. (b) The EPSC is plotted versus time. (c) The series of output spikes, generated by the I&F circuit, is shown versus time. (d) The firing rate of output spikes, from 20 individual trials, is shown versus time. The dashed line represents the best fit of the plotted data. (e) A schematic showing hole carriers ("+" circle) in the p-type CNT channel before an input spike is applied on the CNT/In+ synapstor. (f) A schematic showing the movement of electrons ("-" circles) from the CNT channel into the Al_2O_3 dielectric layer when a positive voltage is applied on the CNT/In+ synapstor. The electrons become trapped in defects induced by the implanted indium (In) ions (grey ovals), increasing the hole concentration in the CNT channel increases. (g) A schematic showing the movement of electrons from the Al_2O_3 dielectric layer back to their original locations near the CNT channel after the spike. This causes a reduction in the hole concentration in the CNT channel.

2.4. Results and Discussion

A typical excitatory carbon nanotube (CNT) synapstor induces an excitatory postsynaptic current (EPSC). The operation of such a CNT/In+ synapstor, operated with a source-drain voltage, V_{ds} = 0.2 V, is described in **Figure 2.3**. A single input spike, with amplitude V_g = 5 V, is applied on the gate electrode of a CNT/In+ synapstor (**Figure 2.3a**), which generates an EPSC (**Figure 2.3b**). The peak amplitude of the EPSC is ~60 nA above the baseline current. After the spike, the device current gradually decays back to the baseline current over a duration of approximately 2.0 s. The generated EPSC flows to the integrate-and-fire (I&F) circuit,

generating output spikes (**Figure 2.3c**). As can be seen from **Figure 2.3d**, decreased EPSC results in decreased firing rates of the output spikes. The firing rate of the output spikes continues to decrease until the EPSC decreases below a preset threshold value, V_{th}, that is set in the I&F circuit. When the EPSC becomes smaller than V_{th}, output spikes will no longer be generated. In the case shown in **Figure 2.3**, output spikes are generated for 0.8 s after the input spike is applied to the CNT/In+ synapstor, indicating that it took 0.8 s for the EPSC to decrease below V_{th}. The data presented in **Figure 2.3** is from 20 individual trials, which have been averaged. The firing rate of the output spikes, f(t), versus time, t, can be fitted with the equation, $f(t) = A\ Exp[-\alpha(t-t_0)]*H(t-t_0)$, where t_0 represents the moment at which the input spike is applied on the CNT/In+ synapstor, and H(t) is a unit step function. Fitting the data shown in **Figure 2.3d**, we determined that $A = 70.2\ s^{-1}$ and $\alpha = 4.1\ s^{-1}$. The leakage current through the gate of the CNT/In+ synapstor is $<10^{-12}$ A and can therefore be neglected, as can the power consumption induced by the input spike applied on the device's gate electrode. The average EPSC of a CNT/In+ synapstor, generated by a single spike, is ~30 nA. The average power consumption of the CNT/In+ synapse is estimated to be 0.2 V x 30 nA = 6 nW/spike.

A reference device was fabricated in parallel with the CNT/In+ synapstor. The structure of the reference device is similar to that of the CNT/In+ synapstor, except that no In ions were implanted in the Al_2O_3 dielectric layer. An input spike, applied on the gate electrode of the control device, did not generate any obvious PSC. The source-drain current of the control device immediately returned to its baseline current value after the spike. Based upon the experimental results, the PSC generated by the CNT/In+ synapstor is related to the In ions that were implanted in the Al_2O_3 dielectric layer. The generated PSC is due to the dynamic response of a CNT/In+ synapstor. The input spike, applied on the gate electrode of the CNT/In+ synapstor, attracts

electrons from the CNT channel to the Al_2O_3 dielectric layer, where they become trapped in the defects associated with the implanted In ions. This is shown in **Figure 2.3**, The negatively charged electrons in the Al_2O_3 dielectric layer attract positively charged holes in the p-type semiconducting CNTs in the channel. When this happens, the concentration of holes in the CNT channel increases, as does the current through the CNT channel. After the spike, the electrons that were trapped in the Al_2O_3 dielectric layer gradually return to their original locations by the CNTs, causing a gradual decrease in the concentration of holes in the CNT channel. This in turn, will cause the current through the CNT channel to decay. The decay rate of the PSC is determined by the speed at which electrons are able to leak out of the Al_2O_3 dielectric layer. The speed at which electrons leak out of the Al_2O_3 dielectric layer could be influenced by the density of defects in the Al_2O_3 dielectric layer, as well as the layer's thickness.

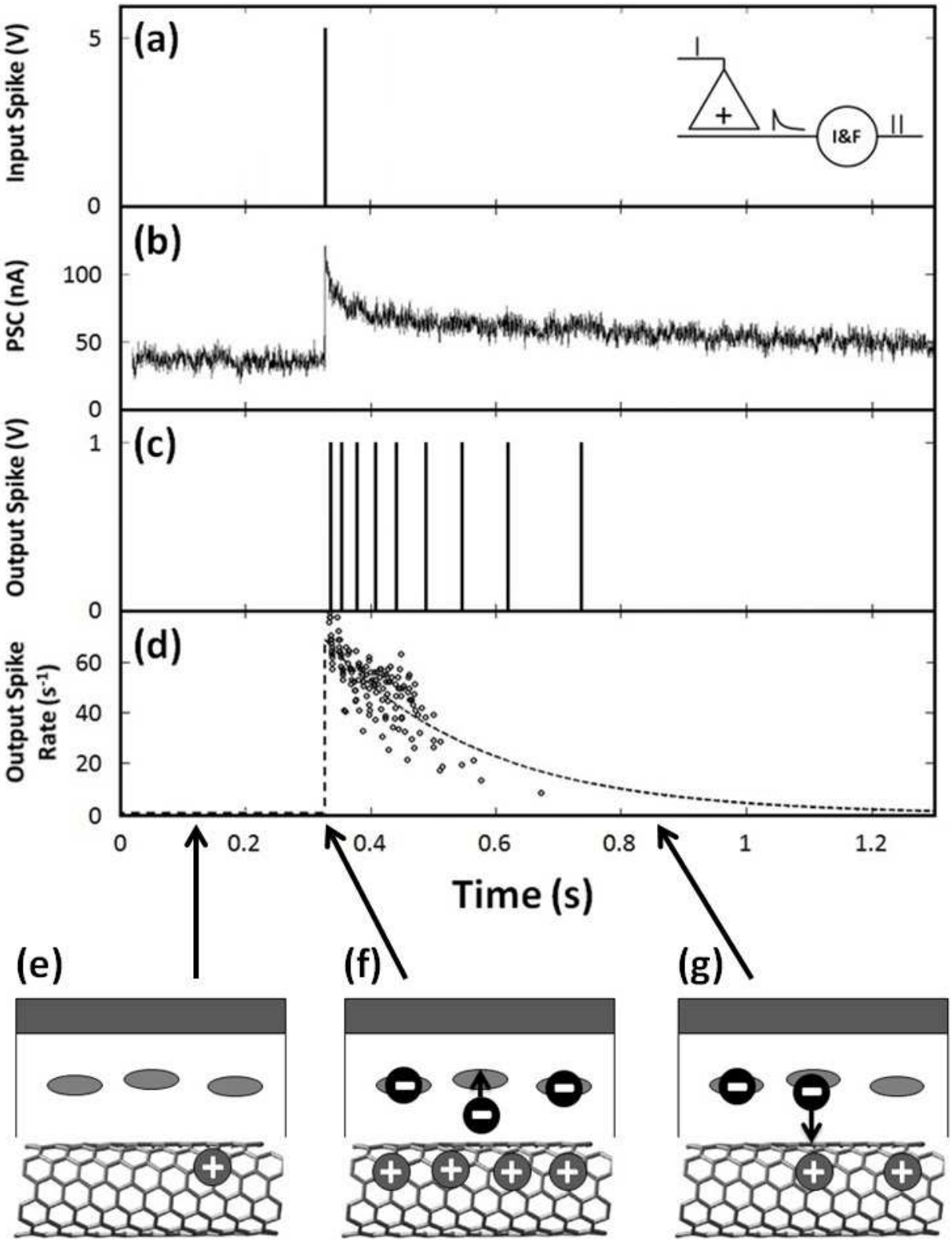
(a)
Input Spike (V)
5
0
I
+
I&F
II
(b)
PSC (nA)
100
50
0
(c)
Output Spike (V)
1
0
(d)
Output Spike Rate (s-1)
60
40
20
0
0
0.2
0.4
0.6
0.8
1
1.2
Time (s)
(e)
(f)
(g)

Figure 2.3. (a) A single input spike is applied on an excitatory CNT/In+ synapstor. The inset is a schematic showing a neuromorphic circuit, where an input spike, applied on an excitatory CNT/In+ synapstor ("+" triangle), generates an excitatory postsynaptic current (EPSC), triggering output spikes via the integrate-and-fire (I&F) circuit. (b) The EPSC is plotted versus time. (c) The series of output spikes, generated by the I&F circuit, is shown versus time. (d) The firing rate of output spikes, from 20 individual trials, is shown versus time. The dashed line represents the best fit of the plotted data. (e) A schematic showing hole carriers ("+" circle) in the p-type CNT channel before an input spike is applied on the CNT/In+ synapstor. (f) A schematic showing the movement of electrons ("-" circles) from the CNT channel into the Al_2O_3 dielectric layer when a positive voltage is applied on the CNT/In+ synapstor. The electrons become trapped in defects induced by the implanted indium (In) ions (grey ovals), increasing the hole concentration in the CNT channel increases. (g) A schematic showing the movement of electrons from the Al_2O_3 dielectric layer back to their original locations near the CNT channel after the spike. This causes a reduction in the hole concentration in the CNT channel.

In the biological model, stimulating a neuron with a pair of input spikes, with different time interval, can test its response to temporally correlated signals.[2] In order to test our neuromorphic module in a similar way, a pair of input spikes was applied on the gate of a CNT/In+ synapstor, generating an EPSC, and inducing output spikes (**Figure 2.4a**). In our experiments, we varied the time interval between the pair of input spikes, Δt, between 1 ms and 40 ms. A pair of spikes with a time interval of 40 ms, applied on an excitatory CNT/In+ synapstor, is shown in **Figure 2.4a**. **Figure 2.4b** shows the EPSC that is generated by the pair of input spikes, which then flows to the I&F circuit, inducing output spikes (**Figure 2.5c**). The

EPSC generated by the second input spike was superimposed on the EPSC generated by the first input spike. Shorter Δt values result in larger increases of the amplitude of the EPSC peak, immediately after the second spike is applied on the gate electrode of the CNT/In+ synapstor. In biological synapses, this type of short-term correlation between the pair of presynaptic spikes is called paired-pulse facilitation (PPF).[3] **Figure 2.4d** shows the rate at which output spikes are fired, f(t), versus time. The data presented is averaged from 20 individual trials, and is fitted by the equation, $f(t) = A_1*\text{Exp}[-\alpha_1(t-t_1)]\ H(t-t_1) + A_2*\text{Exp}[-\alpha_2(t-t_2)]\ H(t-t_2)$, where t_1 and t_2 represent the times at which the first input spike and second input spike are fired, respectively. The best fit of the firing rate of output spikes is shown in **Figure 2.4d** as the dashed line, with $A_1 = 23.5\ s^{-1}$, $\alpha_1 = 0.92\ s^{-1}$, $A_2 = 9.4\ s^{-1}$, and $\alpha_2 = 1.3\ s^{-1}$ when $\Delta t = t_2 - t_1 = 40$ ms. The parameters A_1 and α_1 are associated with the neuromorphic module's response to the first input spike, which does not change against Δt. The parameters A_2 and α_2 were derived from the best fit of the experimental data, as Δt ranged from 1 ms to 40 ms. As Δt increased from 1 ms to 40 ms, the parameter A_2 decreased from $17.8\ s^{-1}$ to $9.4\ s^{-1}$, and the parameter α_2 fluctuated between $0.77\ s^{-1}$ and $20.9\ s^{-1}$ without an observable trend versus Δt.

The experimental results show that parameter A_2 changes versus the Δt. This suggests that the output spikes, triggered by a pair of input spikes, are not simply the linear superposition of output spikes triggered by the two separated input spikes. The short-term memory of the CNT/In+ synapstor could cause parameter A_2 to decrease as Δt increases. Electrons are attracted from the CNT channel into the Al_2O_3 dielectric layer when the first spike is applied on the CNT/In+ synapstor. After the spike, the electrons begin moving back toward the CNT channel, out of the Al_2O_3 dielectric layer. When the second input spike is applied, the electrons are still moving out of the Al_2O_3 dielectric layer, back to their original locations near the CNT channel.

The residual electrons move to the defects located deeper in the Al_2O_3 dielectric layer. When the pair of input spikes is applied on the CNT/In+ synapstor with a smaller time interval, Δt, between them, more electrons could move into the Al_2O_3 dielectric layer. This would result in an increased concentration of holes in the CNT channel, and a larger EPSC generated by the CNT/In+ synapstor.

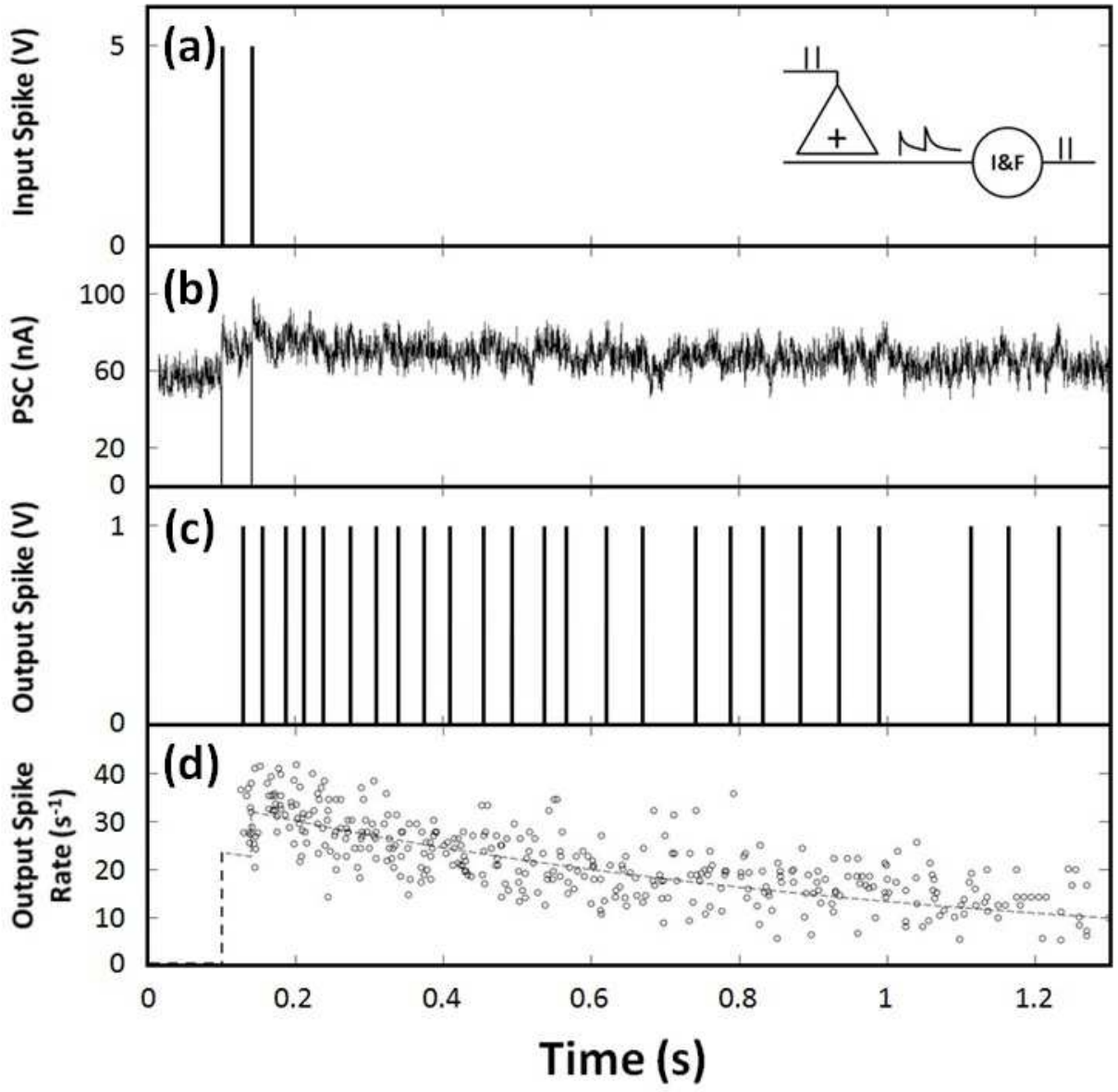

Figure 2.4. (a) A schematic showing a pair of input spikes, 40 ms apart, applied on an excitatory CNT/In+ synapstor. The inset is a schematic showing a neuromorphic circuit, where a pair of input spikes, applied on an excitatory CNT/In+ synapstor ("+" triangle), generates an excitatory postsynaptic current (EPSC), triggering output spikes via the integrate-and-fire (I&F) circuit. (b) The EPSC is plotted versus time. (c) The series of output spikes, generated by the I&F circuit, is shown versus time. (d) The firing rate of output spikes, from 20 individual trials, is shown versus time. The dashed line represents the best fit of the plotted data.

Applying a pair of input spikes on two individual synapses can test the spatiotemporal correlation between the input and output spikes in a neuron. In order to test this in our neuromorphic module, a pair of input spikes is applied to two excitatory CNT/In+ synapstors, each inducing individual EPSCs, which are then summed, and generate output spikes. Two input spikes are applied separately on two excitatory CNT/In+ synapstors, connected in the neuromorphic module, with time interval, Δt = 300 ms (**Figure 2.5a**). **Figure 2.5b** shows the summed EPSC from the two CNT/In+ synapstors, which flows to the I&F circuit, generating output spikes (**Figure 2.5c**). When the EPSCs are summed, the EPSC induced by the second input spike is superimposed onto the EPSC caused by the first input spike, increasing the combined EPSC. The firing rate of the generated output spikes, f(t), increases with the summed EPSC. **Figure 2.5d** shows f(t) versus time, t, from 20 individual trials. The firing rate of the output spikes is fitted with the equation, $f(t) = A_1*\mathrm{Exp}[-\alpha_1(t-t_1)]\ H(t-t_1) + A_2*\mathrm{Exp}[-\alpha_2(t-t_2)]\ H(t-t_2)$, where t_1 and t_2 represent the times at which the first input spike is applied on CNT/In+ synapstor 1 and the second input spike is applied on CNT/In+ synapstor 2, respectively. The best fit of the experimental data, shown as the dashed line in **Figure 2.5d**, indicates that when $\Delta t = t_2$

– t_1 = 300 ms, A_1 = 43.0 s^{-1} and α_1 = 0.99 s^{-1} for the CNT/In+ synapstor 1, and that A_2 = 33.2 s^{-1} and α_2 = 0.29 s^{-1} for the CNT/In+ synapstor 2. The parameters A_1 and α_1 are associated with the neuromorphic module's response to the first input spike, which does not change against Δt. As Δt increased from 5 ms to 300 ms, the parameter A_2 increased from 20.1 s^{-1} to 32.1 s^{-1}, and the parameter α_2 fluctuated between 0.05 s^{-1} and 0.82 s^{-1} without an observable trend versus Δt.

The experimental results show that parameter A_2 changes versus the Δt. This suggests that the output spikes, triggered by a pair of spikes, applied on two excitatory synapses, is not simply the linear superposition of output spikes triggered by the two separated input spikes. The nonlinear correlation between the input and output spikes, when individual input spikes are applied on separate CNT/In+ synapstors, is not the same as that of a pair of spikes applied on a single CNT/In+ synapstor. There is a nonlinear relationship between the generated PSC and the firing rate of output spikes in the I&F circuit, which could cause the parameter A_2 to increase as Δt increases. When Δt is small, larger PSC values appear after the second spike is applied to the CNT/In+ synapstor 2, leading to a smaller increase of the firing rate of the output spikes. This could be due to nonlinear saturation of the I&F circuit, with the output spike firing rate showing saturation behavior with increasing PSC values.

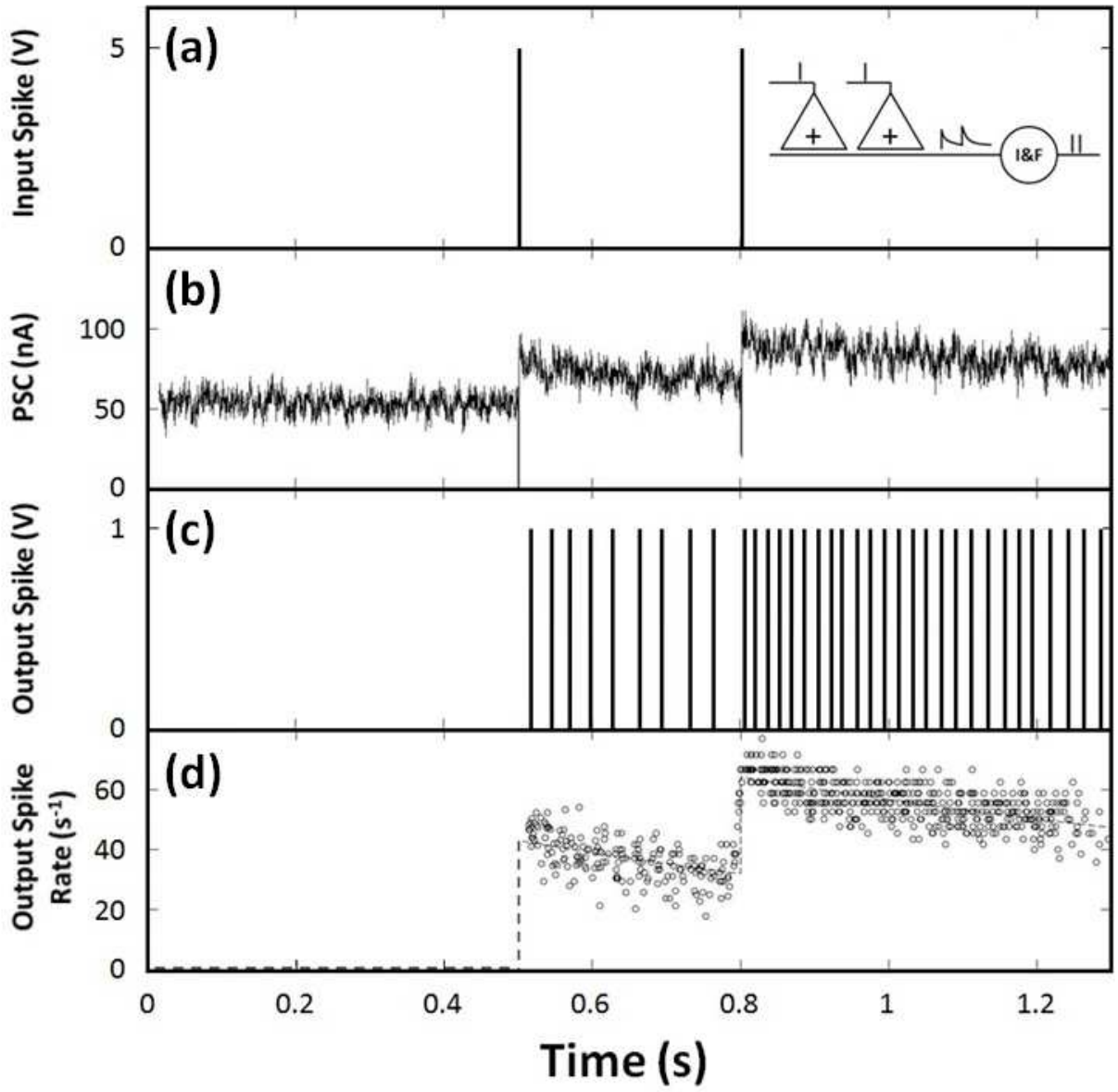

Figure 2.5. (a) A schematic showing a pair of input spikes, 300 ms apart, applied separately on two individual excitatory CNT/In+ synapstor. The inset is a schematic showing a neuromorphic circuit, where a pair of input spikes, applied separately on two individual excitatory CNT/In+ synapstors ("+" triangle), generates an excitatory postsynaptic current (EPSC), triggering output spikes via the integrate-and-fire (I&F) circuit. (b) The combined EPSC, generated by the two excitatory CNT/In+ synapstors, is plotted versus time. (c) The series of output spikes, generated

by the I&F circuit, is shown versus time. (d) The firing rate of output spikes, from 20 individual trials, is shown versus time. The dashed line represents the best fit of the plotted data.

The spatiotemporal correlation between the input and output spikes was also tested for a neuromorphic module with one excitatory CNT/In+ synapstor and one inhibitory CNT/In+ synapstor. A pair of input spikes is applied to one excitatory CNT/In+ synapstor and one inhibitory CNT/In+ synapstor, inducing an EPSC and an IPSC, respectively. These EPSCs and IPSCS are summed, generating output spikes. Two input spikes are applied separately on one excitatory CNT/In+ synapstor and one inhibitory CNT/In+ synapstor, with time interval, Δt = 328 ms (**Figure 2.6a**). **Figure 2.6b** shows the summed EPSC and IPSC from the two CNT/In+ synapstors, which flows to the I&F circuit, generating output spikes (**Figure 2.6c**). The first applied input spike on the excitatory CNT/In+ synapstor causes an EPSC, which increases the firing rate of the output spikes. The second applied input spike on the inhibitory CNT/In+ synapstor causes an IPSC, which decreases the firing rate of the output spikes. **Figure 2.6d** shows the firing rate of the generated output spikes, f(t), versus time, t, from 20 individual trials. The firing rate of the output spikes is fitted with the equation, $f(t) = A_1*Exp[-\alpha_1(t-t_1)]\ H(t-t_1) + A_2*Exp[-\alpha_2(t-t_2)]\ H(t-t_2)$, where t_1 represents the time at which the first input spike is applied on the excitatory CNT/In+ synapstor and t_2 represents the times at which the second input spike is applied on inhibitory CNT/In+ synapstor. The best fit of the experimental data, shown as the dashed line in **Figure 2.6d**, indicates that when $\Delta t = t_2 - t_1 = 328$ ms, $A_1 = 22.4\ s^{-1}$, $A_2 = -33.4\ s^{-1}$, $\alpha_1 = 0.18\ s^{-1}$, and that $\alpha_2 = 3.5\ s^{-1}$. From our experimental results, as Δt decreased from 328 ms to 100 ms, A_2 decreased from $-33.4\ s^{-1}$ to $-43.4\ s^{-1}$, and α_2 decreased from $3.5\ s^{-1}$ to $2.4\ s^{-1}$. There is

a nonlinear relationship between the generated PSC and the firing rate of output spikes in the I&F circuit, which could cause the parameter A_2 to decrease as Δt decreases.

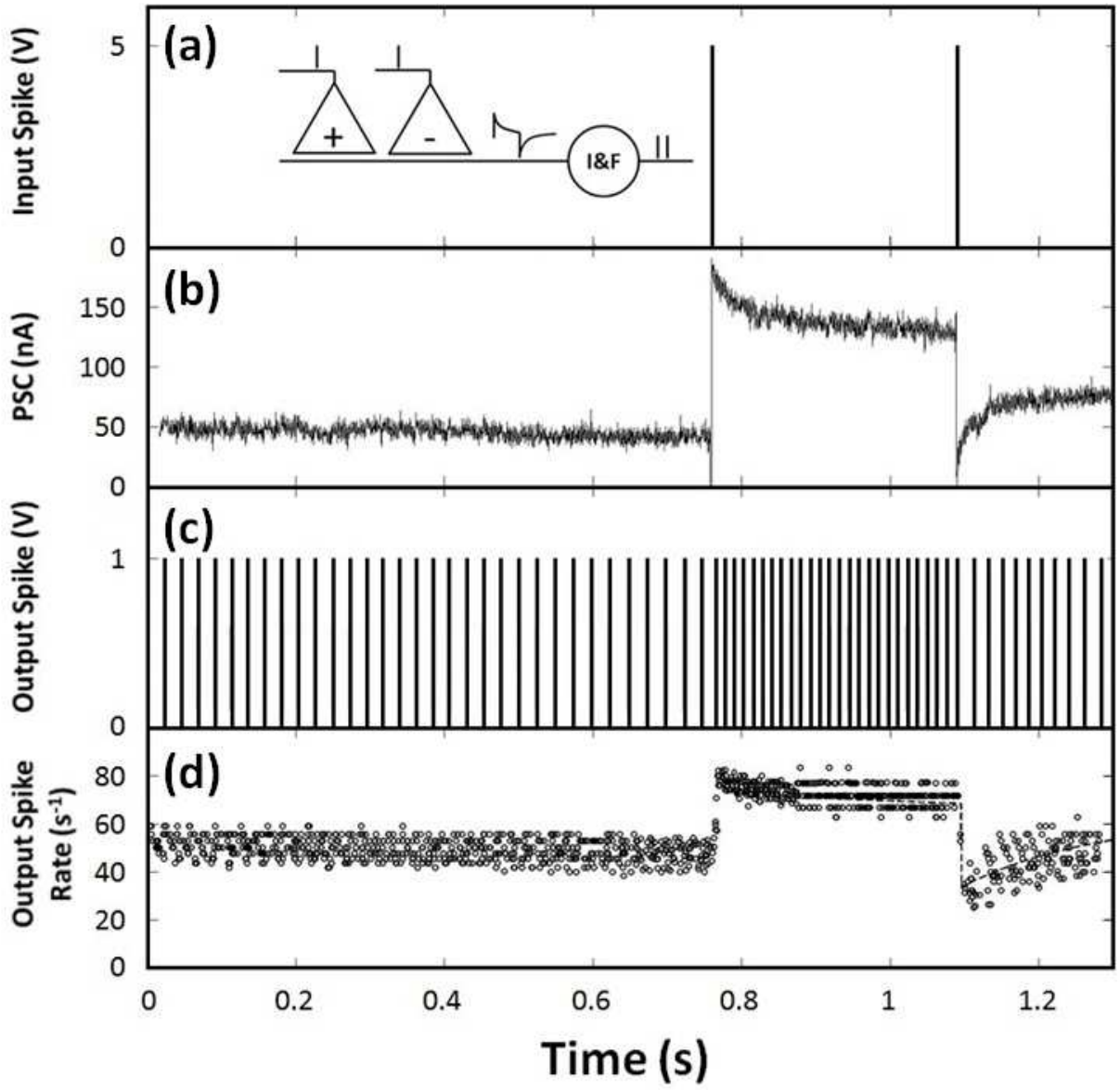

Figure 2.6. (a) A schematic showing a pair of input spikes, 328 ms apart, applied separately on one excitatory and one inhibitory CNT/In+ synapstor. The inset is a schematic showing a neuromorphic circuit, where a pair of input spikes, applied separately on one excitatory ("+" triangle) and one inhibitory ("-" triangle) CNT/In+ synapstor, generates an excitatory

postsynaptic current (EPSC) and an inhibitory postsynaptic current (IPSC), triggering output spikes via the integrate-and-fire (I&F) circuit. (b) The combined PSC, generated by the excitatory and inhibitory CNT/In+ synapstors, is plotted versus time. (c) The series of output spikes, generated by the I&F circuit, is shown versus time. (d) The firing rate of output spikes, from 20 individual trials, is shown versus time. The dashed line represents the best fit of the plotted data.

2.5. Control Device Fabrication

A schematic of the control device for the CNT/In+ synapstor can be seen in **Figure 2.7**. A control device with the same structure as the CNT/In+ synapstor, but without the implanted indium (In) ions was fabricated by using the same processes as for the carbon nanotube (CNT) synapstor. The control device was fabricated on a silicon (Si) substrate with a 300-nm-thick layer of silicon dioxide (SiO_2) grown thermally on top. The back gate was fabricated by depositing a 20-nm-thick layer of titanium (Ti) and an 80-nm-thick layer of aluminum (Al) via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. The device's dielectric layer is comprised of a 25-nm-thick layer of aluminum oxide (Al_2O_3), deposited by atomic layer deposition (ALD) at 250C. This layer of Al_2O_3 is patterned using polyimide (PI) and AZ 5214 photoresist, then etched using a solution of 4% phosphoric acid mixed with 96% deionized water. Following the deposition of a monolayer of (3-Aminopropyl)triethoxysilane (APTES) onto the surface of the Al_2O_3 layer, a random network of single-wall p-type semiconducting CNTs is deposited onto the surface of the APTES-coated Al_2O_3 via spin coating. This CNT network is patterned, using AZ 5214 photoresist and oxygen plasma etching, to form a 15-µm-wide and 20-µm-long transistor channel. The CNT transistor channel is connected with source

and drain electrodes, composed of a 10-nm-thick layer of Ti and an 80-nm-thick layer of gold (Au), deposited via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. Finally, a 2-μm-thick layer of SU-8 polymer was deposited and patterned to cap the entire CNT channel area.

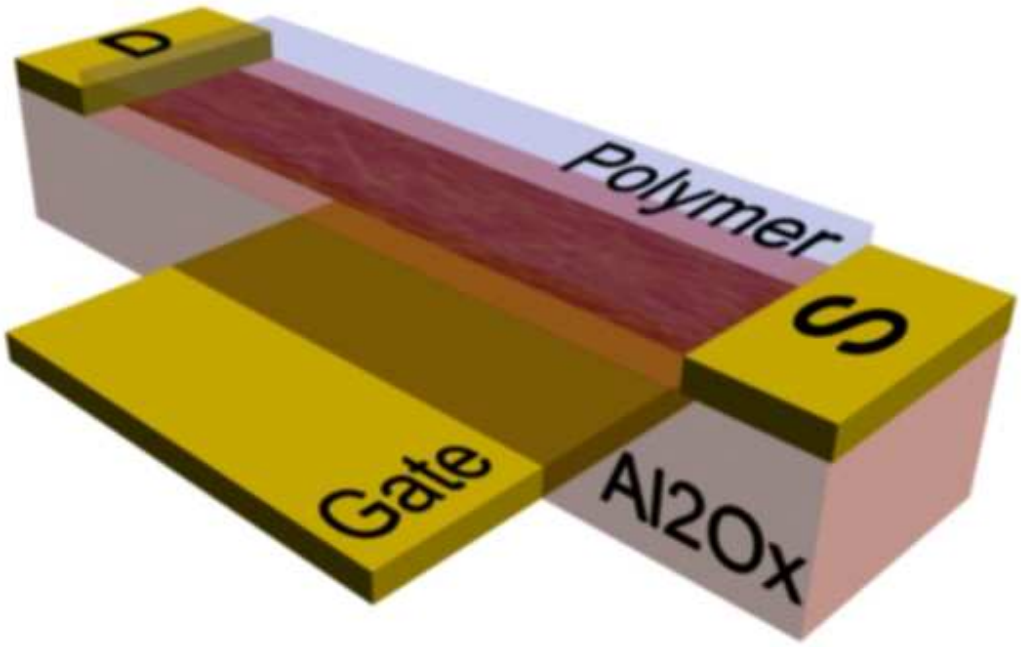

Figure 2.7. A schematic of a control device for the CNT/In+ synapstor, with a channel composed of a random carbon nanotube (CNT) network, bookended by source (S) and drain (D) electrodes. It has an aluminum oxide dielectric layer and an aluminum back gate.

2.6. Electrical Characteristics of the CNT/In+ Synapstors and Their Control Devices

A single spike of amplitude 5 V and duration of 1 ms was applied on the gate electrodes of the CNT/In+ synapstors and their control devices. A positive source-drain electrode voltage, V_{ds} = 0.2 V, was applied on an excitatory CNT/In+ synapstor and its control device, and a negative source-drain electrode voltage, V_{ds} = -0.2 V, was applied on an inhibitory CNT/In+ synapstor and its control device. The source-drain currents measured from the CNT/In+ synapstors and their control devices can be seen in **Figure 2.8**. In the case of the excitatory CNT/In+ synapstor, the input spike applied on the gate electrode induced an excitatory postsynaptic current (EPSC). However, when the same 5 V input spike was applied on the gate electrode of the excitatory CNT/In+ synapstor's control device, no EPSC was observed (**Figure 2.8a**). When the 5 V input spike was applied on the gate electrode of the inhibitory CNT/In+ synapstor, an inhibitory postsynaptic current (IPSC) was induced. When the same 5 V input spike was applied on the gate electrode of the inhibitory CNT/In+ synapstor's control device, no IPSC was observed (**Figure 2.8b**).

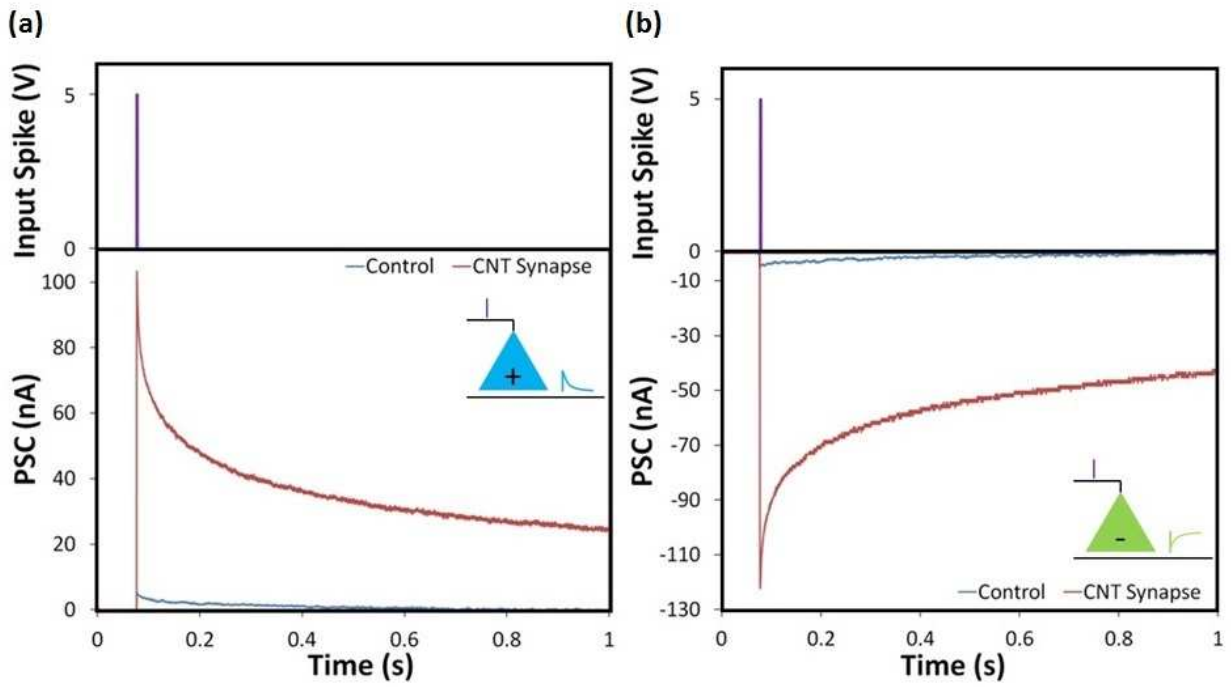

Figure 2.8. (a) An input spike (top) is applied to an excitatory CNT/In+ synapstor, generating a postsynaptic current (PSC) via the CNT channel, shown in red. The PSC generated by an excitatory control device for the CNT/In+ synapstor, with the same input spike, is shown in blue. (b) An input spike (top) is applied to an inhibitory CNT/In+ synapstor, generating a PSC (red) via the CNT channel. The PSC generated by an inhibitory control device for the CNT/In+ synapstor, with the same input spike, is shown in blue.

2.7. Paired-Pulse Testing

A pair of input spikes were applied to the gate electrode of an excitatory CNT/In+ synapstor, inducing an excitatory postsynaptic current (EPSC), and triggering output spikes via an I&F circuit in the neuromorphic module (Inset, **Figure 2.9**). The time interval between the spike pair, Δt, varied between 1 ms and 40 ms. The EPSC induced by the spike pair with Δt = 40 ms is shown in **Figure 2.9a**, where E_1 represents the amplitude of the EPSC induced when the

first input spike is input, and E_2 represents the amplitude of the EPSC induced when the second input spike is input. The EPSC induced by the second input spike was superimposed on the EPSC induced by the first input spike. The paired-pulse ratio, E_2/E_1, represents the relationship between the amplitudes of the two EPSCs induced by the two input spikes. The paired-pulse ratio is plotted against the Δt in **Figure 2.9b**, which shows that the paired-pulse ratio decreases with increasing Δt. The firing rate of the output spikes, f(t), is fitted by the function: $f(t) = A_1*Exp[-\alpha_1(t-t_1)]\ H(t-t_1) + A_2*Exp[-\alpha_2(t-t_2)]\ H(t-t_2)$, where t_1 and t_2 represent the times at which the first input spike and second input spike are fired, respectively, and H(t) is a unit step function. The parameters A_1 and α_1 are associated with the response of the neuromorphic module to the first input spike, which should not change against Δt. The parameters A_2 and α_2 were derived from the best fit to the experimental data when Δt changed between 1 ms to 40 ms. As shown in **Figure 2.10**, when Δt increases from 1 ms to 40 ms, parameter A_2 gradually decreases from 20.1 s^{-1} to 16.3 s^{-1}, and parameter α_2 fluctuates between 0.75 s^{-1} and 2.1 s^{-1}.

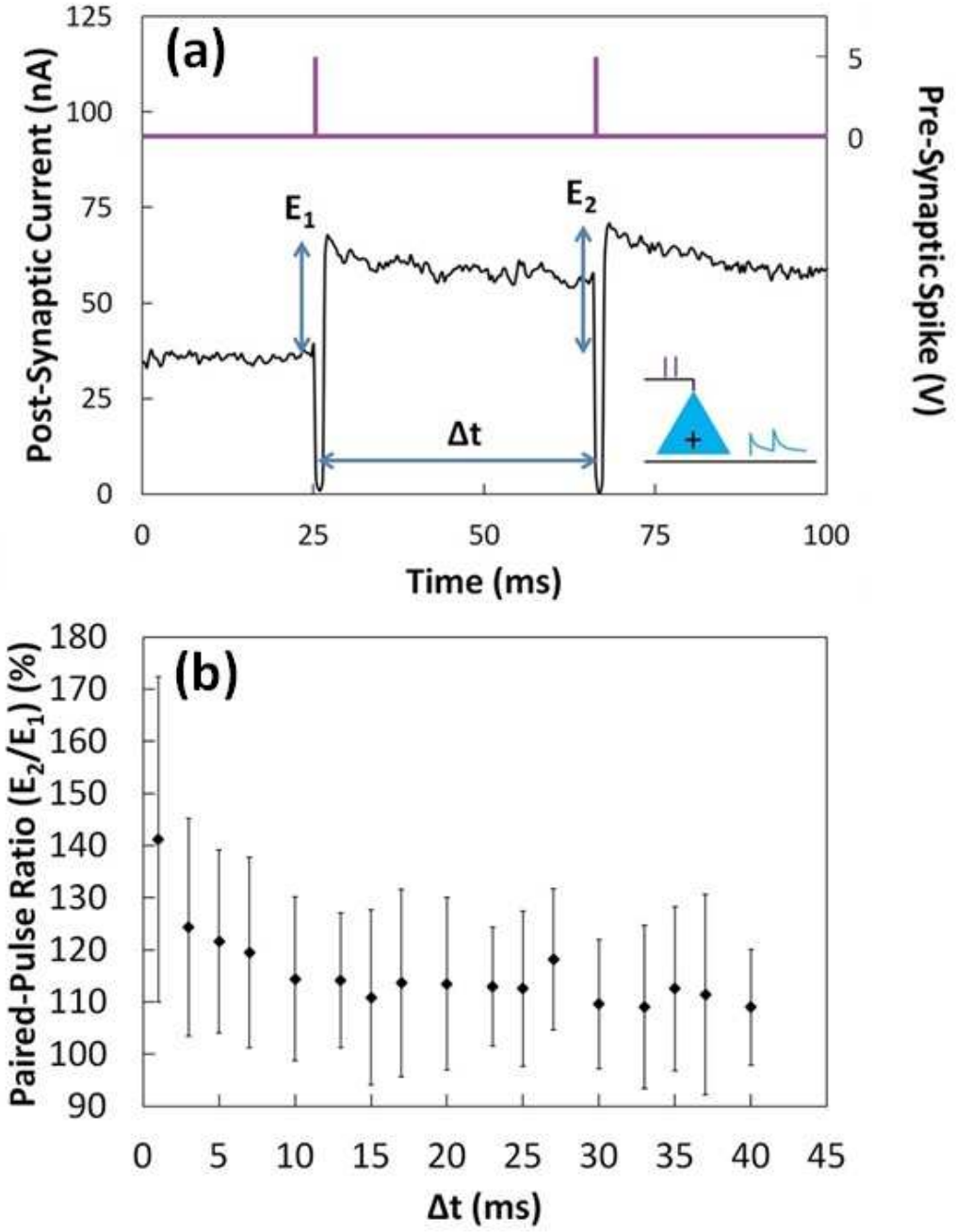

Figure 2.9. (a) A pair of input spikes (purple) are applied on an excitatory CNT/In+ synapstor, generating an excitatory postsynaptic current (EPSC). The inset is a schematic showing a neuromorphic circuit, where a pair of input spikes, applied on an excitatory CNT/In+ synapstor

(blue "+" triangle), generates an excitatory postsynaptic current (EPSC), triggering output spikes via the integrate-and-fire (I&F) circuit. E_1 represents the amplitude of the EPSC generated by the CNT/In+ synapstor when the first input spike is applied. E_2 represents the amplitude of the EPSC generated when the second input spike is applied. Δt represents the time interval between the two applied input spikes. The paired-pulse ratio between the amplitudes of the EPSCs generated by the first and second input spikes (E_2/E_1) is shown versus Δt.

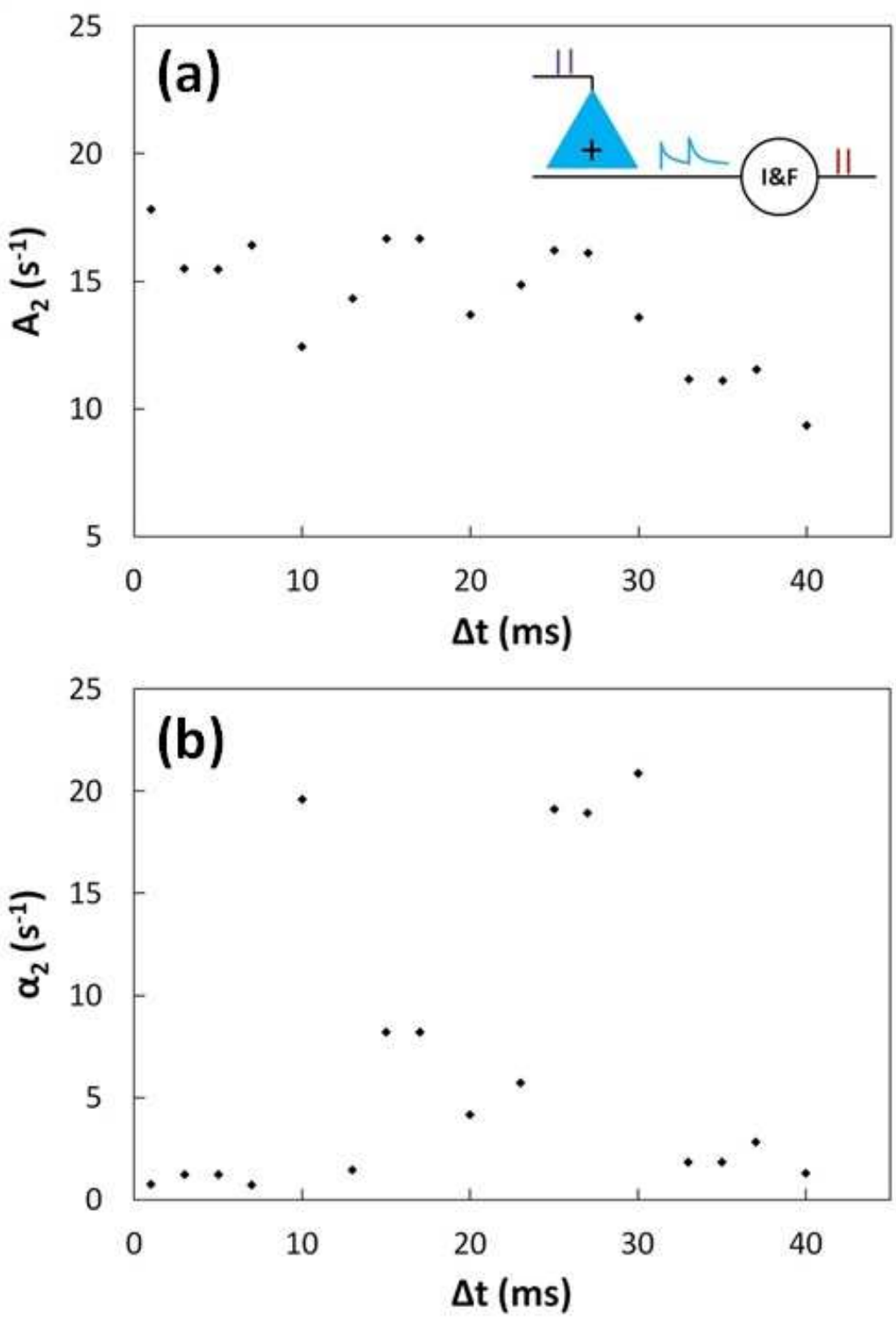

Figure 2.10. (a) The fitting parameter A_2, from the best fit equation of the output spike frequency from a pair of input spikes applied on an excitatory CNT/In+ synapstor, is shown

versus the time interval between the two applied input spikes, Δt. (b) The fitting parameter α_2, from the best fit equation of the output spike frequency from a pair of input spikes applied on an excitatory CNT/In+ synapstor, is shown versus the time interval between the two applied input spikes, Δt.

2.8. Testing on a Neuromorphic Module with Two Excitatory CNT/In+ Synapstors

Two excitatory CNT/In+ synapstors were connected together to form a neuromorphic module. A pair of input spikes was applied on the gate electrodes of the CNT/In+ synapstors separately, inducing excitatory postsynaptic currents (EPSCs), and trigger output spikes in the neuromorphic module (Inset, **Figure 2.11**). The firing rate of the output spikes, f(t), is fitted by the function: $f(t) = A_1*\text{Exp}[-\alpha_1(t-t_1)]\ H(t-t_1) + A_2*\text{Exp}[-\alpha_2(t-t_2)]\ H(t-t_2)$, where t_1 and t_2 represent the moments at which the first input spike is fired on the CNT/In+ synapstor 1 and the second input spike is fired on the CNT/In+ synapstor 2, respectively. The parameters A_1, α_1, A_2, and α_2 are derived from the best fit to the experimental data when Δt changed between 5 ms to 300 ms. **Figure 2.11** shows that when Δt increases from 5 ms to 300 ms, the parameter A_2 gradually increases from 20.1 s^{-1} to 32.1 s^{-1}, and parameter α_2 fluctuates between 0.05 s^{-1} and 0.82 s^{-1}.

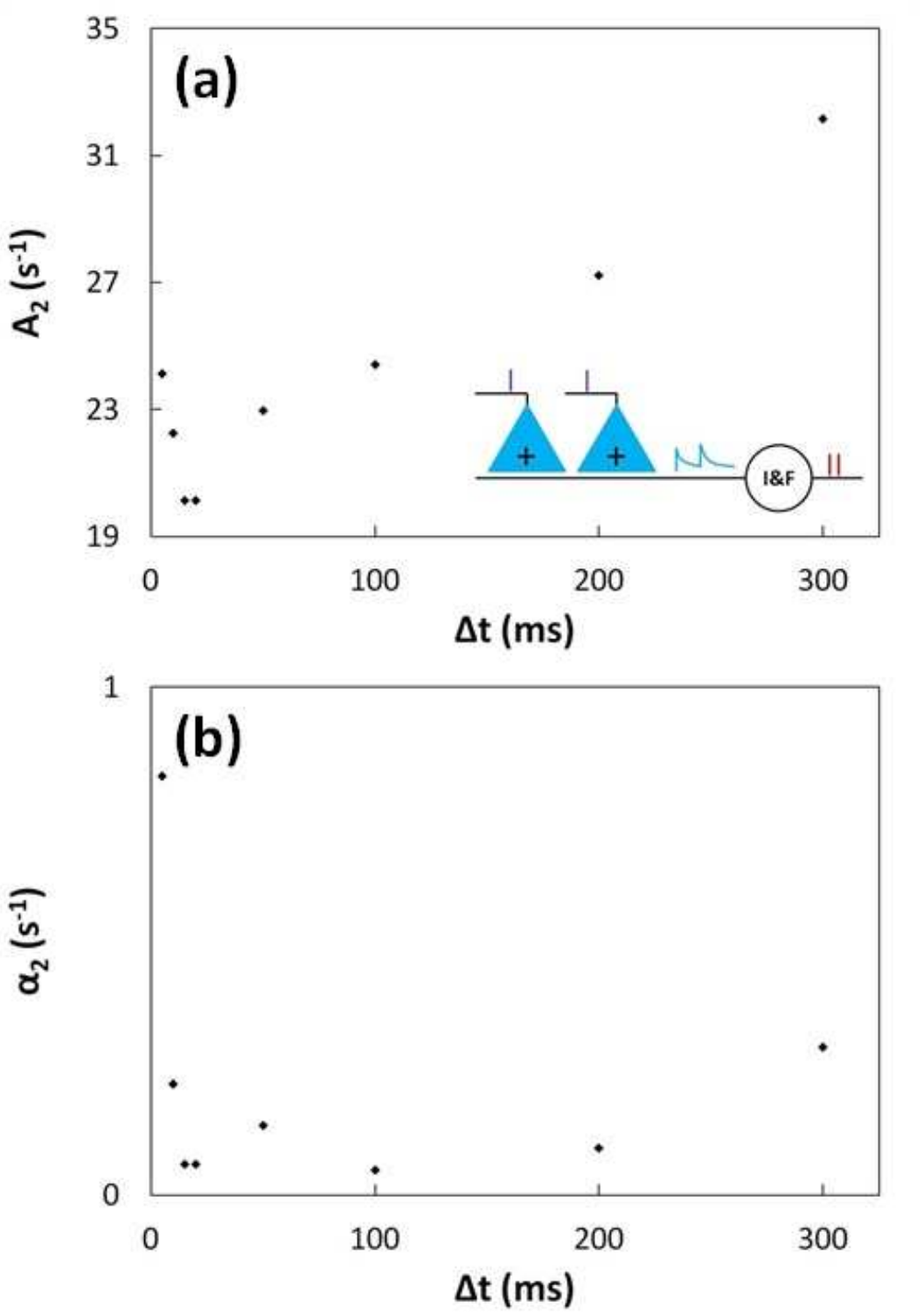

Figure 2.11. (a) The fitting parameter A_2, from the best fit equation of the output spike frequency from a pair of input spikes applied separately on two individual excitatory CNT/In+

synapstors, is shown versus the time interval between the two applied input spikes, Δt. (b) The fitting parameter α_2, from the best fit equation of the output spike frequency from a pair of input spikes applied separately on two individual excitatory CNT/In+ synapstors, is shown versus the time interval between the two applied input spikes, Δt.

2.9. Summary

A nonlinear dynamic analog neuromorphic module composed of excitatory and inhibitory CNT/In+ synapstors and a nonlinear integrate-and-fire (I&F) circuit was demonstrated. The channel of the CNT/In+ synapstor was made from a random carbon nanotube (CNT) network, and indium (In) ions were implanted into an aluminum oxide (Al_2O_3) dielectric layer in its gate. A positive voltage pulse (spike), applied to the gate electrode of the CNT synapstor, causes electrons to move away from the CNT channel, into the Al_2O_3 dielectric layer. These electrons become trapped near defect sites, created by the implanted In ions. This, in turn, modifies the hole concentration in the CNT channel and induces a dynamic postsynaptic current (PSC) through the CNT channel. A spike applied on the gate electrode of an excitatory CNT/In+ synapstor, with a positive source-drain electrode voltage, induces an excitatory PSC (EPSC). An inhibitory PSC (IPSC) is induced when a spike is applied on the gate electrode of an inhibitory CNT/In+ synapstor, with a negative source-drain electrode voltage. Multiple input spikes induce PSCs that collectively flow to an I&F soma circuit, jointly triggering output spikes. The nonlinear analog function of the neuromorphic module is analyzed. The module could potentially be scaled up to emulate biological neural networks with parallel signal processing and low energy consumption.

References:

1. Indiveri, G., In A Low-Power Adaptive Integrate-and-Fire Neuron Circuit. *IEEE Int. Symp. Circuits Syst.* **2003**, pp. IV-820-IV-823 vol. 4.
2. Debanne, D.; Guerineau, N. C.; Gähwiler, B.; Thompson, S. M., Paired-Pulse Facilitation and Depression at Unitary Synapses in Rat Hippocampus: Quantal Fluctuation Affects Subsequent Release. *J. Physiol.* **1996**, *491*, 163-176.
3. Byrne, J.; Byrne, J. H.; Roberts, J. L., *From Molecules to Networks: an Introduction to Cellular and Molecular Neuroscience*. Academic Press: 2009, pp. 470, 478, 544-545.

CHAPTER 3: DOPING MODULATED CNT SYNAPSTORS

3.1. Introduction

We report a carbon nanotube (CNT) based synapstor with analog spike signal processing, plasticity, and memory characteristics with the goal of emulating a biological synapse. The CNT synapstor has a structure similar to that of a field-effect transistor. The device channel, connecting the source and drain electrodes, is composed of a random CNT network. The CNTs used are initially p-type, but half of the CNT channel is converted to n-type, creating a p-n junction in the CNT channel. This p-type to n-type conversion of the CNTs is done by depositing a layer of aluminum oxide (Al_2O_3) on top of the CNTs. Changing the CNTs to n-type also modifies the Schottky barrier at the interface of the CNT channel and the gold (Au) drain electrode.

The doping modulated CNT synapstor generates a dynamic postsynaptic current (PSC) via the CNT channel when an input spike is applied on the gate electrode of the device. The doping modulation in the CNT channel of the device results in a decreased baseline device current, improved ratio between the PSC amplitude and its baseline current, and significantly reduced the power consumed by the CNT synapstor. The doping modulated CNT synapstor also has memory and plasticity characteristics. The PSCs generated from the CNT synapstors flow to an integrate-and-fire (I&F) circuit. As the potential in the I&F circuit increases above a preset threshold value, output spikes are triggered. These doping modulated CNT synapstors could be incorporated, along with I&F circuits, to create a neuromorphic circuit, which could be scaled up to emulate the biological neural network. This neuromorphic circuit could operate with learning

capabilities, fast parallel signal processing, and low power consumption. Area such as artificial intelligence, pattern recognition, and motor control could stand to benefit.

3.2. Doping Modulated CNT Synapstor Fabrication

A schematic of the doping modulated CNT synapstor is shown in **Figure 3.1**. The doping modulated CNT synapstor is fabricated on a silicon (Si) wafer with a 300-nm-thick layer of thermally grown SiO_2 on top. The back gate is composed of a 5-nm-thick layer of Ti and an 80-nm-thick layer of Al, both deposited via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. The device's dielectric layer is comprised of a 25-nm-thick layer of aluminum oxide (Al_2O_3), deposited by atomic layer deposition (ALD) at 250 C. This layer of Al_2O_3 is patterned using PI and AZ 5214 photoresist, then etched using a solution of 4% phosphoric acid mixed with 96% deionized water. Following the deposition of a monolayer of APTES onto the surface of the Al_2O_3 layer, a random network of single-wall p-type semiconducting CNTs is deposited onto the surface of the APTES-coated Al_2O_3 via dry coating. In this dry coating method, the sample is placed on a hotplate at 90C. The CNT solution is dropped onto the sample and allowed to dry. This CNT network is patterned, using AZ 5214 photoresist and oxygen plasma etching, to form a 15-µm-wide and 6-µm-long transistor channel. The CNT transistor channel is connected with source and drain electrodes, composed of a 5-nm-thick layer of Ti and a 50-nm-thick layer of gold (Au), deposited via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. Half of the patterned CNT channel is covered with a layer of 20-nm-thick Al_2O_3, deposited via ALD at 90 C. Finally, a 2-µm-thick layer of SU-8 polymer is deposited and patterned to cap the entire CNT channel area.

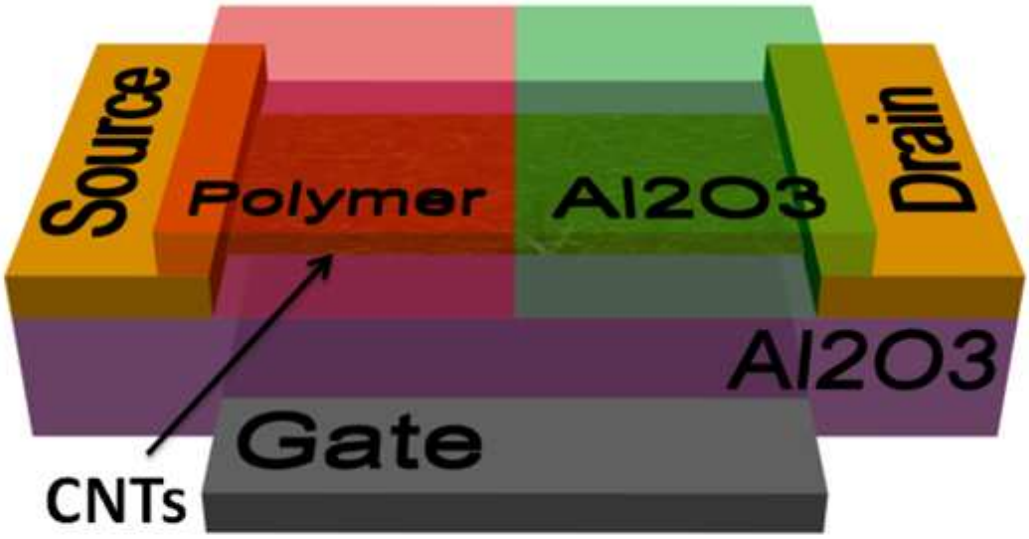

Figure 3.1: A schematic of a doping modulated carbon nanotube (CNT) synapstor, composed of an aluminum oxide (Al_2O_3) dielectric layer and a device channel composed of a random carbon nanotube (CNT) network, bookended by source and drain electrodes. One half of the CNT network is capped with an SU-8 polymer layer, while the other half is capped with a layer of Al_2O_3 deposited by atomic layer deposition at 90 C.

3.3. Device Physics

When aluminum oxide (Al_2O_3) was deposited on top of the carbon nanotube (CNT) network, the CNTs were converted from p-type semiconducting to n-type ones. This change is

due to a modification of the energy band structure of the CNT channel in the synapstor, caused by electrostatic doping of the CNTs. The energy band structure of the doping modulated CNT synapstor can be seen in **Figure 3.2a**. Since the other half of the CNT channel was covered with an SU-8 polymer, and remained p-type semiconducting, a p-n junction was formed in the CNT channel between the p-type CNTs covered by SU-8 polymer and the n-type CNTs covered by low temperature deposited Al_2O_3. The Fermi level of the n-type CNTs (~3.8 eV) results in a large difference between it and the work function of the gold (Au) electrode (-5.1 eV), forming a Schottky barrier between the n-type CNTs and the Au drain electrode of the doping modulated CNT synapstor. Two different types of control devices for the doping modulated CNT synapstor were fabricated and tested in order to better understand the doping modulation. The device structures of the control devices were similar to that of the doping modulated CNT synapstor, but the CNT channels were fully capped with a SU-8 polymer or fully capped with an Al_2O_3 layer, deposited by ALD at 90 C.

When a negative source-drain electrode voltage, $V_{ds} < 0$ V, was applied on the drain electrode of the doping modulated CNT synapstor, the device current, I_{ds}, was increased. This is due to the reduction of the p-n junction barrier, in the CNT channel, and the Schottky barrier, between the n-type CNTs and the Au electrode, caused by the applied V_{ds}. When a positive source-drain electrode voltage, $V_{ds} > 0$ V, was applied on the drain electrode of the doping modulated CNT synapstor, the device current was decreased. This is due to the increase of the p-n junction barrier, in the CNT channel, and the Schottky barrier, between the n-type CNTs and the Au electrode, caused by the applied V_{ds}.

When a negative gate voltage, $V_g < 0$ V, was applied on the gate electrode of the doping modulated CNT synapstor, the device current was increased. This is due to the reduction of the

Schottky barrier, between the n-type CNTs and the Au electrode, caused by the applied V_g. When the Schottky barrier is decreased, holes are injected into the CNT channel, reducing the p-n junction barrier. When a positive gate voltage, $V_g > 0$ V, was applied on the gate electrode of the doping modulated CNT synapstor, the device current was decreased. This is due to the increase of the Schottky barrier, between the n-type CNTs and the Au electrode, caused by the applied V_g. When the Schottky barrier is increased, carriers have a harder time flowing through the CNT channel.

When a positive voltage spike is applied on the aluminum (Al) back gate of the doping modulated CNT synapstor, electrons are attracted away from the CNT channel and into the Al_2O_3 dielectric layer. These electrons become trapped locally near the defects in the Al_2O_3 dielectric layer. When this happens, the hole concentration in the CNT channel increases, thereby increasing the current through the CNT channel. After the spike is removed, the electrons are gradually released from the dielectric layer. As electrons return from the Al_2O_3 dielectric layer to their original locations near the CNT channel, the concentration of holes in the CNT channel decreases. As this happens, the current through the CNT channel will gradually decrease, returning to its initial baseline value. This is what generates a dynamic postsynaptic current (PSC) through the CNT channel. When a positive source-drain electrode voltage, $V_{ds} = 0.2$ V, is applied to the doping modulated CNT synapstor, a positive voltage spike applied on the gate electrode induces an excitatory PSC (EPSC), and the CNT transistor functions as an excitatory synapse. When a negative source-drain electrode voltage, $V_{ds} = -0.2$ V, is applied to the doping modulated CNT synapstor, a positive voltage spike induces an inhibitory PSC (IPSC), and the CNT transistor functions as an inhibitory synapse.

The PSC, generated from the doping modulated CNT synapstor, flows toward an integrate-and-fire (I&F) circuit. The PSC is amplified and integrated with respect to time by a capacitor in the I&F circuit. When the PSC is below a preset threshold current, no output spikes are generated by the I&F circuit. When the PSC is increased above the preset threshold current, an output spike is triggered, and the PSC integration starts over again from zero.[1] The output spike rate increases nonlinearly with increasing PSC. The input spike, PSC, and output spikes of the neuromorphic module can be measured by analog-to-digital converters (ADC). The operation of a typical excitatory doping modulated CNT synapstor, inducing an EPSC can be seen in **Figure 3.3**.

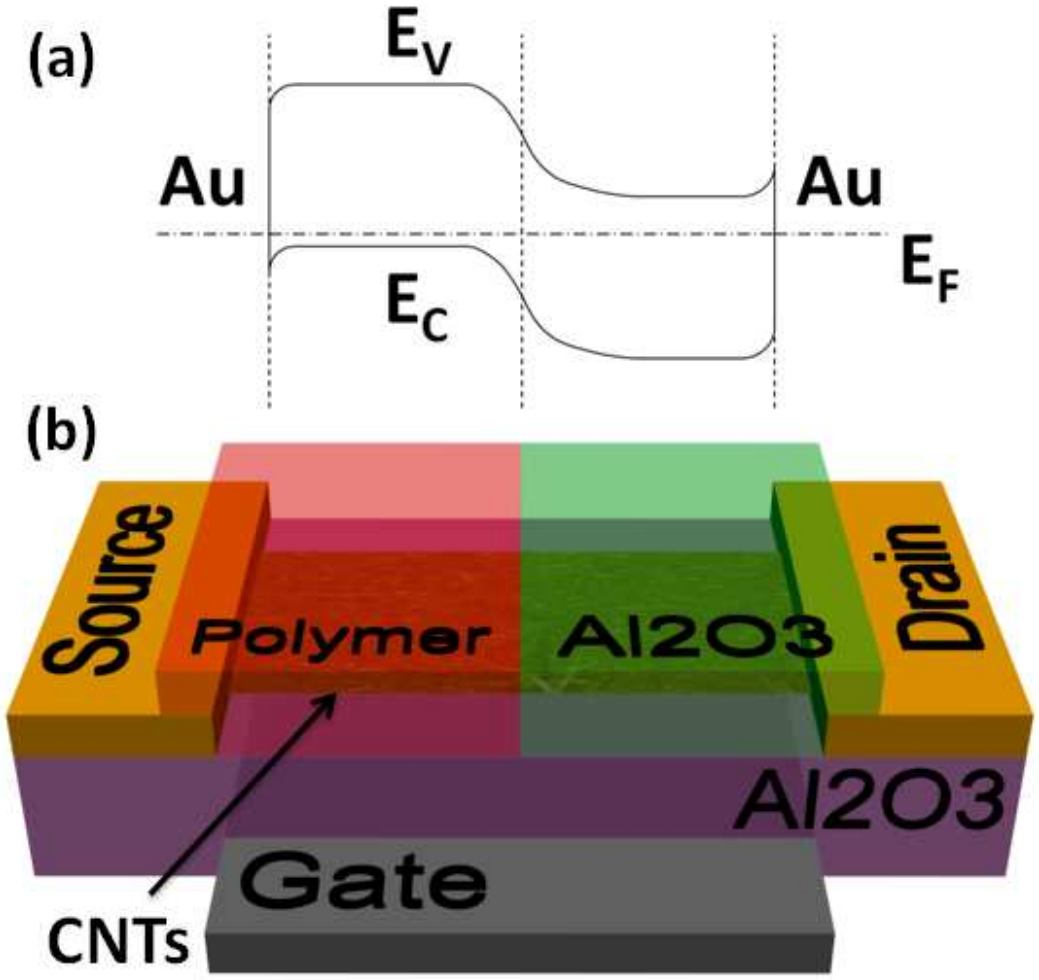

Figure 3.2. (a) The energy level diagram for the doping modulated CNT synapstor. (b) A schematic of a doping modulated carbon nanotube (CNT) synapstor, composed of an aluminum oxide (Al_2O_3) dielectric layer and a device channel composed of a random carbon nanotube (CNT) network, bookended by source and drain electrodes. One half of the CNT network is capped with an SU-8 polymer layer, while the other half is capped with a layer of Al_2O_3 deposited by atomic layer deposition at 90 C.

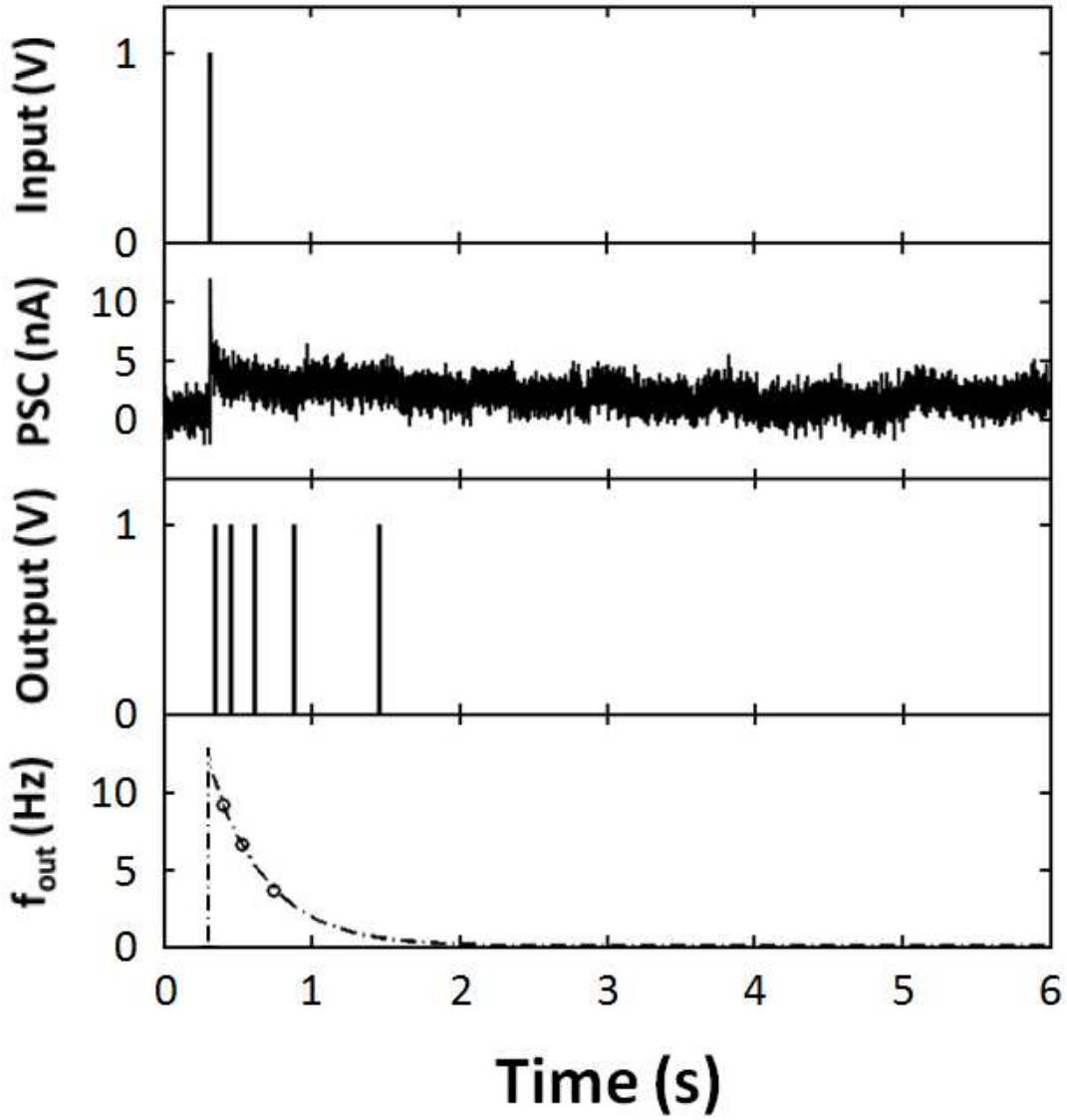

Figure 3.3. (a) A single input spike is applied on an excitatory doping modulated carbon nanotube (CNT) synapstor. (b) The EPSC, generated by the doping modulated CNT synapstor, is plotted versus time. (c) The series of output spikes, generated by the integrate-and-fire (I&F)

circuit, is shown versus time. (d) The firing rate of output spikes is shown versus time. The dashed line represents the best fit of the plotted data.

3.4. Results and Discussion

Figure 3.4 shows a typical source-drain electrode current, I_{ds}, versus source-drain electrode voltage, V_{ds}, for a doping modulated CNT synapstor. This measurement was done with the gate voltage, V_g, fixed at 0 V. When a negative source-drain voltage, $V_{ds} < 0$ V, was applied on the drain electrode of the doping modulated CNT synapstor, the energy band (shown in **Figure 3.4**, inset on the left) was bent upward. This resulted in a reduction of the p-n junction potential barrier in the CNT channel, as well as a reduction in the Schottky barrier between the n-type CNTs and the Au electrode. Carriers were then able to flow through the CNT channel, between the source and drain electrodes, more easily, increasing the device current. The magnitude of the device current increased from ~0 A to ~200 nA when V_{ds} was swept between 0 V and -2 V. When a positive source-drain voltage, $V_{ds} > 0$ V, was applied on the drain electrode of the doping modulated CNT synapstor, the energy band (shown in **Figure 3.4**, inset on the right) was bent downward. In this case, the p-n junction potential barrier in the CNT channel remained, and the Schottky barrier between the n-type CNTs and the Au electrode increased. This made it more difficult for carriers to flow through the CNT channel, between the source and drain electrodes, decreasing the device current. The magnitude of the device current was less than ~3 nA when V_{ds} was swept between 0 V and 2 V.

The same I_{ds} versus V_{ds} measurement was performed on the control devices for the doping modulated CNT synapstor. In the case of the control device with the entire CNT channel

covered with an SU-8 polymer, all of the CNTs remained p-type, so there was no p-n junction barrier in the CNT channel or a Schottky barrier at the interface between the CNT channel and Au electrode. The device current increased with increasing magnitude of the source-drain voltage, V_{ds}, regardless of if V_{ds} was swept between 0 V and 2 V or between 0 V and -2 V. These results indicate that there is no p-n junction barrier or Schottky barrier present in the CNT channel of the SU-8 polymer capped control device. The test was also done for the control device with the entire CNT channel covered with a layer of Al_2O_3 deposited by ALD at 90 C. In this control device, all of the CNTs were converted to n-type, so there was no p-n junction barrier in the CNT channel. However, there were Schottky barriers formed at the interfaces between the CNT channel and the Au electrodes. When a negative source-drain voltage, $V_{ds} < 0$ V, was applied on the drain electrode of the doping modulated CNT synapstor, the Schottky barrier was reduced, allowing carrier to flow more freely through the CNT channel between the source and drain electrodes. The control device's source-drain current increased with increasing magnitude of V_{ds}. When a positive source-drain voltage, $V_{ds} < 0$ V, was applied on the drain electrode of the doping modulated CNT synapstor, the Schottky barrier was increased, making it more difficult for carriers to flow through the CNT channel between the source and drain electrodes.

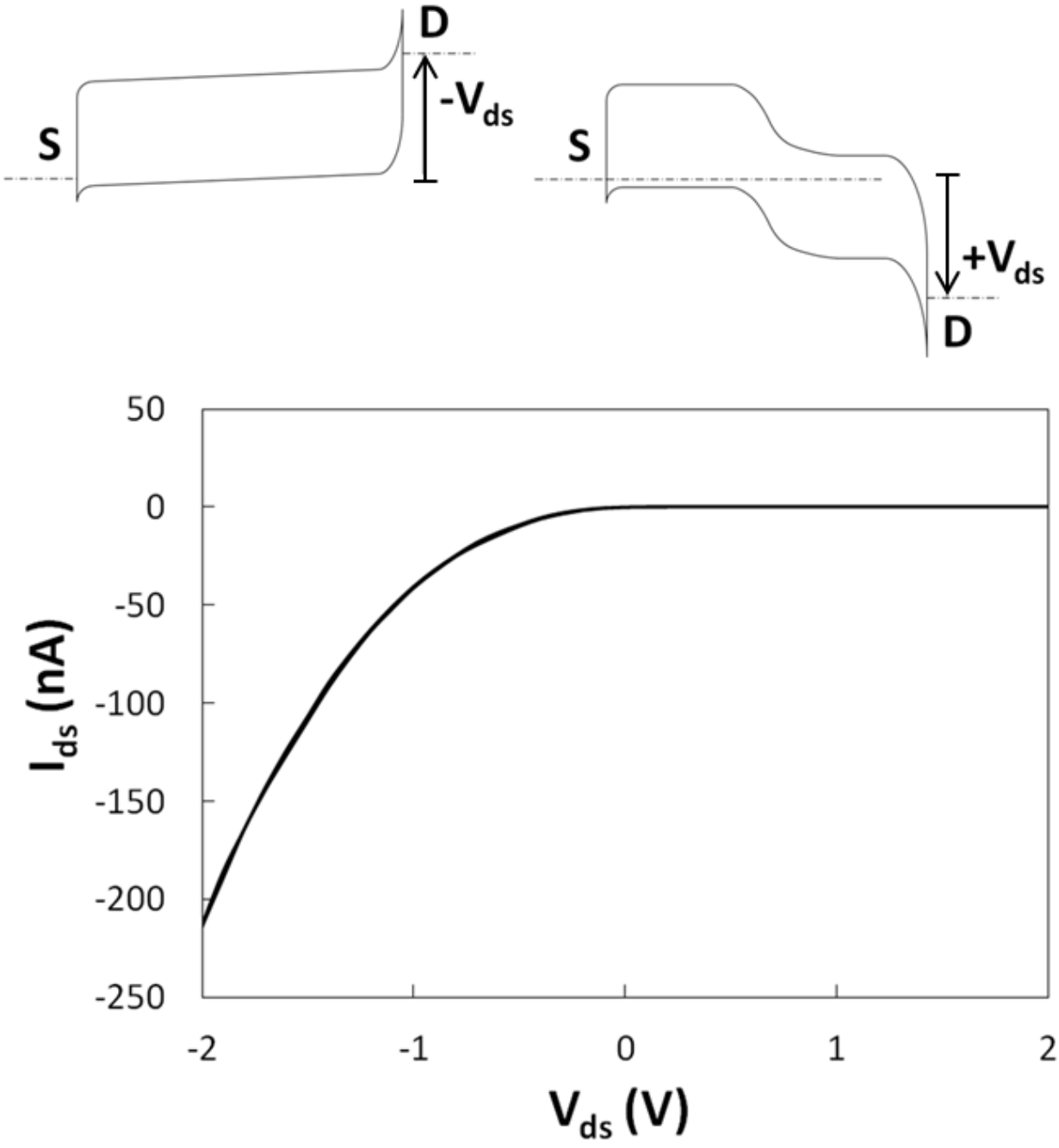

Figure 3.4. The source-drain current, I_{ds}, of the doping modulated carbon nanotube (CNT) synapstor is shown versus the source-drain voltage, V_{ds}, which is swept from -2 V to 2 V to -2 V. The insets at the top show the energy level diagrams for the doping modulated CNT synapstor are shown when $V_{ds} < 0$ V (left) and when $V_{ds} > 0$ V (right).

Figure 3.5a shows a typical source-drain electrode current, I_{ds}, versus gate electrode voltage, V_g, for a doping modulated CNT synapstor. This measurement was done with the source-drain voltage, V_{ds}, fixed at 0.5 V. When a negative gate voltage, $V_g < 0$ V, was applied on the doping modulated CNT synapstor, the energy band (shown in **Figure 3.5**, inset on the left) was bent upward. This resulted in a reduction of the Schottky barrier between the n-type CNTs and the Au electrode. Holes were then able to move into the CNT channel, eliminating the p-n junction potential barrier, increasing the device current. When a positive gate voltage, $V_g > 0$ V, was applied on the doping modulated CNT synapstor, the energy band (shown in **Figure 3.5**, inset on the right) was bent downward. This resulted in an increase of the Schottky barrier between the n-type CNTs and the Au electrode. This made it more difficult for carriers to move through the CNT channel, reducing the device current.

The doping modulated CNT synapstor showed memory characteristics. When V_g was swept from -5 V to 5 V, with V_{ds} fixed at 0.5 V, the device current decreased from ~106 nA to ~0.4 nA. The device current increased from ~0.4 nA to ~109 nA when the gate voltage was swept from 5 V to -5 V, resulting in a counter-clockwise hysteresis loop in the I_{ds}-V_g plot. When the gate voltage was swept between 0 V and 5 V, electrons moved from the CNT channel into the Al_2O_3 dielectric layer. These electrons became trapped in the defects in the Al_2O_3 dielectric layer when the gate voltage is swept from 5 V to 0 V. These trapped electrons attract holes, increasing the hole carrier concentration in the CNT channel, thereby increasing the device current. This is shown in **Figure 3.5b**. The electrons at the bottom of the Al_2O_3 dielectric layer become depleted when the gate voltage is swept between 0 V and -5 V. **Figure 3.5c** shows that the hole concentration in the CNT channel decreases when the gate voltage is then swept from -5

V to 0 V. This causes the device current to decrease. The counter-clockwise hysteresis loop seen in the I_{ds}-V_g curve, which demonstrates the memory of the doping modulated CNT synapstor, is due to electrons being trapped in the bottom Al_2O_3 dielectric layer. The leakage current through the gate of the doping modulated CNT synapstor was negligible, as it was < 1 pA.

The same I_{ds} versus V_g measurement was performed on the control devices for the doping modulated CNT synapstor. The control device with the entire CNT channel covered with an SU-8 polymer showed similar trends to the doping modulated CNT synapstor. The device current decreased from ~117 nA to ~0 A when the gate voltage was swept from -5 V to 5 V, with V_{ds} fixed at 0.5 V. When the gate voltage was then swept from 5 V to -5 V, the device current increased from ~0 A to ~130 nA. This trend was expected, due to the CNT channel in the control device being p-type. The hole concentration increased when negative gate voltages are applied to the control device, increasing the current in the CNT channel. Similar to the doping modulated CNT synapstor, the SU-8 polymer capped control device showed a counter-clockwise hysteresis loop in the I_{ds}-V_g curve. This results from the electrons that become trapped in the Al_2O_3 dielectric layer.

The same measurement was also done on the control device that was fully capped with Al_2O_3, deposited by ALD at 90 C. When the gate voltage was swept from -5 V to 5 V, the device current increased from ~17 nA to ~160 nA. The device current decreased from ~160 nA to ~ 20 nA when the gate voltage was swept from 5 V to -5 V, signifying that the CNT channel in the control device was n-type. This means that the electron concentration in the CNT channel increased when the gate voltage became more positive, thereby increasing the device current. When positive gate voltages were applied to the control device, capped with a layer of Al_2O_3, electrons moved from the CNT channel into the Al_2O_3 dielectric layer. This repelled electrons in

the CNT channel, decreasing the device current. On the other hand, electrons became depleted from the Al_2O_3 dielectric layer when negative gate voltages were applied on the control device. This caused the electron carrier concentration to increase in the CNT channel, thereby increasing the device current. The electrons that become trapped in the Al_2O_3 dielectric layer cause the clockwise hysteresis loop that can be seen in the I_{ds}-V_g curve.

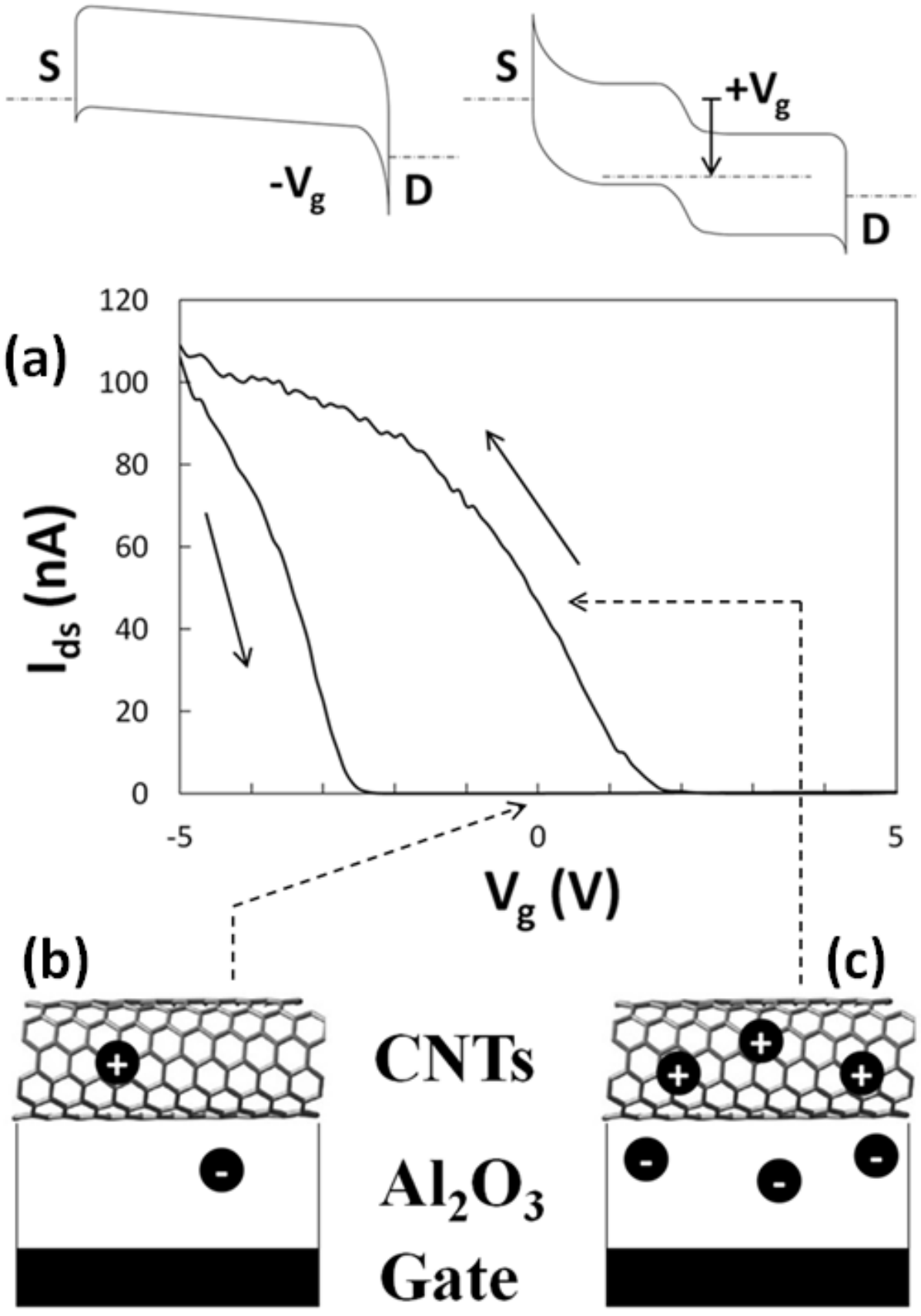
S
-V_g
D
S
+V_g
D
(a)
120
100
80
60
40
20
0
I_ds (nA)
-5
0
5
V_g (V)
(b)
(c)
CNTs
Al2O3
Gate

Figure 3.5. (a) The source-drain current, I_{ds}, of the doping modulated carbon nanotube (CNT) synapstor is shown versus the gate voltage, V_g, which is swept from -5 V to 5 V to -5 V. The insets at the top show the energy level diagrams for the doping modulated CNT synapstor are shown when $V_g < 0$ V (left) and when $V_g > 0$ V (right). (b) A schematic showing the concentration of holes ("+" circles) in the CNT channel when $V_g < 0$ V. (c) A schematic showing the concentration of holes ("+" circles) in the CNT channel when $V_g > 0$ V.

A typical excitatory doping modulated CNT synapstor induces an excitatory postsynaptic current (EPSC). The operation of an excitatory doping modulated CNT synapstor, operated with a source-drain voltage, V_{ds} = 0.2 V, is described in **Figure 3.6**. A single input spike, with amplitude V_g = 2.25 V and duration of 1 ms, is applied on the gate electrode of a doping modulated CNT synapstor (**Figure 3.6a**), which generates an EPSC (**Figure 3.6b**). The peak amplitude of the EPSC is ~12 nA above the baseline current. After the spike, the device current gradually decays back to the baseline current over a duration of approximately 4.0 s. The generated EPSC flows to the integrate-and-fire (I&F) circuit, generating output spikes (**Figure 3.6c**). As can be seen from **Figure 3.6d**, decreased EPSC results in decreased firing rates of the output spikes. The firing rate of the output spikes continues to decrease until the EPSC decreases below a preset threshold value, V_{th}, that is set in the I&F circuit. When the EPSC becomes smaller than V_{th}, output spikes will no longer be generated. In the case shown in **Figure 3.6**, output spikes are generated for 1.2 s after the input spike is applied to the doping modulated CNT synapstor, indicating that it took 1.2 s for the EPSC to decrease below V_{th}. The firing rate of the output spikes, f(t), versus time, t, can be fitted with the equation, $f(t) = a^{b * x}$, where a = 26.29 and b = -2.621. The leakage current through the gate of the doping modulated CNT

synapstor is < 1 pA and can therefore be neglected, as can the power consumption induced by the input spike applied on the device's gate electrode. The average EPSC of a doping modulated CNT synapstor, generated by a single spike, is ~12 nA. The average power consumption of the doping modulated CNT synapstor is estimated to be 1.2 nW/spike.

The same testing was done on the control devices of the doping modulated CNT synapstor. For the doping modulated CNT synapstor, electrons move from the CNT channel into the Al_2O_3 dielectric layer when a positive voltage input spike is applied on the gate electrode. When these electrons become trapped in the defects in the Al_2O_3 dielectric layer, the hole concentration in the p-type CNTs in the channel increases, causing a transient PSC through the CNT channel. After the spike, the electrons move back to their original locations near the CNT channel, decreasing the hole concentration in the CNT channel, thereby decreasing the PSC back to its baseline value of ~0 A. Applying a positive voltage spike on the gate of the control device, with its CNT channel covered by an SU-8 polymer layer, generated a PSC in similar fashion. However, the control device had a high device baseline current, causing the I&F circuit to generate output spikes before and after the positive voltage input spike was applied on the gate electrode. The increased device baseline current also results in an increased power consumption (4.6 nW/device) for the device. This high baseline current is due to the lack of a p-n junction potential barrier in the CNT channel, and a Schottky barrier at the interface of the CNT channel and the Au electrode. In the case of the control device, capped entirely with Al_2O_3 deposited by ALD at 90 C, there was no PSC generated when an input spike was applied on the gate electrode of the control device. Based upon the experimental results, the PSC generated by the doping modulated CNT synapstor is related to the electrons trapped in the Al_2O_3 dielectric layer. Applying a positive voltage input spike on the gate electrode of the Al_2O_3 capped control device

also causes electrons to move from the CNT channel into the Al_2O_3 dielectric layer. However, electrons are the carriers in the n-type CNTs, which are repelled by these attracted electrons due to the applied gate voltage. As a result, no PSC was triggered in the Al_2O_3 capped control device.

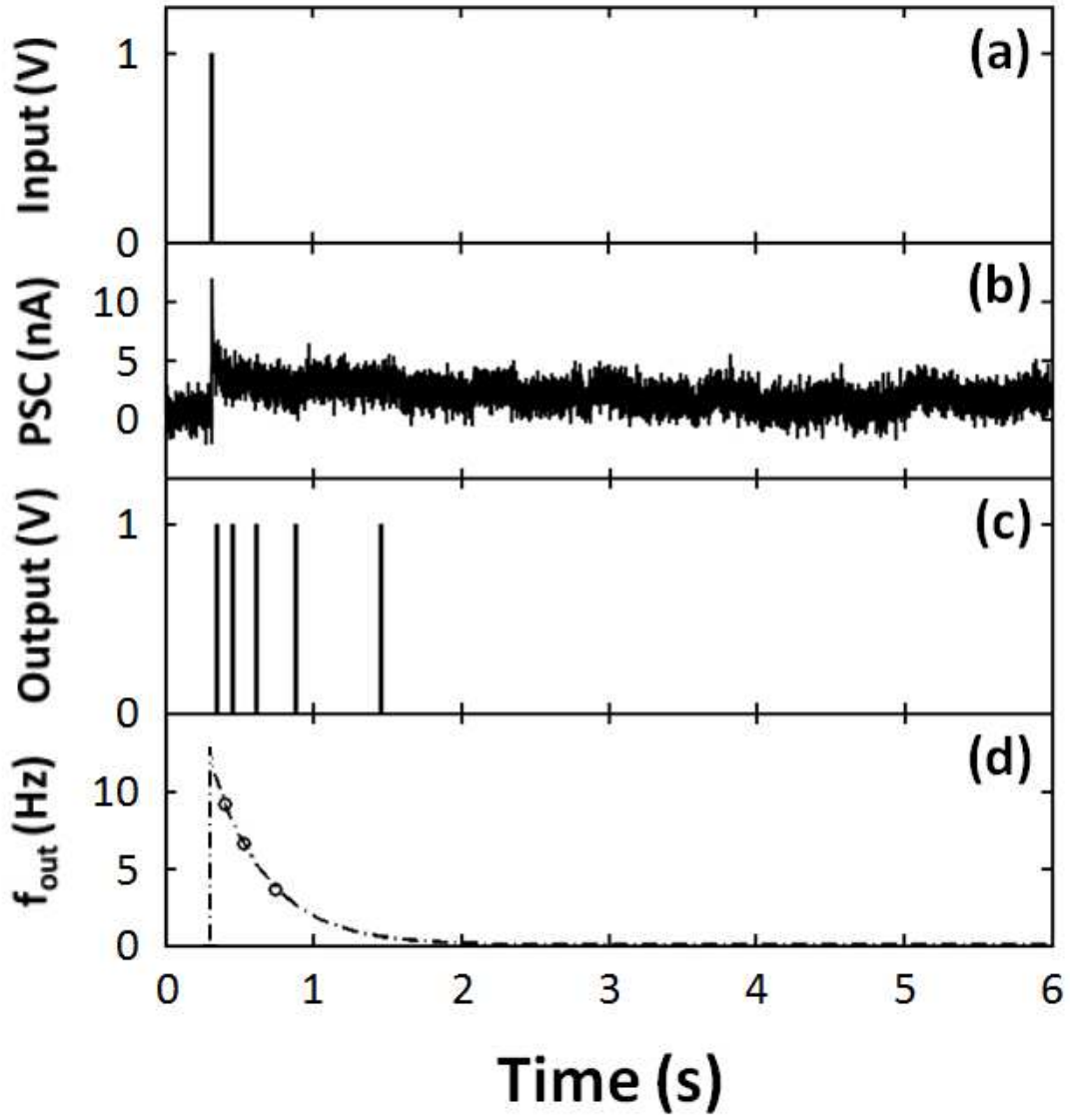

Figure 3.6. (a) A single input spike is applied on an excitatory doping modulated carbon nanotube (CNT) synapstor. (b) The EPSC, generated by the doping modulated CNT synapstor, is

plotted versus time. (c) The series of output spikes, generated by the integrate-and-fire (I&F) circuit, is shown versus time. (d) The firing rate of output spikes is shown versus time. The dashed line represents the best fit of the plotted data.

The doping modulated CNT synapstor can be tuned by applying voltage spikes on its gate electrode. A series of 50 tuning spikes, with amplitude of 3 V or -3 V and duration of 1 ms, was applied on the gate electrode of a doping modulated CNT synapstor to test its plasticity under a source-drain voltage, V_{ds} = 0.2 V. A reading pulse, with amplitude of 2.25 V and duration of 1 ms, was applied on the gate electrode of the CNT synapstor between each tuning pulse. The resulting output spikes, generated by the I&F circuit, were measured and recorded. The output spikes generated by 18, 22, and 25 tuning spikes of amplitude -3 V, is shown in **Figure 3.7a-c**. **Figure 3.7d** shows how the average frequency of output spikes, f_{out}, changes with the total number of -3 V tuning pulses applied on the doping modified CNT synapstor. As more -3 V tuning pulses are applied to the device, f_{out} decreases from ~45 Hz to 0 Hz. The progression of output spikes due to 2, 3, and 4 tuning spikes, with amplitude 3 V, is shown in **Figure 3.7e-g**. **Figure 3.7h** shows f_{out} versus the number of 3 V tuning pulses applied on the device. As more 3 V amplitude tuning pulses are applied to the doping modulated CNT synapstor, f_{out} increases from 0 Hz to ~42 Hz.

The same plasticity test was performed on the control devices of the doping modulated CNT synapstor. In the case of the control device, completely capped with the Al_2O_3 layer, no output spikes were generated (f_{out} = 0) and no tuning effects could be found. For the control device, fully capped with the SU-8 polymer, applying tuning spikes with amplitude of -3 V caused f_{out} to decrease from ~32.5 Hz to ~20.8 Hz. f_{out} increased from ~10.8 Hz to ~20.8 Hz

when tuning spikes, with amplitude of 3 V, were applied to the device. The tuning range of the SU-8 polymer capped control device was much smaller than that of the doping modulated CNT synapstor. It was also found that f_{out} of the SU-8 polymer capped control device could not be tuned to 0 Hz, largely due to its high baseline current.

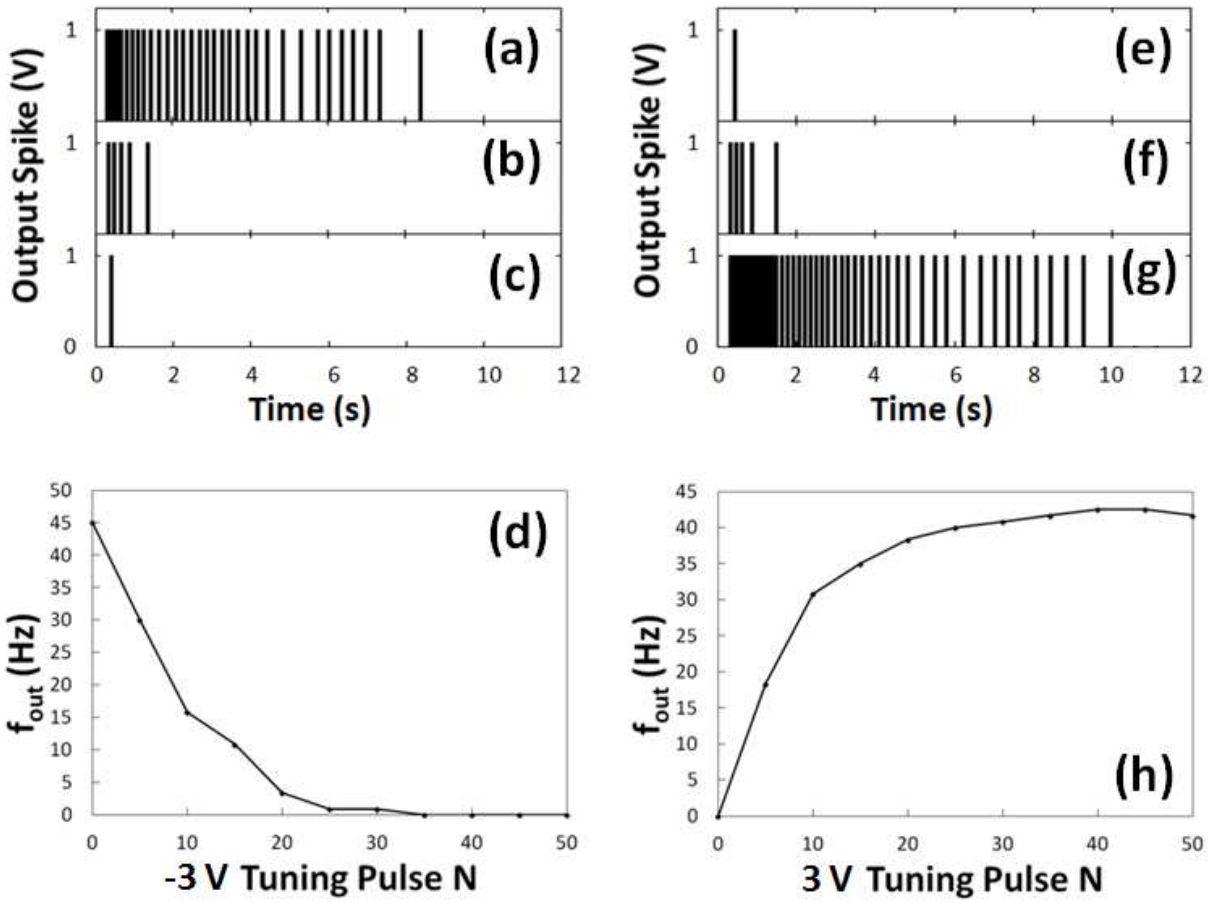

Figure 3.7. A reading pulse, with amplitude 2.25 V and duration 1 ms, is applied to the gate electrode of the doping modulated carbon nanotube (CNT) synapstor before each -3 V or 3 V tuning pulse. This sequence was repeated 50 times. (a) The series of output spikes generated from the 18th reading pulse. (b) The series of output spikes generated from the 22nd reading

pulse. (c) The series of output spikes generated from the 25th reading pulse. (d) The frequency of output spikes, f_{out}, is shown versus the number of applied -3 V tuning pulses. (e) The series of output spikes generated from the 2nd reading pulse. (f) The series of output spikes generated from the 3rd reading pulse. (g) The series of output spikes generated from the 4th reading pulse. (h) The frequency of output spikes, f_{out}, is shown versus the number of applied -3 V tuning pulses.

3.5. Control Device Fabrication

Schematics of the control devices for the doping modulated carbon nanotube (CNT) synapstor and their energy level diagrams (**Figure 3.8a** and **Figure 3.9a**) are shown in **Figure 3.8b** and **Figure 3.9b**. Two different control devices, with the same structure as the doping modulated CNT synapstor, were fabricated by using the same processes as for the CNT synapstor. The control device was fabricated on a Si substrate with a 300-nm-thick layer of SiO_2 grown thermally on top. The back gate was fabricated by depositing a 5-nm-thick layer of Ti and an 80-nm-thick layer of Al via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. The device's dielectric layer is comprised of a 25-nm-thick layer of Al_2O_3, deposited by atomic layer deposition (ALD) at 250C. This layer of Al_2O_3 is patterned using polyimide (PI) and AZ 5214 photoresist, then etched using a solution of 4% phosphoric acid mixed with 96% deionized water. Following the deposition of a monolayer of APTES onto the surface of the Al_2O_3 layer, a random network of single-wall p-type semiconducting CNTs is deposited onto the surface of the APTES-coated Al_2O_3 via dry coating. In this dry coating method, the sample is placed on a hotplate at 90C. The CNT solution is dropped onto the sample and allowed to dry. This CNT network is patterned, using AZ 5214 photoresist and oxygen plasma etching, to form a 15-µm-wide and 6-µm-long transistor channel. The CNT transistor

channel is connected with source and drain electrodes, composed of a 5-nm-thick layer of Ti and an 50-nm-thick layer of Au, deposited via electron beam evaporation at rates of 0.5 Å/s and 1.0 Å/s, respectively. The final step is to cover the entire CNT channel areas of the control devices. One of the control devices has a 2-μm-thick layer of SU-8 polymer deposited and patterned to cover the CNT channel area. The other control device has a 20-nm-thick layer of Al_2O_3, deposited via ALD at 90C, covering the CNT channel area.

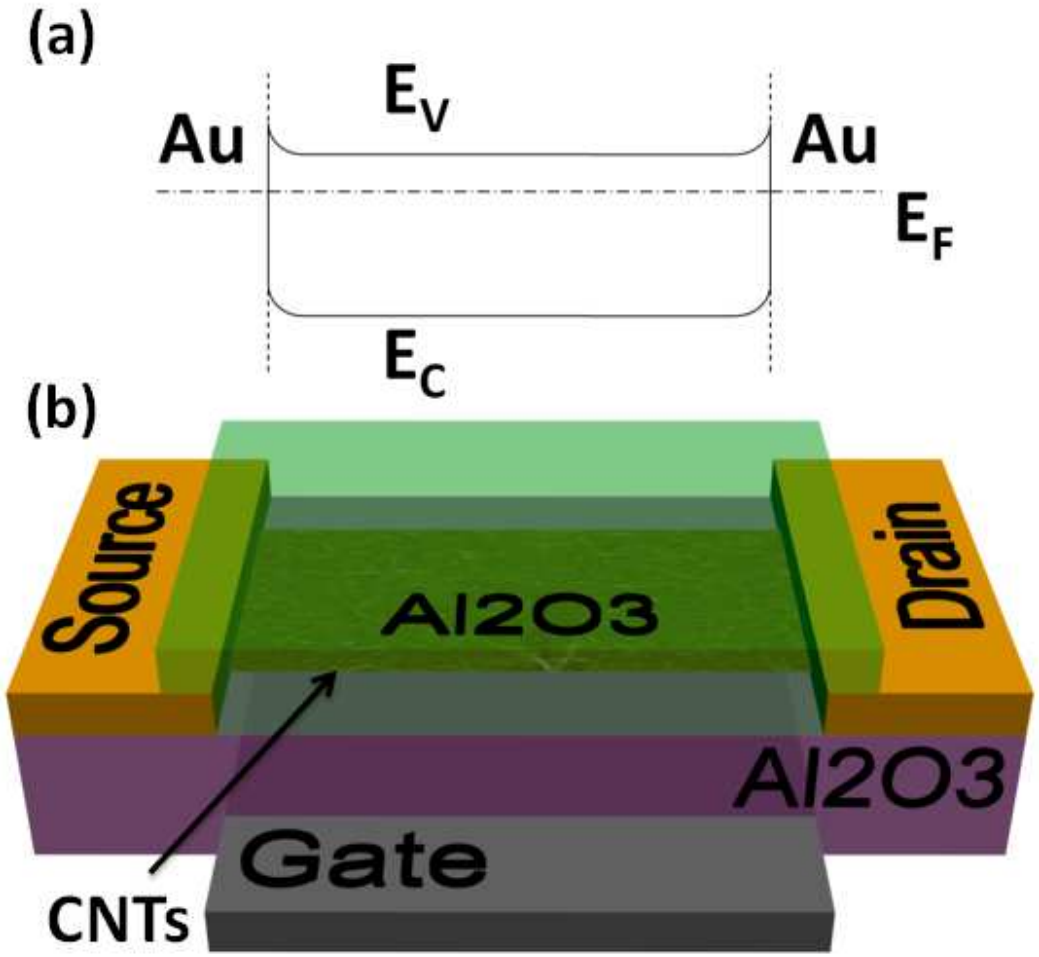

Figure 3.8. (a) The energy level diagram for the Al_2O_3 capped control device. (b) A schematic of an aluminum oxide (Al_2O_3) capped control device for the doping modulated carbon nanotube (CNT) synapstor, composed of an Al_2O_3 dielectric layer and a device channel composed of a random carbon nanotube (CNT) network, bookended by source and drain electrodes. The entire CNT network is capped with a layer of Al_2O_3 deposited by atomic layer deposition at 90 C.

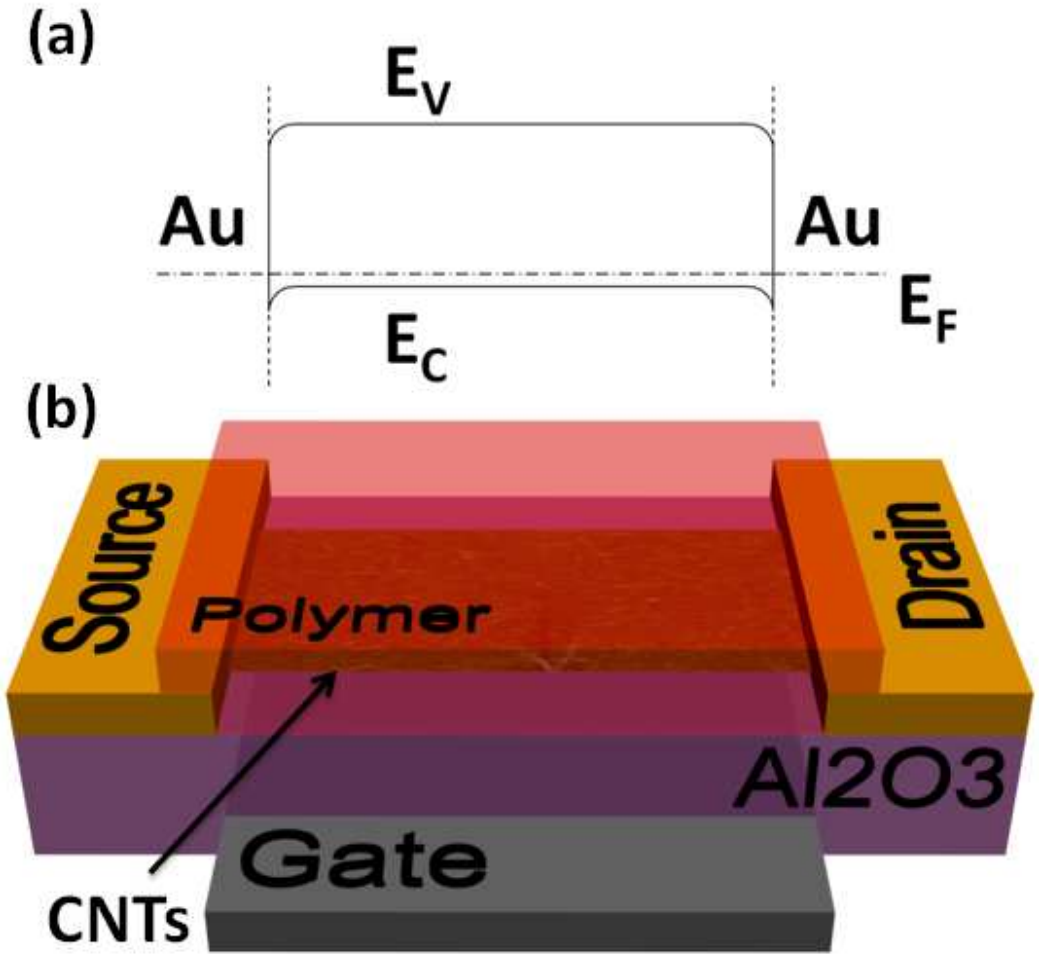

Figure 3.9. (a) The energy level diagram for the SU-8 polymer capped control device. (b) A schematic of an SU-8 polymer capped control device for the doping modulated carbon nanotube (CNT) synapstor, composed of an Al_2O_3 dielectric layer and a device channel composed of a random carbon nanotube (CNT) network, bookended by source and drain electrodes. The entire CNT network is capped with a layer of SU-8 polymer.

3.6. Characterization of SU-8 Polymer Capped Control Device

Figure 3.10 shows a typical source-drain electrode current, I_{ds}, versus source-drain electrode voltage, V_{ds}, for a control device of the doping modulated CNT synapstor, which has the entire CNT channel capped with a SU-8 polymer layer. This measurement was done with the gate voltage, V_g, fixed at 0 V. The I_{ds}-V_{ds} plot shows that the magnitude of the device current increases with the magnitude of the source-drain voltage. This means that the carrier concentration in the CNT channel will increase, regardless of what polarity voltage bias is applied to the drain electrode of the control device. When the carrier concentration in the CNT channel increases, so does the device current through the channel. The leakage current through the device was negligible, as it was < 1 pA. When a negative source-drain voltage, $V_{ds} < 0$ V, was applied on the drain electrode of the control device, the energy band (shown in **Figure 3.10**, inset on the left) was bent upward. This resulted in a reduction of the contact barriers between the CNT channel and the Au electrodes. Carriers were then able to flow through the CNT channel, between the source and drain electrodes, more easily, increasing the device current. When a positive source-drain voltage, $V_{ds} > 0$ V, was applied on the drain electrode of the control device, the energy band (shown in **Figure 3.10**, inset on the right) was bent downward. This resulted in an even larger reduction of the contact barriers between the CNT channel and the Au electrodes. Carriers were then able to flow through the CNT channel even more easily, resulting in even higher device currents.

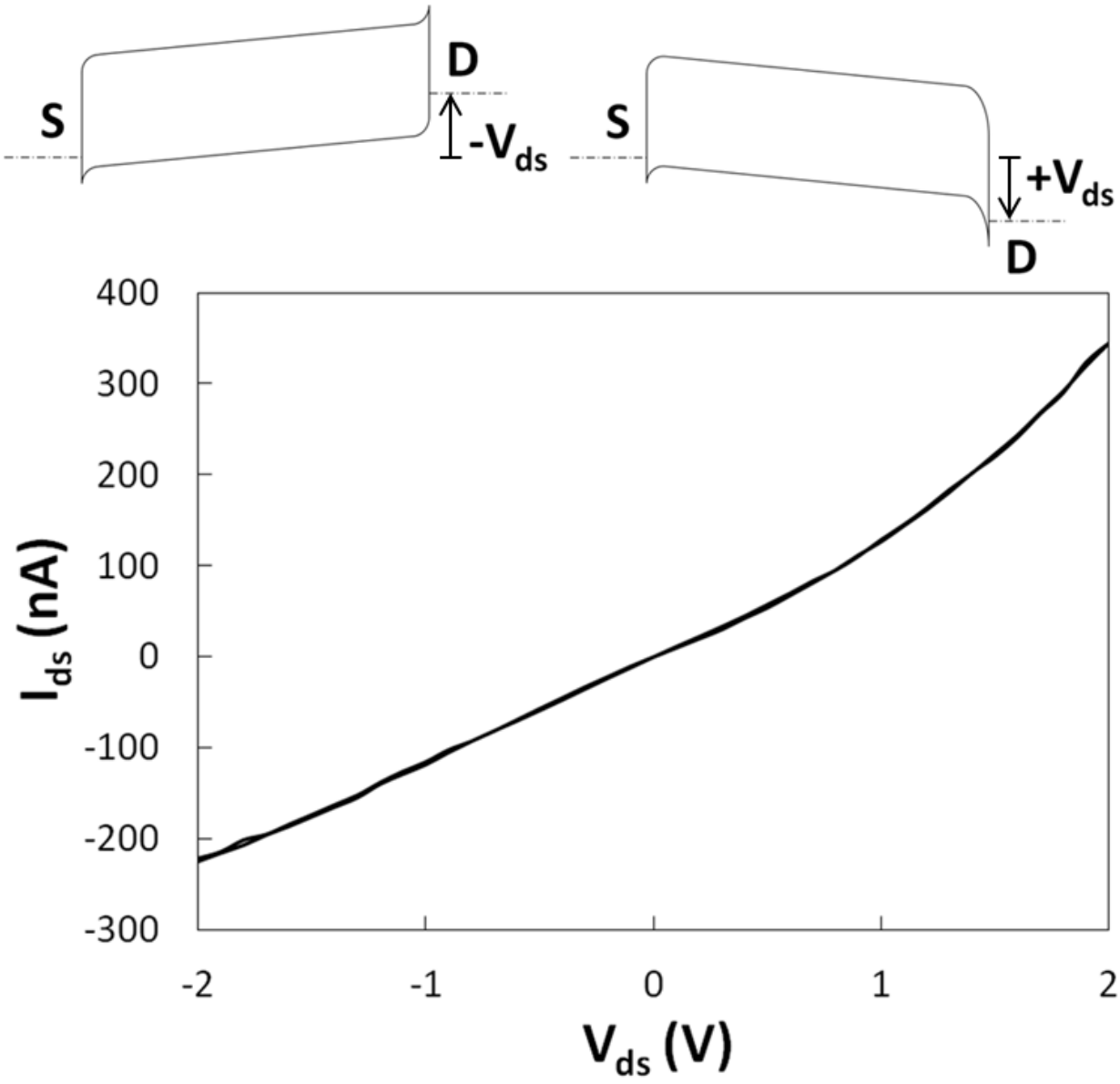

Figure 3.10. The source-drain current, I_{ds}, of the SU-8 polymer capped control device for the doping modulated carbon nanotube (CNT) synapstor is shown versus the source-drain voltage, V_{ds}, which is swept from -2 V to 2 V to -2 V. The insets at the top show the energy level diagrams for the SU-8 polymer capped control device are shown when $V_{ds} < 0$ V (left) and when $V_{ds} > 0$ V (right).

Figure 3.11a shows a typical source-drain electrode current, I_{ds}, versus gate electrode voltage, V_g, for a control device of the doping modulated CNT synapstor, which has the entire CNT channel capped with a SU-8 polymer layer. This measurement was done with the source-drain voltage, V_{ds}, fixed at 0.5 V. When a negative gate voltage, $V_g < 0$ V, was applied on the control device, the energy band (shown in **Figure 3.11**, inset on the left) was bent upward. This resulted in a reduction of the contact barriers at the interface between the CNT channel and the Au electrodes. Holes were able to move through the CNT channel, between the source and drain electrodes, increasing the device current. When a positive gate voltage, $V_g > 0$ V, was applied on the control device, the energy band (shown in **Figure 3.11**, inset on the right) was bent downward. This resulted in an increase in the contact barriers at the interface between the CNT channel and the Au electrodes. This makes it more difficult for holes to move through the CNT channel, between the source and drain electrodes, reducing the device current.

The control device of the doping modulated CNT synapstor, which has the entire CNT channel capped with a SU-8 polymer layer, showed memory characteristics. When V_g was swept from -5 V to 5 V, with V_{ds} fixed at 0.5 V, the device current decreased, turning the device off. The device current increased, turning the device on, when was swept from 5V to -5V. This resulted in a counter-clockwise hysteresis loop in the I_{ds}-V_g plot. During the forward sweep, the control device's I_{ds} = ~0 nA when V_g = 0 V. However, during the backward sweep, the control device's I_{ds} = ~8 nA when V_g = 0 V. Applying voltages on the gate electrode of the control device causes charges to build up in the aluminum oxide (Al_2O_3) dielectric layer (**Figure 3.11b** and **c**), causing this memory effect. The leakage current through the gate of the control device was negligible, as it was < 1 pA.

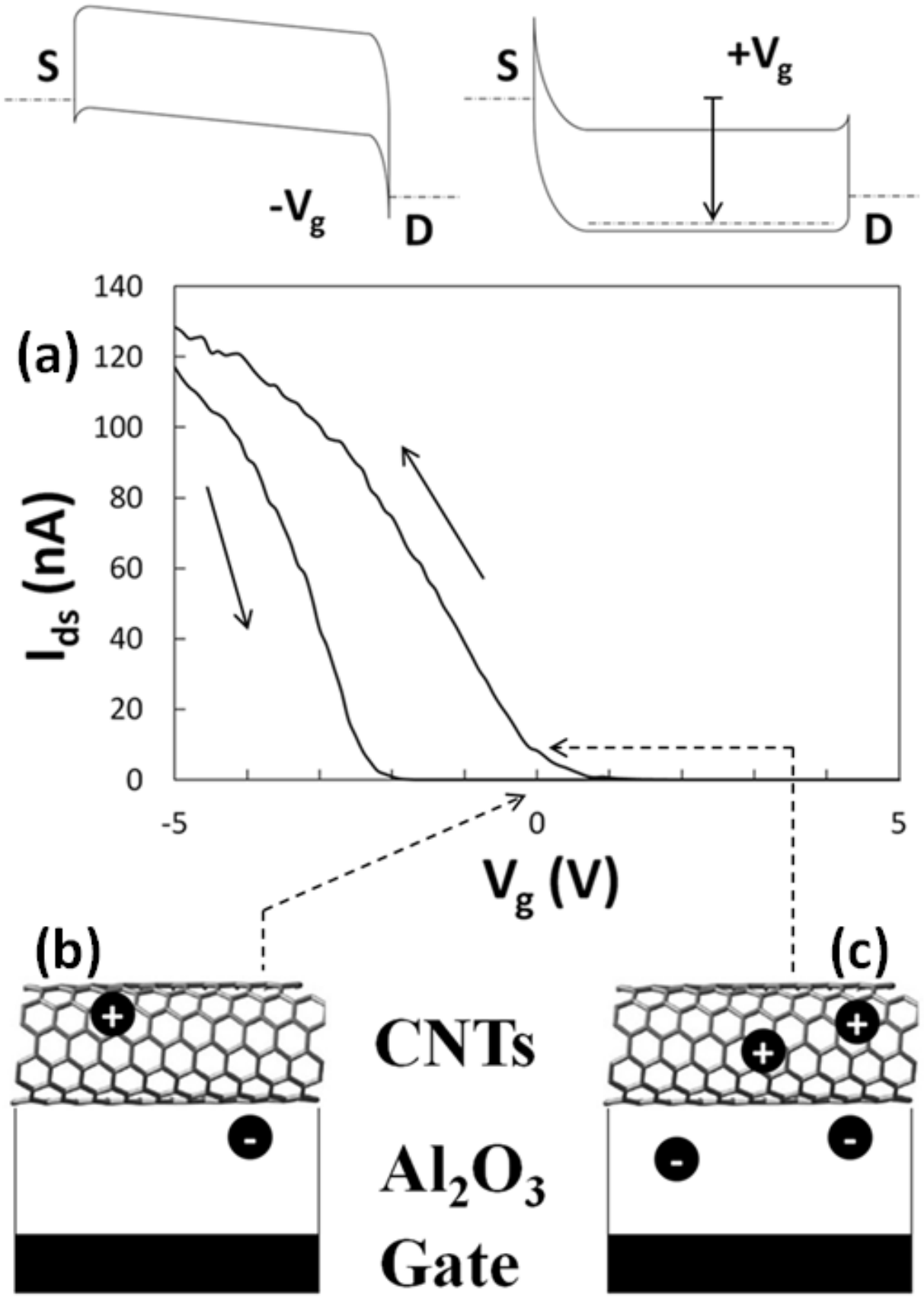
S
-Vg
D
S
+Vg
D
(a)
140
120
100
80
60
40
20
0
Ids (nA)
-5
0
5
Vg (V)
(b)
(c)
CNTs
Al2O3
Gate

Figure 3.11. (a) The source-drain current, I_{ds}, of the SU-8 polymer capped control device for the doping modulated carbon nanotube (CNT) synapstor is shown versus the gate voltage, V_g, which is swept from -5 V to 5 V to -5 V. The inset at the top shows the energy level diagrams for the SU-8 polymer capped control device are shown when $V_g < 0$ V (left) and when $V_g > 0$ V (right). (b) A schematic showing the concentration of holes ("+" circles) in the CNT channel when $V_g < 0$ V. (c) A schematic showing the concentration of holes ("+" circles) in the CNT channel when $V_g > 0$ V.

A typical excitatory control device for the doping modulated CNT synapstor, which has the entire CNT channel capped with a SU-8 polymer layer, induces an excitatory postsynaptic current (EPSC). The operation of such a device, operated with a source-drain voltage, $V_{ds} = 0.2$ V, is described in **Figure 3.12**. A single input spike, with amplitude $V_g = 2.25$ V and duration of 1 ms, is applied on the gate electrode of the control device (**Figure 3.12a**), which generates an EPSC (**Figure 3.12b**). The peak amplitude of the EPSC is ~4 nA above the baseline current. After the spike, the device current gradually decays back to the baseline current over a duration of approximately 5.0 s. The generated EPSC flows to the integrate-and-fire (I&F) circuit, generating output spikes (**Figure 3.12c**). As can be seen from **Figure 3.12d**, decreased EPSC results in decreased firing rates of the output spikes. The firing rate of the output spikes continues to decrease until the EPSC decreases below a preset threshold value, V_{th}, that is set in the I&F circuit. When the EPSC becomes smaller than V_{th}, output spikes will no longer be generated. In the case shown in **Figure 3.12**, output spikes are generated even before the input spike is applied due to the control device's baseline current being above the preset threshold value.

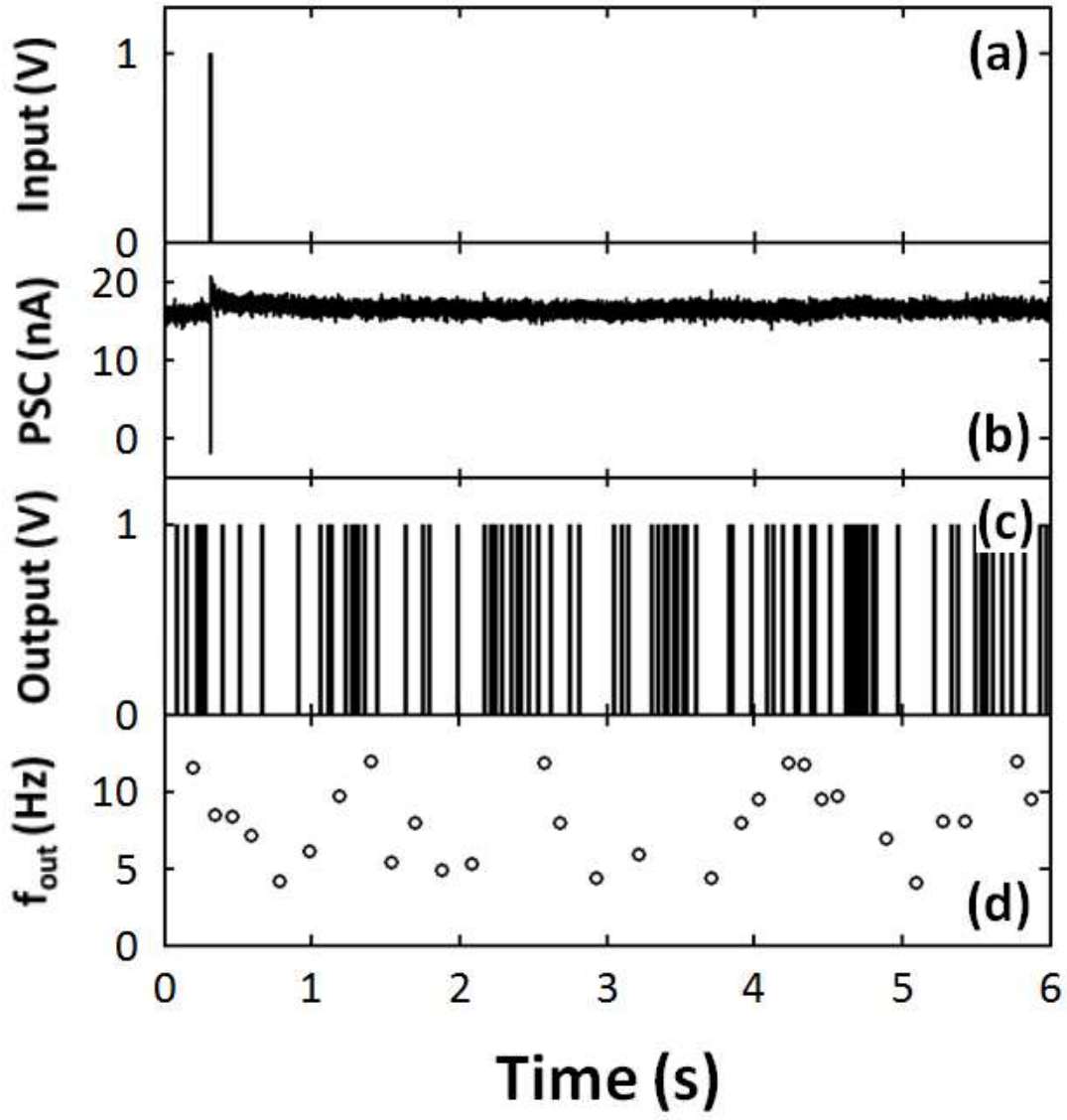

Figure 3.12. (a) A single input spike is applied on an excitatory SU-8 polymer capped control device of the doping modulated carbon nanotube (CNT) synapstor. (b) The EPSC, generated by the control device, is plotted versus time. (c) The series of output spikes, generated by the integrate-and-fire (I&F) circuit, is shown versus time. (d) The firing rate of output spikes is shown versus time.

The control device for the doping modulated CNT synapstor, which has the entire CNT channel capped with a SU-8 polymer layer, was also tested for plasticity characteristics. This was tested in the same way as the doping modulated CNT synapstor. A series of 50 tuning spikes, with amplitude of 3 V or -3 V and duration of 1 ms, was applied on the gate electrode of a SU-8 polymer capped control device under a source-drain voltage, V_{ds} = 0.2 V. A reading pulse, with amplitude of 2.25 V and duration of 1 ms, was applied on the gate electrode of the control device between each tuning pulse. The resulting output spikes, generated by the I&F circuit, were measured and recorded. **Figure 3.13a** shows how the average frequency of output spikes, f_{out}, changes with the total number of -3 V tuning pulses applied on the control device. As more -3 V tuning pulses are applied to the device, f_{out} decreases from ~32.5 Hz to ~20.8 Hz. **Figure 3.13b** shows f_{out} versus the number of 3 V tuning pulses applied on the device. As more 3 V amplitude tuning pulses are applied to the doping modulated CNT synapstor, f_{out} increases from ~10.8 Hz to ~20.8 Hz. In either case, tuning with -3 V or 3 V gate pulses, no clear trend can be seen from the plots.

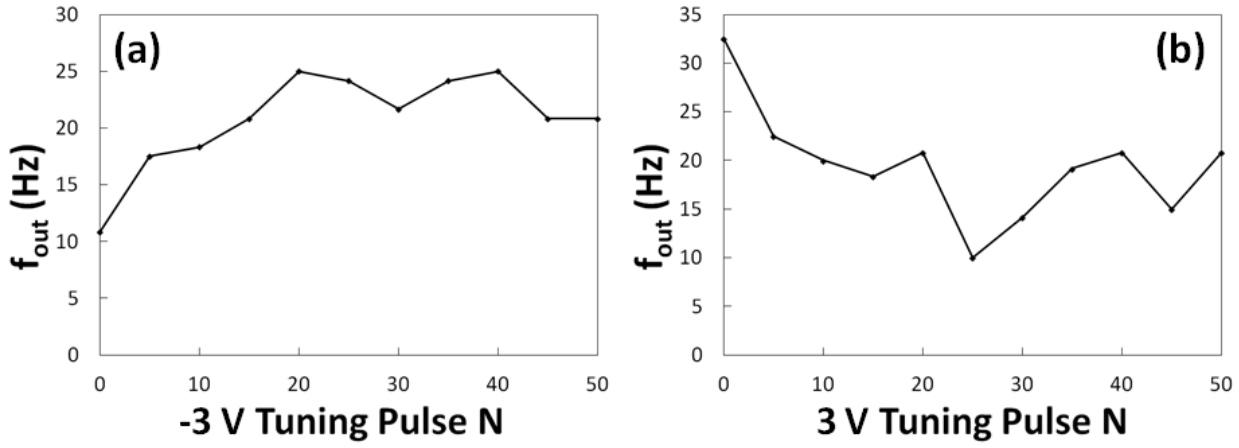

Figure 3.13. A reading pulse, with amplitude 2.25 V and duration 1 ms, is applied to the gate electrode of the SU-8 polymer capped control device for the doping modulated carbon nanotube (CNT) synapstor before each -3 V or 3 V tuning pulse. This sequence was repeated 50 times. (a) The frequency of output spikes, f_{out}, is shown versus the number of applied -3 V tuning pulses. (b) The frequency of output spikes, f_{out}, is shown versus the number of applied -3 V tuning pulses.

3.7. Characterization of Al_2O_3 Capped Control Device

Figure 3.14 shows a typical source-drain electrode current, I_{ds}, versus source-drain electrode voltage, V_{ds}, for a control device of the doping modulated CNT synapstor, which has the entire CNT channel capped with a layer of aluminum oxide (Al_2O_3). This measurement was done with the gate voltage, V_g, fixed at 0 V. The I_{ds}-V_{ds} plot shows that the magnitude of the device current decreases as the source-drain voltage is swept from -2 V to 2 V. This means that the carrier resistance in the CNT channel increases as V_{ds} becomes more positive, decreasing the device current. The leakage current through the device was negligible, as it was < 1 pA. When a negative source-drain voltage, $V_{ds} < 0$ V, was applied on the drain electrode of the control device, the energy band (shown in **Figure 3.14**, inset on the left) was bent upward. This resulted in a reduction of the contact barriers between the CNT channel and the Au electrodes. Carriers were then able to flow through the CNT channel, between the source and drain electrodes, more easily, increasing the device current. When a positive source-drain voltage, $V_{ds} > 0$ V, was applied on the drain electrode of the control device, the energy band (shown in **Figure 3.14**, inset on the right) was bent downward. This resulted in an increase of the contact barriers between the

CNT channel and the Au electrodes. This makes it more difficult for carriers to flow through the CNT channel, resulting in lower device currents.

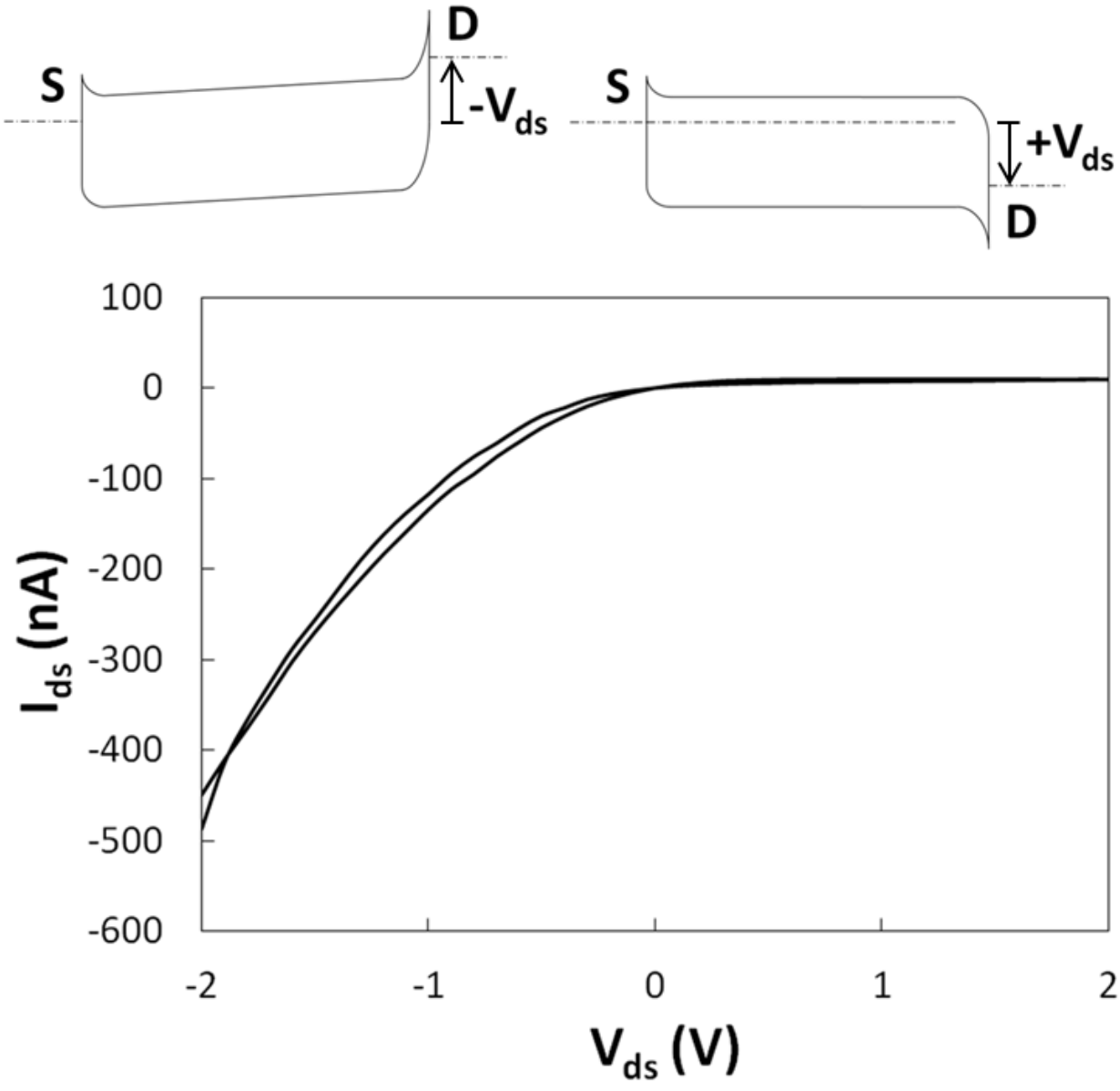

Figure 3.14. The source-drain current, I_{ds}, of aluminum oxide (Al_2O_3) capped control device for the doping modulated carbon nanotube (CNT) synapstor is shown versus the source-drain voltage, V_{ds}, which is swept from -2 V to 2 V to -2 V. The inset at the top shows the energy level

diagrams for the Al_2O_3 capped control device are shown when $V_{ds} < 0$ V (left) and when $V_{ds} > 0$ V (right).

Figure 3.15a shows a typical source-drain electrode current, I_{ds}, versus gate electrode voltage, V_g, for a control device of the doping modulated CNT synapstor, which has the entire CNT channel capped with a layer of Al_2O_3. This measurement was done with the source-drain voltage, V_{ds}, fixed at 0.5 V. When a negative gate voltage, $V_g < 0$ V, was applied on the control device, the energy band (shown in **Figure 3.15**, inset on the left) was bent upward. This resulted in an increase of the contact barriers at the interface between the CNT channel and the Au electrodes. This made it more difficult for carriers to move through the CNT channel, between the source and drain electrodes, reducing the device current. When a positive gate voltage, $V_g > 0$ V, was applied on the control device, the energy band (shown in **Figure 3.15**, inset on the right) was bent downward. This resulted in a decrease of the contact barriers the interface between the CNT channel and the Au electrodes. Carriers were able to move more easily through the CNT channel, between the source and drain electrodes, increasing the device current.

The control device of the doping modulated CNT synapstor, which has the entire CNT channel capped with a layer of Al_2O_3, showed memory characteristics. When V_g was swept from -5 V to 5 V, with V_{ds} fixed at 0.5 V, the device current increased, turning the device on. The device current decreased, turning the device off, when was swept from 5V to -5V. This resulted in a clockwise hysteresis loop in the I_{ds}-V_g plot. During the forward sweep, the control device's I_{ds} = ~55 nA when V_g = 0 V. However, during the backward sweep, the control device's I_{ds} = ~0 nA when V_g = 0 V. Applying voltages on the gate electrode of the control device causes charges

to build up in the Al_2O_3 dielectric layer (**Figure 3.15b** and **c**), causing this memory effect. The leakage current through the gate of the control device was negligible, as it was < 1 pA.

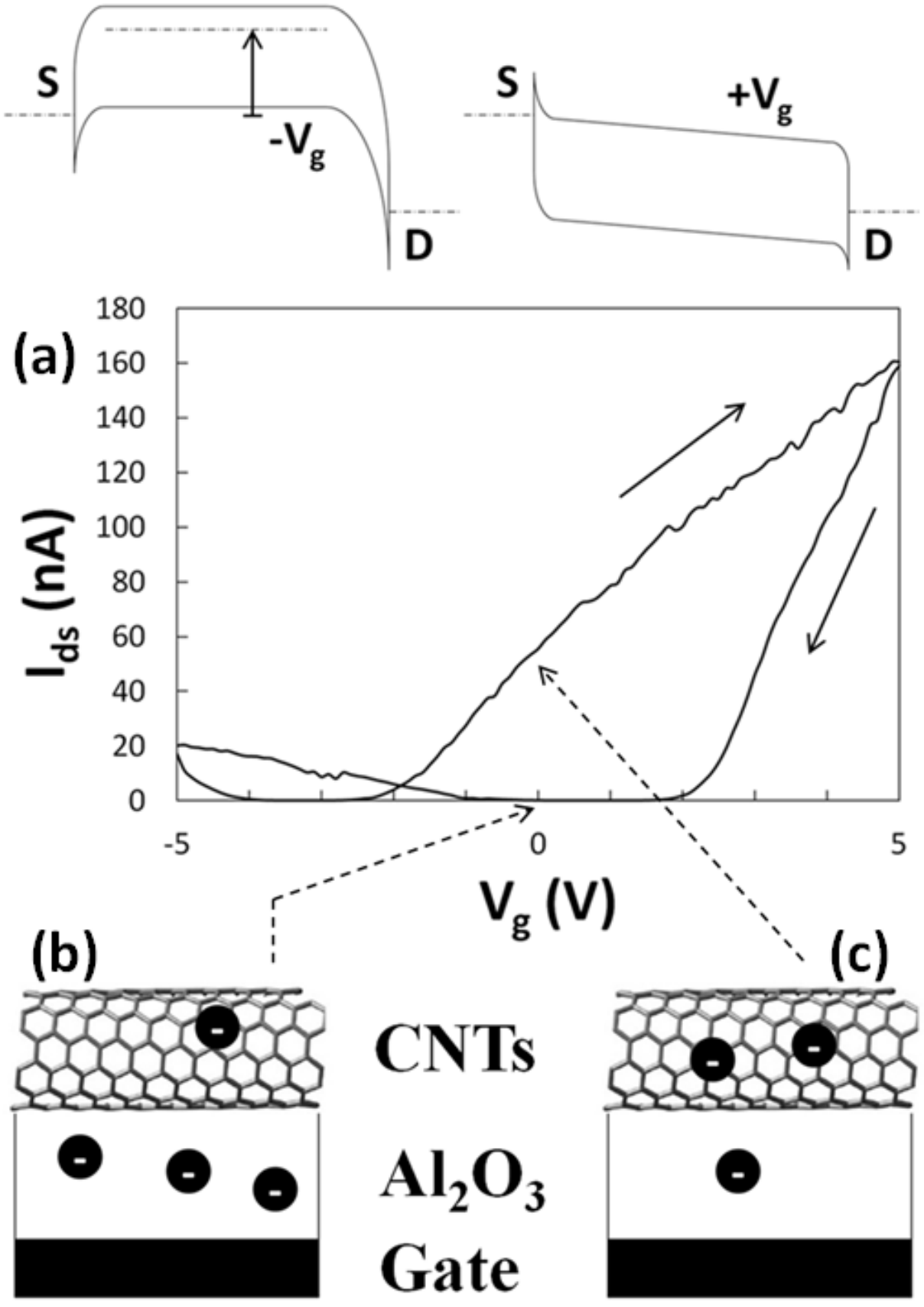
S
-Vg
D
S
+Vg
D
(a)
180
160
140
120
100
80
60
40
20
0
Ids (nA)
-5
0
5
Vg (V)
(b)
(c)
CNTs
Al2O3
Gate

Figure 3.15. (a) The source-drain current, I_{ds}, of the aluminum oxide (Al_2O_3) capped control device for the doping modulated carbon nanotube (CNT) synapstor is shown versus the gate voltage, V_g, which is swept from -5 V to 5 V to -5 V. The inset at the top shows the energy level diagrams for the Al_2O_3 capped control device are shown when $V_g < 0$ V (left) and when $V_g > 0$ V (right). (b) A schematic showing the concentration of electrons ("-" circles) in the CNT channel when $V_g < 0$ V. (c) A schematic showing the concentration of electrons ("-" circles) in the CNT channel when $V_g > 0$ V.

The operation of a typical control device for the doping modulated CNT synapstor, which has the entire CNT channel capped with a layer of Al_2O_3, operated with a source-drain voltage, $V_{ds} = 0.2$ V, is described in **Figure 3.15**. A single input spike, with amplitude $V_g = 2.25$ V and duration of 1 ms, is applied on the gate electrode of the control device (**Figure 3.15a**), which generates a PSC (**Figure 3.15b**). The CNTs in the Al_2O_3 capped control device are n-type, causing the device to behave inversely to the SU-8 capped control device and doping modulated CNT synapstor, which have device channels comprised of p-type CNTs. The positive voltage input spike causes the device current of the Al_2O_3 capped control device to decrease. When this PSC flows to the integrate-and-fire (I&F) circuit, no output spikes are generated because the preset threshold value is never reached.

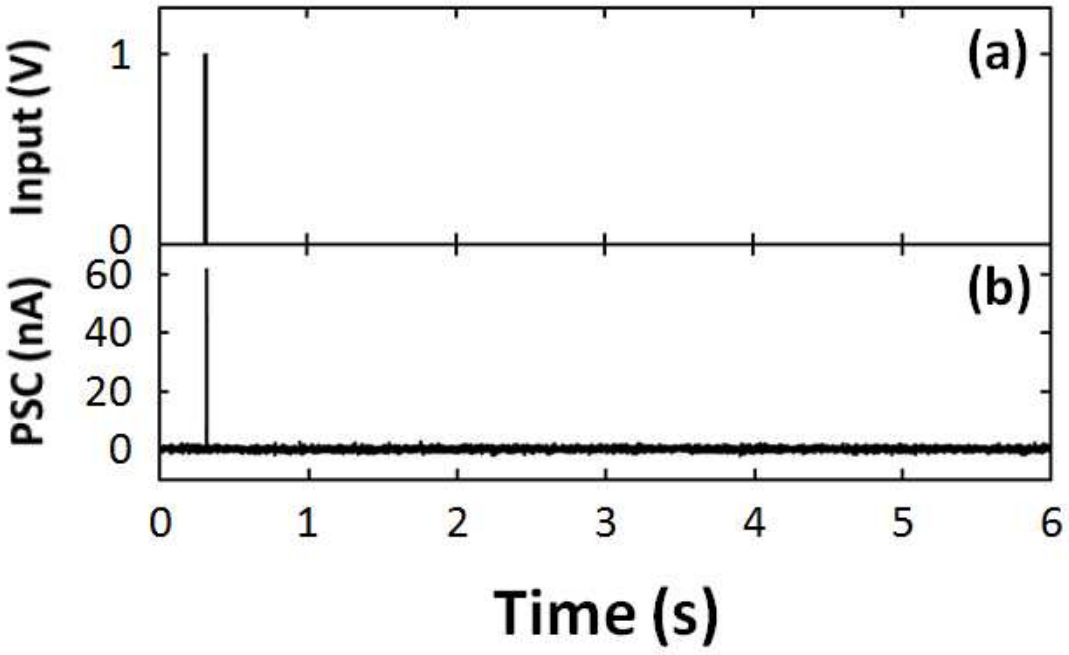

Figure 3.16. (a) A single input spike is applied on an excitatory aluminum oxide (Al_2O_3) capped control device of the doping modulated carbon nanotube (CNT) synapstor. (b) The EPSC, generated by the control device, is plotted versus time.

The control device for the doping modulated CNT synapstor, which has the entire CNT channel capped with a layer of Al_2O_3, was also tested for plasticity characteristics. This was tested in the same way as the doping modulated CNT synapstor. A series of 50 tuning spikes, with amplitude of 3 V or -3 V and duration of 1 ms, was applied on the gate electrode of an Al_2O_3 capped control device under a source-drain voltage, V_{ds} = 0.2 V. A reading pulse, with amplitude of 2.25 V and duration of 1 ms, was applied on the gate electrode of the control device between each tuning pulse. The resulting output spikes, generated by the I&F circuit, were measured and recorded. **Figure 3.16a** shows how the average frequency of output spikes, f_{out},

changes with the total number of -3 V tuning pulses applied on the control device. As stated, the Al_2O_3 capped control device has a device channel comprised of n-type CNTs. Thus, positive voltage pulses applied on the gate electrode of the control device decreases the device current, below the preset threshold value of the I&F circuit, making it difficult to generate output spikes. This is true in either case, tuning with -3 V or 3 V gate pulses, making it difficult to find any clear trends from the output spike frequencies. Before starting the tuning tests, with -3 V amplitude gate pulses, the control device's baseline current was high enough to trigger output spikes. This can be seen in **Figure 3.16a**. However, the positive voltage gate pulses quickly decreased the device current below the threshold value, bringing the output spike frequency to zero.

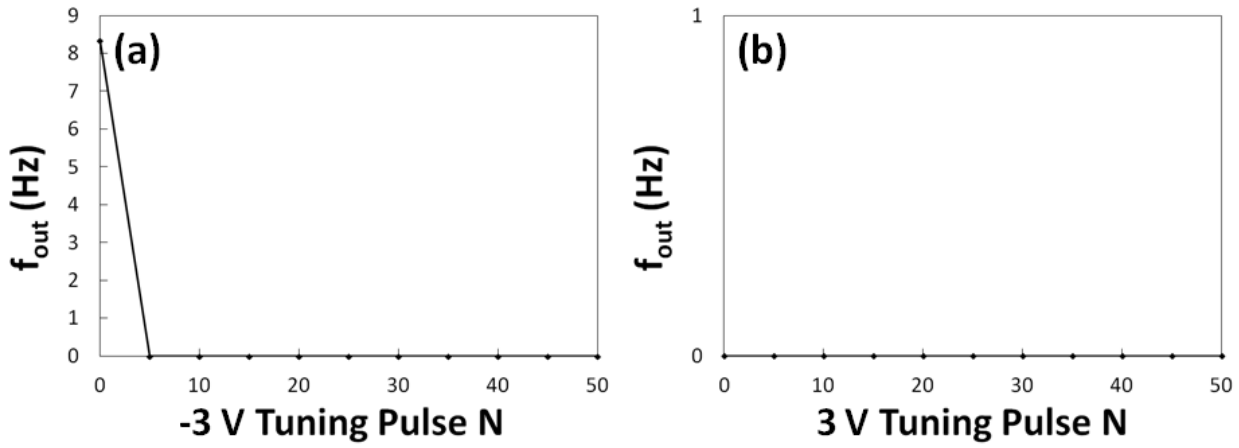

Figure 3.17. A reading pulse, with amplitude 2.25 V and duration 1 ms, is applied to the gate electrode of the aluminum oxide (Al_2O_3) capped control device for the doping modulated carbon nanotube (CNT) synapstor before each -3 V or 3 V tuning pulse. This sequence was repeated 50 times. (a) The frequency of output spikes, f_{out}, is shown versus the number of applied -3 V tuning pulses. (b) The frequency of output spikes, f_{out}, is shown versus the number of applied -3 V tuning pulses.

3.8. Summary

A carbon nanotube (CNT) based synapstor, with a structure similar to a field-effect transistor, was developed to emulate the biological synapse. The device channel was fabricated by depositing a random network of p-type CNTs. Aluminum oxide (Al_2O_3) was deposited, via atomic layer deposition (ALD) at 90 C, on top of half of the CNT channel. This converted the p-type CNTs to n-type, creating a p-n junction in the CNT channel, and a Schottky barrier at the interface of the n-type CNTs and the gold (Au) drain electrode. The presence of the p-n junction potential barrier and the Schottky barrier resulted in a reduction of the device's baseline current. This led to an improved ratio between the postsynaptic current (PSC) and the baseline current, decreased the power consumption of the device, and expanded the plasticity and tunability range. These doping modulated CNT synapstors were integrated into a neuromorphic circuit, along with silicon (Si) based integrate-and-fire (I&F) circuits. These neuromorphic circuits could be scaled up and emulate the biological neural network with high speed parallel signal processing, low power consumption, learning, and memory properties.

References:

1. Indiveri, G., In A Low-Power Adaptive Integrate-and-Fire Neuron Circuit. *IEEE Int. Symp. Circuits Syst.* **2003**, pp. IV-820-IV-823 vol. 4.

CHAPTER 4: SUMMARY

4.1. Conclusion

Two carbon nanotube (CNT) based electronic devices, called "synapstors," were presented. These CNT synapstors were fabricated to emulate the functions of a biological synapse, capable of analog spike signal processing with low power consumption. These synaptic devices, like biological synapses, are capable of logic, learning, and memory in a single element. The CNT synapstors have a field-effect transistor structure, utilizing a random network of single-wall semiconducting CNTs as its conductive channel. These CNT synapstors were integrated, along with silicon (Si) based integrate-and-fire (I&F) circuits, to create analog spike neuromorphic circuits. These neuromorphic circuits were developed with the goal of emulating the biological neural network, capable of high speed parallel signal processing, dynamic learning and memory, and low power consumption.

The operation of such a neuromorphic circuit is described as follows. A voltage spike is applied on the gate electrode of a CNT synapstor, inducing a change in the charge carrier concentration. This, in turn, generates a postsynaptic current (PSC) via the CNT channel of the device. The CNT synapstors can be excitatory or inhibitory, generating excitatory PSCs (EPSC) or inhibitory PSCs (IPSC), relatively. Multiple input spikes can be applied on individual CNT synapstors, connected together in the neuromorphic circuits. The collective PSCs, generated by the CNT synapstors, flow to a I&F circuit, where they are integrated with respect to time by a capacitor. When this integration reaches a threshold value, an output spike is generated, and the integration of the PSC restarts.[1]

The created CNT synapstors are scalable and integratable with complementary metal-oxide-semiconductor (CMOS) technology. The analog spike neuromorphic circuit, based on such CNT synapstors, could be scaled up to achieve signal processing speed superior to that of supercomputers, while consuming far less power. Such neuromorphic circuits could find applications that supercomputers are still incapable of, in fields such as unmanned aerial vehicles, telecommunications networks, robotics, distributed sensing networks, and voice recognition.

References:

1. Indiveri, G., In A Low-Power Adaptive Integrate-and-Fire Neuron Circuit. *IEEE Int. Symp. Circuits Syst.* **2003**, pp. IV-820-IV-823 vol. 4.