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Analysis and Design of High-Speed ADCs

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Analysis and Design of High-Speed ADCs

A dissertation submitted in partial satisfaction
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Doctor of Philosophy in Electrical Engineering

by

Seyedeh Sedigheh Hashemi

2013

Abstract of the Dissertation

Analysis and Design of High-Speed ADCs

by

Seyedeh Sedigheh Hashemi

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2013

Professor Behzad Razavi, Chair

High-speed analog-to-digital converters (ADCs) are at the heart of many applications such as digital communication, video, and instrumentation. However, the power efficiency of ADCs tends to degrade as higher speeds and/or resolutions are sought. In this research, we introduce a low-power high-speed pipelined ADC architecture that employs a precharged resistor-ladder digital-to-analog converter (RDAC) and a multi-bit front end with a low-gain op amp. Avoiding the need for op amp nonlinearity calibration, the ADC only computes the gain errors and corrects them in the digital domain. In addition, RDAC simplifies the calibration logic and enables high-speed gain error calibration, thus correcting for the incomplete settling of the MDACs. Using simple differential pairs with gains of about 5 as op amps and realized in 65-nm CMOS technology, the 10-bit ADC consumes 36 mW at a sampling rate of 1 GHz and exhibits an FOM of 70 fJ/conv.-step.

A critical issue in the design of high-speed ADCs relates to errors that result from comparator metastability. Studied for only flash architectures, this phenomenon assumes new dimensions in pipelined converters, creating far more

complex error mechanisms. In this dissertation, we present a comprehensive analysis of comparator metastability effects in pipelined ADCs and develop a method to precisely predict the error behavior for a given input signal p.d.f.

The dissertation of Seyedeh Sedigheh Hashemi is approved.

Mau-Chung Frank Chang

Sudhakar Pamarti

Katsushi Arisaka

Behzad Razavi, Committee Chair

University of California, Los Angeles

2013

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Acknowledgments

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Finally, I am so grateful for my parents, for their constant love, endless patience, and never-ending knowledge.

Vita

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CHAPTER 1

Introduction

Evolving world of the integrated circuits (ICs) mandates improved analog-to-digital converter (ADC) performance, as well as high power efficiency. However, the power efficiency tends to degrade at higher rates [7, 18]. Interleaving can be employed to enhance the speed at the price of high power consumption, limited signal-to-noise-and-distortion ratio (SNDR), and increased input capacitance [21–23]. Therefore, it is desired to architect a single-channel ADC at gigahertz ranges that achieves a high resolution in conjunction with a low power consumption.

Pipelined architecture is one of the best candidates for designing high speed ADCs with medium-to-high resolutions, offering a small input capacitance along with high power efficiency [24]. At high sampling rates, the bottleneck of such an architecture, however, is the design of the operational amplifiers (op amps) used in its front-end stages, both in terms of its limited bandwidth, power, and gain trade-offs, and its nonlinearity. In particular, by emerging new technologies with reduced device dimensions and low supply voltages, the intrinsic gain of transistors, $g_m r_o$, is quite low, resulting in considerable gain error and nonlienarity. Therefore, attempts to employ high-gain high-speed op amps lead to large power penalties. Nonlinearity calibration techniques, on the other hand, pose significant challenges. For example, [25] requires one clock for the ADC and another clock for the sample-and-hold (SHA) and has a limited bandwidth, [26] has a limited dynamic range, and [6] requires a complex polynomial implementation

that consumes about 6 mW at 500 MHz. Therefore, it is desired to avoid op amp nonlinearity.

In this research, we propose a precharged pipelined architecture that utilizes a resistor-ladder digital-to-analog-converter (DAC) in a multi-bit front end with a moderate gain of 2. Due to the reduced signal swing, the nonlinearity is avoided and the op amp is realized as a simple differential pair with resistive loads, perhaps the fastest amplifier one can build without using inductors. In addition, relying on a highly-linear resistor ladder, the required calibration is simplified and reduced to only gain error correction. The low-voltage architecture in conjunction with a high-speed high-precision resistor-ladder DAC enables calibrating at high clock rates. Thus, the calibration scheme can also capture and correct the dynamic gain errors due to the op amp limited settling. The 10-bit ADC prototype is fabricated in 65-nm CMOS technology and achieves an FOM of 70 fJ/conv.-step at a sampling rate of 1 GHz.

A major issue in the design of high-speed ADCs relates to errors that result from comparator metastability, particularly at high clock rates. Such ADC errors are random and cause bit error rate (BER) and/or sparkles [1]. Fig. 1.1 plots the BER requirements for a number of applications [1]. Moderate to demanding BER specifications are desired in applications such as wireless LAN, ultra-wideband communications, optical communication without error correction, and instrumentation. Pipelined architecture is used in many of these applications. Therefore, it is essential to analyze the effects of comparator metastability in a pipelined ADC. In this dissertation, a comprehensive analysis of the metastability effects in a pipelined environment is presented and different error mechanisms

[1]It should be noted that most communication systems have built-in error detection and correction codes that correct some of the ADC error codes; therefore the analysis of the actual BER degradation due to the ADC metastability is quite difficult and requires a well-analyzed study of the ADC error.

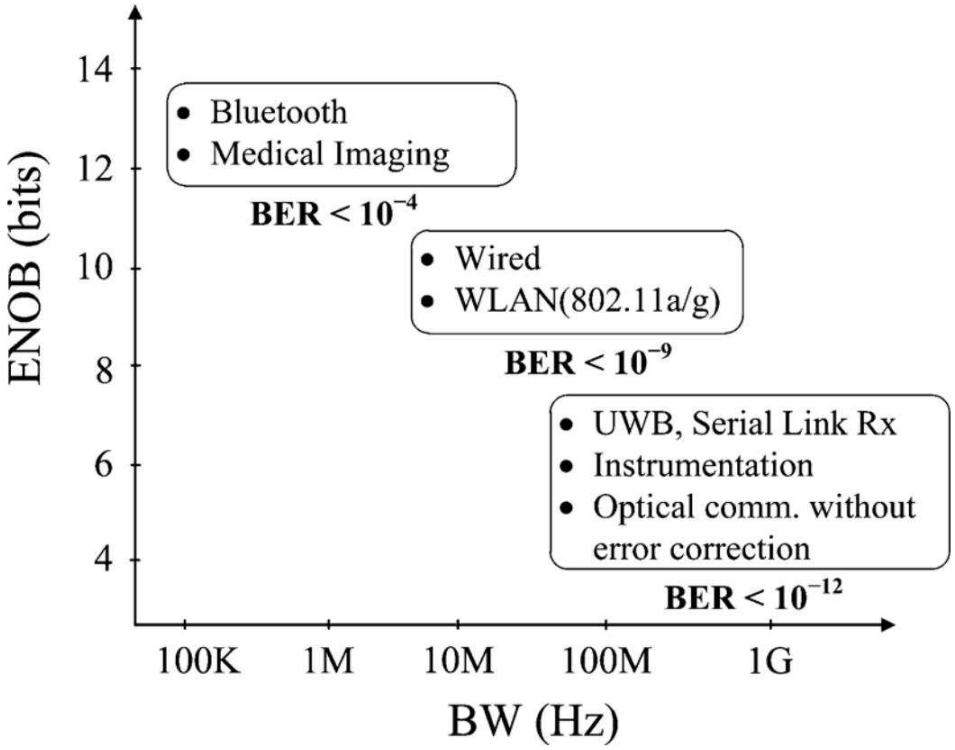


Figure 1.1: BER requirements for different applications [1].

in a pipelined stage are identified. Using the proposed models for MDAC and sub-ADC operations, the metastability error is formulated and the probability of the cumulative error versus the magnitude of error is extracted. In addition, it has been shown that, both the maximum magnitude of error and the probability of error fall exponentially with higher resolutions of the stage, suggesting that using multi-bit stages at the front end, significantly improves the metastability of the ADC system.

The thesis is organized as following: first, in Chapter 2, the proposed ADC architecture is introduced by focusing on two key ideas: the concept of precharged resistor-ladder DAC, and calibration at high clock frequencies. In addition to design details, experimental results are presented in this chapter. Following that, Chapter 3 describes the design and implementation of an 8-bit two-step flash ADC

that employs a precharged resistor-ladder DAC in conjunctions with a number of circuit and system techniques to achive an FOM of about 30 fJ/conv.-step at a sampling rate of 1.2 GHz.

Chapter 4 describes our proposed method to analyze the effects of metastability in a pipelined ADC. Our modeling approach is introduced and developed to formulate different error mechanisms to derive the metastability error behavior. The result is then used to characterize the probability of error versus the magnitude of error for a given input p.d.f. Finally, Chapter 5 summarizes the contributions of this research and suggests some aspects that require more exploration and improvement.

CHAPTER 2

Design of a 10-bit 1-GS/s Pipelined ADC

2.1 Introduction

The figure of merit (FOM) of ADCs, defined as

$$FOM = \frac{Power}{2^{ENOB} \times min\{f_s, ERBW\}}, \tag{2.1}$$

tends to degrade as higher speeds and/or resolutions are sought. For example, the FOM rises from 6.3 fJ/conv.-step for an 8-bit, 1.1-MHz ADC [18] to about 500 fJ/conv.-step for a 12-bit 3-GHz design [7]. It is therefore desirable to develop low-power gigahertz ADCs in the resolution range of 10 to 12 bits. This trend is illustrated in Fig. 2.1, where the FOM is plotted for a number of designs, versus the sampling rate at different technology nodes. This trend shows that the definition of the FOM is indeed not a fair measure. Nonetheless, we would like to see how the FOM can be improved in the gigahertz ranges.

This chapter presents the design and implementation of a pipelined ADC that employs a precharged resistor-ladder digital-to-analog converter (RDAC) and a multi-bit front end with a low-gain op amp. Avoiding the need for op amp nonlinearity calibration, the ADC only computes the gain errors at high speeds and corrects them in the digital domain.

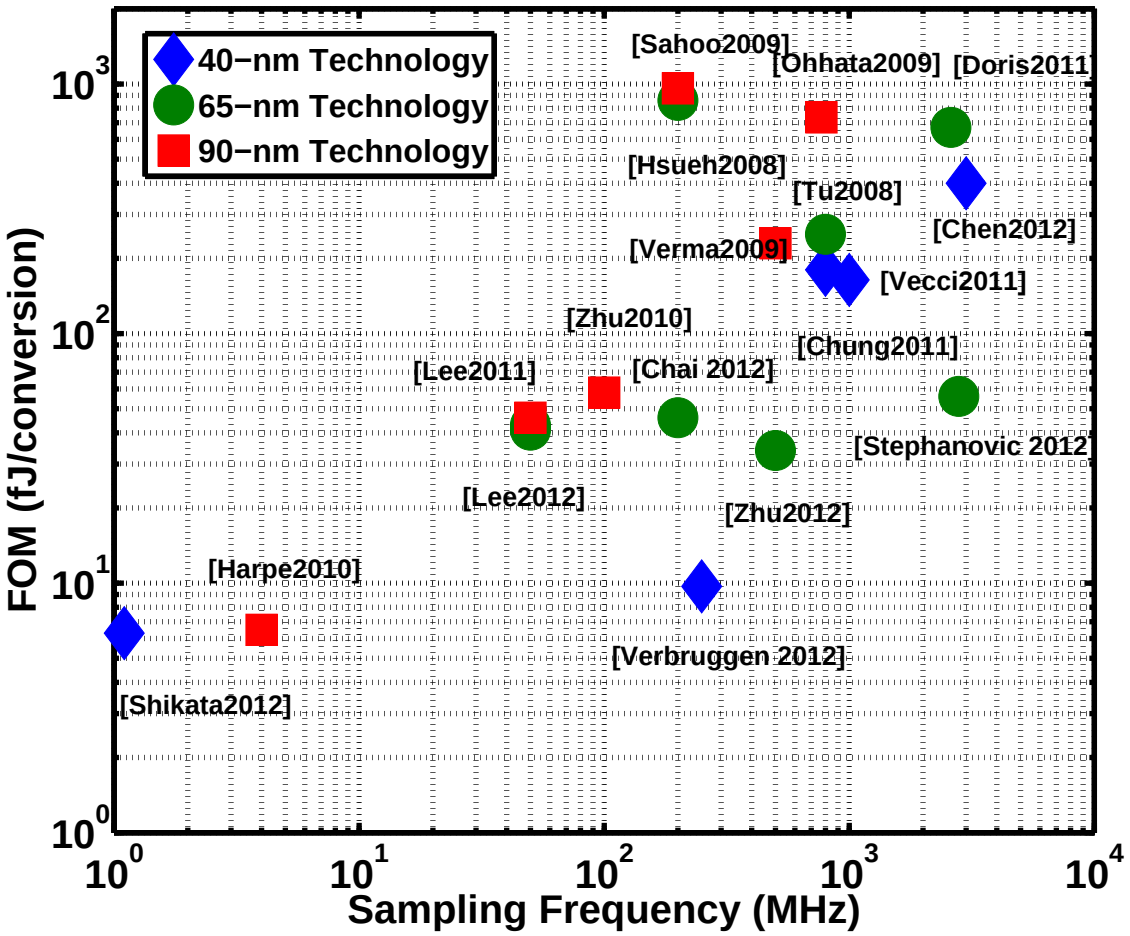


Figure 2.1: Reported FOM of the state-of-the-art designs versus their sampling rates [2–19].

2.2 Pipelined Architecture

Fig. 2.2 shows a block diagram of a pipelined ADC composed of N stages that work on successive input samples. This architecture achieves high conversion rate at the expense of latency [24,27]. Each stage consists of a sub-ADC, a digital-to-analog converter (DAC), a subtractor, and a gain stage. The sub-ADC digitizes

the input signal and drives the DAC to generate the analog equivalent of the input signal. The difference between the input signal and its analog equivalent (residue voltage) is then amplified by a gain of A_{res} to relax the design requirements of the subsequent stages. Therefore, by downscaling the device sizes along the pipe, significant power saving can be obtained. In addition, employing redundancy reduces the design requirement of the sub-ADC comparators. However, pipelined ADCs require high-precision DACs and interstage amplifiers with high bandwidths and gains.

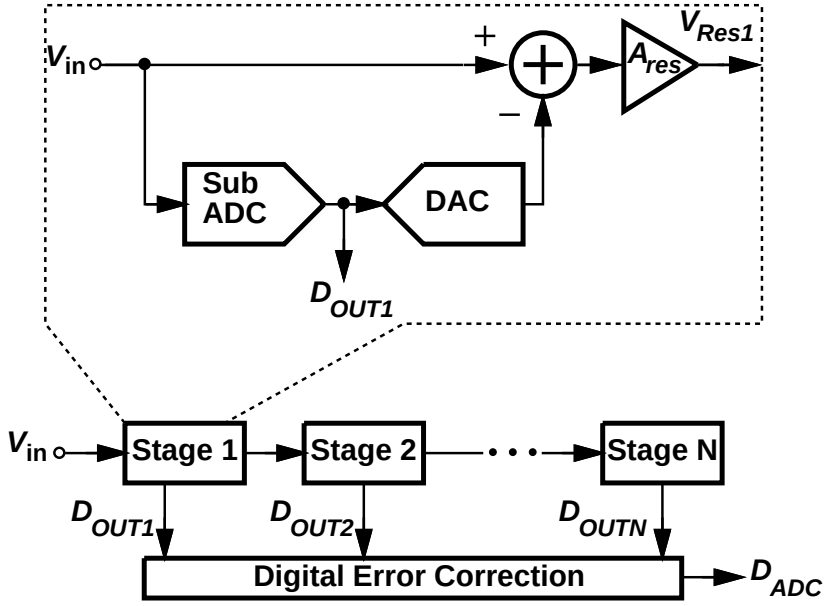


Figure 2.2: Block diagram of a pipelined architecture.

2.3 Multi-Bit Front End

The power consumption and performance of a pipelined ADC are primarily determined by the op amps used in its first few stages that require the largest accuracy. Due to the gain of front-end stages, the accuracy requirements of the

subsequents stages reduce exponentially leading to a lower power dissipation in the back end. Among the imperfections afflicting the op amps, the finite gain and the nonlinearity have been the targets of numerous calibration techniques. However, the nonlinearity poses difficult challenges: foreground calibration may not adequately hold as the temperature varies, and background calibration restricts the input signal bandwidth or dynamic range, does not correct for capacitor mismatch, or requires a slow but accurate auxiliary ADC [28–30]. These issues are summarized in [6].

It is desirable to architect the ADC such that the stages *inherently* avoid nonlinearity. To this end, the ADC can resolve several bits in the front end, thus allowing the first multiplying DAC (MDAC) to operate with small output swings, if an appropriate amplification gain is chosen. However, a large resolution of first stage requires a high-resolution flash [1] as the sub-ADC that complicates its design. Moreover, a low MDAC gain increases the power consumption of the back-end ADC as the signal range of the back end is reduced. Therefore, optimized choices of first stage resolution and first stage gain are needed.

The subtractor and the gain stage are conventionally implemented as a single switched-capacitor (SC) circuit, as conceptually shown in Fig. 2.3. Operating in two phases, through a bootstrapped switch [31], the circuit samples the input signal over a sampling capacitor,C_S, in one phase while the feedback capacitor, C_F, is reset. Then in the second phase, C_S samples the corresponding reference voltage determined by the sub-ADC, and the op amp, in a capacitive feedback configuration, amplifies the difference between the sampled input and sampled reference. Depending on the resolution of the sub-ADC, stage configuration (flip-around versus non flip-around), and type of the DAC, an array of

[1]Flash architecture is the conventional way of implementing the sub-ADC due to its speed and power efficiency at low resolutions.

properly switched capacitors act as C_S and/or C_F. For example, a capacitive DAC in a non-flip-around arrangement , as shown in Fig. 2.4, can be employed. Such a DAC has a zero static power and thus is attractive in a low-power design. However, since the total input capacitance is determined by kT/C noise, after decomposition to 2^M units in an M-bit stage, the capacitor matching is poor. It should be noted that, these unit capacitors can be several hundreds micrometer apart in the layout and it is hard to guarantee enough matching for a 10-bit design. Therefore, such a DAC requires a complex calibration algorithm and is not suitable for high resolutions.

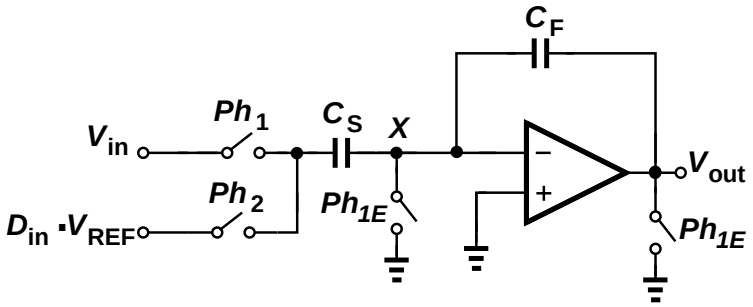


Figure 2.3: Switched-capacitor implementation of the MDAC.

Another DAC choice is the resistor-ladder DAC, as depicted in Fig. 2.5. It has been shown in [6] that by proper layout design, such a DAC can achieve linearities of better than 11 bits. However, there are two main issues: limited speed and static power. The ladder must drive the top plate of the sampling capacitor, C_S, as well as all the parasitic capacitance of the switches at node X. Therefore, the settling performance of the DAC at its output node X is limited. In addition, the ladder draws static current, which is not desired in a low-power design.

It can be shown that a multi-bit front-end sub-ADC along with a proper residue gain stage greatly reduces the power consumption of a high-speed pipelined

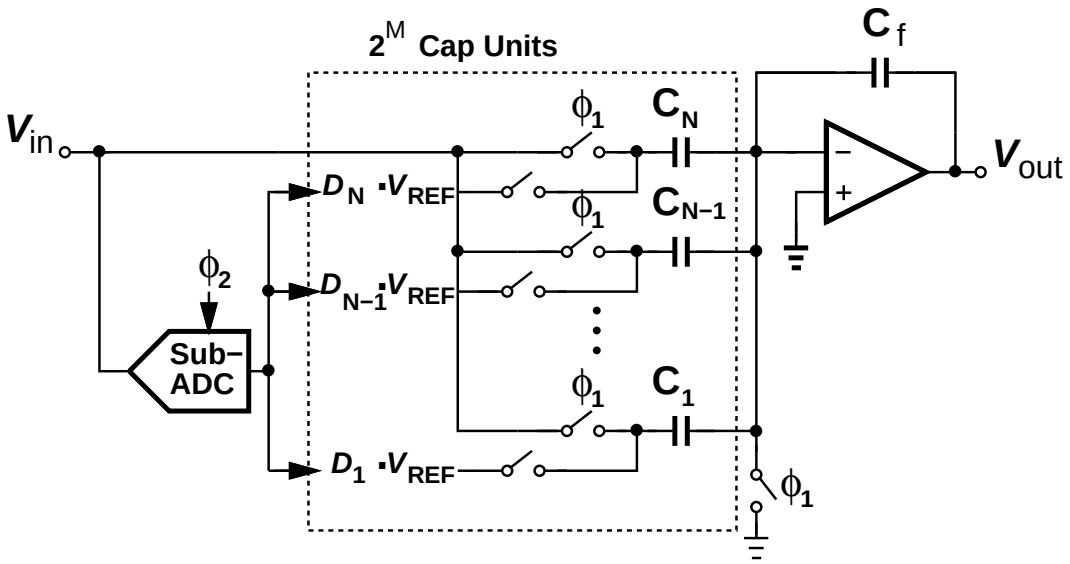


Figure 2.4: A capacitive DAC in the non-flip-around configuration.

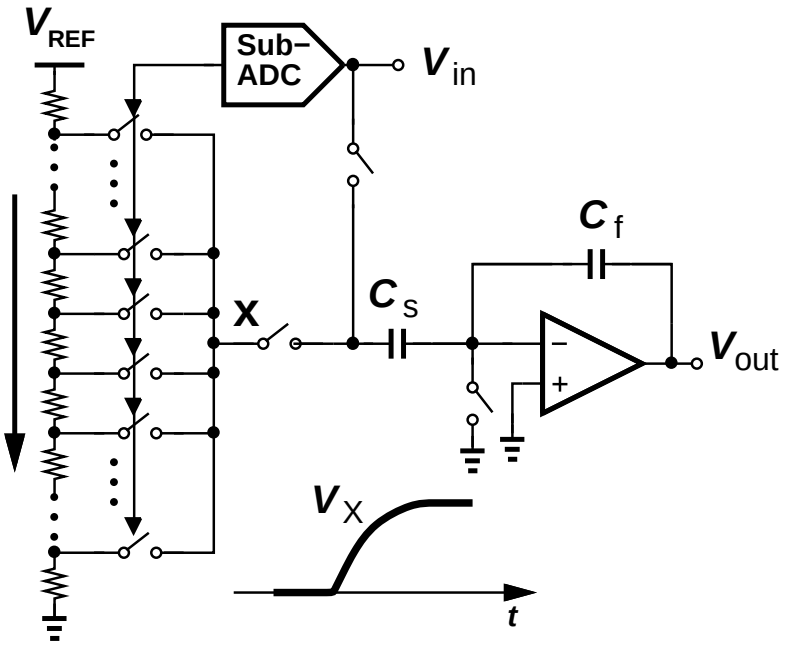


Figure 2.5: A resistor-ladder DAC in the non-flip-around configuration.

ADC. In the rest of this section, we discuss this matter in detail.

2.3.1 Front-End Gain

The subranged signal swing at the output of the first stage, V_{swing1}, can be expressed as

$$V_{swing1} = A_{res}. \frac{V_{REF}}{2^M}, \tag{2.2}$$

where V_{REF} denotes the ADC signal range, M is the number of bits resolved in front end, and A_{res} represents the closed-loop gain of the first MDAC, which can be obtained from

$$A_{res} = \frac{\frac{C_S}{C_F}}{1 + \frac{1}{A}(\frac{C_S}{C_F})}. \tag{2.3}$$

A in Eq. 2.3 is the op amp open-loop gain. The worst-case settling performance of the op amp, on the other hand, is given by

$$V_{err-sett} = \frac{V_{swing1}}{2} . e^{-\frac{T \beta g_m}{C_L}}. \tag{2.4}$$

Here, T is the allowed settling time, β is the feedback factor ($\beta \approx C_F/(C_F + C_S)$), g_m is the op amp transconductance, and C_L is the total load capacitance. For an N-bit ADC, to keep the settling error less than half of the LSB, the available settling time, T must be longer than

$$T_{min} = (N - M) . ln(2) \times \frac{C_L}{\beta g_m}. \tag{2.5}$$

Eq. 2.5 and 2.3 suggest that larger gain values ,A_{res}, reduces the feedback factor and hence worsens the speed. However, the load capacitance, C_L also decreases. To account for this effect, we can assume that the total capacitance required by the thermal-noise limited design is $C_{L,tot}$, while the load capacitance, C_L is $C_{L,tot}/A_{res}^2$. Thus, we can rewrite Eq. 2.5 as

$$T_{min} = (N - M) . ln(2) \times \frac{1}{\beta g_m} \frac{C_L}{A_{res}^2}. \tag{2.6}$$

Therefore, it is beneficial to choose a large closed-loop gain. However, limited by the maximum attainable open-loop gain, A, and op amp linearity (Eq. 2.2), we choose a closed-loop gain of 2 in our design.

2.3.2 Front-End Resolution

Eq. 2.2 and Eq. 2.6 show that a larger resolution of first stage is advantageous for the ADC linearity and speed. Thus, it is desirable to increase the resolution of the sub-ADC. However, practical limitations arising from comparator offset, ADC input capacitance, and power consumption restrict the attainable resolution. Now, we discuss these limitations in detail.

A prudent choice of a high-speed low-to-medium-resolution sub-ADC architecture is flash. A major drawback of such an architecture is that, the power consumption and the circuit complexity increases exponentially by resolution. Therefore, an optimum resolution must be chosen to fully exploit the advantages of a multi-bit front end.

Comparator offset and noise are the main sources of error in a flash ADC. Redundancy, can be employed to relax the required comparator specifications. The cost, however, is increased range and resolution of the back-end ADC. Another issue is the kick-back noise associated with the latch operation of a comparator to the input and reference voltages that can cause erroneous decisions of that comparator and its neighbors resulting in systematic offset and nonlinearity. In our design, a resolution of 4 bits is chosen for the first stage.

2.3.3 Input Sampling Accuracy

Another advantage of a multi-bit front end is suppressing the memory effect of the sampled input voltage. Recalling from Fig. 2.3, the input signal is sampled over C_S during phase Ph_1 while during the previous hold phase, Ph_2, the DAC reference voltage corresponding to the previous input sample was stored over C_S. Therefore, after a sampling time of T, the voltage stored on the sampling capacitor is

$$V_{in,Sampled} = V_{in}\,(1 - e^{\frac{-T}{\tau}}) + V_{DAC,prev.}\,.\,e^{\frac{-T}{\tau}}, \tag{2.7}$$

where V_{in} is the current input signal, τ is the sampling time constant, and $V_{DAC,prev.}$ is the quantized voltage representing the previous input sample. Thus, we can rewrite Eq. 2.7 as following

$$V_{in,Sampled} = V_{in}\,(1 - e^{\frac{-T}{\tau}}) + V_{in,prev.}\,.\,e^{\frac{-T}{\tau}} + Q_{n,prev.}\,.\,e^{\frac{-T}{\tau}}. \tag{2.8}$$

Here, $V_{in,prev.}$ denotes the prior sampled input voltage and $Q_{n,prev.}$ is the quantization noise associated with the previous sample. It is evident that higher front end resolutions reduce the noise, $Q_{n,prev.}$, thus improving the memory effect.

2.3.4 MDAC and Sub-ADC Timing Mismatches

In a pipelined architecture, an active front-end sample-and-hold (S/H) is usually avoided because it consumes significant power and adds noise and nonlinearity. However,without a S/H, the ADC may suffer from timing mismatches between the sampling paths of the MDAC and those of the sub-ADC. Distinctions among the sampling time constants and clock skew are the main sources of such timing errors. Assuming a sinusoidal input with amplitude V_{amp} and frequency f_{in} is applied to the ADC as

$$V_{in} = V_{amp}\,sin(2\pi f_{in} t), \tag{2.9}$$

then the voltages sampled by the MDAC and sub-ADC are

$$V_{S,MDAC} = V_{amp}\, sin(2\pi f_{in}(t_1 - \tau_1)), \tag{2.10}$$

$$V_{S,SADC} = V_{amp}\, sin(2\pi f_{in}(t_2 - \tau_2)). \tag{2.11}$$

Here, t_1 and t_2 are the sampling instants, while τ_1 and τ_2 are the sampling time constants of the MDAC and the sub-ADC, respectively. Defining a timing error as

$$\Delta t = (t_1 - t_2) - (\tau_1 - \tau_2), \tag{2.12}$$

it can be shown that the maximum voltage error is given by

$$\begin{aligned} \Delta V_{max} &= max(V_{S,MDAC} - V_{S,SADC}) \\ &= 2V_{amp}\pi f_{in}\Delta t. \end{aligned} \tag{2.13}$$

Eq. 2.13 shows that the resulting error is inversely proportional to the input frequency. On the other hand, in a multi-bit front end, the tolerable decision error decreases exponentially by the stage resolution. Hence, it is of significant importance to minimize the timing mismatches, when designing a high-speed multi-bit front end.

Timing calibration algorithms can remedy these sampling errors, but they usually are effective only for certain input frequencies. Another alternative is increasing the tolerable error range by calibrating the sub-ADC comparator offsets.

2.3.5 ADC Linearity

As a result of a multi-bit front end, the ADC input range is no longer limited by the op amp nonlinearity, but could be limited by the input sampling accuracy and/or DAC linearity. Bootstrapped sampling switches provide enough linearities for medium-to-high resolutions. However, the linearity of the DAC poses a

significant challenge, requiring precise components that leads to a high power consumption, or demanding calibration methods to correct for DAC non-idealities.

In a conventional pipelined stage, a capacitive DAC (CDAC) is an efficient choice in terms of power and speed. To ensure enough linearity, calibration algorithms are employed that compute and correct for capacitor mismatches. However,if the multi-bit DAC in the first stage incorporates capacitors, then the mismatches between *each* of these capacitors and the MDAC feedback capacitor must be computed and corrected. Hence, a complex calibration method with a long convergence time is mandatory. In addition, the number of unit capacitors increases exponentially by the stage resolution resulting in larger ADC input capacitance due to the practical limitations on the size of unit capacitor.

We may instead consider a resistor-ladder DAC (RDAC), given that such DACs can achieve linearities exceeding 11 bits ([6]). However, it is generally believed that resistor-ladder DACs are slow, a true statement for stand-alone designs. Nonetheless, our key observation here is that, in a pipelined ADC environment, the DAC output node can be *precharged* to the analog input level, thereby considerably relaxing the settling performance. In addition, since we require a resistor ladder for the multi-bit sub-ADC, we can utilize the same ladder for the RDAC too. Therefore, the power penalty is negligible. In the next Section, we discuss these matters in detail.

2.4 Proposed ADC Architecture

Fig.2.6 depicts a block diagram of the proposed ADC. It consists of nine stages followed by a single comparator at the end. The first stage resolves four bits while the other stages resolve 1.5 bits each. Since our low-voltage architecture does not

require op amp nonlinearity correction, we only apply gain error calibration to all the stages. To simplify and reduce the calibration complexity, we decided to break the tradition and use a highly-linear resistor-ladder DAC in the first stage. But, we must deal with its limited speed and its power consumption.

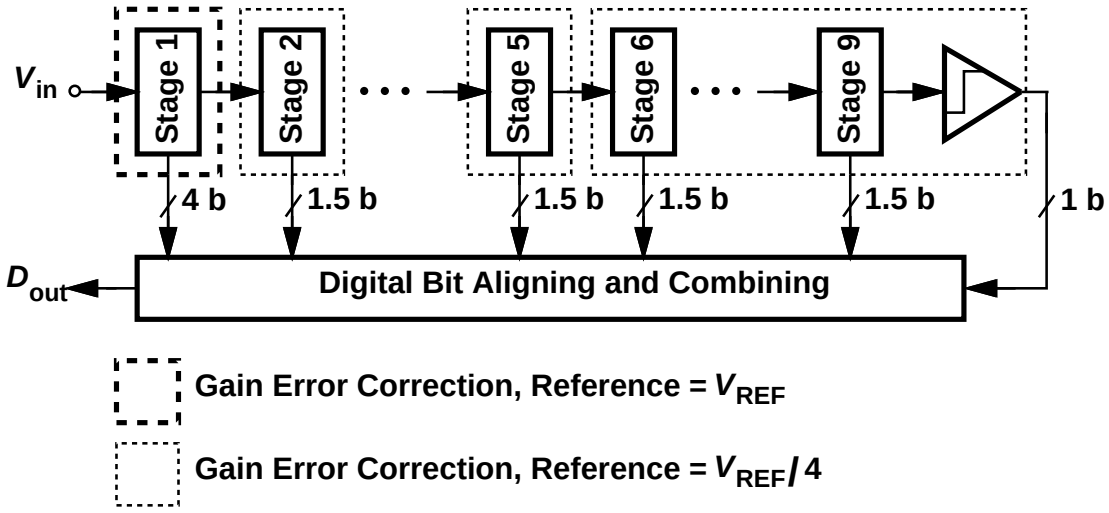


Figure 2.6: Block diagram of the proposed ADC architecture.

To overcome the limited speed of the RDAC, we propose a precharged architecture. Fig. 2.7(a) shows the first stage of the ADC architecture followed by the back end. A 4-bit sub-ADC in the first stage along with an MDAC gain of 2 greatly simplifies the design of the op amp. Moreover, a precharged resistor-ladder DAC rapidly establishes the analog equivalent of the sub-ADC output at node X. One bit of redundancy accommodates various errors, including the offsets of the comparators in the sub-ADC and the timing mismatches between the sub-ADC and the MDAC.

The operation of the front end and the timing budgets thereof are explained with the aid of the waveforms shown in Fig. 2.7(b). For 25% of the clock period (250 ps), bootstrapped switches sample the analog signal on the RDAC

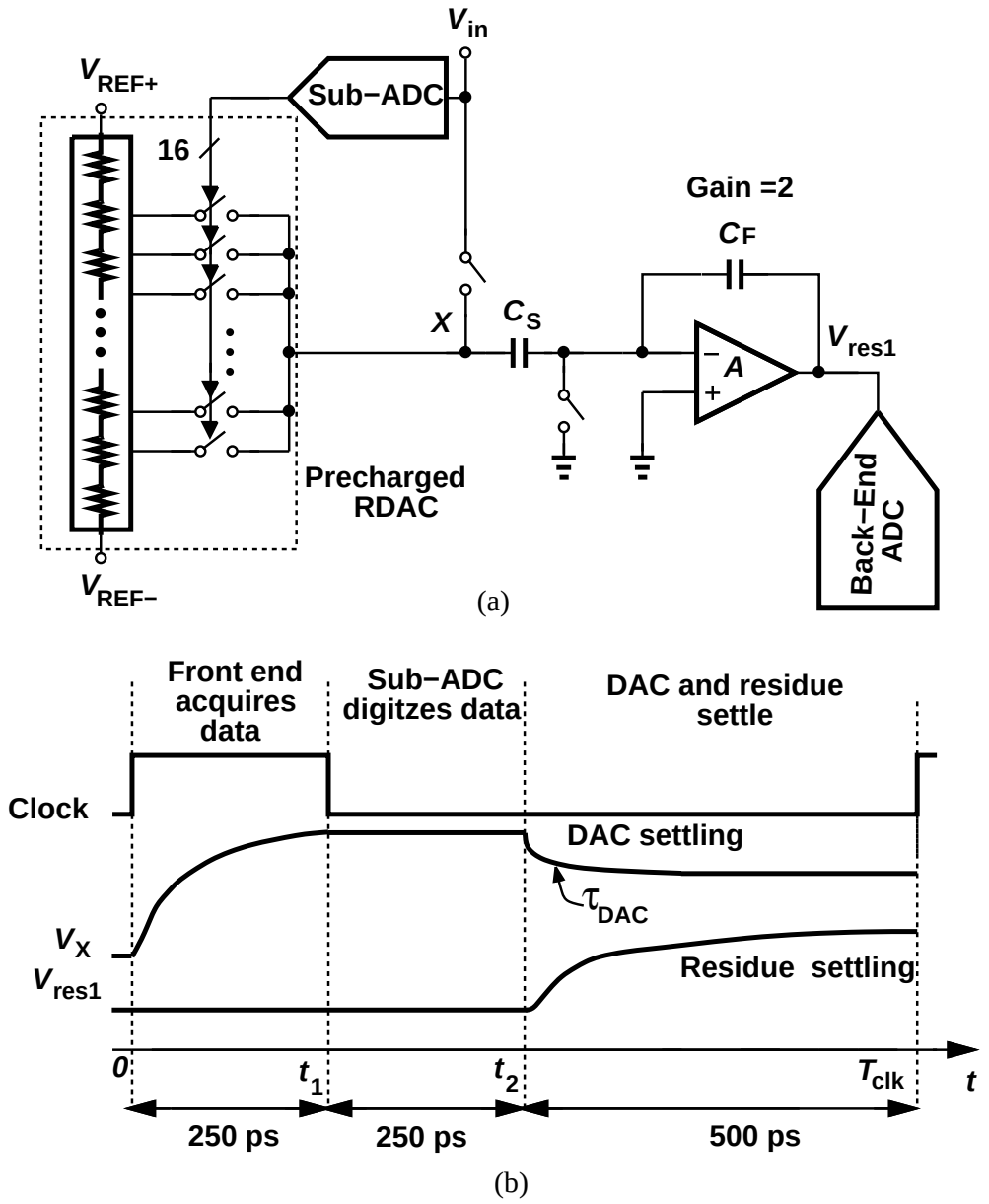


Figure 2.7: (a)Front-end stage employs a precharged RDAC and a gain of 2 to improve linearity and speed and (b) conceptual DAC and residue waveforms.

output [node X in Fig. 2.7(a)], the input capacitor of the MDAC, and the input capacitors of the sub-ADC comparators. Next, the sub-ADC is clocked while V_X is held, The coarse digital estimate arrives after 250 ps, turning on one switch in

the RDAC and driving V_X to the corresponding value. A non-flip-around gain stage amplifies the residue by a gain of two and feeding the back-end ADC. The last 500 ps of the clock period is allocated to the settling of V_X and the MDAC output, V_{res1}.

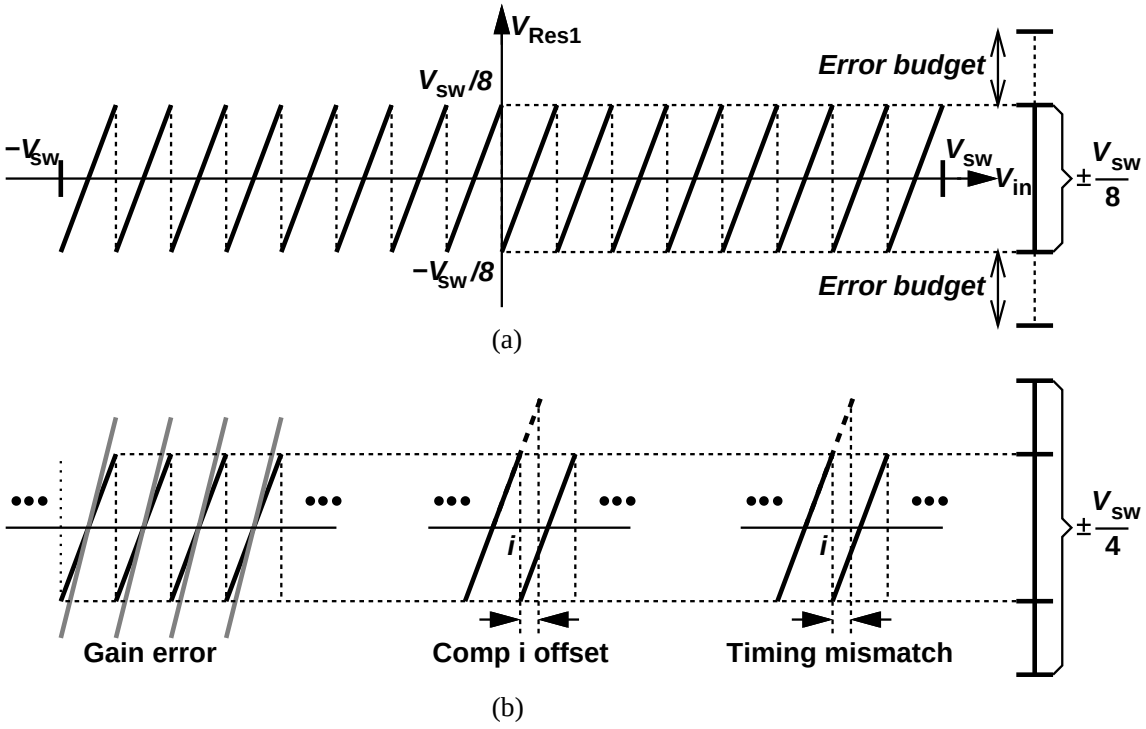


Figure 2.8: (a)Ideal characteristic of V_{res1}, (b)characteristic of V_{res1} with the presence of errors, and (c) impact of the reference error.

With ideal components, V_{res1} has a swing of $1/8th$ of the input signal range, $V_{sw,in}$, as depicted in Fig. 2.8(a). However, due to the stage gain error, ΔG_1, offsets of sub-ADC comparators, $V_{OS,i}$, and timing mismatches between sampling paths of sub-ADC and those of MDAC, err_{samp}, the range of $V_{sw,in}$ could be wider. These effects are illustrated in Fig. 2.8(b).

Gain error arises from capacitor mismatch [2] and op amp low gain and is

[2]Mismatch between sampling and feedback capacitors of the gain stage.

corrected for by calibration. Redundancy corrects comparator offset and timing mismatches in digital domain. Assuming 1-bit overlap leads to a swing of $1/4th$ of input signal swing at the output of first stage and accommodates a budget of $1/8th \times V_{sw,in}$ for error.

2.5 Building Blocks

2.5.1 Precharged RDAC

To save power, the front end employs a single high-speed resistor ladder to provide three sets of quantities:
(1) reference taps for the first sub-ADC,
(2) first stage RDAC voltages, and
(3) high-precision voltages for foreground calibration of the ADC.
As such, the design of the ladder and its associated circuitry plays a critical role in the overall performance. It is important to note that the fast settling of the ladder also allows performing calibration at a high sampling rate and hence correcting for incomplete settling of the MDAC.

The reference ladder, shown in Fig. 2.9, is realized as a continuous rectangular geometry made of non-silicided polysilicon, with its taps positioned on the edge to minimally disturb the current flow.

Depending on the input signal voltage, the resistance seen at the output of RDAC, i.e. node X in Fig. 2.7(a), varies. The worst-case Thevenin equivalent resistance of the ladder is $R_l/4$, where R_l is the total ladder resistance. Hence, the worst-case time constant at node X is (see Fig. 2.10)

$$\tau_{X,max} = (\frac{R_l}{4} + R_{sw}) \times [C_w + C_S \parallel (C_p + (1 + A).C_F)]. \tag{2.14}$$

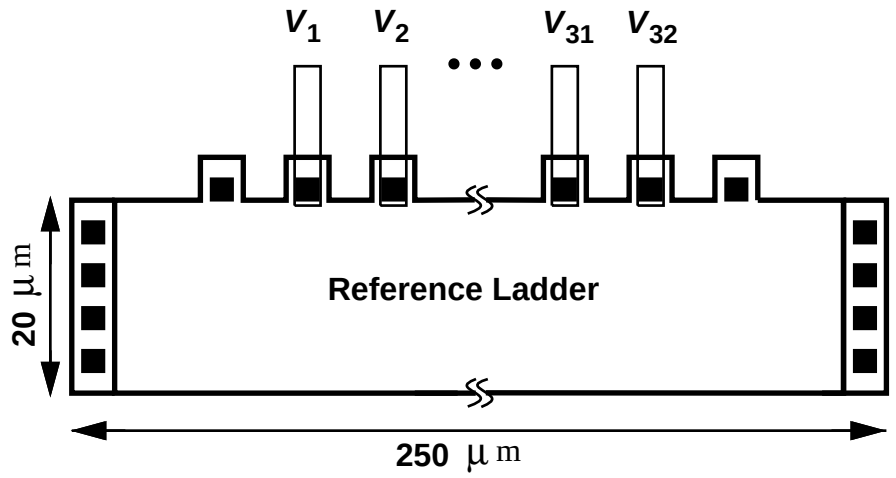


Figure 2.9: Structure of the precise reference ladder.

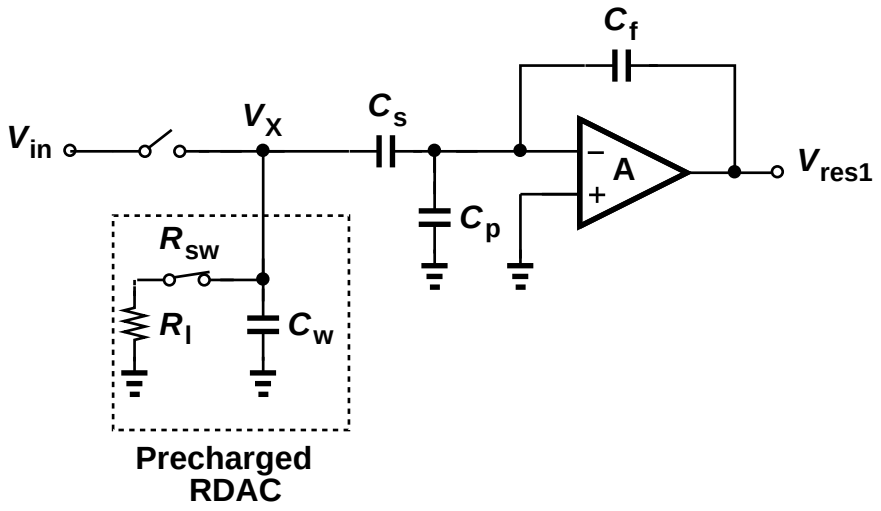


Figure 2.10: Calculating worst-case RDAC time constant.

Here, R_{sw} denotes switch resistance, while C_w and C_p represent parasitics at node X and at the op amp virtual ground, respectively. To enhance the speed, low ladder and switch resistances are desirable. However, the former leads to a high static power consumption of the ladder and the latter requires wide switch devices resulting in a large parasitic capacitor at node X, i.e. C_w, which degrades

RDAC settling.

In this design, a 150-Ω resistor ladder [3] along with a 300-fF sampling capacitor, exhibits a worst-case RDAC time constant value of 26 ps. In addition, having the RDAC output precharged to the analog voltage, only $4.2 \times \tau_{DAC}$ is sufficient for the RDAC output to settle to its final value within $LSB/2$.

Although calibration methods can be employed to correct for reference inaccuracies due to the resistor mismatches, this design relies on high linearities of the resistor ladders, as previously demonstrated in literature ([6]). However, if higher linearities and/or resolutions are sought, the reference inaccuracies must be corrected.

2.5.2 Sub-ADC

The best candidate for a high-speed low-resolution sub-ADC is flash architecture, which consists of 2^N comparators to resolve N bits. The main sources of error include: comparator offset, comparator noise, timing mismatches between sampling paths of MDAC and Those of sub-ADC. Compared with a conventional 1.5-bit/stage pipelined stage, since the sub-ADC is engaged in a multi-bit stage, the tolerable error is considerably reduced. Hence, design of the sub-ADC has a significant impact on the ADC overall performance.

Detailed information about analyzing and simulating offset and noise of a comparator can be found in [32–34]. To minimize the timing mismatches between the sampling paths of the MDAC and those of the sub-ADC, a sampling network is used in front of each comparator of the sub-ADC that is matched with the sampling network of the MDAC. As illustrated in Fig. 2.11, the sampling network

[3] The resistance of the ladder is also governed by the sub-ADC kick-back noise that disturbs the ladder. In next subsection, we discuss it in detail.

acts as a subtractor: first in Ph_1 it samples and stores the input signal over a sampling capacitor, C_S and then in Ph_2 samples the reference voltage. Hence, as a result of charge conservation, the difference between the sampled analog voltage and the reference voltage appears at the input of the comparator. The comparator then detects the sign of its input.

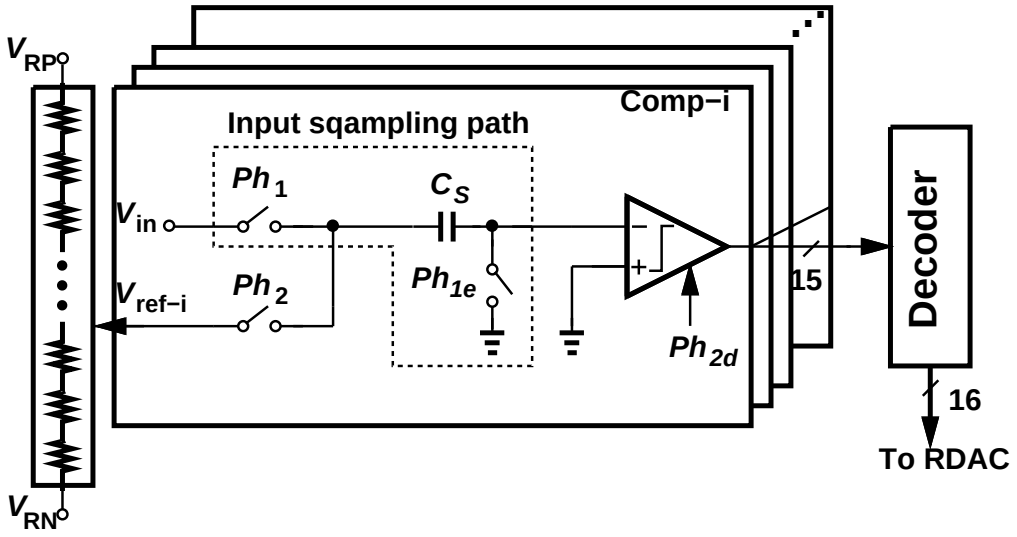


Figure 2.11: The 4-bit sub-ADC with its sampling paths matched to the sampling paths of the MDAC.

The presence of the sampling network, however, limits the signal swing to $\pm V_{DD}/2$. It is to ensure that the residue voltage produced at the input of the comparators do not fall below V_{SS} or above V_{DD}. This effect is illustrated in Fig. 2.13 where a sub-ADC comparator together with its sampling network is shown. Assume $V_{in+} = 0$ while $V_{ref+} = V_{DD}$. Also, suppose the common-mode (CM) voltage is $\frac{V_{DD}}{2}$. Then, when node P jumps from 0 to V_{DD}, node Q must jump from $\frac{V_{DD}}{2}$ to $3\frac{V_{DD}}{2}$ that can turn on the diode junctions of the CM-sampling switches and causes reliability issues. That means, the signal swing is limited to $\pm\frac{V_{DD}}{2}$.

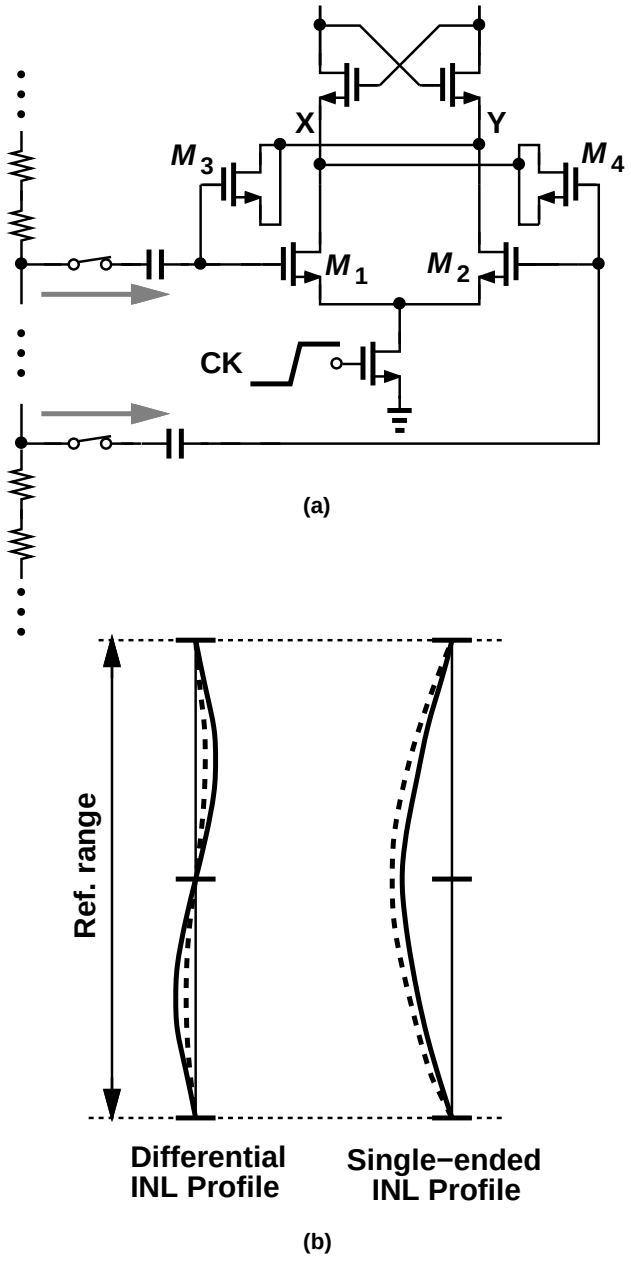


Figure 2.12: (a) Effect of sub-ADC kickback noise on the reference ladder, and (b) single-ended and differential INL profile of the ladder without (solid line) and with (dashed line) transistors M_3 and M_4.

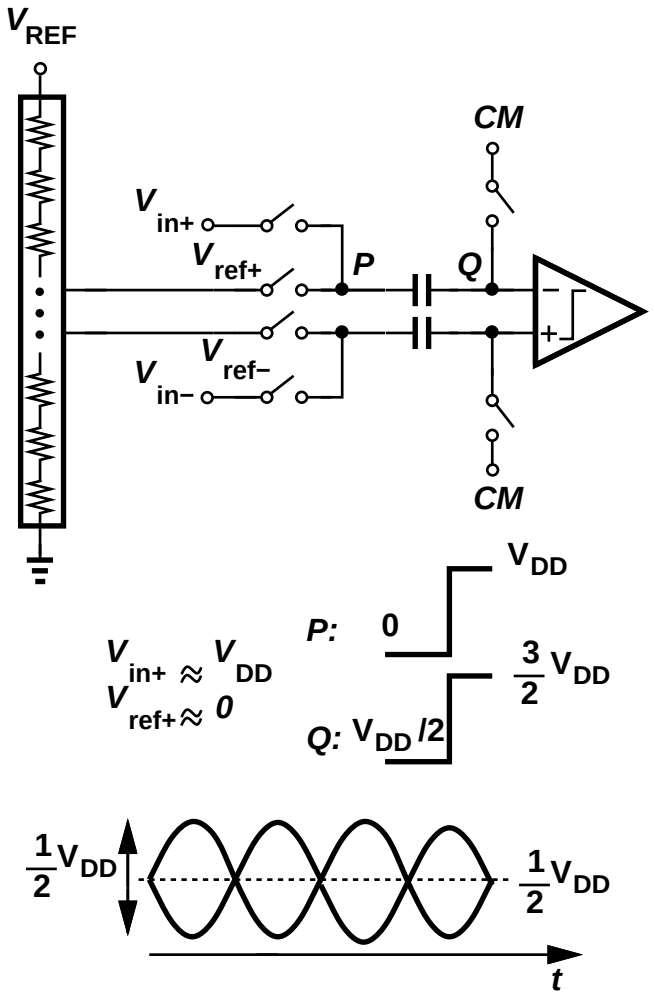


Figure 2.13: The 4-bit sub-ADC with its sampling paths matched to the sampling paths of the MDAC.

A critical issue in sharing a single ladder between the sub-ADC and the DAC is that the kickback noise of the former may substantially disturb the tap voltages utilized by the latter. It is therefore essential that the disturbance decays rapidly. This design employs a StrongArm comparator for low power consumption, but must deal with its large kickback noise. Fig. 3.9 illustrates the kickback noise mechanism. When CK goes high, V_X and V_Y are at V_{DD}, and one falls toward

ground, coupling through the gate-drain capacitance of M_1 or M_2 and drawing a current from the ladder. Since for most of the 15 comparators in the sub-ADC, the change in V_X is much larger than in V_Y (or vice versa), the kickback noise contains a high differential component.

To mitigate this effect, transistors M_3 and M_4 are added so that the large change in V_X or V_Y is coupled to both inputs. In other words, most of the differential error is converted to a common-mode error. Simulations indicate that the kickback noise due to the sub-ADC creates a peak jump of 2.5 mV on the *differential* voltages produced by the ladder and decays in about 30 ps. That is, by $t = t_2$ in Fig. 2.7(b), the ladder voltages safely settle to their static values.

The outputs of the 15 comparators (thermometer codes) are decoded to one-of-N code by using 3-input NAND gates to reduce the bubble effect [24]. The outputs of the decoder then drive the RDAC and are converted to binary codes using a low-power high-speed ROM. The ROM is shown in Fig. 2.14 and operates as following: in reset phase when $CLK = 0$, the bit lines are precharged to V_{DD}. After clock goes high, the precharging PMOS devices turn on and depending on the arrived one-of-N codes S_1 to S_{16} at the input, the appropriate bit lines are driven to zero.

2.5.3 Op Amp Design

The multi-bit operation results in a peak single-ended swing of only 75 mV at the output of the MDAC. One-bit of redundancy, however, doubles the required output range. The MDAC op amp is therefore implemented as a simple differential pair with resistor loads and an open-loop gain of 5. A tail current of about 3 mA affords fast settling in the first stage.

Any op amp offset in the first stage translates to a systematic offset for the

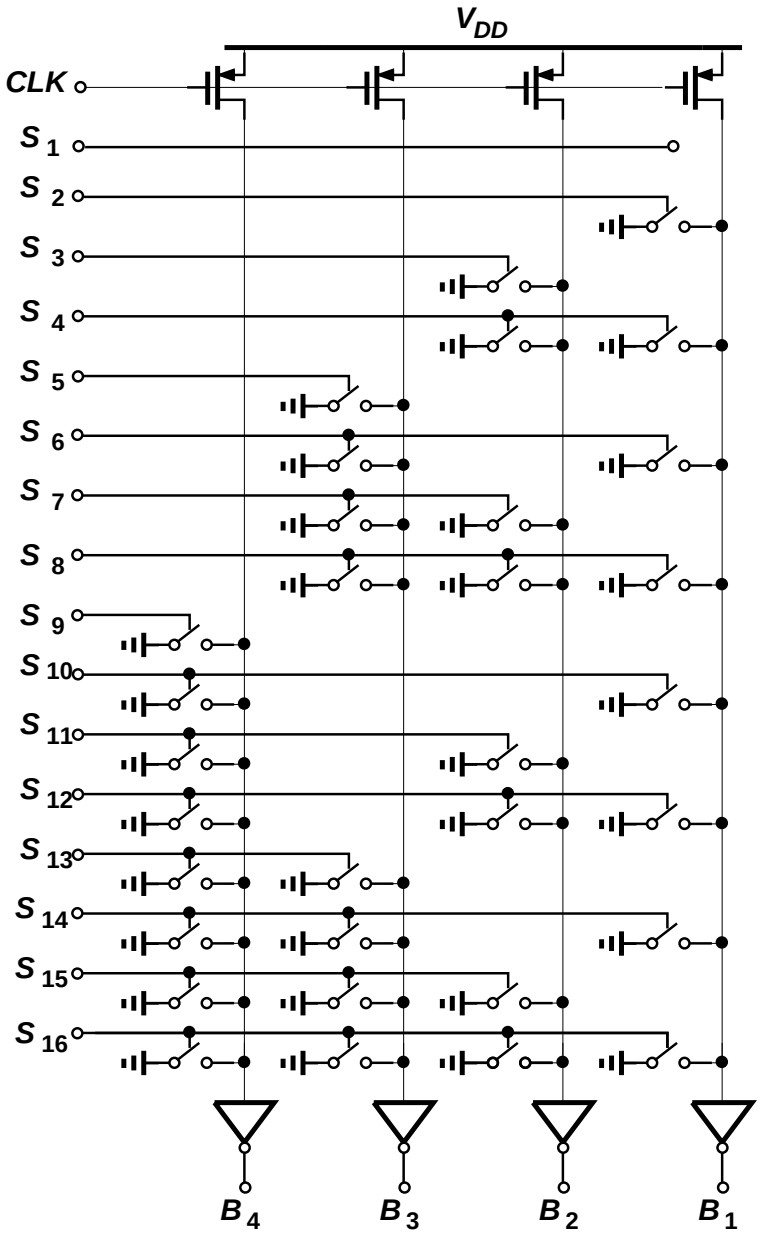


Figure 2.14: ROM implementation.

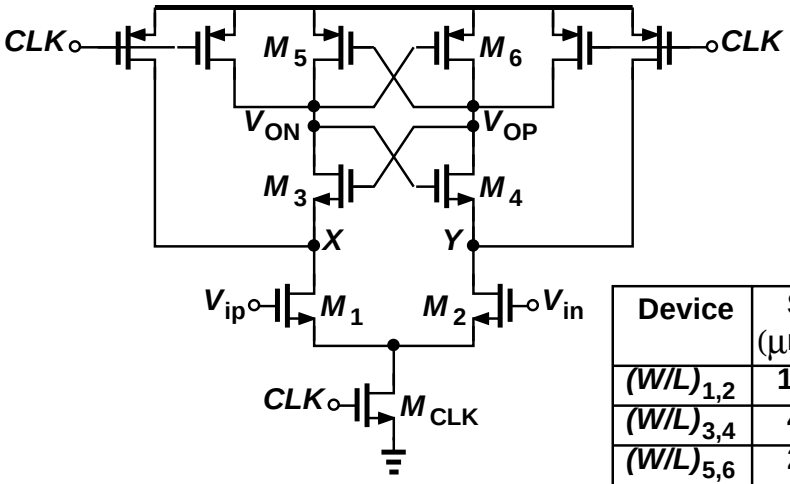
entire ADC. Hence, it does not require correction, given that the residue voltage is still within the range of the back-end ADC.

2.5.4 Comparator Design

Shown in Fig. 2.15 is the StrongArm comparator circuit used in this design, in conjunction with the device sizings, operating as following: when CLK is low, the comparator is in reset phase precharging the outputs and the drains of input transistors, i.e. V_{OP}, V_{ON}, X, and Y to V_{DD}. When CLK goes high, the tail transistor M_{CLK} turns on enabling input devices M_1 and M_2 that discharge nodes X and Y with currents corresponding to the input voltages. Transistors M_3 and M_4 turn on after a voltage drop of about V_{th} on nodes X and Y, respectively, discharging the output nodes. In the same manner, transistors M_5 and M_6 turn on after a V_{th} drop of the output nodes and together with M_3 and M_4, exponentially amplify the differential voltage V_{XY} to establish the digital output.

Noise and offset are the most crucial errors associated with the comparator, particularly in a multi-bit stage that has a limited error budget. With the sizings depicted in Fig. 2.15, and according to the simulations, the input-referred comparator noise and offset are 10 mV and 1.2 mV, respectively, occupying about 50% of the available error range (75 mV).

Another issue associated with the sub-ADC comparators, in particular in the design of high-speed multi-bit stages, is the metastability. Comparator outputs take a long time to reach valid logic levels for small input voltage differences. If the input voltage difference is too small such that the comparator outputs do not reach valid logic levels within the allocated time, the sub-ADC output becomes metastable resulting in an ADC error. In Chapter 4, a comprehensive analysis of comparator metastability effects in a pipelined environment is presented and a method is developed to precisely predict the probability of such ADC errors versus the magnitude of error.



Device	Size (μm/μm)
$(W/L)_{1,2}$	10/.06
$(W/L)_{3,4}$	4/.06
$(W/L)_{5,6}$	2/.06
$(W/L)_{CLK}$	2/.06

Figure 2.15: Comparator circuit and device sizings.

2.5.5 Back-End ADC

To obtain a high-speed operation, the back-end ADC has a non-flip-around 1.5-bit/stage pipelined architecture that resolves 8 bits to achieve 7-bit effective resolution. Since the signal swing at the input of the back-end ADC is less than 1/4th of input signal range, the reference voltages of the back-end ADC are 1/4th of ADC reference voltages. Although reference ladder of the first stage can provide such voltages, a secondary low-power ladder has been used for the back-end ADC to do more experiments by changing the reference range of the back-end ADC. It should be noted that the sub-ADC comparators of the back-end ADC do not introduce any kickback noise on the ladder as they make their decisions right after falling edge of their sampling phase. Moreover, due to the capacitor down-scaling, MDACs of the back-end stages do not require any stringent RDAC settling. The secondary ladder has a total resistance of 300Ω. Any discrepancy between this ladder and front-end ladder is absorbed in gain error correction of the back-end ADC.

Depicted in Fig. 2.16(a) and (b) are the MDAC and sub-ADC circuit implementations of the back-end ADC. First, during PH_{1E}, bottom-plate sampling of the input voltage on the sampling capacitor C_s is performed, while the op amp is configured as a unity gain stage and its offset is sampled and stored on capacitor C_f. Then in PH_2, after arrival of the sub-ADC output, the appropriate reference voltage is sampled on C_s and the gain stage amplifies the produced residue voltage. The sub-ADC consists of two comparators and operates as following: in phase $PH_{1E}$the sampling network samples the input signal on the capacitors that have been previously precharged by the comparator reference voltage. Since the input is held by the preceding stage, right after sampling phase is over, i.e at the rising edge of PH_2, the comparators are clocked feeding the decoder to generate the controlling voltages of the DAC. Then, in PH_{ref}, the sampling capacitors are again precharged to the reference voltage. Fig. 2.16(c) shows the timing diagram of the 50%-duty-cycle clock phases of the back-end ADC.

As a result of the reduced signal-swing, back-end ADC also employs a simple high-speed differential pair with resistor loads as its op amp. As in a conventional pipeline, down scaling along the pipe starts with 200 fF sampling capacitor in stage two of the ADC and and proceeds with a scaling factor of two until stage 4 without any scaling afterwards to ease the design phase. However, a continued down-scaling can result in more power saving.

2.6 High-Speed Calibration

Due to the op amp low gain and capacitor mismatches between sampling capacitors and feedback capacitors of the MDACs, a gain error correction algorithm is demanded. Therefore, a foreground calibration method similar to the one proposed in [6] is adapted. This algorithm applies precise voltages generated by the

reference ladder of the first stage to the stage under calibration and computes its gain based on the digital outputs of the following back-end stages.

The foreground calibration is performed by applying to the ADC five differential dc voltages provided by the ladder: zero, $\pm V_{REF}/32$, and $\pm 2\,V_{REF}/32$. In a manner similar to that described in [6], calibration begins in the back and proceeds towards front, as depicted in Fig. 2.17(a). While calibrating stage j, it is disconnected from its input and instead, it samples known calibration voltages produced by the RDAC. Therefore, the output of stage j with a gain of α_j is $\alpha_j \times V_{cal}$ and is digitized by subsequent stages to yield D_{BE}. Thus, by comparing D_{BE} with D_{CAL} we can adjust α_j value by using a least-mean-square (LMS) engine. It should be noted that since the calibration runs at the start-up, once the gain values are computed, they are stored in registers. However, if a large temperature change occurs, the values must be computed again.

Fig. 2.17(b) shows the correction logic. Since we have a 1.5-bit topology for the back-end stages, multiplexing can be employed where w_j in stage j indicates the inverse of residue gain of preceding stages, i.e.

$$w_j = \frac{1}{\alpha_{j-1}...\alpha_2} \quad j > 2. \tag{2.15}$$

However, we still need one multiplier to combine the 4 bits of the front end with the outputs of the back end using coefficient w_2 that equals to $\frac{1}{\alpha_1}$. Therefore, compared to the design in [6], the complexity of the calibration logic is significantly reduced.

High-speed reference ladder advantages the calibration to operate at high clock rates and hence, any incomplete settling of the op amps, if does not saturate the stage output can also be computed and corrected. Note that dynamic gain errors are calibrated even though the input in each case is constant because the MDAC outputs must start from zero and settle anew each time. This is

in particular beneficial for high-speed designs that are limited by the op amp bandwidth. Restricted by the layout parasitics, the calibration can be performed at frequencies up to 700 MHz.

2.7 Clock Generation and Distribution

Depicted in Fig. 2.18 is the block diagram of the clock generator that receives differential current-mode-logic (CML) inputs with twice the ADC clock frequency and larger than 150-mV amplitude. To generate rail-to-rail clock phases, a CML to CMOC converter composed of a two-stage amplifier is employed. The frequency of the CMOS-level differential clock signal is then divided by two to produce 0°, 90°, 180°, and 270° phases. Using these phases, non-overlapping clock generator blocks produce 25%-duty-cycle and 50%-duty-cycle non-overlapping and early clock phases required for the front end and back end stages, respectively.

2.8 Measurement Results

The prototype ADC has been fabricated in 65-nm digital CMOS technology. Shown in Fig. 2.19 is the die active area, which measures 250 μm $\times$700 μm. The ADC reference voltages are provided externally and the calibration is performed off-chip. Careful simulations including bond wire inductance reveal that V_{REF+} and V_{REF-} in Fig. 2.7(a) must have *no* bypass capacitors so that they can quickly recover from the switching action of the DAC.

The maximum differential nonlinearity (DNL) and integral nonlinearity (INL) reach 2 LSB and 6 LSB, respectively, before gain error calibration. Fig. 2.20 plots the calibrated DNL and INL for a sampling rate of 1 GHz. To demonstrate

the efficacy of calibration at high clock rates, two cases are investigated: the calibration itself is performed at 100 MHz [Fig. 2.20 (a)], or at 700 MHz [Fig. 2.20 (b)]. We observe that the maximum DNL and INL respectively fall from 1.4 LSB and −3 LSB to 0.74 LSB and 1.4 LSB when calibration is performed at 700 MHz. These results suggest that the MDAC in the first stage (and possibly second stage) exhibits incomplete settling and greatly benefits from calibration at a high clock frequency. Note that only the gain error of each stage is calibrated.

Fig. 3.13 plots the measured output spectrum for input frequencies of 1.7 MHz and 490 MHz at a sampling rate of 1 GS/s. The third-order harmonic at −63.5 dB in the former case confirms the high linearity provided by the resistor ladder. The signal-to-(noise+distortion) ratio (SNDR) is possibly limited by ringing on the reference lines.

The dynamic performance of the ADC is shown in Fig. 2.22 for a sampling rate of 1 GS/s and analog input frequencies up to 490 MHz. The SNDR varies from 57 dB to 52.7 dB. The spurious-free dynamic range (SFDR) is also measured and observed to vary from 63.5 dB to 60 dB in this frequency range.

The ADC draws 36 mW from a 1.2-V supply, of which 2.5 mW is consumed by the reference ladder, 14.4 mW by the op amps, and 18 mW by the clock tree and the pipeline alignment latches. Computed as 36 mW/(2×460 MHz×2^{ENOB}), the figure of merit is 70 fJ/conversion. A less conservative clock tree design could improve the FOM considerably.

Table 2.1 summarizes the measured performance of the ADC and Fig. 2.23 expands the FOM plot in [8] to include our work. Note that the design reported in [35] is realized in 40-nm technology and, due to time-interleaving, may suffer from a large input capacitance. Moreover, the design relies on the raw device matching of the technology and does not calibrate the gain error.

Table 2.1: Performance Summary of the Pipelined ADC

Resolution	**10 Bits**
Sampling Rate)	**1 GHz**
Input Capacitance	**0.7 pF**
Input Range	**1.2 $V_{pp-diff}$**
Power Consumption **Ref. Ladder Power** **Analog Power** **Digital Power**	**36 mW** **2.5 mW** **14.4 mW** **18 mW**
SNDR	**57 dB**
Supply Voltage	**1.2 V**
Technology	**65 nm**
FOM	**70 fJ/Conv.**
Active Area	**0.175 (mm^2)**

2.9 Conclusion

Pipelined ADCs can greatly benefit from the use of multi-bit front ends that incorporate precharged resistor-ladder DACs. With the settling speed afforded by the low-resistance ladder, the ADC can be calibrated at high sampling rates, thus correcting for the incomplete settling of the MDACs. In addition, RDACs simplify the calibration logic by reducing the required correction to only that of the gain error. Utilizing these concepts, a 10-bit 1-GS/s ADC has been demonstrated that improves the FOM by a factor of 2.6 with respect to the state of the art.

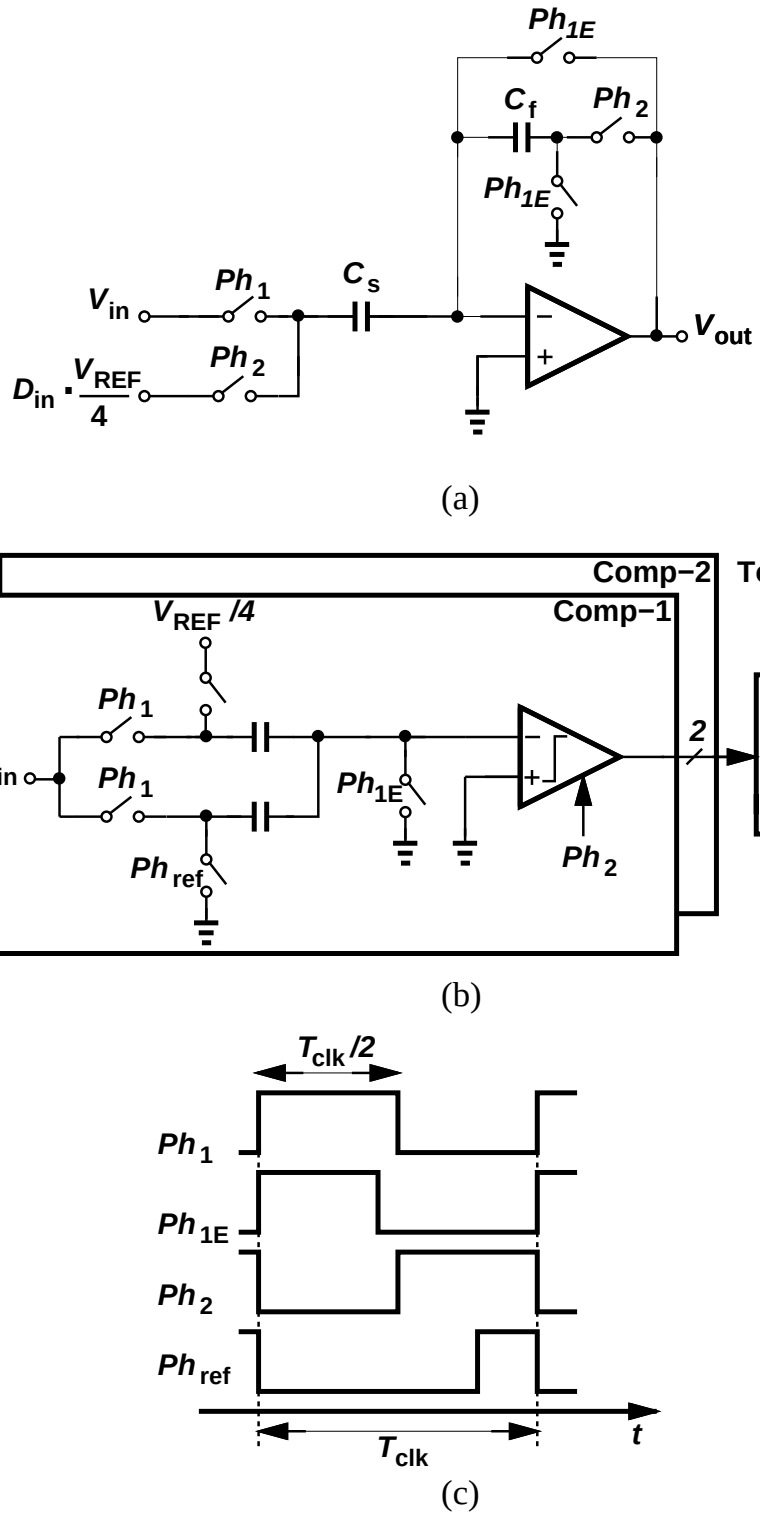


Figure 2.16: Block diagram of (a) back-end MDAC, (b) back-end sub-ADC, and (c) back-end timing waveforms.

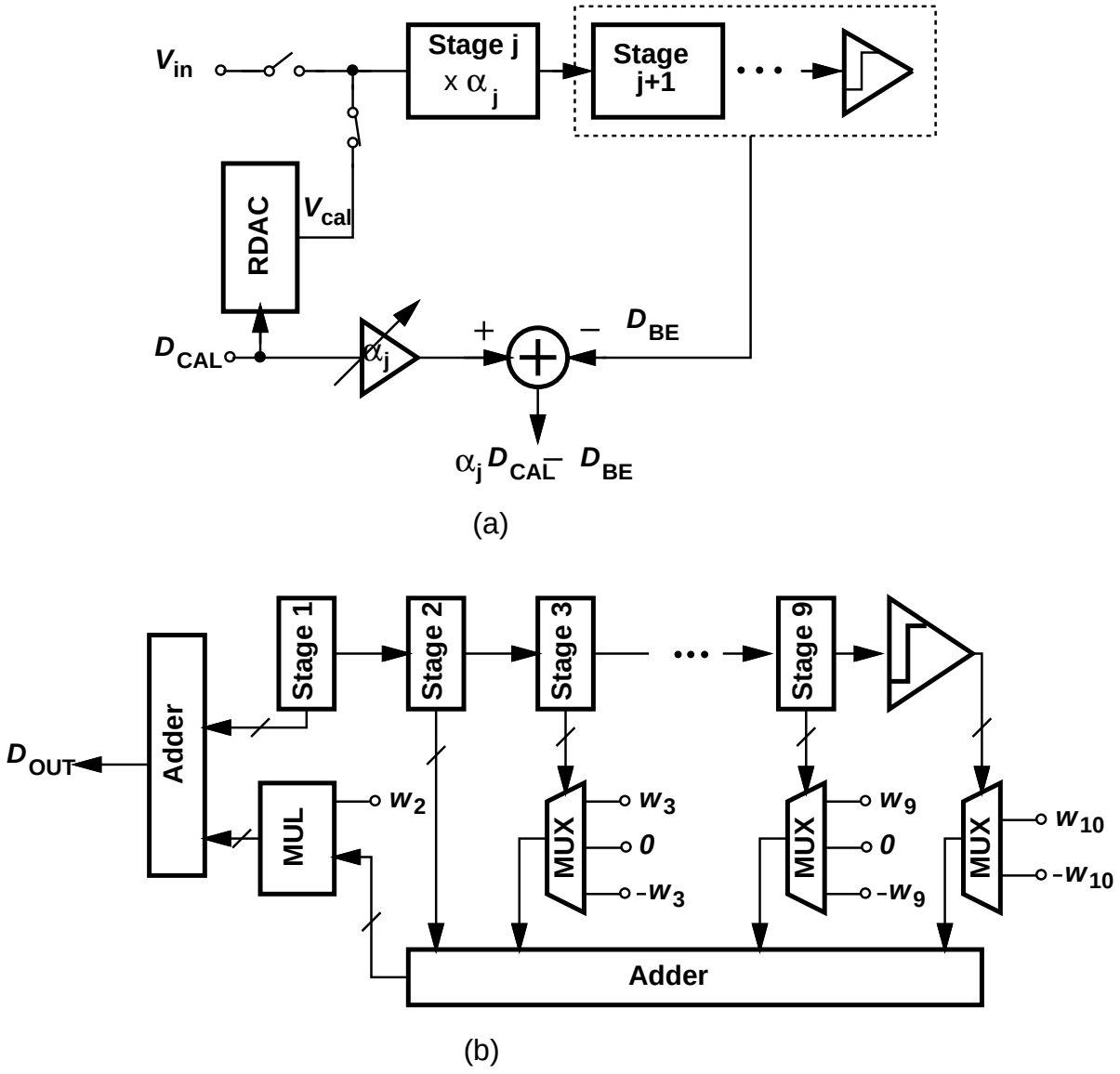


Figure 2.17: Block diagram of the gain error (a) calibration, and (b) correction in digital domain.

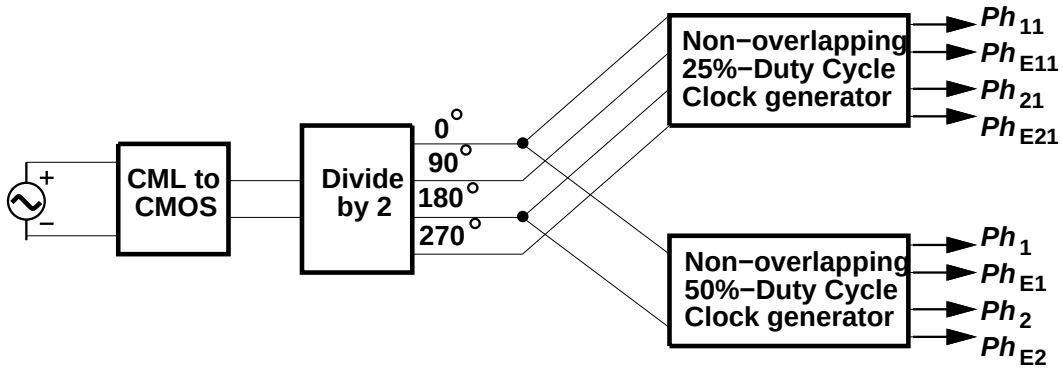


Figure 2.18: Block diagram of the clock generation and distribution.

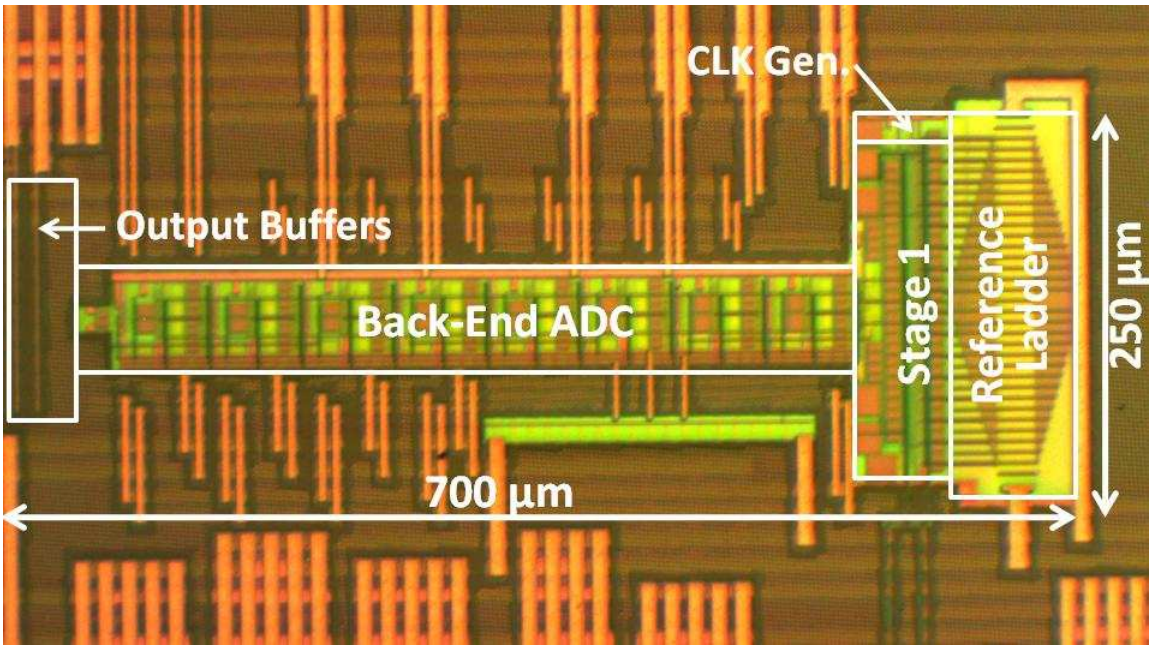


Figure 2.19: Die photograph.

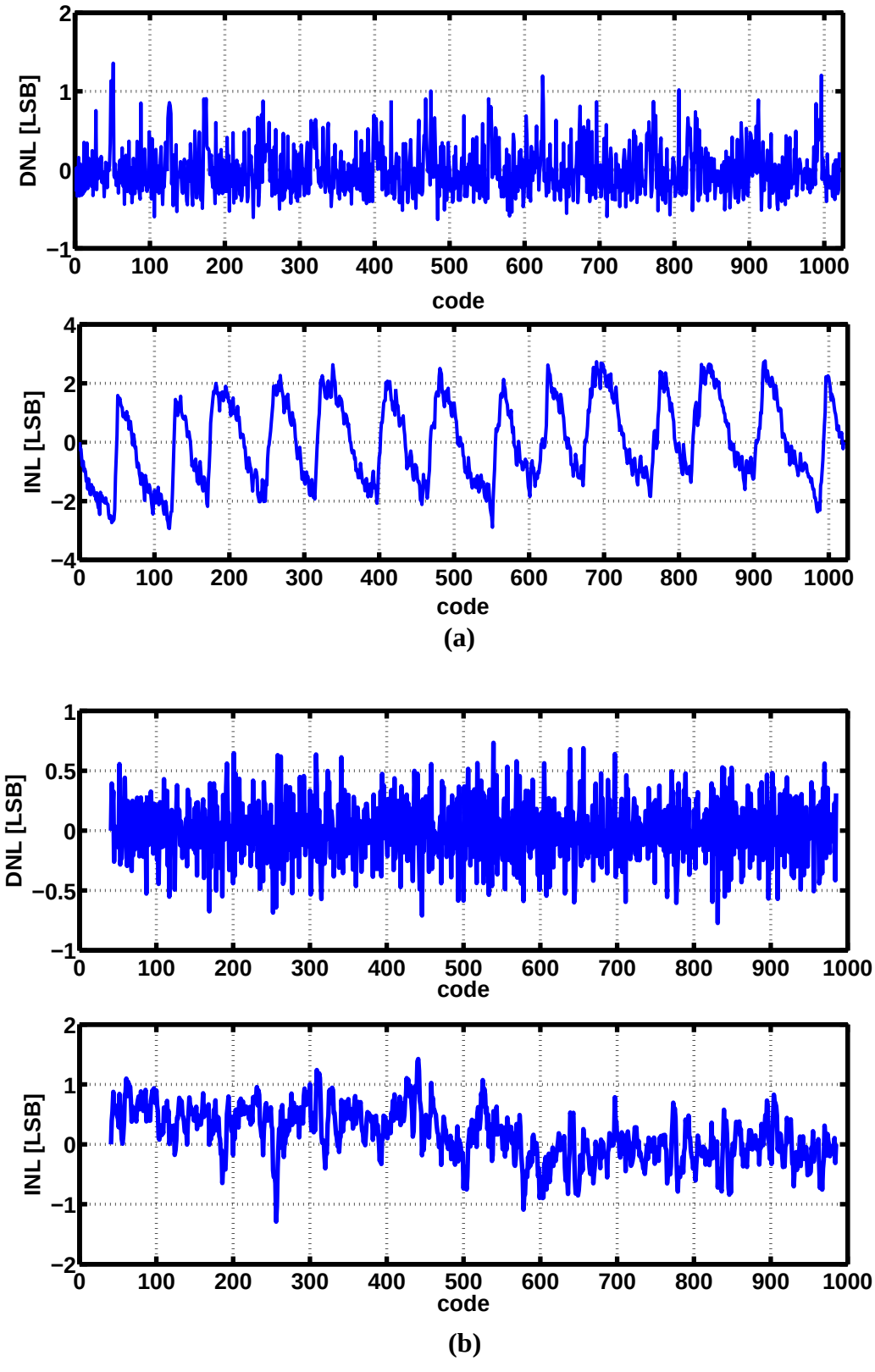
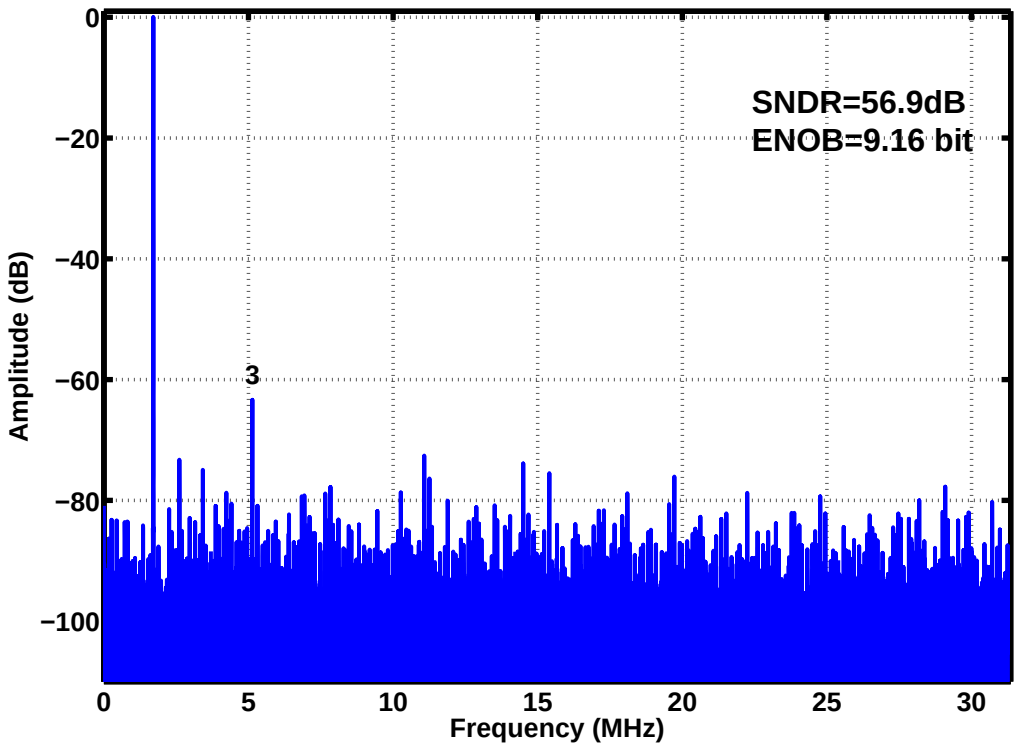
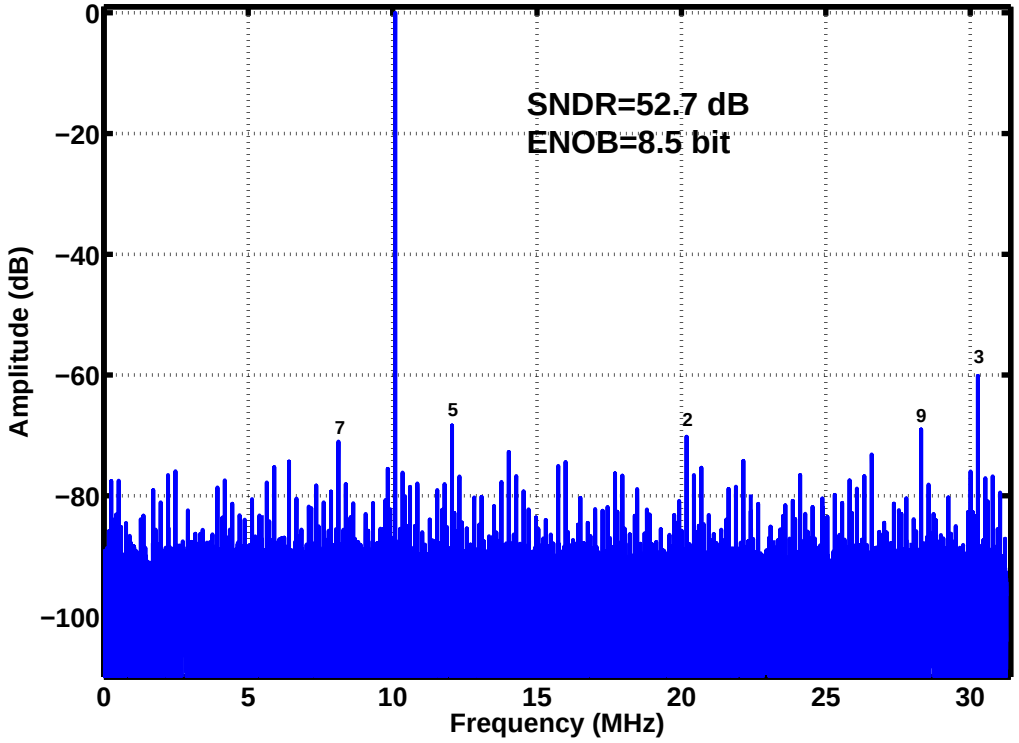


Figure 2.20: Measured DNL and INL at f_{sample}=1 GS/s with gain error calibration run at (a) 100 MHz and (b) 700 MHz.



(a)



(b)

Figure 2.21: Measured spectrum at f_{sample}=1 GS/s with (a) f_{in}=1.7 MHz and (b) f_{in}=490 MHz (down-sampled by a factor of 16).

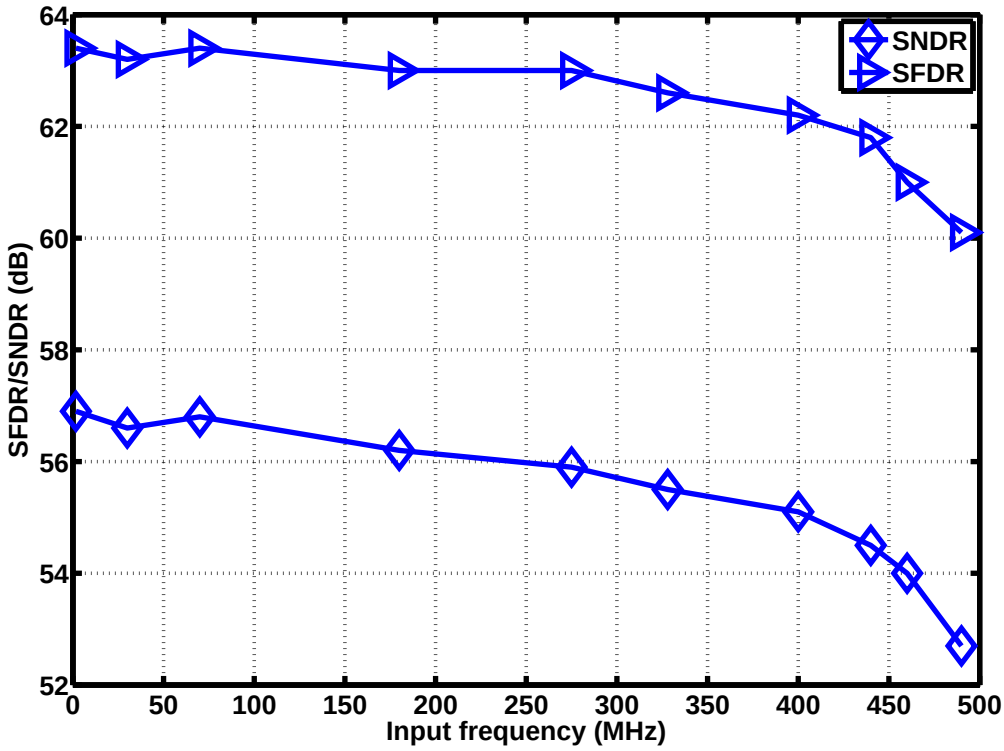


Figure 2.22: Measured SNDR/SFDR as a function of input frequency at f_{sample}=1 GS/s.

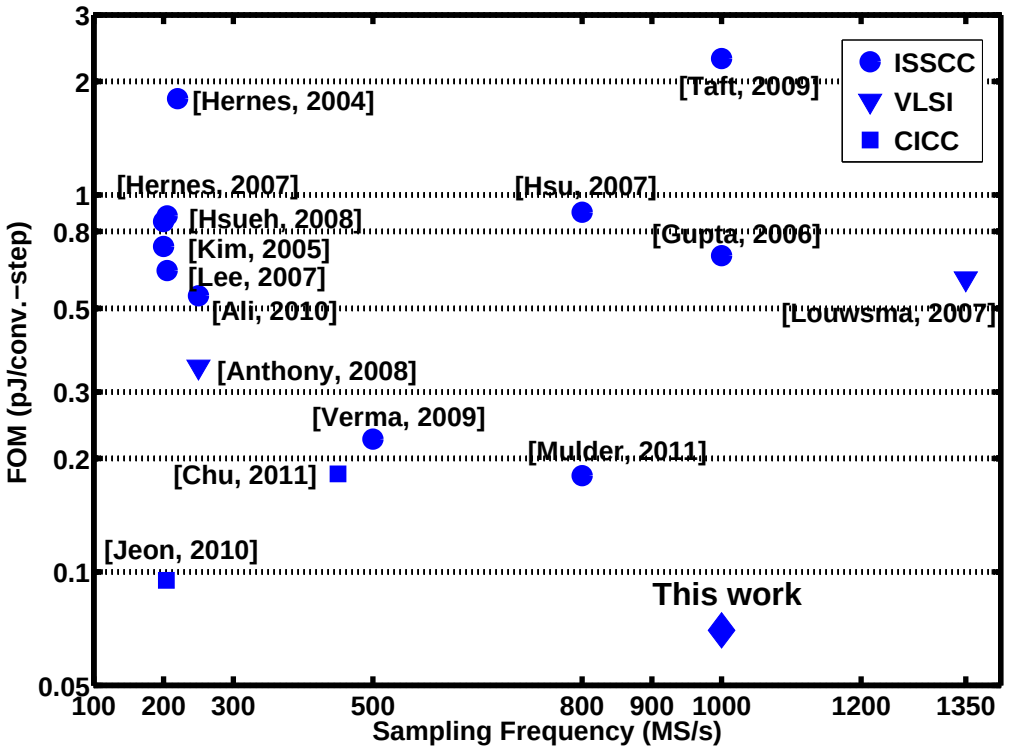


Figure 2.23: FOM comparison with the prior art.

CHAPTER 3

Design of an 8-bit 1.2-GS/s Two-Step Flash ADC

3.1 Introduction

Flash ADCs are the most popular architectures in high-speed low-resolution applications, due to their power efficiency. If higher resolutions are sought, however, flash architectures lose their attraction as their power and area grow exponentially. Two-step architectures, on the other hand, mitigate such issues by breaking the data conversion into two steps: coarse and fine; at the price of increased latency and requiring a high-speed highly-linear op amp to produce the residue voltage for the fine conversion block.

In this chapter, we present the design and implementation of an 8-bit two-step flash ADC that employs a powerful calibration technique along with the precharged resistor ladder DAC to operate at high frequencies with a low power consumption. In addition, circuit design techniques are proposed to increase the signal swing to rail-to-rail , operate the RDAC at lower frequencies, and reduce the flash ADC kick-back noise to the reference ladder. The latter two result in smaller static power burnt by the reference ladder. The achieved FOM is 32 fJ/conv.-step.

3.2 ADC Architecture

Shown in Fig. 3.1(a) is the block diagram of the proposed two-step flash ADC architecture that is composed of a 5-bit flash as the coarse ADC, a gain stage with double-sampling scheme[1] to relax the precharged RDAC settling performance, and a 5-bit fine flash.

The coarse ADC consists of 16 comparators and uses reference-swapping technique to resolve 5 bits. A sampling network together with a precharged RDAC generate the residue voltage by subtracting the analog equivalent of the input signal from the sampled input voltage. This difference is then amplified by a high-speed open-loop op amp, driving the fine ADC. The fine block is also a 5-bit flash ADC consisting of 31 comparators, out of which only 16 are activated for every data conversion, with the aid of subranging. Hence, the total number of active comparators involved for every data conversion is 32 that results in a considerable power saving. Moreover, a powerful calibration algorithm that corrects for the comparator offset (in coarse and fine blocks), gain error, and op amp nonlinearity (in fine block) is employed to relax the required comparator specifications resulting in more power saving.

To reduce the power consumptions of the fine resistor ladder, a double-sampling scheme, as depicted in Fig. 3.1(a) and explained with the aid of Fig. 3.1(b) is exploited. Two sampling networks 1 and 2 are used to enhance the settling performance of the MDAC. While the first network is sampling the current input, the second network is in the hold phase letting the MDAC (precharged RDAC and op amp) to take the entire ADC clock period for their settlings. It should be noted that, to employ precharging, two separate DAC switching networks are used, where their voltages are indicated by V_{DAC1} and V_{DAC2} in Fig.

[1] the bottom-plate sampling switches are not shown for simplicity.

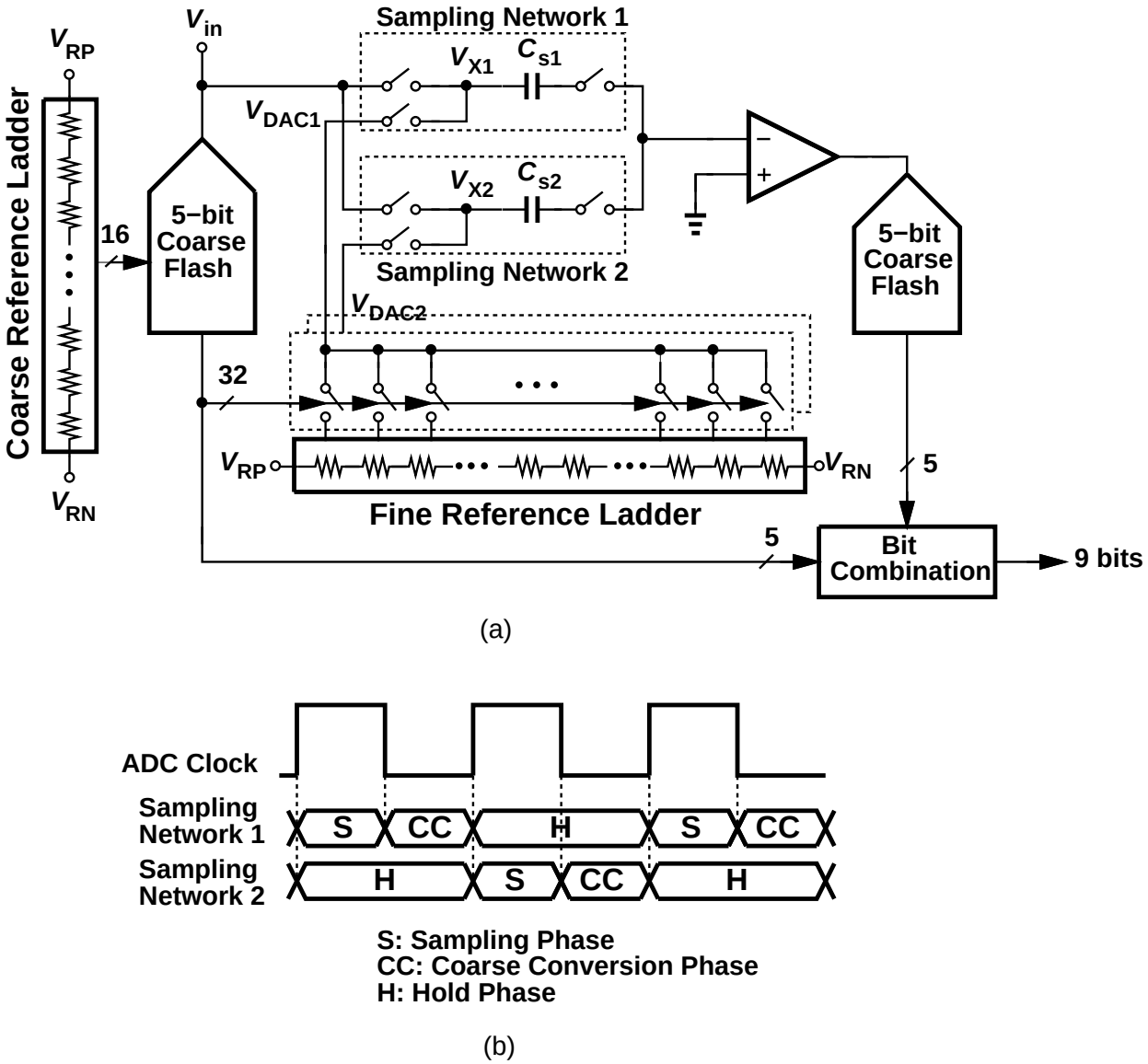


Figure 3.1: (a) Block diagram of the proposed ADC, and (b) timing diagram of the double-sampling scheme.

3.1 (a).

3.3 Design of the Coarse ADC

Since the coarse ADC (CADC) and the MDAC, both sample the input signal during the sampling phase, it is vital to match their sampling paths in order to reduce the timing mismatches, as explained in Chapter 2. Thus, a sampling network identical to the one used in the MDAC is employed in front of every coarse comparator to sample the input and the reference voltages and subtract them from each other, producing the residue voltage. Therefore, the comparator acts as a zero-crossing detector, generating high and low outputs for positive and negative residue voltages, respectively. The presence of the sampling network, however, limits the signal swing to half of V_{DD}, as explained in Section 2.5.2.

In this design, we introduce a reference-swapping technique to achieve a rail-to-rail signal swing in order to increase the ADC dynamic range. This techniques is shown in Fig. 3.2(a) and operates as following: after sampling the input signal, first, a high-speed sign-detector comparator is clocked, comparing the input voltage with the ADC common-mode voltage to detect sign of the input signal. Then, based on the decision of the sign-detector comparator, the sampling networks of the comparator bank sample either positive or negative reference voltages. Therefore, the residue voltage has a maximum swing of $V_{DD}/2$ and does not limit the signal swing, if the common-mode voltage is set to half of the supply voltage. After sampling the reference voltages, the comparator bank is clocked to coarsely digitize the input signal.

The timing diagram illustrated in Fig. 3.2(b) elaborates the operation of the CADC. After sampling phase finishes, the sign-detector comparator samples the signal common-mode level as its reference voltage and starts making its decision at time t_1 completing its conversion by time t_2. The reference controlling signals are then generated for the comparator bank and the coarse conversion clock

arrives at t_3. The rest of the clock period is allocated to the coarse conversion.

Although the reference-swapping technique reduces the available conversion time for the coarse ADC, but it is of minor importance since this design employs an offset calibration algorithm, and hence is effectively optimized for speed and noise performance. Moreover, enhanced signal swing allows for a larger tolerable error (noise and nonlinearity) thus considerably improving the SNDR.

3.3.1 Comparator Offset Calibration

Comparator offset is one of the main obstacles of designing high-resolution flash ADCs. Device mismatches are the primary sources of the offset that arise from random variations of the fabrication process parameters. Upsizing the devices reduces the mismatches due to the increased averaging, as discussed in [36]. Using larger devices, on the other hand, increases the area and power, degrading the achievable FOM, considerably. To overcome this issue, a number of offset calibration techniques have been proposed in the literature that compute and correct the offsets of comparators [10, 37].

The efficiency of a calibration technique is dependent upon two main parameters: (1) minimum offset correction step that determines the accuracy of the calibrated ADC, and (2) offset correction range that impels the maximum allowable offset and hence, device sizes and power consumption. It is desirable to correct a wide range of the offset with a fine step to achieve a low-power highly-linear design, while avoiding complicated calibration algorithms with bulky implementations. In this design, we utilize the reference ladder of the ADC to compensate for the comparator offsets by sliding their reference inputs along the ladder. This way, the reference voltage is different from the nominal value to include the effect of the comparator offset.

The offset calibration algorithm is shown in Fig. 3.3(a) for one comparator. During Calibration, the comparator is disconnected from the input sampling the nominal reference voltage instead. The reference input of the comparator slides along the offset correction range looking for a proper tap. For each comparator, the algorithm operates as following:

1) Set the calibration voltage to the first tap of the correction range, i.e. $V_{cal} = V_{tap,i}, \quad i = 1$.

2) The nominal reference voltage is sampled as the input of the comparator.

3) The calibration voltage is sampled as the comparator reference voltage.

4) Comparator is clocked and its output is stored in the processing block.

5) Rea peat (1-3) k times[2] to average out noise.

6) From the stored data, measure the average duty cycle of the comparator output by counting 1s and 0s.

7) Move the calibration voltage to the next tap of the correction range, i.e. $V_{cal} = V_{tap,i}, \quad i = i + 1$; If still in the correction range, go back to step (2).

Fig. 3.3(b) shows the output of the comparator under calibration while connected to a proper reference tap that compensates for the comparator offset. Ideally, if the calibration resolution is high enough, there is a calibration tap that completely compensates for the comparator offset and places the comparator in metastable condition generating a $50-\%$-duty-cycle output. However, due to the finite resolution of the calibration algorithm that is determined by the size of the calibration step, the offset is not fully compensated resulting in an uncalibrated offset voltage, V_{UC} in Fig. 3.3(b). In this design, since we are utilizing the reference ladder of the coarse block to calibrate its comparator offsets, the maximum amount of V_{UC} is equal to the half of coarse LSB.

[2]k depends on the comparator noise and the calibration hardware.

3.4 Design of MDAC

Fig. 3.4(a) shows the circuit implementation of the MDAC in detail. As described earlier, to enhance the operation speed of the RDAC, a double-sampling scheme is employed that consists of two input sampling paths functioning in parallel in time. All the switches are implemented as transmission gates (TGs) except for those indicated by circles that are bootstrapped switches.

The MDAC timing waveforms are depicted in Fig. 3.4(b) and the circuit operates as following: During the sampling phase of the first sampling path, Ph_{S1}, the input is sampled on the sampling capacitor C_{S1} through bootstrapped and TG switches. Then at the falling edge of the early phase, Ph_E, the bottom-plate sampling is finished and the MDAC holds the sampled voltage until the decision of the coarse ADC arrives and drives the output of the first RDAC switching network, i.e. V_{DAC1}, to the analog equivalent of the input. It should be noted that the sampling instant is determined by the falling edge of Ph_E that is in common among the two sampling paths of MDAC and those of the coarse ADC, to minimized the timing errors. The reference sampling starts at the rising edge of Ph_{DAC1} and takes the entire period of the clock to settle, as a result of double-sampling scheme. Precharging with the input voltage at node V_{X1} also significantly increases the RDAC settling. Hence, a $2-k\Omega$ resistor ladder affords fast settling within $\frac{LSB}{2}$ while operating at 1.2 GS/s.

While the first sampling path is holding the previous sample and the MDAC is amplifying the resulting residue voltage, the second sampling path starts sampling the current input voltage during Ph_{S2} and the data conversion follows afterwards in the same manner as described above.

The op amp of the MDAC requires relaxed linearity and speed specifications

because its signal swing is very low and it has an open-loop configuration. Thus, a simple differential pair with resistive loads has been employed to provide a gain of about 7 (Fig. 3.5). Also, to save power, the op amp switches off by cutting off the tail current during the sampling phase. Since the input of the op amp swicthes between the two sampling paths, a memory from the previous sample can affect the current sample, hence degrading the performance. To avoid this issue, resetting switches have been added at the inputs of the op amp to remove the memory effect. In addition, a bleeding current source with a small current is used to enhance the speed.

Another issues attributed to the op amp are the gain error and variation of gain at different process corners and temperatures. The gain of the op amp is roughly $g_m.R_D$, where g_m is the transconductance of the input devices, $M_{1,2}$. Values of both g_m and R_D are dependent upon process parameters and temperature and thus, gain of the op amp is not accurately known and varies with process and temperature. According to simulations, the op amp gain exhibits 20% variation over different process corners. We address these issues by proposing a powerful calibration method in the fine block that simultaneously corrects for gain error and comparator offsets. Section 3.5.1 describes the details of the proposed calibration method.

3.5 Design of the Fine ADC

The fine ADC (FADC) digitizes the amplified residue voltage to provide 3-bit effective resolution. The FADC also needs to accommodate enough overlapping to digitally correct for (1) coarse comparator noise, (2) coarse comparator uncorrected offset, and (3) timing mismatches between the CADS and the MDAC. Hence, 31 comparators have been employed to resolve 5 bits. To save power,

three techniques are used: subranging, pipelining, and calibration. We discuss the first two in this section and calibration is described in the next section.

Fig. 3.6(a) shows the pipelining scheme at the input of the FADC. The amplified residue voltage is sampled on the input capacitance of the comparators and additional hold capacitors C_H. This way, the op amp and the FADC, each have half of the ADC clock period to settle and finish the conversion, respectively. After amplification phase Ph_{AMP} is over, the sampling swicthes turn off and the FADC is clocked. The addition of the hold capacitor C_H slows down the op amp, but improves the thermal noise and reduces the effect of comparator kick-back noise after FADC is clocked. In addition, it reduces the effect of nonlinear input capacitance of the fine comparators. Since the adjacent comparators make their decisions almost simultaneously, the effect of their kick-back noise on each other is less. Thus, three separate sampling paths are used to isolate the kick-back noise of one comparator bank from another bank.

Fig. 3.6(b) shows the subranging scheme that reduces the number of clocked comparators and leads to power saving. To this aim, first, a sign-detector comparator is clocked, comparing the sampled signal with zero, then if the signal is larger than zero, the positive comparator bank is clocked. Otherwise, the negative comparator bank is clocked. Each comparator bank is composed of 14 comparators. Moreover, to reduce the effect of the sign-detector noise, the very last and very first comparators of positive and negative banks are always clocked. Hence, only 17 comparators are active for each data conversion that results in about 50% power reduction. Fig. 3.7 shows the comparator circuit along with the device sizes.

The outputs of the comparators are converted to one-of-N-code by using 3-input NAND gates to reduce the bubble effect. Then, using a ROM as described

in Fig. 2.14, the binary outputs are produced.

3.5.1 Fine ADC Calibration

The calibration of the fine ADC is critical because the accuracy of the ADC is ultimately limited by the accuracy of the fine block. Thus, the fine calibration algorithm must correct for all the present errors with an adequately fine correction step. The required correction range is determined by the followings:

1) Fine comparator offset

2) Fine comparator noise

3) Fine comparator kick-back noise

4) Charge injection and clock feedthrough

5) Op amp gain variation

6) Op amp non-linearity

7) Incomplete residue settling.

The proposed calibration algorithm reduces the above errors to less than 1 LSB by adjusting the reference voltages of the fine ADC comparators. To compute the amount of error, precise calibration voltages provided by the fine ladder are sampled instead of input signal. Configured as a gain stage, the op amp then amplifies the sampled voltage and feeds the fine ADC. The comparator offset correction mechanism is same as the offset correction algorithm introduced in 3.3.1. Moreover, by distorting the reference connections of the fine comparators, the threshold levels are adjusted such that the other mentioned errors (errors 3-7) are corrected too, given that the input/output characteristic at the input of the fine block is monotonic.

Fig. 3.8 conceptually shows how the comparator threshold voltage adjustment removes the errors. First, in Fig. 3.8(a) the ideal residue-input characteristic is

shown where no error is present and hence, the fine threshold voltages are evenly positioned across the residue voltage swing. Then, in Fig. 3.8(b) and (c), cases are shown where the gain error and nonlinearity exist, respectively. Thus, the fine threshold levels are expanded and distorted to correct for gain and nonlinearity errors.

3.5.2 Comparator Kick-Back Noise

As described in 2.5.2, a crucial issue in sharing a single resistor ladder between the MDAC and the fine ADC is the kick-back noise of the FADC comparators, which disturbs the reference voltages of the MDAC and could result in significant performance degradation. The kick-back noise has two differential and common mode components. One way to reduce the differential term, as explained previously in 2.5.2, is to use cross-connected devices in parallel with the input transistors. The common-mode term could also be troublesome as it can change the common mode level at the input of the comparators and reduce heir gains and performance.

In this design, we introduce a compensation circuit technique to reduce the common-mode and differential terms of the kick-back noise, without significantly degrading speed and power. The kick-back noise occurs afetr both rise and fall edges of the clock. After clock goes high, nodes X, Y, $P1$, and $P2$ in Fig. 3.7 are rapidly discharging to zero coupling to the input signal and reference voltages. In addition, after clock goes low, the comparator enters reset phase and nodes X and Y are charged up to V_{DD} causing voltage coupling to the inputs.

Fig. 3.9 illustrate the circuit technique that compensates for the kick-back noise. For simplicity, only one of the differential pairs of the comparator is shown while the other differential pair uses the same scheme. Transistors M_X and M_Y are added at the signal and reference inputs to resemble a charge injection equal

to kick-back noise charge injection, but with opposite signs. The circuit operates as following: when clock goes high, nodes X, Y, $P1$, and $P2$ are discharging injecting negative charge into input nodes. Meanwhile, since M_X and M_Y connect to V_{DD}, the charge due to the kick-back noise is compensated. When clock goes low, the resetting swicthes drive the internal nodes of the comparator to V_{DD}, injecting positive charge to the inputs. In this case, M_X and M_Y connect to GND, supplying negative charge.

Another concern arising from ladder sharing, is coupling between the input and reference nodes of the comparator, as shown in Fig. 3.10. To resolve this issue, a resetting switch is added that resets the sources of input devices to V_{DD} and removes the coupling.

3.6 Measurement Results

The prototype ADC is fabricated in 65-nm standard CMOS technology. The die active area is $280\,\mu$m $\times 425\,\mu$m. The ADC reference voltages are provided externally and the calibration is performed off-chip.

Due to a layout mistake, half of the comparators in the fine block are not functional, thus the ADC suffers from a large quantization noise. Fig. 3.11 shows the INL/DNL plots of the calibrated ADC, at the sampling rate of 1.2 GHz, where the maximum INL and DNL reach 0.66 LSB and 0.86 LSB, respectively. The maximum SNDR is 46.6 dB at a sampling rate of 1.2 GS/s, as illustrated in Fig. 3.12 that plots the SNDR versus input frequency. The SNDR falls to 44 dB at the Nyquist rate, mainly due to the limited bandwidth of the input sampling networks. Fig. 3.13 shows the spectrum of the ADC output for an input frequency of 590 MHz.

Discounting power of non-functional comparators, the total power consumption of the ADC is 6.8 mW from a 1-V supply. The achieved FOM is about 30 fJ/conv.-step. Despite the layout mistake, the FOM is still comparable with the state of the art, as depicted in Table 3.1.

Table 3.1: Performance Summary of the Two-Step Flash ADC [5, 10, 20]

	This Work	VLSI' 11 [Chung]	VLSI' 12 [Chan]	VLSI' 08 [Tu]
Technology (nm)	65	55	65	65
Supply Voltage (V)	1	1.2	1	1.2
Resolution (bit)	8	8	8	8
Sampling Rate (GS/s)	1.2	1	1	0.8
ENOB @ Nyquist (dB)	7	6.2	6.8	7.1
Power (mW)	6.8	16	3.8	30
FOM (fJ/conv.−step)	32	125	24	187
Area (mm^2)	0.12	0.2	0.013	0.12

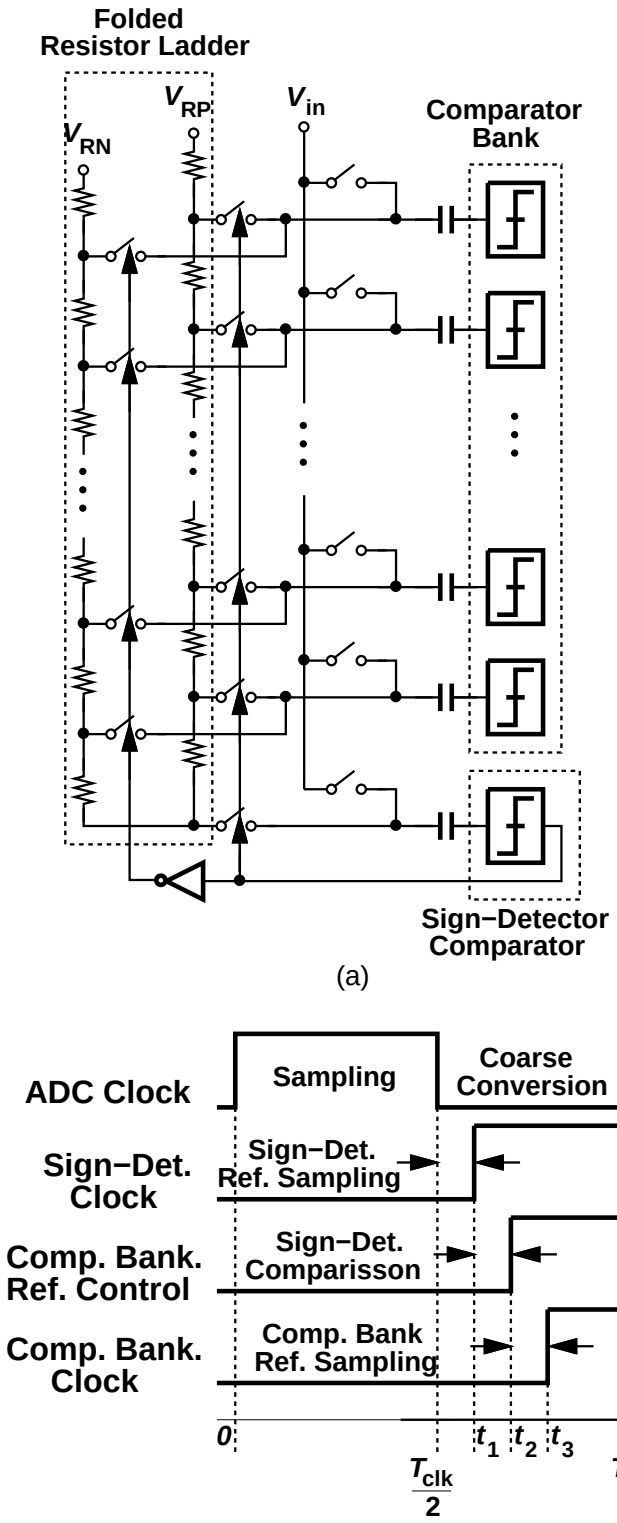


Figure 3.2: (a) Coarse ADC and (b) its timing diagram.

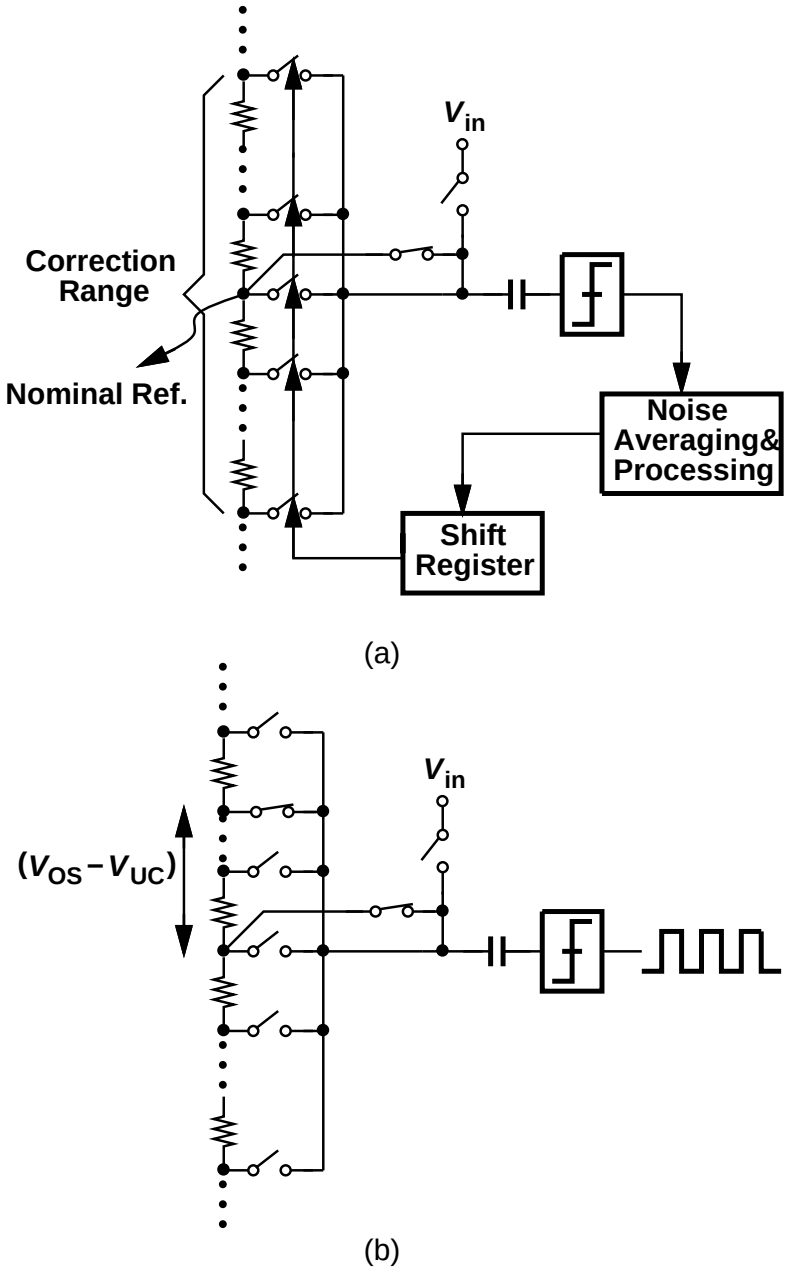


Figure 3.3: (a) Comparator offset calibration technique and (b) comparator output while connected to a proper references tap.

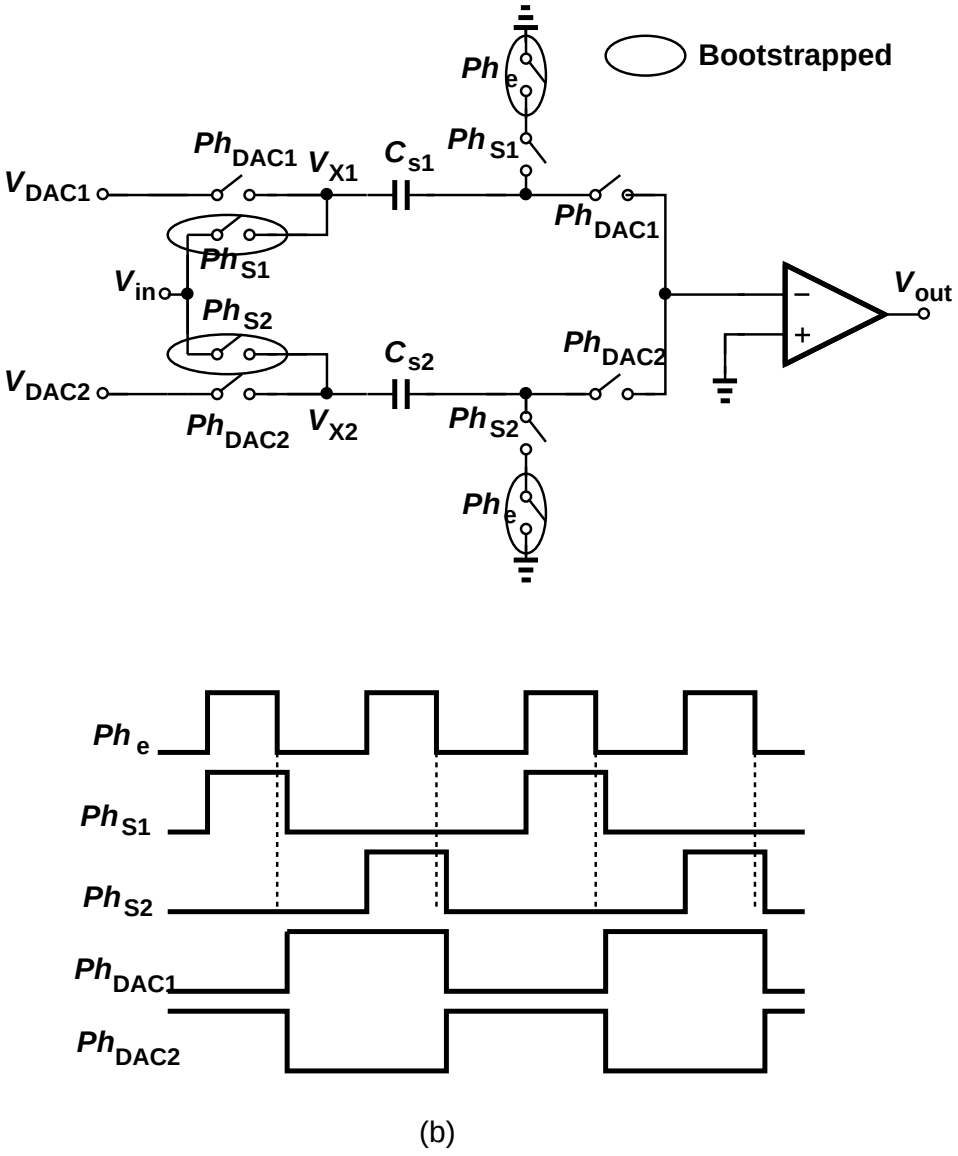


Figure 3.4: (a) MDAC circuit and (b) MDAC timing waveforms.

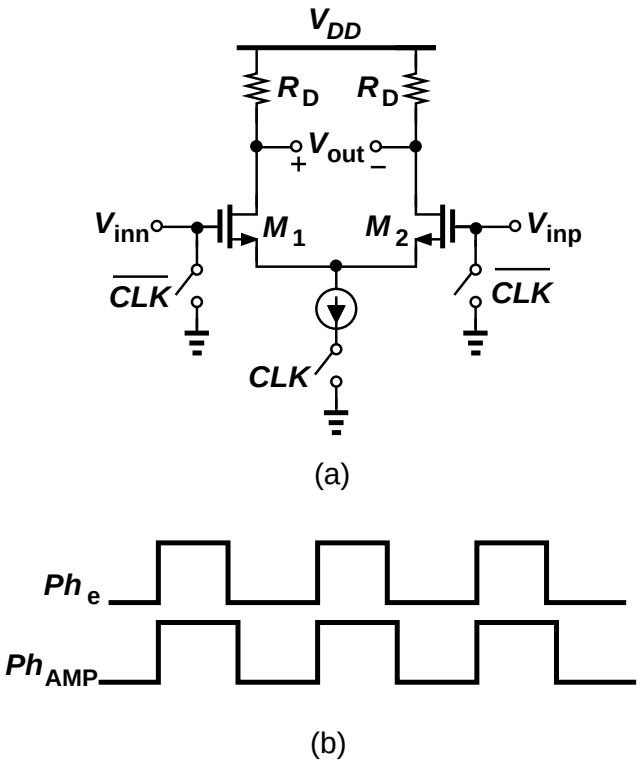


Figure 3.5: Op amp implementation.

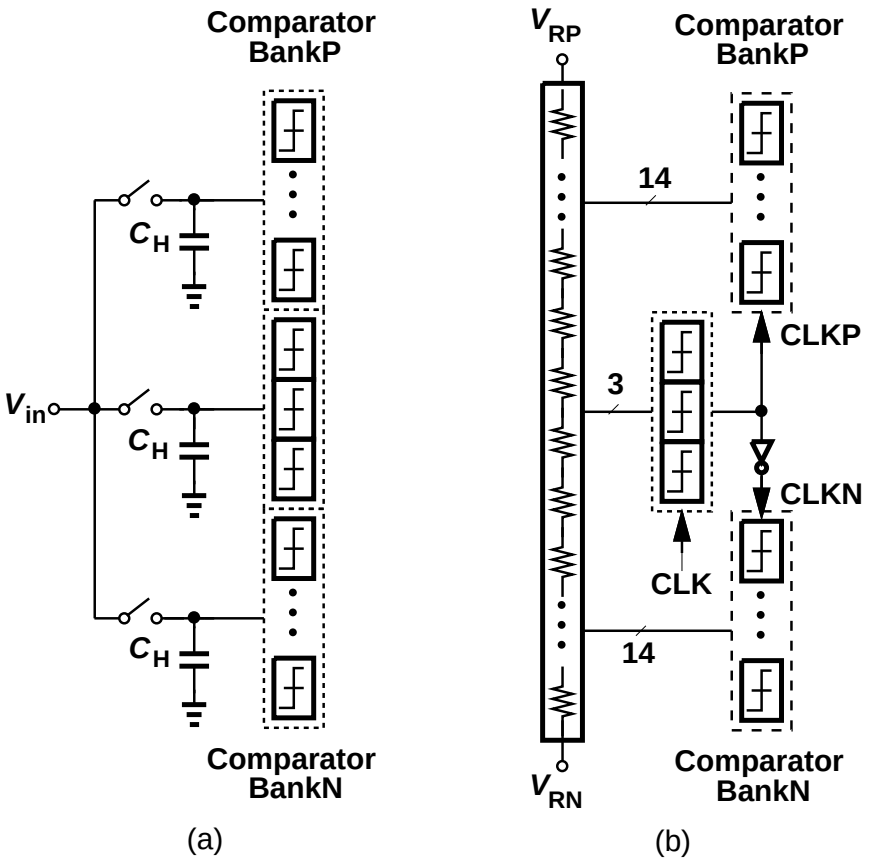
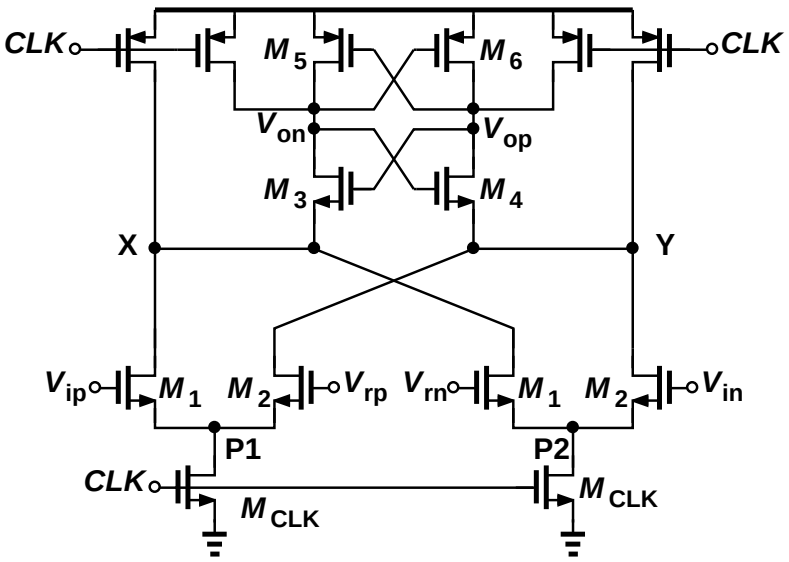


Figure 3.6: (a) Pipilining and (b) subranging in the FADC.



Device	Size ($\mu m/\mu m$)
$(W/L)_{1,2}$	6/.06
$(W/L)_{3,4}$	1/.06
$(W/L)_{5,6}$	0.5/.06
$(W/L)_{CLK}$	0.5/.06

Figure 3.7: Fine ADC comparator circuit and device sizings.

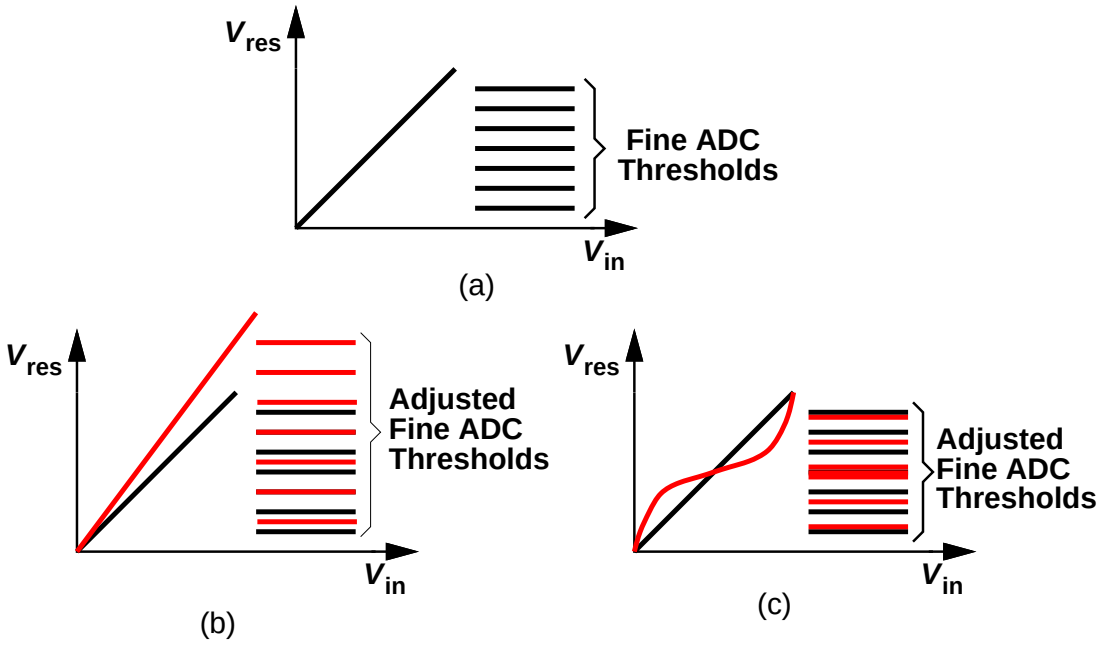


Figure 3.8: Residue-input characteristic in fine comparator thresholds positions (a) ideal case with no error (b) with gain error (c) with nonlinearity error.

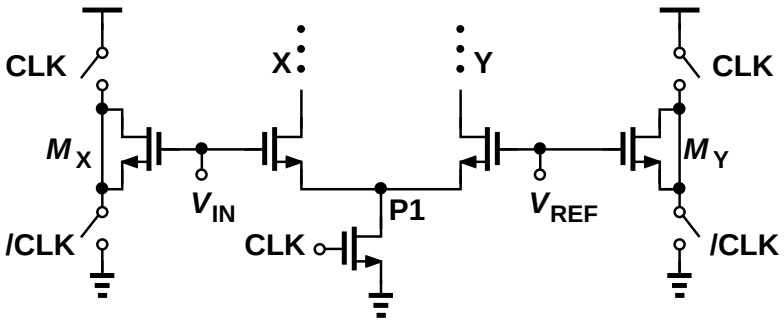


Figure 3.9: Kick-back noise reduction technique.

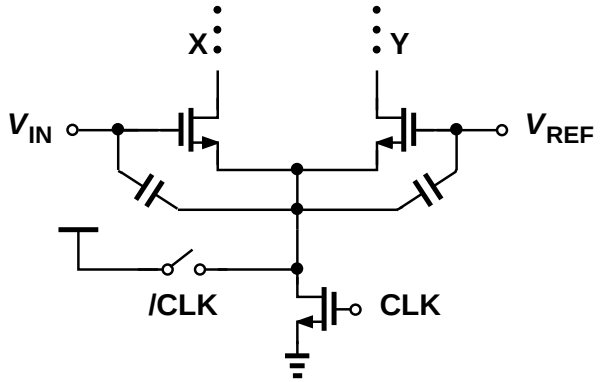


Figure 3.10: Kick-back noise reduction technique.

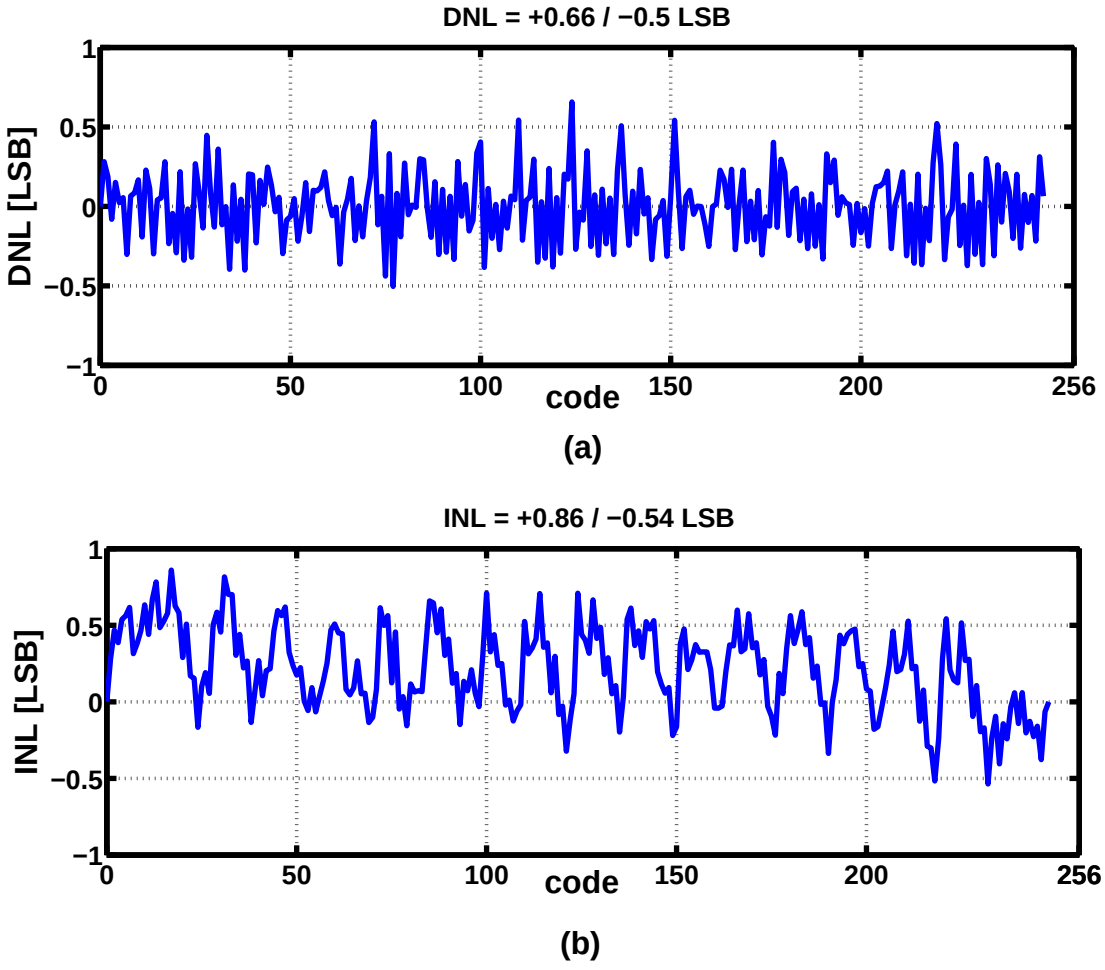


Figure 3.11: Static measurement results at $f_s = 1.2GS/s$.

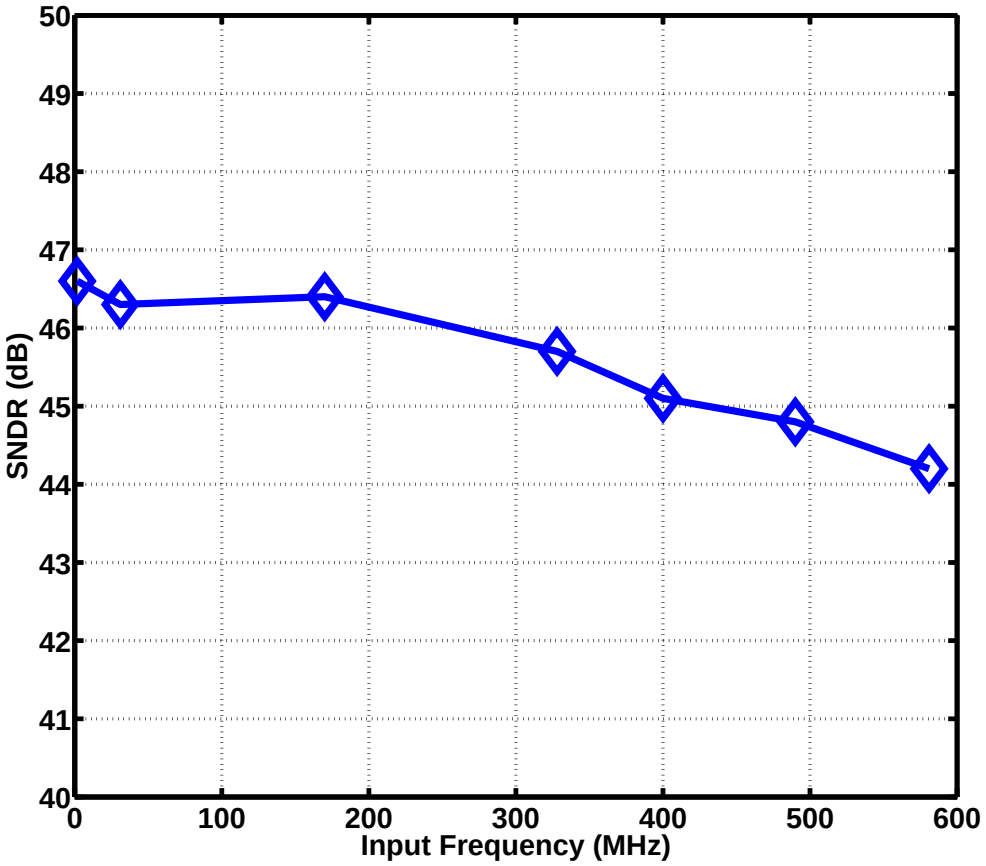


Figure 3.12: Dynamic measurement results at $f_s = 1.2GS/s$.

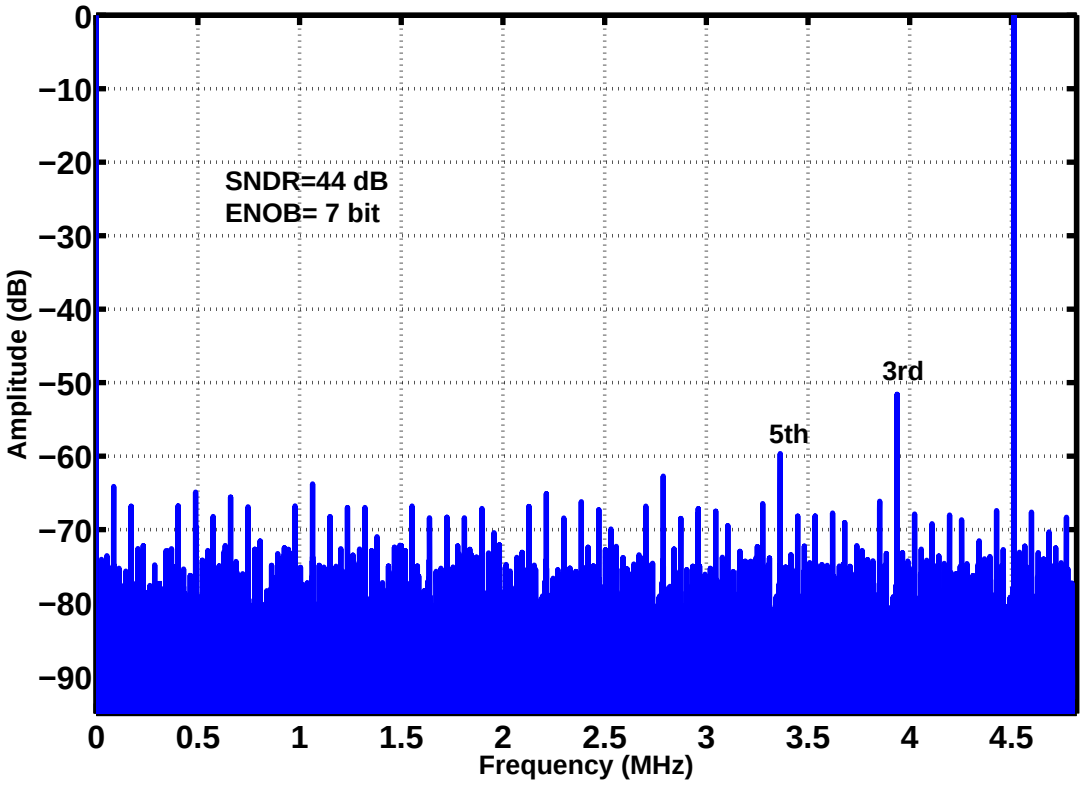


Figure 3.13: ADC output spectrum for $f_{in} = 590MHz$.

CHAPTER 4

Analysis of Metastability in Pipelined ADCs

4.1 Introduction

A critical issue in the design of high-speed ADCs relates to the errors that result from comparator metastability [38]. Studied for only flash architectures, this phenomenon assumes new dimensions in pipelined converters, creating far more complex error mechanisms. In this chapter, we present a comprehensive analysis of comparator metastability effects in pipelined ADCs and develop a method to precisely predict the error behavior for a given input signal p.d.f.

4.2 Metastability in ADCs

Comparators are the main building blocks of the ADCs that convert the input signal, from analog to digital domain. When the input voltage level is sufficiently close to the comparator threshold level, the comparator outputs take long time to reach logic voltage levels. This effect is illustrated in Fig. 4.1, where a typical case is shown, in which a preamp senses the analog voltage difference and drives the latch. The latch block regeneratively amplifies the voltage difference and drives the logic block. As the waveforms show, for small input voltage differences, the outputs of the logic do not reach the valid logic levels within the available comparison time, which is half of the clock period in most cases. Therefore, the

outputs of the logic block are undefined and can lead to different types of errors depending on the ADC architecture.

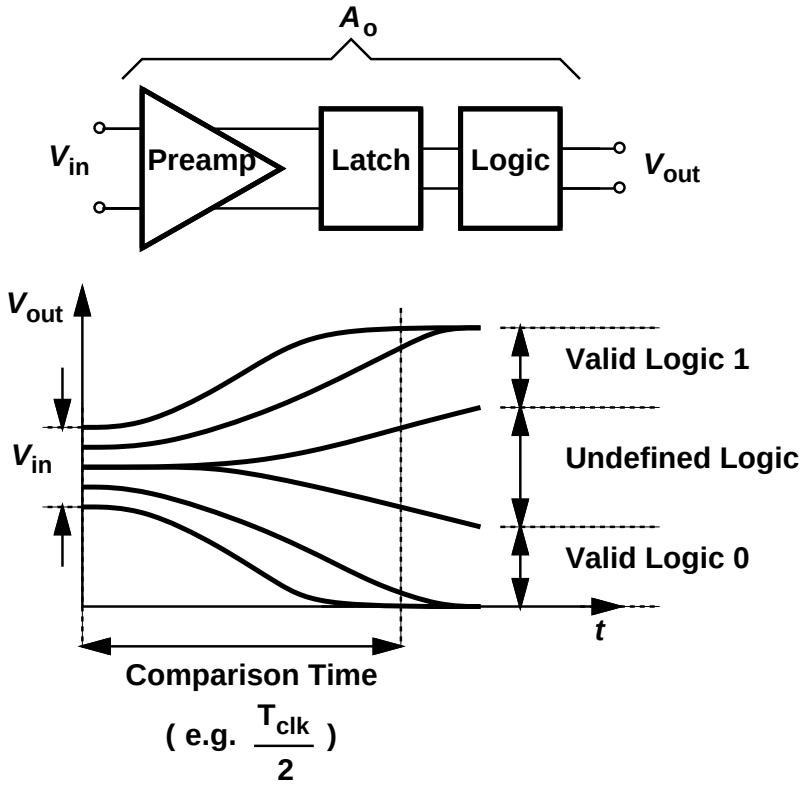


Figure 4.1: Due to the comparator metastability, its digital outputs do not reach a valid logic level within the available comparison time.

It can be shown that the voltage level at the output of logic block in Fig. 4.1 is

$$V_{out}(t) \; = \; A_o e^{(\frac{t - t_1}{\tau_{lat}})} V_{in}, \tag{4.1}$$

where, A_o is the overall voltage gain from the preamp input to the logic output, t_1 is the delay time required to turn on the latch, and τ_{lat} is the latch regenerative time constant. It is evident that small input voltages require longer time for the outputs to reach a valid logic level.

Shown in Fig. 4.2, is a flash architecture with a metastable comparator. The amount of metastability error in a flash converter is dependent upon its thermometer code detector and encoder. The probability of error, is straightforward and has been shown that, for a uniformly distributed signal, is given by [39]:

$$P_E(t) = \frac{2(2^n - 1)V_o}{V_{REF}A_o} e^{\frac{-t}{\tau_{lat}}}. \tag{4.2}$$

V_o and V_{REF} in Eq. 4.2 are the valid logic level and the full range of the input signal, respectively. There are a number of techniques that can be employed to reduce the amount and the probability of error in a flash ADC. For example, pipelining extends the latch time, reducing the probability of error arbitrarily. In addition, proper encoder designs lead to a small amount of error. Duplex-Gray-encoded ROM results in an error of 4 LSB and Gray-encoded ROM along with valid-high comparators in [40] achieve only 1 LSB error.

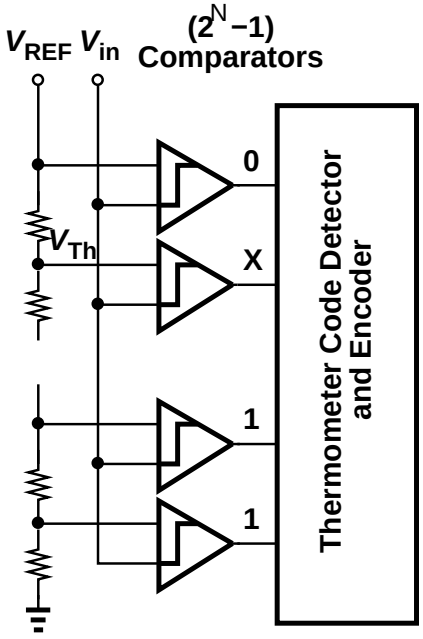


Figure 4.2: Flash architecture.

Metastability in the piepilined converters, on the other hand, is far more com-

plex. The comparator is in the critical path, thus pipelining can not be employed. Metastability leads to different error mechanisms and creates error magnitudes that are dependent on the input voltage level. Our goal is to determine the probability of error versus the magnitude of error.

To recall the operation of a pipelined ADC, Fig. 4.3 shows a block diagram of a pipelined architecture and its timing waveforms. After the sampling phase, V_{in}

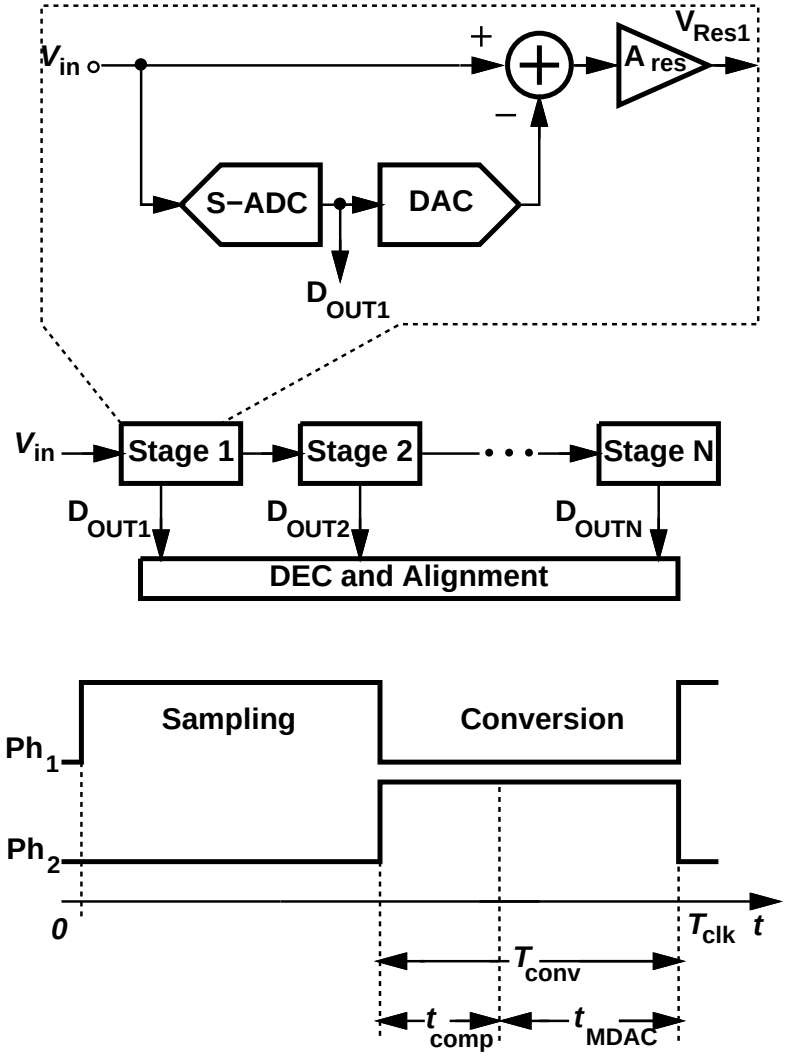


Figure 4.3: Block diagram of a pipelined ADC with its timing waveforms.

is held and the conversion begins by the sub-ADC quantizing the input signal. The sub-ADC comparators complete their decisions in t_{comp} and drive the DAC to convert the produced digital code D_{OUT1} to its equivalent analog voltage. The DAC voltage is subtracted form the held signal and the difference is amplified by the gain of A_{res}. The amplifier output settles to a constant value, V_{Res1}, and is sampled by the following stage. The available time for the DAC voltage acquisition and residue settling is t_{MDAC}.

For an input voltage level that is near to a threshold level of the sub-ADC, the corresponding comparator becomes metastable and takes longer time to complete its decision. Therefore, t_{comp} increases, resulting in smaller t_{MDAC}. As a result and depending on how deep the comparator is in metastable condition, an error mechanism happens that produces a residue error, which propagates to the subsequent stages.

Shown in Fig. 4.4, is a block diagram of a 1.5-bit pipelined stage consisting of a sub-ADC, a switched-capacitor sampler and subtractor, and a residue amplifier. When a sub-ADC comparator is metastable, three distinct error mechanisms are identified: 1) sub-ADC output does not turn on the DAC switch, 2) sub-ADC output turns on the DAC switch, but very slowly, resulting in DAC settling error and op amp settling error, and 3) DAC and decoder interpret the metastable output of sub-ADC inconsistently.

In this Section, we study these error mechanisms in details for a non-flip-around 1.5-bit stage and we show that similar analysis applies to stages with other resolutions.

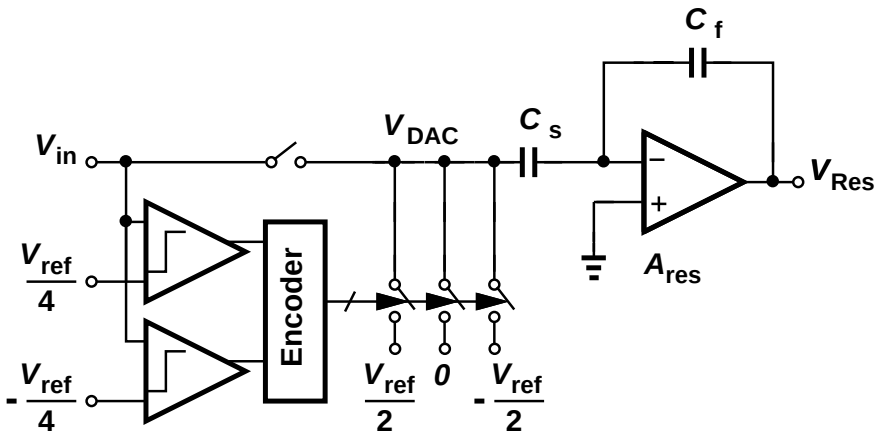


Figure 4.4: Block diagram of a 1.5-bit pipelined stage.

4.3 Modeling Approach

4.3.1 Comparator Modeling

The outputs of the sub-ADC comparator latch drives the logic block as depicted in Fig. 4.5. For a metastable comparator, it can be shown that the logic voltage, V_{Logic}, which drives the DAC switch, is given by:

$$V_{out}(t) \; = \; A_1 A_2 e^{(}\frac{t - t_1}{\tau_{lat}})A_1 V_{in}, \tag{4.3}$$

where A_1, A_2, and A_3 are the voltage gains associated with preamplification, latching, and logic blocks and related to their circuit parameters. [34] conducts an accurate analysis for a StrongARm comparator and extracts the circuit parameters.

4.3.2 DAC Switch Modeling

To model the gradual turn-on of the DAC switch, we assume an abrupt, but delayed turn-on together with an average conductance, as illustrated in Fig. 4.6. The average conductance corresponds to the gate voltage level V_{ON} and the switch

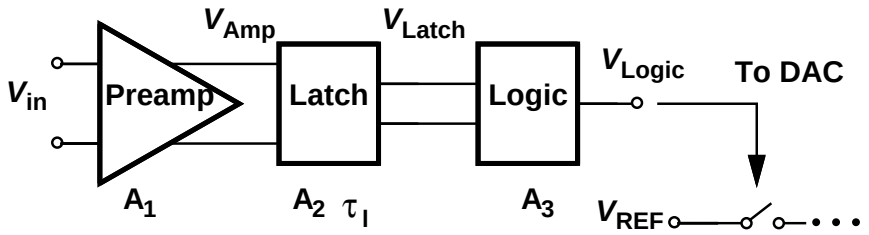


Figure 4.5: Sub-ADC comparison time modeling.

turn-on time t_{ON} and is half of the switch conductance when V_{Logic} reaches the rail voltage. The required comparison time, t_{comp}, is obtained from Eq. 4.3 and is

$$t_{comp} = t_1 + \tau_{lat} \ln \frac{V_{ON}}{A_o|V_{in} - V_{Th}|}, \tag{4.4}$$

where A_o is the overall voltage gain. The available time for the MDAC settling is then

$$t_{MDAC} = T_{conv} - t_{comp}. \tag{4.5}$$

To simplify our study, we remove t_1, which is a delay term, from Eq. 4.4, while its effect can be easily absorbed into the voltage gain A_o.

4.3.3 MDAC Modeling

The settling of the DAC in Fig. 4.4 is formulated as a RC settling model given by

$$V_{DAC} = D_{in}\frac{V_{ref}}{2}(1 - e^{-\frac{t_{MDAC}}{\tau_{DAC}}}) + V_{in}e^{-\frac{t_{MDAC}}{\tau_{DAC}}}. \tag{4.6}$$

The first term in Eq. 4.6 shows the settling of the DAC voltage to its final value, whereas the second term indicates the initial condition. Besides, D_{in} denotes the sub-ADC decision that has one of the following values: -1, 0, or 1. The DAC time constant, τ_{DAC} is given by

$$\tau_{DAC} = R_{sw}\, C_{DAC}, \tag{4.7}$$

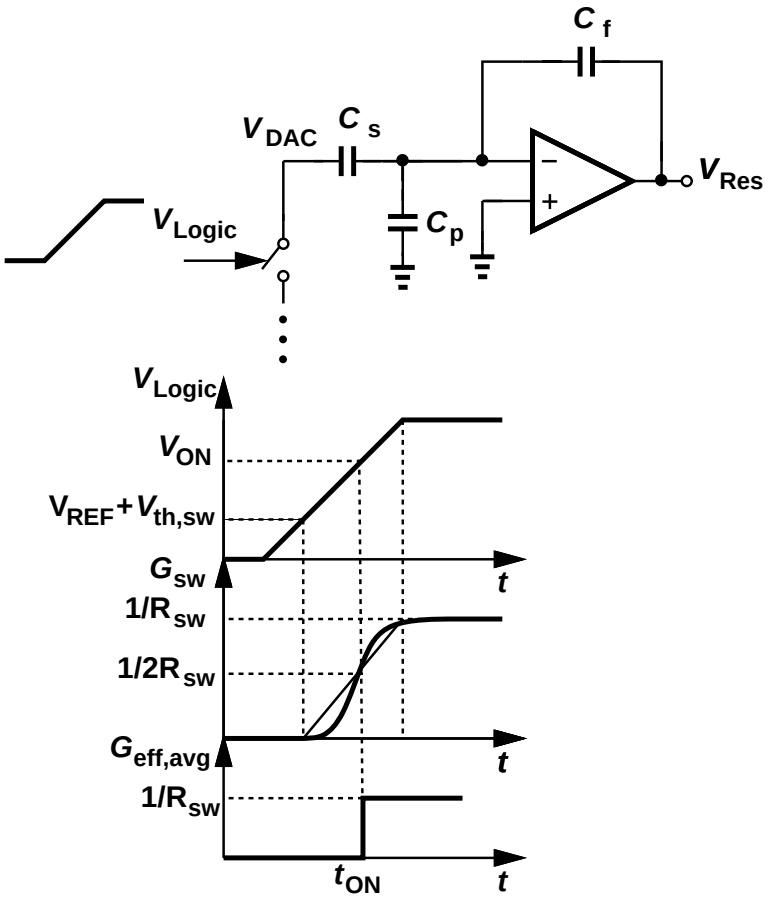


Figure 4.6: Gradual turn-on of the DAC switch and its conductance modeling.

where C_{DAC} is the capacitance seen at the output of DAC, i.e. node V_{DAC}, and can be obtained as

$$C_{DAC} = \frac{C_S[C_p + (1 + A_{res})C_F]}{C_S + [C_p + (1 + A_{res})C_F]}, \tag{4.8}$$

and R_{sw} is the switch average resistance, as shown in Fig. 4.6.

The residue settling is approximated by two independent terms and with a single-pole model for the residue op amp as:

$$V_{Res} = A_{res}(V_{in} - V_{DAC})(1 - e^{-\frac{t_{MDAC}}{\tau_{amp}}}), \tag{4.9}$$

where A_{res} and τ_{amp} are the residue gain and the op amp settling time constant,

respectively. It should be noted that, for simplicity, the op amp slewing is not included in this analysis, which is a reasonable assumption in low-swing high-speed designs. However, we show later that the effect of slewing can be added to this analysis as a simple delay term.

4.4 Metastability Error Mechanisms in a Pipelined ADC

4.4.1 Sub-ADC Output Does Not Turn on the DAC Switch

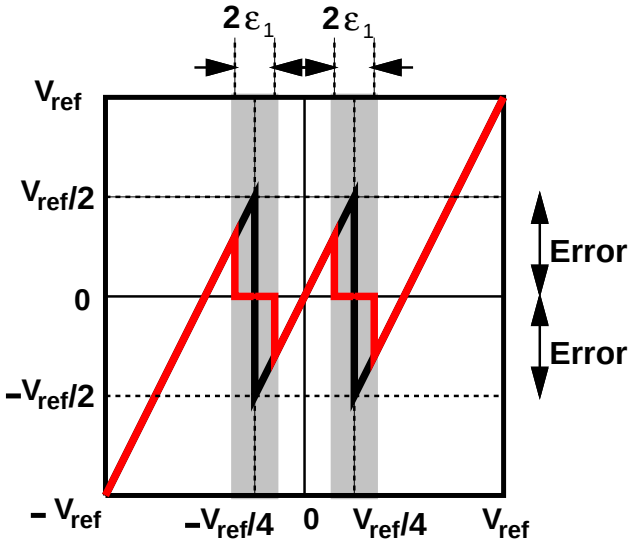


Figure 4.7: Residue error for a 1.5-bit stage when MDAC does not receive any decision from the sub-ADC.

For the input voltage levels that are too close to a threshold voltage such that the required sub-ADC conversion time, i.e. t_{comp}, is longer than the total conversion time, i.e. T_{conv}, the DAC does not receive any decision from the sub-ADC and the MDAC produces zero at its output. This effect is shown in Fig.

4.7 for a 1.5-bit stage. The resulting input-referred error is [1]

$$E = \pm \frac{1}{A_{res}^{N-1}} \frac{V_{ref}}{4}, \tag{4.10}$$

where N and A_{res} denote the number of stage and the gain of all stages, respectively. The corresponding metastability region is defined by ε_1 and can be calculated using Eq. 4.4 as following

$$\varepsilon_1 = \frac{V_{ON}}{A_o\, e^{\frac{T_{conv}}{\tau_{lat}}}}. \tag{4.11}$$

For input voltage levels closer to the sub-ADC threshold than ε_1, the resulting error stays constant as $error_{meta}$. It should be noted that, even though the sub-ADC comparator does not complete its decision within T_{conv}, by proper decoder design and due to the presence of several stages of pipelined aligning latches in a pipelined architecture, it is less probable that the digital outputs do not reach valid logic levels. Thus, the output digital code of the stage is correct while its residue voltage has an error of $error_{meta}$.

4.4.2 Incomplete Reference Acquisition and Residue Settling

For the input voltage levels further away from the sub-ADC threshold than ε_1, but within ε_2 in Fig. 4.8, the MDAC receives the decision of the sub-ADC metastable comparator after t_{comp}. But, since t_{MDAC} is short, the acquisition of the DAC reference voltage is incomplete resulting in a large residue error.

To calculate the amount of residue error, we combine Eq. 4.6 and 4.9:

$$\begin{aligned} V_{Res} &= A_{res}(V_{in} - V_{DAC})(1 - e^{-\frac{t_{MDAC}}{\tau_{amp}}}) \\ &= A_{res}(V_{in} - D_{in}\tfrac{V_{ref}}{2}(1 - e^{-\frac{t_{MDAC}}{\tau_{DAC}}}) - V_{in}e^{-\frac{t_{MDAC}}{\tau_{DAC}}})(1 - e^{-\frac{t_{MDAC}}{\tau_{amp}}}). \end{aligned} \tag{4.12}$$

[1] Assuming all the stages have gains of A_{res}

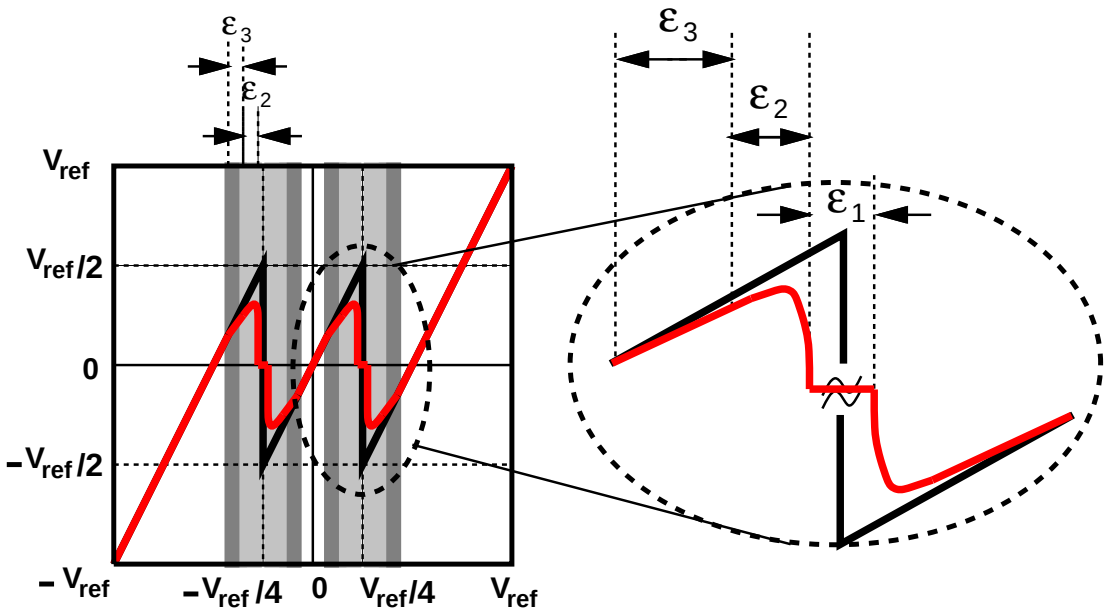


Figure 4.8: Residue error for a 1.5-bit stage due to the incomplete reference acquisition and op amp settling.

By rewriting Eq. 2.8 while substituting V_{in} by $\pm\frac{V_{FS}}{4}$ and D_{in} by $1, 0, -1$ we obtain

$$\begin{aligned} V_{Res} &= A_{res}(V_{in} - D_{in}\frac{V_{ref}}{2}) \\ &\pm A_{res}\frac{V_{ref}}{4}(e^{-\frac{t_{MDAC}}{\tau_{DAC}}} + e^{-\frac{t_{MDAC}}{\tau_{amp}}} - e^{-t_{MDAC}[\frac{1}{\tau_{DAC}}+\frac{1}{\tau_{amp}}]}). \end{aligned} \tag{4.13}$$

Since the first term in Eq. 4.13 indicates the ideal residue voltage, the input-referred error is

$$E = \pm\frac{1}{A_{res}^{N-1}}\frac{V_{ref}}{4}(e^{-\frac{t_{MDAC}}{\tau_{DAC}}} + e^{-\frac{t_{MDAC}}{\tau_{amp}}} - e^{-t_{MDAC}[\frac{1}{\tau_{DAC}}+\frac{1}{\tau_{amp}}]}). \tag{4.14}$$

Eq. 4.14 presents the general relation between the residue error due to the sub-ADC comparator metastability and the available time for the MDAC, t_{MDAC} without any assumption on the level of the input voltage. For example, for the input volatge levels smaller than ε_1, t_{MDAC} is zero and Eq. 4.14 reduces to $\pm\frac{1}{A_{res}^{N-1}}\frac{V_{ref}}{4}$ which was obtained previously by Eq. 4.10.

Recall from Eq. 4.15 than in all the above equations, t_{MDAC} is

$$t_{MDAC} = T_{conv} - \tau_{lat} \ln(\frac{V_{ON}}{A_o|V_{in} - V_{Th}|}). \tag{4.15}$$

For the input voltage levels in the second metastability region defined by ε_2 in Fig. 4.8, we can rewrite Eq. 4.14 by substituting t_{MDAC} from Eq. 4.15 to obtain the relation between the error and the input as following

$$\begin{aligned} E = \pm\tfrac{1}{A_{res}^{N-1}}\tfrac{V_{ref}}{4} \quad & ([e^{-T_{conv}}(\tfrac{V_{ON}}{A_o|V_{in}-V_{Th}|})^{\tau_{lat}}]^{\frac{1}{\tau_{DAC}}} \\ & +[e^{-T_{conv}}(\tfrac{V_{ON}}{A_o|V_{in}-V_{Th}|})^{\tau_{lat}}]^{\frac{1}{\tau_{amp}}} \\ & -[e^{-T_{conv}}(\tfrac{V_{ON}}{A_o|V_{in}-V_{Th}|})^{\tau_{lat}}]^{\frac{1}{\tau_{amp}}+\frac{1}{\tau_{amp}}}). \end{aligned} \tag{4.16}$$

To analyze Eq. 4.16, one should note that the value of the term inside the brackets is always equal or less than 1,[2] i.e.

$$0 < e^{-T_{conv}}(\frac{V_{ON}}{A_o|V_{in} - V_{Th}|})^{\tau_{lat}} \leq 1. \tag{4.17}$$

Thus, the error exponentially falls with smaller DAC and op amp time constants. In addition, shorter latch time constant, τ_{lat} reduces the value of the term inside the brackets exponentially, leading to a smaller residue error. It is worth noticing that the upper bound in nonequality 4.17 correspond to the maximum error, i.e. region ε_1, while the lower bound determines ε_3 in Fig. 4.8, where the residue error due to the sub-ADC comparator metastability is close to zero.

In a typical pipelined stage, the time constant of the DAC is much smaller than that of the op amp, i.e. $\tau_{DAC} << \tau_{amp}$. Therefore, Eq. 4.16 reduces to

$$E = \pm\frac{1}{A_{res}^{N-1}}\frac{V_{ref}}{4}e^{-T_{conv}}(\frac{V_{ON}}{A_o|V_{in} - V_{Th}|})^{\frac{\tau_{lat}}{\tau_{amp}}}. \tag{4.18}$$

Eq. 4.18 also gives the magnitude of error for the case when the DAC settling is complete and the op amp incomplete settling is the only source of error.

[2]This constrain results from the fact that $t_{MDAC} \geq 0$ and by using Eq. 4.15.

4.4.3 Inconsistency Between Sub-ADC Outputs to the MDAC and Decoder

As shown in Fig. 4.9 (a), the sub-ADC comparators outputs drive two different blocks: the decoder in the digital error correction (DEC) and alignment block and the MDAC. Therefore, the output path of the sub-ADC has to split into two paths: one path drives the gates of DAC swicthes and the other path drives logic gates or swicth gates of the decoder,depending on the decoder type.

If the sub-ADC comparator is metastable, its differential outputs stay very close to each other for a long time. Hence, the two receivers may interpret the sub-ADC output in different ways, due to the offset between the gate thresholds and noise, resulting in large errors. This effect is illustrated in Fig. 4.9, where for an input voltage level close to $\frac{V_{FS}}{4}$, the MDAC and the decoder receive codes 3 and 2, respectively leading to an input-referred error of $\frac{V_{FS}}{4}$. In a well-designed ADC, the two paths must match adequately [3] so then such error happens only when the comparator is in deep metastable condition, i.e. in regions ε_1. In this case, no matter what the digital output of the stage is, the input-referred error is estimated by Eq. 4.10.

4.4.4 Summary of the Error Due to the Sub-ADC Metastability

Fig. 4.10 plots the residue error due to the sub-ADC metastable comparator against input voltage in the three metastable regions, ε_1, ε_2, and ε_3. It should be noted that the conventional metastability analysis methods only calculate the metastability effect in the first region and do not address the second and third regions [1]. However, the effects of the second and third regions are not negligible

[3]For example, the sub-ADC output drives the MDAC switches and the ROM-based decoder switches simulators.

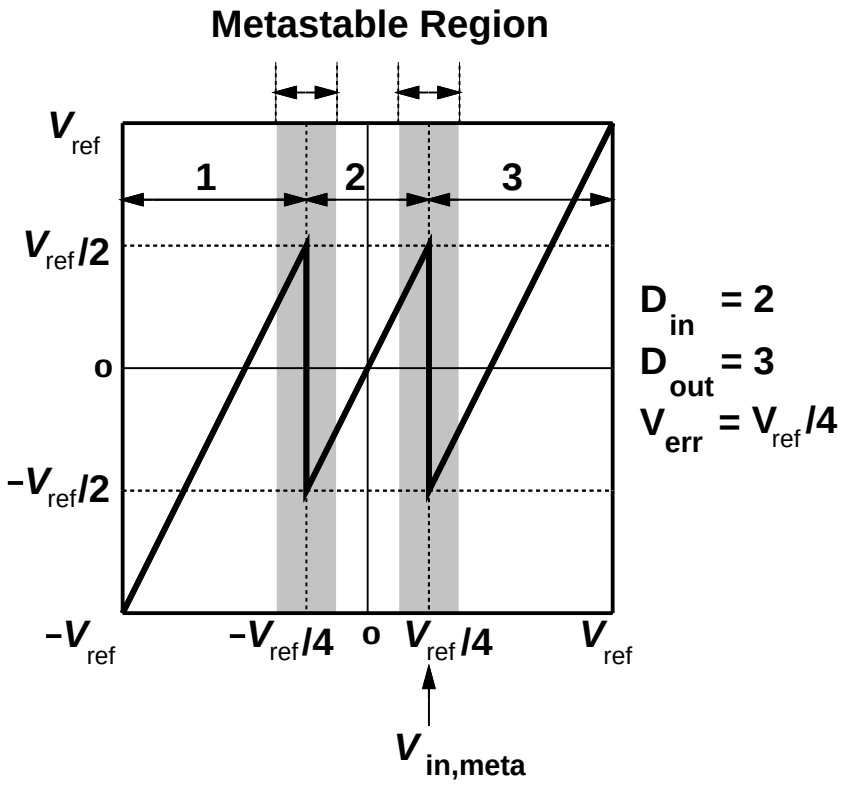


Figure 4.9: Inconsistency between sub-ADC outputs to the MDAC and decoder causes large ADC errors.

in most cases, because they happen for a wider range on input voltage levels and thus it is more probable to get an error due to the effects of these two regions rather than error due to the first mechanism.

To verify the proposed modeling of the residue error due to the sub-ADC comparator metastability, we simulate a 1-bit stage design in Cadence and compare the obtained residue error to the results from our model. Fig. 4.11 plots the residue error for input voltage levels close to zero in both cases: Cadence simulations, and calculation by the proposed model. The two cases show good agreement.

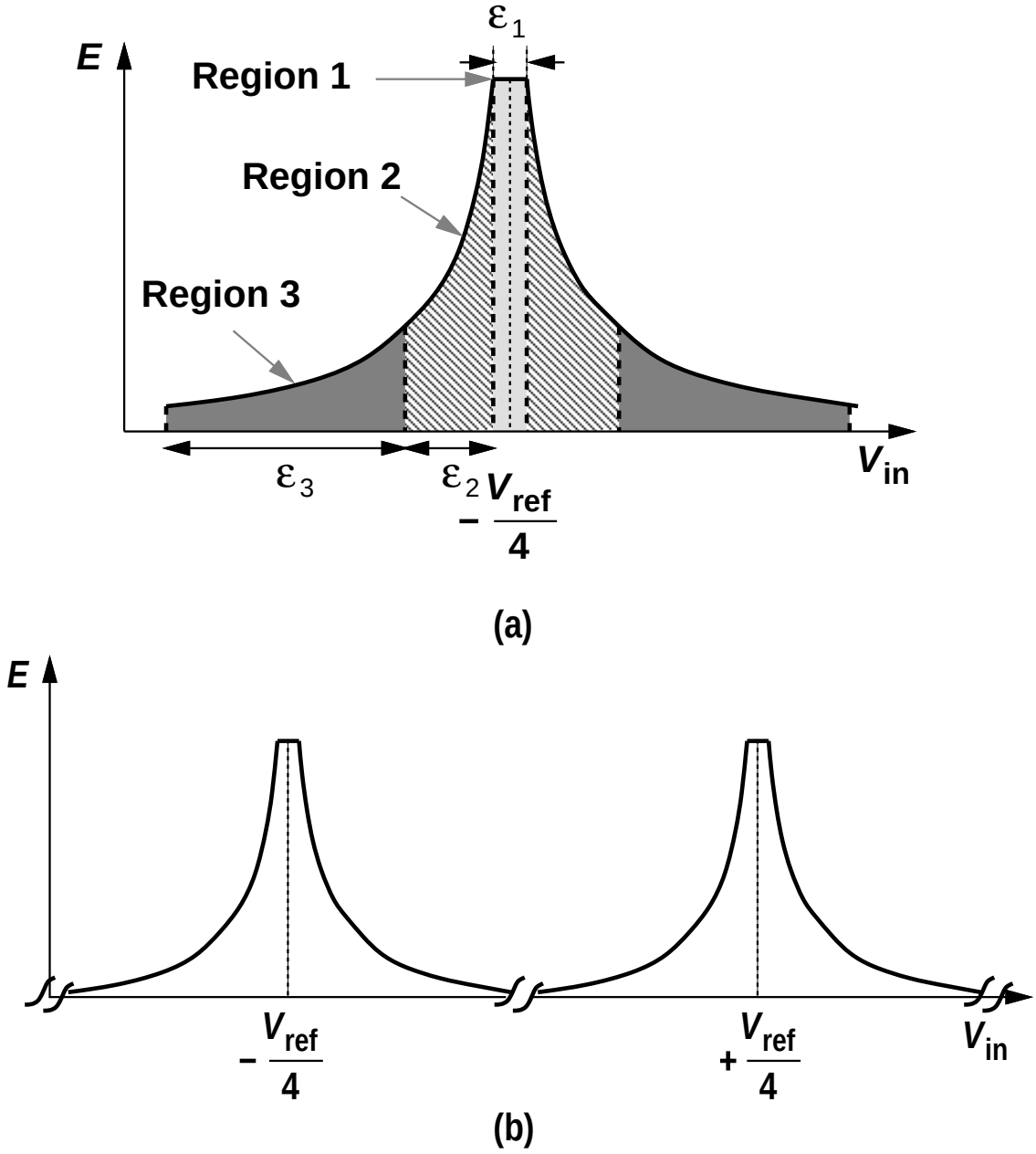


Figure 4.10: Input-referred stage error due to the sub-ADC comparator metastability shown for (a) a single threshold level and (b) a 1.5-bit stage.

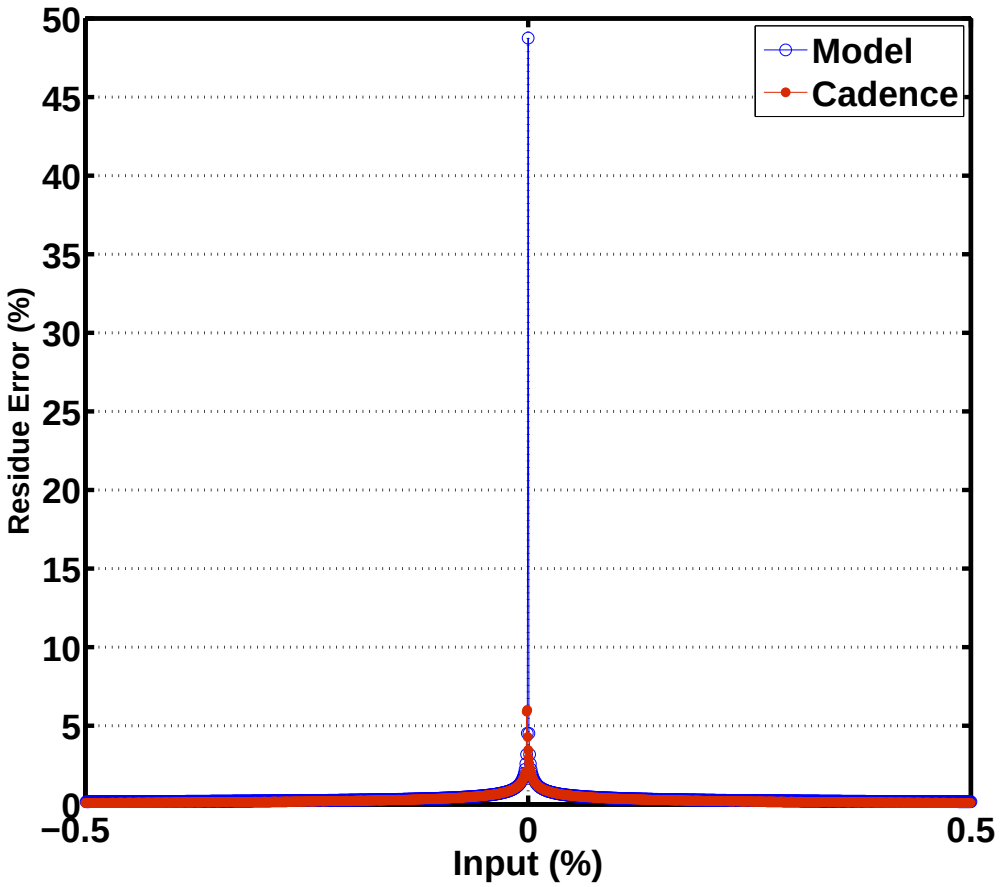


Figure 4.11: Comparison between the Cadence simulation results of a 1-bit pipelined stage and results of the proposed model.

4.5 Probability of Cumulative Error

Having the ADC error due to metastability known, we can derive all the error statistical characteristics for a given p.d.f of input signal. However, it is desired to obtain an error characteristic that can be related to the BER requirement of the system. Recall from Fig. 4.18, for input voltage levels that are at a distance of less than ε from a threshold voltage of the sub-ADC, the magnitude of the

residue error is greater than the amount of error at a voltage difference of ε. Therefore, for a sub-ADC threshold voltage of V_{Th}, we can write

$$if \;\; |V_{in} - V_{Th}| < \varepsilon \;\; then \;\; E > E(\varepsilon), \tag{4.19}$$

which means, the probability of getting an error greater than $E(\varepsilon)$, is equal to the probability of receiving an input voltage level in the range of $|V_{in} - V_{Th}| < \varepsilon$. Thus, letting $E(\varepsilon) = err$, we can write

$$P_{E>err} \;=\; prob\{|V_{in} - V_{Th}| < \varepsilon\}, \tag{4.20}$$

where, since $\varepsilon << V_{ref}$, the quantity on the right can be approximated as

$$P_{E>err} \;=\; prob\{|V_{in} - V_{Th}| < \varepsilon\} \;\approx\; 2\varepsilon f_{in}(V_{Th}), \tag{4.21}$$

where f_{in} is the p.d.f of the input signal. Note that Eq. 4.21 gives the probability of error due to the metastability effect around V_{Th}, or equivalently, due to the metastability of the sub-ADC comparator that compares the input with the threshold level V_{Th}. To obtain the total probability of error due to the sub-ADC comparators, we need to sum the probability of error due to each comparator. For example, for a 1.5-bit pipelined stage

$$P_{E>err} \;=\; 2\varepsilon[f_{in}(\frac{V_{ref}}{4}) + f_{in}(-\frac{V_{ref}}{4})]. \tag{4.22}$$

It is worth noticing that the quantity on the left side of Eq. 4.19 indicates the probability of accumulated error and hence, $P_{E>err}$ determines the rate with which, the ADC generates a metastability-induced error of greater than err. This rate is then can be used to determine the BER or the mean time to failure (MTF) of a system.

To obtain a more useful characteristic, it is desired to express the probability of error versus the magnitude of error. Thus, using Eq. 4.18, we obtain

$$\varepsilon = \frac{V_{ON}}{A_o} e^{-\frac{T_{conv}}{\tau_{lat}}} \left(\frac{err}{V_{ref}/(4A_{res}^{N-1})}\right)^{-\frac{\tau_{amp}}{\tau_{lat}}}. \tag{4.23}$$

Recalling that the maximum amount of error happens due to the first error mechanism and is given by

$$err_{max} = \frac{1}{A_{res}^{N-1}} \frac{V_{ref}}{4}, \tag{4.24}$$

and using the edge of the first region, ε_1, we can rewrite Eq. 4.23 as

$$\varepsilon = \varepsilon_1 \left(\frac{err}{err_{max}}\right)^{-\frac{\tau_{amp}}{\tau_{lat}}}. \tag{4.25}$$

Therefore, by substituting ε in Eq. 4.21 with its value from Eq. 4.25, we obtain

$$P_{E>err} \;=\; 2\varepsilon_1 \left(\frac{err}{err_{max}}\right)^{-\frac{\tau_{amp}}{\tau_{lat}}} f_{in}(V_{Th}), \tag{4.26}$$

that expresses the probability of getting a metastability-induced error greater than *err* in terms of the amount of error. As an example and using the proposed model, we calculate the probability of cumulative error for the one-bit pipelined stage introduced in Fig. 4.11. The results for different input signal distributions are shown in Fig. 4.12.

4.6 Overall Probability of Metastability in a Pipelined ADC

As illustrated in Fig. 4.8 and characterized by Eq. 4.16, due to the exponential growth of the residue voltage in the metastable regions 2 and 3, metastability in the subsequent stages has much lower probability when the first stage is metastable. Therefore, to calculate the overall ADC error in a pipelined system,

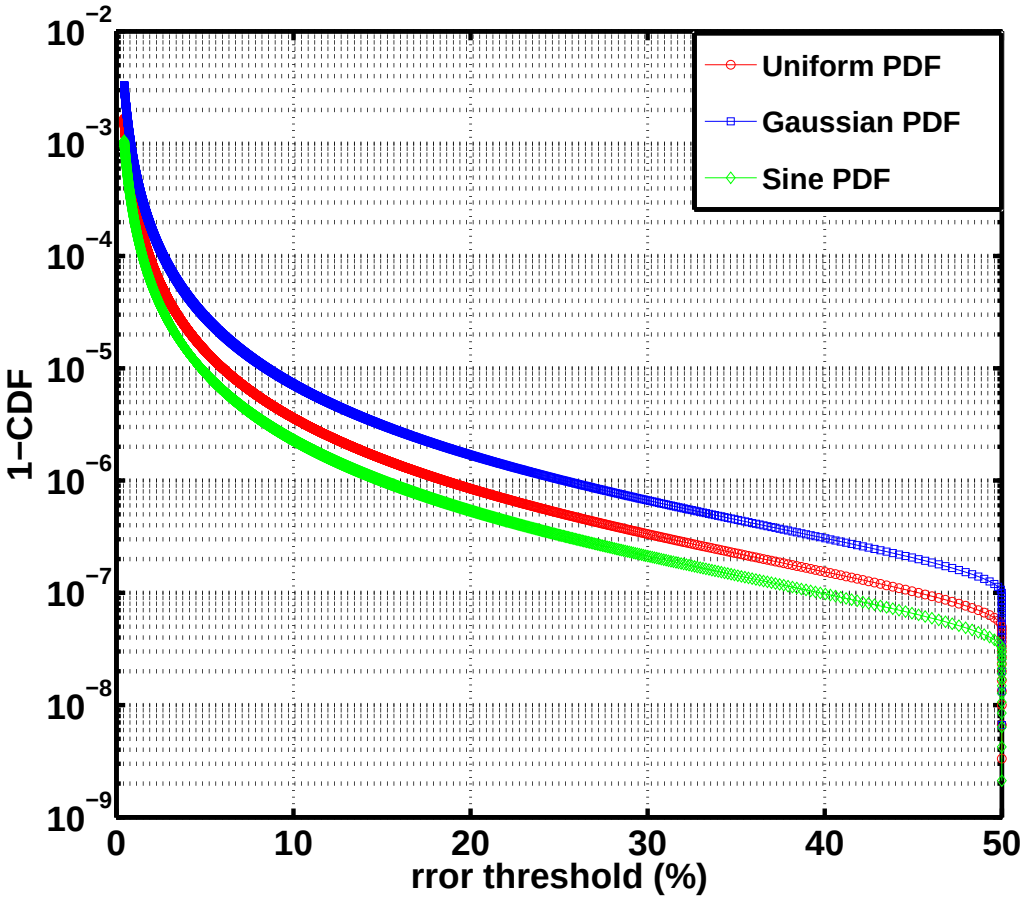


Figure 4.12: Probability of the cumulative error versus magnitude of error for a 1-bit stage.

we add the residue error of all stages, as illustrated in Fig. 4.13. It should be noted that the front stages result in larger ADC error due to the sub-ADC comparator metastability, whereas the stages at the back lead to smaller errors. On the other hand, the metastability happens for a larger number of threshold levels in the back-end stages. However, we show in the following that the probability of metastability reduces exponentially along the pipe.

The probability of an ADC metastability error greater than *err* for the overall

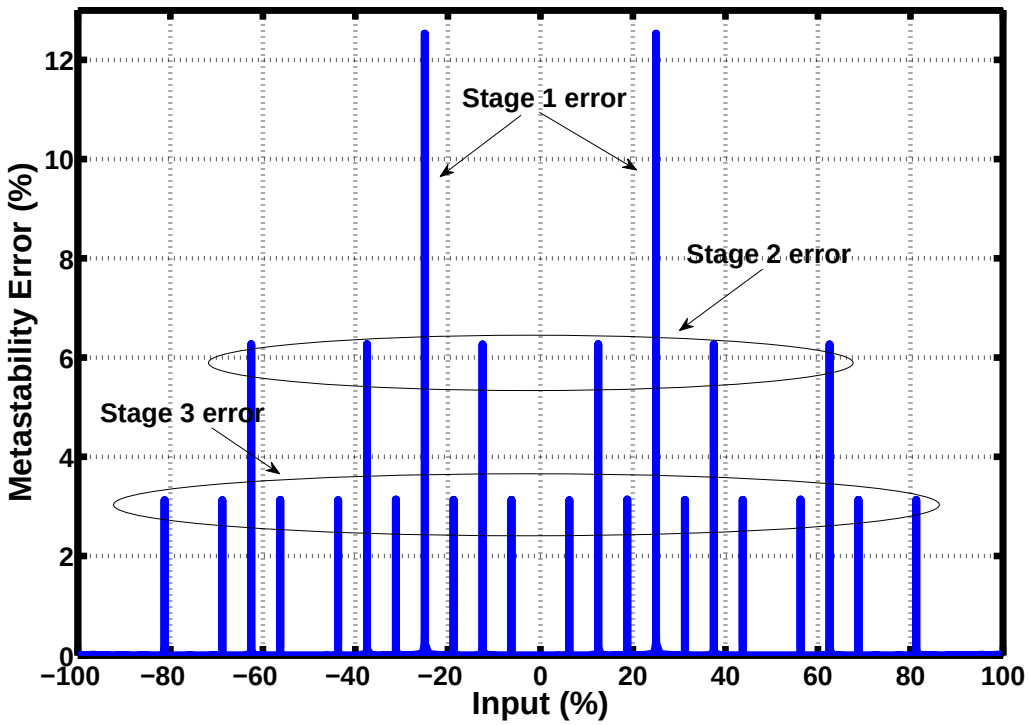


Figure 4.13: ADC error due to the sub-ADC comparator metastability of the first three 1.5-bit stages.

pipelined architecture can be written as

$$P_{E>err} = \sum_{i=1}^{n} 2\varepsilon f_{in}(V_{Th,i}), \tag{4.27}$$

where n is the total number of thresholds of all the stages and ε is the metastability region around each threshold level. Recall, for threshold voltages due to the sub-ADC comparators of stage N

$$\varepsilon_{i,N} = \varepsilon_1 (\frac{err}{err_{max}/2^{N-1}})^{-\frac{\tau_{amp}}{\tau_{lat}}}. \tag{4.28}$$

Thefore, we rewire Eq. 4.27 as

$$P_{E>err} = \sum_{N=1}^{N_{ADC}} [2\varepsilon_1 (2^{N-1}\frac{err}{err_{max}})^{-\frac{\tau_{amp}}{\tau_{lat}}} \sum_{k=1}^{2^N-1} f_{in}(\pm\frac{(2k-1)V_{ref}}{2^{N+1}})]. \tag{4.29}$$

N_{ADC} in Eq. 4.29 denotes the number of stages in the pipelined ADC. To examine the effect of back-end stages on the overall ADC probability, let's assume the simple case of uniformly distributed input with a p.d.f of $\frac{1}{2V_{ref}}$. Then, Eq. 4.29 turns to

$$P_{E>err} \;=\; 2\varepsilon_1(\frac{err}{2err_{max}})^{-\frac{\tau_{amp}}{\tau_{lat}}}\frac{1}{V_{ref}}\sum_{N=1}^{N_{ADC}}[(2^{-N\frac{\tau_{amp}}{\tau_{lat}}}(2^N-1)], \tag{4.30}$$

which means the contribution of stage N is approximately proportional to $2^{N(1-\frac{\tau_{amp}}{\tau_{lat}})}$. Since in most cases, $\tau_{amp} > \tau_{lat}$, Eq. 4.30 shows that the effect of pipelined stage metastability on the overall ADC metastability rate reduces exponentially with N.

4.7 Metastability Analysis of a multi-bit Stage

Similar approach we used for a 1.5-bit stage can be applied to a multi-bit stage with a resolution of M bits. Thus, magnitude of the error due to the stage sub-ADC metastability is given by

$$E = \pm\frac{V_{ref}}{2^M}(e^{-\frac{t_{MDAC}}{\tau_{DAC}}} + e^{-\frac{t_{MDAC}}{\tau_{amp}}} - e^{-t_{MDAC}[\frac{1}{\tau_{DAC}}+\frac{1}{\tau_{amp}}]}). \tag{4.31}$$

Eq. 4.31 indicates that the maximum amount of error is equal to $\frac{V_{ref}}{2^M}$ and hence reduces exponentially with M. If we neglect the DAC settling error, it can be shown that the probability of the metastability for an M-bit stage is

$$P_{E>err} \;=\; 2\varepsilon_1(2^M\frac{err}{V_{ref}})^{-\frac{\tau_{amp}}{\tau_{lat}}}\sum_{k=-(2^{M-1}-1)}^{k=(2^{M-1}-1)} f_{in}(\frac{kV_{ref}}{2^M}). \tag{4.32}$$

For a uniform input with a p.d.f of $\frac{1}{2V_{ref}}$, by using Eq. 4.32 we obtain

$$P_{E>err} \;\approx\; \frac{\varepsilon_1}{V_{ref}}(\frac{err}{V_{ref}})^{-\frac{\tau_{amp}}{\tau_{lat}}}\;2^{M(1-\frac{\tau_{amp}}{\tau_{lat}})}, \tag{4.33}$$

which shows an exponentially reducing behavior with higher stage resolutions. Therefore, the use of multi-bit stages, particularly in the front end, is beneficial to reduce the metastability effect in a pipelined ADC.

4.8 Measurements

To verify the proposed metastability analysis, we measure the metastability rate of the pipelined ADC introduced in Chapter 2. The measurement setup is shown in Fig. 4.14 where a sinusoidal input is applied at the input of the ADC. If, as

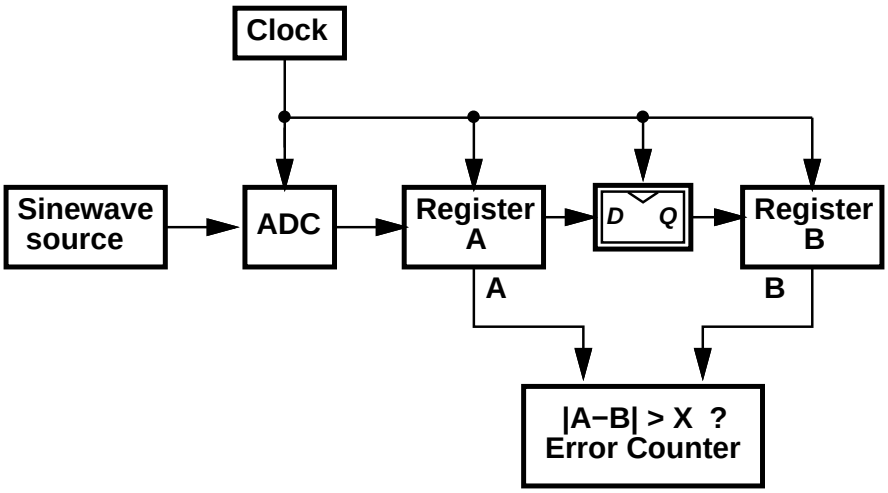


Figure 4.14: Setup of the metastability measurement.

depicted in Fig. 4.15, the input frequency is chosen such that, the analog change between every two successive samples is less than 1 LSB, i.e.

$$f_{in} < \frac{f_s}{2^N \pi}, \tag{4.34}$$

then by comparing the difference between every two successive ADC outputs, we can detect an irregular error. Thus, the ADC output is collected and stored in register A while the delayed output is stored in register B. Therefore, by

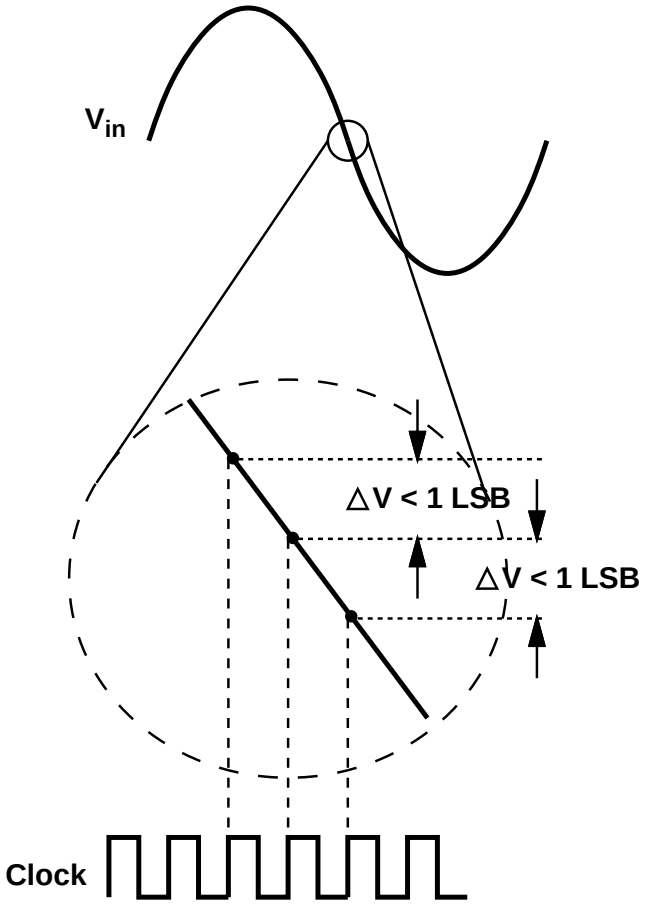


Figure 4.15: To measure the metastability, input frequency is chosen such that every two successive samples have an analog difference of less than 1 LSB.

comparing the values of register A with those of register B, we can obtain the number of erroneous outputs versus the amount of error, indicated as X in Fig. 4.15. It should be noted that the ADC is expected to produce small errors due to different error sources like quantization noise, thermal noise, and nonlinearity. However, such errors are small and have magnitudes of less than few LSB. But large errors that have magnitudes of greater than several LSB are counted as metastability errors, since it is the only mechanism that can result in such large amounts.

Fig. 4.16 plots the measurement result together with the result derived from the proposed model, for the pipelined ADC introduced in Chapter 2, while operating with a 600-MHz clock frequency. The metastability rate is measured versus the magnitude of metastability error, by collecting about 10^{10} samples in 20 days. The comparison shows an error shift of 0.4% that originates from different sources such as thermal noise, nonlinearity, and setup error, that are not included in the analysis. However, the measurement results concur with the analysis in showing the trend of the error rate versus the error quantity. In addition, to measure the probability of larger metastability error, more samples must be collected that would take quite long time and hence, is not practical. In fact, such a costly experiment proves the vitality of the proposed analysis in the design phase.

4.9 Conclusion

Metastability is a problem associated with any latch-based comparator, which is the main building block of a typical ADC. While studied for only flash converters, the effect of comparator metastability is far more complex in a pipelined ADC. In this chapter, a comprehensive analysis of the metastability effects in a pipelined environment is presented. Different error mechanisms in a pipelined stage are identified. Using the proposed models, the metastability error is formulated and the probability of the cumulative error versus the magnitude of error is extracted. In addition, it has been shown that, both the maximum magnitude of error and the probability of error fall exponentially with higher resolutions of the stage, suggesting that using multi-bit stages at the front end improves the metastability significantly.

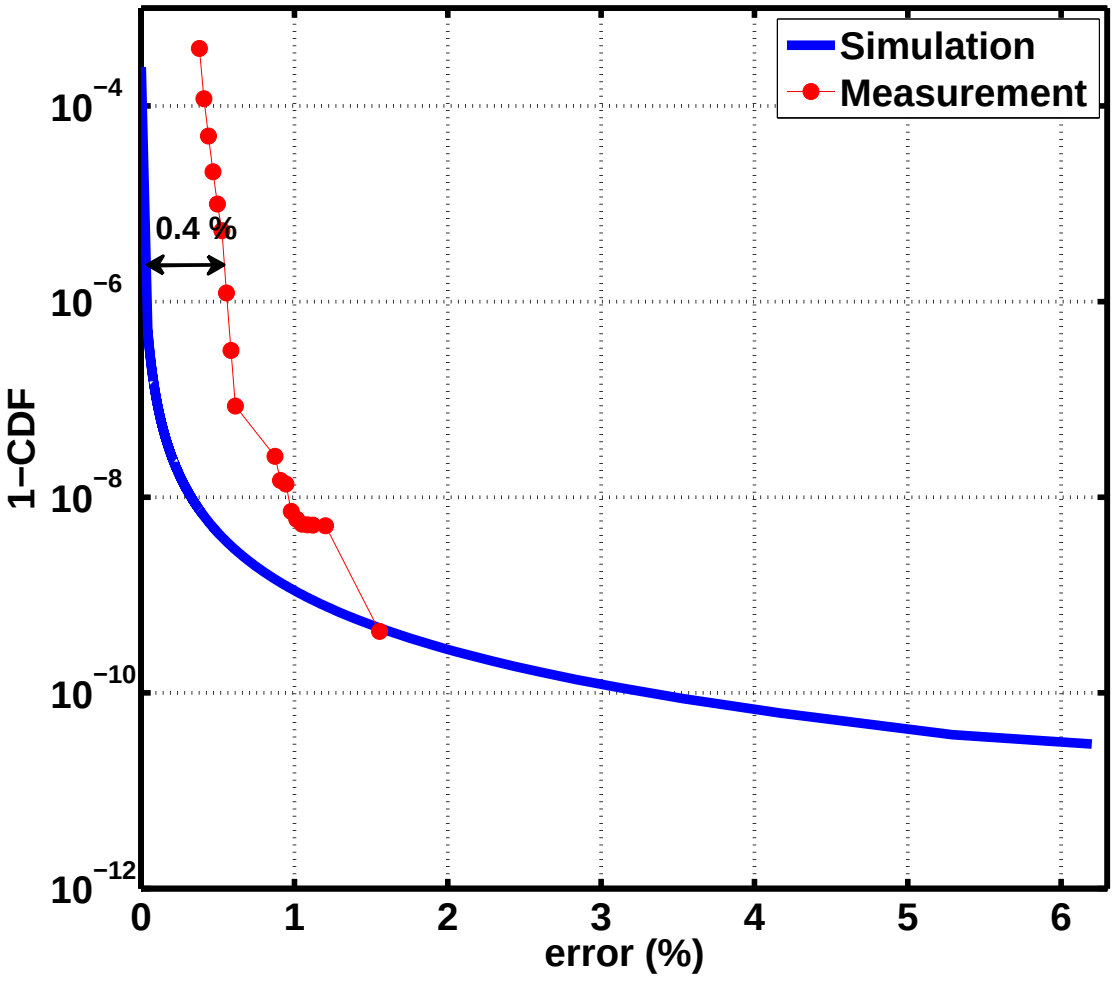


Figure 4.16: Comparison between measurement and analysis results.

CHAPTER 5

Conclusion and Future Work

It is desirable to architect the ADC such that it avoids the op amp nonlinearity, in particular with reduced intrinsic gain of transistors in modern technologies. In this research, we demonstrated that the pipelined ADCs can greatly benefit from a multi-bit front end that incorporates a precharged resistor-ladder DAC. Due to the reduced signal swing, the nonlinearity is avoided and the op amp is realized as a simple differential pair with resistive loads, perhaps the fastest amplifier one can build without using an inductance. In addition, relying on a highly-linear resistor ladder, the required calibration is simplified and reduced to only gain error correction. The low-voltage architecture in conjunction with a high-speed high-precision resistor-ladder DAC enables calibrating at high clock rates. Thus, the calibration scheme can also capture and correct the dynamic gain errors due to the op amp limited settling. The 10-bit ADC prototype is fabricated in 65-nm CMOS technology and achieves an FOM of 70 fJ/conv.-step at a sampling rate of 1 GHz.

Although it has been shown that it is beneficial to resolve more bits in the first stage of the pipe, we stopped at 4 bits, mainly due to the sub-ADC comparator offsets. However, by using a simple offset correction algorithm, the comparator offsets are reduced and higher resolutions can be used, leading to a faster resistor-ladder DAC. Moreover, the required redundancy to cover for the comparator offset becomes smaller, resulting in more power saving. Another aspect that can

be improved is the signal swing that is limited to $\pm\frac{V_{DD}}{2}$ by the sub-ADC input sampling networks. Using a two-step coarse conversion, this limit is avoided resulting in a rail-to-rail ADC operation that significantly improves the power efficiency by enhancing the dynamic range.

A critical issue in the design of high-speed ADCs relates to the errors that result from comparator metastability. Studied for only flash architectures, this phenomenon assumes new dimensions in pipelined converters, creating far more complex error mechanisms. In this dissertation, we presented a comprehensive analysis of comparator metastability effects in pipelined ADCs and develop a method to precisely predict the error behavior for a given input signal p.d.f. Different error mechanisms in a pipelined stage are identified. Using the proposed models, the metastability error is formulated and the probability of the cumulative error versus the magnitude of error is extracted. In addition, it has been shown that, both the maximum magnitude of error and the probability of error fall exponentially with higher resolutions of the stage, suggesting that using multi-bit stages at the front end improves the metastability significantly.

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