UNIVERSITY OF CALIFORNIA SAN DIEGO

28 GHz Phased-Array Transceivers for 5G Communications

A dissertation submitted in partial satisfaction of the
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in

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by

Kerim Kibaroglu

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor Peter M. Asbeck
Professor Gert Cauwenberghs
Professor William S. Hodgkiss
Professor Daniel F. Sievenpiper

2018

The dissertation of Kerim Kibaroglu is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

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DEDICATION

To my parents

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Chapter 2, in full, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer and G. M. Rebeiz, "A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a 2x2 Beamformer Flip-Chip Unit Cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260-1274, May 2018. The dissertation author was the primary investigator and author of this paper.

Chapter 3, in part, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer and G. M. Rebeiz,"A 28 GHz Transceiver Chip for 5G Beamforming Data Links in SiGe BiCMOS," *IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM)*, October 2017. The dissertation author was the primary investigator and author of this paper.

Chapter 4, in full, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer, T. Phelps and G. M. Rebeiz, "A 64-Element 28-GHz Phased-Array Transceiver With 52 dBm EIRP and 8-12 Gb/s 5G Link at 300 Meters Without Any Calibration," *IEEE Transactions on Microwave Theory and Techniques*, 2018. The dissertation author was the primary investigator and author of this paper.

Chapter 5, in part, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer, A. Nafe and G. M. Rebeiz, "A Dual-Polarized Dual-Beam 28 GHz Beamformer Chip Demonstrating a 24 Gbps 64-QAM 2x2 MIMO Link," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2018. The dissertation author was the primary investigator and author of this paper.

VITA

2013	B. S. in Electronics Engineering, Sabanci University, Istanbul, Turkey
2015	M. S. in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego, La Jolla, CA
2018	Ph. D. in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego, La Jolla, CA

PUBLICATIONS

K. Kibaroglu, M. Sayginer, T. Phelps and G. M. Rebeiz, "A 64-Element 28-GHz Phased-Array Transceiver With 52 dBm EIRP and 8-12 Gb/s 5G Link at 300 Meters Without Any Calibration," *IEEE Transactions on Microwave Theory and Techniques*, 2018.

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B. Ustundag, K. Kibaroglu, M. Sayginer and G. M. Rebeiz, "A Wideband High-Power Multi-Standard 23-31 GHz 2x2 Quad Beamformer Chip in SiGe with $>$ 15 dBm OP1dB Per Channel," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2018.

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K. Kibaroglu, M. Sayginer and G. M. Rebeiz, "A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a 2x2 Beamformer Flip-Chip Unit Cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260-1274, May 2018.

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K. Kibaroglu, M. Sayginer and G. M. Rebeiz, "A Quad-Core 28-32 GHz Transmit/Receive 5G Phased-Array IC with Flip-Chip Packaging in SiGe BiCMOS," *IEEE International Microwave Symposium (IMS)*, June 2017.

K. Kibaroglu and G. M. Rebeiz, "An N-Path Bandpass Filter with a Tuning Range of 0.1-12 GHz and Stopband Rejection $>$ 20 dB in 32 nm SOI CMOS," *IEEE International Microwave Symposium (IMS)*, May 2016.

ABSTRACT OF THE DISSERTATION

28 GHz Phased-Array Transceivers for 5G Communications

by

Kerim Kibaroglu

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

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Professor Gabriel M. Rebeiz, Chair

The fifth-generation (5G) communication links promise a revolution in mobile communications with data rates on the order of 1-10 Gbps by utilizing the available bandwidth at mm-wave bands such as 28, 39 and 60 GHz. To overcome the increased path loss at mm-wave bands, the next generation communication links will rely on directive communications, enabled by phased-array techniques, and can result in lower power consumption compared to sub-6 GHz links due to the array antenna gain. While phased-arrays have been used for many years for defense applications and satellite communications, their cost needs to be significantly lowered for massive use in 5G applications. This requires the use of highly integrated chips based on silicon technologies (SiGe or CMOS), low-cost PCB designs and a great reduction in testing costs

by eliminating array calibration. A scalable, low-cost phased-array capable of scanning in both azimuth and elevation at mm-wave frequencies is needed to deliver Gbps data to several users at a link distance on the order of hundreds of meters. This dissertation presents circuits, system architectures, phased-array design and measurement techniques to achieve $>$10 Gbps data rates at link distances of up to 300 meters without any calibration for 28 GHz 5G communications.

Chapter 1

Introduction

1.1 Phased-Array Systems for 5G Communications

The fifth-generation (5G) communication links promise a revolution in mobile communications with data rates on the order of 1-10 Gbps by utilizing the available bandwidth at mm-wave bands such as 28, 39 and 60 GHz. To overcome the increased path loss at mm-wave bands, the next generation communication links will rely on directive communications, enabled by phased-array techniques, and can result in lower power consumption compared to sub-6 GHz links due to the array antenna gain [1–3]. While phased-arrays have been used for many years for defense applications and satellite communications, their cost needs to be significantly lowered for massive use in 5G applications. This requires the use of highly integrated chips based on silicon technologies (SiGe or CMOS) rather than GaAs or InP based modules [4–12], low-cost PCB designs and a great reduction in testing costs by eliminating array calibration. A scalable, low-cost phased-array capable of scanning in both azimuth and elevation at mm-wave frequencies is needed to deliver Gbps data to several users at a link distance on the order of hundreds of meters.

Recently, there have been several demonstrations of phased-array based data links in the mm-wave bands [4–7]. All of these phased-arrays rely on an all-RF beamforming architecture

for reduced power consumption due to the elimination of a mixer for each channel (for LO or IF beamforming), reduced complexity by eliminating the LO distribution network to several chips in a large array, and the ability to cancel any out-of-beam interferer before the mixer (at the sum point) resulting in higher dynamic range [13, 14]. The antennas can be placed on-chip [4] or integrated on the PCB [5–8], and the beamformer core chip may include the RF front-end only [4] or, for a large number of channels on-chip, include the up/down conversion mixers and synthesizers in addition to the RF front-end [5–8].

To achieve Gbps links at 28 GHz using 2D phased-arrays, the most efficient solution is to combine a multitude of 4-element transmit/receive chips which are assembled on the top PCB layer with an antenna array on the bottom side. This scalable all-RF architecture minimizes the line losses from the chip bumps to the antenna feeds on the PCB to improve both the receiver NF as well as the transmitter output power resulting in increased link distance at the same aperture size and power consumption. This architecture also allows the symmetric design of the 2x2 beamformer chips as well as the array PCB to operate without any calibration for further cost reduction.

1.2 Thesis Overview

The thesis presents circuits, system architectures, phased-array design and measurement techniques to achieve Gbps 5G links at 28 GHz at distances of hundreds of meters.

Chapter 2 presents the low-cost, scalable phased-array architecture based on 2x2 transmit/receive beamformer chips. Circuit design techniques are developed to results in a state-of-the-art 28 GHz beamformer chip in SiGe with flip-chip packaging. A 32-element array is built using 8 of these chips on an ultra-low cost PCB consisting of only 4 RF layers and a 300 m data link is demonstrated achieving a state-of-the-art data rate of 1.0-1.6 Gbps over all scan angles.

Chapter 3 presents a 28 GHz transceiver chip for up/down conversion to an IF of 2-6 GHz to be placed at the common port of the 5G phased-array. System requirements are analyzed and

an asymmetric chip architecture is developed to result in high-linearity in the RX mode and high single-sideband rejection in the TX mode to meet the requirements of a 16-64 element phased-array link.

Chapter 4 presents a 64-element phased-array transceiver based on the 2x2 quad architecture using a 12-layer PCB with wideband stacked patch antennas. Detailed pattern, effective isotropic radiated power, and link measurements performed without any array calibration are presented and show the robustness of the symmetrical design technique. A 300 m wireless link is demonstrated with a record-setting data rate of 8–12 Gbps over all scan angles using two 64-element TRX arrays and 16-/64-QAM waveforms in a single beam.

Chapter 5 presents a 2x4 element transmit/receive beamformer chip and its use in a polarization based 2x2 MIMO link for further increased capacity. A wireless link is demonstrated using two phased-array boards operating with two independent data streams simultaneously. A data rate of 12 Gbps per polarization (24 Gbps total data rate) is achieved using 64-QAM and 16 Gbps per polarization (32 Gbps total data rate) using 16-QAM waveforms. This work presents the first demonstration of a single-aperture 2x2 polarization MIMO link at millimeter-waves.

The thesis concludes with a summary of the presented work and suggestions for future research.

Chapter 2

32-Element (4×8) Phased-Arrays

2.1 Introduction

This chapter presents a 32-element (4x8) 28 GHz phased-array transceiver for 5G communications based on 2x2 beamformer core chips. Section 2.2 presents the scalable phased-array architecture and Section 2.3 presents system analysis for a 32-element array. Circuit blocks and breakout measurements are presented in Section 2.4. Section 2.5 presents the system measurements of 2x2 and 4x8 arrays and Section 2.6 concludes the chapter.

2.2 5G Phased-Array Transceiver Architecture

The scalable 28 GHz phased-array architecture employed in this work is shown on Fig. 4.1 and is based on 2x2 TRX beamformer chips which are flipped on one side of a PCB with the antennas placed on the other side. Each chip contains four TRX channels with phase and gain control implemented using an all-RF beamforming architecture. Since the core chip contains only four elements, a separate transceiver chip is designed for up/down conversion to an IF (or baseband) signal, and can be placed every 16, 32 or 64 elements depending on the system requirements.

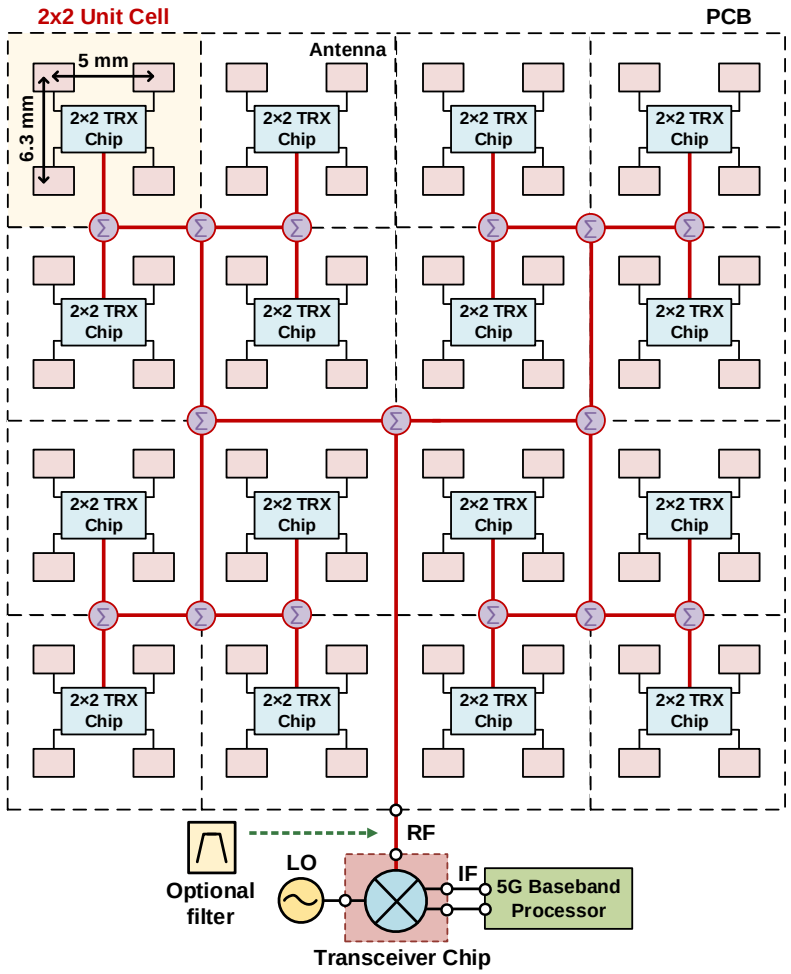


Figure 2.1: Scalable NxN 5G phased-array architecture based on a 2x2 beamformer unit cell.

Compared to previous work which have relied on a large number of elements on a single chip [5, 6, 8], this architecture offers significant advantages. First, the routing distance from the chip to the antenna feeds are minimized which greatly reduces the loss and improves both the system NF and the transmitted power, therefore allowing for a much longer link distance for the same aperture size and power consumption. For example, LG in [7] recently reported a feed line loss of 2 dB between the antenna and the chip while in this work, the equivalent loss is only 0.5 dB, resulting in 3 dB improvement in the system SNR. The feed lines to the antennas can also be designed to be of equal length which, when combined with the symmetric design of the Wilkinson network and the 2x2 TRX beamformer chips, can eliminate any phased-array

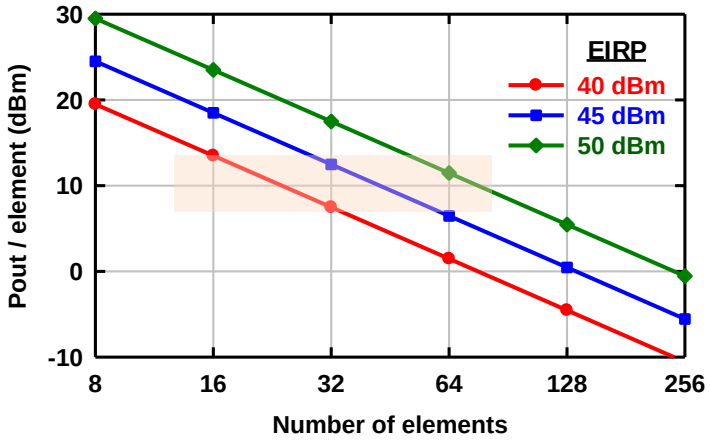


Figure 2.2: Required output power per element for different EIRP values vs. number of array elements.

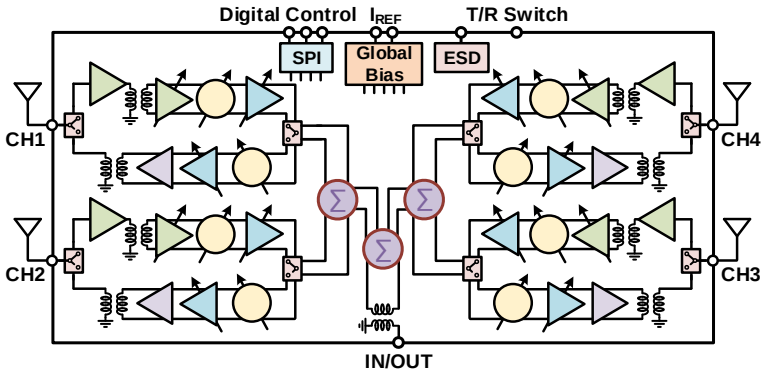


Figure 2.3: Block diagram of the 2x2 transmit/receive beamformer core chip.

calibration for further cost reduction.

Second, the array can be scaled to any size while maintaining symmetry. An example 64-element (8x8) array is shown in Fig. 4.1 with a transceiver chip placed at the common port after the Wilkinson combiner/divider network on the PCB. Base-stations are likely going to require 64 to 256+ elements to meet the EIRP requirements for increased coverage, while end-user equipment may only require 16-32 elements. This architecture allows both to be implemented using the same silicon beamformer RFIC. Note that a single-chip solution with an integrated transceiver (e.g. [8]) may be preferable for cell phones due to its reduced form factor if 8-16 elements are required.

Third, the scalable array architecture results in a more robust design and uniform heat distribution over the aperture. If one of the core chips does not work or underperforms, this results in a loss of only 4 elements out of 32 to 256 elements and will have minimal impact on the system performance compared to the loss of a chip with 16 channels. This architecture also spreads out the heat, generated mostly by the power amplifiers (PA), over the aperture instead of confining it to a single large chip at the center of the array. This makes it significantly easier to cool the array resulting in a more robust performance.

Fourth, the 2x2 beamformer chips can be directly flipped on the PCB without a multi-layer laminate interposer due to the reduced number of I/O ports compared to a phased-array chip with larger number of elements. This also results in a lower cost PCB with a reduced number of layers since the routing complexity is minimal and there is no LO or IF distribution networks to several chips in the phased-array.

Finally, by separating the phased-array front-end chip and the transceiver chip, this architecture offers great flexibility. In this work, both chips have been designed in the TowerJazz SBC18H3 SiGe BiCMOS process [15], but this 2-chip solution allows for different IC processes to be used for the beamformer chip and the transceiver chip. For example, the RF beamformer can be designed in SiGe for increased output power, reliability and low-NF while the transceiver chip can be designed in highly-scaled CMOS and can incorporate the baseband functionality as well. Also, a multi-pole filter with a sharp rejection response can be placed before the transceiver chip, thereby greatly reducing the out-of-band interferers and eliminating any LO radiation (in IF-based architectures).

One disadvantage of this architecture is that the transceiver needs to compensate for the additional ohmic loss of the Wilkinson network and provide a high output power to drive the array. This can be alleviated in 256-element arrays by incorporating bi-directional line amplifiers every 64 or 128 elements on the PCB to compensate for the division and ohmic loss or by placing a transceiver every 64 elements with reduced output power levels. Simulations for 16-, 32- and 64-element arrays show that no additional line amplifiers are required (see Section 2.3, Fig.

Table 2.1: Comparison of 2x2 Quad Beamformer and Larger IC Design Approaches

IC Approach	**2x2 Quad (single or dual polarization) with separated transceiver(s)**	**16 Elements (single or dual polarization) with integrated transceiver(s)**
Interconnect between chips and antennas	Low complexity and short transmission-lines. Requires one RF layer.	High complexity and long transmission lines, especially for equal-length connections. Requires multiple RF layers.
Loss between chip and antennas	0.25-0.5 dB for equal-length connections	1.5-2 dB for equal-length connections
Single point failures in 8x8 phased-array	Affects 4 out of 64 elements.	Affects 16 out of 64 elements.
Phased-array PCB temperature	Distributed over 16 different ICs in the array. Results in uniform PCB temperature.	Concentrated in 4 ICs − hot spots on the PCB.
High-rejection / high-Q filter before the transceiver (mixer)	Easy to place on the PCB (4-6 pole filter with Q∼100 in stripline on PCB).	Impossible to place on the silicon chip.
Mix and match technologies between the front-end and transceiver for optimal performance	Easy to use two different technologies (e.g. SiGe for the 2x2 quad front-end and scaled CMOS nodes for the transceiver).	Impossible using a single silicon chip.
Design cycles for different designs	Fast and low cost: Easy to change 2x2 quad and respin due to low complexity and small chip size. Transceiver chip and 2x2 quad chip can be optimized separately in two different technologies.	Slow and high cost: Very large chips with integrated transceivers. Complex to change and costly due to chip size.
Assembly	Easy: Low-complexity 2x2 quad with low I/O count.	Hard: Very complex IC with large I/O count.
Overall yield	Very high: High yield per chip due to low 2x2 quad complexity and high assembly yield.	Low: Low yield due to large chip area and low assembly yield.
Delivery	Customers receive tested 2x2 quad chips with 50 Ω ports. Easy to verify performance (e.g. Pout, NF) and accept delivery.	Customers receive complex package with IC and antennas. Cannot be tested except using over-the-air (OTA) methods. Expensive to verify performance (e.g. EIRP, G/T).

2.5(a)).

While this chapter is based on 4-element beamformer chips to generate a single beam, the same architecture can be used to build a dual-polarized dual-beam TRX core chip which can generate two simultaneous beams for polarization-based MIMO systems. Each chip would

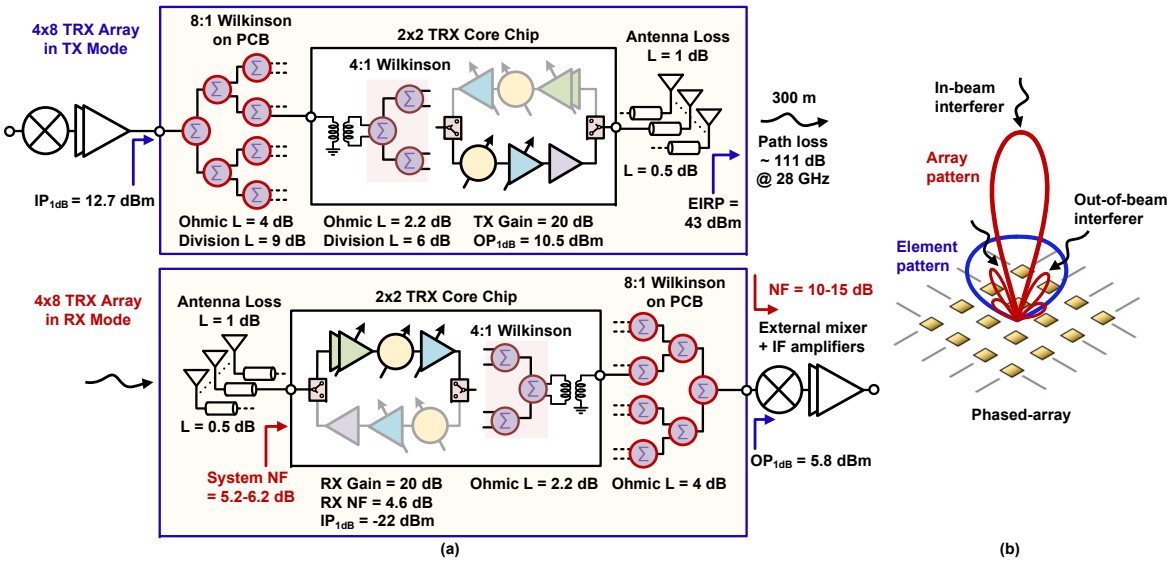


Figure 2.4: (a) System calculations for the 32-element TRX beamformer based on a 2x2 TRX beamformer core chip. (b) Interferer locations for the RX linearity calculations.

then include eight channels, four of which are combined together into two common ports for the vertical and horizontal polarizations. These chips would feed into dual-polarized antennas, and two RF beamformers on the PCB together with two transceivers at the sum points would be used. This dual-beam architecture still retains all the benefits of the scalable array architecture outlined above and summarized in Table 2.1.

2.3 32-Element Phased-Array System Analysis

This section presents the 2x2 phased-array beamformer core chip and system specifications along with the design flow. First, the array EIRP must be chosen and the output power required per element at P1dB (P_{out}) is determined based on the number of array elements. Given an EIRP, P_{out} is calculated using

$$P_{out} = EIRP - 10\log N - G_{ANT} + L_M \tag{2.1}$$

where N is the number of array elements, G_{ANT} is the (N-element) transmit/receive antenna gain assuming uniform distribution across the array and includes the antenna ohmic and mismatch

loss ($\sim$1 dB) and the feed line loss ($\sim$0.5 dB), L_{M} is the power loss due to any amplitude and phase mismatch between the elements ($\sim$0.5 dB). G_{ANT} is approximated using [16]

$$G_{ANT} = 10\log(\frac{4\pi N_x d_x N_y d_y}{\lambda^2}) - L_{ANT} \tag{2.2}$$

where λ is the wavelength in air, N_{x} and N_{y} are the number of array elements in the horizontal and vertical directions, d_{x} and d_{y} are the antenna spacings in the horizontal and vertical directions and L_{ANT} includes the antenna ohmic and mismatch loss, and feed line loss.

Fig. 2.2 presents the required P_{out} for different EIRP values and array sizes. In this work, we chose P_{out} to be around 10 dBm for low power consumption per chip and to mitigate the thermal issues discussed in Section 2.2. An EIRP of 43-49 dBm can be achieved with an array size of N = 32-64 (4x8 or 8x8 elements). This was calculated for a single-beam design in which the common ports of all 4-element chips are summed on the PCB.

The transmit chip gain of the 2x2 TRX core chip (Fig. 2.3) must then be chosen such that a transceiver chip at the sum point will be able to deliver enough power to operate the 32-element array at the P1dB level. This gain is defined as the output power per channel divided by the available power at the chip input, and includes the 6 dB on-chip Wilkinson division loss and the 2.2 dB on-chip Wilkinson, transmission-line and balun ohmic loss. For a TX channel gain of 20 dB (see Fig. 2.4(a) for channel definition) and an OP1dB of 10.5 dBm, the chip transmit gain is 11.8 dB and the required input P1dB for each 2x2 beamformer chip is -0.3 dBm. For a 32-element array and starting from the transceiver, the RF power is distributed using a PCB-based Wilkinson network to 8 beamformer chips (1:8) with a division loss of 9 dB and an ohmic network loss of 4 dB. The ohmic network loss is due to the PCB Wilkinson loss of 0.4 dB per stage, and a transmission-line loss of 0.5 dB/cm, all at 28 GHz. This results in a required transceiver output power of 12.7 dBm for a 32-element array.

Fig. 2.5(a) presents the required transceiver OP1dB for several array sizes and TX channel gains at a fixed OP1dB of 10.5 dBm per channel. A transceiver OP1dB of $\sim$18 dBm is required for a 64-element array due to the additional 5 dB loss arising from 3 dB more division

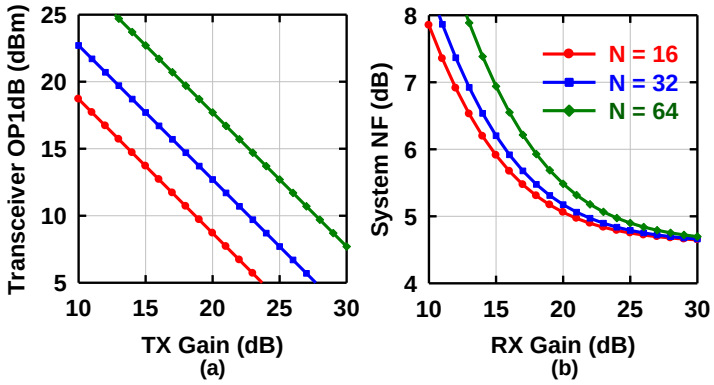


Figure 2.5: (a) OP1dB required from the transceiver chip to obtain 10.5 dBm OP1dB per channel and (b) system NF for different channel gains and array sizes.

loss and 2 dB more ohmic loss in the 1:16 beamformer. In hindsight, it would have been better to design the TX channel gain to be 27 dB to keep the transceiver output power $<$10 dBm up to 64 elements.

In the RX mode, the received power per antenna element (at the chip port), P_{EL} is calculated using

$$P_{EL} = EIRP + 10\log(\frac{\lambda}{4\pi R})^2 - L_{ATM} + G_{EL} \tag{2.3}$$

where R is the link distance, L_{ATM} is the atmospheric attenuation at 28 GHz (0.15 dB/km [17]) and G_{EL} is the microstrip patch antenna element gain (4.5 dB: 6 dB antenna directivity for d_{x} = 0.5λ and d_{y} = 0.63λ $-$ 1.5 dB antenna and feed line loss). The factor $(\frac{4\pi R}{\lambda})^2$ is called the path loss factor (PLF) and is 111 dB at 28 GHz at a range of 300 meters. Assuming a base station transmitting with an EIRP of 65 dBm at a distance of 50-300 meters, P_{EL} is -26 to -41 dBm which sets the linearity requirement per channel. An IP1dB of -22 dBm per channel was chosen for this work since the microstrip antenna has a wide pattern and can receive several interfering base-stations from several directions simultaneously, resulting in a complex interference signal with high peak-to-average-power-ratio (PAPR) at the antenna port.

The linearity of a phased-array is complex to define and depends on the incidence angle of the interferer signals [Fig. 2.4(b)]. First, all interferers are received by each antenna element and fed to the low-noise amplifier (LNA) and the RX channel. The interferers are amplified,

phase-shifted and added together in the 1:32 or 1:64 Wilkinson network, and interferers located at angular directions away from the main-lobe are dissipated in the Wilkinson beamformer and are present at the transceiver port with reduced intensity given by the phased-array sidelobes (-15 to -30 dB depending on how far away from the main-lobe) [18]. The interferers at angles close to the main-lobe are not attenuated by the Wilkinson beamformer and are present at the transceiver with full intensity. Note that the main-lobe is constantly being steered over wide angles, and an interferer located in a sidelobe at timeframe t_1 may be in the main-lobe at timeframe t_2.

The worst-case design is for an interferer in the main-lobe direction. Referring to Fig. 2.4(a) with an RX channel gain of 20 dB, an input P1dB of -22 dBm, and an on-chip Wilkinson loss of 2.2 dB, the OP1dB per 2x2 beamformer chip is -22 dBm + 20 dB RX gain + 6 dB (4 channels) $-$ 2.2 dB ohmic loss $-$ 1 dB for compression = 0.8 dBm. This RX OP1dB increases to +5.8 dBm at the transceiver (sum) port when power from all 8 beamformer chips are added together (0.8 dBm + 9 dB (8 chips) $-$ 4 dB Wilkinson ohmic loss = 5.8 dBm). This shows that a very high linearity transceiver is required if the interferer is at -22 dBm per antenna element and in the main-lobe direction. Note that an IP1dB of -22 dBm per element is conservative and assumes several 65 dBm EIRP base-stations at 50 meters away. The RX OP1dB at the sum point of the array can also be reduced using 5-8 dB gain control on each channel without affecting the system NF. In general, a transceiver IP1dB of -3 to 0 dBm is sufficient for most cases, and such a transceiver will have an NF of $\sim$10-15 dB at 28 GHz.

It can be shown that the NF of an active antenna array should be calculated using the electronic gain from the antenna port to the transceiver, and includes only the ohmic losses of all the Wilkinson combiner stages and not any signal addition [19]. For the 32-element array, there is a total ohmic loss of 6.2 dB following the RX channel, followed by a high-linearity mixer with 10-15 dB single-sideband NF (Fig. 2.4). The 2x2 TRX beamformer chip has an RX channel gain of 20 dB and an RX NF of 4.6 dB, and the resulting system NF is 5.2-6.2 dB using the Friis equation.

Fig. 2.5(b) presents the system NF for different RX gains and array sizes with a 2x2 TRX beamformer NF of 4.6 dB and a transceiver NF of 10 dB. It can be seen that the additional ohmic loss from the combiner has little impact on the system NF for an RX channel gain >20 dB, demonstrating the scalability of this architecture.

2.4 Circuit Design and Building Block Measurements

Fig. 2.3 presents the beamformer core chip block diagram. Each TRX channel includes a single-ended single-pole double-throw switch (SPDT) at the antenna port (ANT), variable gain amplifiers (VGA), phase shifters with 6-bit phase control and a differential SPDT on the Wilkinson side. All circuit blocks are differential except for the SPDT at the antenna port and the first LNA stage. This is to achieve low NF while ensuring stability and avoiding any performance degradation due to bump inductance when the chip is flipped on a PCB. A bidirectional 4:1 Wilkinson network is used to combine the signals from 4 channels in the RX mode or to divide the signal to 4 channels in the TX mode.

Channel selection, phase and gain settings are controlled through a serial peripheral interface (SPI) which can operate up to a clock frequency of 100 MHz. A separate hardwire T/R switch is used to enable fast switching between the TX and RX modes. All pads have electrostatic discharge (ESD) protection and all internal bias currents are generated from two external reference currents, one for the PAs and another for all other blocks.

The schematic of the single-ended SPDT at the antenna port is shown in Fig. 2.6(a). A shunt switch using reverse-saturated HBTs [20] is employed to achieve low insertion loss. The shunt switch emitter length is chosen to be 15 μm which results in an on-resistance, Ron = 5.4 Ω and an off-capacitance, Coff = 37.8 fF. The HBTs are turned on in the isolation mode with a bias current of 600 μA generated through a CMOS current mirror. A lumped CLC impedance inverter with compact area is used to isolate the TX and RX paths, and one capacitor is implemented using the Coff of the shunt HBT transistor. Fig. 2.6(b) and (c) present measurements done on

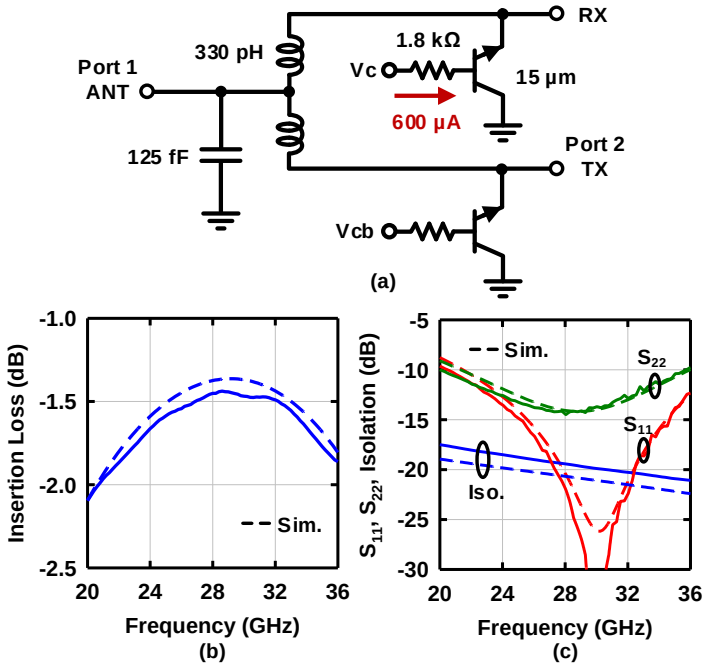


Figure 2.6: (a) Schematic of SPDT, measured (b) insertion loss, (c) matching and isolation.

an SPDT breakout cell for the ANT to TX path. The measured insertion loss is 1.45 dB and the measured isolation is 19 dB at 28 GHz, and agree well with simulations. This level of isolation is adequate since all bias currents of the TX (RX) blocks are turned off in the RX (TX) mode. The IP1dB from the TX port to the antenna port is 15 dBm and results in 0.3 dB gain compression when driven by a PA with an OP1dB of 12 dBm. The switch linearity is limited by the turn-on voltage of the shunt HBTs in the off state [21]. The simulated switching time is 105 ns.

2.4.1 RX Channel

The RX channel consists of a single-ended LNA followed by a passive balun and a differential LNA stage with 5 dB gain control. This is then followed by a 6-bit active phase shifter and a VGA with 4-bit gain control.

The LNA is shown in Fig. 5.3(a). The single-ended first stage has a gain of 6-7 dB with an NF of 2-2.1 dB at 28 GHz. Since the medium-voltage HBTs with high-f_T in this process

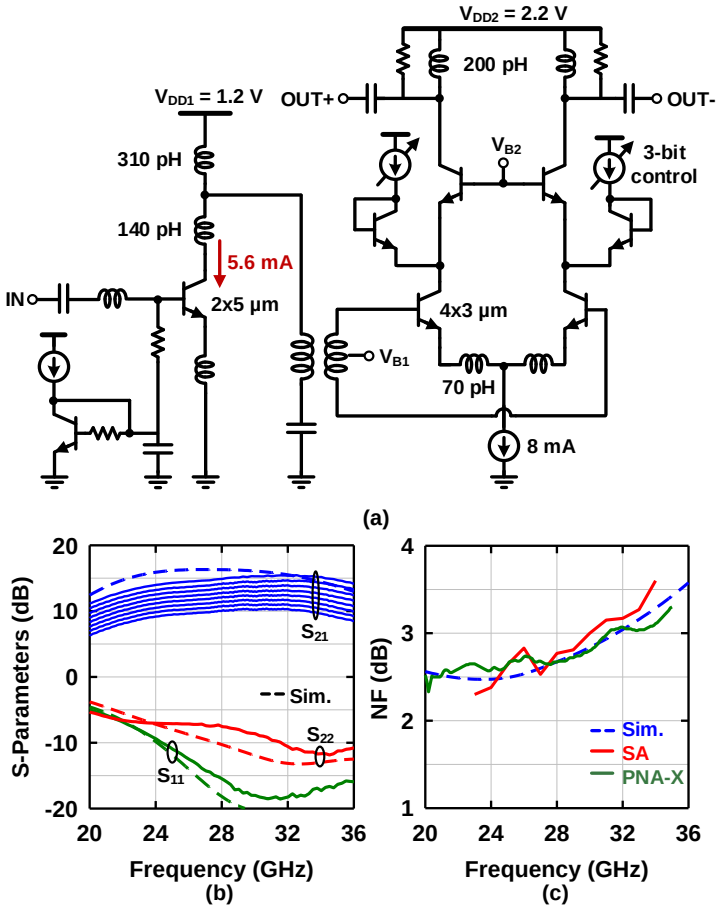


Figure 2.7: (a) Schematic of the 2-stage LNA, (b) measured S-parameters with 5 dB gain control and (c) measured noise figure.

have a breakdown voltage of 1.6 V, the common-emitter stage is operated from a supply of 1.2 V while all other blocks in the chip use a supply of 2.2 V. The gain control is based on current steering at the cascode node proposed in [22] to achieve linear-in-dB gain control. The measured S-parameters of an LNA breakout are shown in Fig. 5.3(b). The test cell includes an additional balun at the output port for single-ended measurements and the balun loss of 1.1 dB was not deembedded. The LNA has a gain of 15.2 dB at 28 GHz and the measurements agree well with simulations. The measured phase change is $<\pm 1.5^{\circ}$ over 5 dB gain control.

The NF of the LNA was measured using two different methods and the results are shown in Fig. 5.3(c). The first method (labeled SA) uses a Keysight 346CK01 noise source with an

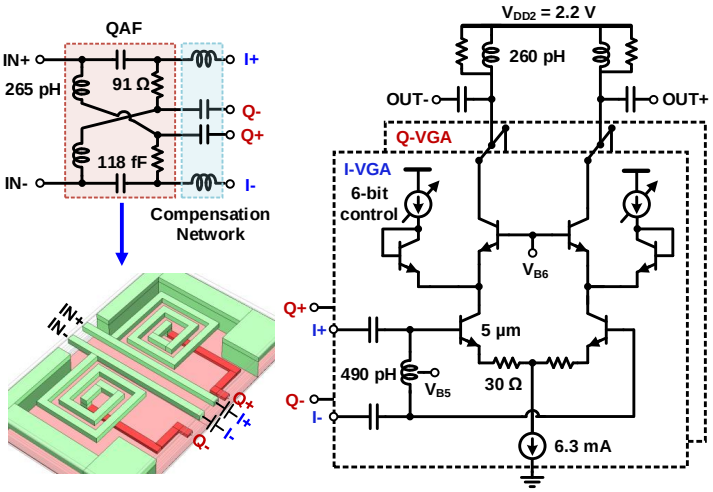


Figure 2.8: Vector modulator design based on a compensated QAF network.

excess noise ratio (ENR) of 12 dB at 28 GHz followed by the LNA under test. The LNA is followed by an external amplifier with 32 dB gain and 4.5 dB NF to suppress the noise contribution of the spectrum analyzer (SA) and the measured NF is plotted after the cable and probe losses are deembedded. The second method uses a Keysight PNA-X calibrated up to the probe tips. The measured LNA NF is 2.6-2.7 dB at 27-28 GHz and the results agree within $\pm$0.1 dB for both measurement methods and with simulations.

The LNA is followed by a 6-bit vector modulator (VM) phase shifter shown in Fig. 2.8. Two orthogonal vectors are generated by a quadrature-all-pass filter (QAF) network. Unlike conventional designs where the QAF is designed for a capacitive load [23, 24], the QAF in this work is designed for a 50 Ω load using an LC compensation network. The compensation network is eventually merged into the vector modulator VGA input matching network resulting in different series capacitance values for the I- and Q-VGAs. This results in an overall narrowband response, but lower NF compared to conventional designs. The layout of the QAF network is also shown in Fig. 2.8 and is critical in generating I/Q vectors with high accuracy.

The I/Q vectors are scaled and added using 6-bit VGAs controlled by a custom 6-bit current DAC to achieve 5.6° phase steps with low gain imbalance. The gain control mechanism

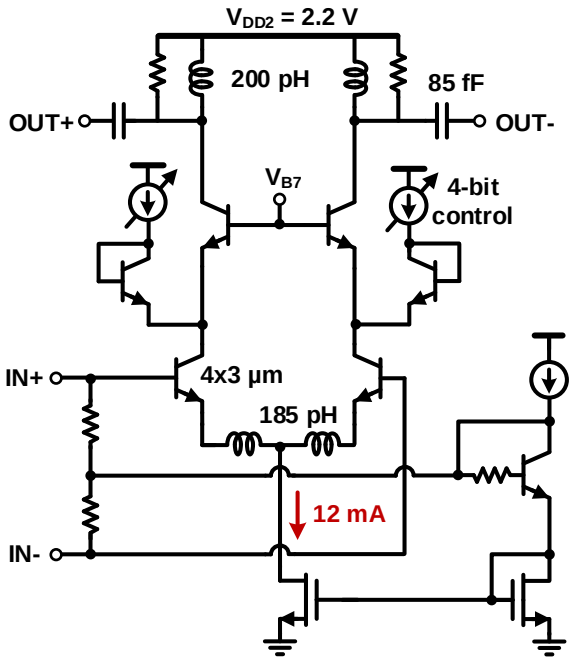


Figure 2.9: VGA schematic with 4-bit gain control using current steering at the cascode node.

used in the second LNA stage is employed for the VM as well as all VGA blocks. Since this VM topology has a fixed tail current and uses current steering at the cascode node, the g_{m} of the input transistors remains constant for all phase settings. This results in a constant input impedance and the VM can operate up to its P1dB without any phase distortion against input power. The RX channel linearity is limited by the VM IP1dB of -7 dBm.

The vector modulator is followed by a high-linearity VGA block (Fig. 5.4) with 9 dB gain control and employs a similar current-steering topology as the second LNA stage. The measured phase change is $<\pm 3^{\circ}$ over 9 dB gain control. The low phase change is critical in order to taper the beam and to calibrate any mismatch between elements in an array using a simple algorithm.

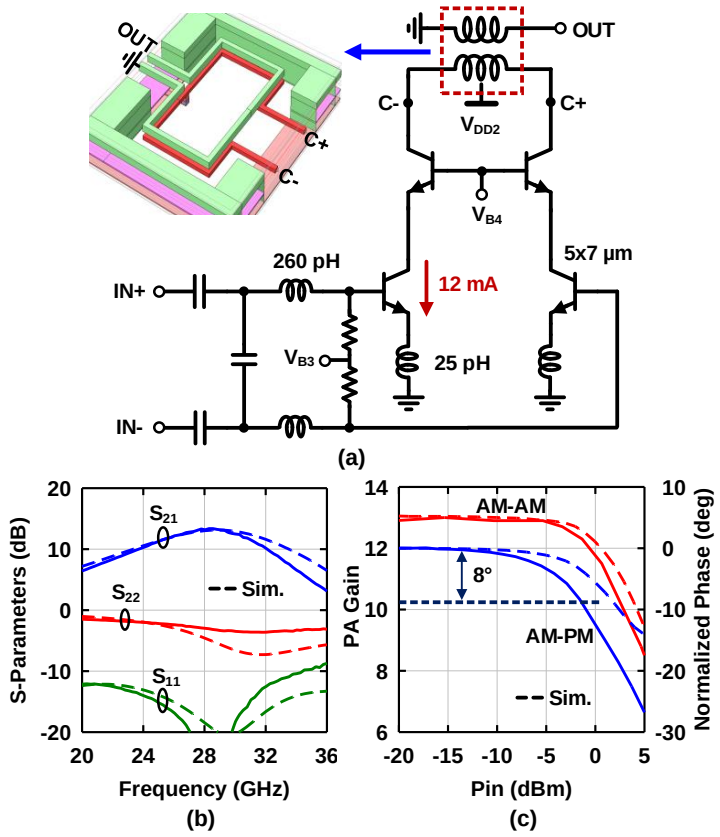


Figure 2.10: (a) Class-AB PA schematic, (b) measured S-parameters, (c) AM-AM and AM-PM distortion.

2.4.2 TX Channel

The TX channel uses a similar 6-bit phase shifter as the RX channel (Fig. 2.8) followed by a VGA with 14 dB gain control, similar to the RX VGA. Since VGAs that do not employ attenuators typically have constant IP1dB with gain control, the output power will drop when the gain is reduced. Therefore the VGA would need to deliver enough power to the PA in the lowest gain setting in order to operate the PA at P1dB which would lead to very high power consumption in the VGA. In this design, the TX VGA can deliver an OP1dB of 3 dBm to the following PA (which has an IP1dB of -1 dBm) to ensure that the channel OP1dB does not drop within 4 dB of gain control. This gain control can be used for array calibration or to taper the beam.

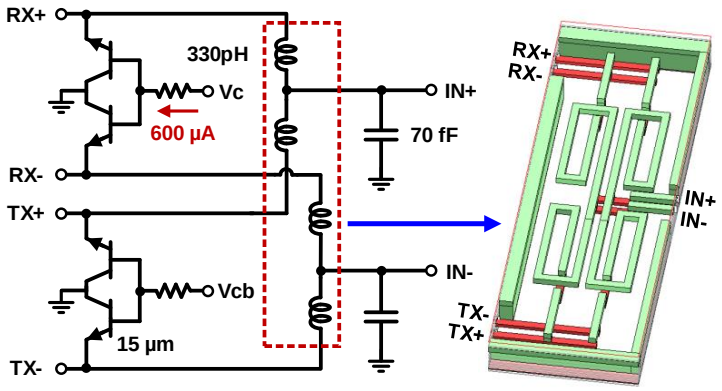


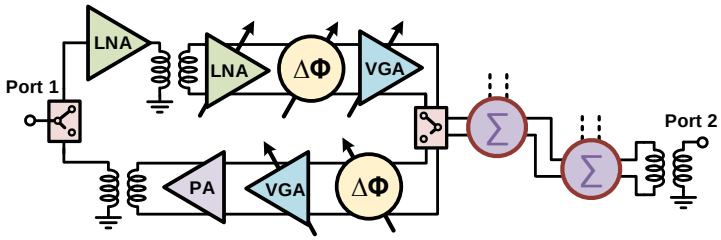
Figure 2.11: Schematic of the differential SPDT on the Wilkinson side.

The PA is implemented with a single-stage pseudo-differential cascode topology biased in class-AB [Fig. 2.10(a)]. The nominal bias current is 12 mA per branch and increases to 24 mA at the P1dB power level. The cascode is loaded by a 1:1 transformer balun which also provides ESD protection at the antenna ports. The transformer balun is implemented using a single turn in the top two metal layers [Fig. 2.10(a)] with L = 260 pH, Q = 17.5 and a coupling value of 0.6 which results in an insertion loss of 0.8 dB at 28 GHz.

The measured S-parameters of a PA breakout are shown in Fig. 2.10(b) and show excellent agreement with simulations. The breakout includes an extra balun at the input side for single-ended measurements and its loss was not deembedded. The PA can deliver an output power of 12 dBm at 28 GHz with a power-added efficiency (PAE) of 13% at P1dB. Note that this PAE includes the differential to single-ended transformer.

A critical metric for a PA operating under modulation is the AM-PM distortion since 5G data links will rely on complex modulated waveforms with high PAPR. The measured AM-AM and AM-PM distortion are shown in Fig. 2.10(c) at 28 GHz, and the AM-PM is $<8^\circ$ at P1dB with a total bias current of 24 mA. This ensures that the PA can amplify complex waveforms with little distortion.

The RX and TX channels are combined on the Wilkinson side using the differential SPDT shown in Fig. 2.11. The design is similar to the single-ended SPDT at the antenna port



	SE SPDT	LNA	VM	RX VGA	TX VGA	PA	DE SPDT	4:1 Wilk.	Balun
Gain (dB)	-1.5	16.3	1.0	8.2	11.3	14.1	-1.6	-1.1	-1.1
NF (dB)	1.5	2.7	12.0	3.3	3.6	–	1.6	1.1	1.1
IP_{1dB} (dBm)	15	-19	-7	-5	-7	-1	18	–	–

Figure 2.12: Gain, NF and IP1dB of the 2x2 TRX beamformer core chip blocks.

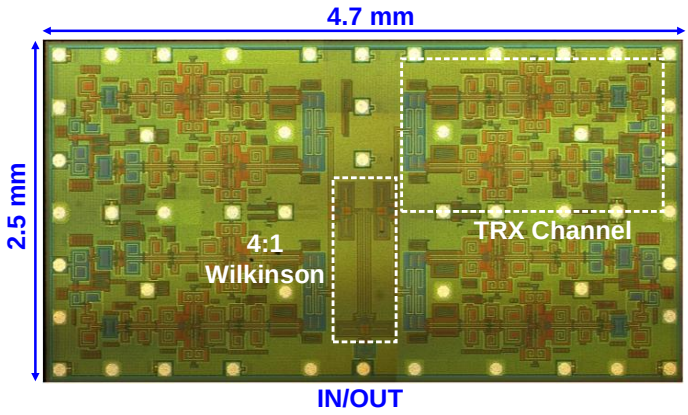


Figure 2.13: Chip photograph of 2x2 TRX core chip with 400 μm pitch bumps.

and uses shunt reverse-saturated HBTs. The layout is designed to match the TX and RX channel layouts resulting in larger area and 0.1 dB higher loss compared to the single-ended SPDT.

The four channels are combined using a 4:1 differential Wilkinson combiner/divider network with a simulated ohmic loss of 1.1 dB including the interconnecting transmission lines. Each Wilkinson is based on a wideband lumped CLC implementation to achieve compact area [25] and the 100 Ω isolation resistors are placed very close to the input ports to achieve $>$20 dB isolation. This is followed by a passive balun with 1.1 dB loss to enable single-ended routing on the PCB from the chip common port. Fig. 2.12 summarizes the gain, NF and IP1dB of all building blocks in the core chip.

2.4.3 2×2 TRX Chip Measurements

The chips were fabricated in the TowerJazz SBC18H3 SiGe BiCMOS process with a size of 2.5 x 4.7 mm^2 and a minimum pad (bump) spacing of 400 μm (Fig. 2.13). The measured S-parameters of a single-channel are shown in Fig. 2.14 from the common port to the antenna port with the port definitions shown in Fig. 2.12. The S-parameter measurements include the ohmic loss of the Wilkinson network and the balun at the common port, but 6 dB has been added to both TX and RX S-parameter measurements to characterize the channel response together with the on-chip Wilkinson network ohmic loss. In the RX mode, the actual chip gain will be the same as presented in Fig. 2.14. In the TX mode, the actual chip gain will be 6 dB lower due to 6 dB division loss to 4 channels.

The measured RX and TX channel gain is 20 dB [Fig. 2.14(a) and (b)] and the measurements agree well with simulations. The measured reverse isolation is -55 to -60 dB in both the TX and RX modes. Fig. 2.14(c) presents the insertion phase for all 64 phase states in the RX mode and Fig. 2.14(d) shows the corresponding RX gain for all 64 phase states. The measured average rms phase error in the RX and TX modes is 3.4° and the average rms gain error is 0.5 dB at 29 GHz [Fig. 2.14(j)]. The measured NF for all phase states is shown in Fig. 2.14(e) (4.6-4.8 dB) and is the lowest reported-to-date for a transmit/receive beamformer chip at 28 GHz.

Previous work using vector modulator phase shifters at mm-waves have reported significant distortion in phase states against input power [26, 27]. The measured RX channel insertion phase for 16 phase states is shown in Fig. 2.14(f) against input power, and the VM can operate well up to the RX IP1dB of -22 dBm due to the VM topology employed with a fixed tail current (see Fig. 2.8). Beyond P1dB, there is some phase distortion due to AM-PM conversion, but the phase characteristic against input power is similar for all phase states and the phase difference is conserved.

The measured gain states are shown in Fig. 2.14(g) and (h). Both TX and RX modes have 14 dB gain control (5 dB LNA control, 9 dB VGA control for the RX mode) and the measured

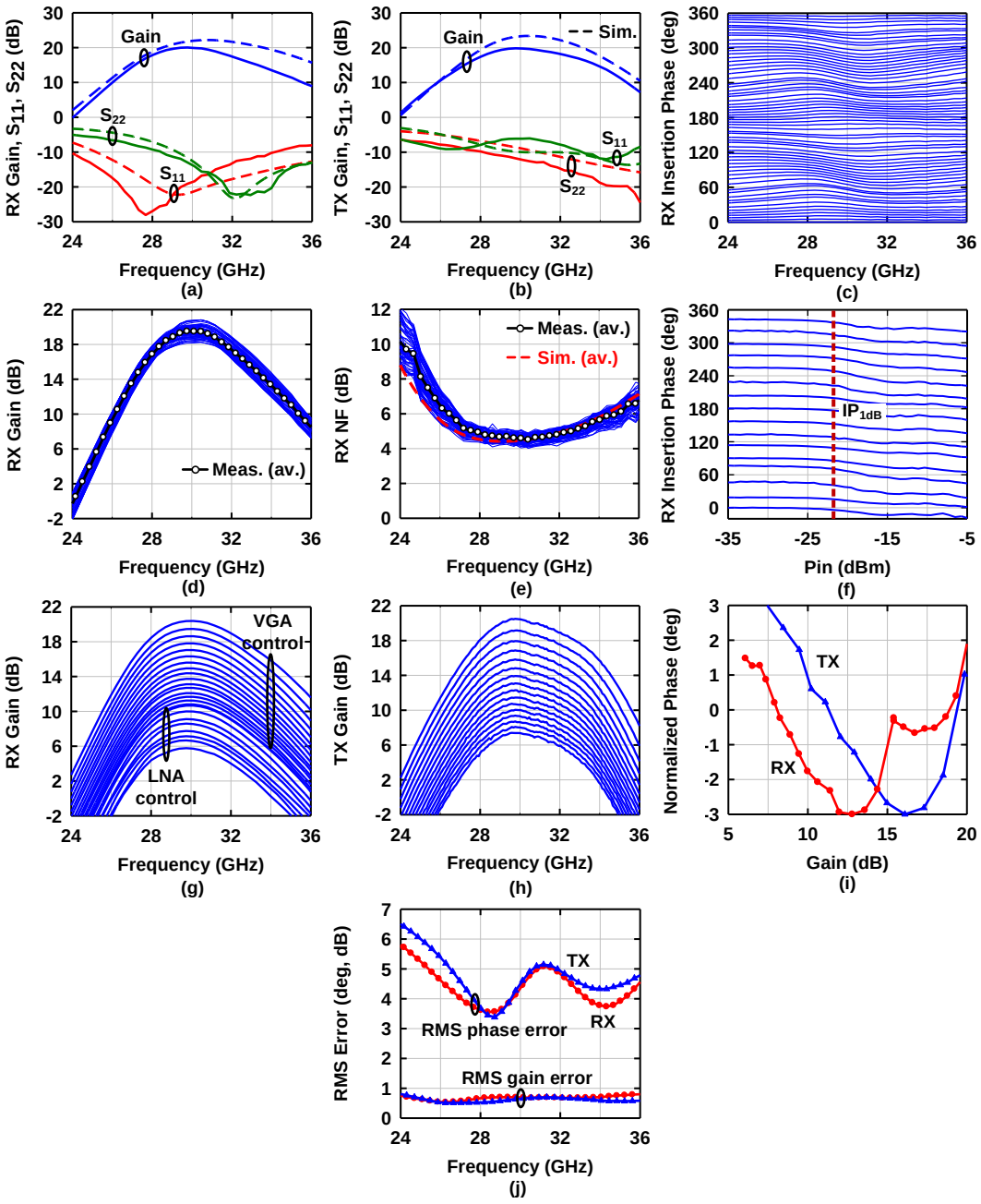


Figure 2.14: Measured (a) RX S-parameters, (b) TX S-parameters, (c) RX phase states, (d) RX gain for all phase states, (e) RX NF for all phase states, (f) RX phase vs. input power, (g) RX gain control, (h) TX gain control, (i) channel phase change with gain control, (j) phase shifter rms gain and phase errors.

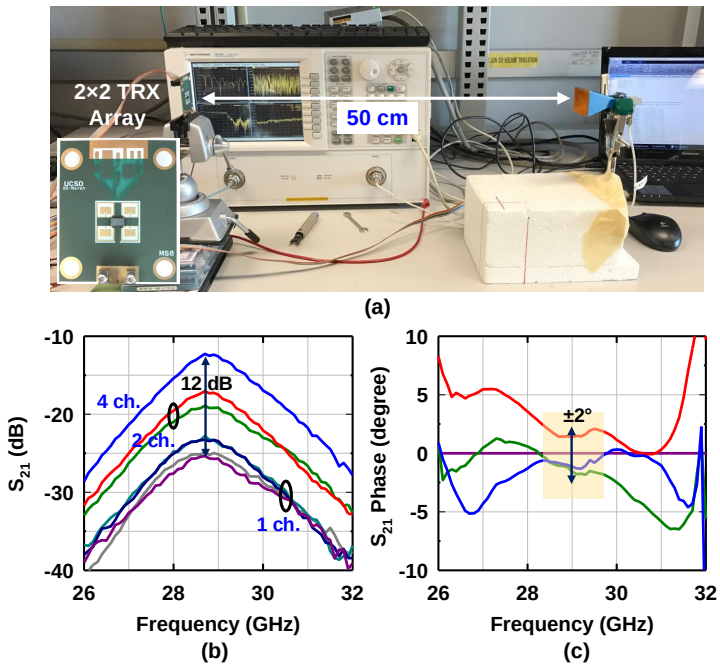


Figure 2.15: (a) Measurement setup of the flip-chip TRX array with 2x2 antennas on a PCB. Measured (b) gain and (c) phase of all 4 channels in the RX mode.

channel phase change is $<\pm 3^\circ$ over 14 dB gain control range [Fig. 2.14(i)]. This allows for a near-perfect orthogonality between gain and phase control, and allows the user to compensate for chip to chip variations and taper the array over a wide range without the need for additional phase trimming.

The chip consumes 130 mW per channel in the RX mode with an IP1dB of -22 dBm and an input 3rd order intercept point (IIP3) of -12 dBm. In the TX mode, the chip consumes 200 mW per channel at the OP1dB of 10.5 dBm. Note that the RX power consumption is high due to the very high IP1dB specifications.

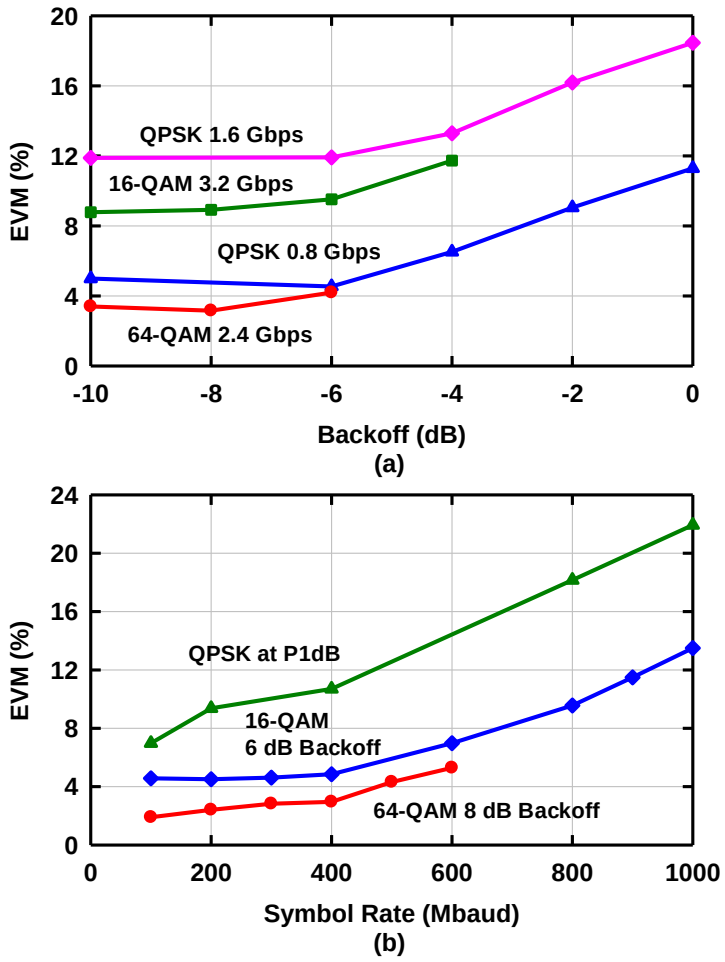


Figure 2.16: Measured EVM using two single-chip TRX array boards at (a) different back-off levels and (b) different symbol rates for various modulation schemes at 1 meter link distance.

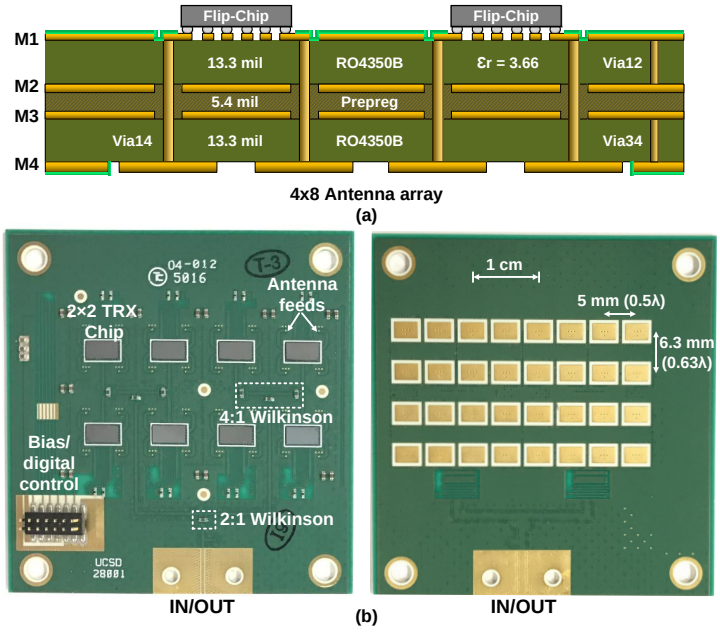


Figure 2.17: (a) 4-layer PCB stackup for the low-cost 32-element (4x8) TRX array, and (b) top and bottom views of the array PCB with flip-chip beamformer ICs and PCB integrated microstrip antennas.

2.5 System Measurements

2.5.1 2×2 TRX Phased-Array Measurements

The 2x2 TRX chip was first flipped on a test board with a single 6.6 mil RF layer and 2x2 antennas on the same side as the chip, as presented in [28]. The chip was tested in the RX mode in the far-field using a vector network analyzer (VNA) and a standard gain horn antenna as the transmitter [Fig. 2.15(a)]. The channels were turned on individually using the SPI control. A gain difference of ± 1 dB [Fig. 2.15(b)] and a phase difference of $\pm 2^{\circ}$ was obtained between the 4 channels within the test antenna S_{11} bandwidth of 400 MHz [Fig. 2.15(c)]. The gain difference can easily be corrected using the VGA on each channel, but this is not required as presented in the next section. Also, part of the gain difference could be due to standing waves in the test setup. Since the channel responses match well, the gain increases as N^2 as the number of channels increases [Fig. 2.15(b)].

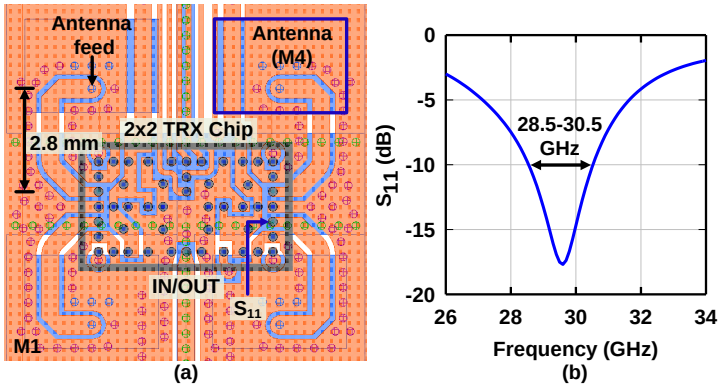


Figure 2.18: (a) PCB design of the 2x2 flip-chip unit cell (M1 and M4 are shown) and (b) simulated antenna impedance (S_{11}) at the chip port including the antenna feed line.

The 2x2 array has a measured EIRP of 24.5 dBm at 29 GHz with a 3-dB bandwidth of 28.4-29.4 GHz. A 1-meter test link was set up using two of these 2x2 TRX arrays and the EVM was measured using various modulations and back-off levels (Fig. 2.16). The back-off level is defined as the difference between the average symbol power and the 2x2 array P1dB. The maximum data rate measured is 3.6 Gbps using 64-QAM at 8 dB back-off and 4.0 Gbps using 16-QAM at 6 dB back-off. The measured EVM increases above 400 Mbaud symbol rate, and is limited by the antenna S_{11} bandwidth of 400 MHz.

2.5.2 32-Element (4×8) TRX Phased-Array Measurements

To achieve higher EIRP and Gbps data links at hundreds of meters, a 32-element (4x8) phased-array was designed with the PCB stackup shown in Fig. 4.9(a). This stackup is very low cost since it uses only 4 RF layers with two RO4350B cores of 13.3 mil thickness. The top and bottom views of the 32-element array PCB are shown in Fig. 4.9(b), and PCB design of the 2x2 unit cell is shown in Fig. 4.6(a). The beamformer chips are flipped on M1, the antennas are placed on M4, and the chip-to-antenna feed line loss is only 0.5 dB at 29 GHz. A 10-mil (250 μm) via hole is used from M1 to M4 to feed the antenna, with M3 used as the antenna ground plane. The via-fed microstrip antenna can achieve an S_{11} bandwidth of 2 GHz (28.5-30.5 GHz) when the feed line is included in the antenna-to-chip matching network [Fig. 4.6(b)]. The

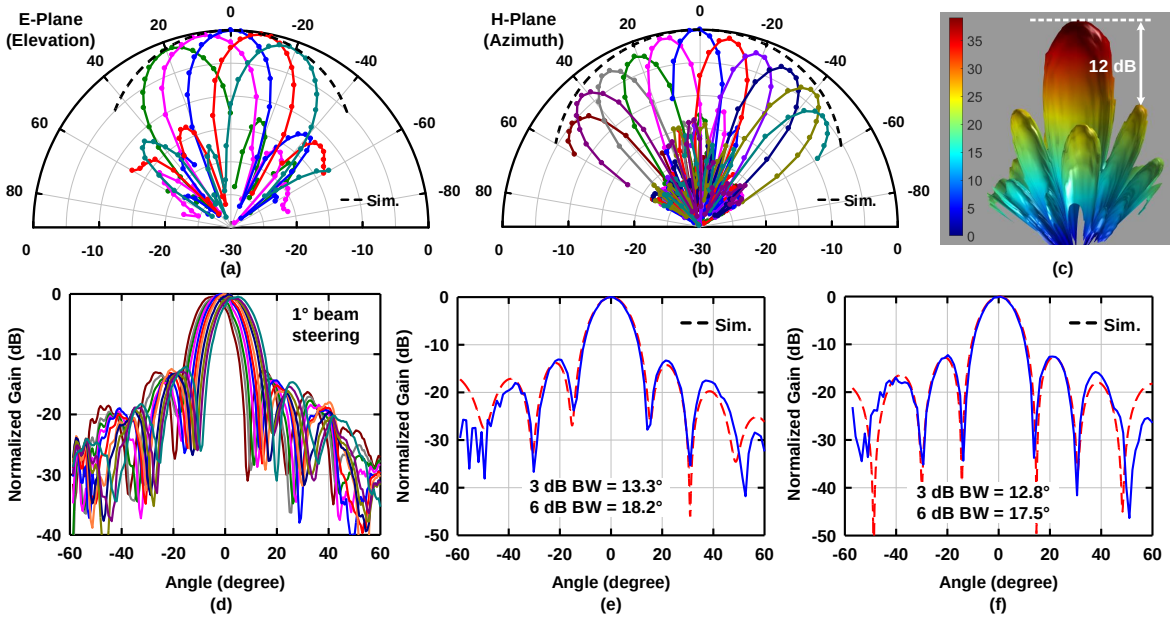


Figure 2.19: Measured (a) E-plane and (b) H-plane patterns of the 4x8 TRX array in the RX mode at 29.5 GHz, (c) 3-D pattern (H-plane is shown), (d) fine resolution beam steering in the H-plane without calibration. Measured H-plane patterns at boresight (e) without calibration and (f) with calibration.

antenna efficiency of $\sim$90% and S_{11} of -10 dB results in 1 dB antenna ohmic and mismatch loss. M1 is used for the 8:1 Wilkinson network based on standard $\lambda/4$ transmission lines and lumped 100 Ω resistors are placed on M1 to provide isolation. M1 and M2 layers are also used as RF ground for the Wilkinson network, and for digital control and bias distribution.

The scanning requirements for the 4x8 array are $\pm 50^{\circ}$ in azimuth and $\pm 25^{\circ}$ in elevation for a 50- to 300-meter 5G data link. An antenna spacing, d_x = 5 mm in the horizontal direction (0.5λ at 30 GHz) and d_y = 6.3 mm (0.63λ at 30 GHz) in the vertical direction are chosen to satisfy this scanning requirement without a grating lobe [29]. Note that the antennas are vertically polarized, and therefore, the E-plane and H-plane scans are in the elevation and azimuth directions, respectively.

The 32-element phased-array antenna patterns were measured in an anechoic chamber in the RX mode and are shown in Fig. 4.11. First, the E- and H-plane patterns were measured at 29.5 GHz without any phase or amplitude calibration and agree very well with simulations [Fig.

4.11(a) and (b)]. The peak of the array pattern closely follows the simulated H-plane element factor ($\sim cos^{1.3}(\theta)$), and the array gain is 5 dB lower at $\pm 50^{\circ}$ scan angle. The sidelobe levels are < -12 dB over all scan angles (no taper used) due to the symmetric design of the beamformer chips and the Wilkinson distribution network. This shows that the 32-element phased-array can be used without any calibration, thus greatly reducing the testing costs. A 3-D pattern plot at boresight from the H-plane view is shown in Fig. 4.11(c) and agrees well with the E- and H-plane 2-D patterns.

The 6-bit phase shifter step is 5.6° which would result in a minimum beam step of 1.8° if a progressive phase shift is applied between the elements, but the beam can be steered in much finer resolution as demonstrated in [30]. For example, by setting the phases of the 8 antenna columns to $\{0^{\circ}, 0^{\circ}, 5.6^{\circ}, 5.6^{\circ}, 11.2^{\circ}, 11.2^{\circ}, 17^{\circ}, 17^{\circ}\}$, the average phase change per unit cell becomes 2.8° and the beam can be steered in the H-plane with 1° steps as shown in Fig. 4.11(d). The phase interpolation will result in quantization lobes. However, for 5.6° phase shifter steps, these quantization lobes remain < -29 dB even at large scan angles [31], and do not appear in the measured patterns since they are at a much lower level than the typical array sidelobes (-12 to -20 dB).

The placement of the chips on the PCB and any small deviation between the PCB traces will cause slight mismatches between the phase and gain response of the array elements and could result in higher sidelobes, wider beamwidth and lower EIRP. In order to test this, the 32-element array was calibrated by measuring the phase and gain of each element in the far-field using a VNA after turning on the elements individually. A maximum gain and phase difference of ± 1.5 dB and $\pm 10^{\circ}$ was measured between the elements. This difference was then calibrated using the gain and phase control on each element and the measured boresight H-plane patterns are shown in Fig. 4.11(e) and (f) (before and after calibration). The simulated patterns based on the measured response of each channel are also plotted and agree well with measurements.

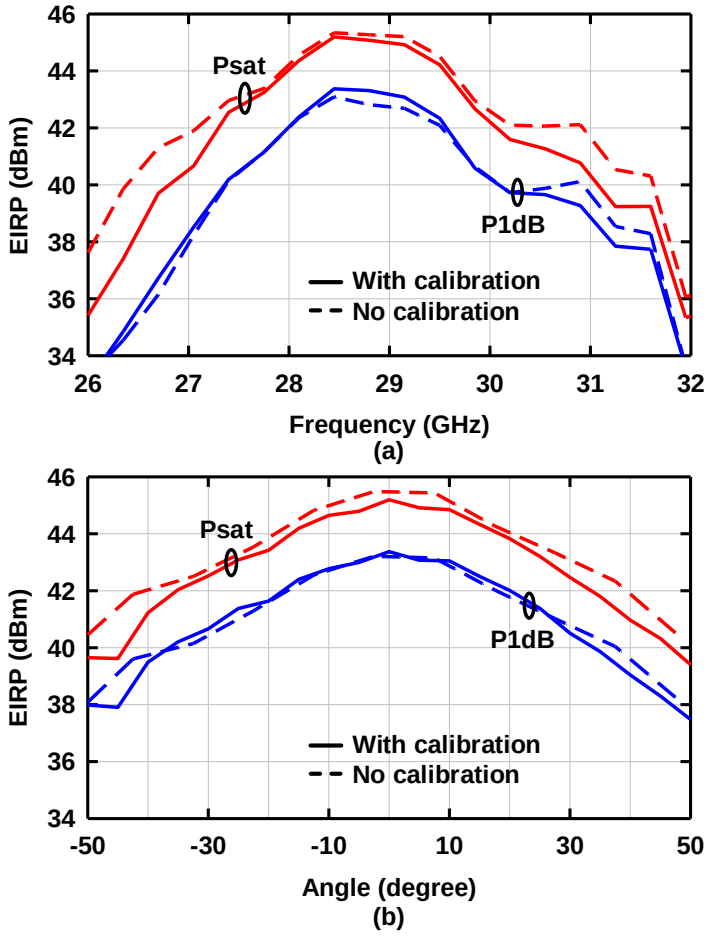


Figure 2.20: (a) Measured calibrated and uncalibrated EIRP of the 4x8 array at P1dB and Psat. (b) Measured EIRP vs. scan angle in the H-plane at 29 GHz.

The 3-dB beamwidth at normal incidence is approximated using

$$BW_{3dB} \simeq \frac{0.886\lambda}{N_x d_x} \tag{2.4}$$

for uniform distribution. This results in 12.8° at 29.5 GHz with the antenna spacing used. With calibration, the 3-dB beamwidth is reduced from 13.3° to 12.8° which is the theoretically expected value. However, the sidelobe levels for the uncalibrated array are already <-12 dB, and these measurements prove that the array can work with excellent performance without any calibration.

The 32-element phased-array EIRP was then measured with and without calibration [Fig. 4.17(a)]. The peak EIRP is achieved at 28.5-29 GHz and is 43 dBm at P1dB and 45 dBm

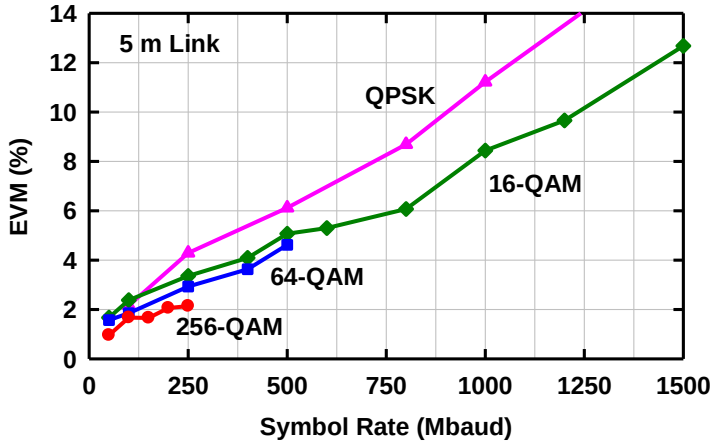


Figure 2.21: Measured EVM vs. symbol rate for different modulation schemes at 5 meters link distance using two 32-element 5G phased-arrays.

at the saturated output power (Psat), with a 3-dB bandwidth of ∼27.5-30.5 GHz. The array was calibrated at an input power close to P1dB in the TX mode at 29 GHz, and therefore the calibrated EIRP is 0.5 dB higher than the uncalibrated EIRP at P1dB at 29 GHz. Note that the uncalibrated phased-array Psat levels are slightly higher than the calibrated phased-array results since the VGAs are not used to lower the gain for some channels. The measured EIRP at 29 GHz vs. scan angle in the H-plane is shown in Fig. 4.17(b) (with and without calibration) and agrees with the measured H-plane patterns [Fig. 4.11(b)]. Overall, the results indicate that the 32-element array operates well without calibration due to its symmetrical design.

A 5-meter link was set up using two 32-element arrays and the measured EVM values at normal incidence for different modulations and symbol rates are shown in Fig. 2.21 at the back-off level equal to the PAPR of the modulated waveform. The maximum measured data rate was 6 Gbps with 16-QAM with 12.6% EVM, again limited by the antenna bandwidth (no forward error correction (FEC) or equalization used). The array can support up to 2 Gbps 256-QAM modulation with 2.1% EVM. The EVM was then measured using the Verizon pre-5G 64-QAM orthogonal frequency division multiplexing (OFDM) waveform with 8 component carriers spaced at 100 MHz. Fig. 2.22 presents the measured constellations and spectra for the first-two and last-two component carriers. The measured EVM values are shown with the worst case

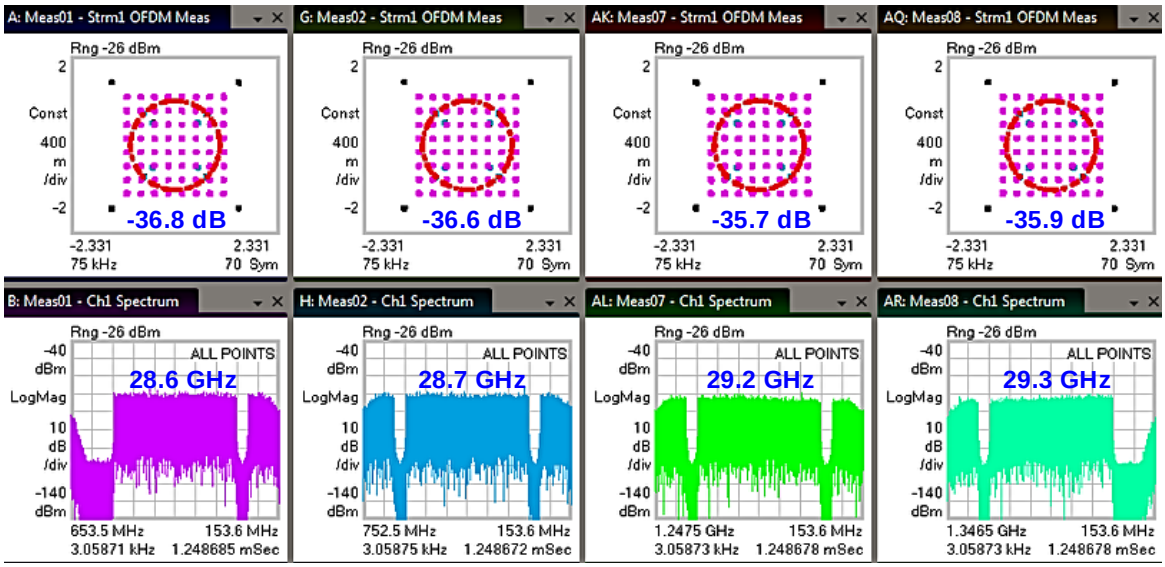


Figure 2.22: Measured constellations and spectra using the Verizon pre-5G 64-QAM OFDM waveform with 8 component carriers spaced at 100 MHz (800 MHz total bandwidth). Carrier frequencies and measured EVM values are shown for 4 carriers with a worst case EVM of -35.7 dB (1.64%).

EVM of 1.64% at 12 dB back-off from P1dB.

2.5.3 300-Meter 5G Link Measurements

Based on the EIRP and short distance EVM measurements, a link budget can be calculated to determine the expected performance of the 32-element array at a link distance of 300 meters. Without using digital pre-distortion (DPD), the TX array should operate at 6-7 dB back-off for a 16-QAM waveform with 2.55 dB PAPR which increases to 6.6 dB when a root-raised-cosine filter with a roll-off factor $\alpha = 0.35$ is applied [32]. This results in an average EIRP of 36-37 dBm with a peak symbol power of 42-43 dBm under modulation. The total received power, P_{R}, system noise, P_{N} and SNR at the receiver output are calculated using

$$P_R = EIRP - PLF - L_{ATM} + G_{ANT} - L_{MIS} \tag{2.5}$$

$$P_N = 10\log(kT(1+\alpha)B) + NF_{SYS} \tag{2.6}$$

$$SNR = P_R - P_N \tag{2.7}$$

where G_{ANT} is the transmit/receive antenna gain (19 dB) including 1 dB antenna and mismatch loss and 0.5 dB feed-line loss, L_{MIS} is the power loss due to array misalignments (1 dB), k is the Boltzmann constant, T is the absolute temperature, B is the modulation bandwidth, NF_{SYS} is the system NF calculated for Fig. 2.24(a) (7.5 dB) and EIRP is that of the TX array at 6-7 dB back-off. Since the receiver SNR is dominated by the noise floor, other sources of EVM degradation such as LO phase noise, receiver I/Q mismatch and TX nonlinearity can be ignored in estimating the expected EVM. Any incoming signal at the image frequency (LO $-$ IF) will also be greatly attenuated by the narrowband antennas and the TRX chips and will not degrade the EVM. The calculated SNR is plotted in Fig. 2.23(a) for different modulation bandwidths at normal incidence, $\pm 50^{\circ}$ scan in the azimuth (H-plane) and $\pm 20^{\circ}$ scan in the elevation (E-plane) direction [see Fig. 4.17(a) and (b)].

Fig. 2.23(b) presents the corresponding EVM obtained from the calculated SNR using

$$EVM(\%) = 100 * 10^{(-(SNR+PAPR)/20)} \tag{2.8}$$

where PAPR is that of the ideal constellation before any filtering is applied [32]. The EVM limits to achieve a bit-error-rate $<10^{-3}$ are also marked [33]. Based on these calculations, the 32-element array can operate at 300 meters with a maximum data rate of 600 Mbps (100 Mbaud) using 64-QAM, and 1.5 Gbps (375 Mbaud) using 16-QAM over all scan angles. The simulations do not take into account any gain and phase ripple within the modulation bandwidth due to the components used in the measurement setup which will ultimately limit the maximum data rate if FEC, DPD or equalization are not used.

The measurement setup for the 300-meter link using two 32-element arrays is shown in Fig. 2.24(a). A 16-QAM signal is generated at an IF of 6 GHz using a Keysight M8195A arbitrary waveform generator (AWG) and upconverted to 29 GHz using an external mixer with an LO of 23 GHz. A variable attenuator is employed following the upconversion mixer to adjust the RF power into the array. The received signal at the RX phased-array is downconverted using a passive mixer, amplified and demodulated using a Keysight DSO-S804A real-time oscilloscope

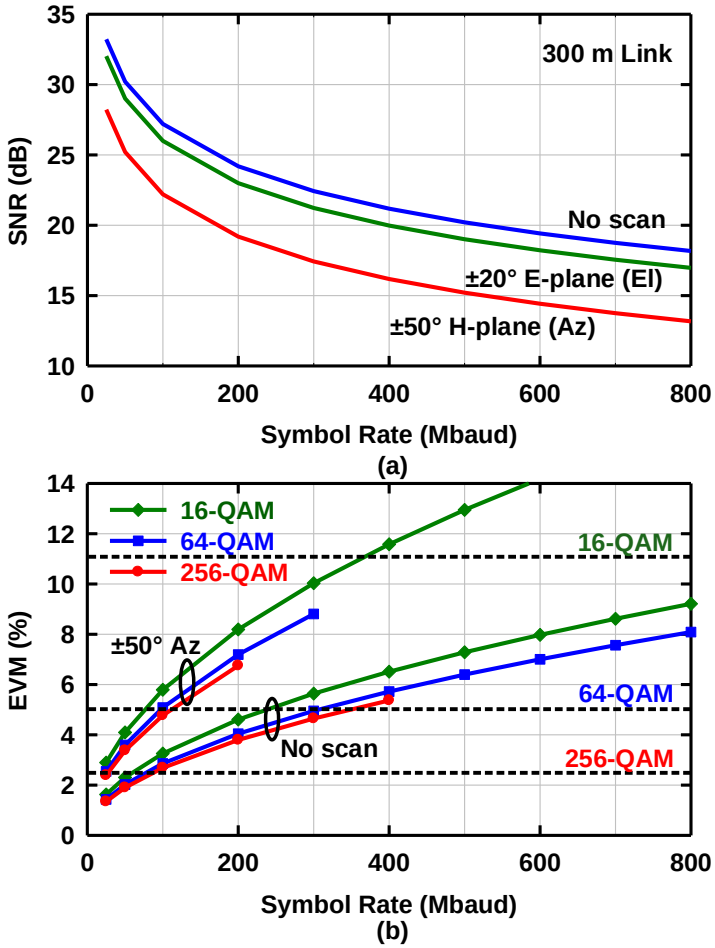


Figure 2.23: Simulated (a) SNR and (b) corresponding EVM at different modulation bandwidths for a 300-meter link using 32-element phased-arrays.

running the VSA 89600 software. A photograph of the measurement setup is also shown in Fig. 2.24(a) where the TX array is placed at the 6th floor of a building and the RX array is placed at a parking lot 300 meters away. The arrays are placed in line-of-sight and scanned in the E- and H-planes by mechanically turning the RX array and electronically steering the beam back towards the TX array.

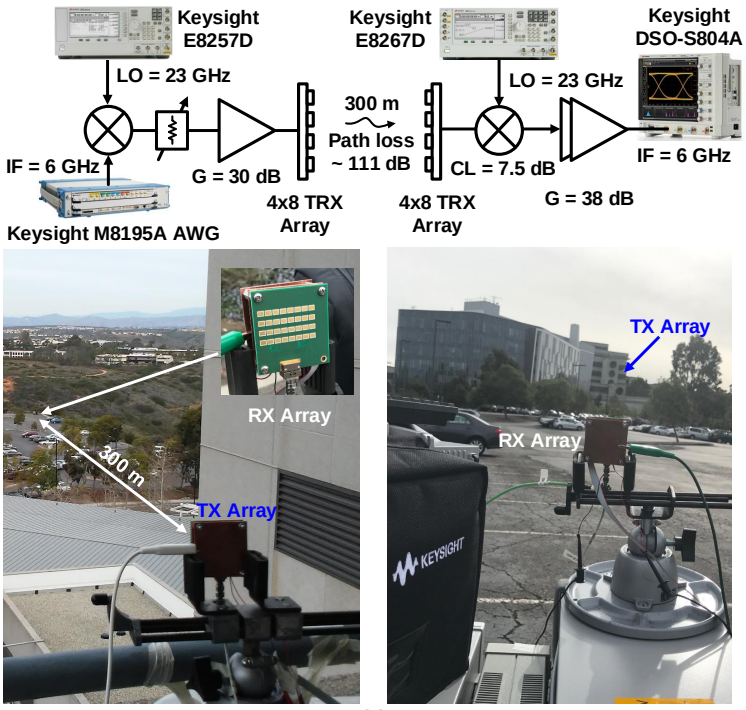
The measured constellations at different distances, data rates, scan angles and modulated waveforms are presented in Fig. 2.24(b). All of the measurements are performed without any array calibration, FEC, DPD or equalization. Example constellations from the measurements presented in Fig. 2.21 for a 5-meter link are also shown.

The 32-element array can achieve a data rate $>$1 Gbps over all scan angles using 16-QAM with 9.6-12.1% EVM (simulated 6.5-9.3% without taking into account any TX nonlinearities and LO phase noise effects, and assuming no gain and delay ripple vs. frequency). The maximum data rate at normal incidence is 1.6 Gbps with 10.9% EVM for the 300-meter 5G link. These results are the highest data rate at the longest link distance reported-to-date for a 28 GHz 5G phased-array to our best knowledge.

Table 2.2 summarizes the performance of this work and compares it with state-of-the-art mm-wave phased-array transceivers.

2.6 Conclusion

A 32-element 5G phased-array transceiver is built using a very low-cost PCB design and is based on 2x2 TRX beamformer core chips with state-of-the-art performance. The design can easily be scaled to larger arrays and can operate without any calibration and with excellent performance. Future work includes the demonstration of 64- to 256-element dual-polarized TRX arrays with wider bandwidth and simultaneous data links in a MIMO configuration.



(a)

Measured Constellations at Different Distances, Data Rates, Scan Angles and Modulations				
16-QAM				
Data rate EVM	5 m / +50° H 2 Gbps / 3.7%	5 m / +50° H 4 Gbps / 6.7%	300 m / 0° 400 Mbps / 5.9%	300 m / 0° 1.6 Gbps / 10.9%
16-QAM 300 m 1 Gbps				
Data rate EVM	300 m / +50° H 1 Gbps / 12.1%	300 m / -50° H 1 Gbps / 11.7%	300 m / +20° E 1 Gbps / 10.3%	300 m / -20° E 1 Gbps / 9.6%
Different mod. 5 m 0° scan				
Data rate EVM	QPSK 3 Gbps / 16.9%	16-QAM 6 Gbps / 12.6%	64-QAM 3 Gbps / 4.6%	256-QAM 2 Gbps / 2.1%

(b)

Figure 2.24: (a) Measurement setup of the 300-meter communication link, and (b) measured constellations at different link distances, data rates, scan angles and modulations.

2.7 Acknowledgment

This work was supported in part by Facebook, in part by Keysight Technologies, and in part by the Defense Advanced Research Projects Agency (DARPA). The authors would like to thank Bhaskara Rupakula at University of California San Diego for the 32-element array calibration and Michael Millhaem at Keysight for the Verizon waveform measurements.

Chapter 2, in full, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer and G. M. Rebeiz, "A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a 2x2 Beamformer Flip-Chip Unit Cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260-1274, May 2018. The dissertation author was the primary investigator and author of this paper.

Table 2.2: Comparison with State-of-the-Art mm-Wave Phased-Array Transceivers

Parameter	**This work**	LG '17 [7]	IBM '17 [8]	Broadcom '14 [6]
Process	**0.18 μm SiGe BiCMOS**	28 nm LP CMOS	0.13 μm SiGe BiCMOS	40 nm LP CMOS
Frequency (GHz)	**28**	28	28	60
Elements per chip	**4 TRX**	2x4 TRX	2x16 TRX	16 TRX
Elements in array	**32 TRX**	2x8 TRX	2x64 TRX	16 TRX
Chip area (mm^2)	**11.7**	7.3	165.9	26.3
IC integration level	**RF front-end**	RF front-end + RF/IQ conversion + VCO	RF front-end + RF/IF conversion	RF front-end + RF/IF conversion + PLL
Polarization	**Single**	Dual	Dual	Single
RF gain control RX / TX (dB)	**14 / 14**	22 / 42	8 / 8	10 / -
Phase step (°)	**5.6**	45	4.9	5.6
Scan angles E- / H-planes (°)	**±25 / ±50**	- / ±20	±50 / ±50	±50 / ±50
Sidelobe level (dB)	**<−12**	<−9	<−12	<−10
Beam steering resolution (°)	**<1**	-	1.4	-
TX OP_{sat} / OP_{1dB} / el. (dBm)	**12.5 / 10.5**	10.5 / 9.5	16 / 13.5	>6 / 3.2
RX IP_{1dB} (dBm)	**−22.0**	-	−22.5	-
RX NF / chip (dB)	**4.6 (5.2)***	6.7	6.0	<10
TX power dissipation / el. (mW)	**200 @ P_{1dB}**	85 @ 24 dBm EIRP	319 @ P_{sat}	74
RX power dissipation / el. (mW)	**130**	50	206	60
TX power dissipation / IC (W)	**0.80 @ P_{1dB}**	0.68 @ 24 dBm EIRP	5.1 @ P_{sat} / pol.	1.19
RX power dissipation / IC (W)	**0.52**	0.4	3.3 / pol.	0.96
EIRP at P_{sat} (dBm)	**45**	31.5	54 / pol.	27
Calibration	**No**	-	Yes	Yes
Constellation	**QPSK/16-64-256-QAM**	64-QAM	-	QPSK/16-64-QAM
Over-the-air data rate	**6.0 Gbps 16-QAM at 5 m** **3.0 Gbps 64-QAM at 5 m** **2.0 Gbps 256-QAM at 5 m** **1.6 Gbps 16-QAM at 300 m**	LTE 20 MHz 64-QAM at 2.5 m	-	4.6 Gbps 16-QAM at 10 m 3.0 Gbps 16-QAM at 20 m

*System NF = 5.2 dB with 4 dB combiner loss and 10 dB transceiver NF [(see Fig. 2.5(b)].

Chapter 3

28 GHz Transceiver Chip

3.1 Introduction

The fifth-generation (5G) communication links will rely heavily on 2-dimensional phased-array antennas to achieve high data rates at large link distances using directive beamforming at mm-wave bands [1]. The number of antenna elements will vary between 4-16 elements on a hand-held unit and 64-256 elements for base-stations with multiple-input multiple-output (MIMO) capabilities. A suitable architecture to meet these requirements at the 28 GHz band was presented in Chapter 2 and is based on 4-channel transmit/receive chips with gain and phase control on each channel that are integrated with antennas on a PCB.

Fig. 3.1 presents the block diagram of a 4x4 element phased-array. The 2x2 TRX core chips are based on an all-RF beamforming architecture to achieve high-linearity and to enable the use of a low-cost PCB [14]. A transceiver chip is placed at the sum point of 16 elements to upconvert or downconvert the IF signal to the array common port. This is followed by a baseband processor to generate the modulated data, and may use the same waveforms and standards of 4G radios operating below 6 GHz.

In the TX mode, each array element radiates 11 dBm at P1dB with a gain of 22 dB per channel. Including 12 dB division loss to the 16 elements and 3 dB Wilkinson ohmic and line

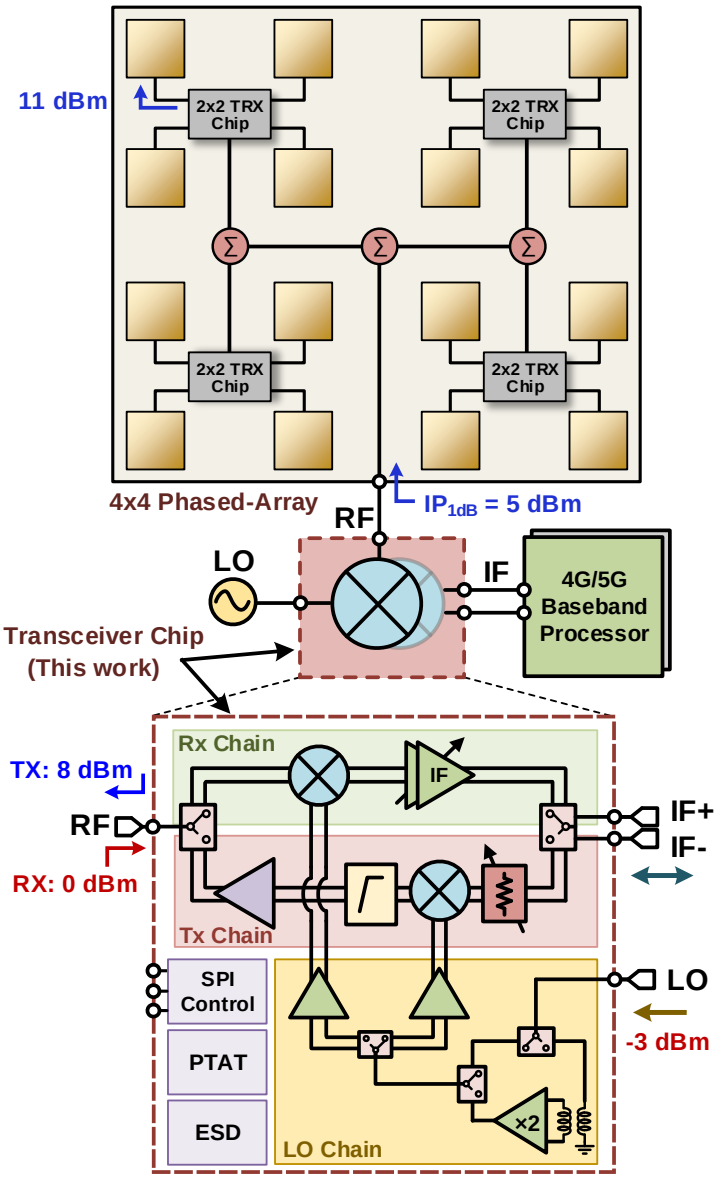


Figure 3.1: Block diagram of a 4x4 phased-array system and the transceiver chip.

loss on the PCB, the transceiver chip needs to deliver at least 5 dBm in TX mode to operate the 4x4 array at the P1dB level. In the RX mode, each channel has an IP1dB of −22 dBm and 18 dB gain. This results in an output power of 4 dBm at the array common port when 3 dB PCB losses and 12 dB signal addition from 16 channels are included. The 4x4 array OP1dB can be lowered to −10 dBm at the maximum received power using 14 dB gain control on each

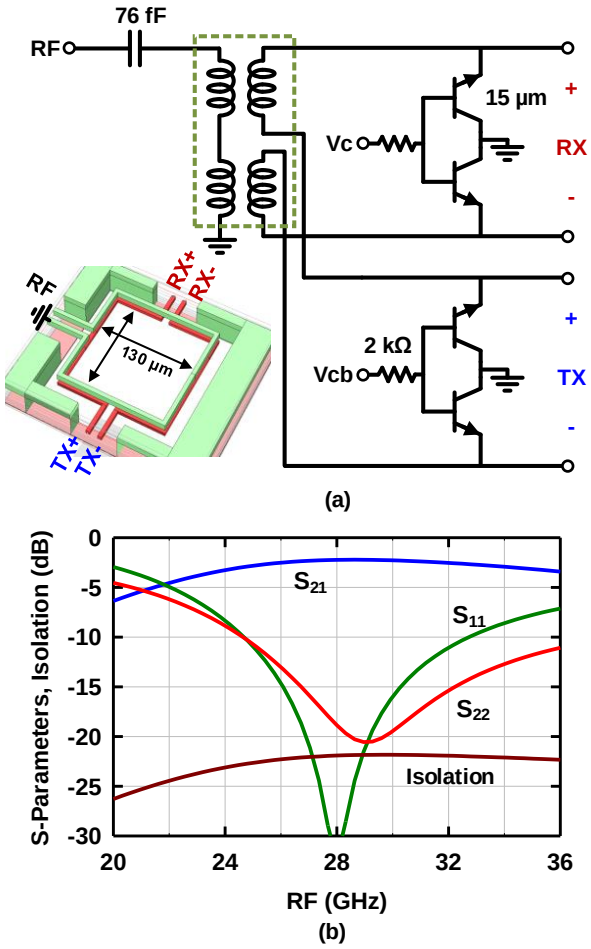


Figure 3.2: (a) Schematic of SPDT and balun combination. (b) Simulated S-parameters and isolation.

TRX channel. Still, the high output power in the TX mode and high-linearity requirement in the RX mode makes the architecture of the transceiver chip critical, so that it does not limit the system performance. The purpose of this work is to design a 28 GHz transceiver chip to meet the challenging requirements of a 5G phased-array system through the use of an asymmetric design in the TX and RX paths.

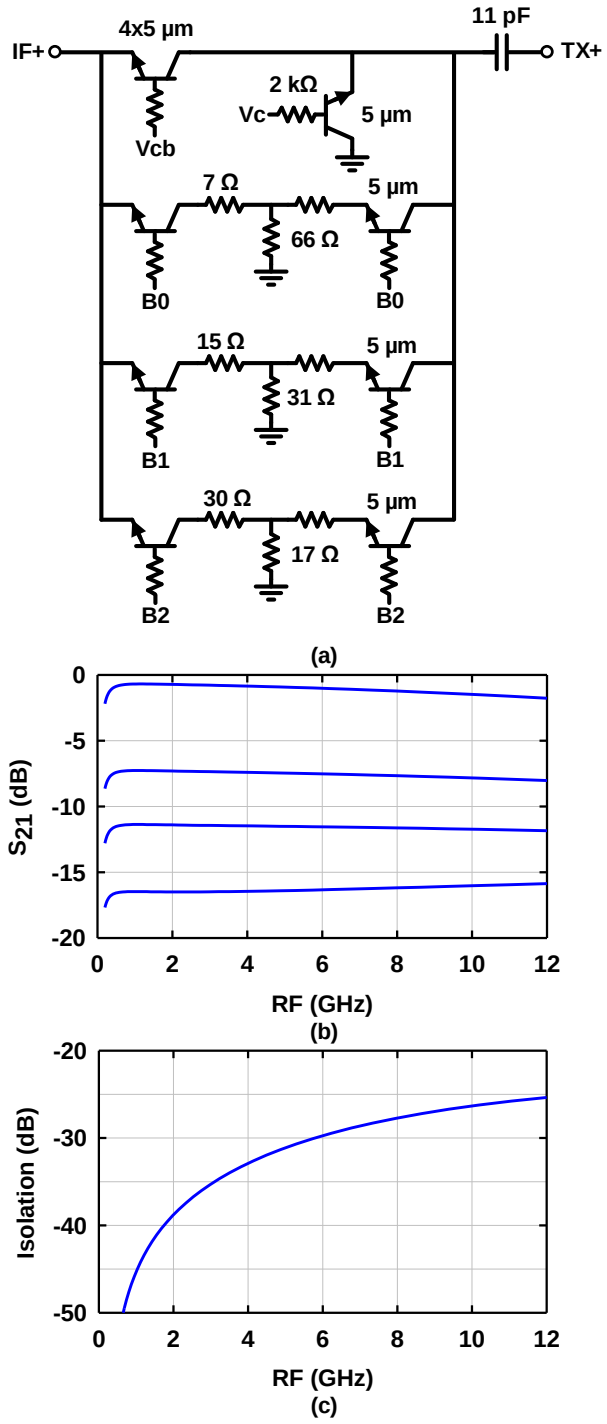


Figure 3.3: (a) Schematic of 2-bit step attenuator. Simulated (b) S-parameters and (c) isolation.

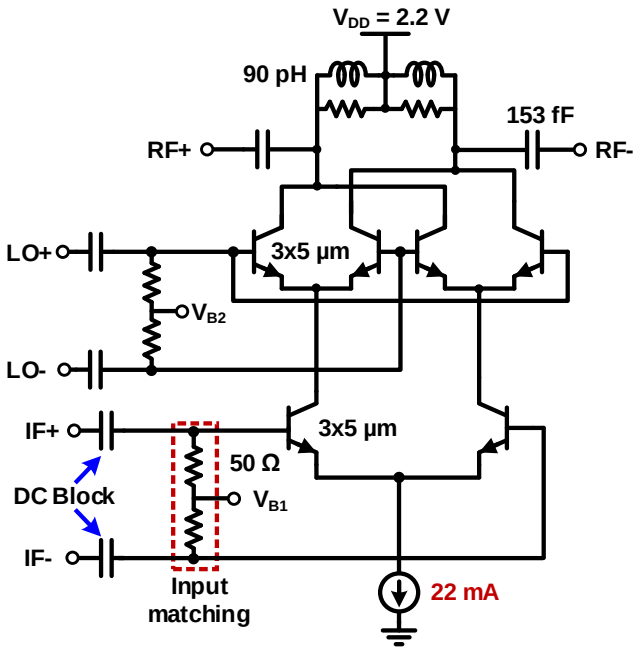


Figure 3.4: Schematic of active upconversion mixer.

3.2 Transceiver Circuit Design

The block diagram of the transceiver chip is presented in Fig. 3.1. Due to the relatively high output power requirement, active mixers are used in both TX and RX paths and are implemented using SiGe HBTs. All circuits are differential for stability and to avoid any degradation in performance due to packaging affects. An SPDT-balun combination [Fig. 3.2(a)] is used at the RF port to convert the signal to differential mode and to switch between the TX and RX modes. The design is based on [34], but uses reverse-saturated HBT switches for low insertion loss [20]. This design is particularly suitable for mm-wave frequencies since the transformer balun can be implemented using a single turn and very compact area. The SPDT-balun combo has 2.2 dB insertion loss at 28 GHz [Fig. 3.2(b)] which is lower than a separate single-ended SPDT (IL = 1.5 dB) and balun (IL = 1.1 dB).

3.2.1 TX Path

The TX path includes a 2-bit step attenuator [Fig. 3.3(a)] followed by a double-balanced active upconversion mixer (Fig. 3.4). The step attenuator is based on series-shunt HBT switches with pi-type matched attenuators with 1 dB insertion loss, 8/12/17 dB attenuation levels, isolation >25 dB, and with a 3 dB bandwidth >10 GHz [Fig. 3.3(b) and (c)]. Wideband matching at the upconversion mixer input is achieved using shunt 50 Ω biasing resistors. The image at LO-IF generated at the upconversion mixer output would compress the following PA, reducing its output power by 6 dB if it were not filtered out. To cancel the image, a 2-pole high-pass elliptic filter is implemented after the mixer [Fig. 3.5(a)]. The filter has a measured insertion loss of 2.2 dB at 29 GHz and provides >13 dB of filtering for the image and any LO leakage due to mismatches in the double-balanced mixer or coupling due to layout parasitics. For example, for an LO of 24.5 GHz and an IF of 4 GHz, the upconverted RF is at 28.5 GHz and the image is at 20.5 GHz. Both the LO and the image are greatly attenuated by the on-chip filter. This level of filtering is adequate since the image and LO will be further filtered by the 2x2 TRX core chips as well as the phased-array antenna elements. The group delay of the filter is ±6 ps at 28-32 GHz [Fig. 3.5(b)] and does not degrade the system EVM when used with modulated wideband signals. The filter is followed by a single-stage class-AB cascode power amplifier with 15 dB gain and 11 dBm OP1dB to deliver 8.5 dBm at the transceiver RF port.

3.2.2 RX Path

Unlike the TX path, the RX path does not require an image rejection filter since any signal at the image frequencies will already be filtered out by the antennas and the 2x2 TRX chips. Due to the high linearity requirement of the RX path, a mixer-first design is preferred after the RF switch. Since passive mixers have high conversion loss and high LO drive requirement (5-10 dBm), an active mixer is chosen for the downconversion path with a similar topology to the upconversion mixer (Fig. 3.4). The downconversion mixer employs inductive peaking at its

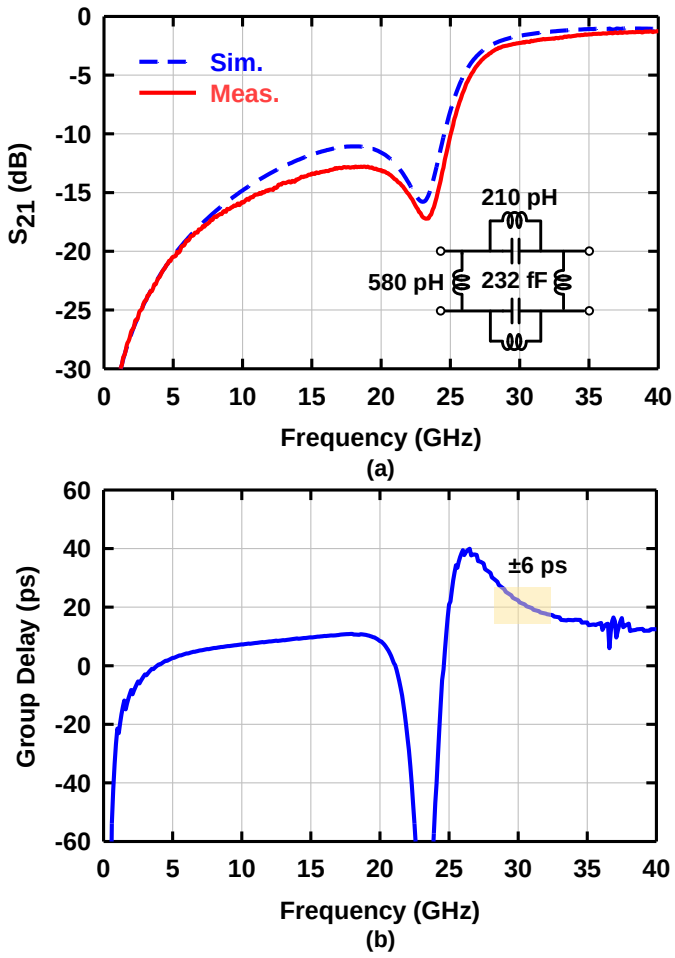


Figure 3.5: (a) Schematic and measured response of 2-pole elliptic high pass filter breakout to reject the image and LO leakage. (b) Measured group delay.

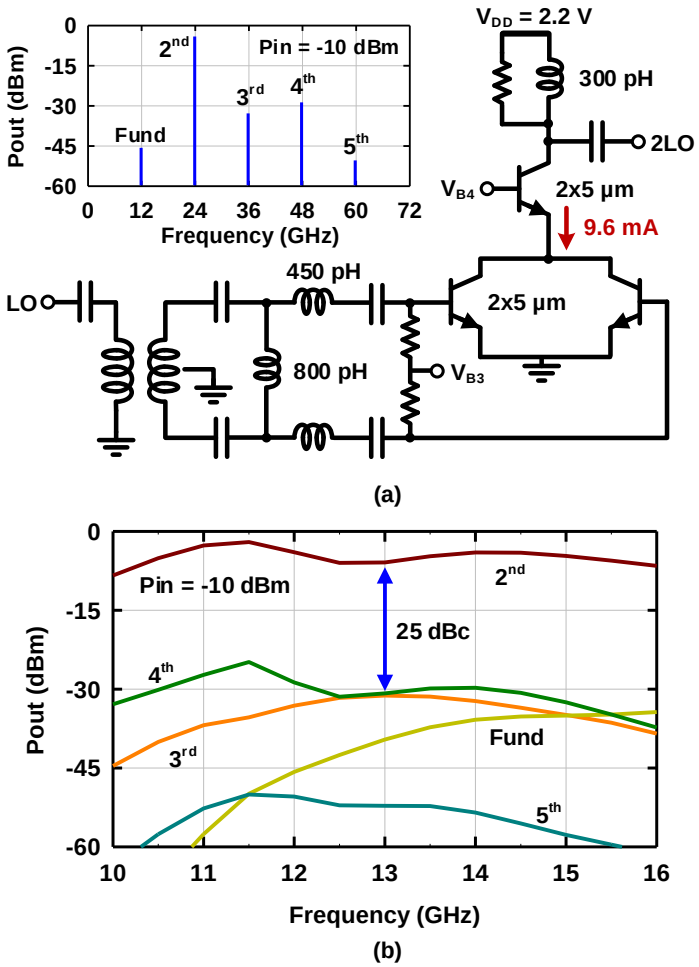


Figure 3.6: (a) Schematic of LO doubler and simulated output harmonics at 12 GHz input. (b) Simulated output harmonics at 10-16 GHz input.

load to widen the IF bandwidth. To improve the linearity further, the load resistance of the mixer can be switched between two values for medium-linearity and high-linearity modes. The high linearity mode results in 4 dB lower gain and 2 GHz wider IF bandwidth. The mixer is followed by a 2-stage IF amplifier with 3-bit 12 dB gain control on its second stage using current-steering at the cascode node [22]. A series-shunt switch provides isolation between the TX and RX paths at the IF port.

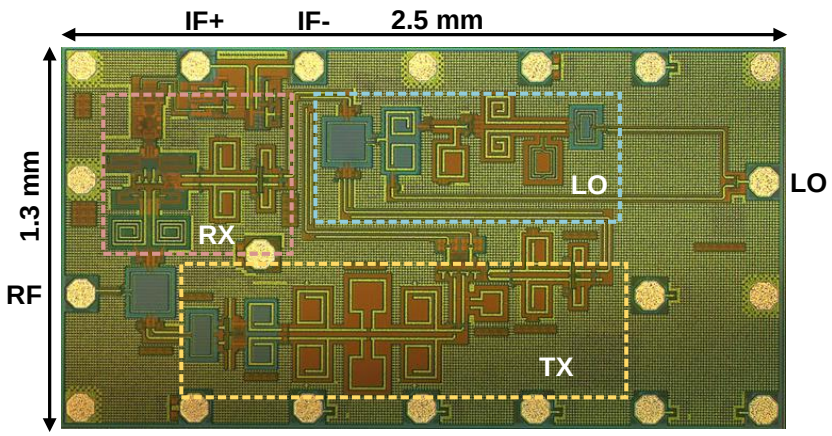


Figure 3.7: Transceiver chip photograph.

3.2.3 LO Path

The chip can operate with an LO input of 10-16 GHz or 20-28 GHz through the use of an on-chip doubler. A wideband series-shunt switch, again using reverse saturated HBTs, is employed in the LO path to bypass the doubler when an LO of 20-28 GHz is used. The doubler schematic and simulated output harmonics are shown in Fig. 3.6(a). At an input LO power of -10 dBm at 12 GHz, the doubler has a conversion gain of 6 dB and all harmonics are below -25 dBc. The output harmonics of the doubler are shown at an input of 10-16 GHz in Fig. 3.6(b), and the doubler provides wideband conversion gain at the 2nd harmonic with high rejection for the other harmonics. The doubler is followed by the same SPDT-balun combo at the RF port (Fig. 3.2) to convert its single-ended output to differential and to switch the LO between the RX and TX modes. A driver amplifier is used to deliver 0 to -5 dBm LO power to the active mixers.

3.3 Measurements

The chip was fabricated in the Jazz SBC18H3 SiGe BiCMOS process with a size of 1.3 x 2.5 mm^2 and a minimum pad spacing of 400 μm for chip-scale packaging (Fig. 3.7). All bias

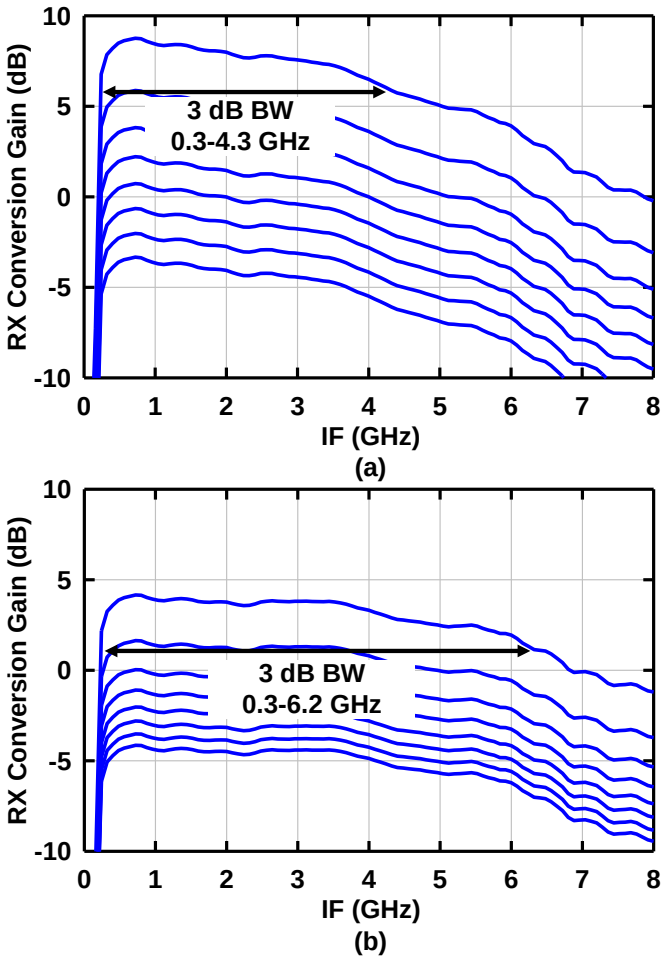


Figure 3.8: Measured RX conversion gain for (a) high-linearity and (b) medium-linearity modes with LO = 24 GHz.

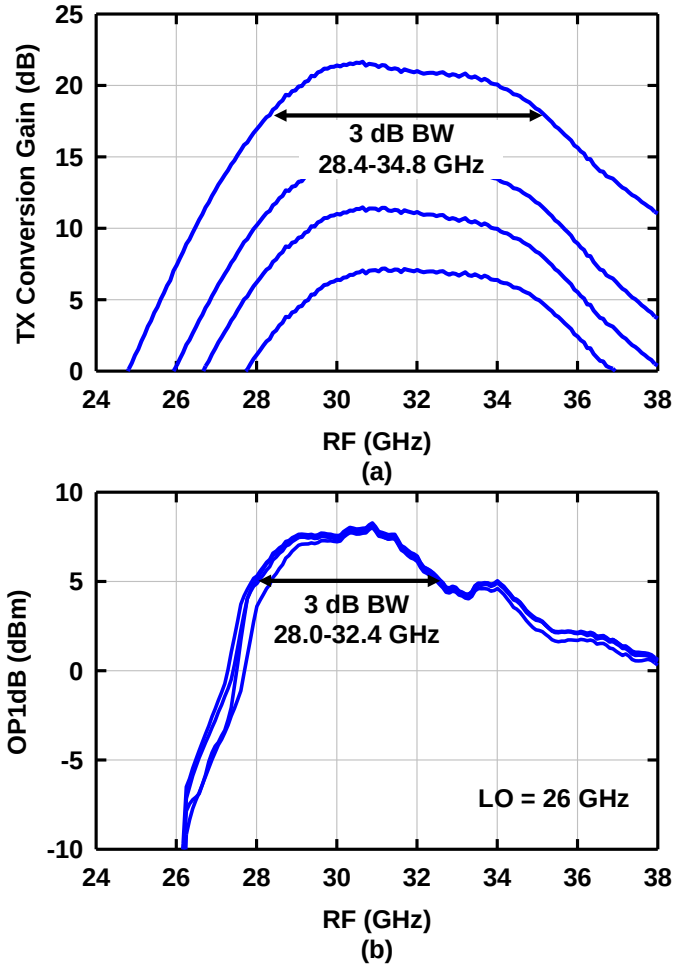


Figure 3.9: Measured (a) TX conversion gain and (b) TX OP1dB for all gain settings with LO = 24 GHz.

currents are generated on chip using a PTAT current generator and all dc pads are ESD protected. A serial interface is used for gain control, current control and RX linearity and doubler mode settings. A hardwire T/R switch pin is used for fast switching between the TX and RX modes.

The conversion gain, power, and noise figure measurements were done using a Keysight PNA-X with the dc and IF ports bonded to a PCB and the LO and RF ports probed. The measured RX mode conversion gain is shown in Fig. 3.8(a) versus IF with a fixed LO input of 12 GHz for the medium-linearity mode. The maximum gain is 9 dB with a 3 dB bandwidth of 0.3-4.3 GHz. In the high-linearity mode, the RX mixer gain is reduced, and the measured peak gain is 4.5 dB with a 3 dB bandwidth of 0.3-6.2 GHz [Fig. 3.8(b)].

In TX mode, the conversion gain is shown in Fig. 3.9(a) at an LO = 12 GHz and shows a maximum gain of 21 dB and 15 dB gain control. TX OP1dB remains constant for all attenuation settings with a peak OP1dB of 8.5 dBm and 3 dB RF bandwidth of 28.0-32.4 GHz [Fig. 3.9(b)]. The results without the doubler option are identical and not shown.

Fig. 3.10(a) presents the measured TX OP1dB at a fixed RF of 30 GHz with the IF and LO swept together. The chip can deliver $>$7 dBm OP1dB at an IF of 1.5-7.5 GHz. Below 1.5 GHz IF, the output power drops since the image is not filtered out by the elliptic filter and compresses the PA. The measured IP1dB in RX mode is shown in Fig. 3.10(a) at a fixed LO of 24 GHz. The chip can achieve IP1dB as high as 0 dBm to meet the requirements of short distance phased-array links with high received power. The measured DSB NF in the RX mode is 13 dB in the medium-linearity mode and 15 dB in the high-linearity mode at an IF of 2 GHz [Fig. 3.10(b)]. The measured LO leakage is <-40 dBc for LO $<$25 GHz due to the on-chip elliptic filter [Fig. 3.10(c)].

The chip was tested with all ports bonded to a PCB in the TX mode using an 802.11ad MCS-10 modulated signal with 1.8 GHz bandwidth and 6 dB PAPR, at an IF of 4.7 GHz and an LO of 24 GHz. The measured constellation and spectrum are shown in Fig. 3.11. The chip meets the spectral mask requirements of 802.11ad with 3 Gbps physical rate at 4 dB backoff with 3.9% (-28.2 dB) EVM. The chip performance is summarized on Table 3.1.

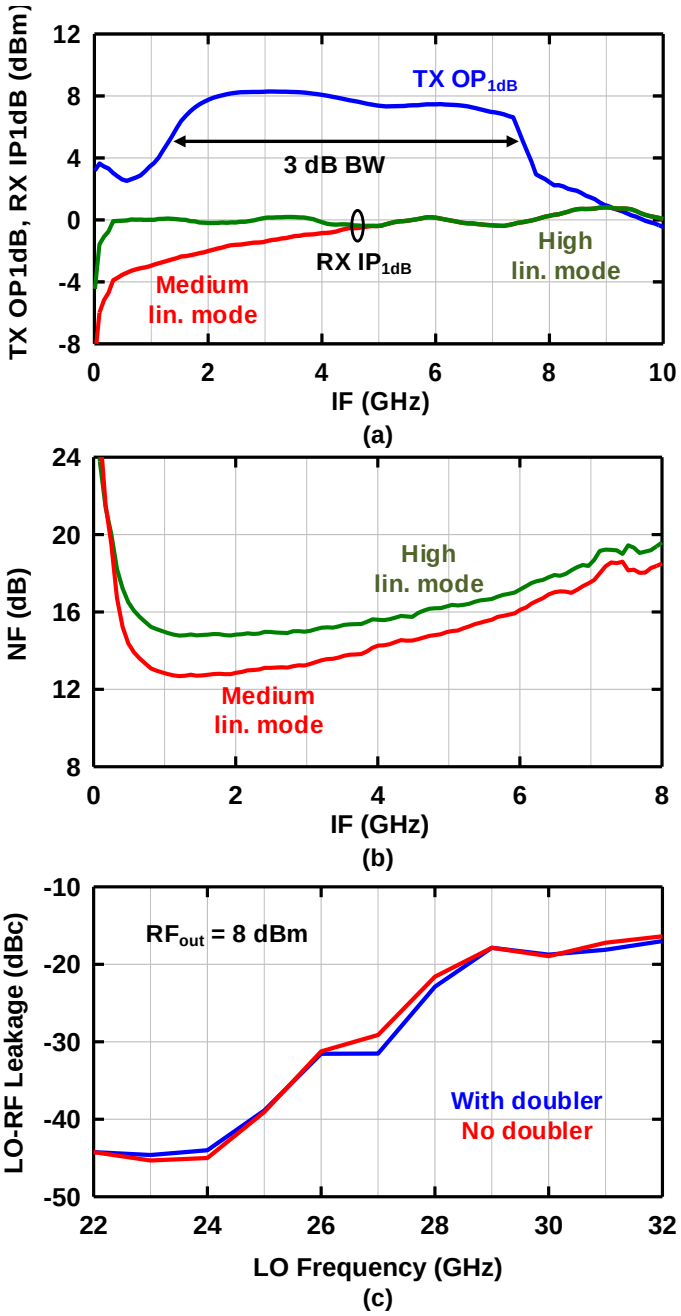


Figure 3.10: Measured (a) TX OP1dB, RF IP1dB in high-linearity and medium-linearity modes, (b) RX NF and (c) LO-RF leakage in TX mode with and without doubler in the LO path.

3.4 Conclusion

This chapter demonstrates a 28-32 GHz transceiver chip in SiGe BiCMOS. A 5G phased-array communication link will be demonstrated using this transceiver chip and a 4x16 element

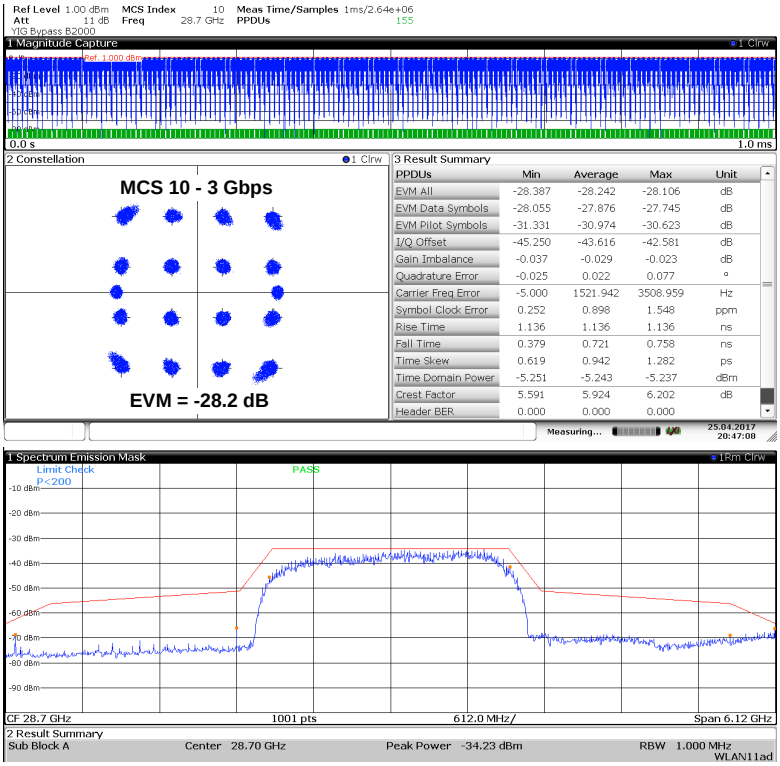


Figure 3.11: Measured constellation and spectrum with 802.11ad MCS-10 waveform with 3 Gbps data rate and 3.9% EVM.

phased-array in a MIMO configuration.

3.5 Acknowledgment

Chapter 3, in part, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer and G. M. Rebeiz, "A 28 GHz Transceiver Chip for 5G Beamforming Data Links in SiGe BiCMOS," *IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM)*, October 2017. The dissertation author was the primary investigator and author of this paper.

Table 3.1: Transceiver Chip Performance Summary

Parameter	**RX**	**TX**
Gain (dB)	9 / 4.5	21 / 7
NF (dB)	13 / 15	-
3 dB IF BW (GHz)	0.3-4.3 / 0.3-6.2	0.3-4.8
IF gain control (dB)	12 (3-bit)	-1 / -8 / -12 / -17 (2-bit)
IP1dB (dBm)	-3 / 0	-11.5 / 2.5
OP1dB (dBm)	5 / 3.5	8.5
LO range (GHz)	10-16 / 20-28	10-16 / 20-28
LO power (dBm)	-5 to 0	-5 to 0
Power consumption (mW)	290	260

Chapter 4

64-Element (8×8) Phased-Arrays

4.1 Introduction

The development of highly-integrated and high-performance phased-arrays in silicon technologies over the last decade has enabled their commercial use in fifth-generation (5G) communications at millimeter-waves in the coming years [1,4,6,11,13,35–42]. To deliver Gbps data to multiple users with low latency, 5G base stations and user equipment will rely on directive communications to overcome the increased path loss. These phased-arrays need to be placed every several hundred meters to provide enough coverage and capacity, and therefore, this requires the development of low-cost phased-array solutions for customer premise equipment (CPE) and base stations.

To date, there have been several demonstrations of mm-wave phased-array communication links at short distances [6, 37, 39] and at 100-300 meters with data rates on the order of 1-2 Gbps in a single beam [4, 42, 43]. The data rates achieved so far fall short of 10 Gbps promised by 5G links. In this chapter, a 64-element (8x8) 28 GHz phased-array transceiver is presented with a focus on system level requirements such as effective isotropic radiated power (EIRP) and bandwidth, amplitude and phase mismatch between the elements, LO and image rejection, and transmit noise to achieve $>$ 10 Gbps data links using 16-/64-QAM waveforms at

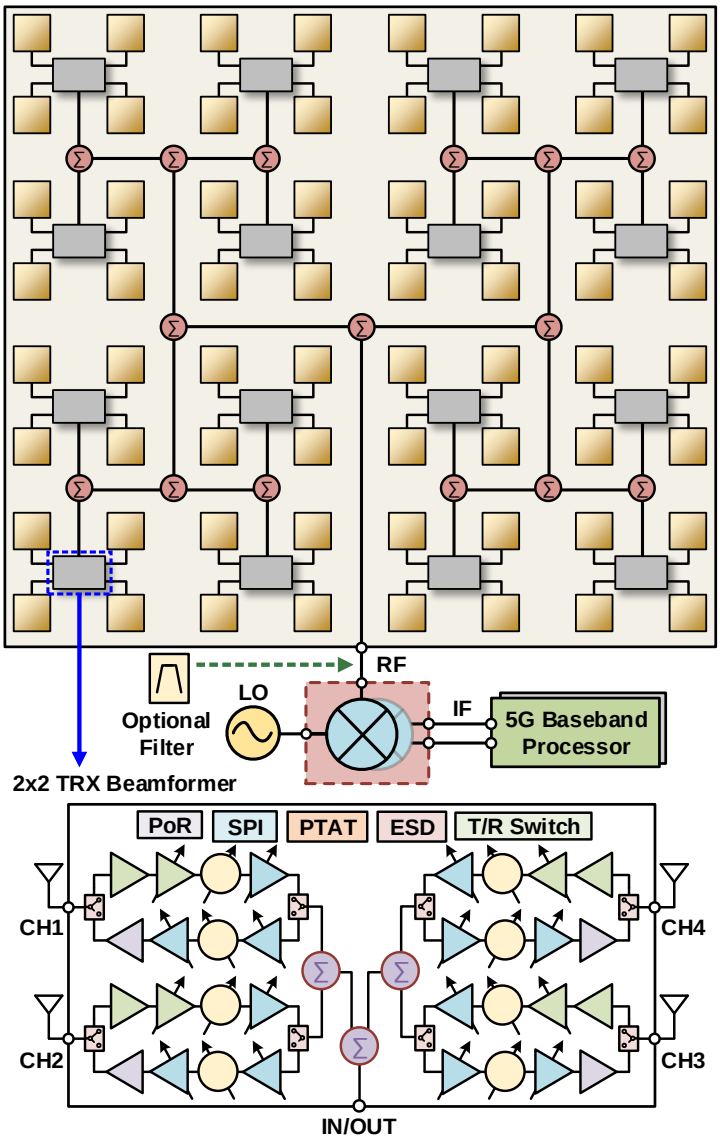


Figure 4.1: Scalable 64-element 5G phased-array architecture based on 2x2 TRX beamformer chips.

300 meters. Section 4.2 discusses the system architecture and the effect of random phase and amplitude errors in large phased-array. Section 4.3 presents the design of a 64-element array based on 2x2 transmit/receive (TRX) beamformer chips. System measurements are presented in Section 4.4, link measurements are presented in Section 4.5 and Section 4.6 concludes the chapter.

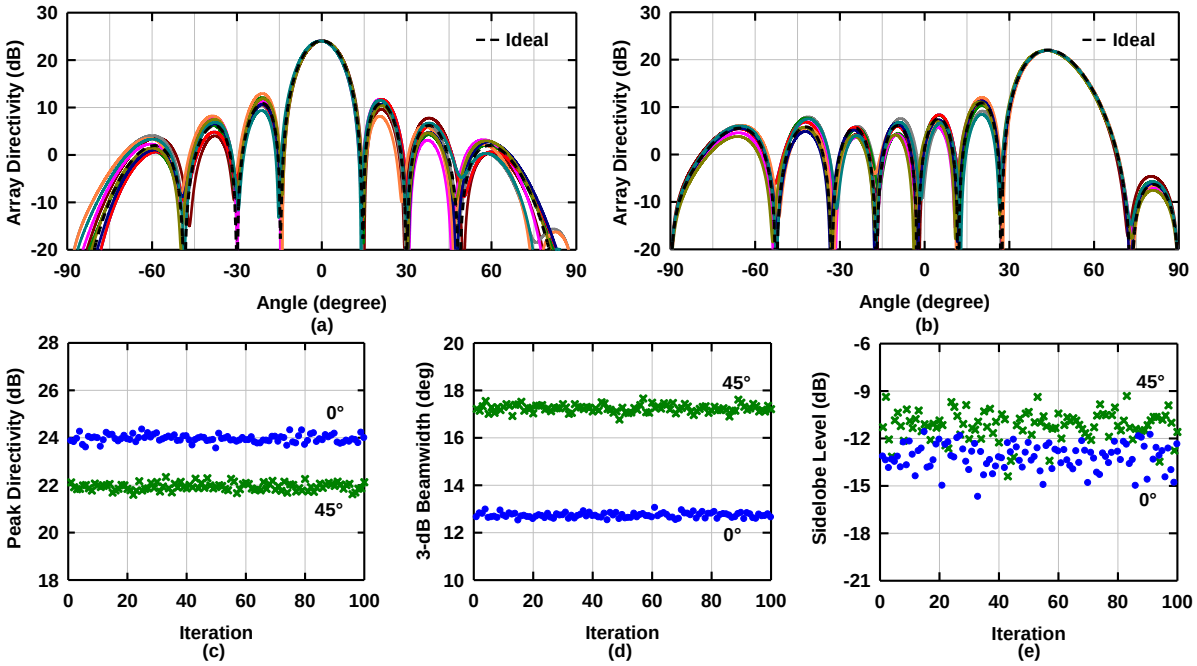


Figure 4.2: Simulated H-plane patterns at (a) 0° and (b) 45° with random ±2 dB gain and ±20° phase errors for 10 iterations. Simulated (c) peak antenna directivity, (d) 3-dB beamwidth and (e) first sidelobe level for 100 iterations.

4.2 Amplitude and Phase Error Effects on 64-Element (8×8) Phased-Arrays

Fig. 4.1 presents the 28 GHz phased-array architecture employed in this work and the advantages of this architecture were discussed in detail in [42]. The design is based on 2x2 TRX beamformer chips which are assembled on one side of a printed circuit board (PCB) with the antennas placed on the other side and can be scaled to any size depending on the system requirements. The common ports of sixteen 2x2 TRX chips are combined at RF using a Wilkinson network on the PCB and a transceiver chip (e.g. [44]) is placed at the common port for up/down conversion to an IF or baseband.

Traditionally, one of the main phased-array cost drivers was calibration and test, since the variation between the antenna elements when using GaAs phased-array T/R modules with different PCB line lengths could add up to as much as ±4 dB and ±180°. Also, the yield

of the T/R modules was not very high (93-96%), which necessitated each T/R module to first be individually tested before insertion into the phased-array. After assembly, the phased-array was calibrated by turning on each T/R module individually, and measuring the gain and phase response of each element from the common port to the far-field. These calibration coefficients (variations in gain and phase response) were also measured at several temperatures, and then loaded into the phased-array controller to determine the offsets needed for each element. A calibration accuracy of $\pm$0.25-0.5 dB and $\pm$3-6° could be achieved, but this added a lot of cost to each phased-array.

The use of silicon beamformer chips with flip-chip [or ball grid array (BGA)] packaging, PCB-based phased-arrays with printed antennas and without any connectors, symmetrical PCB-based Wilkinson distribution networks, and the use of proportional to absolute temperature (PTAT) biasing on each silicon chip for accurate amplitude and phase control over temperature can result in 5G phased-arrays without the need for any calibration [39,42,45,46]. While there is some chip-to-chip variation and the Wilkinson network is not ideal, it is possible to build phased-arrays with a peak amplitude error of $\pm$2 dB (rms error of 1 dB) and a peak phase error of $\pm$18° (rms error of 9°). Fig. 4.2 presents the simulated patterns for an 8x8 phased-array spaced at 0.5λ x 0.63λ with uniform illumination, an element factor of $\cos^{1.4}(\theta)$ and such random errors on its aperture (100 simulations with 100 different random error profiles). The averaging effects of the phased-arrays are clearly seen with minimal changes in the directivity and 3-dB beamwidth [Fig. 4.2(c) and (d)]. The sidelobe level changes by $\pm$1.6 dB from the ideal value of $-$13.3 dB [Fig. 4.2(e)]. The averaging effects also apply at all scan angles, and the patterns at 45° scan angle are shown in Fig. 4.2(b). A 6-dB raised-cosine distribution without calibration can still achieve $-$20 dB sidelobes, but with $\pm$2 dB sidelobe variation with these random errors.

For completeness, the effect of random gain and phase errors have been derived before

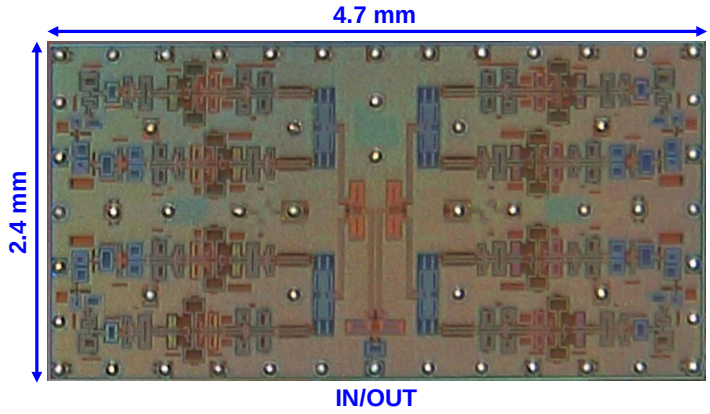


Figure 4.3: 2x2 TRX beamformer chip photograph.

by Ruze [47], Mailloux [48] and Allen [49], and are given by [50]:

$$\frac{D}{D_0} = \frac{1}{1+\sigma^2} \tag{4.1}$$

$$SLL^2 = SLL_0^2(1+\frac{\sigma^2}{D_0 SLL_0^2}) \tag{4.2}$$

$$\sigma^2 = (\sigma_a - 1)^2 + \sigma_p^2 \tag{4.3}$$

where D_0 is the error-free directivity, SLL_0 is the design sidelobe level, σ_a is the rms amplitude error and σ_p is the rms phase error in radians. Note that large arrays with a high D_0 result in a reduced sidelobe level error. In the case above with 8x8 arrays and σ_a = 1 dB (1.122) and σ_p = 9° (0.157 radians), the gain reduces by 0.17 dB for both uniform illumination and 6-dB raised-cosine taper.

4.3 64-Element (8×8) Phased-Array Design

4.3.1 2×2 TRX Beamformer Chip

The block diagram of the 2x2 TRX beamformer chip is shown in Fig. 4.1. The 2x2 chip contains four TRX channels and a Wilkinson combiner/divider network. Each channel contains single-pole double-throw switches (SPDTs), a low noise amplifier (LNA), a power amplifier

Table 4.1: Measured 2x2 TRX Beamformer Performance

Parameter	**RX Mode**	**TX Mode**
Gain (dB)	19	19
3-dB Bandwidth (GHz)	28-34	29-35
NF (dB)	4.8	11
IP_{1dB} (dBm)	-21	-6
OP_{1dB} (dBm)	-3	11-12
Phase step (°)	5.6	5.6
RMS phase error (°)	2.9-5.5	4.3-6.1
RMS gain error (dB)	0.4-0.7	0.6-0.8
Gain control (dB)	26	20
P_{DC} / ch. (mW)	150	220 @ P1dB

(PA), variable gain amplifiers (VGAs) and 6-bit phase shifters. All circuits are differential except for the first LNA stage and the SPDT at the antenna port to maintain stability and high isolation when the chip is flipped on a PCB. The chip is controlled using a serial peripheral interface (SPI) for gain, phase and bias current settings. A hardwire T/R switch is used to enable fast switching (50-100 ns) between the transmit (TX) and receive (RX) modes. The SPI includes an enable pin which allows the user to pre-load the phase and gain states for each channel, and allows the beam to remain fixed while the next beam state is loaded onto the chip. A power-on-reset (PoR) circuit is also included to set the initial states of all registers to zero when the chip is powered up. All pads are electrostatic discharge (ESD) protected and the chip operates from two supplies of 1.2 V and 2.2 V. All bias currents are generated using an on-chip PTAT current generator.

The 2x2 beamformer chip was fabricated in the TowerJazz SBC18H3 SiGe BiCMOS process with 400 μm pitch bump so that it can be directly flipped on a PCB without a multi-layer laminate interposer (Fig. 4.3). The measured chip performance is summarized in Table 4.1. In the RX mode, each channel has 19 dB peak gain [Fig. 4.4(a)], 4.8 dB noise figure (NF) [Fig. 4.4(c)], an input 1-dB compression point (IP1dB) of -21 dBm and consumes 150 mW. In

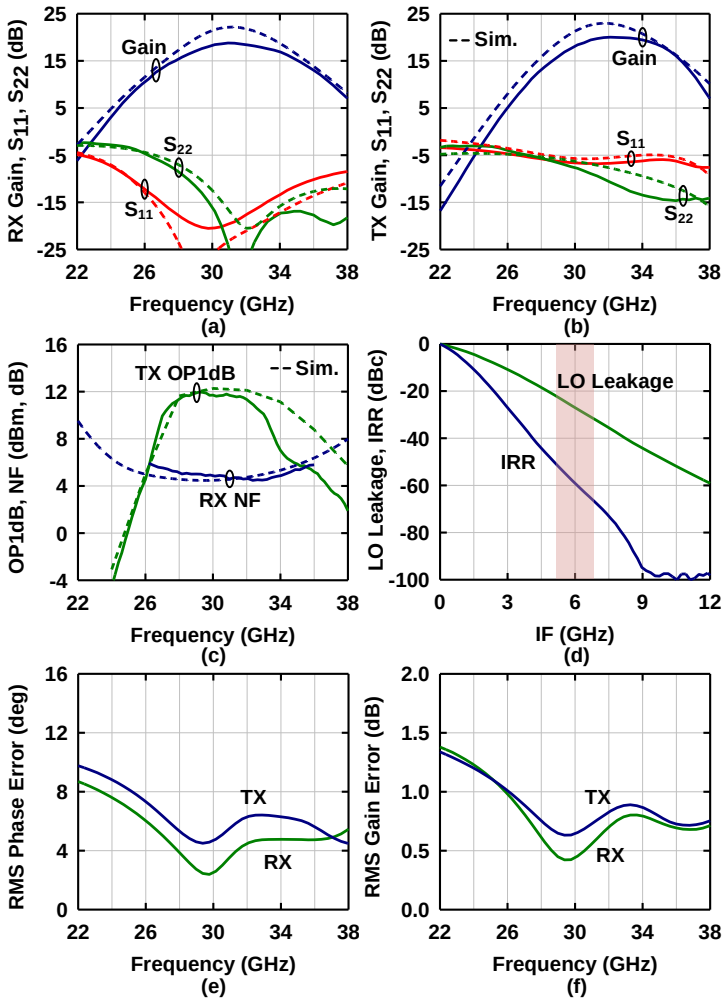


Figure 4.4: Measured 2x2 beamformer chip S-parameters in the (a) RX mode, (b) TX mode, (c) RX NF and TX OP1dB, (d) LO leakage and IRR in the TX mode, (e) rms phase error, (f) rms gain error.

the TX mode, each channel has 20 dB peak gain including 6 dB division loss to four channels [Fig. 4.4(b)], 11-12 dBm output 1-dB compression point (OP1dB) [Fig. 4.4(c)] and consumes 220 mW at the OP1dB level. The chip gain in both TX and RX modes is defined from the antenna port (port 1) to the common port (port 2) and includes 2.2 dB on-chip Wilkinson network ohmic loss. Note that the RX dc power consumption is high due to the high IP1dB, and each channel has an electronic gain of 21 dB to result in a chip gain of 19 dB.

Since the 2x2 TRX chip response is relatively narrowband (16-18% fractional band-

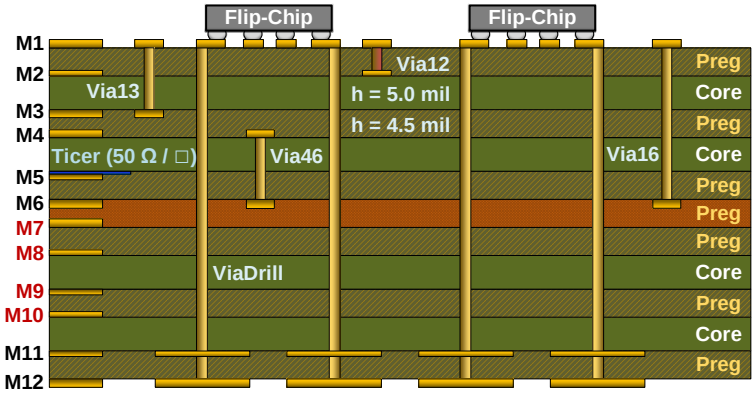


Figure 4.5: 12-layer PCB stackup with wideband antennas and embedded resistive layer for the Wilkinson beamformer network.

width), it can provide significant rejection at the LO and image frequencies. Fig. 4.4(d) presents the LO leakage suppression and image rejection ratio (IRR) at different IF choices for low-side injection in the TX mode for RF = 29 GHz. For IF = 6 GHz, the chip provides 27 dBc LO suppression at 23 GHz and 60 dBc IRR at 17 GHz. Additional rejection is provided by the antenna elements as presented in the next section.

For link measurements in Section 4.5, the IF was chosen as 6 GHz and the optional filter on the PCB was not included (see Fig. 4.1) since the LO and image rejection levels are high enough not to affect the link performance. However, depending on the out-of-band emission requirements and the IF choice, the optional high-pass filter can be implemented on the PCB with a Q of 100-150 at the 8x8 array common port and can provide additional LO and image suppression with low loss ($<$ 1 dB).

The measured phase shifter rms phase and gain errors for 64 phase states (6-bit operation) are presented in Fig. 4.4(e) and (f) for both TX and RX modes. The rms phase and gain errors are 2.9-5.5° and 0.4-0.7 dB in the RX mode and 4.3-6.1° and 0.6-0.8 dB in the TX mode at 28-32 GHz, respectively. The 2x2 beamformer chip achieves 5-bit accuracy over a wide frequency range.

4.3.2 Stacked-Patch Antenna and 12-Layer PCB Design

Fig. 4.5 presents the PCB stackup employed for the 64-element phased-array. The PCB alternates Panasonic Megtron-6 (ϵ_r = 3.26-3.37, $\tan\delta$ = 0.005 at 29 GHz) core and prepreg layers with 4.5-5.0 mil thicknesses in a fully symmetric design for improved fabrication yield. The chips are placed on M1, and the antenna ports on M1 are connected to the patch antennas on M11 using a via feed (ViaDrill). A parasitic patch is included on M12 to improve the antenna bandwidth and efficiency. There is no metal on M7-M10, but these layers are included to increase the antenna bandwidth and to maintain symmetry for the PCB stackup. M1-M4 are used for digital routing and supply distribution.

The microstrip antenna is a stacked-patch design on a 0.5λ x 0.63λ grid (f_0 = 30 GHz), and was simulated together with the feed line from M1-M11 using Ansys HFSS and master/slave boundary conditions [51]. The matching network from the coaxial feed on M1 to the chip antenna port was designed using Agilent ADS, and the complete simulation setup including the bump model used for the flipped die is shown in Fig. 4.6(a). The signal and ground bumps were modeled in HFSS with an equivalent 140 pH series inductance, 60 mΩ series resistance and 19 fF shunt capacitance on both ports. An additional 29 fF capacitance is included on the chip side to model the pad capacitance.

The 3-D antenna model is shown in Fig. 4.6(b). Note that an opening is included on the M12 parasitic patch and the via feed only connects to M11. M1-M6 is designed as a coaxial transition with grounded vias around the feed line. The coaxial transition was designed with a characteristic impedance of 27 Ω for improved antenna bandwidth and optimized to realize a real impedance looking into the antenna feed from M1.

A matching network is designed on M1 to present 50 Ω to the chip antenna port [Fig. 4.6(a)]. The matching network also includes a $\lambda/4$ shunt stub to provide additional ESD protection at the chip antenna ports. The simulated antenna S_{11} remains <-10 dB at 28-32 GHz over most scan angles [Fig. 4.6(c)]. The simulated antenna, feed line and matching network ohmic losses up to the chip bump are 0.8-1.3 dB for 0-20° scan in the E-plane [Fig. 4.6(d)] and 0-50°

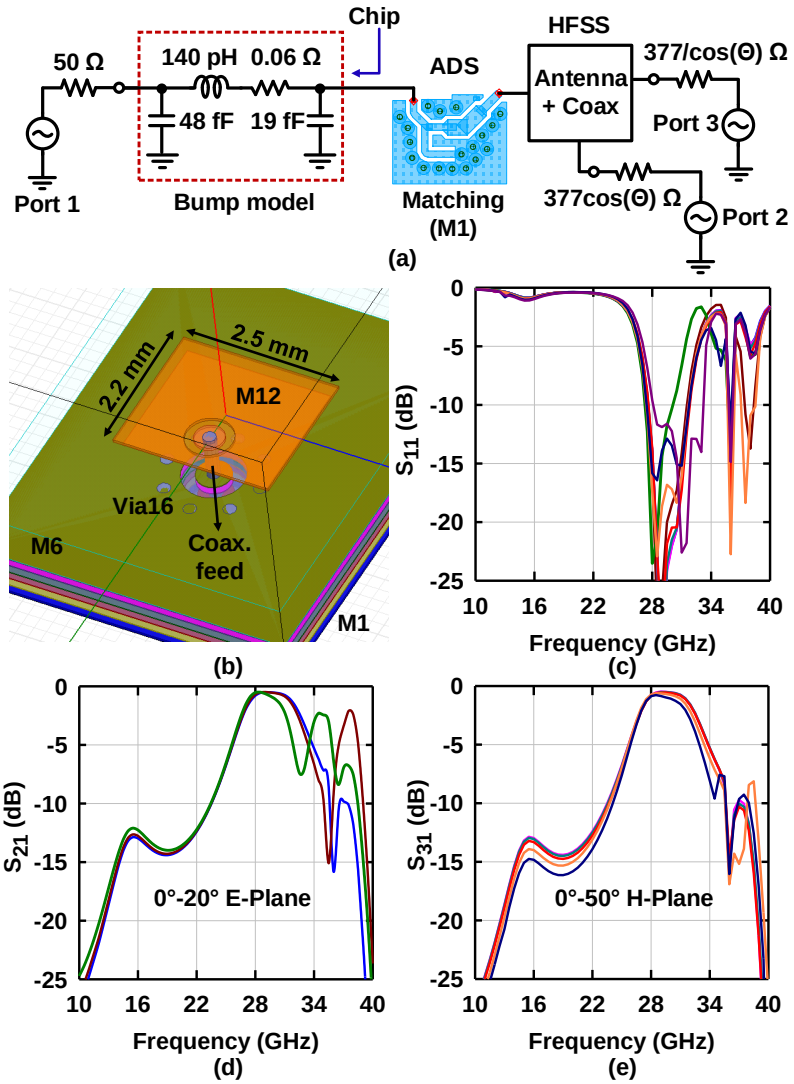


Figure 4.6: (a) Antenna simulation setup. (b) Stacked-patch antenna design. Simulated (c) matching, (d) S_{21} and (e) S_{31} over all scan angles.

scan in the H-plane [Fig. 4.6(e)]. The antenna response also provides an additional 10-11 dB rejection for the LO at 23 GHz and 13-15 dB rejection for the image at 17 GHz.

The Wilkinson combiner/divider network to sixteen chips on the PCB is built using M5 in stripline configuration with ground planes on M4 and M6. This minimizes any radiation or direct coupling to the antenna feeds. The Wilkinson beamformer is designed with a characteristic impedance of 32 Ω and an embedded resistive layer (50 Ω / □ Ticer [52]) is employed on M5 to provide the 64 Ω resistors for isolation. The Wilkinson network is simulated in HFSS including

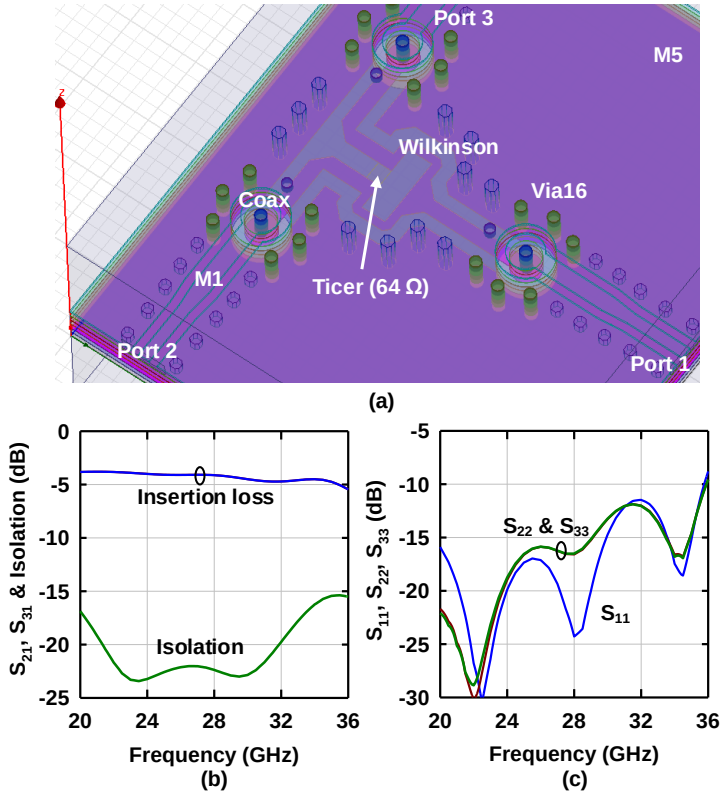


Figure 4.7: (a) Wilkinson combiner/divider design on M5 with embedded resistive layer. Simulated (b) insertion loss and isolation, (c) matching including coaxial transitions from M1 to M5 and chip bump models on ports 2 & 3.

Table 4.2: 5G TRX Array Parameters

Number of elements, N		64 (8x8)	
Antenna S_{11} bandwidth (GHz)		28-32	
Antenna spacing, d_x / d_y (mm)		5 / 6.3	
Feed + antenna ohmic loss (dB)		1.5	
Antenna gain, G_{TRX} (dB)		22.5	
PCB Beamformer ohmic loss (dB)		6	
RX Mode		**TX Mode**	
Chip NF (dB)	4.8	Channel NF (dB)	11
System NF (dB)	5.5-6.7	Output noise / ch. (dBm/Hz)	-136
IP_{1dB} / ch. (dBm)	-21	Array IP1dB (dBm)	12
Array OP_{1dB} (dBm)	9	EIRP @ P1dB (dBm)	51-52

the coaxial transitions from the chip common port on M1 to M5 [Fig. 4.7(a)] and chip bump models on ports 2 and 3. Via16 is used to connect M1 to M5 which results in a short stub between M5-M6 and this was taken into account for the coaxial transition design. The simulated insertion loss including the 3-dB Wilkinson power split, two coaxial transitions and the chip bump is $\sim$4 dB with an isolation $>$ 20 dB [Fig. 4.7(b)]. The Wilkinson is well matched on all ports [Fig. 4.7(c)].

The 2x2 unit cell with the flipped die is shown in Fig. 4.8, and a simplified model of the unit cell is used to simulate port-to-port coupling on the PCB. Grounding vias (Via12) are used around all feed lines to improve the isolation to avoid additional phase and gain errors due to port-to-port coupling [53]. The worst-case coupling is S_{17} or S_{26}, where energy from antenna 1 (or antenna 2) is fed to the adjacent port. The simulated coupling remains <-40 dB over the bandwidth of operation (Fig. 4.8). Note that the design is perfectly symmetrical with equal-length lines between the chip ports and the antenna ports. The simulated insertion loss, S_{72}, between the antenna feed and the chip is 0.25-0.4 dB at 27-34 GHz.

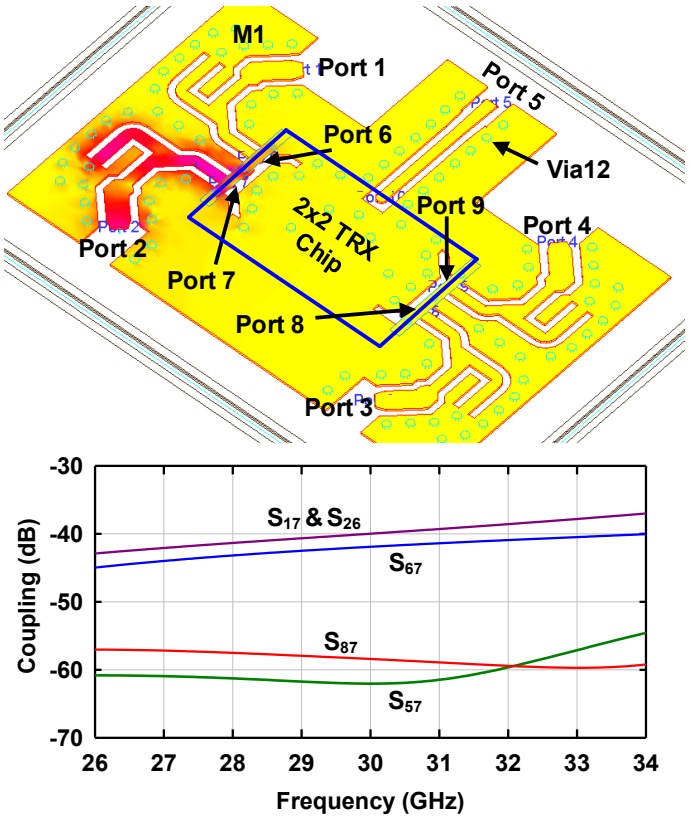


Figure 4.8: Simulated port-to-port coupling on the PCB. Ports 1-4 are the antenna ports, and ports 6-9 are the chip ports. Port 5 is the common port on the PCB.

4.3.3 64-Element TRX Array Specifications

The performance of the 64-element array built using sixteen 2x2 TRX beamformer chips can be calculated as in [42] and is summarized in Table 4.2. The 64-element transmit/receive antenna results in an antenna gain G_{TRX} of 22.5 dB when the feed line and antenna ohmic and mismatch losses (1-1.3 dB) are taken into account. The Wilkinson divider/combiner network on the PCB results in 6 dB ohmic loss including all transmission lines up to the coaxial connector.

In the RX mode, the channel IP1dB is -21 dBm which results in an array OP1dB of 9 dBm at the coaxial port when the PCB combiner ohmic loss (6 dB) and signal addition from 64 channels (18 dB) are included. Therefore, a high-linearity transceiver is required at the array sum point. The chip NF is 4.8 dB which results in a system NF of 5.5-6.7 dB when a high-linearity transceiver with 10-15 dB NF is used at the sum port.

In the TX mode, the IP1dB for each chip is -6 dBm which results in an IP1dB of 12 dBm for the 64-element array at the coaxial connector when the divider ohmic loss (6 dB) and the division loss to 16 chips (12 dB) are taken into account. The OP1dB per element is 11-12 dBm at the chip antenna port which results in an EIRP of 51-52 dBm for the 64-element array at P1dB.

4.4 System Measurements

Fig. 4.9 presents the top and bottom views of the assembled 64-element 5G phased-array with vertical polarization. Note that the Wilkinson network is laid out in a perfectly symmetrical fashion from the coaxial port to each of the sixteen different chip common ports. Also, the connections between the chip ports and the antenna ports are symmetrical and equal length. Therefore, by design, there is no electrical length variation between the coaxial port and each antenna radiation port. An array of dummy antennas surrounds the 8x8 array for improved antenna impedance at large scan angles.

The array was first measured in the TX mode using a vector network analyzer (VNA)

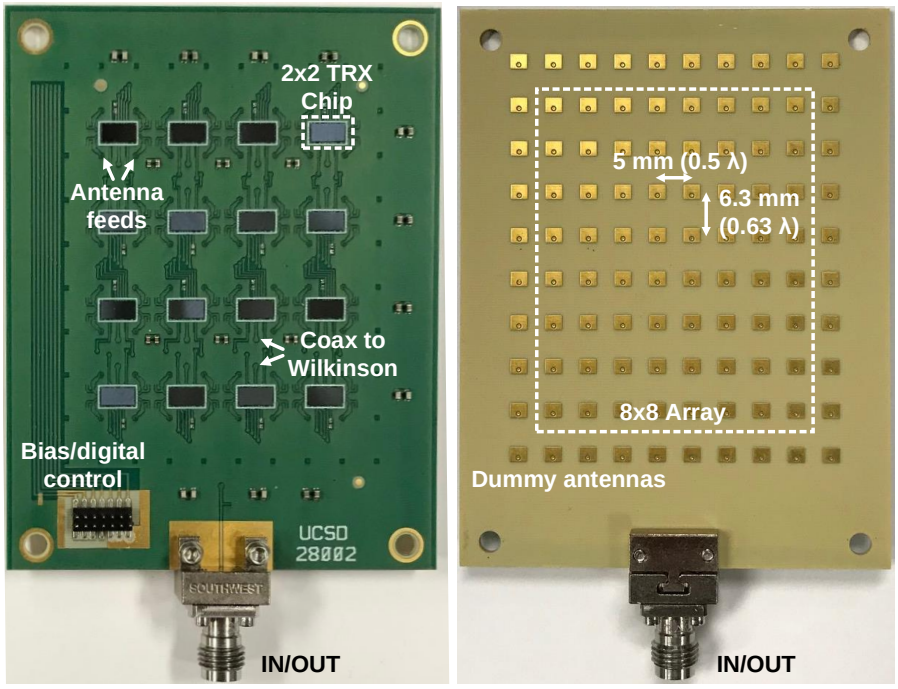


Figure 4.9: Top and bottom views of the 64-element array PCB with flip-chip beamformer ICs and PCB integrated stacked-patch antennas.

with a standard gain horn antenna as the receiver in the far field. Each element was turned on individually with a phase setting of 0° and the same nominal gain setting using the SPI control, and the normalized measured gain and phase of each element is shown in Fig. 4.10. A peak gain difference of ±2 dB and phase difference of ±20° was measured between the elements at 29 GHz with rms values of 1.1 dB and 8.9°. This gain and phase difference takes into account any non-idealities in the Wilkinson network, chip-to-chip variations and any mechanical mounting errors (a shift of ±100 μm results in ±6° at 30 GHz). The gain and phase difference can easily be calibrated using the 6-bit phase shifters and VGAs on each channel, but this was not done since the analysis in Section 4.2 has shown that the impact on the array performance is negligible.

4.4.1 Pattern and EIRP Measurements

Fig. 4.11(a) presents the measured H-plane pattern (azimuth plane) with the array pointing at boresight in the RX mode. All pattern measurements are presented at 29 GHz since this

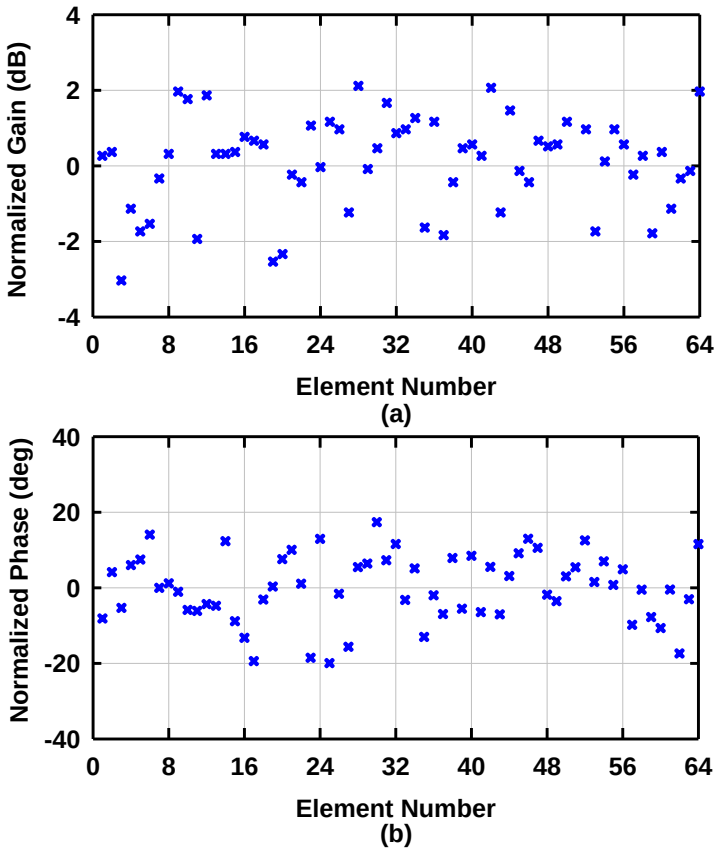


Figure 4.10: Measured normalized (a) gain and (b) phase of all 64 elements in the far field at 29 GHz.

was the center frequency used for the 5G link measurements (see Section 4.5). The measured 3-dB beamwidth is 12.9° in the H-plane with sidelobes <-12 dB and cross-polarization levels <-25 dB and agree well with simulations. The array can scan to $\pm 50°$ in the H-plane [Fig. 4.11(b)] and $\pm 25°$ in the E-plane [Fig. 4.11(c)] with sidelobes <-10 dB over all scan angles. The E-plane 3-dB beamwidth is 10.4° and is narrower due to the vertical antenna spacing of 0.63λ at 30 GHz.

Fig. 4.11(d) presents the measured cross-polarization levels versus scan angle in the H-plane. At boresight, the cross-polarization level is limited by the alignment accuracy of the 64-element array and the horn given by $\tan(\theta_{mis})$, and 3° of misalignment will limit the measured cross-polarization level to -26 dB. Since the patch feed location is asymmetric, the cross-

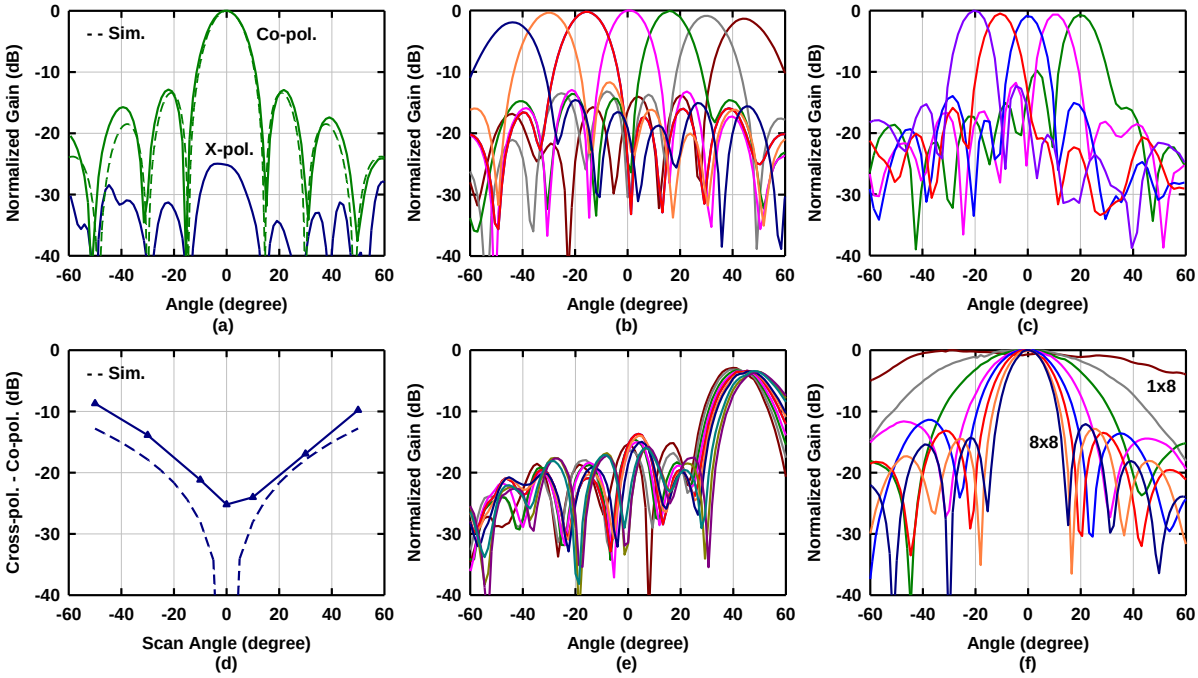


Figure 4.11: Measured (a) H-plane co-pol. and cross-pol. in the RX mode, (b) H-plane and (c) E-plane patterns in the TX mode, (d) cross-pol. versus scan angle, (e) fine resolution beam steering around 45°, and (f) H-plane patterns with different numbers of elements turned on.

polarization level degrades in the H-plane to -10 dB as the beam is scanned to $\pm 50°$ and agrees with simulations. The E-plane cross-polarization level remains < -25 dB over all scan angles and is not shown.

The beam can be scanned in fine resolution around any scan angle by applying a non-uniform phase gradient across the aperture as demonstrated in [42]. For example, the beam is steered in 1° steps around 45° in Fig. 4.11(e) without degrading the measured sidelobe levels. The H-plane patterns are also measured by turning on different consecutive columns, and the beamwidth reduces as more columns are turned on, as expected [Fig. 4.11(f)].

To demonstrate the robustness of the scalable symmetric phased-array architecture versus process variations, the measured uncalibrated patterns in the RX mode from two different 64-element array boards are compared in Fig. 4.12 in the azimuth and elevation scan planes. The measured patterns agree well with each other and with simulations despite different random phase and gain errors between the elements.

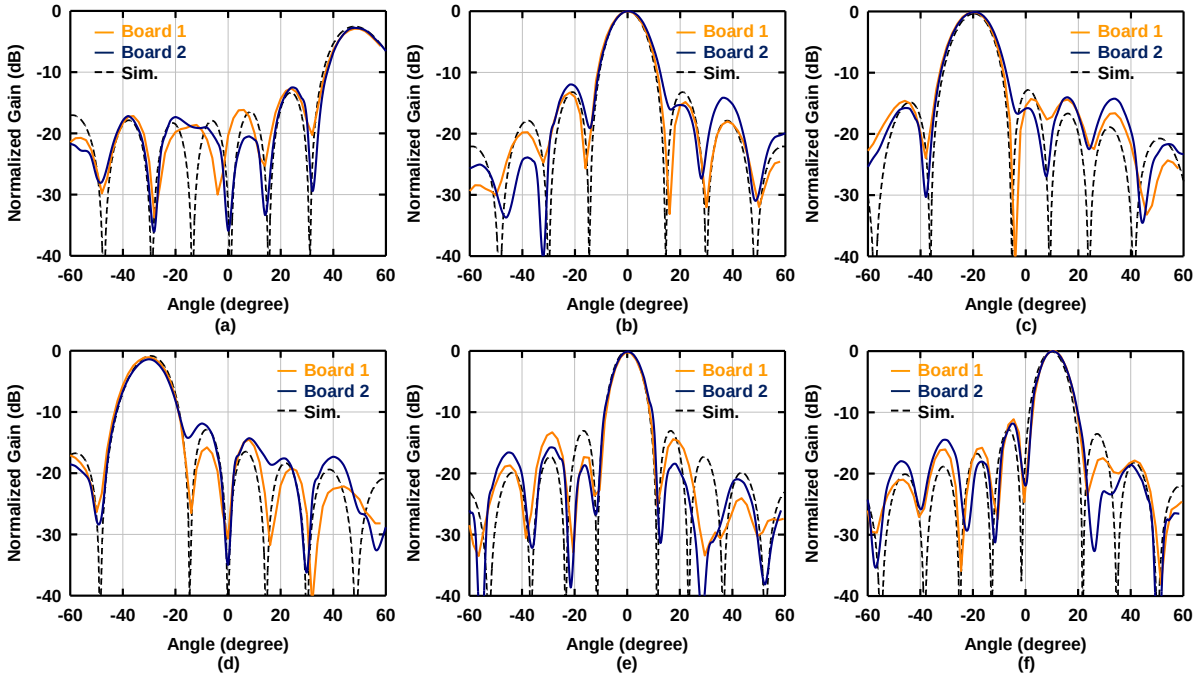


Figure 4.12: Measured uncalibrated patterns for two different arrays at 29 GHz at (a) 50°, (b) 0°, (c) −20°, (d) −30° in the H-plane and (e) 0°, (f) 10° in the E-plane. All H-plane patterns are normalized to the untapered 29 GHz pattern at boresight.

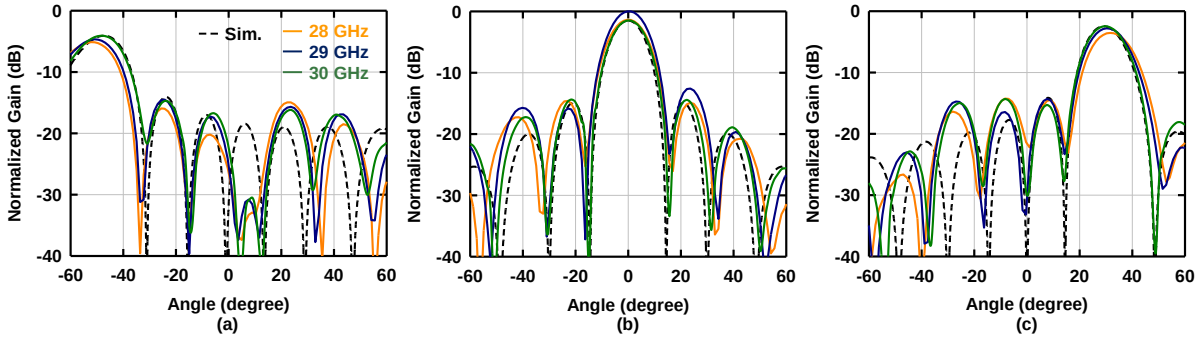


Figure 4.13: Measured beam squint at 28-30 GHz at (a) −50°, (b) 0°, (c) 30° in the H-plane. All H-plane patterns are normalized to the untapered 29 GHz pattern at boresight.

Since the 6-bit phase shifters employed in the 2x2 TRX beamformer chips provide constant phase shift versus frequency rather than constant time delay, the beam will point in slightly different directions at each frequency, called beam squint [54]. This is demonstrated in Fig. 4.13 at 28-30 GHz with the elements phased at f_0 = 30 GHz and patterns normalized to the 29 GHz pattern at boresight. At boresight (θ_{f_0} = 0), the beam points at θ_f = 0° at all frequencies [Fig.

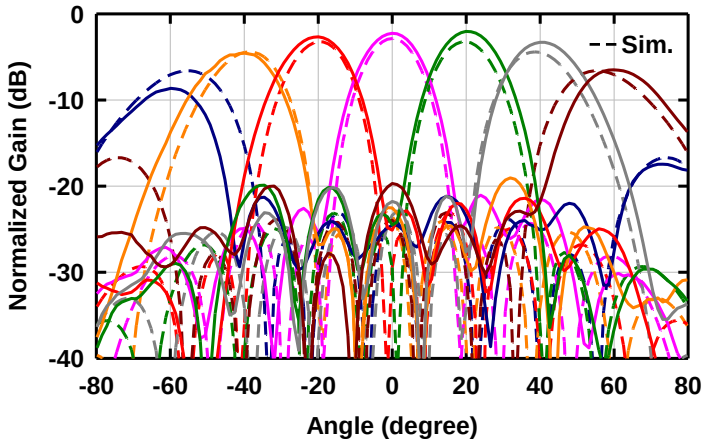


Figure 4.14: Measured H-plane patterns with 6 dB raised-cosine taper. All H-plane patterns are normalized to the untapered 29 GHz pattern at boresight.

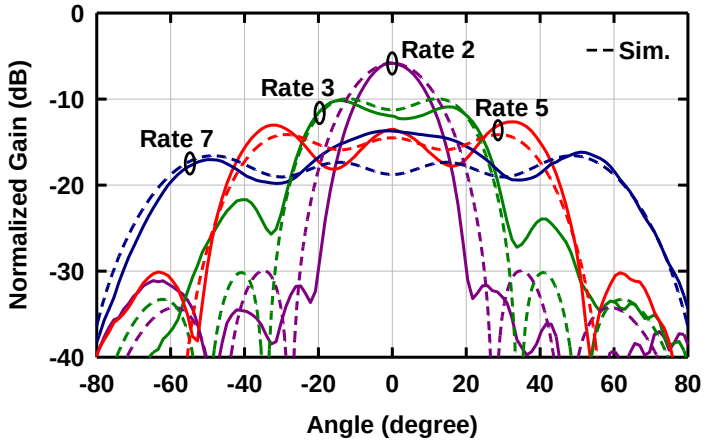


Figure 4.15: Measured flat-top patterns for different rates. All H-plane patterns are normalized to the untapered 29 GHz pattern at boresight.

4.13(b)]. As the beam is scanned to $\theta_{f_0} = -50°$ [Fig. 4.13(a)] and $\theta_{f_0} = 30°$ [Fig. 4.13(c)], the peak occurs at 30 GHz and the beam points at slightly different angles at 28 and 29 GHz. The pointing angle, θ_f is calculated using

$$\theta_f = \sin^{-1}(\frac{f_0}{f}\sin(\theta_{f_0})) \tag{4.4}$$

and varies by $<\pm 2.6°$ over ± 1 GHz bandwidth at a scan angle of 50°. Therefore, the beam squint results in ± 0.5 dB gain variation versus frequency for wideband modulation measurements, but this can be corrected using equalization in the modem and will not affect the measured error

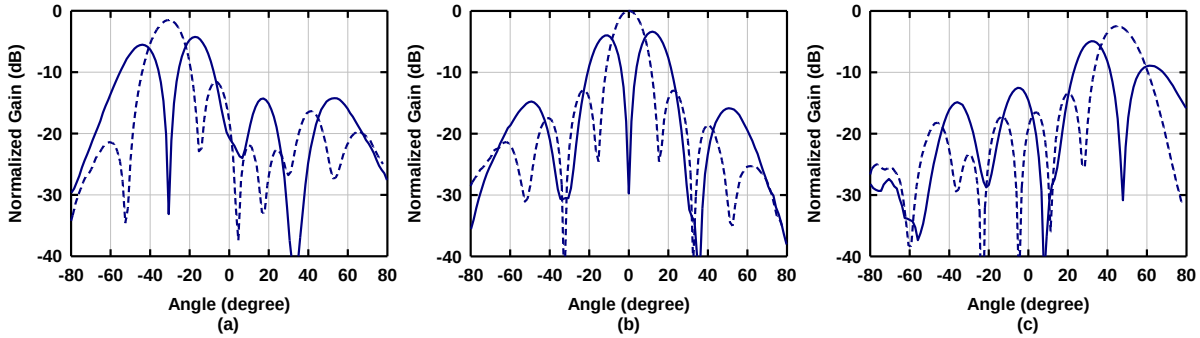


Figure 4.16: Measured monopulse patterns (solid) at (a) $-30°$, (b) $0°$, (c) $45°$ in the H-plane. Uniform illumination patterns are also shown (dashed). All H-plane patterns are normalized to the untapered 29 GHz pattern at boresight.

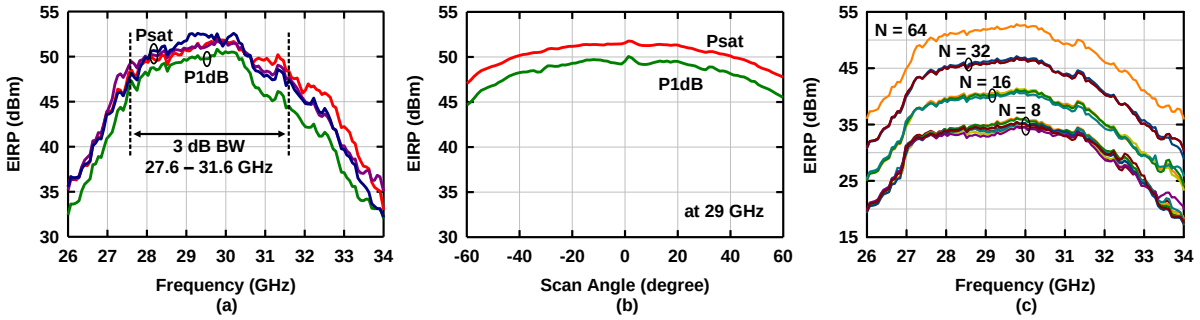


Figure 4.17: Measured (a) EIRP at P1dB and Psat, (b) EIRP versus scan angle, (c) EIRP with different numbers of elements turned on.

vector magnitude (EVM) up to 3 GHz of modulation bandwidth (see Section 4.5).

The patterns can be tapered using the VGAs in each channel with a 6 dB raised-cosine taper as shown in Fig. 4.14 to reduce the sidelobe levels to -20 dB (taper applied in the H-plane). The raised-cosine taper results in 2.9 dB reduced array gain compared to the untapered patterns and agrees with simulations. Tapered patterns at $\pm 60°$ at 29 GHz are also shown in Fig. 4.14 and result in a vestige of a grating lobe. Note that since the spacing in the x-direction is 0.5λ at 30 GHz, there is no full grating lobe in the visible region, and around half of the grating lobe is present at 70-90°.

The phased-array can also be excited to result in flat-top patterns for applications which require a short distance link with large coverage area to serve multiple users at the same time (Fig. 4.15). This can either be achieved by reducing the number of elements [as in Fig.

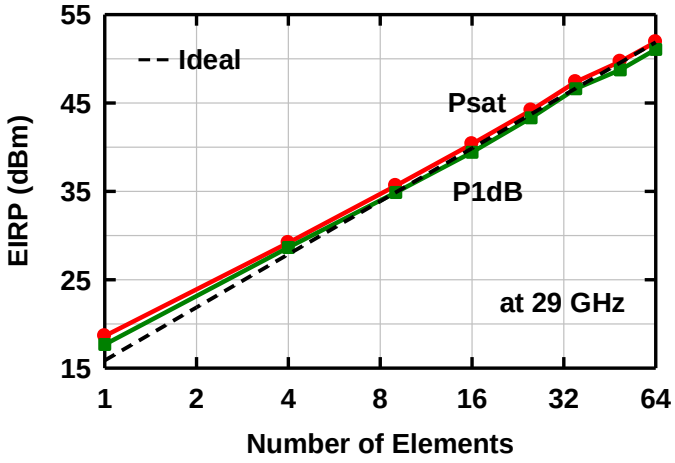


Figure 4.18: Measured EIRP at 29 GHz versus number of elements.

4.11(f)], or by placing a $sinc$ function across the aperture with its width adjusted to determine the beamwidth. The amplitude and phase of each column, $E(n)$ is set using

$$E(n) = sinc(\frac{r * (n - \frac{N_C - 1}{2})}{N_C - 1}) \tag{4.5}$$

where n is the column number, N_C = 8 is the total number of columns and r is the pattern rate to result in flat-top patterns. Fig. 4.15 presents the measured flat-top patterns for r = 2-7. Note that there are many synthesis techniques for flat-top patterns, some of equi-amplitude excitation and with phase-variation only, and this is just one example.

The 64-element 5G phased-array can also be used in tracking applications as demonstrated in [55]. For such applications, a monopulse pattern is desirable to identify the location and speed of the object accurately. The measured monopulse patterns are presented in Fig. 4.16 together with the uniform illumination patterns. It is shown that -30 dB nulls are achieved without any calibration over all scan angles.

Fig. 4.17(a) presents the measured EIRP of the 64-element array versus frequency for 3 different phased-arrays. The measured EIRP is 50 dBm at P1dB with a 3-dB bandwidth of 27.6-30.6 GHz, and is 51-52 dBm at the saturated output power (Psat) with a 3-dB bandwidth of 27.6-31.6 GHz. The measured EIRP at Psat is within $\pm$0.5 dB for 3 different arrays without any

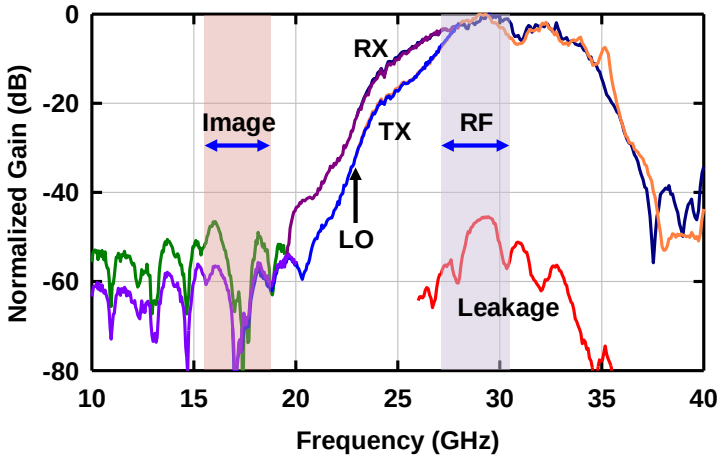


Figure 4.19: Measured wideband frequency response and leakage.

calibration. The EIRP was also measured against scan angle in the H-plane [Fig. 4.17(b)] and drops by 2-3 dB at $\pm 50^{\circ}$ as expected from the pattern measurements [Fig. 4.11(b)].

The EIRP at Psat with different numbers of columns turned on is presented in Fig. 4.17(c). For different combinations of 8 elements, there is ± 1 dB difference in the measured EIRP due to the gain mismatch between the uncalibrated elements [see Fig. 4.10(a)]. As the number of elements increases, the variation is reduced since the gain and radiated power is averaged over many more elements. The measured EIRP increases as N^2 versus the number of elements (N = 1-64) and shows only 0.7 dB deviation at N = 64 from the ideal line centered at 8 elements (Fig. 4.18). The line fitting cannot be started at 1 or 2 elements since there is ± 2 dB variation across the array and these are uncalibrated EIRP measurements.

4.4.2 LO and Image Rejection

Link measurements were performed with an IF signal of 6 GHz which is upconverted to 29 GHz using external mixers and an LO of 23 GHz (see Section 4.5). This results in an upconverted image at 17 GHz which could degrade the system EVM if not filtered out. However, the 2x2 TRX beamformer chips and antennas employed in this work are relatively narrowband. Fig. 4.19 presents the measured frequency response of the 8x8 array in both the TX and RX

modes. This was done using three separate standard gain horns at 10-40 GHz (plotted in different colors for different horns used). The response shows an LO rejection $>$ 30 dBc and an image rejection $>$ 50 dBc from the 8x8 array. This is sufficient to reject the image and LO leakage so that they have no impact on the measured EVM. The measured leakage in the TX mode with all channels turned off is -45 to -60 dBc showing little coupling due to the flipped chips and the PCB traces. The leakage may also be due to the coaxial connector (even if some absorber was placed on it).

4.4.3 EVM versus EIRP and Scan Angle

Modulation measurements were first performed at a link distance of 1.3 m using the setup shown in Fig. 4.20(a) with one array operating in the TX mode and a 19 dB gain horn as the receiver. A 100 Mbaud 64-QAM waveform is generated at an RF of 29 GHz using a Keysight M8195A arbitrary waveform generator (AWG). The AWG is operated at its maximum output power at 29 GHz to achieve the best dynamic range. Since the Mission Microwave amplifier used in the setup is a class AB design, the external amplifiers are operated at a fixed input power with $>$ 10 dB backoff, and the power into the 64-element array is adjusted using a variable attenuator following the amplifiers. This ensures that the EVM degradation due to nonlinearities is only due to the 8x8 TRX array and not due to the driver amplifiers. The power into the TX array is monitored using a 3-dB coupler and a power meter.

The AWG has an SNR $>$ 42 dB at 29 GHz at 8-dB backoff (-14 dBm average power) for a 64-QAM waveform with α = 0.35 and 100 MHz modulation bandwidth [56]. Therefore, the AWG output noise is -56 dBm over the modulation bandwidth (-137 dBm/Hz). Since the driver amplifiers have an NF of 5-6 dB, they do not degrade the SNR, and 42 dB SNR is maintained at the phased-array input port.

The modulated signal is received by the horn and attenuated so that the downconversion mixer is far from its saturation point. The signal is downconverted to an IF of 4 GHz using an external 25 GHz LO, amplified and demodulated [Fig. 4.20(a)]. The measured EVM values are

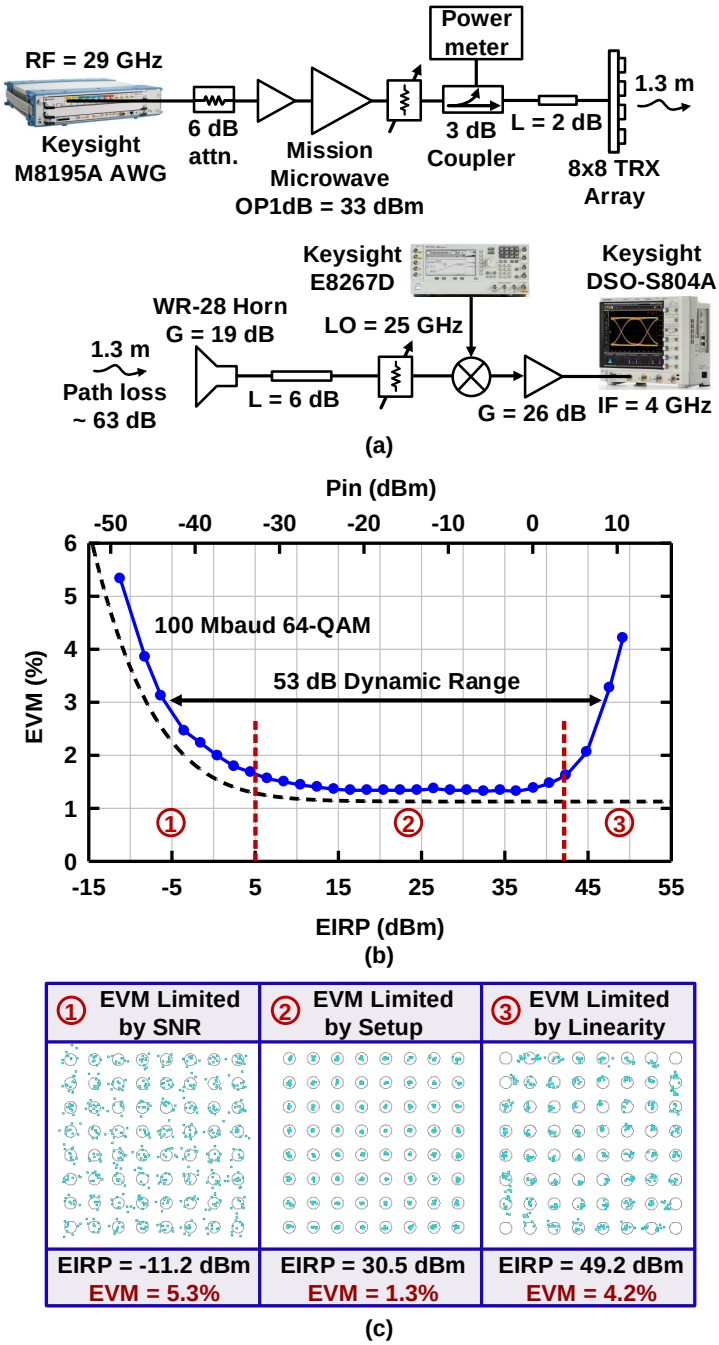


Figure 4.20: (a) EVM measurement setup with one 8x8 TRX array in the TX mode and a standard gain horn as the receiver. Measured EVM at 1.3 m versus (b) different EIRP levels using 100 Mbaud 64-QAM. (c) Example constellations for different EIRP levels.

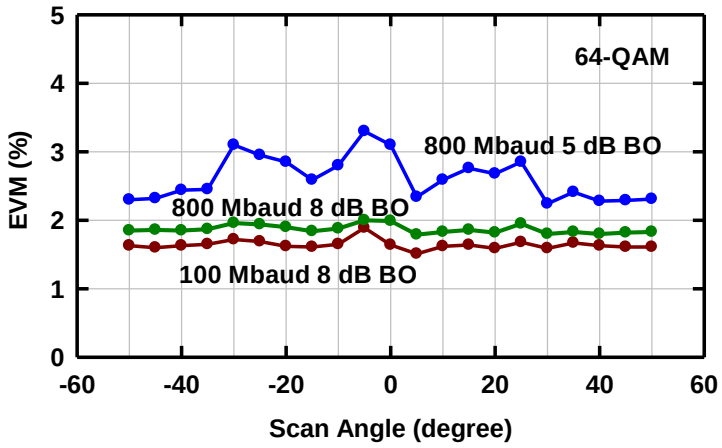


Figure 4.21: Measured EVM for different scan angles using 100-800 Mbaud 64-QAM at 5-8 dB backoff.

shown in Fig. 4.20(b) for different EIRP levels without any array calibration. All EVM values reported are rms values referenced to the constellation peak (EVM_{max} in [57]) and measured using equalization in the VSA software to remove the gain and phase ripple of the components in the measurement setup.

The calculated EVM taking only the TX noise floor into account is also plotted in Fig. 4.20(b) (dashed line) and agrees well with the measurements. Since the 64-QAM waveform filtered with a root-raised-cosine pulse shaping filter with a roll-off factor α = 0.35 has a peak-to-average power ratio (PAPR) of 7.7 dB, the EVM increases beyond an average EIRP of 42 dBm (region 3), which corresponds to 8 dB backoff (BO) from the array P1dB. The EVM remains $< 3\%$ up to an EIRP of 47 dBm (4 dB BO from P1dB). A transmit dynamic range of 53 dB can be achieved with an EVM $< 3\%$ for 100 Mbaud 64-QAM.

Fig. 4.20(c) presents example constellations in the TX mode for different EIRP regions marked on Fig. 4.20(b). The EVM is limited by the SNR (region 1), the measurement setup (region 2) and the TX array nonlinearities (region 3). At -11.2 dBm average EIRP, the EVM is limited by the TX noise. At 49.2 dBm average EIRP, the EVM is limited by the TX nonlinearities and the constellation clearly shows both compression due to AM-AM and rotation due to AM-PM conversion.

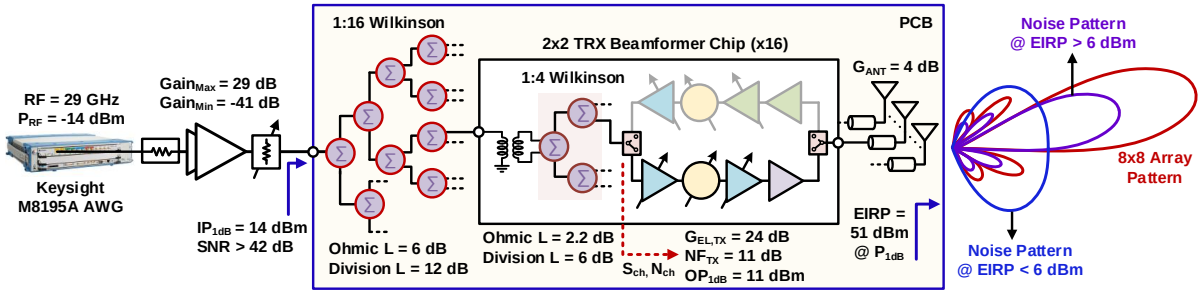


Figure 4.22: SNR calculations for the 64-element (8x8) array in the TX mode for different EIRP levels at 29 GHz.

The EVM was then measured over scan angle in the H-plane using 100 Mbaud and 800 Mbaud 64-QAM waveforms (Fig. 4.21). At 8 dB backoff, the measured EVM is limited by the test setup and some nonlinearity contribution from the phased-array and remains constant at $< 2\%$ over $\pm 50^{\circ}$ scan angle. Note that for an SNR-limited link, the EVM increases with scan angle due to the reduced antenna gain which is not the case here. At 5 dB backoff and 800 Mbaud, the constellation is compressed since the waveform PAPR is 7.7 dB resulting in some EVM variation over scan angle. Still, it is $< 3\%$ over most scan angles.

4.4.4 TX Noise Analysis versus EIRP

The TX noise and SNR can be analyzed as shown in Fig. 4.22. For an EIRP of 40 dBm (EVM limited by the setup), the signal power at the phased-array coaxial port is 2 dBm (the amplifier/attenuator chain has a gain of 16 dB) and the input noise is -40 dBm. Note that this noise is coherent as it is fed to all the phased-array channels. Both the signal and noise are then attenuated by 26 dB, with 18 dB 1:64 division loss and 8 dB Wilkinson divider ohmic loss on the PCB and the silicon chip (Fig. 4.22). The available coherent noise at the input of each channel is therefore -147 dBm/Hz and is much higher than the TX channel input referred noise (NF_{TX} = 11 dB or -163 dBm/Hz). Thus, the array will radiate a noise pattern which is the same as the signal pattern, and with a SNR of 42 dB. Also, if the array pattern is scanned, the noise pattern will scan in the same direction since it is coherent and is phase-shifted in every channel. An

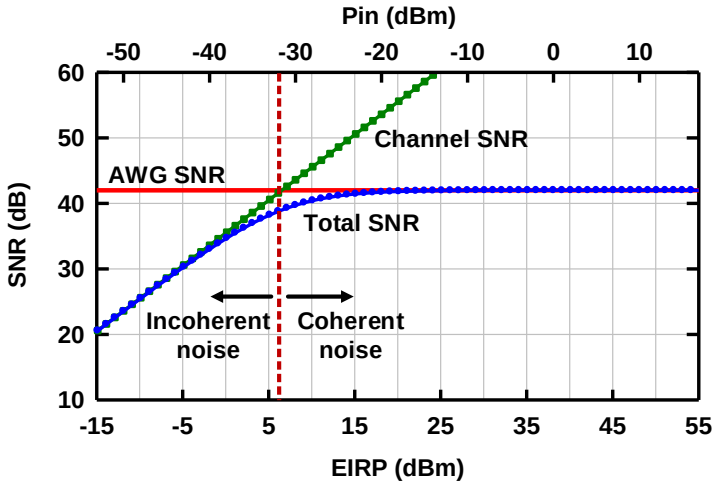


Figure 4.23: Simulated SNR for the TX EVM measurements.

EVM of 1.3% is measured due to the AWG SNR and the LO phase noise contribution (1%) [58] in the receive path (region 2).

This analysis changes completely at an EIRP of -5 dBm. In this case, the signal power at the phased-array coaxial port is -43 dBm and the input coherent noise is -85 dBm (-166 dBm/Hz). Again, the signal and coherent noise are attenuated by 26 dB, resulting in an input signal at each channel of -69 dBm. However, the coherent noise from the AWG drops below the thermal noise floor and levels at -174 dBm/Hz due to the resistors in the Wilkinson combiner. Each channel has an NF of 11 dB (-163 dBm/Hz), but the noise of each channel is incoherent, therefore the radiated noise power has a $\sim\cos(\theta)$ element pattern. On the other hand, the radiated signal power adds coherently and has an 8x8 phased-array pattern.

A detailed analysis for the incoherent mode is shown below. The SNR at the input of each channel, SNR_{ch} is calculated using

$$N_{ch} = 10\log(kTB(1+\alpha)) + NF_{TX} \tag{4.6}$$

$$SNR_{ch} = S_{ch} - N_{ch} \tag{4.7}$$

where S_{ch} is the signal power at the channel input, N_{ch} is the noise power at the channel input (see Fig. 4.22), k is Boltzmann's constant, T is the absolute temperature, B is the modulation

bandwidth (100 MHz) and NF_{TX} is the TX channel NF (11 dB). At S_{ch} = −69 dBm, this results in an SNR_{ch} = 13 dB for every channel. The radiated SNR is calculated using

$$EIRP = S_{ch} + 20\log(N) + G_{EL,TX} + G_{ANT} \quad (4.8)$$

$$EIRP_N = N_{ch} + 10\log(N) + G_{EL,TX} + G_{ANT} \quad (4.9)$$

$$SNR = EIRP - EIRP_N \quad (4.10)$$

where $EIRP$ is the radiated signal power, $EIRP_N$ is the radiated noise power, N is the number of elements (64), $G_{EL,TX}$ is the TX channel electronic gain which does not include the 1:4 on-chip Wilkinson division loss and ohmic loss (24 dB at 29 GHz) and G_{ANT} is the antenna element gain (5.5 dB directivity − 1.5 dB feel line and antenna loss = 4 dB). For S_{ch} = −69 dBm, $EIRP$ is −5 dBm and $EIRP_N$ is −36 dBm, resulting in a radiated SNR of 31 dB. It is seen that a phased-array improves the SNR of a single channel by $10\log N$ (18 dB), provided that the noise at the input of the channels is incoherent. As shown in Fig. 4.20(b), the measured EVM at $EIRP$ = −5 dBm is 2.7% and is partly due to the radiated SNR and partly due to the receive LO phase noise.

Fig. 4.23 presents the simulated SNR contributions of the AWG (coherent) and the TX channel (incoherent) at different EIRP levels. The noise contribution of the AWG falls below the noise floor at Pin = −43 dBm at the array coaxial port [N_{ch} = −43 dBm − 42 dB (AWG SNR) − 26 dB (Wilkinson division and ohmic loss) + 18 dB (coherent addition) = −93 dBm (−174 dBm/Hz)], and does not affect the system SNR. At $EIRP$ = 6 dBm, the radiated noise contribution of the AWG and the TX channel are equal. For $EIRP > 6$ dBm, the AWG noise dominates, and the array will radiate a coherent noise pattern. This transition cannot be observed in Fig. 4.20(b) since the LO phase noise contribution in the RX path (1%) already limits the SNR to 40 dB. For $EIRP < 6$ dBm, the TX channel noise dominates the SNR and the radiated noise is incoherent.

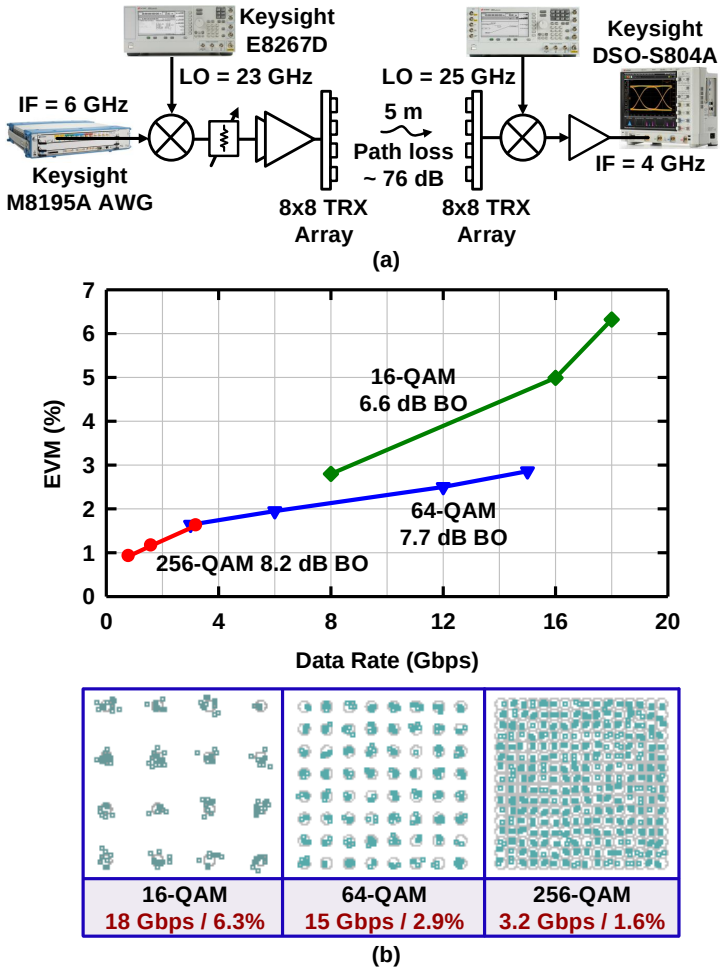


Figure 4.24: (a) Measurement setup for the 5 m and 300 m link. (b) Measured data rate and example constellations using two 8x8 TRX arrays and different modulations at 5 m.

4.5 5-Meter and 300-Meter Link Measurements

Link measurements were performed using two 64-element TRX arrays at a distance of 5 m [Fig. 4.24(a)], and the measured EVM and constellations are presented for different modulations and data rates [Fig. 4.24(b)]. In this experiment, the TX array is operating at a P1dB backoff level equal to the PAPR of the modulated waveform (6.6 dB, 7.7 dB, 8.2 dB for 16-/64-/256-QAM, respectively) which results in 42-43 dBm average EIRP at 29 GHz, and 40-41 dBm average EIRP over the modulation bandwidth. The received power per antenna element at 5 m with 76 dB path loss and G_{ANT} = 4 dB is -32 to -31 dBm and is 10-11 dB lower than the RX

Table 4.3: Link Budget for 5-300 m 5G Link Using 64-Element Phased-Arrays

Parameter	**5 m 16-QAM**	**300 m 16-QAM**	**300 m 64-QAM**
Modulation bandwidth (GHz)	4.5	3	1.5
EIRP (dBm)	41	41	42
Path loss (dB)	76	111	111
Misalignment loss (dB)	0	1.5	1.5
Antenna gain, G_{TRX} (dB)	22.5	22.5	22.5
System NF (dB)	7.5	7.5	7.5
Receiver power (dBm)	-13	-49	-48
Noise power (dBm)	-69	-70	-73
System EVM (referenced to constellation peak)			
Expected SNR / EVM (dB / %)	56 / 0.1	21 / 6.6	25 / 3.7
AWG SNR / EVM (dB / %)	28 / 3.0	30 / 2.3	33 / 1.5
EVM from LOs (%)	1.6	1.6	1.4
System EVM (%)	3.4	7.2	4.2

channel IP1dB. Therefore, only the TX array has some nonlinearity contribution on the EVM as seen on the corner points of all constellations in Fig. 4.24(b).

In the RX mode, the system NF is 7.5 dB including the PCB beamformer loss and the noise contribution of all components in the setup, and the noise power is -69 dBm for 4.5 Gbaud 16-QAM. The system NF is relatively constant (± 0.3 dB) over the modulation bandwidth [see Fig. 4.4(c)]. After coherent signal addition from 64 channels, the resulting receiver SNR is 56 dB, and therefore, the 5 m link is not SNR limited even at the highest modulation bandwidth used. The data rate is limited mainly by the bandwidth of the 2x2 TRX chips and the stacked-patch antennas as well as some contribution from the AWG SNR at large modulation bandwidths. Table 4.3 provides a breakdown of system parameters and the simulated EVM contributions for the 4.5 Gbaud 16-QAM single-carrier waveform.

The 8x8 arrays can achieve a maximum data rate of 18 Gbps (4.5 Gbaud) with 6.3% EVM using 16-QAM and 15 Gbps (2.5 Gbaud) with 2.9% EVM using 64-QAM waveforms. Even though the EVM is only 6.3% with 18 Gbps 16-QAM, the data rate cannot be increased further since the array EIRP drops sharply beyond 4 GHz of bandwidth and this can no longer be corrected using equalization in the VSA software. This is seen in Fig. 4.24(b) as a sharp increase in EVM beyond 4 GHz modulation bandwidth. For higher order modulations (64-QAM and 256-QAM) with large modulation bandwidth, the EVM is limited by the AWG EVM and the LO phase noise.

To demonstrate the maximum achievable data rate in an SNR-limited link, the measurements were then performed at a link distance of 300 m and a photograph of the measurement setup is shown in Fig. 4.25(a). In this case, a Friis link analysis can be used to determine the expected link performance based on the TX and RX array performance [dashed lines in Fig. 4.25(b)]. Additional effects on EVM such as LO phase noise, I/Q mismatch and TX nonlinearities are ignored in this estimation since the EVM is dominated by the system SNR. It is also assumed that there is no phase and gain ripple within the modulation bandwidth since these effects are corrected using equalization in the VSA software.

A Friis link analysis with EIRP = 42 dBm at 8 dB backoff from P1dB, G_{TRX} = 22.5 dB, system NF = 7.5 dB, and link distance R = 300 m results in a simulated receiver SNR of 23-21 dB for 2-3 GHz modulation bandwidth which translates to 5.5-6.7% EVM for 16-QAM. The measured data rate using 16-/64-QAM waveforms at 300 m and normal incidence is shown in Fig. 4.25(b). The maximum data rate achieved is 12 Gbps (3 Gbaud) using 16-QAM with 10.6% EVM and 9 Gbps (1.5 Gbaud) using 64-QAM with 5.6% EVM. Table 4.3 provides a breakdown of simulated EVM contributions for the peak data rates at 300 m using 16-/64-QAM waveforms.

The EVM is also measured at different scan angles in the E- and H-planes using 8 Gbps 16-QAM [Fig. 4.25(c)]. The beam is scanned by mechanically turning the RX array and electronically steering the beam back towards the TX array. The measured EVM is 6.5-10.2% and increases at large scan angles as expected since the link is SNR limited and the antenna gain

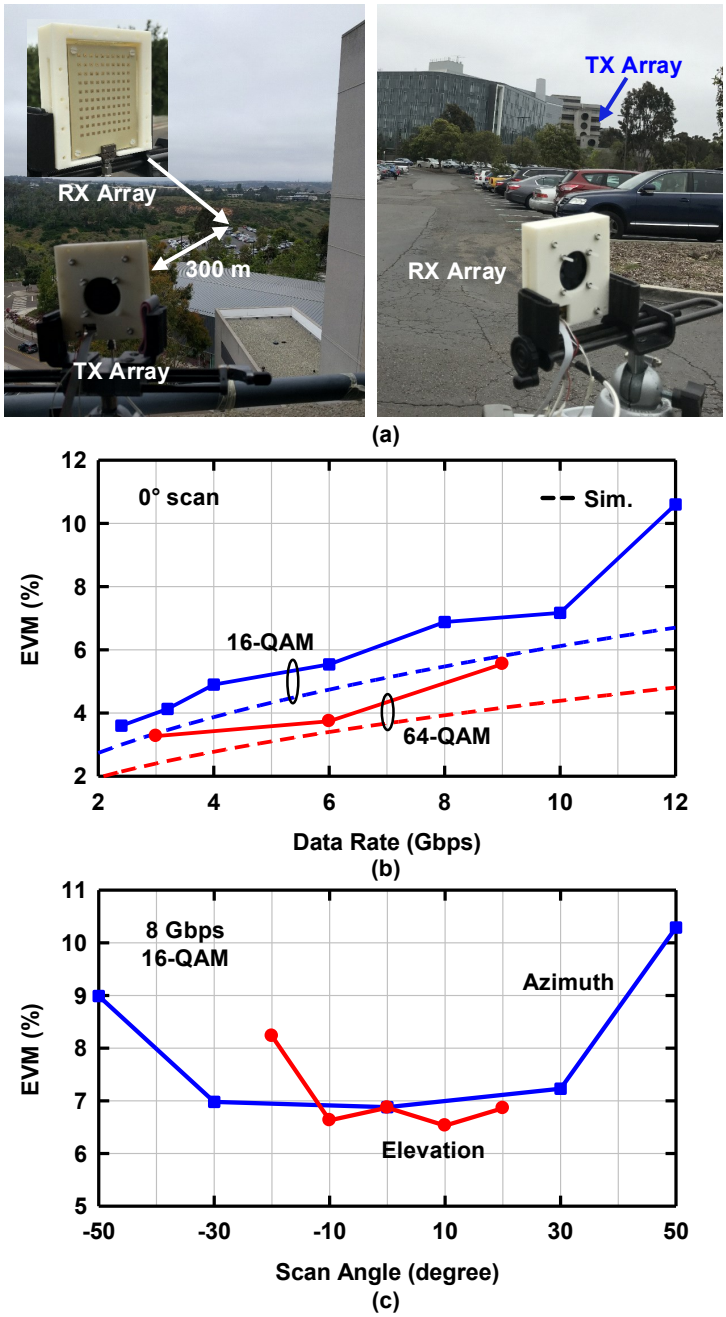


Figure 4.25: (a) Photograph of the 300 m 5G link using two 8x8 TRX phased-arrays. Measured EVM at (b) different data rates using 16-/64-QAM and (c) different scan angles in azimuth and elevation using 8 Gbps 16-QAM.

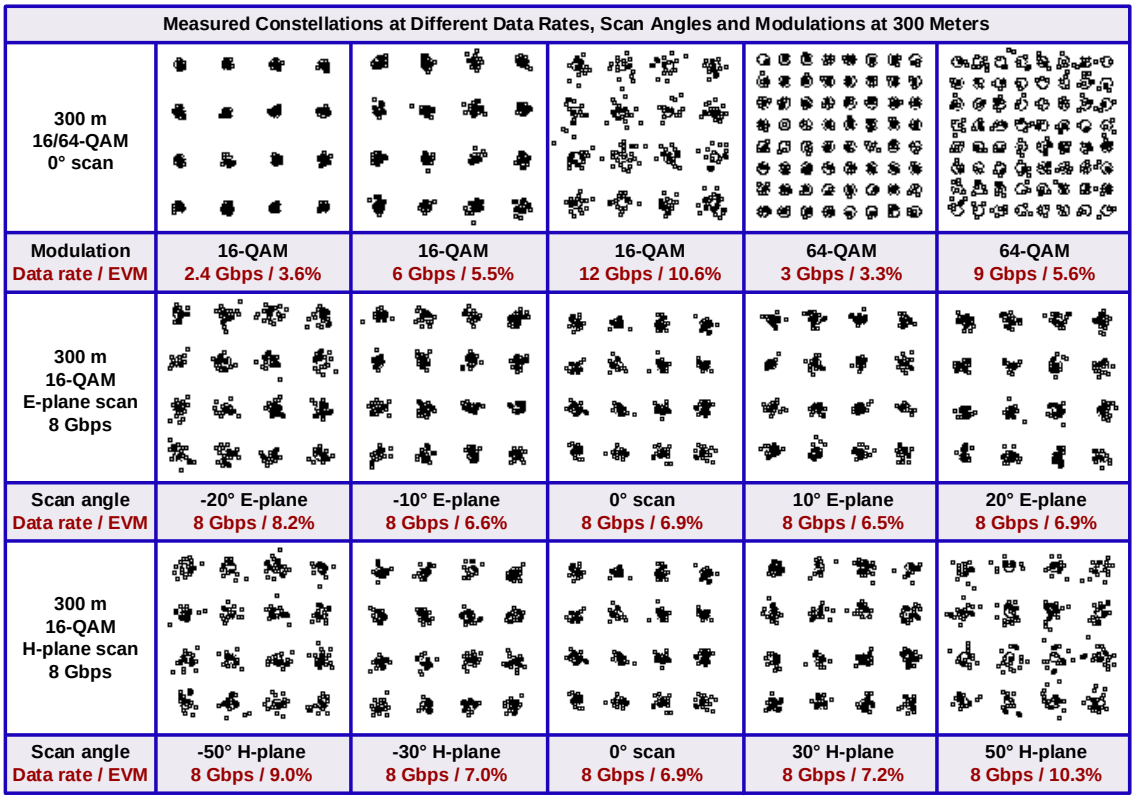


Figure 4.26: Measured constellations at different data rates, scan angles and modulations for the 300 m data link.

drops with scan angle due to the element factor. Example constellations from the 300 m link measurements are provided in Fig. 4.26 and the EVM is mainly limited by the system SNR.

The 8x8 arrays achieve a record-setting data rate of 8-12 Gbps over all scan angles using 16-/64-QAM waveforms at 300 m. Compared with the 4x8 array presented in Chapter 2 which achieved 1.0-1.6 Gbps over all scan angles using 16-QAM at the same link distance of 300 m, this work achieves 8x the data rate. This is due to the N^3 improvement in the link SNR as the number of elements is increased (N^2 on transmit and N on receive) and the 12-layer PCB design with wideband stacked-patch antennas which allow for much larger modulation bandwidths.

Table 4.4 summarizes the performance of this work and compares it with state-of-the-art 28 GHz phased-array transceivers.

4.6 Conclusion

This chapter presented a 64-element 5G phased-array transceiver built using 2x2 TRX beamformer chips with state-of-the-art performance. The effect of mismatch in element gain and phase is investigated and the arrays result in excellent performance without any calibration. Future work includes the demonstration of multi-standard wideband 24-31 GHz 5G phased-arrays with 4x4 multiple-input multiple-output (MIMO) capabilities.

4.7 Acknowledgment

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Chapter 4, in full, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer, T. Phelps and G. M. Rebeiz, “A 64-Element 28-GHz Phased-Array Transceiver With 52 dBm EIRP and 8-12 Gb/s 5G Link at 300 Meters Without Any Calibration,” *IEEE Transactions on*

Table 4.4: Comparison with State-of-the-Art 28 GHz Phased-Array Transceivers

Parameter	**This work**	Qualcomm '18 [39]	LG '18 [40]	IBM '17 [8]	UCSD '18 [42]
Process	**0.18 μm SiGe BiCMOS**	28 nm LP-RF CMOS	28 nm LP CMOS	0.13 μm SiGe BiCMOS	0.18 μm SiGe BiCMOS
Frequency (GHz)	**28-32**	26.5-29.5	25.8-28	27.2-28.7	28-31
Elements per chip	**4 TRX**	2x8 + 8 TRX	8 TRX	2x16 TRX	4 TRX
Elements in array	**64 TRX**	2x4 + 4 TRX	2x8 TRX	2x64 TRX	32 TRX
Chip area (mm^2)	**11.3**	27.8	7.3	165.9	11.7
IC integration level	**RF front-end**	RF front-end + PLL + RF/IF conversion	RF front-end + VCO + RF/IQ conversion	RF front-end + RF/IF conversion	RF front-end
Polarization	**Single**	Dual	Dual	Dual	Single
RF gain cont. RX (dB)	**26**	9	24	8	14
RF gain cont. TX (dB)	**20**	8	39	8	14
Phase step (°)	**5.6**	45	45	4.9	5.6
E- / H-plane scan (°)	**±25 / ±50**	±45 / ±45	±20 / ±20	±50 / ±50	±25 / ±50
Sidelobe level (dB)	**<−10**	<−7	<−9	<−12	<−12
TX OP_{1dB} / el. (dBm)	**12**	>12	9.5	13.5	10.5
TX OP_{sat} / el. (dBm)	**13**	>14	10.5	16	12.5
RX IP_{1dB} (dBm)	**−21**	-	−69	−22.5	−22
RX NF / chip (dB)	**4.8**	4.4-4.7	6.7	6.0	4.6
TX P_{DC} / el. (mW)	**220 @ P_{1dB}**	122 @ P_{1dB}	85 @ 24 dBm EIRP	319 @ P_{sat}	200 @ P_{1dB}
RX P_{DC} / el. (mW)	**150**	42	50	206	130
EIRP at P_{sat} (dBm)	**52**	34-35 / pol.	31.5 / pol.	54 / pol.	45
Calibration	**No**	No	Yes	Yes	No
Over-the-air data rate	**18 Gbps 16-QAM @ 5 m** **9 Gbps 64-QAM @ 300 m** **12 Gbps 16-QAM @ 300 m**	100 MHz OFDM 64-QAM @ 2 m	LTE 20 MHz 64-QAM @ 2.5 m	-	6.0 Gbps 16-QAM @ 5 m 1.6 Gbps 16-QAM @ 300 m

Microwave Theory and Techniques, 2018. The dissertation author was the primary investigator and author of this paper.

Chapter 5

Dual-Polarized Dual-Beam Phased-Arrays

5.1 Introduction

The development of fifth-generation (5G) data links is advancing at a rapid pace. Although the 28 GHz standards are not set yet, it is clear that 5G links will utilize phased-arrays and spectrally efficient waveforms (16-QAM or higher) to achieve data rates of 10 Gbps or higher [7, 8, 59]. For a single-carrier 64-QAM waveform with 800 MHz modulation bandwidth, the data rate that can be achieved is limited to 4.8 Gbps per user, and this motivates the use of multiple-beam phased-arrays with multiple-input multiple-output (MIMO) capabilities to achieve higher capacity.

One way of doubling the link capacity is by employing a 2x2 MIMO configuration with two independent data streams transmitted and received using two separate antenna arrays and beamformer chips for the V- and H-polarizations [5]. Another method is to employ a polarization-based full-duplex system [60, 61] by transmitting and receiving two independent data streams at the same frequency at the same time. These methods are compared in Fig. 5.1.

In the polarization-based full-duplex system, one polarization is used to transmit and the other polarization is used to receive at the same frequency 100% of the time [Fig. 5.1(a)]. Since the receiver must detect a small signal in the presence of a large TX signal at the same

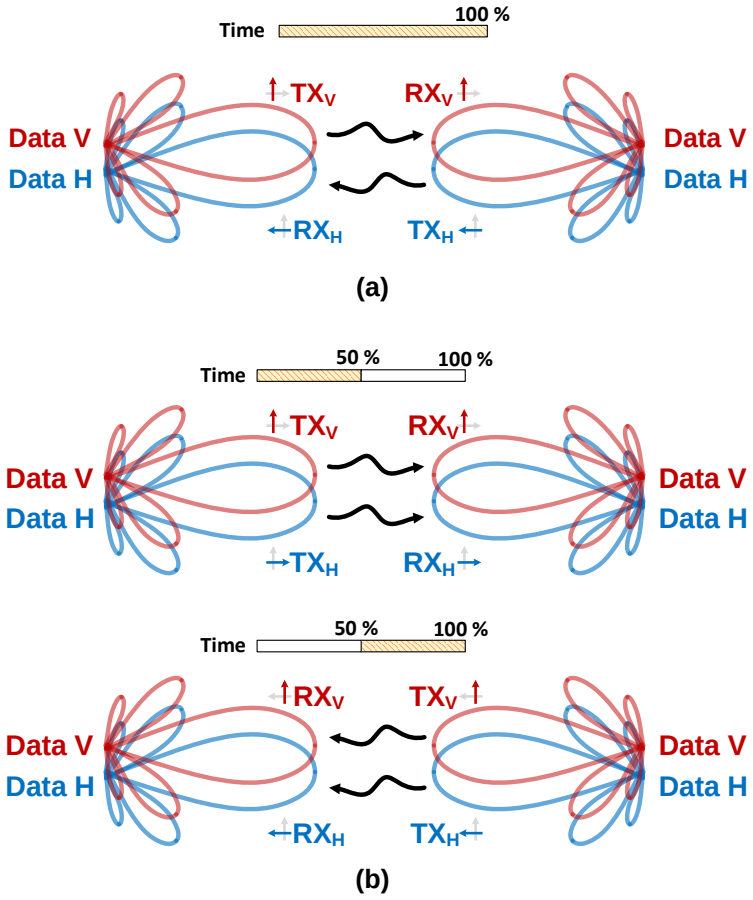

Figure 5.1: Comparison of (a) polarization-based full-duplex and (b) polarization-based MIMO systems.

frequency, additional self-interference cancellation circuits are required which cost additional power and area [60, 61]. The wideband TX noise can also couple to the RX side and significantly degrade the system SNR. On the other hand, the polarization-based 2x2 MIMO system transmits two independent data streams on different polarizations 50% of the time, and receives two independent data streams on different polarizations 50% of the time [Fig. 5.1(b)].

Since the polarization MIMO system either transmits two large signal or receives two small signals, there is no self-interference issue and both systems achieve the same data rate and spectral efficiency. The polarization MIMO system can result in higher latency compared to the full-duplex system due to the switching between the TX and RX modes, but this can be achieved in $\sim$100 ns using a hardwire T/R switch. The polarization MIMO system is favorable since it

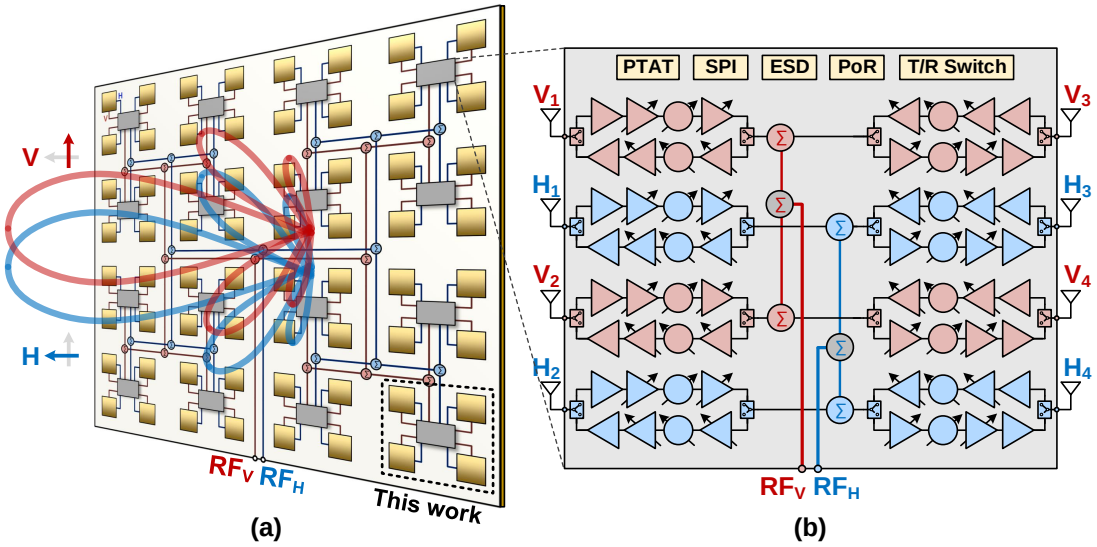

Figure 5.2: Block diagram of (a) 64-element dual-polarized dual-beam 5G phased-array for a 2x2 MIMO link and (b) 2x4 TRX dual-beam quad beamformer chip.

achieves the same data rate as full-duplex at lower power consumption and area since there is no self-interference. On top of this, one can implement full-duplex operation to transmit/receive on both polarizations at the same frequency at the same time to result in 4x data rate and spectral efficiency. However, this has not been demonstrated to-date and cannot be achieved using the techniques employed for polarization-based full-duplex operation [60, 61].

While it is theoretically possible to double the data rate using dual-beam phased-arrays with two different polarizations such as those presented in [7, 8], prior work have not yet demonstrated simultaneous data links using two polarization beams. Port-to-port coupling on-chip or on the PCB, antenna cross-polarization levels and any degradation in the chip performance when both V- and H-channels operate simultaneously could significantly compromise the achievable data rate. These challenges become more severe if the same antenna is used for both polarizations. This work aims to address these challenges and demonstrate a 2x2 MIMO link using dual-polarized dual-beam phased-arrays where both V- and H-beams are directed at the same user to result in twice the data rate.

5.2 2×4 TRX Beamformer Chip

A dual-polarized dual-beam 5G phased-array based on 2x4 TRX beamformer quad chips is shown in Fig. 5.2(a). Each chip contains eight TRX channels, four of which are connected together using an on-chip Wilkinson combiner/divider network into two common ports for the V- and H-polarizations [Fig. 5.2(b)]. Sixteen of these chips are assembled on a PCB with dual-polarized antennas and two independent Wilkinson networks to build a 64-element phased-array. Symmetry is maintained within both the chip and the PCB so that both polarizations show identical responses. Each TRX channel of the 2x4 chip contains SPDT switches, LNA, PA, 6-bit phase shifter and two VGA stages with 20-25 dB gain control. The chip is controlled using an SPI interface and all reference currents are generated from an on-chip PTAT current generator.

5.2.1 Circuit Design

The RX channel consists of a 2-stage LNA with 3-bit gain control on its second stage, and a 6-bit vector modulator (VM) phase shifter followed by another VGA with 4-bit gain control. The LNA employs a single-ended common-source stage followed by a passive balun and a differential stage with 3-bit gain control, and has a measured gain of 16 dB and an NF of 2.7-2.8 dB at the maximum gain state at 28 GHz (Fig. 5.3).

The RX channel linearity is limited by the VM IP1dB of -7 dBm, and reducing the gain before the VM improves the RX linearity. However, current steering in the LNA results in a constant IP1dB against gain control, and thus does not necessarily improve the system linearity. To solve this, a switched-attenuator based on two reverse-saturated HBTs is employed between the two LNA stages to increase the linearity of the RX channel in low gain modes at the cost of higher NF (Fig. 5.3). A small switch size of 3 μm is chosen to result in a low off-state capacitance. The LNA is designed to have an IP1dB of -15 dBm and an NF of 2.7 dB which increases to -6 dBm and 5.6 dB respectively when the attenuator is turned on. This results in improved dynamic range for the beamformer in the RX mode.

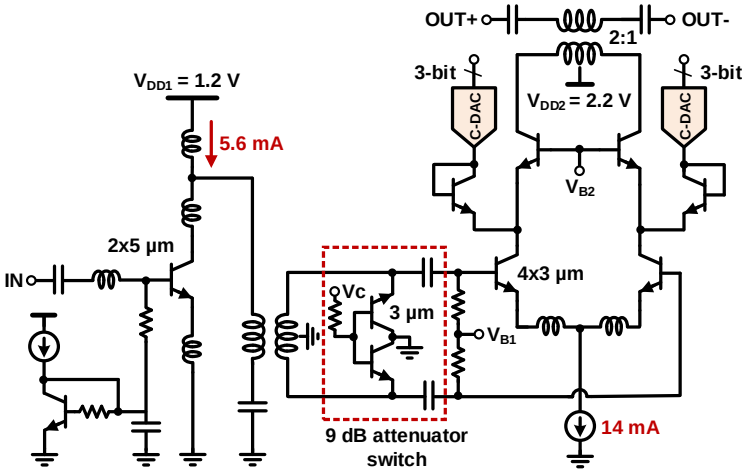

Figure 5.3: Schematic of 2-stage LNA with attenuator switch for improved dynamic range.

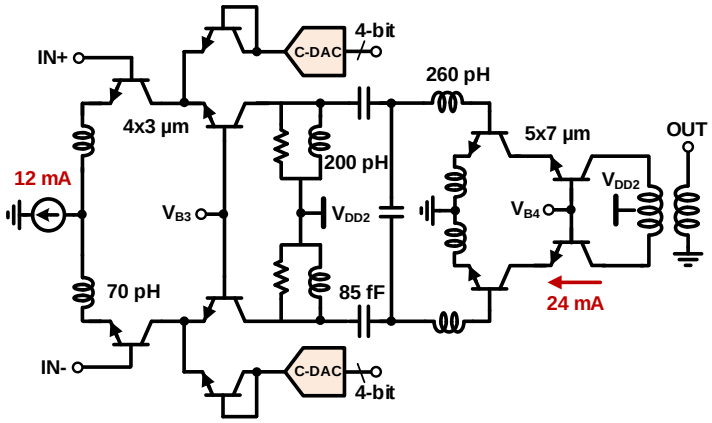

Figure 5.4: Schematic of VGA with 4-bit gain control and PA (bias circuits are not shown).

The TX channel consists of a 4-bit VGA, a 6-bit VM followed by another VGA stage with 4-bit gain control driving a class-AB PA (Fig. 5.4). The TX VGAs employ a similar current steering method for gain control as in the LNA. The PA is a differential cascode design with 25 pH emitter degeneration for improved linearity and is biased in class-AB with some gain peaking for improved efficiency. A transformer balun is used at the PA output to enable single-ended routing from the chip to the antennas. The PA has a simulated OP1dB of 13.8 dBm with a PAE of 18.8% at P1dB and can deliver a saturated output power of 14.9 dBm with a simulated

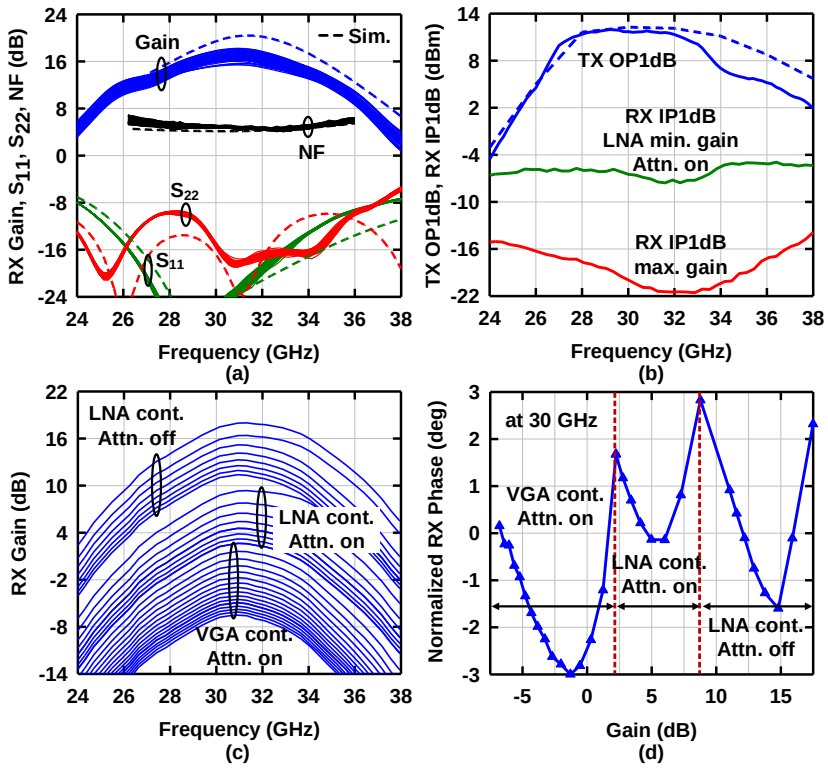

Figure 5.5: Measured (a) RX S-parameters and NF for all phase states, (b) TX OP1dB and RX IP1dB, (c) RX gain control, (d) RX phase change vs. gain control.

PAE of 23.6%, all at 28 GHz (including balun loss). The PA is followed by a single-ended SPDT switch with 1.8 dB loss when driven at 13.8 dBm power and this results in a TX OP1dB of 12 dBm per channel.

5.2.2 2×4 Beamformer Chip Measurements

The 2x4 TRX beamformer quad chips were fabricated in the Jazz SBC18H3 SiGe BiC-MOS process with a die size of 4.8 x 4.8 mm^2 and a minimum pad spacing of 400 μm for chip-scale packaging (Fig. 5.7). Probe measurements of a single channel are shown in Fig. 5.5. The RX gain is 15.5-18 dB over all phase states (rms gain error of 0.6 dB) and with a measured NF of 4.8 dB [Fig. 5.5(a)]. The RX IP1dB is -21 dBm and increases to -7 dBm when the LNA is set to minimum gain and the 9 dB attenuator is turned on [Fig. 5.5(b)]. The TX OP1dB is

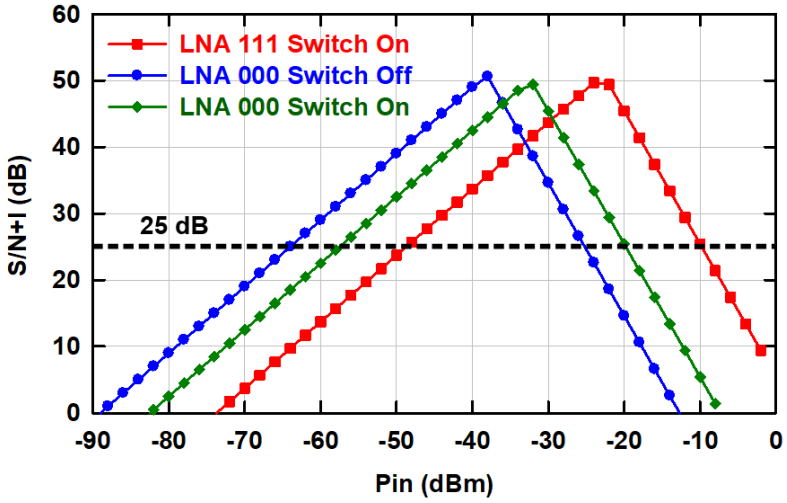

Figure 5.6: Measured signal-to-noise-and-interference ratio for a 100 MHz channel at 30 GHz.

11-12 dBm at 28-32 GHz with a gain of 21 dB, including the 6 dB division loss to 4 channels, and results in a PAE of 7.2% (includes all gain and phase functions, PA, balun and switch). The chip consumes 150 mW per channel in the RX mode due to the very high linearity and 220 mW in the TX mode.

Fig. 5.5(c) presents the gain states in the RX mode. The total gain control range is 25 dB including the two VGA stages and the 9 dB LNA attenuator with a corresponding phase change of only $\pm 3^\circ$ [Fig. 5.5(d)]. The low phase change is achieved at a much higher gain control range compared to previous work [8,59] since the gain control is distributed over multiple stages within the channel.

5.3 System Measurements

5.3.1 2×2 Dual-Polarized Dual-Beam Array Measurements

The chip was flipped on one side of a PCB with a 2x2 dual-polarized antenna array placed on the other side (Fig. 5.7). The antenna is a probe-fed dual-polarized stacked patch design with a -10 dB impedance bandwidth of 28-32 GHz. Two feeds for the V- and H-polarizations are

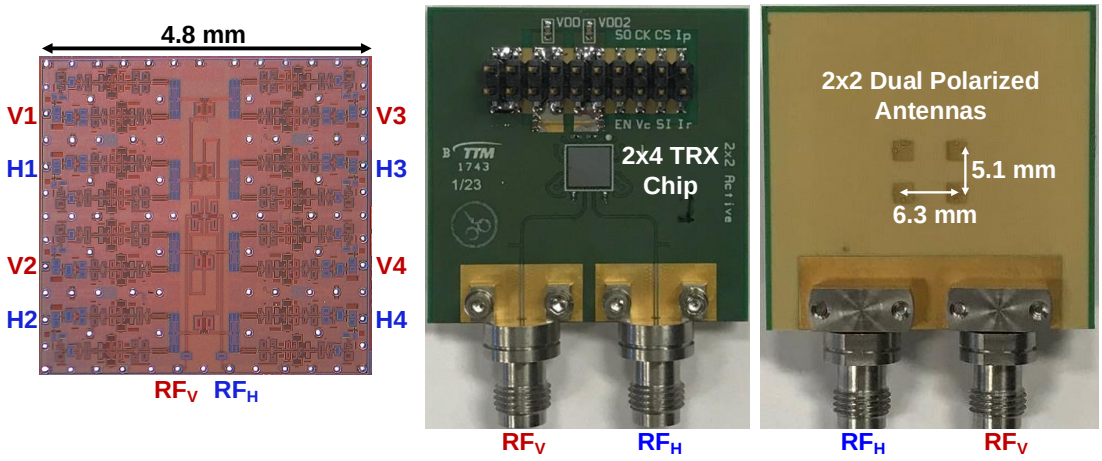

Figure 5.7: Top and bottom views of the 2x2 dual-polarized dual-beam array PCB with flipped die. Chip photograph is also shown with a size of 4.8 x 4.8 mm^2.

connected to the 2x4 TRX chip with a simulated line loss <0.6 dB.

The 2x2 dual-polarized array was first measured in the RX mode using a VNA and with a standard-gain horn antenna as the transmitter. The phase difference due to the different line lengths between the chip and the 2x2 dual-polarized antenna feeds was first corrected using the phase shifter in each channel. Note that this correction was based on simulated line phase difference and not on individual channel measurements. The measured RX frequency response agrees well with the probe measurements and the cross-pol. level is <-27 dB for both polarizations [Fig. 5.8(a) and (b)]. The dip at 33 GHz is due to the onset of the odd-mode resonance of the stacked patches and agrees with simulations.

Fig. 5.8(c) presents the 6-bit phase response for the H-pol. in the RX mode at 29 GHz and is measured by sweeping the phase of all four channels together. The measured response for 64 phase states shows little deviation from the ideal line with an rms phase error <4°. The 2x2 antenna array results in a measured EIRP of 26.2-26.5 dBm at P1dB at 29 GHz for both polarizations [Fig. 5.8(d)]. All measured responses are similar for both polarizations.

The signal-to-noise-and-interference (S/N+I) ratio is calculated for a 100 MHz RX channel centered at 30 GHz based on the NF and linearity measurements in Fig. 5.6 for different gain settings. The RX channel can achieve an S/N+I ratio >25 dB at an input power of -64 to

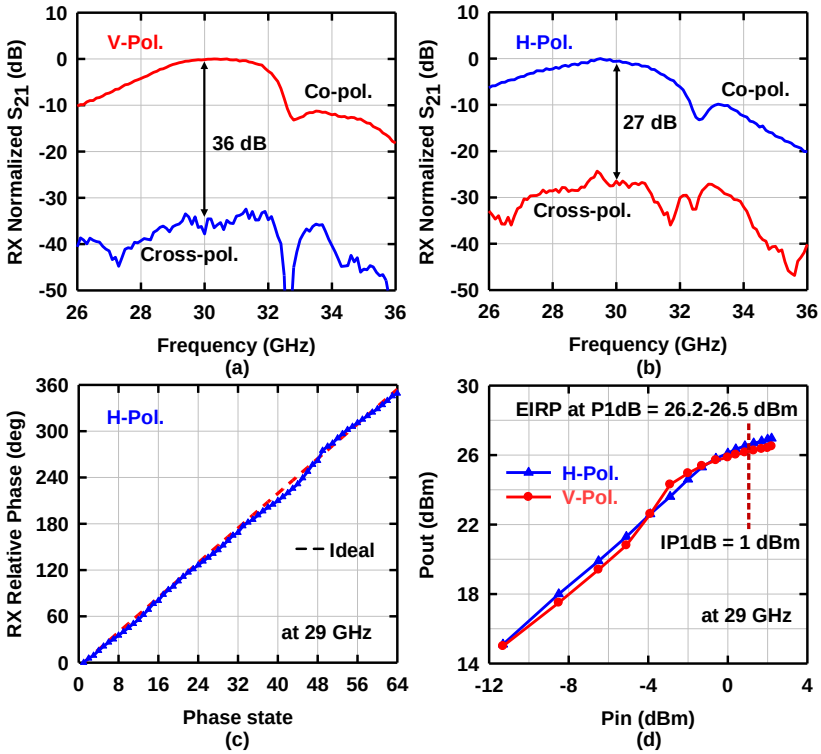

Figure 5.8: Measured co-pol. and cross-pol. in the far-field for (a) V- and (b) H-polarizations in the RX mode, (c) phase states in the RX mode and (d) EIRP at 29 GHz.

−10 dBm which allows the RX channel to be used with 64-QAM signals over a wide dynamic range. The RX dynamic range is significantly improved since the RX linearity improves with reduced RX gain, achieved using the 9 dB attenuator switch and the high-linearity design LNA with gain control on its second stage.

5.3.2 2×2 MIMO Link Measurements

A dual-beam polarization-based 2x2 MIMO link was measured using the setup shown in Fig. 5.9(a). Two independent data streams of 16-/64-QAM signals are simultaneously generated at an RF of 29 GHz using two channels of a Keysight M8195A AWG. The modulated waveforms are amplified and fed into the dual-polarized dual-beam 2x2 antenna array board set in the TX mode. The waveforms are received by another 2x2 antenna array in the RX mode at 1 m link distance, downconverted to an IF of 4 GHz and amplified (using external mixers and

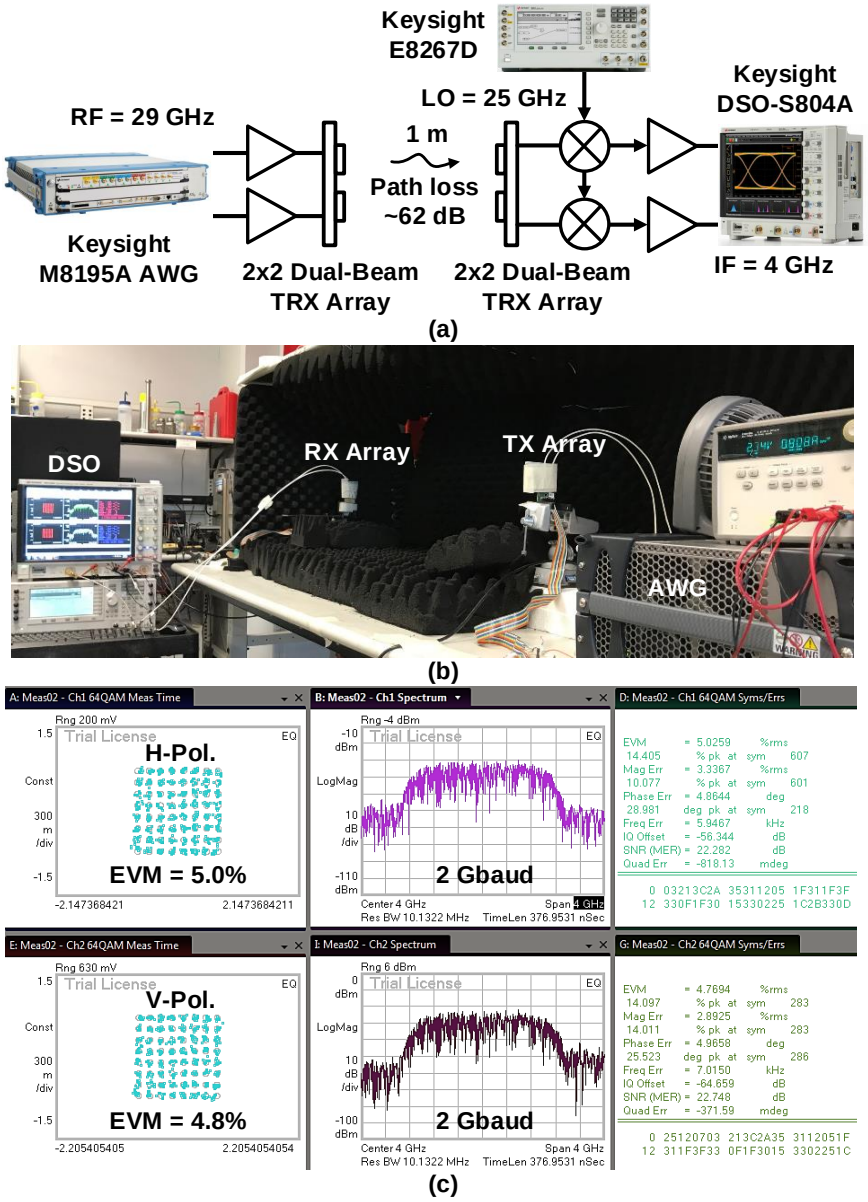

Figure 5.9: (a) Measurement setup of the polarization based 2x2 MIMO link using two 2x2 dual-beam TRX arrays. (b) Photograph of the measurement setup. (c) Measured simultaneous constellations of 2x12 Gbps (2 Gbaud per pol.) 64-QAM link at 8 dB backoff with 4.8-5.0% EVM.

IF amplifiers). The received waveforms are demodulated simultaneously using two channels of a Keysight DSO-S804A oscilloscope running the VSA 89600 software. A photograph of the measurement setup is shown in Fig. 5.9(b).

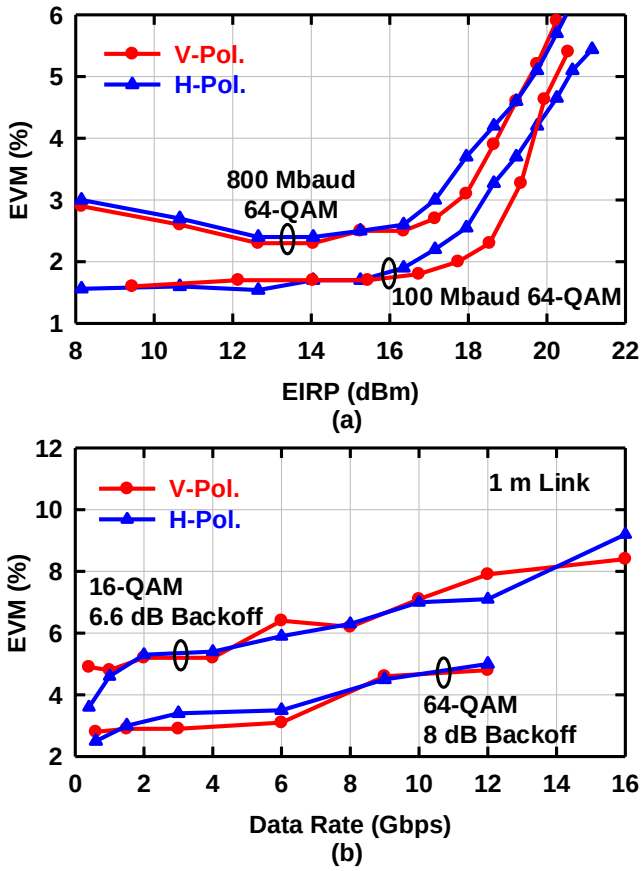

Figure 5.10: Measured EVM at (a) different backoff levels for 100/800 Mbaud 64-QAM and (b) EVM at different data rates using 16-QAM at 6.6 dB backoff and 64-QAM at 8 dB backoff from P1dB for a 1 m 2x2 MIMO link.

The EVM was first measured using 100 Mbaud and 800 Mbaud 64-QAM waveforms with different power levels [Fig. 5.10(a)]. The measurements were performed with both data streams operating at the same time. It was observed that turning on the second data stream results in only $\sim$0.5% degradation in EVM due to the low cross-polarization levels of the antennas. Since the 64-QAM waveform filtered with a roll-off factor of 0.35 has a peak-to-average power ratio of 7.7 dB, the EVM starts to increase beyond the 8 dB backoff level defined as the difference between the average symbol power and the array EIRP at P1dB.

EVM was then measured using 16-QAM at 6.6 dB backoff and 64-QAM at 8 dB backoff from P1dB at different modulation bandwidths and the results are presented in Fig. 5.10(b). The

2x2 MIMO link can achieve a data rate of 24 Gbps (12 Gbps per polarization) using 3 Gbaud 16-QAM or 2 Gbaud 64-QAM. A peak data rate of 32 Gbps (16 Gbps per polarization) was measured using 4 Gbaud 16-QAM with 8.4-9.2% EVM at 6.6 dB backoff. The measured EVM is similar for both polarizations due to the symmetric design and well matched performance of the 2x4 TRX beamformer. A screenshot of the oscilloscope measurement showing two simultaneous constellations with 2 Gbaud 64-QAM and 4.8-5.0% EVM is also shown in Fig. 5.9(c). To our knowledge, this is the first demonstration of a single-aperture 2x2 polarization MIMO link at mm-waves with a record-setting performance of 24 Gbps total data rate using 64-QAM and 32 Gbps total data rate using 16-QAM.

5.4 Conclusion

This chapter demonstrates a 2x4 dual-polarized dual-beam TRX beamformer chip and a 2x2 polarization MIMO link with simultaneous measurements achieving 2x12 Gbps data rate using 64-QAM and 2x16 Gbps using 16-QAM. Future work includes the demonstration of long distance 4x4 MIMO links using 64- to 256-element phased-arrays for further increased capacity.

5.5 Acknowledgment

Chapter 5, in part, is a reprint of the material as it appears in: K. Kibaroglu, M. Sayginer, A. Nafe and G. M. Rebeiz, "A Dual-Polarized Dual-Beam 28 GHz Beamformer Chip Demonstrating a 24 Gbps 64-QAM 2x2 MIMO Link," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2018. The dissertation author was the primary investigator and author of this paper.

Chapter 6

Conclusion

This thesis presented 28 GHz phased-array transceivers for Gbps 5G communication links. A 28-32 GHz 2x2 TRX beamformer chip was developed and achieved state-of-the-art performance with 4.6 dB NF, 11-12 dBm OP1dB, 20-25 dB gain control and 6-bit phase control. A 26-31 GHz transceiver chip was also demonstrated with high linearity in the RX mode and high single-sideband rejection in the TX mode to be used for up/down conversion to an IF of 2-6 GHz in a phased-array system. 32-element TRX arrays using eight 2x2 TRX beamformer chips on a very low cost 4-layer PCB and 64-element phased-arrays using sixteen 2x2 TRX beamformer chips on a 12-layer PCB with wideband stacked-patch antennas and an embedded Wilkinson network were also demonstrated. The arrays results in excellent performance without any calibration due to the symmetric design of the 2x2 TRX chips and the Wilkinson network on the PCB.

A 5G communication link with a record-setting data rate of 8-12 Gbps was established over all scan angles at a distance of 300 m using two 64-element TRX phased-arrays and 16-/64-QAM waveforms. To increase the data rate further with 2x spectral efficiency, a 2x4 dual-polarized dual-beam TRX beamformer was designed and a polarization-based 2x2 MIMO link was demonstrated at 1 m link distance with a record-setting data rate of 32 Gbps using 16-QAM and 24 Gbps using 64-QAM waveforms.

6.1 Future Work

The phased-arrays demonstrated in this work included 2x2 beamformer chips combined with antennas and Wilkinson networks on low-cost PCBs. The 28 GHz transceiver chip was tested separately to characterize each design individually. Future work can incorporate the transceiver on the same phased-array PCB as the beamformer chips and include integrated LO generation as well as LDOs to demonstrate a complete system.

The 2x2 beamformers can be designed to have higher bandwidth to cover additional 5G bands along with wider bandwidth stacked-patch antennas on the PCB. Ultra-wideband 5G phased-arrays covering all 5G bands (24-64 GHz) can also be demonstrated based on the same RF beamforming architecture using 2x2 TRX beamformers.

A large-scale phased-array based on dual-polarized dual-beam 2x4 TRX chips can be built to demonstrate polarization-based 2x2 MIMO links over all scan angles at link distances on the order of hundreds of meters. The capacity can be increased further by building a 4x4 MIMO system with 2V and 2H beams operating simultaneously with polarization-equalization in the digital domain [62, 63]. Full-duplex operation [60, 61] can also be incorporated in the polarization-based MIMO system to result in 4x data rate and spectral efficiency with two beams transmitted and received on both polarizations at the same time.

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