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Performance-Optimized Terahertz Signal Sources in Silicon

DISSERTATION

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for the degree of

DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

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Dissertation Committee:

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Professor Ozdal Boyraz

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2014

DEDICATION

To

Mom, Dad, and Yi-Shan

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Publications

[1] Z. Wang, **P.-Y. Chiang**, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564-580, March 2014

[2] **P.-Y. Chiang**, O. Momeni, and P. Heydari, "A 200GHz inductively tuned VCO with −7dBm output power in 130nm SiGe BiCMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 10, pp. 3666-3673, Oct. 2013

[3] **P.-Y. Chiang**, C.-W. Su, S.-Y. Luo, R. Hu, and C. F. Jou, "Wide-IF-band CMOS mixer design," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 831-840, April 2010

[4] **P.-Y. Chiang,** Z. Wang, O. Momeni, and P. Heydari, "A 300GHz frequency synthesizer with 7.9% locking range in 90nm SiGe BiCMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 260–261

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ABSTRACT OF THE DISSERTATION

Performance-Optimized Terahertz Signal Sources in Silicon

By

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Doctor of Philosophy in Electrical and Computer Engineering

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Professor Payam Heydari, Chair

Terahertz (THz) and sub-millimeter wave band are known to provide unique applications in spectroscopy, imaging and high-data-rate wireless communication. An imaging system operating in this frequency region exhibits non-invasive and high-resolution characteristics due to the non-ionized and short-wavelength radiation waves, which makes it attracting for security surveillance. On the other hand, the THz wireless transceiver operating in the license-free spectrum is capable of achieving tens of gigabits-per-second by utilizing a simple modulation scheme. All the benefits mentioned above make THz a promising research topic. Towards realization of a high-performance THz system, one of the most challenging steps is to design a frequency synthesizer.

A voltage-controlled oscillator (VCO) is one of the important building blocks within a synthesizer. Due to the server performance degradation of varactors and

transistors at high frequencies, new ways of designing VCOs need to be investigated. Here, two different ideas are proposed. First, an inductive-tuning mechanism with high quality-factor and wide tuning-range is introduced. This tuning technique is based on a variable inductor seen at the emitter terminal of a base-degenerated transistor. By adding a series *RL* at the base terminal, the variable inductor, exhibiting low loss and high tunability, improves the VCO output power and phase noise while achieving a wide tuning range. The second idea, double-stacked cross-coupled VCO, is to design a strong negative resistance cell to compensate for the server loss of the varactor at THz frequencies. By implementing a source-degenerated negative resistor of a conventional cross-coupled pair, the overall negative resistance is enhanced. It also reduces the parasitic capacitance, making it an attracting approach for THz applications.

Finally, a novel THz frequency synthesizer is proposed. A 300GHz phase-locked-based synthesizer incorporating a triple-push VCO with Colpitts-based active varactor (CAV) and a three-phase injection locked divider is introduced. The CAV is used to tune the oscillation frequency, enhance output power, and buffer the VCO's fundamental signal. The divider's locking-range is vastly increased attribute to the three-phase injection. This work demonstrates the highest-frequency synthesizer in silicon.

Chapter 1

Introduction

Terahertz (THz) band, extending from the highest millimeter-wave (mm-wave) frequency range to the lowest infrared frequency, has drawn great attention. Recent research in the THz region is expanding to wide range of applications such as spectroscopy, imaging, and ultrahigh-data-rate wireless communications [1]–[6]. For imaging applications, due to the short wavelength and non-ionized characteristic of the THz wave, it provides a non-invasive and high spatial resolution image detection, which fits the requirement of security surveillance including stand-off imaging for detection of hidden objects [7], [8]. The SNR and the resolution can be improved by utilizing a synchronized carrier for time integration. For wireless communication applications, the availability of very wide un-used bandwidth in the THz spectrum makes it possible to build up a wireless data-link with data rates in excess of tens of gigabits-per-second using only a simple modulation scheme such as amplitude-shift keying (ASK) or on-off keying (OOK) [9]–[13]. Due to large atmospheric attenuation of THz waves, one promising application of this spectrum is in the area of scientific satellite communication [14], [15].

Towards realization of a high-performance THz system, one of the most

challenging steps is to design high-power, tunable and efficient voltage controlled oscillators (VCO) and frequency synthesizers. For VCO, a conventional and widely used way of controlling the oscillation frequency is to implement varactors in an LC oscillator [16], [17]. However, tight trade-off exists between quality factor (Q factor) and *Cmax*/*Cmin* tuning ratio of varactors, which will be more stringent at high frequencies. While the use of minimum-length varactors can improve Q factor, it decreases tuning ratio due to parasitic capacitors. Furthermore, varactors' loss varies significantly across the tuning range, resulting in dramatic variation in output power due to the limited negative resistance that transistors can provide. Recently, silicon-based signal sources at low-THz range (e.g., 200- and 300-GHz) using coupled VCOs and harmonic generation have been reported [18]–[20]. [21] presents a SiGe 530 GHz array-based radiator comprising 16 radiating elements each with its own ring-antenna and balanced triple-push oscillator with no tuning capability.

Despite the VCO design challenges, a free-running signal source exhibits severe frequency fluctuation and is vulnerable to temperature, voltage and process (PVT) variations. Moreover, the VCOs reported in prior work exhibit limited tuning range, not often sufficient to tackle these variations and meet bandwidth requirements of the systems they are designed for. For example, in a radar system, both bandwidth and frequency of operation contribute to the resolution, in that, the former affects the

cross-range resolution while the latter contributes to the range resolution [22]. Consequently, the need for precise oscillation frequency with wide tuning range and low close-in phase-noise calls for closed-loop source topologies. Millimeter-wave phase-locked loops (PLLs) incorporating push-push VCOs have been demonstrated up to 164 GHz [23] in silicon technologies. M. Seo, *et al*. presented a 300 GHz PLL with 0.12 % locking range and divider ratio of 10 in a III-IV technology [24]. Due to the low divider ratio, the PLL in this work demands a high-frequency input reference signal which could be generated from another PLL, resulting in a high phase-noise and system complexity.

This thesis includes two individual VCOs operating at 200 GHz and a 300 GHz frequency synthesizer. In Chapter 2, a highly efficient push-push VCO with a new inductive frequency-tuning topology for (sub) THz frequencies is proposed and discussed. In Chapter 3, a new double-stacked cross-coupled VCO operating at the fundamental 200 GHz is presented. The 300 GHz frequency synthesizer is presented in Chapter 4. Finally, the conclusion is in Chapter 5.

Chapter 2

A 200GHz Inductive-Tuning VCO in 0.13μm SiGe BiCMOS

A highly-efficient push-push VCO with a new inductive frequency tuning topology is presented. The tuning technique is based on the variable inductance seen into the emitter terminal of a base-degenerated transistor. The variable inductor exhibits high quality factor and high tuning range due to the tunable transistor transconductance via bias current. Fabricated in a 0.13μm SiGe BiCMOS process with f_{MAX} of 260 GHz, the VCO achieves a tuning range of 3.5% and an output power of −7.2 dBm at 201.5 GHz.

2.1 Frequency-Tuning of An *LC* Tank

Shown in Fig. 2.1 is an *LC* tank with a negative-resistance cell where Q_C and Q_L represent the Q factors of the capacitor and the inductor respectively. If the negative-resistance cell, which is usually implemented using cross-coupled or Colpitts topologies, compensates for the loss of the *LC* tank, then the *LC* tank starts to oscillate. The oscillation frequency ω_{osc} and Q factor of the tank Q_{tank} are expressed as

$$\omega_{osc} = \frac{1}{\sqrt{L(C+C_P)}}, \text{ and } Q_{tank} = \frac{Q_C Q_L}{Q_C + Q_L} \tag{2.1}$$

where C_p denotes the parasitic capacitor of the negative resistor. The conventional varactor-tuning is losing its advantages at high frequencies.

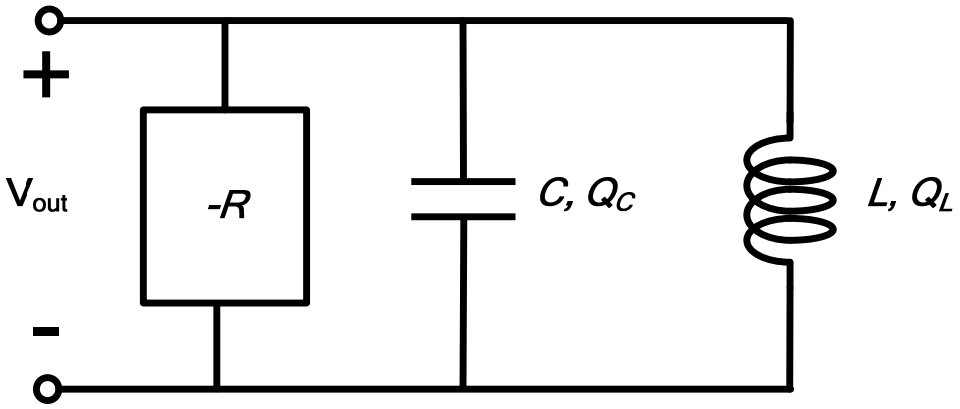


Fig. 2.1. An *LC* tank with negative resistance.

The parasitic capacitors dominate the total capacitance and degrade the tuning range. Furthermore, low Q factor of varactors (i.e., only 2~5 at 100 GHz) decreases the Q factor of the *LC* tank, leading to small output power and high phase noise. On the other hand, as oscillation frequency increases towards THz band, the inductor size will decrease almost quadratically. This implies: (1) achieving Q factor of 15~20 for small size inductors (around hundred pH) is possible, and (2) high magnetic coupling can be achieved. Therefore, inductive-tuning VCOs are considered to be viable candidates for wider tuning range and higher output-power across the band at mm-wave and THz frequencies. Varactor-less VCOs using transformer coupling feedback have already been proposed for wide tuning range and high Q factor *LC* tank [25]–[27]. The tuning range of this transformer coupled

inductance degrades at high frequencies due to the low transconductance of transistors.

2.2 Inductive-Tuning Mechanism Using *RL*-Degenerated Transistor

It is commonly known that an emitter follower circuit with a small base resistor generates an inductive reactance seen at the emitter terminal. Also, an inductor placed at the base terminal causes the emitter follower circuit to go to unstable region due to the negative resistor at the emitter terminal. Here we investigate a series *RL* circuit to be employed as degeneration network of an emitter follower circuit for frequency tuning (i.e., a variable inductor). To illustrate the idea, we first look into a differential base-degenerated amplifier shown in Fig. 2.2 (a). The circuit is comprised of transistors T_3–T_4, the series *RL* network R_{BB}–L_{BB}, and a tail current I_E. The input impedance Z_{in} is expressed as

$$Z_{in}=\frac{R_{BB}+r_\pi+j\omega(L_{BB}+r_\pi C_\pi R_{BB})-\omega^2 r_\pi C_\pi L_{BB}}{1+g_{m3,4}r_\pi+j\omega r_\pi C_\pi} \tag{2.2}$$

$$\cong\frac{(R_{BB}+r_\pi-\omega^2 r_\pi C_\pi L_{BB})(1+j\omega/z_0)}{g_{m3,4}r_\pi(1+j\omega/p_0)} \tag{2.3}$$

$$=R_1\|j\omega L_1+R_2 \tag{2.4}$$

in which,

$$z_0=\frac{R_{BB}+r_\pi-\omega^2 r_\pi C_\pi L_{BB}}{L_{BB}+r_\pi C_\pi R_{BB}},\quad p_0=\frac{g_{m3,4}}{C_\pi}=\omega_T \tag{2.5}$$

and

$$R_2=\frac{R_{BB}}{g_{m3,4}r_\pi}+\frac{1}{g_{m3,4}}-\frac{\omega^2 L_{BB}}{\omega_T} \tag{2.6}$$

Assume $g_{m3,4}r_\pi \gg 1$, (2.2) is simplified to (2.3), which resembles the expression

for the impedance of a network comprising a parallel R_1-L_1 in series with R_2, as shown in Fig. 2.2(b). Replacing (2.5) and (2.6) into (2.2) results in closed form expressions for R_1 and L_1:

$$\begin{aligned} R_1 &= R_2\left(\frac{p_0}{z_0}-1\right) \\ &= R_{BB}-\frac{1}{g_{m3,4}}+\left(\left(\frac{\omega}{\omega_T}\right)^2+\frac{1}{g_{m3,4}r_\pi}\right)\omega_T L_{BB} \end{aligned} \tag{2.7}$$

$$L_1=\frac{R_1}{p_0}=\frac{R_{BB}}{\omega_T}-\frac{1}{g_{m3,4}\omega_T}+\left(\left(\frac{\omega}{\omega_T}\right)^2+\frac{1}{g_{m3,4}r_\pi}\right)L_{BB} \tag{2.8}$$

Replacing (2.6)–(2.8) into (2.4) yields a closed form expression for driving point impedance seen from the emitter terminal of T_3, i.e.,

$$\begin{aligned} Z_{in} &\cong \frac{1}{g_{m3,4}}-\frac{\omega^2 L_{BB}}{\omega_T}+\frac{\omega^2 R_{BB}}{\omega_T^2}+j\omega\left[\frac{R_{BB}}{\omega_T}-\frac{1}{g_{m3,4}\omega_T}+\frac{\omega^2 L_{BB}}{\omega_T^2}\right] \\ &= R_{EFF}+j\omega L_{EFF} \end{aligned} \tag{2.9}$$

R_2 in (2.6) is dominated by the last two terms, as R_{BB} (in the range of tens of ohms) is divided by the transistor's current gain, $\beta_{3,4}$ (≥100). R_2 will be equal to $1/g_{m3,4}$ if there is no L_{BB} and R_{BB}, as expected. L_{BB} contributes a negative term to both R_2 and Z_{in}, thereby decreasing equivalent series loss of the variable inductor. R_{BB} is added to have inductance tuning ability via I_E. From (2.8), R_{BB} helps to boost variable inductance. From (2.9), one can infer that the equivalent inductor L_{EFF} varies with I_E (through $g_{m3,4}$). Furthermore, R_{EFF} is reduced due to L_{BB}, resulting in a higher Q factor.

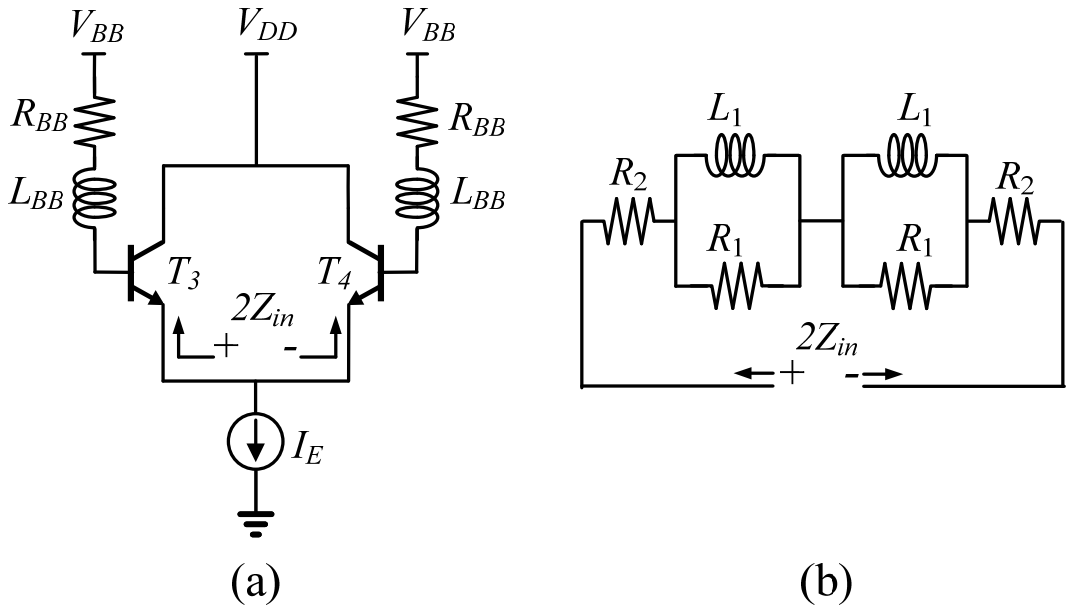


Fig. 2.2. (a) The differential *RL*-degenerated transistor pair, and (b) its equivalent circuit.

Fig. 2.3 shows the simulated L_{EFF} as a function of frequency with differential tail current I_E varying from 2~12 mA. In this simulation, the transistor size is 6μm/0.13μm, R_{BB} is 15 Ω, and L_{BB} is 60 pH. From Fig. 2.3, as I_E increases from 2 mA to 12 mA, L_{EFF} decreases from 70 pH to 30 pH at the 100 GHz fundamental frequency. Trade-off exists between L_{EFF}'s tuning range and its Q factor, as both L_{EFF} and R_{EFF} are directly affected by R_{BB}. Shown in Fig. 2.4 (a) is L_{EFF} vs. I_E at 100 GHz with three different values of R_{BB} where L_{BB} is 60 pH. The simulated L_{EFF} increases with R_{BB}, while L_{EFF}–I_E variation follows the same behavior for all these three values of R_{BB}'s. Fig. 2.4 (b) depicts simulated Q factor of L_{EFF} with respect to I_E, and shows that a higher value of R_{BB} results in a lower Q factor. Fig. 2.5 shows the simulated Q factor at 100 GHz vs. I_E for three different values of L_{BB}, where R_{BB}

is fixed at 15 Ω. In the low I_E region, the Q factor is low because the transistors are not fully biased in forward active region. Once the transistors are biased in forward active region, the Q factor starts to increase. The Q factor is boosted from 5 to 25 at I_E =10 mA when L_{BB} increases from 50~ 60 pH. This notion is also verified in (2.9). Note that if L_{BB} is chosen to be too large, it may cause an undesired oscillation due to the fact that the negative part of R_{EFF} will start dominating the other terms.

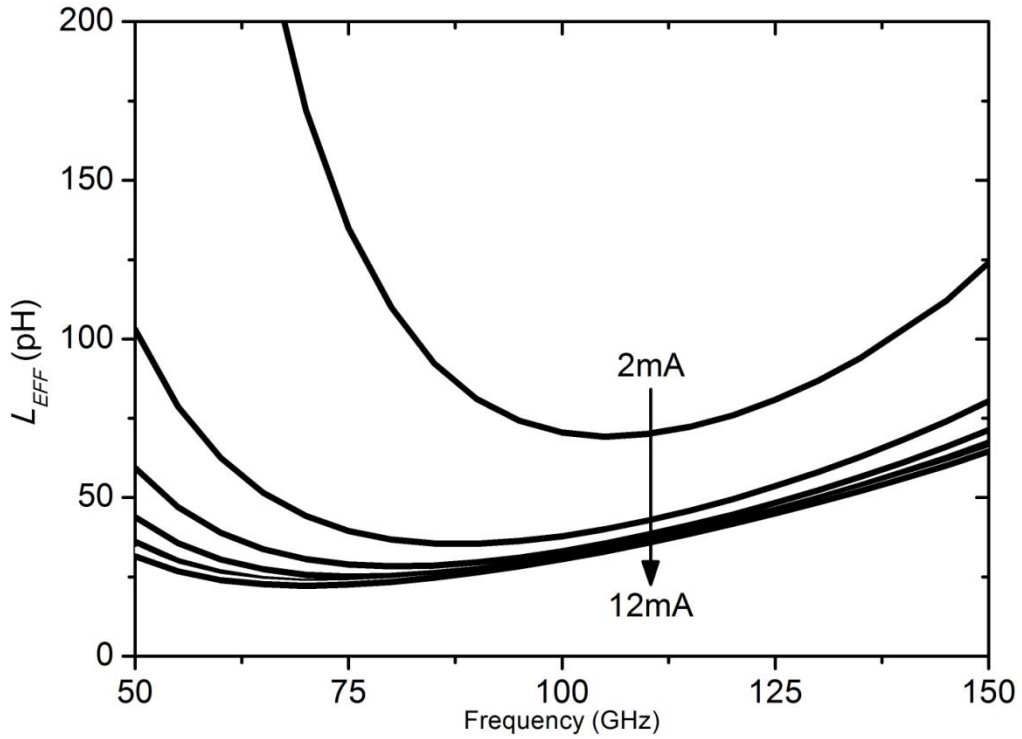


Fig. 2.3. The simulated L_{EFF} with respect to frequency for different values of I_E from 2~ 12 mA.

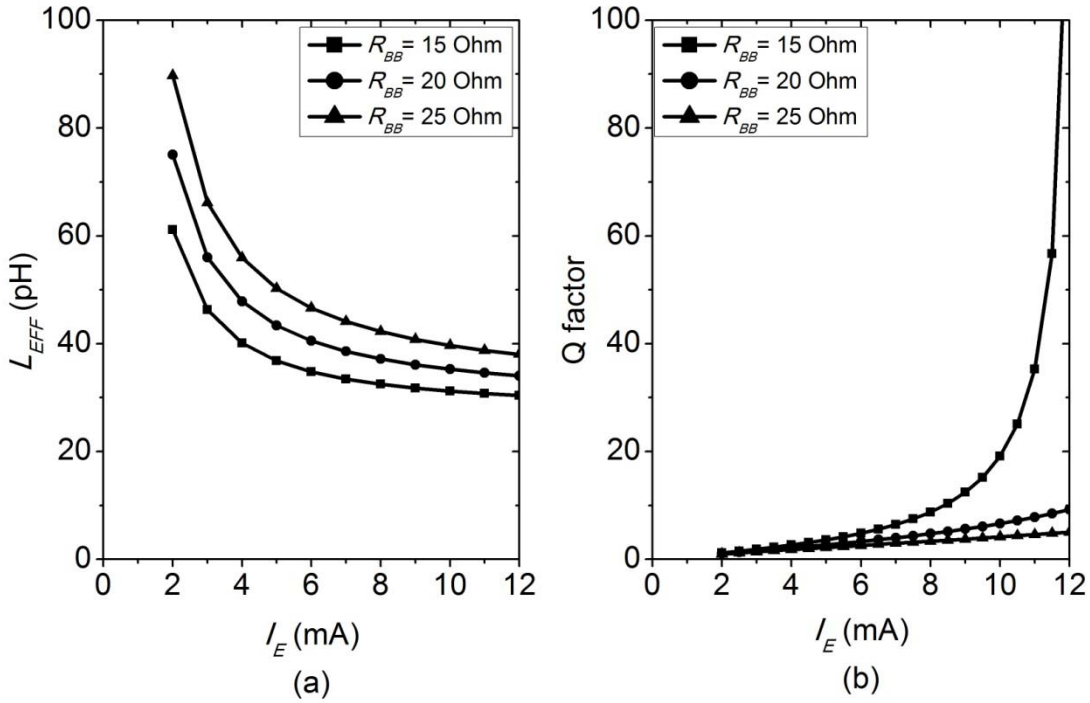


Fig. 2.4. (a) The simulated L_{EFF} versus I_E at 100 GHz for three different values of R_{BB}, and (b) its corresponding Q factor.

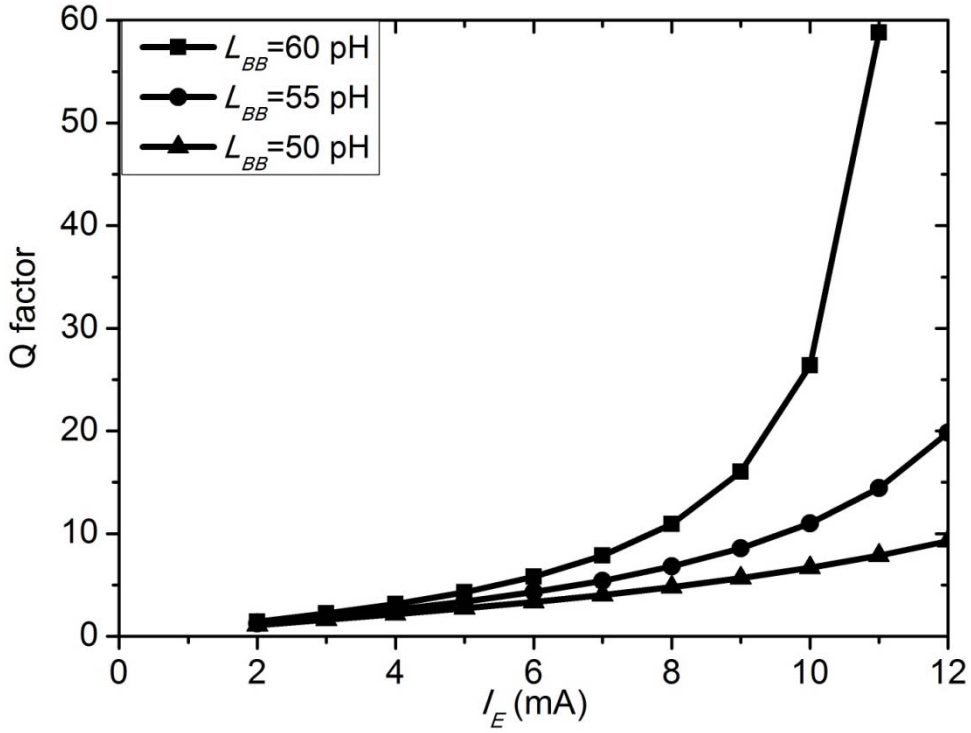


Fig. 2.5. The simulated Q factor of L_{EFF} at 100 GHz with three values of L_{BB}.

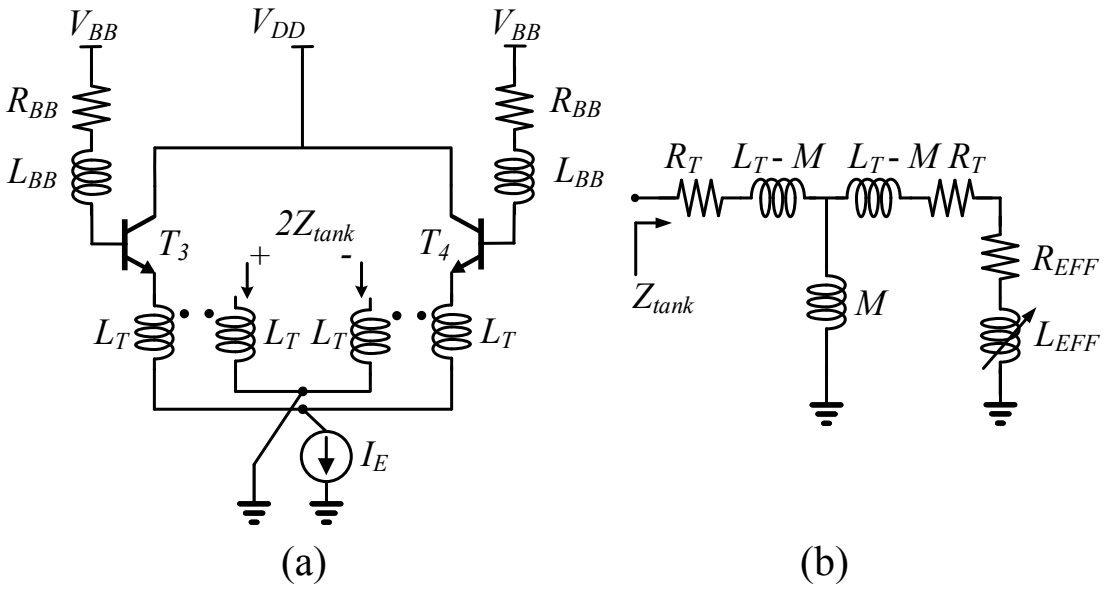


Fig. 2.6. (a) The proposed transformer coupled inductive tuning circuit, and (b) It's half equivalent circuit.

2.3 Transformer Coupled Inductive-Tuning Circuit

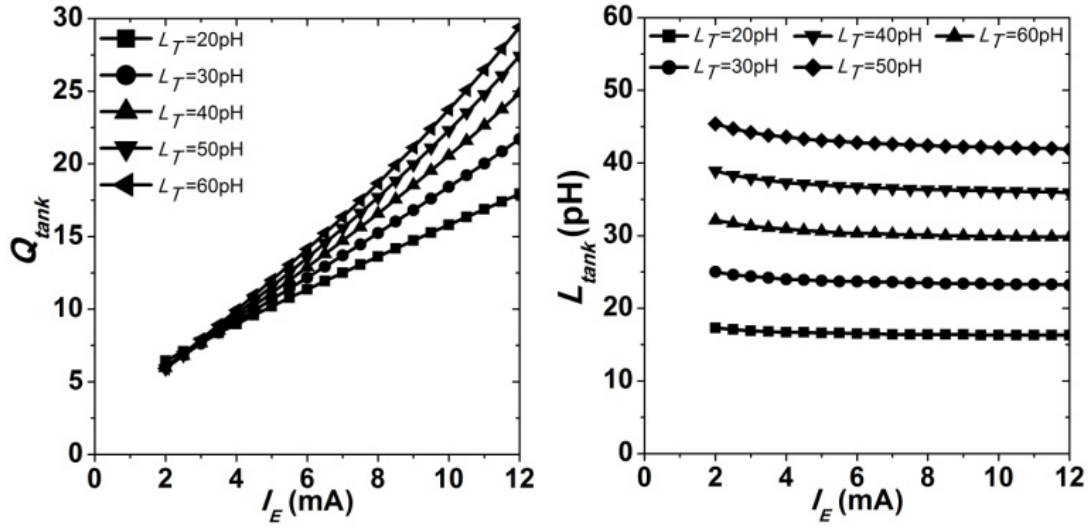
The proposed inductive-tuning circuit is shown in Fig. 2.6 (a) where a 1:1 differential L_T transformer with coupling factor, k_C, is used to couple L_{EFF} to the oscillator's tank. The transformer isolates the DC bias current of the core oscillator from I_E, which is varying to achieve inductive-tuning. A separate constant DC bias current is necessary for a VCO core because it provides constant negative resistance even in low-current tuning region. Furthermore, transformer coupling decreases the variation of the tank's Q factor. As shown in Fig. 2.5, the Q factor variation with a constant L_{BB} can be as high as 55. Such variation leads to significant change in VCO output power, or it may even dampen the oscillation in low Q region. To address this, the half equivalent circuit of the differential transformer coupled inductive-tuning

circuit in Fig. 2.6 (a) is shown in Fig. 2.6 (b). A *T* model [28] is used to represent the 1:1 transformer in Fig. 2.6 (a). R_T represents the series loss of primary and secondary inductors and *M* denotes the mutual inductance. Assuming Q^2 of both the transformer and L_{EFF} to be much larger than 1, Z_{tank} is expressed as

$$Z_{\text{tank}} \cong R_T + \frac{(R_T + R_{EFF})M^2}{(L_T + L_{EFF})^2} + j\omega\left(\frac{L_T L_{EFF} + L_T^2 - M^2}{L_T + L_{EFF}}\right) \qquad (2.10)$$

According to (2.10), Z_{tank} will retain higher percentage of the tuning range contributed by L_{EFF} as the transformer coupling increases, and thus, the transformer is designed to achieve k_C factor of 0.7 and the Q factor of 15. Shown in Fig. 2.7 (a) is the simulated Q factor of Z_{tank}, Q_{tank}, with different L_T values, where L_{BB} and R_{BB} are set to be 50 pH and 15 Ω, respectively. At low I_E region, Q_{tank} is 6, which is higher than that of L_{EFF} in Fig. 2.5. As I_E increases, Q_{tank} will increase due to the reduction of R_{EFF}. Moreover, higher L_T leads to additional improvement in Q_{tank}, for a given I_E. As also shown in Fig. 2.7 (b), for L_T varying from 20 pH to 60 pH, the tuning range slightly increases from 7% to 9%, while the average value of L_{tank} increases from 18 pH to 45 pH. Therefore, the L_T transformer has to be designed based on the desired oscillation frequency with maximum achievable coupling factor. For the VCO in this work, the parameters are set to be L_T = 30 pH, L_{BB} = 60 pH and R_{BB} = 15 Ω. The corresponding simulation results of L_{tank} and Q_{tank} vs. I_E are shown in Fig. 2.8. The VCO's tank, with the proposed inductive-tuning mechanism,

achieves an overall Q factor of three times higher than that of conventional varactor-tuning *LC* tank at 100 GHz. The Q_{tank} will further increase, towards higher end of tuning range. This helps the flatness of the VCO output power across the tuning range, because the higher Q factor at higher oscillation frequency compensates for the degradation of the transistors' transconductance with frequency.



(a) **(b)**

Fig. 2.7. (a) The simulated quality factor of Z_{tank}, Q_{tank}. (b) The inductor L_{tank} of Z_{tank} at 100 GHz where L_{BB} is 60 pH, R_{BB} is 15 Ω, and the coupling factor, k_C is 0.7.

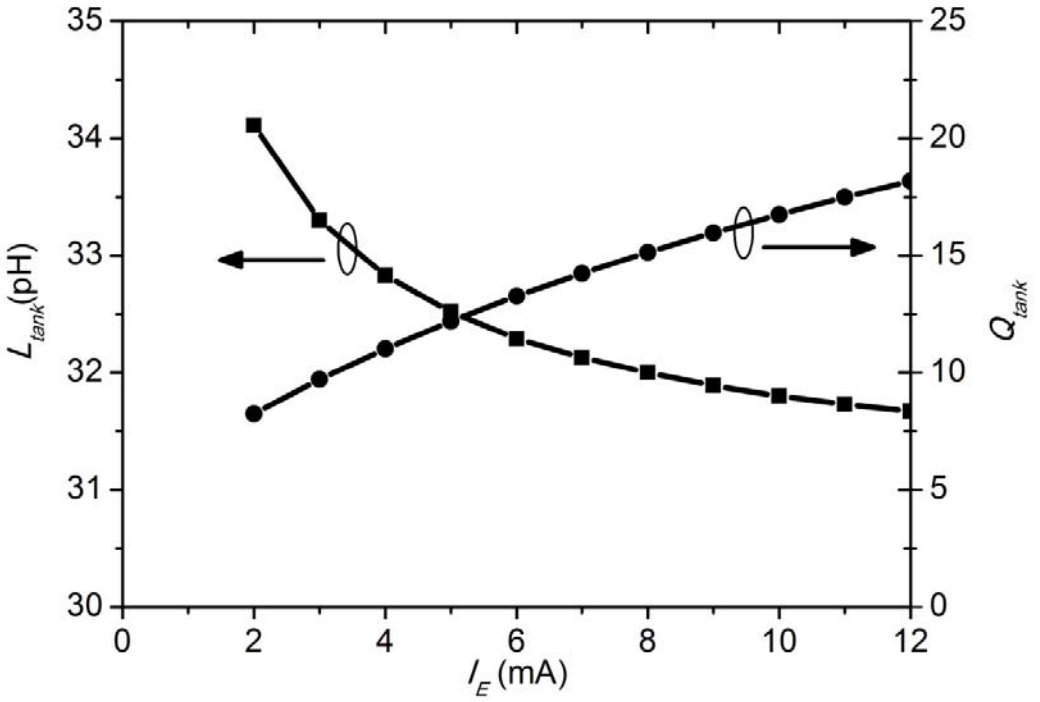
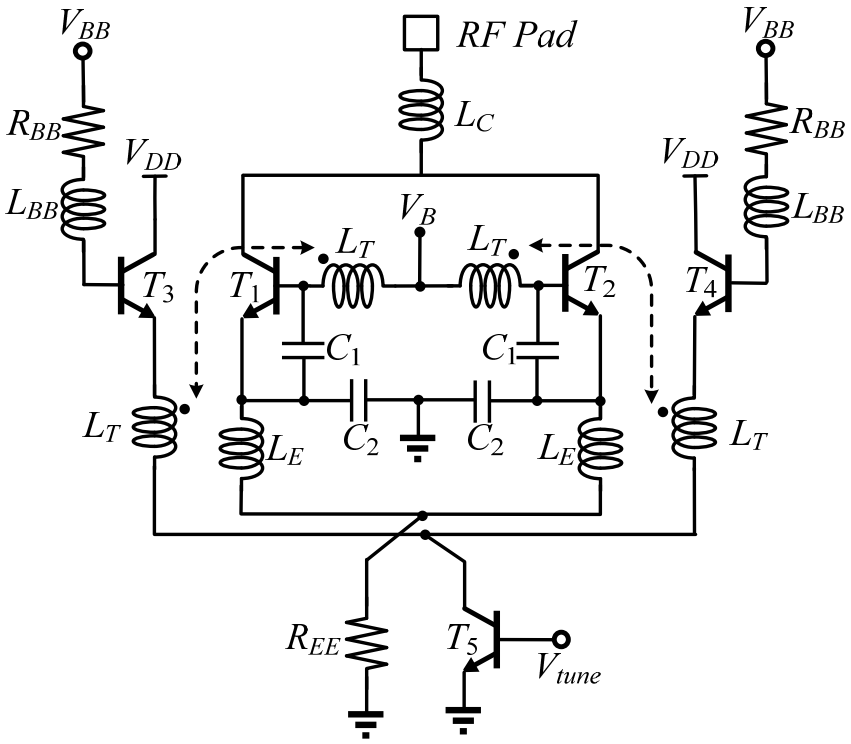


Fig. 2.8. The simulated inductance and Q factor of L_{tank} at 100 GHz where L_T=30 pH, k_C=0.7, L_{BB}=60 pH, and R_{BB}=15 Ω.

2.4 Inductive-Tuning Push-Push VCO

Colpitts topology is proved to achieve higher oscillation frequency than a cross-coupled pair counterpart [29], due to a non-unity gain feedback loop realized using the tapped capacitor resonator, which decreases the capacitance contribution of C_π into the LC tank. Moreover, the phase noise of a Colpitts oscillator is a function of capacitive division ratio [30], making it more flexible to achieve a lower phase noise. Shown in Fig. 2.9 is the proposed schematic of the Colpitts inductive-tuning push-push VCO. Owing to the core circuit comprising the transistor T_1 (T_2) and tapped capacitor network C_1–C_2, a negative resistance can be seen at the base or collector terminals. The tank inductor L_T is placed at the base of

T_1 (T_2) where the inductor loss is compensated by the negative resistance. The VCO oscillation frequency will be $1/[L_T C_1 C_2/(C_1+C_2)]^{1/2}$. Together with the inductive-tuning circuit composed of R_{BB}, L_{BB}, T_3 (T_4), the oscillation frequency is tuned by changing V_{tune}. Note that when the VCO is oscillating, the second harmonic signal, generated from the transistors' non-linearity, can be extracted from any common-mode node of the VCO. In Fig. 2.9, the second harmonics are extracted from the collectors in order to achieve higher output power. The primary reason is that the major portion of the second harmonic current generated by transistors T_1–T_2 flows out from their collector nodes to the output load, while for the other common-mode nodes, the inherent current division will degrade the output power. Also, by placing the tank inductor at the base terminal, the inductor's loss is eliminated in the second harmonic signal path, which would otherwise exist if that inductor would have been placed at collector node. The resistor R_{EE} is used to improve common mode rejection. However, there is a trade-off between second harmonic output power and R_{EE} value to improve common mode rejection, because R_{EE} is in the second harmonic path and could degrade the output power.



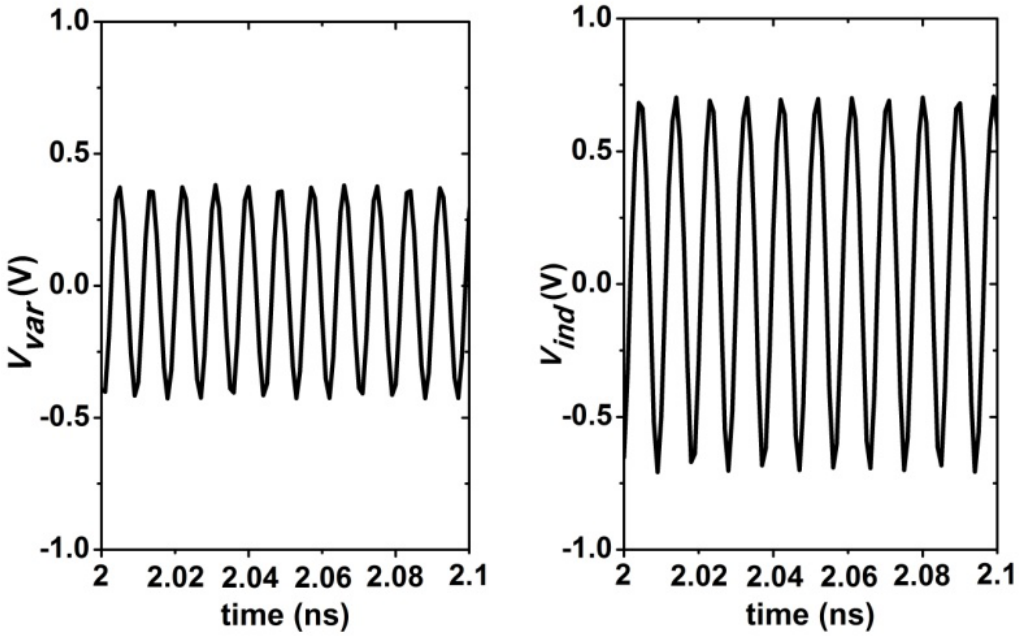
T_1–T_5	C_1	C_2	R_{BB}	R_E	L_T	L_E	L_{BB}
L_E=2×3μm	25fF	86fF	15Ω	38Ω	30pH	55pH	60pH

Fig. 2.9. The proposed inductive-tuning push-push 200 GHz VCO.

The inductor L_C in Fig. 2.9 is modeled as the interconnection from the collectors to the RF pad and is considered as part of the output matching network along with the parasitics of the RF pad. The common-mode node between C_2's is grounded to improve output matching at the second harmonic. With a bias-T implemented on a GSG waveguide probe, the DC supply voltage is applied directly into the circuit, while the signal is brought out from the probe to measurement equipment.

As illustrated in the previous section, the Q factor of the proposed inductive-tuning *LC* tank is higher than that of the conventional varactor-tuning *LC*

tank. To address this, a varactor-tuning VCO with the same oscillation frequency and tuning range is designed for comparison. The simulation shown in Fig. 2.10 is the fundamental voltage swing at the bases of the transistor T_1 (T_2). The proposed inductive-tuning VCO achieves a higher voltage swing than the conventional one. The higher voltage swing implies that: (1) the Q factor of the LC tank is higher so long as the swing does not exceed saturation region, (2) transistors T_1–T_2 generate stronger 2nd harmonic signals, and (3) the VCO phase noise is improved due to the fact that it is proportional to $1/Q_{tank}$ [31]. In addition, from the simulation results, the output power of the proposed inductive-tuning VCO is 3 dB higher than the conventional counterpart.



(a) **(b)**

Fig. 2.10. The simulated fundamental voltage swing at the transistor's base terminal of (a) a Colpitts VCO with conventional varactor-tuning, and (b) the proposed inductive-tuning VCO.

2.5 Measurement

The proposed inductive-tuning VCO was designed and fabricated in a 0.13μm SiGe BiCMOS technology with f_T/f_{MAX} of 240 GHz/ 260GHz. All the transformers and inductors were implemented on the two topmost metal layers, M5–M6, with a ground plain of M1, shielding the loss from the substrate. Fig. 2.11 shows the chip photograph of the VCO where the chip area is 250 × 290 μm^2 excluding the I/O pads. All the elements and routing lines have been placed symmetrically in order to minimize mismatch and improve overall performance.

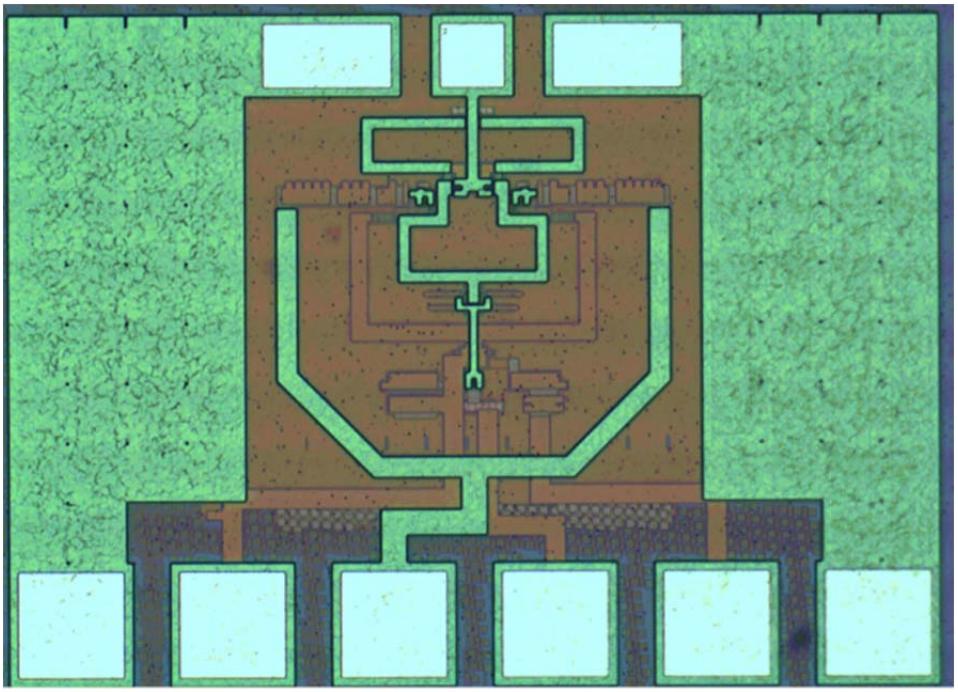


Fig. 2.11. Die photograph of the proposed inductive-tuning VCO where the chip area is 250×290 μm^2 excluding the pads.

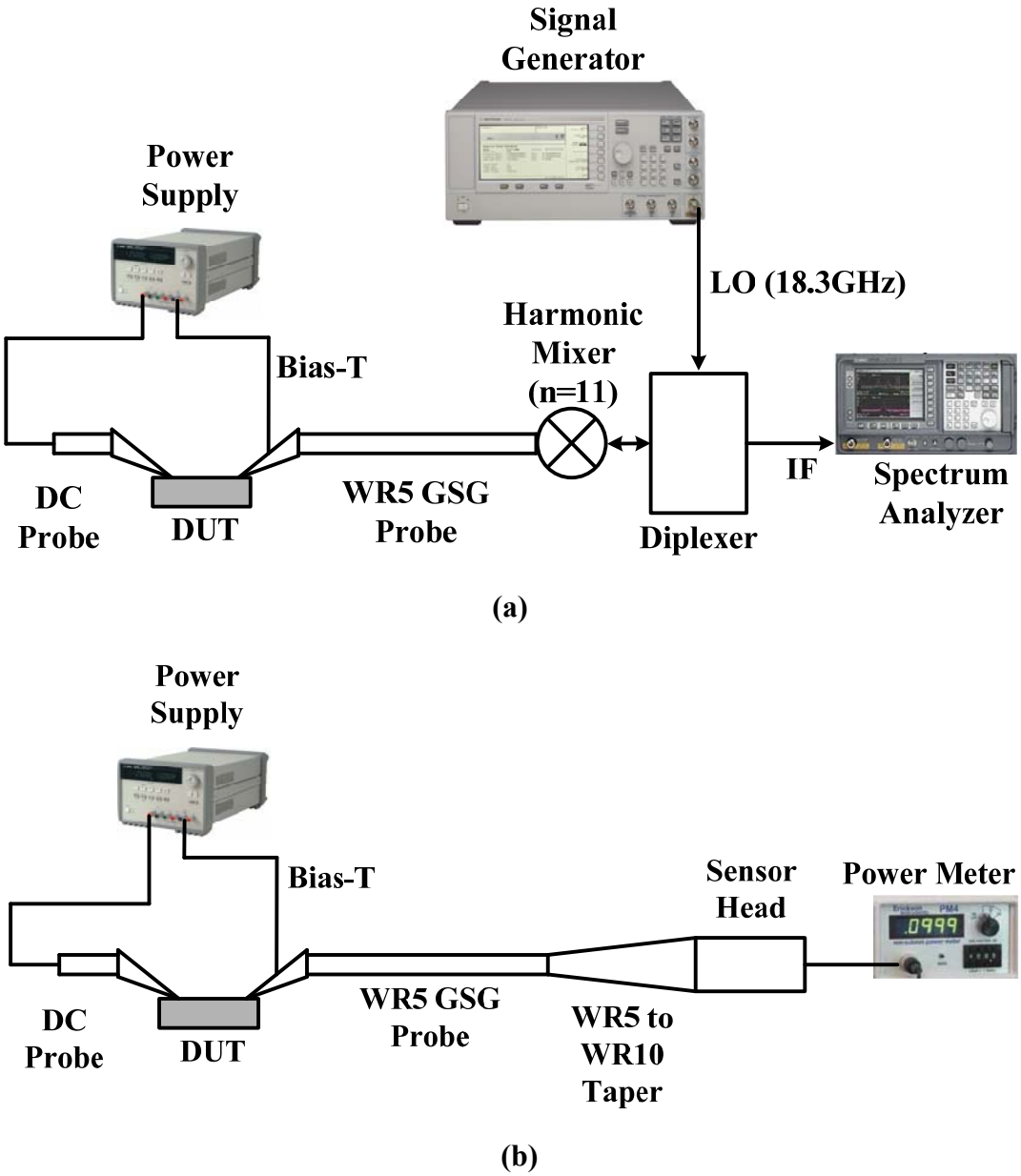


Fig. 2.12. (a) The frequency measurement setup of the 200 GHz VCO, and (b) The output-power measurement setup of the 200 GHz VCO.

The frequency and power measurement setups of the 200 GHz VCO are configured as shown in Fig. 2.12 (a) and (b). For the frequency measurement in Fig. 2.12 (a), the VCO output was connected to the WR5 GSG probe followed by a harmonic mixer, and down-converted the VCO's signal to a spectrum analyzer. Fig. 2.13 shows the VCO's 201.6 GHz signal after down-conversion where the LO signal

is 18.3 GHz and a harmonic number is 11. Due to the narrow IF bandwidth of the diplexer compared to the VCO's tuning range, the LO frequency is adjusted with respect to the VCO oscillation frequency in order to track the VCO output signal. As shown in Fig. 2.12 (b), the VCO output power was measured directly at the VCO output. The WR5 GSG probe is transformed to a WR10 waveguide interface via a taper, and then connected to a power meter. The measured output power was calibrated by the loss of the probe, the waveguide extension, and the taper (i.e., total loss of 3.25 dB).

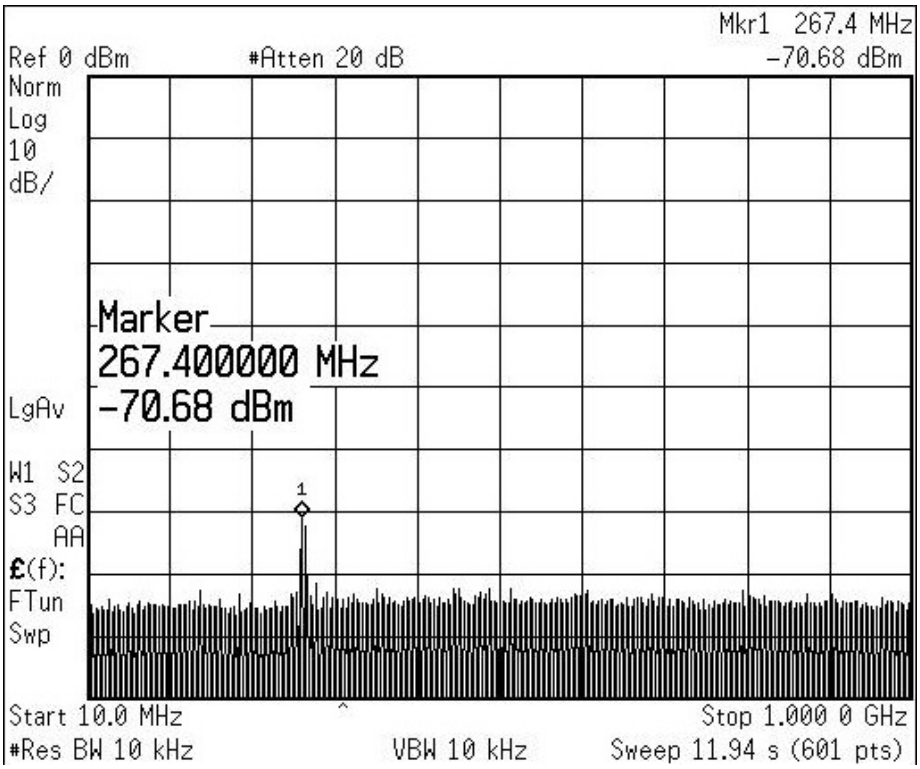


Fig. 2.13. The IF tone measured on the spectrum analyzer after the VCO's 201.6 GHz output signal was down-converted by a harmonic mixer (n=11) with the LO frequency of 18.3 GHz.

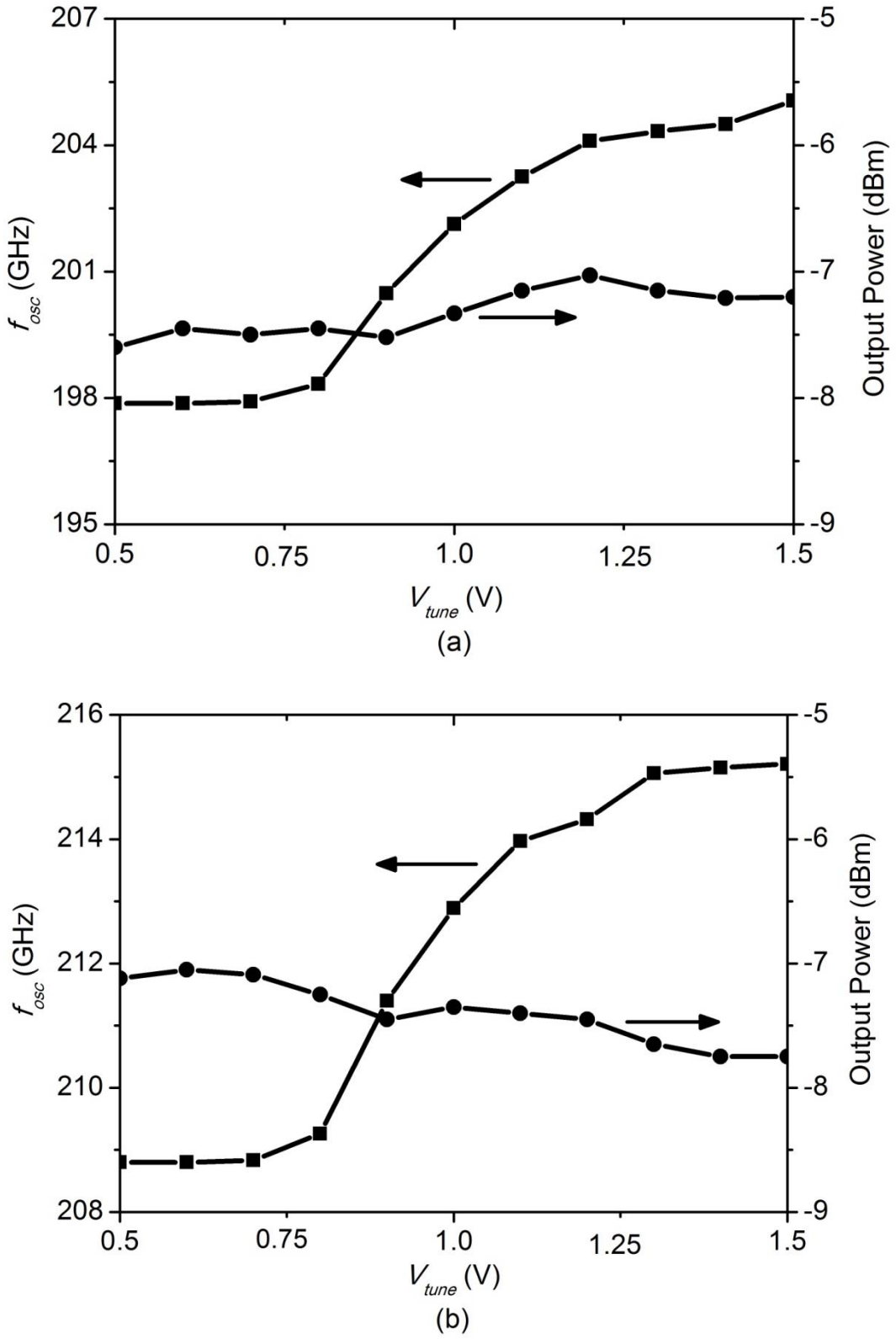


Fig. 2.14. The measured oscillation frequency and output power vs. V_{tune} of (a) the 200 GHz VCO, and (b) the 210 GHz VCO.

Fig. 2.14 (a) shows the measured oscillation frequency and output power of the 200 GHz VCO with respect to the tuning voltage, V_{tune}. By changing V_{tune} from 0.5 V to 1.5 V, the oscillation frequency is varied from 198 GHz to 205 GHz, resulting in a tuning range of 3.5 %. The measured output power is −7.2 dBm with less than 0.5 dB power-variation across the tuning range. Fig. 2.14 (b) shows the measurement results of the proposed 212 GHz VCO prototype, which was designed using the same topology. The tuning range is from 209 GHz to 215 GHz with −7.1 dBm output power. Both VCOs consume a DC power of 30 mW to 57 mW across the tuning range. As shown in Fig. 2.15, two additional VCOs were implemented at operation frequencies of 220 GHz and 227 GHz. The measured tuning range becomes 6 GHz, when the oscillation frequency extends to 229 GHz. Due to the bandwidth limitation of the WR5 waveguide (140–220 GHz), the output power of these two VCOs could not be measured accurately. Fig. 2.16 shows the measured phase noise profile of the 200 GHz VCO, where the phase noise is −87.2 dBc/Hz (−103.1 dBc/Hz) at 1 MHz (10 MHz) offset. Table 2-1 shows the VCO performance comparison with prior work. The proposed VCOs demonstrates the lowest figure-of-merit (FOM_T) of −165.6 dB among the other silicon-based VCOs.

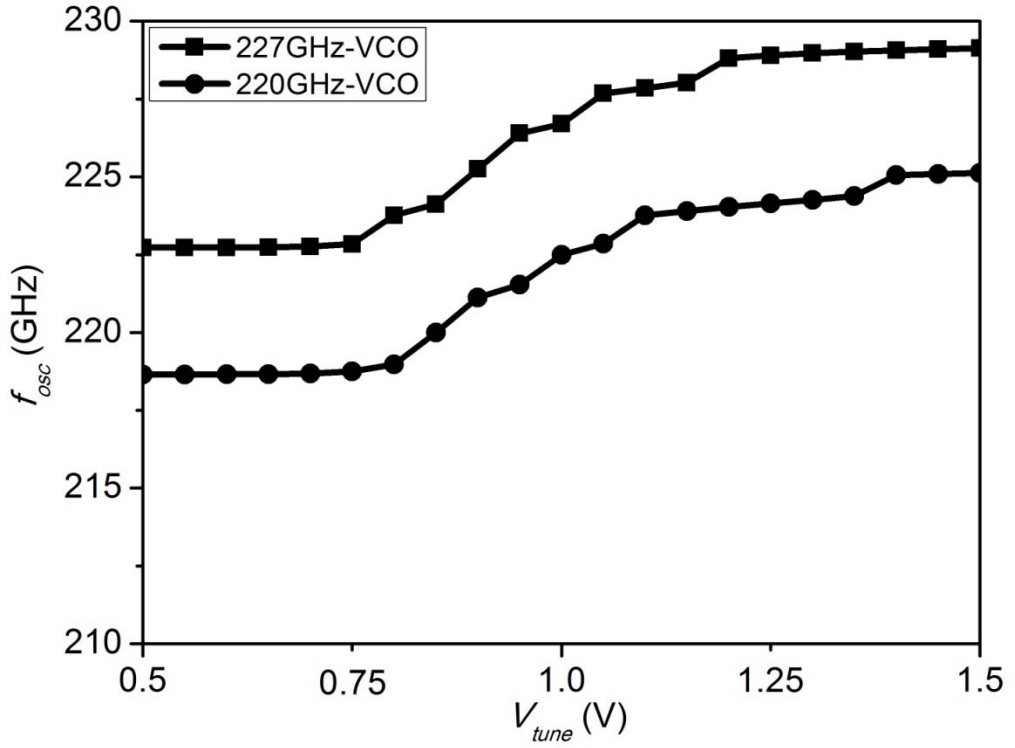


Fig. 2.15. The measured oscillation frequency of the 220 GHz and 227 GHz VCOs.

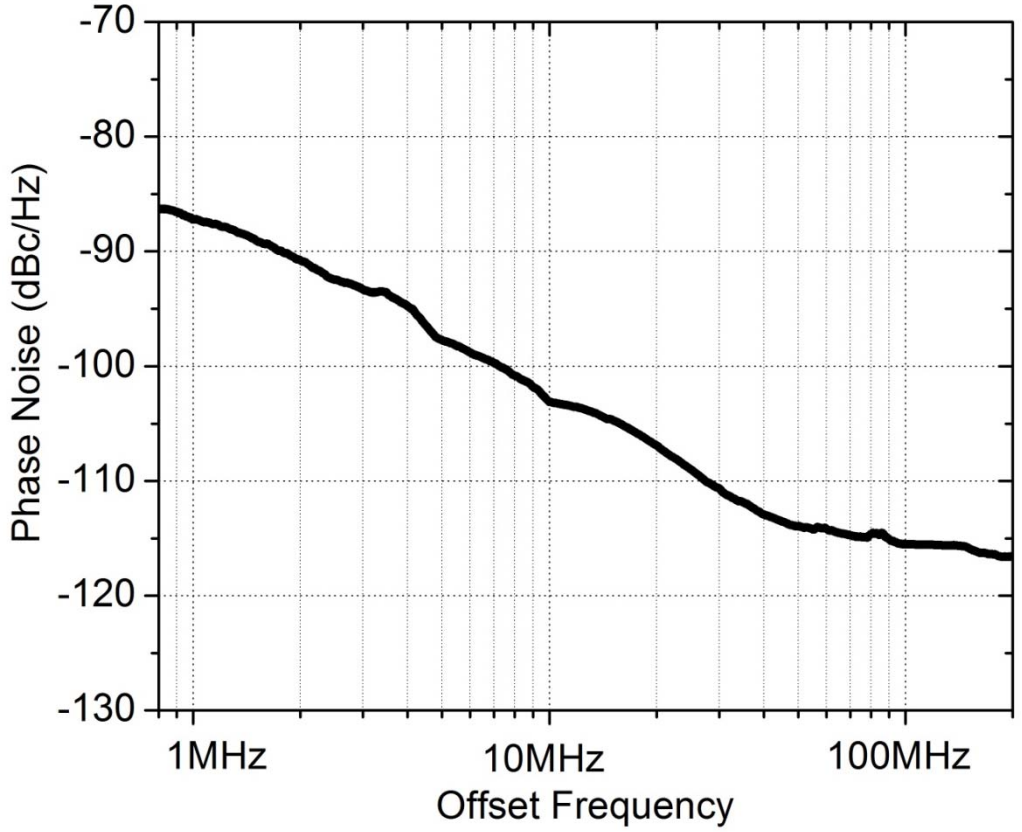


Fig. 2.16. The measured phase noise of the 200 GHz VCO.

TABLE 2-1

VCO Performance Comparison

	This Work	**This Work**	**[32]**	**[33]**	**[34]**	**[35]**	**[36]**	**[37]**
Frequency (GHz)	201.5	212	161.1	184.2	277.6	196.5	139	290
Tuning Range	3.5%	2.8%	4.7%	2%	1.5%	1.5%	0.09%	4.5%
Power(dBm)	−7.2	−7.1	−15	−11	−20	−19	−19	−1.2*
DC Power (mW)	30 (min.)	30 (min.)	46.5	95	132	29	9.6	325
Power Efficiency (%)	0.64	0.65	0.068	0.084	0.0076	0.087	0.13	0.23
PN @ 1MHz (dBc/Hz)	−87	−92	−86	NA	NA	−94	−79	−78
FOM*$_T$*	−162	−165.6	−151.9	NA	NA	−150	−112.1	−154
Technology	0.13μm SiGe	0.13μm SiGe	0.25μm SiGe	0.13μm SiGe	0.13μm SiGe	90nm CMOS	90nm CMOS	65nm CMOS

* Power combination of four cross-coupled oscillators

$$FOM_T = PN - 20\log\left(\frac{f_o}{\Delta f}\cdot\frac{FTR}{10}\right) + 10\log\left(\frac{P_{DISS}}{1mW}\right) - P_{out}$$

2.6 Conclusion

An inductive-tuning push-push VCO topology has been presented and analyzed for mm-wave and THz frequency bands. Four VCOs operating at different frequencies have been implemented to show the feasibility of the proposed approach. The maximum tuning range is 3.5% and highest oscillation frequency is 229 GHz. A power efficiency of 0.65% was achieved with an output power of −7.2 dBm. The proposed inductive-tuning topology increases the Q factor of the VCO's *LC* tank, which improves the output power and phase noise, leading to a high figure-of-merit among the other silicon-based low THz VCOs.

Chapter 3

A Fundamental 200GHz Double-Stacked VCO in 32nm SOI CMOS

As was discussed in the previous section, the transconductance g_m degrades significantly as the operation frequency increases towards half-f_{MAX} of the transistor. Moreover, varactor's loss becomes the dominant contributor to the Q factor degradation of the oscillator's *LC* tank. As a consequence, new circuit techniques need to be examined in the design of a fundamental VCO at 200GHz to overcome these limitations. Inductive tuning was demonstrated to be amenable to high frequencies compared to varactor tuning. Capacitive source degeneration at the buffer stage was proposed to increase equivalent negative resistance for mm-wave frequencies [38]. Also, capacitive source degeneration below the cross coupled pair can decrease undesired parasitic capacitance [39], [40]. In this chapter, a double-stacked cross-coupled pair is introduced to provide a stronger negative resistance and less parasitic capacitance compared with the conventional cross-coupled counterpart, making it attracting for high frequency VCO design.

3.1 A Fundamental Double-Stacked Cross-Coupled VCO

Shown in Fig. 3.1 (a) is a cross-coupled pair with an arbitrary source-degenerated impedance Z_s. By injecting a test voltage source V_t to the cross coupled pair the equivalent admittance Y_{in} is obtained as

$$Y_{in}=\frac{-g_m+sC_{gs}}{2(1+g_mZ_s+sC_{gs}Z_s)}=\frac{1}{-\frac{2}{g_m}-2Z_s-\frac{2sC_{gs}Z_s}{g_m}}+\frac{1}{\frac{2}{sC_{gs}}+\frac{g_mZ_s}{sC_{gs}}+2Z_s} \tag{3.1}$$

From (3.1), the equivalent circuit of Y_{in} can be seen as a parallel combination of Branch A and Branch B, as depicted in Fig. 3.1 (b). Assuming Z_s is a purely negative resistor (i.e., $Z_s = -R_s$), the absolute values of the Q factor in Branch A and in Branch B are expressed as

$$|Q_A|=\left|\frac{\mathrm{Im}[Z_A]}{\mathrm{Re}[Z_A]}\right|=\left|\frac{2\omega C_{gs}R_s/g_m}{-2/g_m+2R_s}\right|=\left|\frac{\omega C_{gs}R_s}{1-g_mR_s}\right| \tag{3.2}$$

$$|Q_B|=\left|\frac{\mathrm{Im}[Z_B]}{\mathrm{Re}[Z_B]}\right|=\left|\frac{-2/\omega C_{gs}+2g_mR_s/\omega C_{gs}}{-2R_s}\right|=\left|\frac{1-g_mR_s}{\omega C_{gs}R_s}\right| \tag{3.3}$$

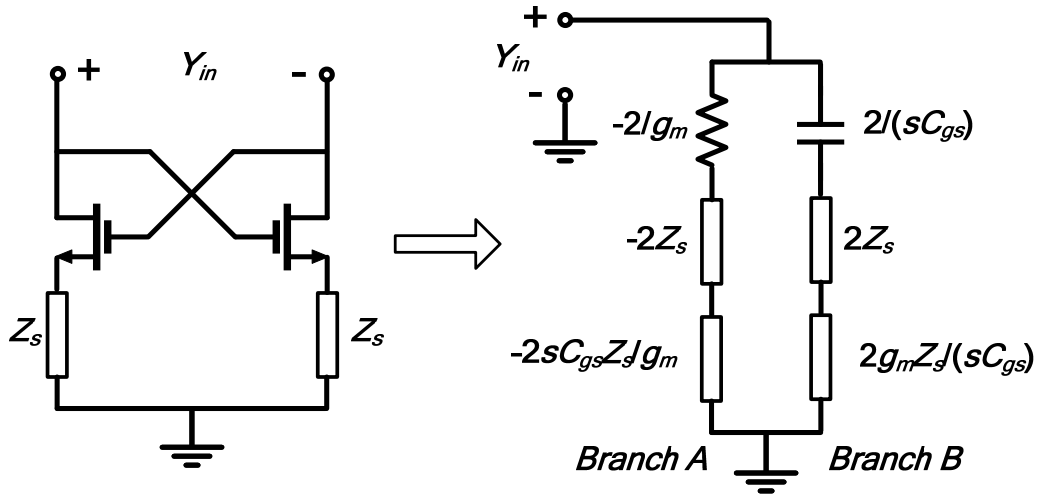
And the product of (3.2) and (3.3) gives

$$|Q_A\times Q_B|=1 \tag{3.4}$$

Under the condition that $R_s<\frac{1}{g_m}\cdot\frac{1}{1+\omega/\omega_T}$, it can be proved that $|Q_B|>1$ and $|Q_A|<1$. Therefore, $\mathrm{Re}[Y_{in}]$ is dominated by Branch A, i.e.,

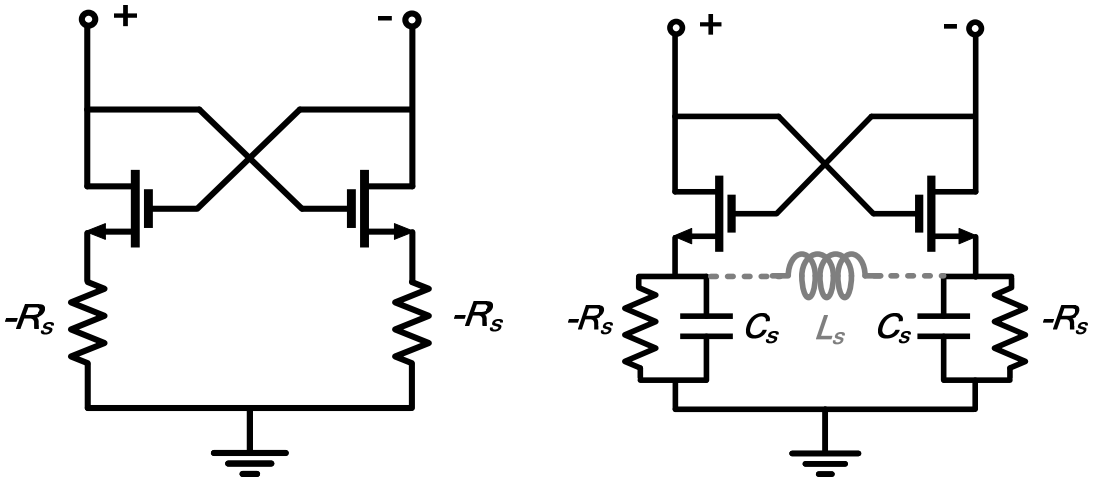
$$\begin{aligned}\mathrm{Re}[Y_{in}]&=\mathrm{Re}[Y_A]+\mathrm{Re}[Y_B]=\frac{1}{1+Q_A^2}\cdot\frac{1}{\mathrm{Re}[Z_A]}+\frac{1}{1+Q_B^2}\cdot\frac{1}{\mathrm{Re}[Z_B]}\\&\approx\frac{1}{\mathrm{Re}[Z_A]}=-\frac{g_m}{2(1-g_mR_s)}<-\frac{g_m}{2}\end{aligned} \tag{3.5}$$

From (3.5), the real part of Y_{in}, representing the negative resistance of the proposed cross-coupled, is enhanced compared to the conventional one.



(a) **(b)**

Fig. 3.1. (a) The cross-coupled pair with source-degenerated impedance, Z_s, and (b) Its equivalent circuit composed of branches.



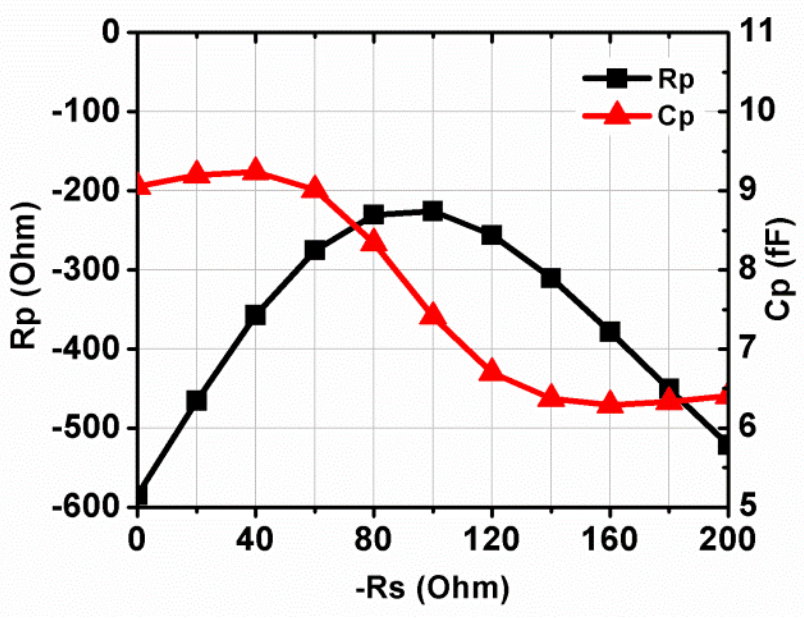
(a) **(b)**

Fig. 3.2. The cross-coupled pair with (a) a negative resistor source-degeneration, and (b) a parallel $-R_s$ and C_s source-degeneration.

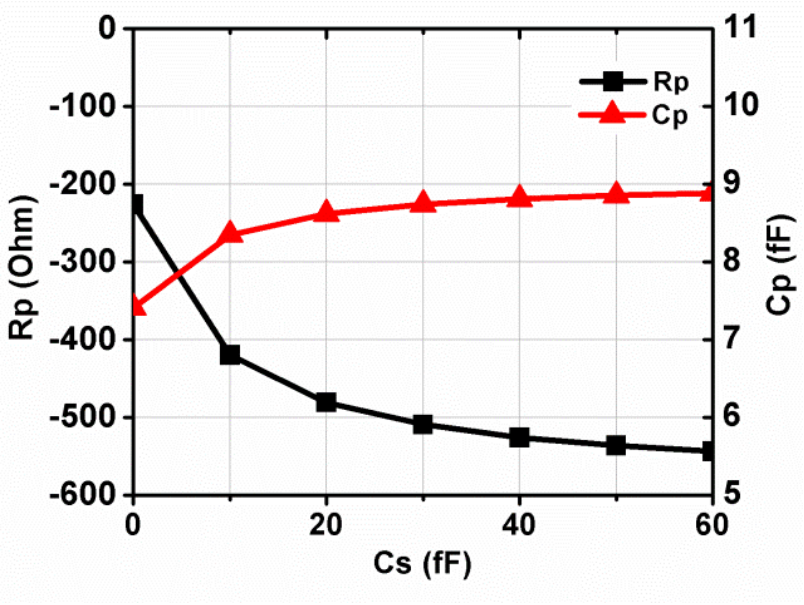
In order to verify the above first-order analysis, two cross-coupled pairs with different source-degenerated impedance as shown in Fig. 3.2 are simulated. Shown

in Fig. 3.3 (a) are the simulation results of the effective parallel resistance, R_p, defined as R_p=1/Re[Y_{in}] and the effective parallel capacitance, C_p, defined as C_p=Im[Y_{in}]/ω at 200 GHz for the circuit depicted in Fig. 3.2 (a) where the source impedance is a negative resistor. From the simulation, R_p reaches its maximum value when R_s is around 90 Ω. As a result, by proper choosing the negative resistor at the source of the cross-coupled pair, R_p is improved by three times, leading to higher loop gain. Moreover, the reduction of the effective capacitance C_p helps widen the tuning range and makes it feasible to design a VCO at high frequencies.

One effective way of realizing the negative resistor ($-R_s$) is by utilizing another cross-coupled pair. However, the effect of the additional parasitic capacitance in the source terminal, as shown in Fig. 3.2 (b), needs to be investigated. Fig. 3.3 (b) shows the effective parallel resistance R_p and parallel capacitance C_p at 200GHz for circuit depicted in Fig. 3.2 (b). In Fig. 3.3 (b), both R_p and C_p decrease as the source parasitic capacitance C_s increases, degrading the performance. In order to eliminate the degradation caused by C_s, an inductor L_s is added between the source terminals of the cross coupled pair to resonant out the undesired parasitic capacitance, as shown in Fig. 3.2 (b).



(a)



(b)

Fig. 3.3. The simulated effective parallel resistor R_p and effective parallel capacitor C_p for the cross-coupled pair with different source impedance; (a) sweep R_s, C_s=0, (b) sweep C_s, $-R_s$=–90Ω.

Fig. 3.4 shows the proposed fundamental double-stacked cross-coupled VCO with OOK modulator. The overall negative resistance of this oscillator is enhanced due to the additional source-degenerated negative resistor provided by M_1–M_2. This

negative resistance compensates for the excessive varactor's loss at high frequencies, thereby improving overall loop gain. As mentioned above, the 30 pH inductor L_S in Fig. 3.4 mitigates the detrimental effect of parasitic capacitance of the bottom cross-coupled pair M_1–M_2. The L_s also provides the DC path between the upper and lower cross-coupled pairs. Assume the VCO is oscillating with full-swing, i.e., M4 is off when M3 is on, and vice versa. If the gate of M3 is "high" and M3 turns on (M4 turns off), the voltage at the gate of M2 follows that of M3 through a common-drain topology, and M2 turns on. The DC current will flow from M3 to M2 through the inductor L_s. The inter-stage matching network between the VCO buffer and the On-off keying (OOK) modulator is realized by transformers, thereby leading to compact layout. The OOK modulator is implemented by using a cascode topology $M_7(M_8)$–$M_9(M_{10})$, where the modulation signal is applied to the gate of transistor $M_9(M_{10})$. The output of the OOK modulator is impedance-matched to 50 Ω by using transformers.

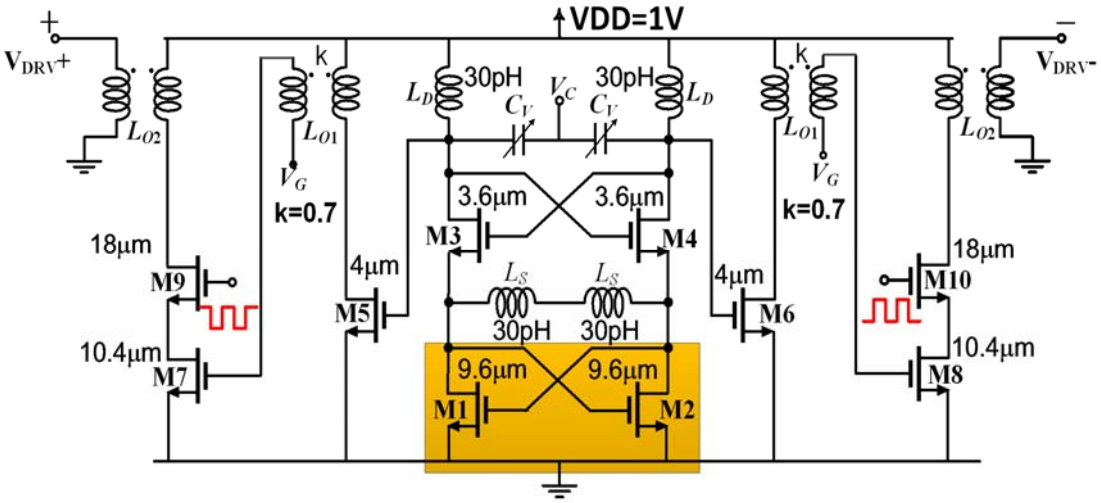
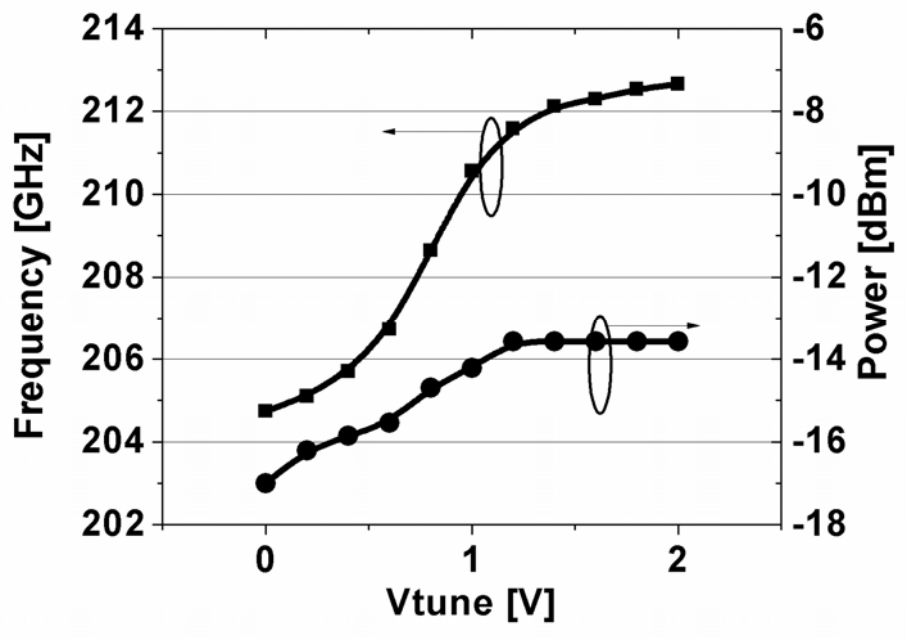


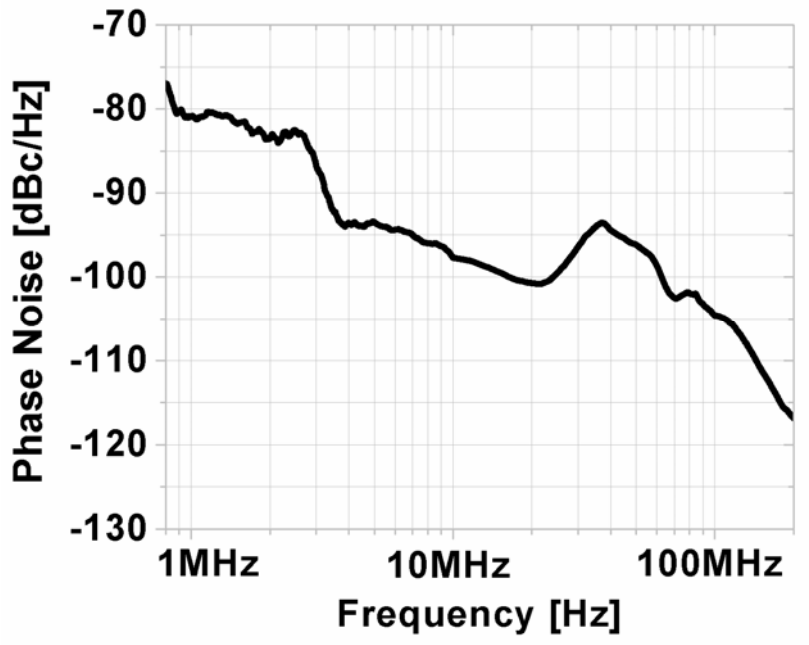
Fig. 3.4. The proposed fundamental 210GHz VCO with OOK modulator.

3.2 Measurement

The proposed VCO with OOK modulator, implemented in IBM 32nm SOI CMOS, occupies a chip area of 100×400 μm^2. Similar to the measurement setup as depicted in Chapter 2, the VCO was characterized using a G-band (140 GHz–220 GHz) RF probe, a power meter and a sub-harmonic mixer. Shown in Fig. 3.5 (a) is the measured VCO oscillation frequency and output power. The VCO exhibits a operation frequency from 204.7 GHz to 212.7 GHz (i.e., a tuning range of 8 GHz) and the output power of −13.5 dBm. Fig. 3.5 (b) shows the measured phase noise profile at 209 GHz where the phase noise is −81 dBc/Hz at 1 MHz offset. The overall VCO current consumption is 42 mA from 1V supply.



(a)



(b)

Fig. 3.5. (a) The measured VCO oscillation frequency and output power across the tuning range, and (b) The measured phase noise profile when the VCO is oscillating at 209 GHz.

3.3 Conclusion

A double-stacked cross-coupled VCO operating at its fundamental 200 GHz is introduced. The proposed cross-coupled pair with a negative source-degenerated resistor provides a stronger negative resistance with less parasitic capacitance compared with the conventional cross-coupled pair. All these benefits make it a good candidate in design a high frequency VCO, because the increasing loss of varactors can be compensated. The VCO with a OOK modulator was implemented in IBM 32nm SOI CMOS where the f_T/f_{MAX} is 250 GHz / 320 GHz. The proposed VCO achieves tuning range of 8 GHz (204.7~214.7 GHz), phase noise of −81 dBc/Hz at 1 MHz offset with a DC power consumption of 42 mW. Of course designing a push-push VCO (i.e., using the 2^{nd} harmonics) operating at the fundamental 100 GHz could be less challenging. However, when a differential signal is necessary, a fundamental VCO achieves a better performance compared with a push-push VCO followed by a balun.

Chapter 4

A Silicon-Based THz Frequency Synthesizer with Wide Locking Range

A 300 GHz frequency synthesizer incorporating a triple-push VCO with Colpitts-based active varactor (CAV) and a divider with three-phase injection is introduced. The CAV provides frequency tunability, enhances harmonic power, and buffers/injects the VCO fundamental signal from/to the divider. The locking range of the divider is vastly improved due to the fact that the three-phase injection introduces larger allowable phase change and injection power into the divider loop. Implemented in 90 nm SiGe BiCMOS, the synthesizer achieves a phase-noise of −77.8 dBc/Hz (−82.5 dBc/Hz) at 100 kHz (1 MHz) offset with a crystal reference, and an overall locking range of 280.32~303.36 GHz (7.9 %).

4.1. Architecture of The THz Frequency Synthesizer

In a THz frequency synthesizer, the VCO and the first stage of the divider chain following the VCO are two of the most important building blocks, which dominate the PLL performance including locking range, phase-noise, and output power. As the

operation frequency approaches the device f_{MAX}, transistors barely provide sufficient power gain or negative resistance even with a proper feedback loop. The transistor's gain limitations along with sever loss of passive components such as capacitors, varactors and inductors make it difficult to design frequency dividers or fundamental oscillators at THz frequencies. A PLL operating at lower frequency followed by a frequency tripler (e.g., harmonic-based or injection locked tripler) alleviates some of the challenges, as was extensively discussed in [29]. While the harmonic-based tripler (HBT) is amenable to high frequencies close to f_{MAX}, it consumes additional DC power and degrades the overall PLL phase-noise. The total phase-noise, S_{Total} ($\Delta\omega$), of a lower-frequency PLL followed by the HBT is expressed as [29]:

$$S_{Total}(\Delta\omega) = 3^2 S_{Fund}(\Delta\omega) + S_{HT}(\Delta\omega) + S_{MN}(\Delta\omega) \tag{4.1}$$

where $S_{HT}(\Delta\omega)$ is the phase-noise of the low-frequency PLL, $S_{HT}(\Delta\omega)$ and $S_{MN}(\Delta\omega)$ represent the phase-noise contributions from the harmonic transistors (the transistors generating 3rd harmonic signals) and the output matching network of the HBT, respectively. The tripler's noise contributions, $S_{HT}(\Delta\omega)$ and $S_{MN}(\Delta\omega)$, cause a deviation from the ideal value, that is, the HBT's input phase-noise $S_{Fund}(\Delta\omega)|_{\mathrm{dB}}$ plus $20log_{10}(3)$.

Fig. 4.1 shows the architecture of the proposed 300 GHz frequency synthesizer composed of a triple-push VCO, a three-phase injection locked divider (÷4)

followed by a ÷256 divider chain, a phase frequency detector / charge pump (PFD / CP) with a tunable current (I_{CP}: 150~300 μA), and a 2-bit programmable 3rd-order loop filter [41]. The input reference is fed by a 96 MHz crystal oscillator. The VCO's 3rd harmonic signal will be the synthesizer's output ($3f_o$=300 GHz) and its three-phase fundamental signals (f_o) are fed to the divider. The use of the triple-push VCO results in the injection of lower frequency signal f_o to the divider chain, thereby relaxing the divider design requirement and lowering its DC power consumption. Although one can clearly implement a higher harmonic VCO and further decrease the fundamental frequency, but it is noteworthy that the VCO's harmonic output power will be limited by the transistor nonlinearity. Since no additional frequency multiplier follows the synthesizer in this design, the noise contribution of the harmonic generation transistors, S_{HT} (Δω), in (1) will no longer exist, resulting in lower phase-noise.

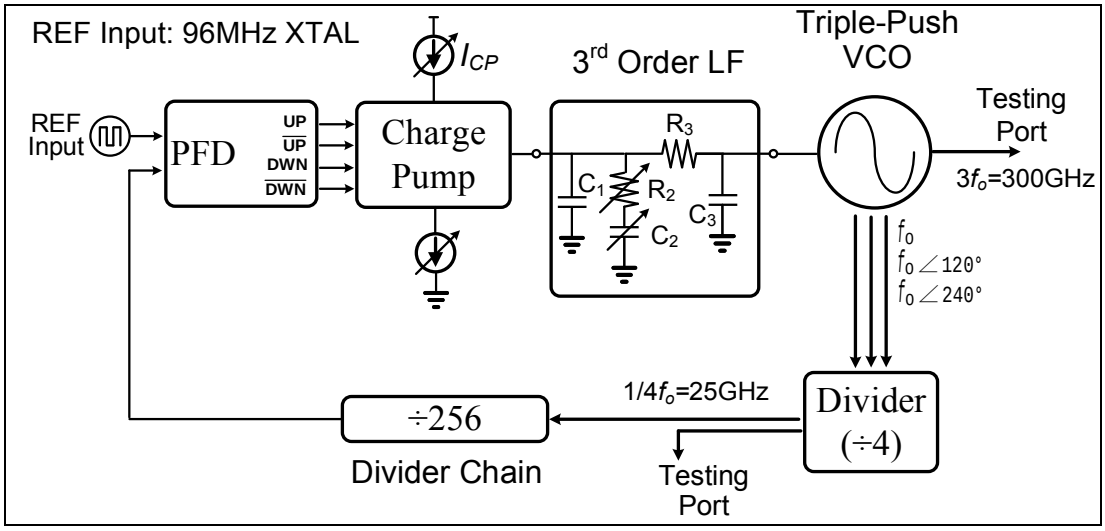


Fig. 4.1. The proposed architecture of the 300 GHz frequency synthesizer.

By using the triple-push VCO, the first-stage divider within the synthesizer operates at around 100 GHz. An injection-locked frequency divider (ILFD) is commonly used at mm-wave frequencies [30]. Nonetheless, an ILFD exhibits small locking range, which limits the frequency range of the synthesizer. One of the solutions to improve the locking range is to use multi-phase injection [42]. The availability of three-phase fundamental frequency signals in the triple-push VCO allows us to consider an ILFD with three-phase injection. The proposed three-phase injection locked divider exhibits a wide locking range, which encompasses the VCO's tuning range. The synthesizer locking range, therefore, follows the VCO's frequency tuning range. The ÷256 divider chain uses ECL- and CML-type topologies for their wide bandwidth characteristic. The PFD is implemented based on a conventional structure similar to the one presented in [43]. By sending an "up" and a "down" current pulses to the CP during each reference cycle, the PFD dead zone is eliminated and the loop gain for small phase error is improved.

An on-chip third-order loop filter is utilized, in which C_2 produces the first pole and together with R_2 is used to generate a zero for the loop stability. C_1 is used to smoothen the control voltage ripples. R_3 and C_3 are used to further suppress reference spurs and high frequency noise. The loop filter's component values are C_1=800 fF, R_2=13 kΩ, C_2=22 pF, R_3=21 kΩ, and C_3=300 fF.

4.2. Triple-Push VCO with CAV

An alternative way of producing a high frequency signal, especially when it is close to the transistor's f_{MAX}, is to make use of the oscillator's harmonics. To retain the output power, minimizing the resonator's loss at both the harmonic and fundamental frequencies is essential. For example, if the resonator's loss is minimized only at the oscillator's fundamental frequency and increased at its harmonics, the fundamental signal swing will be improved and the transistors will thus generate higher intrinsic harmonic power. This harmonic power, once passing through the resonator, will be degraded significantly. In addition, the frequency-tuning mechanism, introduced at the fundamental frequency, exhibits ever-increasing loss at the harmonic frequency, thereby further degrading the harmonic power. Besides, the relative input-output phase difference ϕ and gain A of single transistor, defined in Fig. 4.2, affects the output power that this transistor can generate [44]. If a transistor operates in its optimum condition, expressed by Eq. (4.7), it generates the maximum output power, as will be described later. In our VCO design, all these considerations are taken into account in order to improve the output power, and subsequently, a better phase-noise if the VCO operates in the current-limited region [45], which is usually the case for THz VCOs.

Starting from the transistor's input-output phase and gain conditions, shown in

Fig. 4.2 is a two-port Y-parameter representation of the transistor. The net power that flows into the transistor can be expressed as [46]

$$P_N = V_1^* I_1 + V_2^* I_2 \tag{4.2}$$

where * denotes the complex conjugate. Representing I_1 and I_2 with respect to V_1 and V_2, the real power Re[$-P_N$] that flows out of the transistor is expressed as

$$\mathrm{Re}[-P_N] = |V_1|^2 \left[- A\left|Y_{12} + Y_{21}^*\right| \cos(\angle(Y_{12} + Y_{21}^*) + \phi_{BC}) \right] - |V_1|^2 (G_{11} + A^2 G_{22}) \tag{4.3}$$

where

$$A = \frac{|V_2|}{|V_1|}, \qquad \phi_{BC} = \angle \frac{|V_2|}{|V_1|} \tag{4.4}$$

The real power is comprised of the power dissipated (P_R) and the power generated (P_G) inside the transistor, defined as:

$$P_R = |V_1|^2 \left[(G_{11} + A^2 G_{22}) \right] \tag{4.5}$$

$$P_G = -A|V_1|^2 \left|Y_{12} + Y_{21}^*\right| \cos(\angle(Y_{12} + Y_{21}^*) + \phi_{BC}) \tag{4.6}$$

In Eq. (4.6), P_G reaches its maximum absolute value if

$$\phi_{BC} = \phi_{BC,opt} = (2k+1) - \angle(Y_{12} + Y_{21}^*) \tag{4.7}$$

where k is an integer. Under a given bias condition, there exists an optimum phase difference between the base and the collector, $\phi_{BC,opt}$, that a transistor generates the maximum power. Fig. 4.3 shows the simulated $\phi_{BC,opt}$ versus frequency for a transistor with aspect ratio of L_E/L_B=4μm / 0.09μm and biased at its maximum f_{MAX}. The optimum phase condition varies from 140°~110° across the frequency range from 80~160 GHz. In the proposed VCO design, the transistors are designed to

satisfy this phase condition so as to achieve substantially better VCO performance.

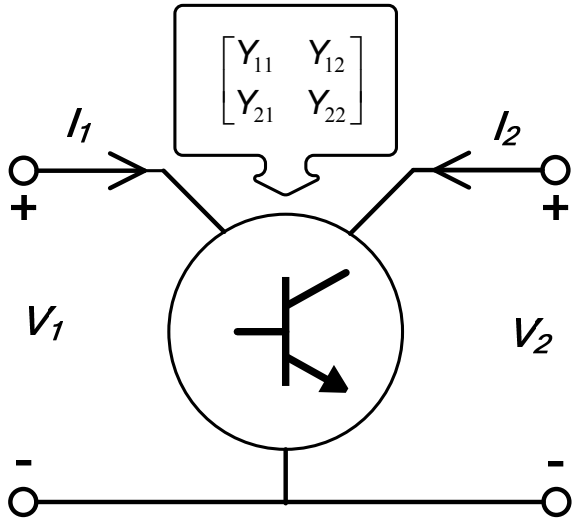


Fig. 4.2. A two-port Y-parameter representation of a single transistor.

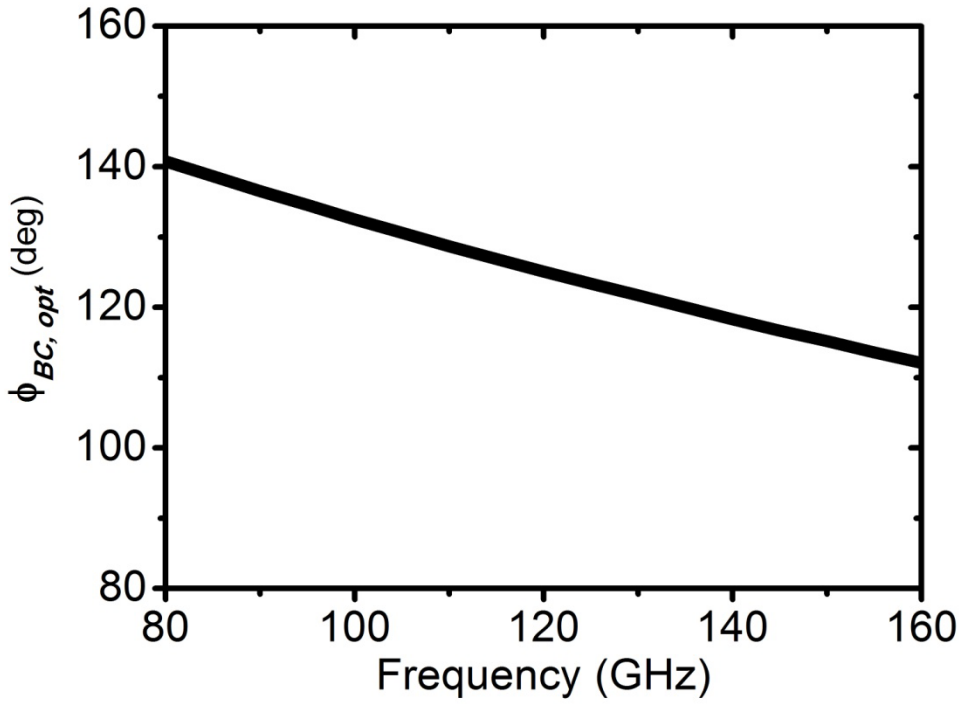
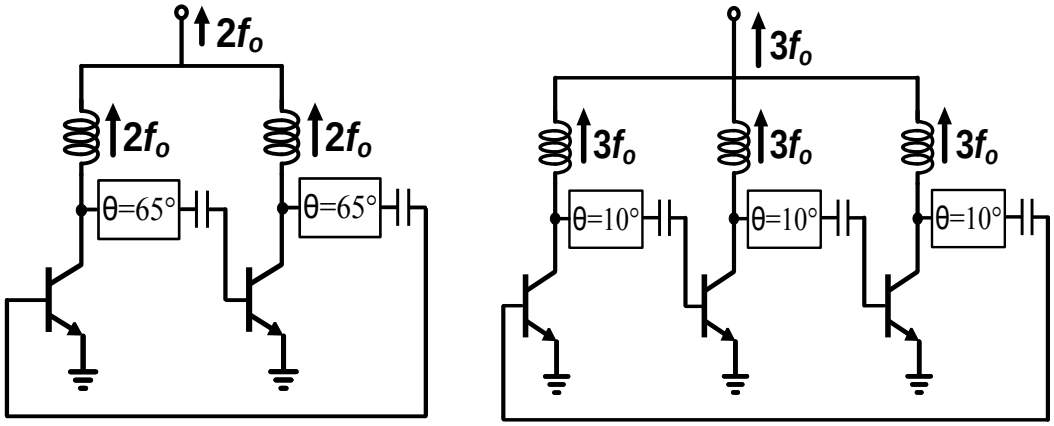


Fig. 4.3. The simulated $\phi_{BC,opt}$ versus frequency for a transistor with aspect ratio of L_E/L_B=4μm/0.09μm and biased at its maximum f_{MAX}.

Based on the net power analysis of the single transistor, a systematic approach of designing a 300 GHz oscillator is now described. A harmonic ring oscillator

offers the ability to achieve $\phi_{BC,opt}$ by adding extra phase shift between stages. Fig. 4.4 (a) shows an example of a two-stage ring (i.e., cross-coupled) oscillator, where the second harmonic signal $2f_o$ is retrieved from common output terminal. Referring to Fig. 4.3, $\phi_{BC,opt}$ at fundamental oscillation frequency of 150 GHz is 115°. Because of the 180° constant phase difference between two stages, an extra phase shift of 65°, realized using a t-line, is required to achieve $\phi_{BC} = \phi_{BC,opt}$. A larger phase shift requires a longer t-line with inevitably larger in-series loss in the signal path. This loss degrades the fundamental voltage swing inside the ring which, in turn, degrades the second harmonic power. Consequently, ring oscillators requiring larger extra phase shifts to achieve $\phi_{BC,opt}$ will produce smaller harmonic power. Shown in Fig. 4.4 (b) is another example using three-stage ring. By virtue of its design, the three-stage ring oscillator requires a small phase shift of 10° to satisfy the optimum phase condition. In addition, compared to the two-stage counterpart, more branches participate in the harmonic power generation, resulting in a higher output power. The three-stage ring oscillator is thus chosen as the VCO core.



(a) **(b)**

Fig. 4.4. (a) A two-stage ring oscillator with a phase-shift of 65° between stages. (b) A three-stage ring oscillator with phase-shift of 10°.

The conventional approach for frequency tuning in a three-stage ring VCO, shown in Fig. 4.5, employs a varactor in parallel with a buffer at the base of each ring transistor. The input parasitic capacitor of the buffer, however, decreases the oscillation frequency. Decreasing the loading inductor, L_C, boosts up the oscillation frequency at the expense of lowering the gain of each stage. Both the loss of the buffer and the varactor degrades the base voltage swing of the ring transistor, especially the severe varactor loss at high frequency becomes a bottleneck. Therefore, a new frequency tuning circuitry called Colpitts-based active varactor (CAV) is introduced. The schematic of the VCO with CAV is shown in Fig. 4.6. The VCO's f_o is traveling along the VCO three-stage ring with 120° phase difference between stages. Its 3rd harmonic signals generated from the transistors nonlinearity will be in-phase and collected at the common-mode output $3f_o$. The t-line L_{VB} is used

to introduce 10° phase shift for transistor's optimum phase condition. In a conventional Colpitts oscillator, the Colpitts cell is an essential part of the oscillator that enables sustainable oscillation by providing loss compensation mechanism for the resonator. On the other hand, the CAV in this design merely realizes extremely low-loss tunable capacitance and isolates the varactor loss from the VCO ring. In addition, it buffers the VCO's f_o to the divider, and thus, avoids loading the VCO ring. In the CAV schematic, node A_i ($1 \le i \le 3$) is connected to each stage of the VCO ring and output node B_i ($1 \le i \le 3$) is connected to the divider. Inside the CAV, the cascode stage T_1-T_2 with its T-junction matching network buffers the VCO's f_o and feeds the signal to the divider. The bypass capacitor C_{b2}, the large resistor R_B, and bias voltage V_T are used to level-shift V_{CTRL} within the voltage range required by the charge pump. The t-line L_T models the short interconnect between the CAV and the VCO ring in the actual layout. The three CAVs are placed in close proximity of the VCO ring so that the L_T effect on the oscillation frequency and tuning range becomes negligible.

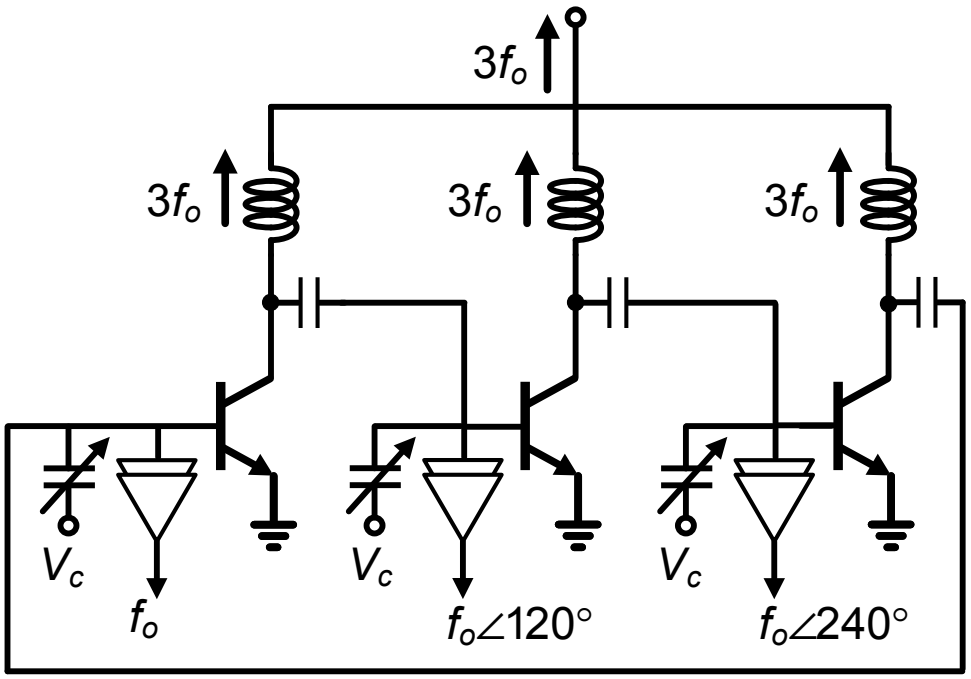


Fig. 4.5. A conventional three-stage ring VCO employing a varactor in parallel with a buffer at the base terminals of the transistors.

Shown in Fig. 4.7 are the simulation results of the CAV including the tunable capacitor C_{tune} and the parallel conductance Re[Y_P] seen form node A_i ($1 \le i \le 3$). C_{tune} monotonically decreases from 42~26 fF with V_{CTRL} varying from 0~2 V for frequency tuning. The negative conductance Re[Y_P] across the tuning range compensates for the large varactor loss and also helps the VCO start-up condition. Shown in Figs. 4.8 (a) and (b) are the simulated fundamental voltage swings of the conventional and the CAV tuning ring VCOs, respectively, with the same tuning range and oscillation frequency. The proposed VCO achieves more than three times higher base voltage swing than the conventional counterpart.

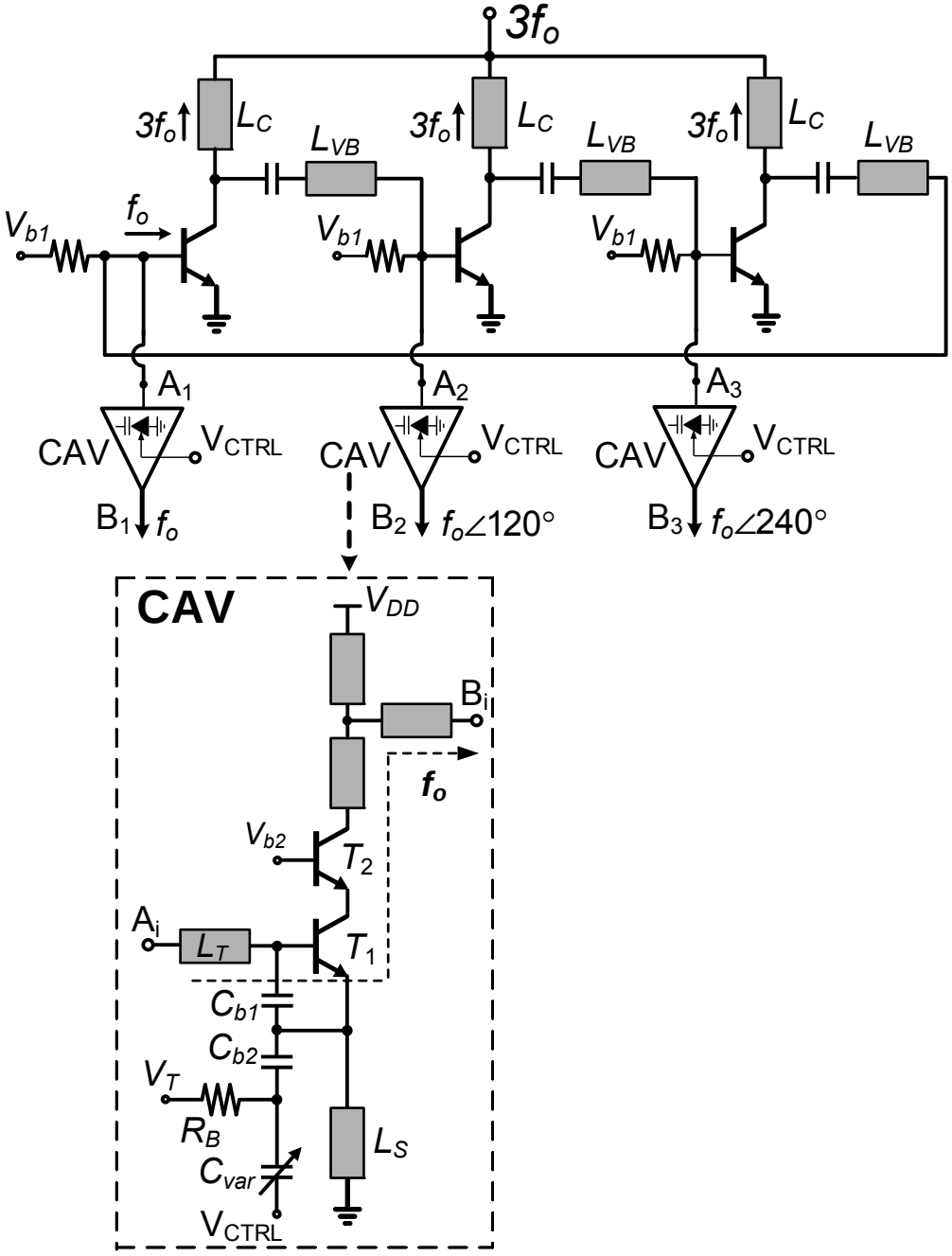


Fig. 4.6. The schematic of the proposed triple-push VCO with CAV (CAV: Colpitts-based active varactor).

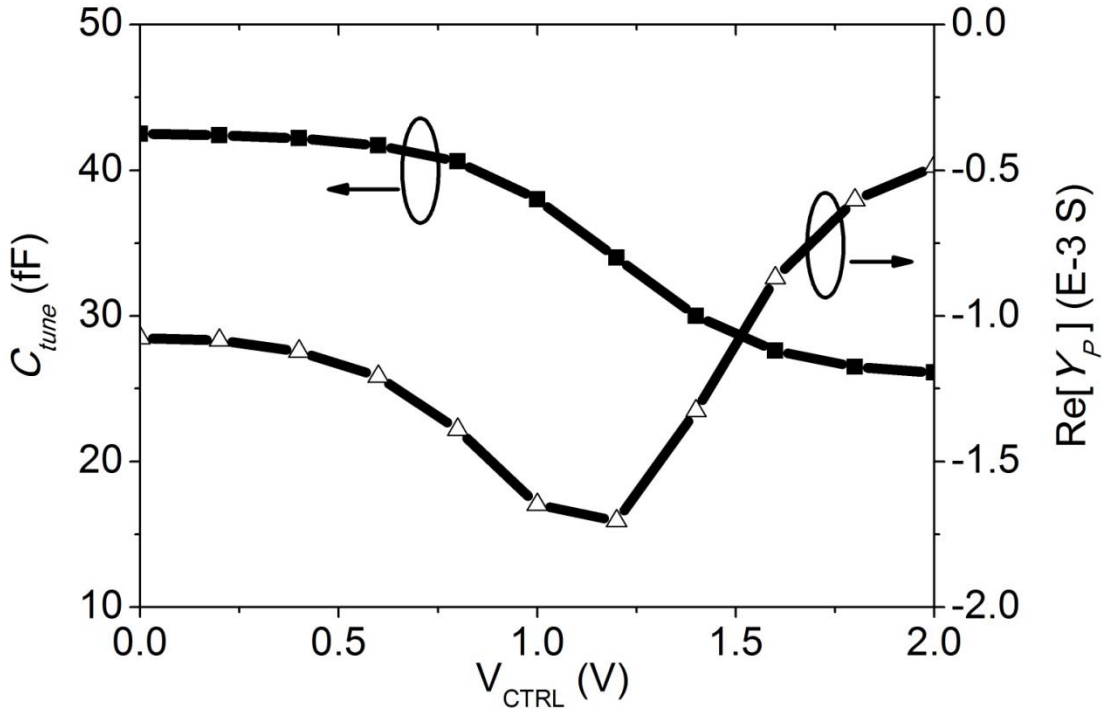
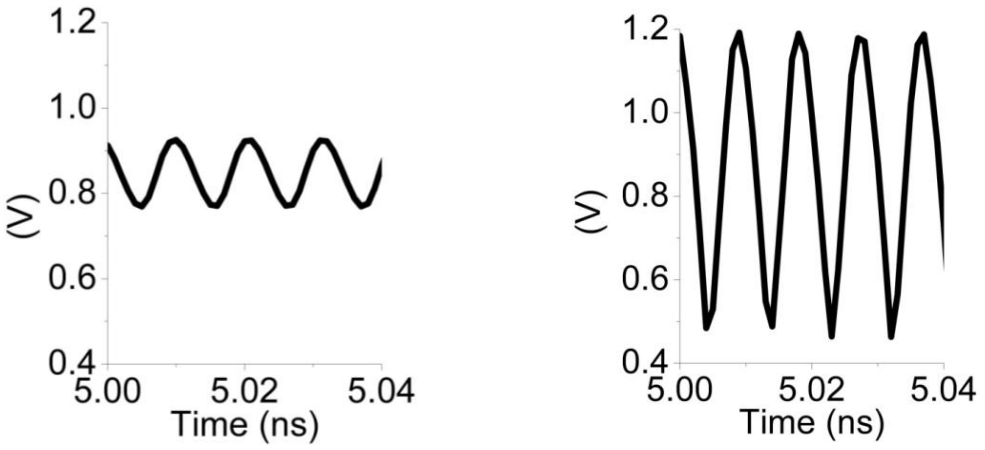


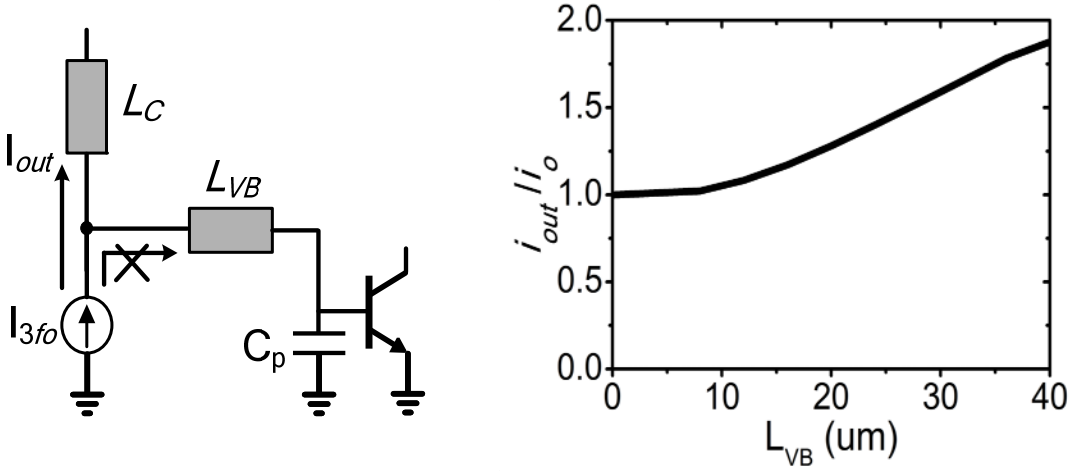
Fig. 4.7. The simulated tunable capacitor C_{tune} and the parallel conductance Re[Y_P] of the CAV (seen from node A_i of Fig. 4.6).

In addition to providing 10° phase shift, the L_{VB} also enhances the $3f_o$ power collection by blocking the $3f_o$ from flowing to the next stage as shown in Fig. 4.9 (a). The current source I_{3fo} represents the 3rd harmonic current generated from a transistor and C_p is the input parasitic capacitor of the next stage. At the 3rd harmonic frequency, L_{VB} partially resonates with C_P, resulting in high impedance. Therefore, the large portion of the 3rd harmonic current will flow into the load, I_{out}. The plot shown in Fig. 4.9 (b) is the current I_{out} normalized to I_o (the current flowing to the load without L_{VB}). As L_{VB} increases to 40 μm, I_{out} is improved by as much as 1.9 times.



(a) **(b)**

Fig. 4.8. The simulated fundamental voltage swings for (a) a three-stage ring VCO with a conventional varactor tuning as shown in Fig. 4.5, and (b) a three-stage ring VCO with CAV tuning.



(a) **(b)**

Fig. 4.9. (a) The 3rd harmonic power enhancement by using L_{VB} to partially resonate with C_p. (b) The simulation of the normalized 3rd harmonic current flowing to the load versus the length of the t-line L_{VB}.

4.3. Three-Phase Injection Locked Divider (÷4)

Shown in Fig. 4.10 is the conceptual loop of the proposed injection locked divider. Each stage is composed of an amplifier, a mixer, and a low-pass filter (LPF). The free-running frequency of the loop is designed close to $1/4f_o$, and each stage

contributes 120° phase-difference between its input and output. The three 3rd-harmonic signals ($3/4f_o$) generated from the amplifiers are all naturally in-phase. The input three-phase signals coming from the VCO's three-phase output are mixed with $3/4f_o$ signals. The mixers' outputs ($1/4f_0$, $1/4f_0\angle 120°$, $1/4f_0\angle 240°$) are injected back to the loop and are added constructively with the loop's signal. In the steady-state, the loop is locked to the injected signals and divide-by-4 operation is performed. The same conceptual loop can readily perform divide-by-5 by simply swapping the last two input signals, as depicted in Fig. 4.11. Assuming the free-running frequency of the loop is close to $1/5f_o$, the three-phase input signals are mixed with the loop's 4th harmonic ($4/5f_o$). The loop will be locked to the mixer's output signals ($1/5f_o$, $1/5f_0\angle 120°$, $1/5f_0\angle 240°$).

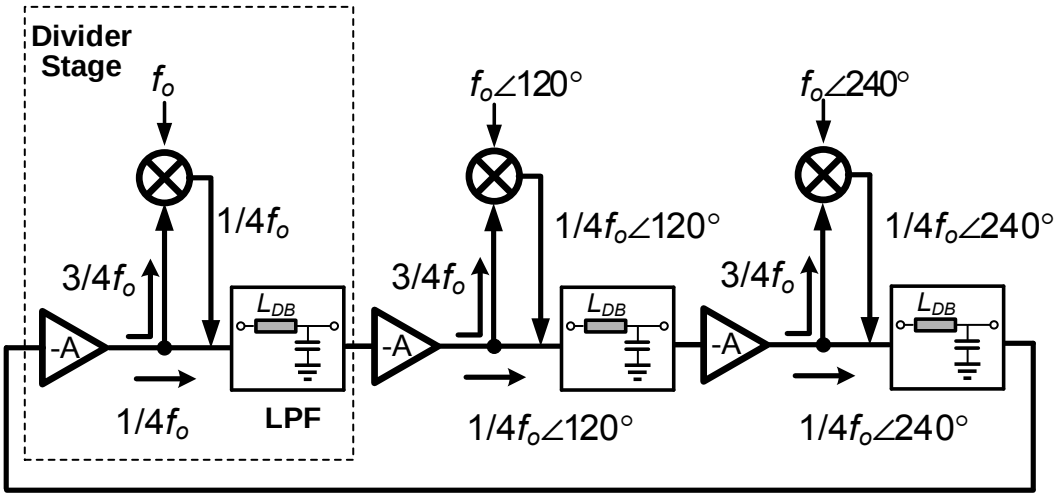


Fig. 4.10. The conceptual loop of the proposed three-phase injection locked divider (divide-by-4).

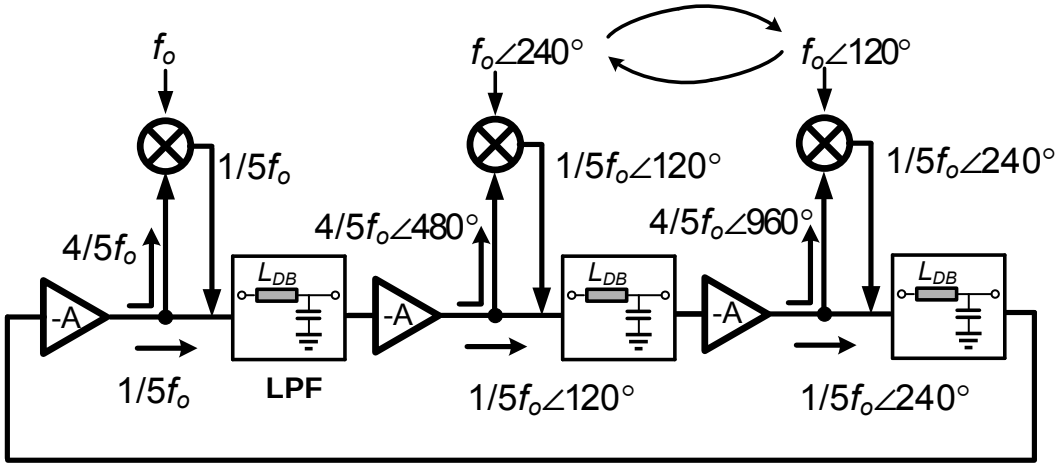


Fig. 4.11. By swapping the last input signals, the same conceptual loop performs divide-by-5.

Compared with the single injection, the multi-phase injection achieves wider locking range and requires lower input power. For a general case of *N*-stage divider with *M*-phase injection, in the phasor domain, each injection current, I_{in}, introduces a phase change ϕ to the loop signal (I_{osc}), and each LPF needs to compensate for a phase change θ in order to satisfy Barkhausen criteria. The phase change θ of each LPF is expressed as

$$\theta = \frac{M}{N}\phi \tag{4.9}$$

If I_{in} is much smaller than I_{osc}, the normalized single-side locking range is then expressed as [47]:

$$\frac{\Delta f}{f_a} \le \frac{M}{N} \cdot \frac{1+\tan^2\frac{\pi}{N}}{\tan\frac{\pi}{N}} \cdot \left|\frac{I_{in}}{I_{osc}}\right| \tag{4.10}$$

where f_a is the free-running frequency of the *N*-stage divider. From (4.10), it is seen that (a) the locking range is proportional to the number of injected phases (*M*); (b)

Under the same locking range, the injection current I_{in} is lowered by M times; (c) With higher mixer's efficiency, the injection current is increased, resulting in wider locking range. Fig. 4.12 demonstrates the special case when N=M=3. With three-phase injections, the phase change of each LPF θ is equal to the phase change (ϕ) introduced by the injection current. The overall phase shift of each LPF thus becomes $-\pi/3+\phi$.

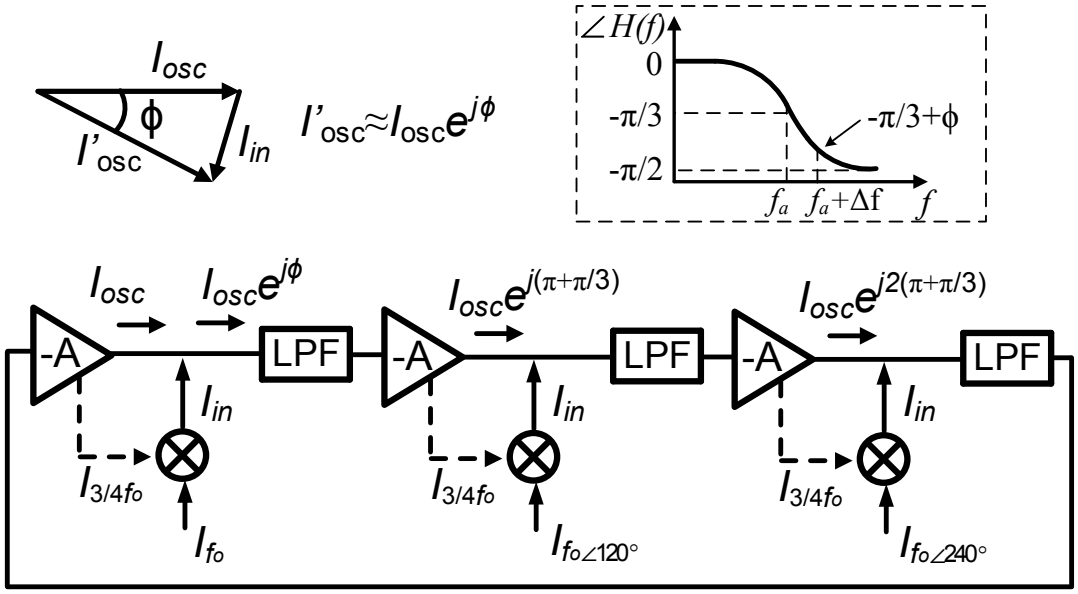


Fig. 4.12. The three-stage divider with three-phase injection (N=M=3), where the phase change of each LPF is equal to the phase change ϕ introduced by the injection current I_{in}.

Fig. 4.13 shows the circuit implementation of the proposed divider. The amplifying stages (T_{a2}~T_{c2}) with the t-lines of L_{DM} and L_{DB} form the divider's three-stage ring and transistors T_{a1}~ T_{c1} act as the three mixing cells. The three-phase input signals are fed to the base terminals of the mixing cells, and mixed with the loop's 3rd harmonic signals. The mixer's outputs ($1/4f_0$, $1/4f_0\angle 120°$, $1/4f_0\angle 240°$)

flow back to the loop at three injection points. Similar the VCO of Fig. 4.6, L_{DB} blocks the loop's 3rd harmonic signal $3/4f_o$ to flow to the next stage, forces it to flow into the mixer. This enhances the mixing efficiency and thus further increases the locking range. A buffer is used to feed the divider's output $1/4f_o$ to the rest of the divider chain (÷256) and two dummy buffers are added to provide symmetric parasitic loading to other stages.

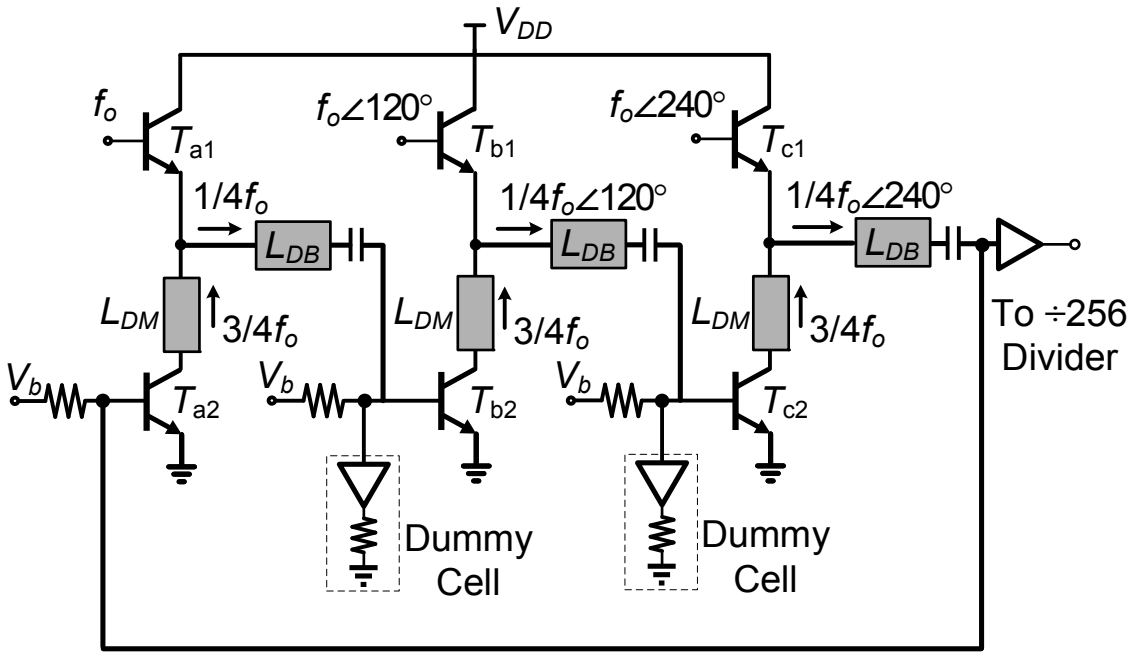


Fig. 4.13. The schematic of the proposed three-phase injection locked divider (÷4).

4.4. Integration and Layout of VCO and Divider

At high frequencies, any interconnect or cross-over introduces parasitics that cause severe signal distortion. This distortion will adversely affect the performance of the synthesizer's VCO and divider such as phase-noise, output power, and input sensitivity. The structural similarity of the proposed VCO and the three-phase

injection divider helps us co-design/co-optimize these blocks and develop a compact layout. Shown in Fig. 4.14 is the integration of the VCO and the divider within the synthesizer, where the inner blue circle indicates the VCO ring. The VCO's f_o travels along the inner blue ring and its 3rd harmonic signals are collected coherently at the center's $3f_o$ pad. The t-line's length realizing L_C determines the perimeter of the VCO ring and the length of L_{VB}. The t-line L_{VB}, used to introduce 10° phase shift for transistor optimum condition, forms the ring's perimeter. By narrowing L_C and widening L_{VB} to proper values, the L_{VB}'s t-line is fitted into the VCO ring. Three CAVs are placed in the layout with respect to divider's three-phase inputs such that no extra t-line or signal cross-over is required. The outer rectangle realizes the divider's loop, which is locked to the VCO ring and performs divide-by-4. The divider's output $1/4f_o$ is then fed to the synthesizer divide-by-256 and forms a close-loop through PFD/CP and LF. Two testing ports ($3f_o$ and $1/4f_o$) are used to measure the synthesizer's output spectra and its locking behavior.

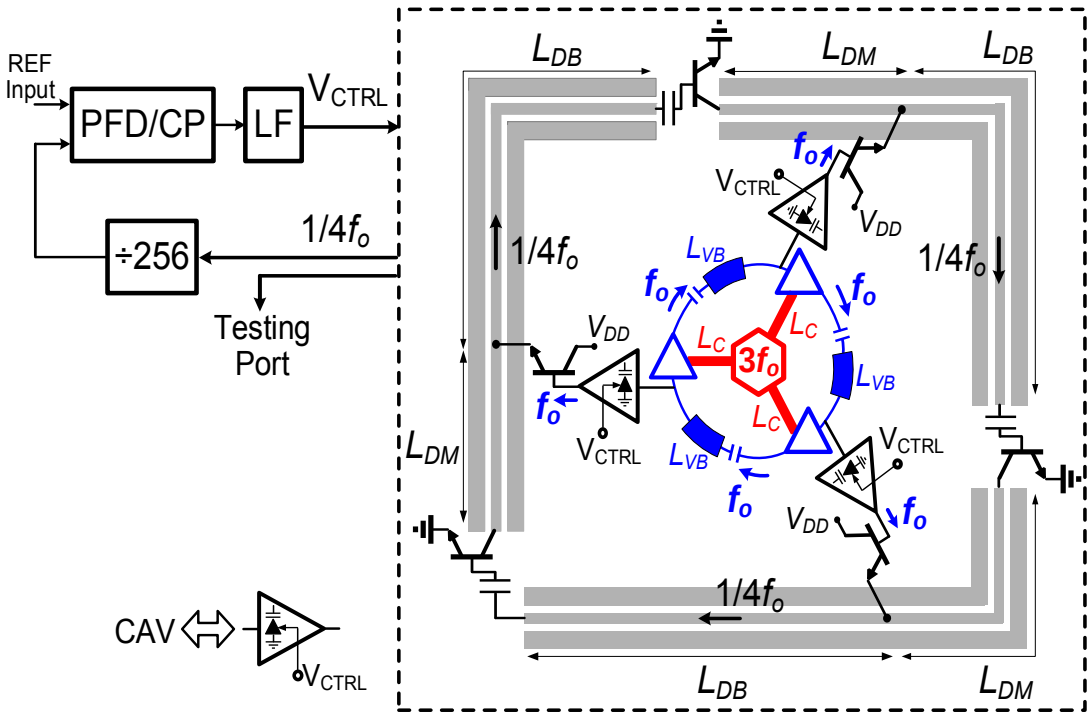


Fig. 4.14. The integration of the proposed VCO and divider within the synthesizer where the inner blue circle and outer rectangle indicate the VCO's and the divider's three-stage rings, respectively.

4.5. Measurement

Three individual circuits including a divider, a VCO+divider and a 300 GHz frequency synthesizer were fabricated in 90 nm SiGe BiCMOS with six metal layers and f_T / f_{MAX} of 260 GHz / 315 GHz. Their die micrographs are shown in Fig. 4.15 (a) and (b). The synthesizer chip area is 1.6 × 1.6 mm^2 including DC and RF pads. All the t-lines were implemented using coplanar waveguides (CPWs) with a 2.8 μm thick-top-metal (M6) as the signal line and M3 as the shielding ground. The CPWs and the interconnection lines were carefully characterized using planar 3-D electromagnetic simulations.

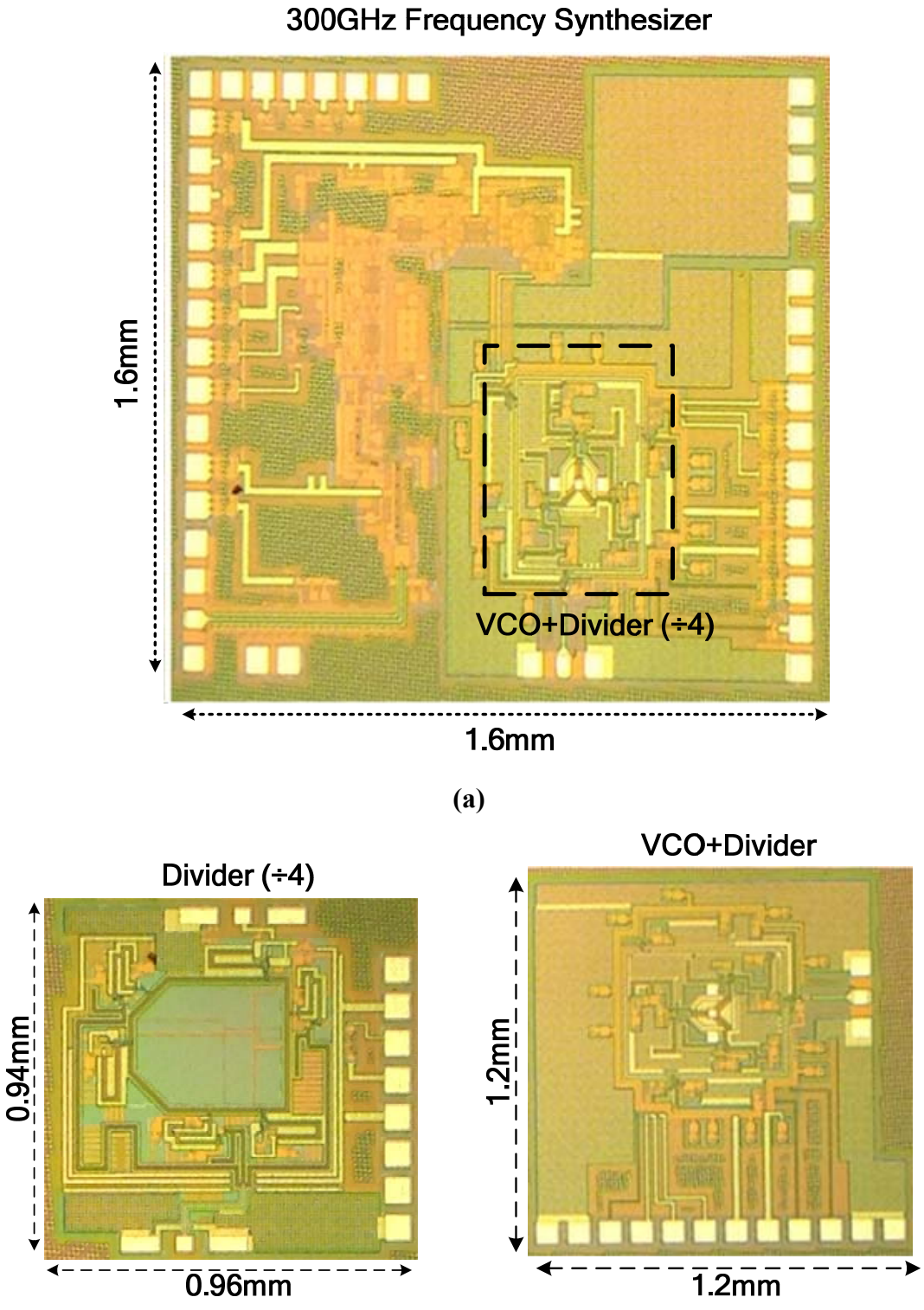


Fig. 4.15. The die micrographs of (a) the proposed 300 GHz frequency synthesizer, and (b) the stand-alone divider (÷4) and the VCO+divider.

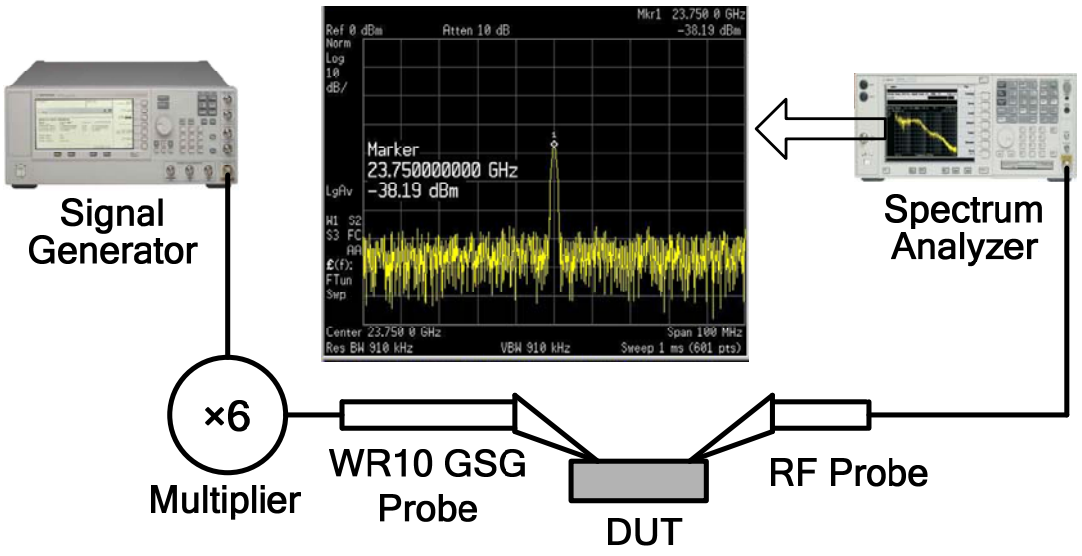


Fig. 4.16. The stand-alone divider measurement setup.

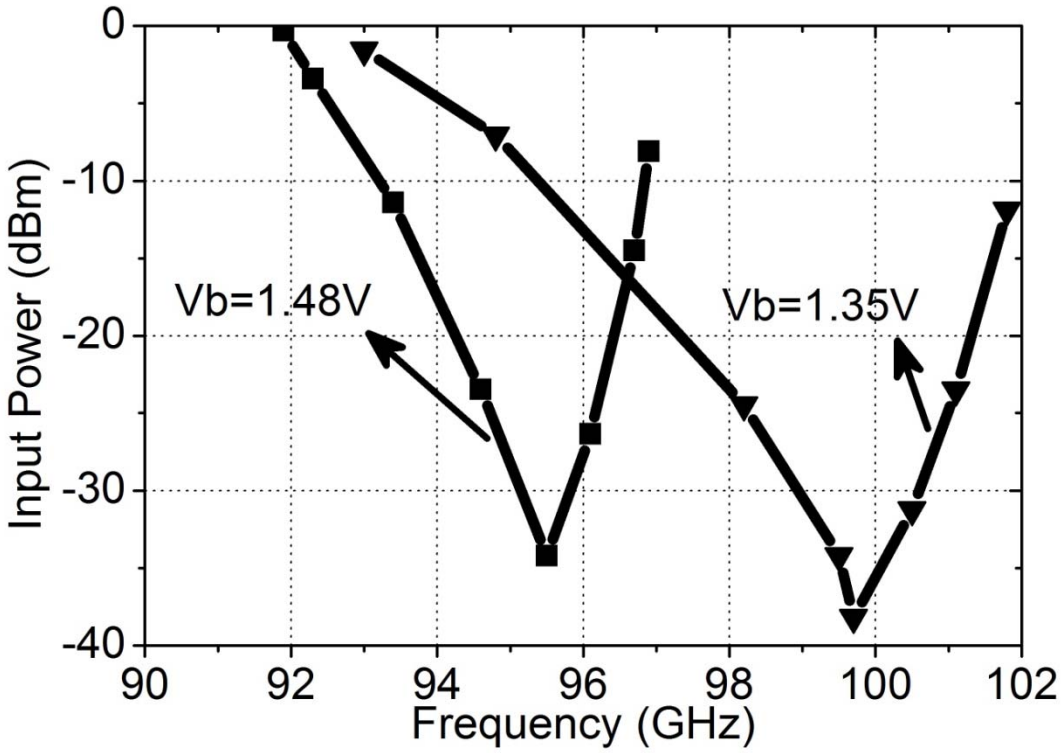


Fig. 4.17. The measured divider's input sensitivity with two bias settings.

In order to generate a three-phase signal for measuring the divider's input sensitivity, an on-chip three-way power divider and two on-chip phase shifters were used to provide input to the stand-alone divider. In the divider measurement setup

shown in Fig. 4.16, an external W-band signal from a multiplier (×6) was applied to the divider input using a WR-10 GSG waveguide probe, and the divider output was connected to the spectrum analyzer (SA). With the measured divider's output spectrum and the input frequency, the divider's locking to the input signal was verified. By sweeping the input frequency and power, the divider's input sensitivity was measured. Fig. 4.17 shows the plot of the input sensitivity versus input frequency for two bias settings (Vb=1.35 V and Vb=1.48 V). With the two bias settings, the measured overall locking range is 91.9~101.8 GHz and the divider's average DC power consumption is 48.4 mW. At Vb=1.35 V, the divider's free-running frequency is 99.5 GHz. At the higher bias voltage (i.e., Vb=1.48 V), the free-running frequency decreases to 95.5 GHz due to the larger C_{π}'s of the divider's amplifying transistors. Moreover, under this bias condition the amplifying transistors generate smaller 3rd harmonic signals, results in locking-range degradation.

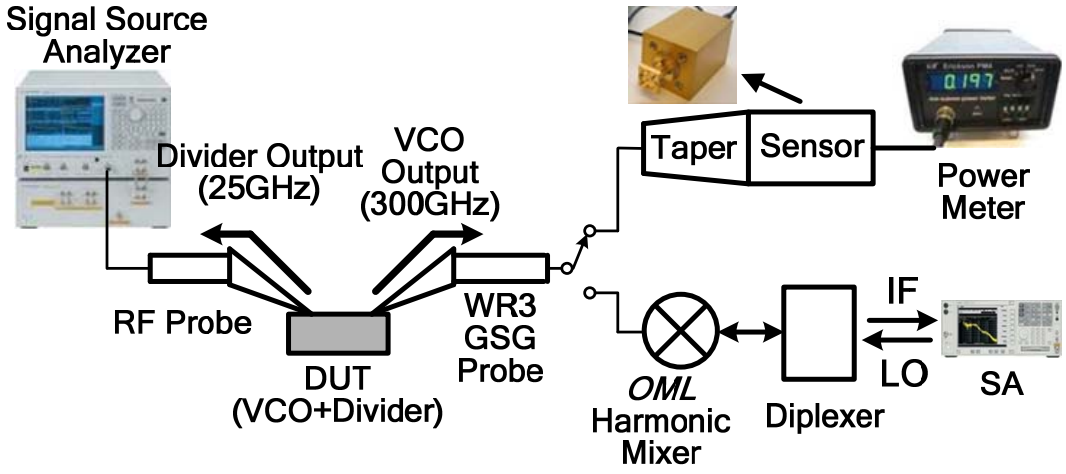


Fig. 4.18. The VCO+divider measurement setup.

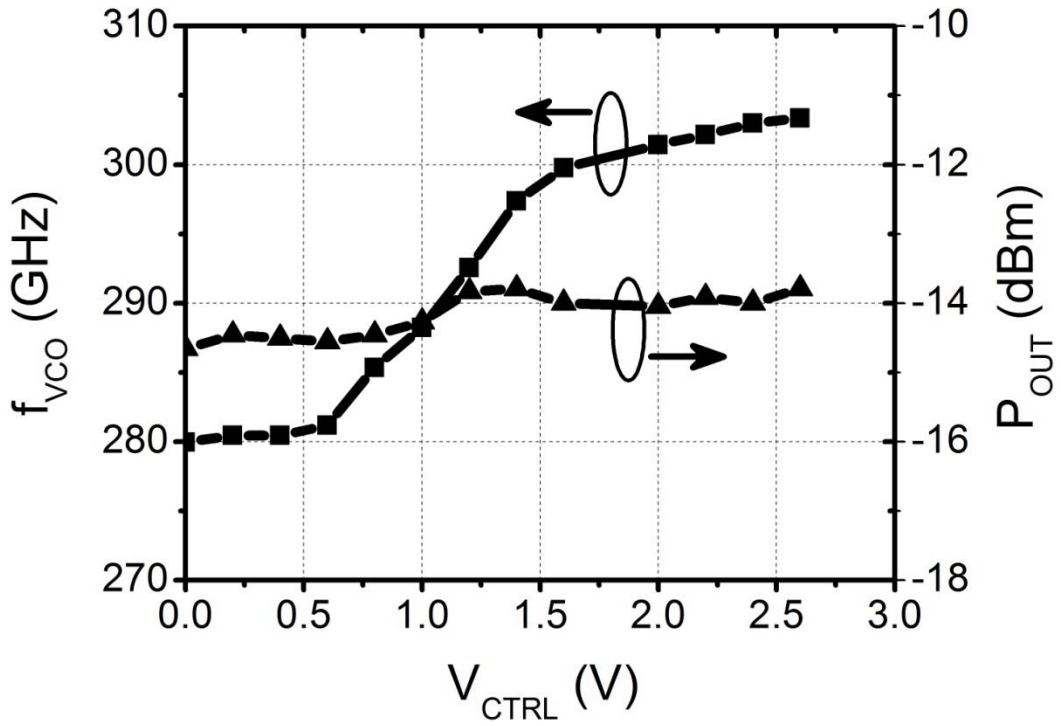


Fig. 4.19. The measured VCO's oscillation frequency and output power versus V_{CTRL}.

The VCO+divider chip was used to measure the VCO free-running performance and verify the divider's functionality with its input fed by the VCO. Fig. 4.18 shows the measurement setup. For the VCO's output power measurement, the VCO output was connected to a WR-3 waveguide GSG probe followed by the calorimetry power sensor. The waveguide taper was used to transform waveguide interface from WR-3 to WR-10. The measured power was calibrated by the loss of the signal path including the probe and the taper. For the VCO's oscillation frequency and tuning range measurement, the VCO's output signal was down-converted to the SA by using the harmonic mixer. Meanwhile with the divider's measured output spectrum, the divider locking characteristic was validated

over the whole VCO tuning range. Since the divider is locked to the VCO and the conversion loss of the harmonic mixer is high (>70 dB), the VCO phase-noise is measured at the divider output. This phase-noise measurement is close to the direct measurement of the VCO's output. This is because that the output phase-noise profile of an injection locked divider is similar to a first-order PLL, where the input noise is low-pass-filtered while the divider noise is high-pass-filtered and is thus negligible [48].

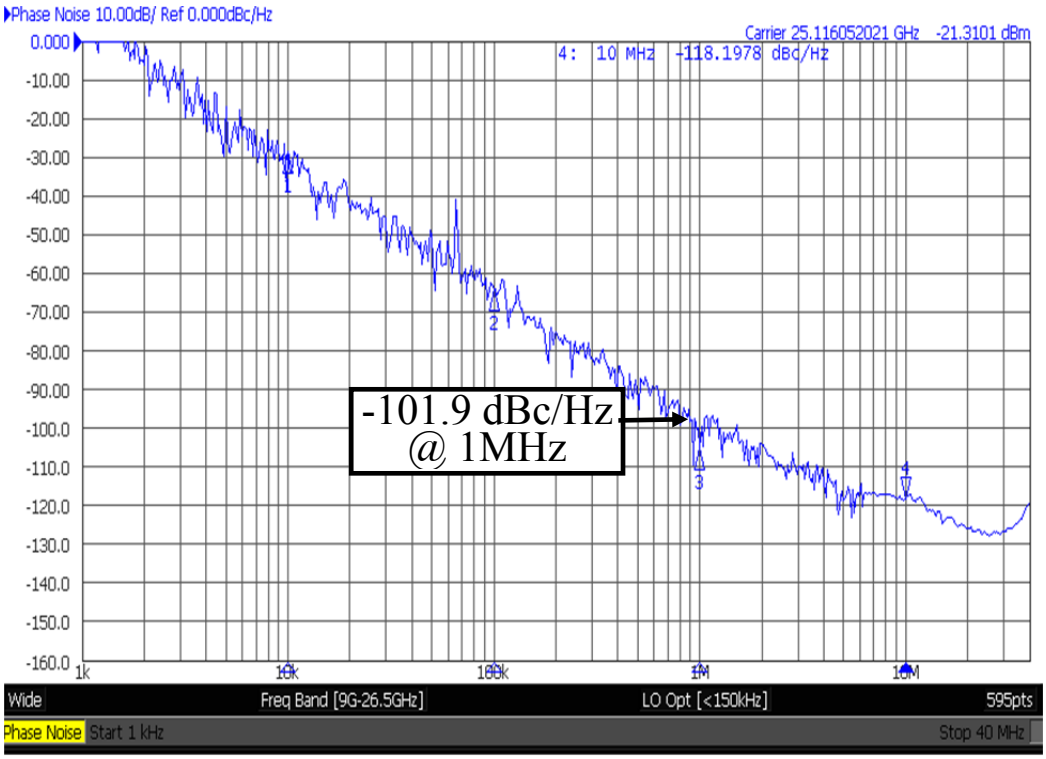


Fig. 4.20. The measured phase-noise profile at the divider's output where the input VCO frequency is 100.4 GHz.

Shown in Fig. 4.19 is the measured VCO's oscillation frequency and output power. The oscillation frequency varies from 280~303.36 GHz (i.e., 8 % of tuning range) with V_{CTRL} varying from 0~2.6 V. The measured output power is −14 dBm

with less than 0.5 dB variation. Fig. 4.20 shows the measured phase-noise profile at the divider's output where the input VCO frequency is 100.4 GHz. The phase-noise at 1 MHz offset is −101.9 dBc/Hz, and the corresponding VCO phase-noise is −80.3 dBc/Hz (with a factor of $20log_{10}4$). The VCO's DC power consumption is 105.6 mW.

The synthesizer measurement setup is similar to that of the VCO where the synthesizer's $3f_o$ output was down-converted to the SA and its $1/4f_o$ was connected to the signal source analyzer. The synthesizer input was fed using a crystal oscillator or a signal generator (SG) for measuring the synthesizer's locking range. The measured synthesizer's output spectrum was shown in Fig. 4.21 when the synthesizer was locked at 300.8 GHz. Fig. 4.22 shows the measured phase-noise profile at the $1/4f_o$ output port when the synthesizer was locked to a 95 MHz reference feeding by the SG. The profile depicts a close-loop locking behavior, in which the frequency response for input noise is low-pass-filtered and VCO noise is high-pass-filtered. The synthesizer's locking range was measured by sweeping the input frequency from the SG and measuring the output spectra. Shown in Fig. 4.23 is the measurement of the synthesizer's scale-up phase-noise versus its output frequency. The locking range varies from 280~303 GHz, which closely follows the VCO's tuning range. The minimum phase-noise at 1 MHz offset is −75.4 dBc/Hz when the synthesizer's

output frequency is 296 GHz. With the input signal fed from a 96 MHz crystal oscillator (i.e., the synthesizer's output frequency is 294.9 GHz), the measured phase-noise is −82.5 dBc/Hz (−89.6 dBc/Hz) at 1 MHz (10 MHz) offset. Fig. 4.24 shows the measured phase-noise profiles at 294.9 GHz for the free-running VCO, the synthesizer with its input from the SG (labeled as FS_SG) and from the crystal oscillator (labeled as FS_XTAL), input signal from the SG (labeled as SG) and from the crystal oscillator (labeled as XTAL). In a comparison between the two plots of FS_SG and FS_XTAL, the in-band phase-noise follows the input noise, and thus a better input signal results in a lower phase-noise. Note that one of the important advantages using a synthesizer over a VCO is that, because of the close-loop locking behavior, the phase-noise within the synthesizer's loop bandwidth is significantly reduced (e.g., −45 dBc/Hz and −77.8 dBc/Hz at 100 kHz offset for the VCO and the synthesizer, respectively). Table 4-1 shows the measured performance summaries of the proposed divider, VCO and synthesizer.

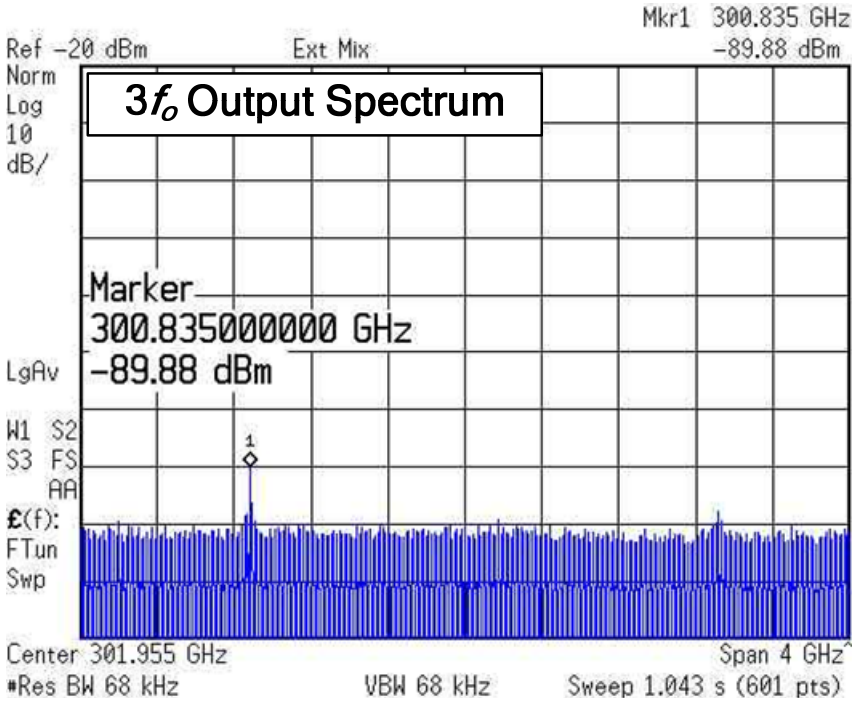


Fig. 4.21. The measured synthesizer's output spectrum.

Tables 4-2 and 4-3 provide the performance comparison with the prior work for the VCO and the 300 GHz synthesizer, respectively. In the VCO's comparison table, the proposed VCO demonstrates the widest tuning range and a better phase-noise with a less DC power consumption. Note that for the oscillators reported in [49] and [51], the frequency tuning is achieved by changing the supply voltage, and thus suffer from considerable output power variation.

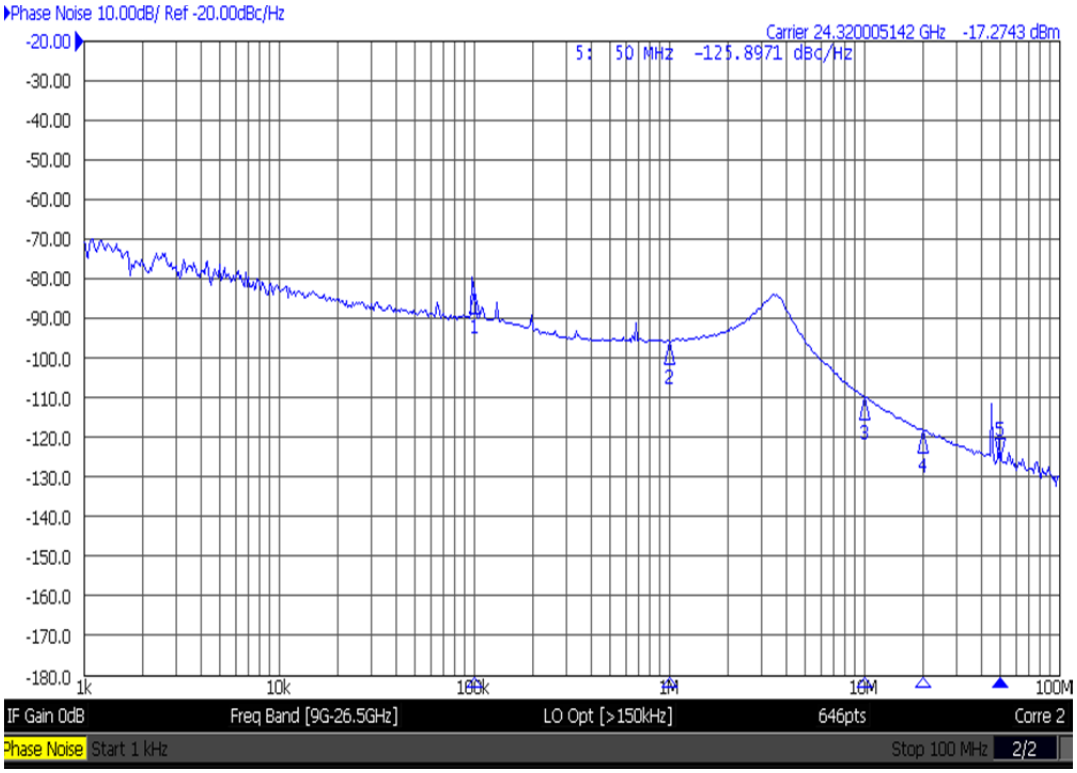


Fig. 4.22. The measured phase noise profile at the synthesizer's $1/4f_o$ output when the synthesizer was locked to a 95 MHz reference feeding by the SG.

In the synthesizer comparison table, [24] reports the highest synthesizer in III-IV technology with an f_{MAX} of 800 GHz, and [23] presents the highest in silicon using a similar technology to our work. Our synthesizer demonstrates higher operation frequency and divider ratio, wider locking range (60 times wider than that in [24]), and comparable phase-noise. The use of a crystal oscillator instead of an SG makes our synthesizer a practical and complete system. The proposed synthesizer achieves a 20 dB better figure-of-merit (FOM_T) among the other work.

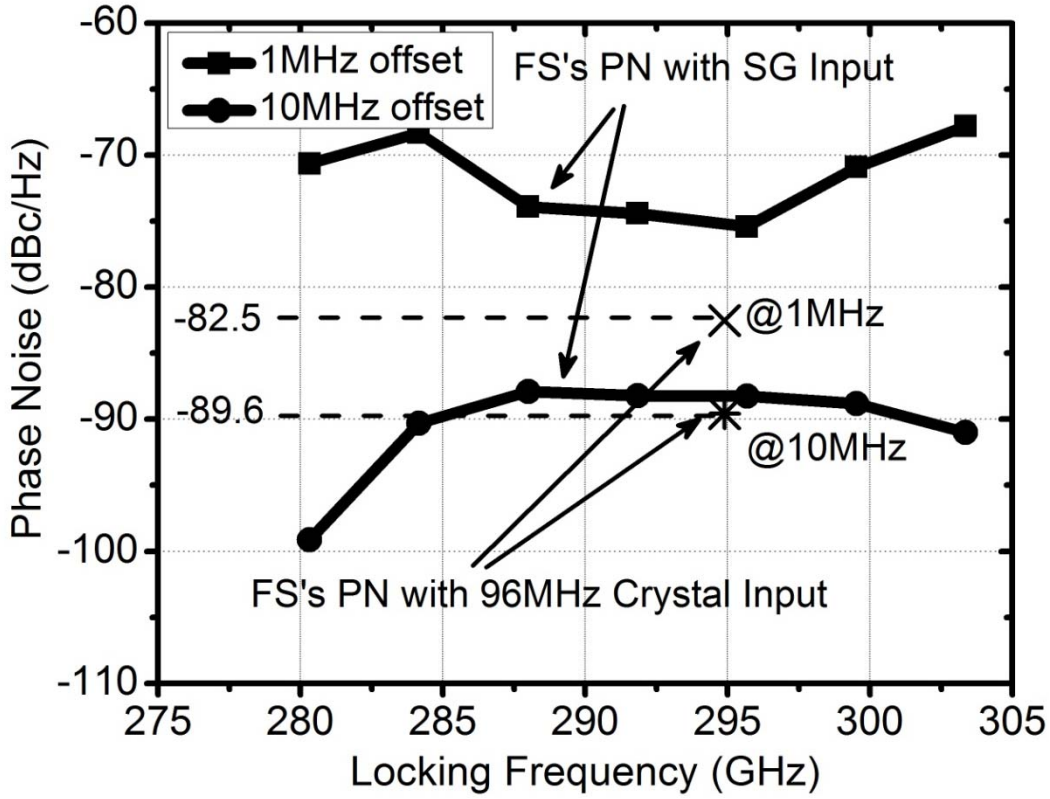


Fig. 4.23. The measurement of the synthesizer's scale-up phase-noise versus its output frequency with the synthesizer's input reference from a SG and a crystal oscillator.

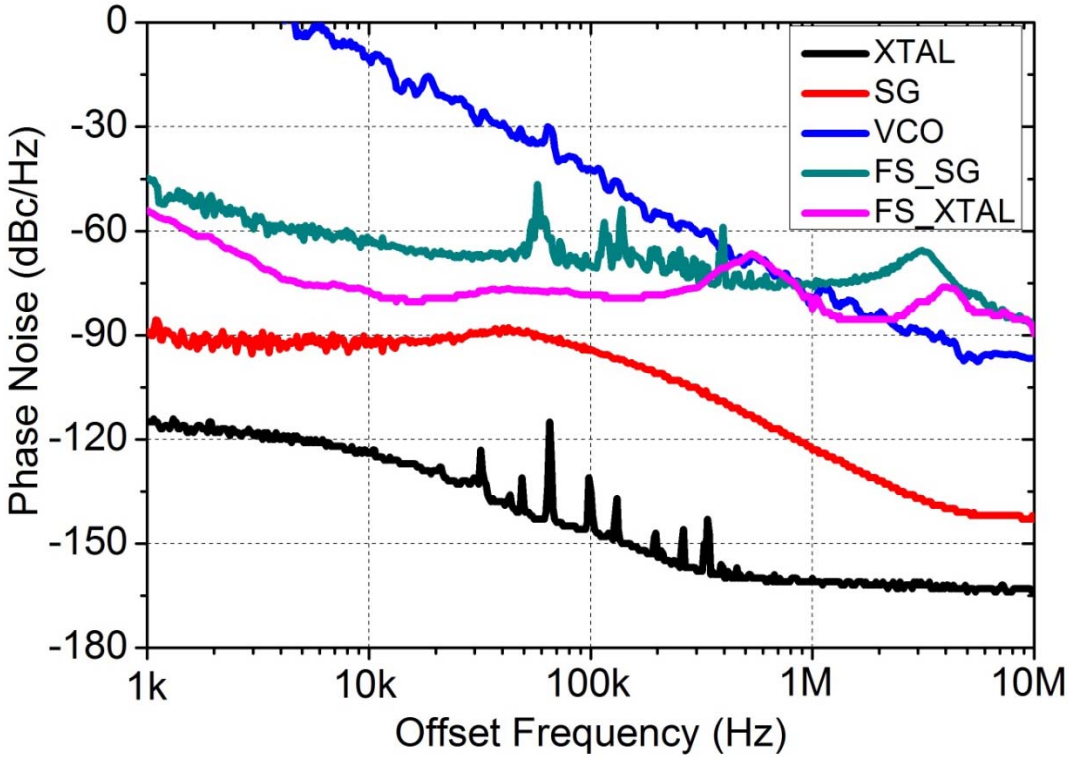


Fig. 4.24. The measured phase noise profiles of the synthesizer, the VCO and the input reference.

4.6. Conclusion

A fully integrated THz frequency synthesizer including a triple-push VCO with Colpitts-based active varactor (CAV) and a three-phase injection locked divider was implemented in 90 nm SiGe BiCMOS. By using the VCO's 3rd order harmonic as the output signal and injecting its fundamental to the divider chain, the synthesizer's operation frequency was designed to become close to the transistor f_{MAX} while relaxing the divider's operation frequency. Meanwhile, the three-phase injection improved the divider's locking range to cover the VCO's tuning range. The proposed synthesizer thus achieved a wide locking range which follows the VCO's tuning range. The proposed CAV provided frequency tunability and varactor isolation to the VCO, and acted as a buffer between the VCO and the divider. In addition to the similar structure of the VCO and the divider, an efficient circuit co-design and compact layout was achieved. To the best of our knowledge, this work reports the highest frequency synthesizer in silicon and is capable of using a crystal oscillator as the input.

TABLE 4-1
Performance Summary

Three-Phase Injection-Locked Divider		**Triple-Push VCO**		**300GHz Frequency Synthesizer**	
Frequency (GHz)	93 ~ 101.8	**Frequency (GHz)**	280 ~ 303.36	**Frequency (GHz)**	280.32 ~ 303.36
Divider Ratio	4	**Tuning Range**	8%	**Divider ratio**	1024
Locking Range	10.2%	**Output Power (dBm)**	−14	**Locking Range**	7.9%
Input Power (dBm)	< 0	**PN @ 1MHz offset (dBc/Hz)**	−80.28	**PN @ 100kHz offset (dBc/Hz)**	−77.8 @ 294.9GHz
Supply (V)	2	**Supply (V)**	1.8	**PN @ 1MHz offset (dBc/Hz)**	−82.5 @ 294.9GHz
DC Power (mW)	48.4	**DC Power (mW)**	105.6	**DC Power (mW)**	376

TABLE 4-2
VCO Comparison

	This work	[19]	[49]	[50]	[51]
Frequency (GHz)	**290**	290	288	280	316
Tuning Range (%)	**8**	4.5	1.4*	3.2	1.9*
PN @ 1MHz offset (dBc/Hz)	**−80.28**	−78	−87	NA	NA
Output Power (dBm)	**−14**	−1.2	−1.5	−7.2	−21
DC Power (mW)	**105.6**	325	275	810	46.4
Technology	**90nm SiGe BiCMOS**	65nm CMOS	65nm CMOS	45nm SOI CMOS	45nm SOI CMOS

TABLE 4-3

Synthesizer Comparison

	This work	**[24]**	**[23]**
Frequency (GHz)	**280.32 ~ 303.36 (3^{rd})**	**300.76 ~ 301.12 (fund.)**	**160 ~ 169 (2^{nd})**
Divider ratio	**1024**	**10**	**128**
Locking Range	**7.9%**	**0.12%**	**5.5%**
PN @ 100kHz/1MHz offset (dBc/Hz)	**–77.8 / –82.5**	**–78 / –85**	**–75 / –78**
DC Power (P_D)	**376 mW**	**301.6 mW**	**1250 mW**
FOM_T^* @ 100kHz/1MHz offset	**–179.4 / –163.9 dBc/Hz**	**–144.4 / –131.4 dBc/Hz**	**–163.1 / –146.1 dBc/Hz**
Technology (f_{max})	**90nm SiGe BiCMOS (315 GHz)**	**InP HBT (800 GHz)**	**130nm SiGe BiCMOS (280 GHz)**

$$*FOM_T = PN - 20\log\left(\frac{f_o}{\Delta f}\cdot\frac{Locking\ Range}{10}\right) + 10\log\left(\frac{P_D}{1mW}\right)$$

Chapter 5

Conclusion

In this dissertation, a push-push inductive-tuning 200 GHz VCO in SiGe BiCMOS, a fundamental 200 GHz double-stacked VCO in 32nm SOI CMOS, and a 300GHz frequency synthesizer with wide locking range implemented in 90nm SiGe BiCMOS have been demonstrated. New circuit and architecture topologies have been proposed, and implemented of capable of achieving the performance requirements. Sophisticated measurement has been carried out to verify the fabricated prototypes.

In Chapter 2, a detailed circuit analysis of the proposed variable inductor was presented, which shows in agreement with circuit simulation. Following the analytical steps to choose the component values (i.e., the resistor and the inductor at the base terminal), a variable inductor with high quality factor is obtained. In cooperating with a transformer, the inductor can be used to control the VCO's oscillation. A push-push 200GHz VCO utilizing the idea was fabricated for verification. Base oo the measurement results, the VCO achieves a oscillation frequency from 198 GHz to 205 GHz, a output power of −7.2 dBm, and a phase noise of −87.2 dBc/Hz at 1 MHz offset. With the proposed high-Q variable inductor,

the DC-to-RF power efficiency of the VCO is higher than the prior work.

Even if a push-push VCO could oscillate at half frequency of the output signal, it always outputs a single-ended signal. In many advanced transceiver architectures, a differential local oscillator (LO) signal is required. One way of transforming a single-ended signal to differential is by using a passive balun. The insertion loss of the balun degrades the LO's signal power and its phase noise. A fundamental VCO (differential-type) by its nature provides a differential output with small amplitude/phase error. In Chapter 3, a new double-stacked cross-pair was proposed to increase the negative resistance. An intuitive way to explain is that by adding a pure negative source-degenerated resistor of a cross-coupled pair, the transconductance of the transistor is increased, leading to a stronger negative resistance. By using this technique, the loss of the LC tank is compensated at high frequency, resulting in a oscillation. The proposed VCO achieves a oscilaltion frequency of 204.7 GHz to 212.7 GHz, a output power of −13.5 dBm and a phase noise of −81 dBc/Hz at 1 MHz offset.

Having discussed VCOs in the previous chapters, in Chapter 4, a 300 GHz frequency synthesizer with wide-tuning range was proposed. A free-running VCO surfers from frequency fluctuation, and is vulnerable to temperature/process/supply induced frequency drift. And the close-in phase noise is high compared to a

close-loop counterpart. In this chapter, the design challenges of both the VCO and the first-stage frequency divider were discussed with its effects on the synthesizer performance. After that, a 300 GHz phase-locked-based synthesizer incorporating a triple-push VCO with Colpitts-based Active Varactor (CAV) and a frequency divider with three-phase injection was introduced. The synthesizer, implemented in 90 nm SiGe BiCMOS with f_T/f_{MAX} of 240/315 GHz, achieves 7.9% of locking range (280.32~303.36 GHz) and generates −14dBm of power at 290 GHz. Based on the measured 24.64 GHz output signal of the divider, the frequency-scaled phase noise of 294.9 GHz signal is −77.8 dBc/Hz (−82.5 dBc/Hz) at 100 kHz (1 MHz) offset.

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