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Santa Barbara

Highly Scaled High Dielectric Constant Oxides on III-V CMOS with Low Interface Trap and Low Leakage Densities

A dissertation submitted in partial satisfaction
of the requirements for the degree

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in
Materials

by

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With love,

Varistha (Gift) Chobpattana

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Abstract

Highly Scaled High Dielectric Constant Oxides on III-V CMOS with Low Interface Trap and Low Leakage Densities

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Varistha Chobpattana

Complementary metal-oxide-semiconductor (CMOS) transistors are being aggressively scaled, reaching the fundamental limits of silicon. Due to their much higher electron mobilities, III-V semiconductors are being considered as alternative channel materials to potentially replace Si. This requires the integration of high dielectric constant (high-k) oxides with III-V semiconductor layers, which is the most significant challenge to achieve high performance of III-V metal-oxide-semiconductor field-effect transistors (MOSFETs). Large interface trap densities, inherent to these interfaces, degrade the transistor performance.

In this dissertation, we utilize *in-situ* atomic layer deposition (ALD) combined with surface passivation techniques to reduce the interface traps densities between high-k oxides and III-V semiconductors to obtain highly scaled, low defect density interfaces. Cycles of hydrogen and/or nitrogen plasmas and metal-organic precursors were applied directly onto n- and p-type $In_{0.53}Ga_{0.47}As$ surfaces before high-k oxide ALD. The high-k oxides investigated include Al_2O_3, HfO_2, ZrO_2, and TiO_2. We examined the electrical characteristics of MOS capacitors (MOSCAPs), surface morphology of the surface, and chemical components of the interface.

High quality interfaces of high-k oxide and n-type $In_{0.53}Ga_{0.47}As$ with low interface trap densities (D_{it}) of 10^{12} eV^{-1} cm^{-2}, low leakage current density, and high capacitance densities gate stacks (>5 $\mu F/cm^2$) were achieved by the optimized cycles of

nitrogen plasma+tetrakis(dimethylamido)titanium (TDMAT) ALD surface cleaning. Using x-ray photoelectron spectroscopy, the interface region indicates that the removing As-oxides, sub-oxides, and As-As bonding are responsible for decreasing frequency dispersion in the midgap region of the n-type $In_{0.53}Ga_{0.47}As$, reducing midgap D_{it}, and unpinning Fermi level. The modified interface chemistry from Al_2O_3 to TiO_2 leads to lower frequency dispersion in accumulation. The highly polarized TiO_2 layer produces dipole, which serves to increase barrier height between oxide and semiconductor, controlling leakage current issue. Optimized plasma condition to the specific III-V surface creates rapid and complete coverage interface layer on the III-V surface and increases nucleation density for the high quality surface, which allows for the growth of extremely scaled high-k oxide directly on III-V channels. High quality interface also prevents subcutaneous oxidation. Different conditions of p-type $In_{0.53}Ga_{0.47}As$ surface passivation were investigated. Unpinned Fermi level on p-type $In_{0.53}Ga_{0.47}As$ surface was achieved. Comparison of electrical characteristics between n- and p-type $In_{0.53}Ga_{0.47}As$ MOSCAPs are presented. Different surface plasma treatment is needed for p-type $In_{0.53}Ga_{0.47}As$ for achieving high quality interface.

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Chapter 1

Introduction

1.1 III-V Complementary Metal-Oxide- Semiconductor (CMOS)

The silicon-based metal oxide semiconductor field effect transistor (MOSFET) has been the most important component of integrate circuits (ICs) since the 1960s. It is used as a building block for analog and digital applications such as amplifiers and switches. According to a famous projection, Moore's law, the number of transistors per area on each IC doubles every two years as the feature size decreases to improve performance and reduce cost. However, we are approaching fundamental limits for scaling Si MOSFETs. The International Technology Roadmap for Semiconductors predicts that the rate would slow down in 2013[1]. Following the update, while the physical gate length for microprocessors in manufacturing in 2012 was 22 nm, the processing nodes were 14 nm in 2014. As a result, vast research and development efforts are dedicated to finding new materials and device structures to enhance the performance and allow continued scaling. These include the use of strained Si,

Table 1.1: Principal Material Properties of Si, Ge, and III - V Semiconductor Compounds[2]

Property	Si	Ge	InP	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
e^* (m^*/m_0)	0.19	0.082	0.077	0.067	0.041	0.023	0.0145
E_g (eV)	1.12	0.66	1.35	1.42	0.74	0.36	0.17
μ_e (cm^2/Vs)	1500	3900	4600	8500	12,000	33,000	80,000
μ_h (cm^2/Vs)	450	1900	150	400	300	460	1,250
v_{sat} ($\times 10^7$ cm/s)	1	0.6	2.5	2.1	3.1	8	5

high-k/metal gate, and FinFETs device structures. However, more innovative device structures and novel materials may be needed to continue CMOS scaling.

High mobility materials, such as III-V compound and Ge semiconductors, have shown promise for future high-speed and low power applications. Figure 1.1 shows materials for "More Moore" diversification towards III-V logic applications[2]. Table 1.1 shows properties of Si, Ge, and the prominent III-V semiconductor compound substrates, including effective mass (e^*), energy gap (E_g), electron and hole mobility (μ_e and μ_h, respectively), and saturation velocity (v_{sat}). Materials such as InGaAs, InAs, and InSb have superior characteristics in terms of these properties that makes them promising candidates for low noise, low power, and high speed digital applications for n-type channel devices. Furthermore, they have flexibility to be band-engineered. For example, InAs has electron mobility as high as 33,000 cm^2/Vs. In combination with InGaAs, mobility and peak saturation velocity can thus be improved. In addition, InSb, GaSb, and various Sb-based alloys have high electron and hole mobilities and can be strained to be utilized in p-channel III-V logic applications[3, 4].

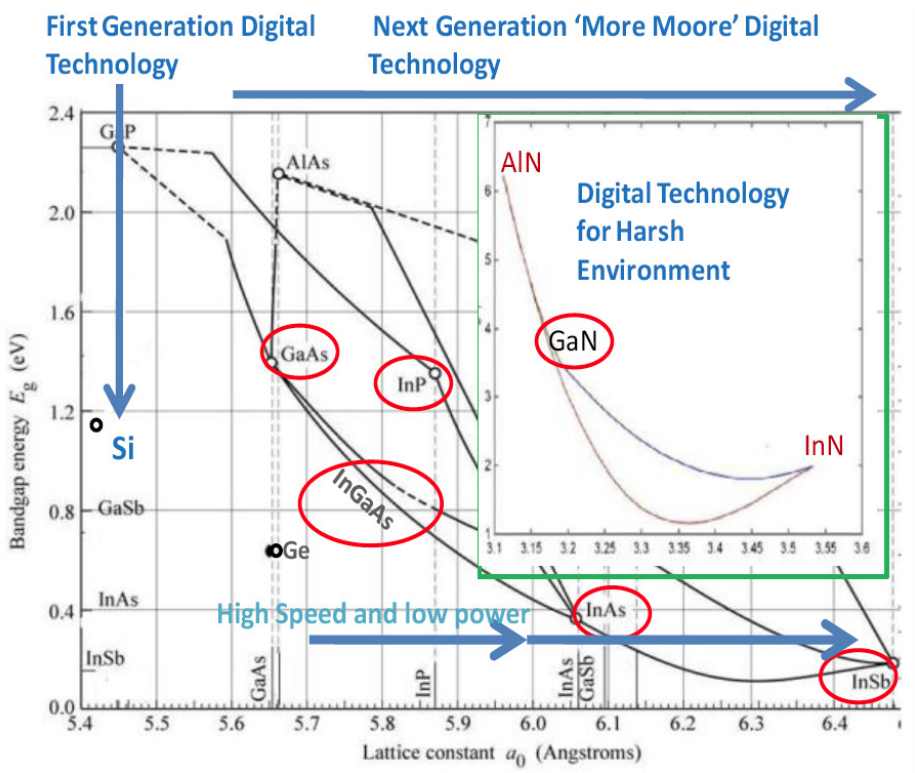

Figure 1.1: Diversity of III-V materials that can be used for logic applications, compared to to Si and Ge. Reprinted with permission from ref.[2]. © 2014 JNEP

There are a wide range of III-V compounds and they have low effective masses, which gives rise to high injection velocities. Their lower density of states, comparing to Si, yield less scattering, but limits achievable carrier densities. Higher mobilities also give lower access resistance. These superior transport properties paired with smaller bandgaps result in higher speed MOSFET performance. As for more performance per gate width, having more current requires less applied bias, which in turn reduce power consumption. In addition, higher performance decrease FET widths, which reduces IC overall size. Structurally, III-V compounds can be engineered to have strong heterojunction properties such as large band offsets, which give rise to better carrier confinement, decreasing leakage current issues in the devices.

Primary candidates for III-V channel MOSFET beyond 16 nm node normally include $In_xGa_{1-x}As$ ($0 \leq x \leq 1$) alloys. Because of their small bandgap ($0.36 \leq E_g \leq 1.42$ eV), they are suitable for low power applications with operating supply voltage ≤ 0.7 V and short gate length ($L_g < 7$ nm)[5]. Studies on various In contents have been conducted including $x = 15$ % In[6, 7], 20 % In[8, 9, 10], 53 % In[11, 12, 13], 65 % In[14], 75 % In[15], 100 % In[16] with Al_2O_3 ALD. Alloys with more than 50% content of In are of interest for nMOS applications with high performance due to their high electron mobility ($\sim 10^4$ cm^2 V^{-1} s^{-1}). However, the Fermi level pinning in the conduction band of InAs hinders it from being a strong candidate despite its high electron mobility. Only few results have been reported using InAs channels as a replacement for Si FET channels[17, 18]. Lattice-matched $In_{0.53}Ga_{0.47}As$ on InP substrate appears to be among the most studied particularly in terms of their potential in improving electron mobility by strain engineering.

1.2 Materials Challenges

1.2.1 Interface States in III-V Semiconductors

A universal challenge in developing III-V MOSFETs is the large interface trap densities (D_{it}). Interface trap densities scatter and trap charge carriers resulting in low drive current and low subthreshold slope (SS), which degrade transistor performances, and pin the Fermi level. Major sources of interface traps come from defects of the III-V semiconductor surface. The traps can be dangling bonds, vacancies, antisites, and native oxides. Studies of III-V semiconductor defects have been carried-out since the 1980s. Spicer *et al.* proposed the "unified model" for some III-V oxide interface states[19]. Using photoemission spectroscopy to determine the surface Fermi level position, energy levels of acceptor and donor due to missing atoms from the substrates are shown in Figure 1.2. These represent prominent defect levels at room temperature of these three semiconductors. The energy levels are known to ± 0.1 eV. They also propose the levels of interface states in the semiconductors as shown in Figure 1.3. The schematic shows that interface states occur in different parts of the III-V band gap for different semiconductors, including top part for InP, middle part for GaAs, or lower part for GaSb. These interface states affect the efficiency of Fermi level movement. Substantial density of traps states leads to Fermi level pinning, which creates an energy barrier for electrons and holes. No carrier modulation is obtained, degrading device performance. For GaAs, the Fermi level is pinned at the interface when density of interface states is 10^{12} - 10^{13} cm^{-2} eV^{-1}[20, 21].

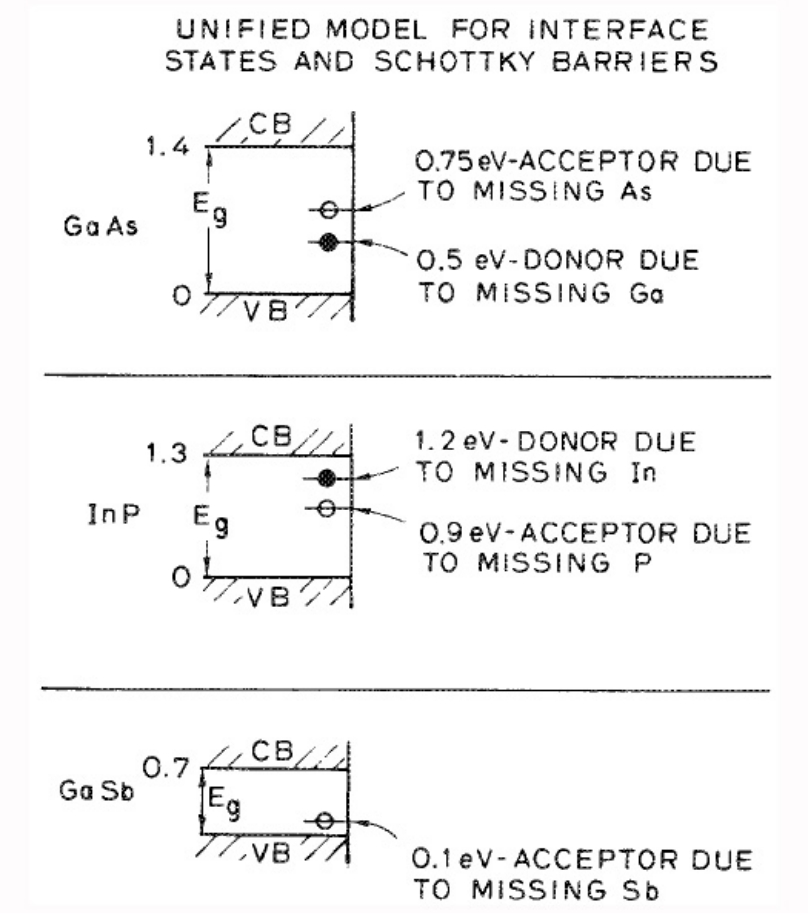

Figure 1.2: Unified model of interface states and Schottky barriers of GaAs, InP, and GaSb. Reprinted with permission from ref.[19]. © 1980 AIP Publishing LLC.

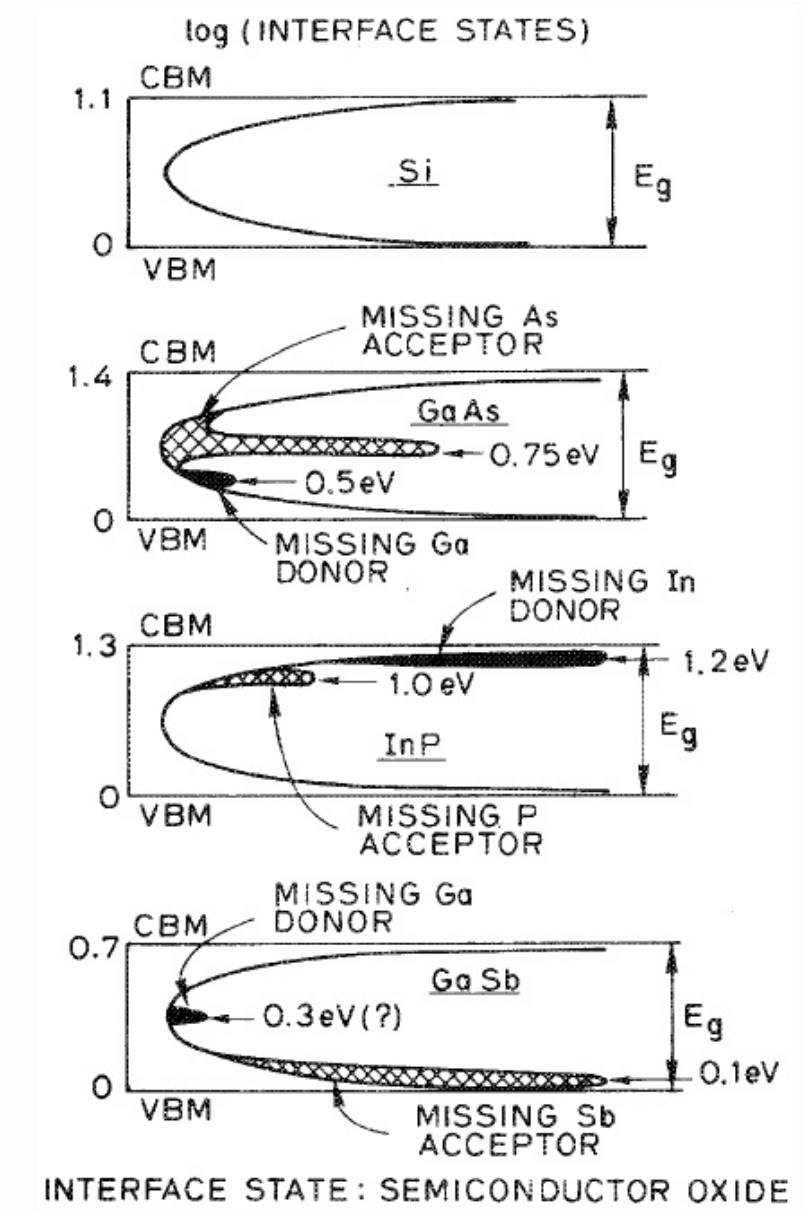

Figure 1.3: Energy level and the interface states of Si, GaAs, InP, and GaSb. Reprinted with permission from ref.[19]. © 1980 AIP Publishing LLC.

The energy level of the Fermi level pinning positions has been theoretically calculated for $In_xGa_{1-x}As$ $(0 \leq x \leq 1)$ alloys. Figure 1.4 shows the energy level as a function of In content[22]. The measured energy level for Fermi level pinning is around 1.0 to 1.2 eV. These energy levels are in good agreement with the reported theoretical values for As-As dimers states at the interface. Other defects also contribute to inefficient Fermi level movement and pinning behavior. The diagram in Figure 1.4 suggests that Ga and As vacancies and As antisites can contribute to Fermi level pinning. For example, calculations for As_{Ga} and Ga_{As} antisites on GaAs surface[23] suggested that As_{Ga} is a majority defect for the GaAs surface because the Fermi level normally locates above 0.5 eV from the valence band corresponding to the energy level of As_{Ga}. This result is in agreement with the report in ref.[22].

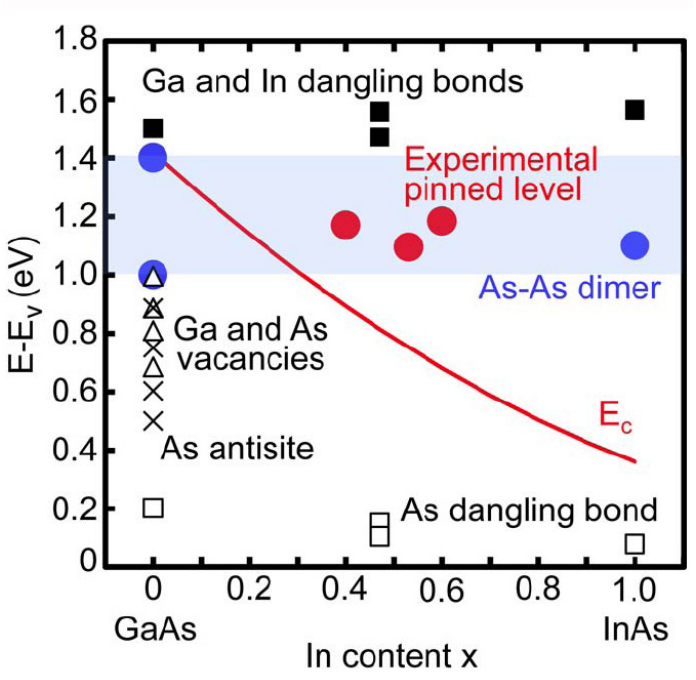

Figure 1.4: Energy levels from valence band maximum of Fermi level pinning and defect levels as a function of In content. Reprinted with permission from ref.[22]. © Copyright 2013 IEEE

The unusual structure of (2 × 4) GaAs surface also leads Robertson *et al.*[24] to

conclude that the Fermi level pinning results from As-As dimer bonds. The defect states shown in Figure 1.5 are from calculations where the bulk band edges have been aligned using bulk charge neutrality level (CNL) energies. Ga dangling bond states are all above the conduction band, creating no state in the band gap. On the other hand, As dangling bond states are above the valence band in all of these semiconductors, causing states in the lower half of the band gap. In addition, As-As dimers form states only in the GaAs band gap. It is also pointed out that the Fermi level depends on the surface termination of a specific system. For example, by applying electron counting rule to the interface, the Ga-terminated face results in the Fermi level lying in the valence band due to its 1/2 electron lacking from bonding to O-terminated HfO_2(100) layer. On the other hand, the As-terminated face yields an extra 1/2 electron, and the Fermi level lies in the conduction band.

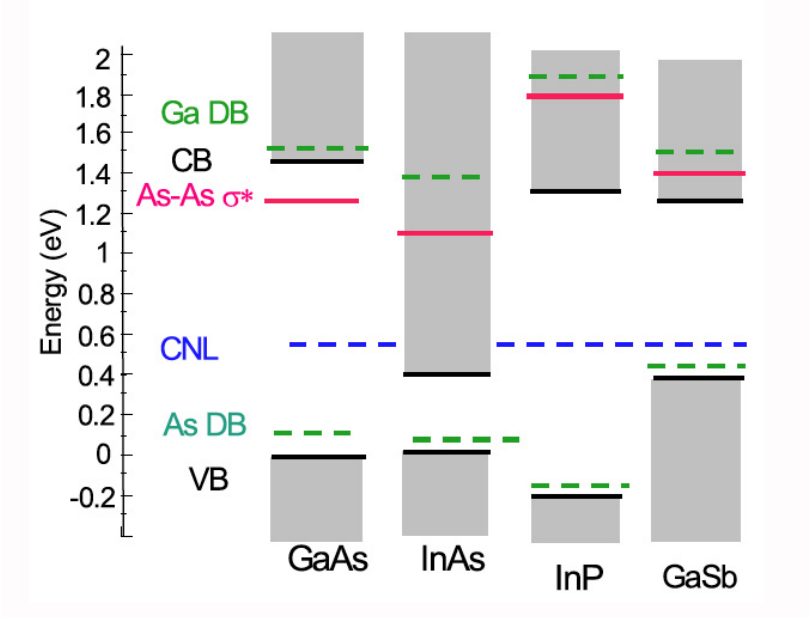

Figure 1.5: Defect energy levels for dangling bonds and dimer bonds of GaAs, InAs, InP, and GaSb. Reprinted with permission from ref.[24]. © 2015 AIP Publishing LLC.

Native oxides form as a result of oxidation of air-exposed III-V semiconductor

surface. The oxides form in several distinct layers with different compositions and thicknesses[25]. A report found that oxygen binds to Group V without breaking III-V bonds on the (110) GaAs surface[20]. It is suggested that bonding of oxides or other insulators to III-V surfaces will be through the Group V elements and only submonolayer quantities of oxygen are required to result in Fermi level pinning. The positions of the Fermi level pinning depends on the defects produced by this strain-induced oxygen chemisorption. These defects are considered as extrinsic states and provide approximately 10^{12} cm^{-2} surface states to pin the Fermi level. For Si, the presence of oxygen can remove the Fermi level pinning. On the other hand, oxygen exposure yields or modifies the Fermi level pinning on III-V materials[26, 27]. Some examples are shown in Figure 1.6. Since 10^8 langmuirs corresponds to approximately a tenth of a monolayer, the plots indicate that only a small fraction of a monolayer of oxygen coverage is needed to saturate the Fermi level pinning in GaAs. It is noted that the pinning mechanism for thick oxides and fraction of submonolayer oxide coverage may be the same due to defect formation by the adlayer of oxide or metal[28]. Another contrast behavior to the Si-SiO_2 is the direction of the formation of the addition defects. For Si-SiO_2, oxygen moves through the oxide to react with the Si at the Si-oxide interface. On the other hand, III-V atoms move outward to form interface defects. The III-V materials were found to move even further out into the upper deposited oxide and metal in a large amount[29, 30, 31].

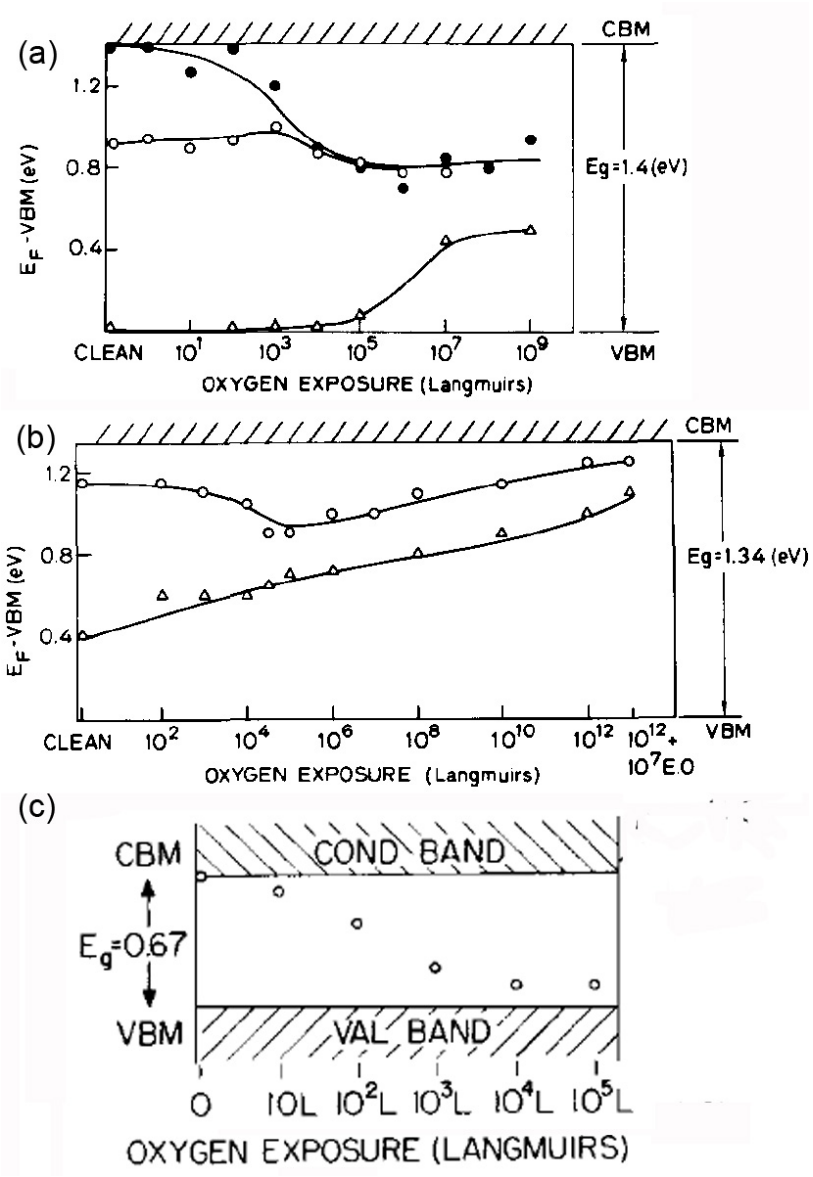

Figure 1.6: Fermi level pinning position as a function of oxygen exposure for (a) n-type GaAs ($\bullet, \circ$) and p-type GaAs ($\triangle$) ;(b) n-type InP ($\circ$) and p-type InP ($\triangle$);and (c) GaSb ($\circ$). Reprinted with permission from ref.[20, 27]. © 1976 and 1979 AIP Publishing LLC.

Oxides can also be formed during wet chemical treatment. These defects generate electronically active sites, which cause instability to the surface and impact device performance. The stability of the oxides is also important for determining the density of interface states. The instability of oxides such as As-oxides can lead to leakage problems. Overall oxidation of the surface is responsible for the formation of the large interface state defects, which also control the Fermi level position in the semiconductor bandgap[32]. Thus, As-oxide, As dangling bonds, and excess of As on the surface are responsible for the Fermi level pinning [33, 34, 35]. In addition, the presence of Ga oxide can also be associated with defects in device electrical characteristics [36]. There is evidence suggesting that In- and Ga- oxides states also locate primarily near the surface. However, due to their high thermal stability compared to As-oxides, they are likely not to critically impact device performance[37]. On the other hand, Ga- and In- oxides such as Ga_2O and In_2O, could help decrease interface disruption between high-k oxides and semiconductor [37, 38, 39].

There are also theoretical calculations suggesting the possibility of defects in the valence and conduction bands for other III-V semiconductors. These states also cause the Fermi level pinning and degrade mobility in MOSFETs[22]. This information indicates that different surface treatments are required to remove these states from different energy levels. In summary, surface and bulk chemistry should be strongly emphasized because an understanding of the interface chemistry does not only benefit the semiconductor industries, but it is important to understand the fundamentals of the interface phenomena.

1.2.2 Scaling Limits

As CMOS devices are scaled, the MOSFET performance is mainly controlled by the inversion charge capacitance. However, the effect of large electric field on the scaled dielectric thickness causes dramatic leakage issues and short channel effects. High-dielectric permittivity (k) materials are required as a replacement of SiO_2 for increasing charge density without reducing physical dielectric thickness. The equivalent oxide thickness (EOT) is a measure to relate high-k dielectric thickness to physical oxide thickness of SiO_2:

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} t_{ox} \tag{1.1}$$

where ε_{SiO_2} is the dielectric constant of SiO_2 (3.9), ε_{high-k} is the dielectric constant of high-k oxide and t_{ox} is the physical thickness of the high-k oxide. The EOT has to reach below ∼0.6-nm range to be suitable for devices of gate length below 22 nm. It is possible for the EOT to reach the ∼0.6-nm range without substantial leakage current.

High-k oxides currently studied include transition metal oxides and binary oxides. Many attentions have focus on the transition metal oxides, including group IVB, group IIIB, and rare-earth oxides[40, 41, 42, 43, 44]. However, many of them often show poor thermal stability to integrate onto Si devices. With some exceptions, more attention has been focused on specific high-k dielectrics such as HfO_2, Hf-based oxides, ZrO_2, or Zr-based oxides with high permittivity, and relatively high thermodynamic stability with low leakage current density[45, 46, 47, 48]. In fact, Hf-based materials are extensively studied and used as the gate dielectric in Si-CMOS since early 2000s. ZrO_2 are found to be slightly reactive with Si, forming $ZiSi_2$[49]. For this reason, HfO_2 is more preferable over ZrO_2. In addition, regardless of its high dielectric constant,

TiO_2 is not widely used due to issues with thermodynamic stability on Si[49, 50]. On the other hand, it is possible on III-V[51, 52].

In summary, HfO_2 passes many criteria to be a favorite as high-k gate dielectric. The requirements includes high-k-value, thermodynamically stability, kinetically stability, sufficient band offsets, compatibility with fabrication process, and good electrical interface. Thus, the development of high-k deposition without Fermi level pinning, surface and interface states need to be highlighted. In addition, the interface between the oxides and semiconductor needs to be controlled in order to maintain good electrical performances.

1.3 State of the Art

The most difficult and enduring problem is the passivation or avoidance of defects between gate insulators and III-V channel materials. As mentioned earlier, air-exposure causes traps on the III-V surfaces. Covering these surfaces until right before processing seems to be an intuitive solution to the problem. As-capping of III-V materials became useful for *in-situ* surface cleaning technique of the III-V surfaces. One of the early successful work has been shown that the As-cap on $In_xGa_{1-x}As$ surface can be removed and cleaned to achieve ordered surface [53]. Normally, the cap is deposited immediately after the III-V layer growth in the molecular beam epitaxy (MBE) machine. The cap is thick and dense enough for reasonable amount of time to protect the surface from oxidation during transportation. The cap will later remove by decapping process at relatively low temperature ($\sim$400 °C) in the ultra-high vacuum chamber before oxide deposition. Results from MOS capacitor experiments using As-decapping process have been showing with high quality interface with low midgap D_{it} response[54, 55].

Different wet chemical treatments were investigated as surface preparation methods of III-V semiconductor mainly for removing native oxides. Many of the chemicals are acids or bases, which preferably do not etch the semiconductor substrate. Some of the examples are HCl, HF, H_2SO_4, and NH_4OH. Other wet-cleaning related methods also include digital etching, which consists of a few cycles of oxidizing agent, diluted acid, or plasma treatment. The combination of these steps reduces damage on III-V semiconductors[56, 57, 58, 59]. Some chemicals show advantages over the others in a specific process or substrate materials[60]. However, all of these studies show only a slight improvement in the device performance. It was suggested that the method is considered effective as long as the solution is strong enough and the time is suf-

ficient to etch away the native oxide[61]. Alternatively, sulfur passivation of GaAs surface has been proposed for achieving lower defect states either using $Na_2S{\cdot}9H_2O$ or $(NH_4)_2S$ [62, 63, 64]. The study on $In_{0.53}Ga_{0.47}As$ also emphasized the benefits [13, 65]. It is explained in ref.[23] that excess arsenic (As_{Ga}) is soluble in sulfide solutions and removed by the sulfur reaction. This effect makes the Fermi level movement more efficiently near the valence band.

Plasma etching (or reactive-ion etching) of III-V semiconductors has been studied mainly to remove carbon contaminated molecules and native oxides. Various reactive agents were investigated such as fluorine (HF, CF_4, CHF_6, CF_3Cl), chlorine (CCl_4, C_2Cl_4, $CHCl_3$, CBr_2Cl_2,PCl_3), oxygen, and hydrogen[66, 67, 68, 69, 70]. However, dry-etching methods can cause more damage to the III-V semiconductor surface compared to wet-cleaning methods[71, 72]. Careful investigation and optimized conditions are needed to remove the contamination without damaging the high quality III-V surfaces. Hydrogen plasma treatment is one of the popular surface preparation methods that has been investigated for III-V semiconductors[73, 74, 21, 75, 76]. It is used as an *in-situ* cleaning method immediately prior to the high-k oxide deposition. One of the advantages of this method is its effectiveness at low temperature. It is believed to remove carbon contaminants and some native oxides from the surface. In same cases, hydrogen plasma etching can also help obtaining a preferred surface reconstruction[76, 77]. However, substrate damage can still be expected if the plasma conditions are not optimized for a specific substrate.

One of the most effective hydrogen plasma treatment before Al_2O_3 deposition by atomic layer deposition (ALD) on $In_{0.53}Ga_{0.47}As$ is investigated in ref.[78]. The experiment was done on air-exposed samples, which is convenient for transistor processing. Figure 1.7 shows capacitance-voltage curves as a function of frequency on four samples with different pre-deposition treatments. The frequency dispersion in

the negative bias region ("hump") qualitatively represents the amount of midgap D_{it} response of the samples. The result indicates that the hump significantly decreases when the sample is exposed to cycles of the *in-situ* hydrogen plasma. In addition, further decrease in the frequency dispersion is shown in the sample with combination of the hydrogen plasma and trimethylaluminium (TMA) [Figure 1.7(d)]. Conductance maps (not shown) indicate that the Fermi level is unpinned. This behavior suggests that the midgap trap density, D_{it}, is strongly reduced. The minimum D_{it} value reported in this work is in the low 10^{12} eV^{-1} cm^{-2}. This process offers a greatly enhanced flexibility to the device process flow.

Nitrogen plasma has been reported to passivate surface state density and effectively reduce D_{it} on III-V semiconductors, particularly GaAs and InGaAs[73, 79, 80, 81, 82]. Activated nitrogen atoms incorporate onto the semiconductor surface and form an interface of oxynitride layer. It was suggested that nitrogen predominently bonds to In and Ga atoms from $In_{0.53}Ga_{0.47}As$ substrate[80]. The increase in the amount of Ga-N bond attributes to replacement of As atoms by N atoms. This behavior might reduce As dimers and As-oxides, which are proposed to cause high D_{it} at the GaAs and InGaAs MOS interface[24]. The nitridation can also convert some of the Al_2O_3 layer into AlN, which acts as a diffusion barrier. In addition, in terms of avoiding Fermi level pinning, it was calculated that there is no presence of N-N dimer bonds and the N dangling bond states lie deeper in the valence band edge well below the band gap[83].

As mentioned earlier, plasma treatment combined with TMA exposure can provide beneficial surface treatment effects for Al_2O_3 on III-V semiconductors. Al_2O_3 acts as a diffusion barrier better than other oxides to prevent the oxidation of Ga and avoids formation of As interstitials[24]. A few cycles of ALD Al_2O_3 under a HfO_2 gate stack were sufficient to reduce interface traps[84, 85]. Some of the reports are shown in

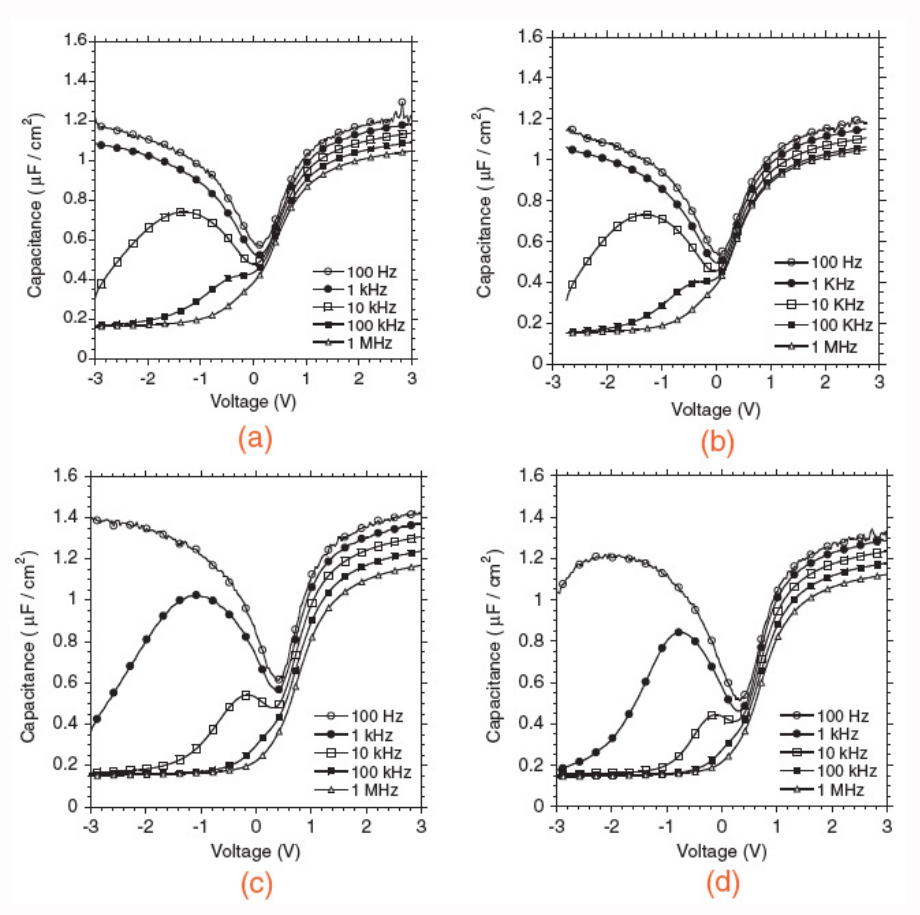

Figure 1.7: Capacitance-voltage curves as a function of frequency for (a) untreated samples; (b) TMA-treated sample; (c) hydrogen-plasma-treated sample; and (d) hydrogen-plasma and TMA-treated sample. Reprinted with permission from ref.[78]. © Copyright (2011) The Japan Society of Applied Physics

Figure 1.8. These examples are for gate stacks with a thin layer of Al_2O_3 under a HfO_2 dielectric layer on n-type $In_{0.53}Ga_{0.47}As$[86, 87, 88, 84]. The capacitance densities versus voltage curves at different frequencies show well-behaved curves and small response from midgap interface states densities. There are furthermore indications that TMA helps cleaning the III-V surface. One report suggests that the Al from TMA reacts with As^{+3} and Ga^{+3} oxidation states and form Al-oxide [7], and removes As-O and Ga-O bonds from the GaAs surface. An abrupt interface between Al_2O_3 and GaAs is possible by matching Ga-terminated face of GaAs to O-terminated face of the oxide or As-terminated face of GaAs to Al-terminated face of the oxide[24]. It was also suggested that the small TMA molecule inserts itself into As-As bonds and breaks them[89]. This reaction is referred to as the "self-cleaning" effect from TMA. Thus, it is important to introduce TMA into the first half-cycle of Al_2O_3 ALD deposition on a III-V surface. The clean-up reaction is believed to depend on the oxidation state. According to this, Hf precursor would not have the same effect as TMA because of its +5 state. The TMA self-cleaning effect appears to be effective in controlling the degree of interface oxidation, which results in unpinning Fermi level and decreasing D_{it}.

Overall, a sophisticated surface passivation scheme is required for high performance III-V MOSFETs to form a high-quality interface. The strict criteria to reach such performance includes low D_{it} in the range of 10^{12} - 10^{11} cm^{-2} eV^{-1}, low gate current density leakage of 10^{-8} A/cm^2 at gate voltage of flatband voltage + 1 V, scalable high-k dielectric to EOT of 0.5 nm with sufficient band offsets $>$ 1 eV as electrons and holes barrier, and high thermal stability at temperature $>$ 800 °C[90]. The effective surface cleaning can be a process of both wet and dry cleaning techniques. The details have to be optimized for the specific III-V substrate.

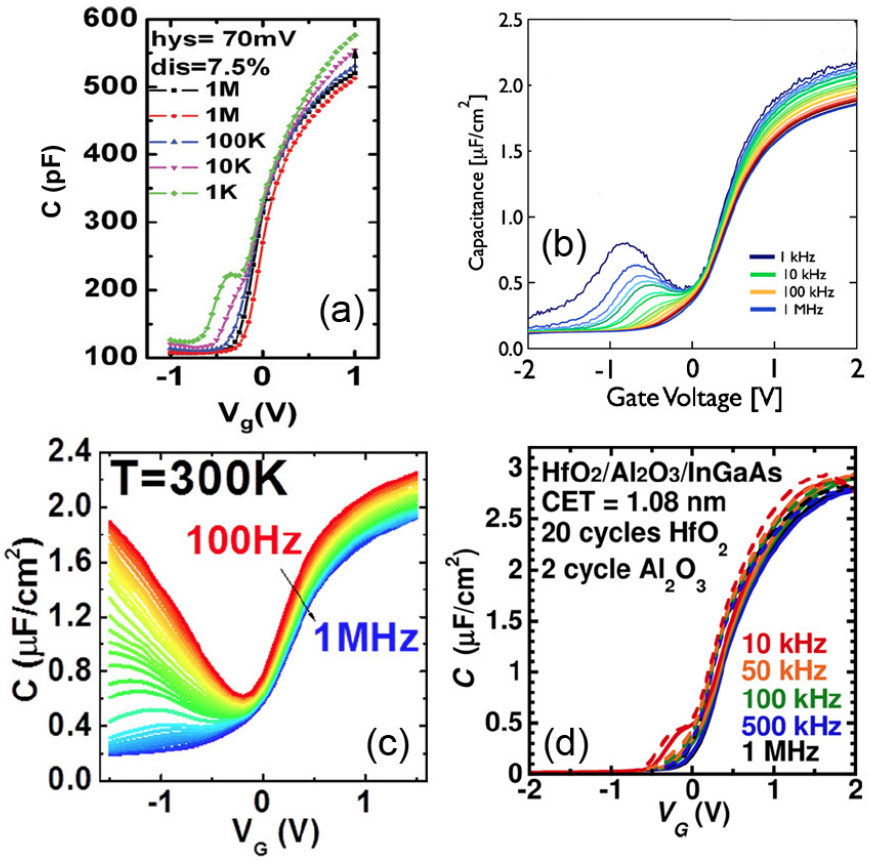

Figure 1.8: Capacitance-voltage curves as a function of frequency of samples with Al_2O_3/HfO_2 gate dielectrics on n-type $In_{0.53}Ga_{0.47}As$ from ref.(a) [86] Reproduced by permission of the Electrochemical Society; (b) [87]; (c) [88]; and (d) [84]. Reprinted with permission from ref.[87, 88, 84]. © 2011 and 2012 AIP Publishing LLC.

1.4 Atomic layer deposition (ALD)

Atomic layer deposition (ALD) is a vapor phase deposition technique which synthesizes sub-monolayers of ultra-thin films by typically alternating two half-cycles at sub-atmospheric pressure. During first half of the cycles, precursor adsorps to the starting surface followed by a purge step to remove excessive materials. For the second half of cycles, the surface is exposed to a reactant gas, vapor, or plasma species depending on a specific process. By the sequential steps, ALD offers self-limiting reaction with precision of monolayer coverage. Other high vacuum chemical vapor depositions (CVD) do not offer control at the Angstrom level. Consequently, ALD facilitates uniform coverage over large areas and conformal deposition of non-planar structures with high aspect ratio. ALD is also compatible with integration to transistors production processes. It is typically conducted at modest temperature (<400 °C). ALD is also an excellent tool for exploring new high-k compounds by straightforwardly controlling material composition during alternate cycle of growth.

These advantages led to the semiconductor industry's interest in ALD in the mid-1990s for deposition of high-k materials on Si[1, 91]. Intel introduced ALD high-k gate dielectric into their production line in 2007[92]. It was the key to advance the scaling to 45 node technology. Furthermore, for tri-gate design of Fin field effect transistor (FinFET) at 22 nm node, the deposition of gate oxide is possible by the conformal capability of ALD. Further development of other designs such as semiconductor wires, tubes, or sheets can also be enable[93].

The ALD growth rate is determined by thickness per cycle instead of a flux-dependent deposition. The typical growth rate (growth per cycle, GPC) range is between 0.05 - 0.1 nm per cycle. Multiple ALD processes can be combined to create "super cycles", where compositions of different films are stacked on to one another

such as $HfZrO_2$, zinc tin oxide (ZTO), and $SrTiO_3$. In addition, the purge step is critical for avoiding CVD-like or physical vapor deposition (PVD)-like reactions. These reactions can appear when both precursor and reactant are present in the chamber at the same time. In addition, a pump step can be added to ensure that no residual remains in the reactor. During the initial cycles of ALD, the GPC normally varies from the saturated value due to the reactive sites on the substrate differing from the deposited film and surface reconstructions. The initial cycles sometimes create island-growth or a rough surface, which is detrimental for scaling down of the oxides. Therefore, the initial steps are important for achieving stable dielectric morphology.

1.5 Outline of this dissertation

In the introduction, III-V complementary metal-oxide-semiconductor (CMOS) was introduced for replacement of Si-based MOSFETs. The motivation, based on intrinsic electronic properties are mentioned. On the other hand, the challenges for III-V semiconductors are significant, due to their large number of interface trap densities (D_{it}). Various important surface cleaning techniques have been studied to address these issues including both wet and dry processes. Plasma surface passivation technique by ALD is the focus of this dissertation. In Chapter 2, the standard MOS capacitor fabrication process used mainly in this dissertation is explained in detail for $In_{0.53}Ga_{0.47}As$ substrate. The importance of ALD plasma surface cleaning steps for III-V semiconductors and thermal oxide ALD processes are discussed. The properties for different precursors used for surface cleaning and oxide deposition are introduced. In addition, analysis for electrical properties of MOSCAPs are explained, including frequency dependent capacitance-voltage curves as well as conductance and Terman methods for D_{it} extraction in III-V semiconductors. Furthermore, x-ray photoelectron spectroscopy (XPS) is mentioned for analyzing high-k on III-V semiconductors. Effects of annealing and gate metal deposition methods are then discussed with regards to III-V surfaces. In Chapter 3, experimental results on the influence of different wet cleaning and *in-situ* ALD nitrogen plasma on surface and interface layers are shown. The improvement from the process are reported and the scientific insights on the interface layer are discussed. The exceptional MOSFETs characteristics from the novel *in-situ* ALD surface cleaning technique are also shown. Chapter 4 discusses further scaling of equivalent oxide thickness by scaling high-k-oxides and the interfacial layer, including Al_2O_3, HfO_2, ZrO_2, and TiO_2. These gate stacks present exceptional low midgap D_{it} and record-high capacitance densities. The gate stacks with TiO_2 in-

terfacial layer demonstrate remarkably low frequency dispersion in accumulation. In Chapter 5, n- and p-type $In_{0.53}Ga_{0.47}As$ MOSCAPs results are compared and analyzed by frequency dependent capacitance-voltage curves and Terman methods. Chapter 6 summarizes this dissertation and proposes some future work for further development and understanding of high-k on III-V interfaces.

Chapter 2

Experimental Details

2.1 Standard MOSCAPs Procedures

The experiments in this study were carried out on 300-nm-thick, n-type or p-type $In_{0.53}Ga_{0.47}As$ (Si or Be: 1×10^{17} cm^{-3}) commercially grown by molecular beam epitaxy on (001) n^+- or p^+- InP substrates (S or Zn: 3×10^{18} cm^{-3}). Samples were cleaned in 10:1 deionized H_2O:HCl for 2 min or buffered HF for 3 min. They were then rinsed in deionized H_2O to remove the acid. The samples were immediately loaded into the ALD reactor (Oxford Instruments FlexAL ALD) with a Si witness piece for growth rate measurement by ellipsometer (Woolam M2000DI Variable Angle Spectroscopic Ellipsometer) after deposition. The samples were set at the deposition temperature for 3 min in order to ensure that the substrate reached thermal equilibrium. Most experiments were carried out at 300 °C. The sample surfaces were exposed to an optimum number of alternating cycles of plasma (hydrogen, nitrogen or oxygen) and metal organics precursors (TMA or TDMAT). Each cycle consisted of an inductively coupled plasma pulse and a dose of precursor. Some recipes included a subsequent Ar purge and pump step, a dose of precursor, and another Ar purge

and pump step. The chamber reactor pressure was 200 mTorr.

Gate dielectrics were deposited by using a metal organic precursor (trimethylaluminium [TMA], tetrakis(ethylmethylamino)hafnium [TEMAH], or tetrakis (ethylmethylamino)zirconium [TEMAZr]) and water. Dielectric thicknesses were determined *ex-situ* using variable angle spectroscopic ellipsometry on the witness Si piece. After dielectric deposition, 500-nm SiO_2 was deposited on the backside of the samples at a high deposition rate at 50 °C by plasma-enhanced chemical vapor deposition (Unaxis VLR). The SiO_2 layer is used as a protection layer for InP during the high temperature annealing step. Low temperature deposition was selected to minimize effects on the samples. The samples were then annealed in a quartz tube furnace set at 400 °C for 15 min in forming gas (95% of N_2 and 5% of H_2). The ramping rate was set to 10 °C/min to avoid thermal expansion of the samples. The samples were also cooled down in the same annealing gas environment. Then, they were removed from the annealing furnace when the temperature cooled down to below 100 °C. More details of annealing procedure is explained in Appendix A.

For MOSCAP metal deposition, 80-nm-thick Ni gate electrodes were deposited through a shadow mask by thermal evaporation. The sizes of the circular devices in the shadow mask were 250, 200, 150, and 100 μm in diameter. Photoresist was then spin-coated on the topside of the samples for protection during backside SiO_2 removal. The SiO_2 was removed by dipping the samples in a strong buffered HF etchant for 3 min. After the photoresist was removed, the samples were transferred into a thermal evaporator for 20-nm Cr/100-nm Au backside deposition. Capacitance-voltage and conductance-voltage measurements were performed using an impedance analyzer (4294A Precision Impedance Analyzer) at room temperature and at frequencies between 100 Hz and 1 MHz in the dark. The oscillation level of the source was set to 50 mV with measurement range of 1 mA. The sweep delay time was normally set

to 3 s. The diameter of the Ni gate metal was measured by an optical microscope to obtain the device area. Typical diameters of the devices from the shadow mask used in the study were 150 and 100 μm. Conductance and Terman methods were used to estimate the D_{it} and its distribution in the band gap. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) was carried out using a 300 kV field-emission transmission electron microscope (FEI Titan) by Jack Zhang. X-ray photoelectron spectroscopy (Kratos Axis Ultra XPS) was used to investigate the interface and secondary ion mass spectrometry (Physical Electronics 6650 Dynamic SIMS) was used to investigate the interfacial composition.

2.2 ALD for *in-situ* Plasma Surface Cleaning and High-k Oxide Deposition

2.2.1 Important criteria for optimizing plasma conditions

Optimized plasma conditions for a specific substrate are essential for achieving high-quality high-k-III-V interfaces. Many factors are important for acquiring good physical and chemical properties. Parameters include the order of the chemical exposure of the substrate, step time, plasma power, plasma time, purge and pump steps, etc. Plasma power and plasma time are the key parameters for plasma process. Different substrate materials and precursor types require certain conditions. For example, it was found that with the same total plasma time, oxygen plasma is more damaging compare to hydrogen and nitrogen plasma for $In_{0.53}Ga_{0.47}As$. The number of total cycles and the total time of plasma exposure have to be optimized together to achieve the best conditions for a certain surface. If the plasma exposure is too high, damage occurs to the semiconductors[75].

It is also necessary to control the environment of the plasma chamber. No contamination from other precursors should be present. The presence of other precursors can cause the plasma conditions to change or hinder the spark. Contamination is avoided by closing the valve between the deposition chamber and the plasma chamber when the plasma is not in use. Furthermore, the plasma can be reluctant to strike, which can be checked by running a warm-up process before the real deposition to ensure the reactiveness of the system. In addition, for low temperature deposition with plasma, flaking can occur due to residue on the isolation valve. It is suggested that before plasma process, opening and closing the isolation value for number of cycles can shake off the flakes. Thus, the *in-situ* plasma process requires attentions to details both

before and during the experiment.

2.2.2 Thermal Oxide ALD

The most common thermal ALD high-k oxides are binary compounds such as Al_2O_3, TiO_2, HfO_2, Ta_2O_5, and ZrO_2[94]. During the deposition, when a precise saturating dose of the metal precursor or reactants is used, a stepwise deposition is observed. Dosing less than saturation results in incomplete coverage of the surface and roughness. The surface roughness can prevent thickness scaling because a thicker film is required to form a complete layer. A complete coverage of semiconductor surface is essential. A saturated dose time can be found when the growth per cycle curve is constant with increasing dose time. Typical ALD growth rate is about 0.1 nm/cycle. On the other hand, over-dosing can create residual precursor around the deposition line and chamber. Excessive residues need to be purged (Ar or N_2 gas) and pumped out of the reactor before the next dose of precursor or reactant arrives to avoid reactions before reaching the substrate. However, too long purge and/or pump step will significantly increase the overall deposition time. Therefore, the time for all steps has to be optimized for every precursor and reactant.

2.2.3 Metal Organic Precursors

Trimethylaluminum (TMA) is one of the most well known ALD precursors, and is commonly used for deposition of Al_2O_3. It is an ideal metalorganic precursor due to its direct bonding between the metal ion and carbon, which provides self-terminating reactions on the substrate. It is highly volatile and very reactive. Water is the most commonly use as an oxygen source in the ALD. TMA decomposes at temperatures above 300 °C. The GPC in TMA/H_2O process at 300 °C is about 0.09

nm, corresponding to about 30% of a monolayer of Al_2O_3[95]. Many properties of Al_2O_3 make it desirable as a high-k gate dielectric. It has dielectric constant $\sim$ 8-10, compared to 3.9 for SiO_2. Al_2O_3 has a wide bandgap ($\sim$ 9 eV), providing high potential barrier with the III-V semiconductor, which results in reduced gate leakage current. It has high breakdown field of 5-30 MV/cm[9], high thermal stability, and usually remains amorphous during ALD process conditions. TMA is also reported to have a self-cleaning effect on the III-V surfaces, which help create high quality oxide/semiconductor interface.

Tetrakis[ethylmethylamino]hafnium (TEMAH) [$Hf(NCH_3C_2H_5)_4$] is used for deposition of high-k HfO_2, and can be used with the most common reactants including H_2O, O_2, and O_3. TEMAH has high vapor pressure that allows reasonable deposition rate at relatively low deposition temperatures. It reacts immediately upon contact with the reactants. HfO_2 has been reported to grow on OH- and H- terminated surfaces using this precursor, which is convenient for subsequent cycle in ALD. In the standard ALD setting, TEMAH requires a carrier gas bubbling through the canister at 70 °C to the deposition chamber. This TEMAH precursor can be used for depositing HfO_2 at relatively low temperature because of the metal amides group. Compared to metal halides, the metal amides should be more reactive toward hydroxylated surface. Metal-nitrogen bond is weaker than metal halide bond, which facilitates the removal of the residuals during ALD process[96].

Thermal ALD HfO_2 have been developed by using TEMAH as a precursor and H_2O as a reactant[96, 97]. However, one of the main concern for using H_2O as a reactant for TEMAH is that H_2O requires long purge time because of its sticking coefficient to surfaces. H_2O is prone to physisorb onto surface, including samples and chamber. It is necessary to have a sufficiently long purge time to remove excess H_2O from the reactor, especially at low temperature. A study of purge time needs

to be completed to confirm the saturation on the HfO_2 growth rate. If the purge time is not sufficient, TEMAH ligands can react with the excess water and chemisorb onto surface sites. This is called parasitic growth, which can lower reactive sites and non-uniformly affect the growth rate of the HfO_2. Higher growth per cycle can be presented due the excessive residues. The scaling of high-k thickness become hard to control, which will affect the electrical properties of the film. This includes capacitance density and leakage issues from the contaminated film (leakage path). In addition, it has been shown that too long H_2O pulse can induce dehydroxylation of the surface, which lowers the HfO_2 growth rate[98]. Another concern is its limited thermal stability. TEMAH starts to decompose at 140 °C, which give rise to the increase of C impurities in the deposited film. As mentioned earlier, this can increase leakage throughout the gate stack. Thus, the ALD line temperature need to be controlled. In our experiment, ALD precursor line temperatures are set to 120 °C to avoid the decomposition of TEMAH.

Tetrakis[ethylmethylamino]zirconium (TEMAZr) is a metal organic precursor that is almost identical to TEMAH except it is used for deposition of high-k ZrO_2. The same reactants can be used, which in this case is water. It also requires carrier gas bubbling through the canister. Therefore, the deposition mechanism for HfO_2 and ZrO_2 is almost identical. The proposed mechanism is shown in Figure 2.1. The first step of the reaction is the metal precursor dose, which is a chemical absorption of the metal-amide onto the OH- terminated surface. The metal-nitrogen bonds break apart, then metal-oxygen bonds are formed. Consequently, the metal ligands byproduct is purged out. In the second step, water reacts with the surface-bound metal amides to create fully oxidized metal-oxides bonds and regenerate surface hydroxyl group for the subsequent metal precursor dose step. The byproducts of dialkylamines are also purged out at the end of this step.

Table 2.1: Average Dielectric Constant for Three Crystalline Phases of ZrO_2 and HfO_2[101]

Phase	ZrO_2	Experimental value	HfO_2	Experimental value
Cubic	37	(35-50)[102]	29	
Tetragonal	47	(35-50)[102]	70	
Monoclinic	20		16	(16-45)[99, 103]

Properties of HfO_2 and ZrO_2 are very similar. They have relatively wide band gap (5-7 eV). Their thermal stability is high ($\sim$900-950 °C)[99]. Table 2.1 compares dielectric constant of ZrO_2 and HfO_2 from different crystalline phases. The diectric constant depends on crystal phase. ZrO_2 gives higher permittivity than HfO_2 due to the presence of cubic and tetragonal phase. These phases have a higher dielectric constant than monoclinic phase in HfO_2 because of the smaller unit cell parameters[100]. Thus, ZrO_2 is a promissing alternative for high-k oxides. HfO_2 and ZrO_2 normally show microcrystalline structure. Their average dielectric constant is $\sim$17-18 and $\sim$22-23[101], respectively.

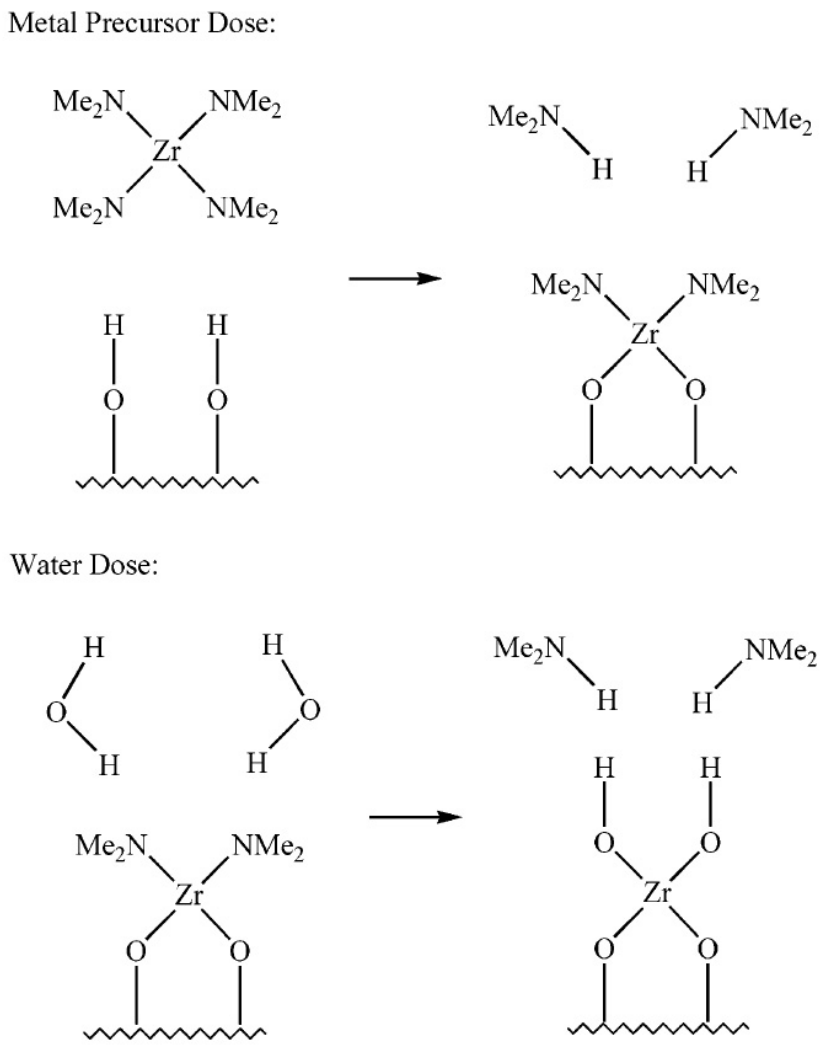

Figure 2.1: Schematic of propose mechanism for deposition of ZrO_2. Reprinted with permission from [96]. Copyright © 2002 American Chemical Society

Tetrakis(dimethylamido)titanium(TDMAT) is normally used for the deposition of TiN by chemical vapor deposition, but it can be used in both thermal and plasma ALD. It can also be use for deposition of TiO_2 as an alternative of titanium tetrachloride ($TiCl_4$) due to its non-corrosive property and low temperature deposition ($<$ 400 °C). Since the vapor pressure of TDMAT is relatively high when slightly heated, there is no need of bubbler during the dosing step in the ALD. However, for a better conformality, a hold step is usually added to after the dosing step to allow more transport time without increasing the dose material.

Among all binary oxides, TiO_2 has the highest dielectric constant[104]. The dielectric constant in rutile phase can be as high as 170 [105]. It is thermally stable on III-V semiconductors and can form an abrupt interface[106]. It is reported that lower capacitance-voltage hysteresis is observed in a TiO_2 gate stack on GaAs[107]. The band gap is $\sim$3.2 eV [105]. The valence band offset between TiO_2 and $In_{0.53}Ga_{0.47}As$ is 2.5 eV. However, there is almost no conduction band offset (0.05 eV) as shown in Figure 2.2 [106]. This property is expected to cause high leakage current for n-$In_{0.53}Ga_{0.47}As$ device. However, it was shown that effect of dipole at the interface can compensate and change the effective band offset to achieve low leakage current[108]. Ti has a high oxygen solubility[109], which can impede the formation of III-V native oxides on the surface and remove low-k interface layer. In addition, experiments suggest that Ti incorporation acts as a barrier to As out-diffusion and inhibit the formation of GaO[110]. Thus, TDMAT can be used as an effective precursor to provide high quality interface between oxide and III-V semiconductors.

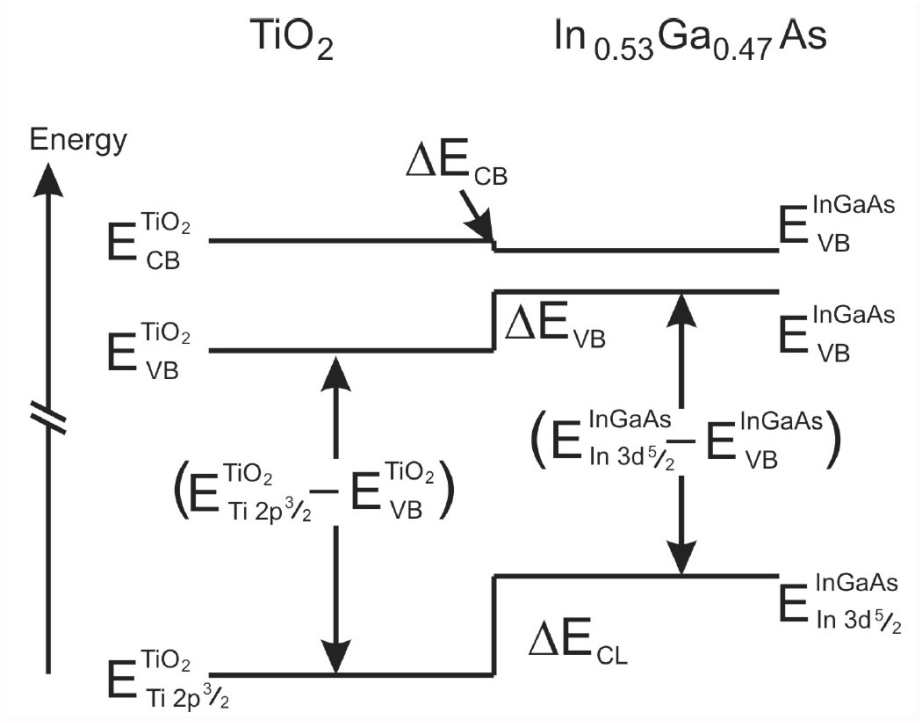

Figure 2.2: Schematic band diagram of $TiO_2/In_{0.53}Ga_{0.47}As$ interface. Reprinted with permission from [106]. Copyright © Materials Research Society 2009

2.3 Capacitance-Voltage Dispersion

The midgap D_{it} response can be qualitatively determined from the frequency dispersion behavior in the negative bias region of the capacitance-voltage (CV) curves. The D_{it} extraction from CV of n-type $In_{0.53}Ga_{0.47}As$ MOSCAPs can be done at room temperature, due to its small bandgap[111, 112]. For small bandgap semiconductors, the weak inversion response will show an admittance contribution due to interface traps in the minority carrier half of the bandgap. At different measurement frequencies (1 kHz - 1 MHz), the frequency dispersion in the depletion region of the CV curves results from exchange of carriers between traps and both majority and minority carrier bands. When the frequency dispersion is large, it indicates that the D_{it} response is high. Measurements over a temperature range are needed to extract D_{it} across the bandgap. The minimal temperature range for different semiconductor materials for extracting midgap D_{it} is shown in Figure 2.3. For $In_{0.53}Ga_{0.47}As$, room temperature measurement can be used to determine the D_{it} near midgap. Temperature below 300 K is required to extract D_{it} near the band edges.

Frequency dispersion behavior in accumulation appears as a decrease in the maximum capacitance as the frequency increase. This behavior is caused by defect states[113, 25] and appears most severely when the dielectric is highly scaled[114]. Some explanations associate this behavior to border traps, which are defects in the oxide[115, 116]. However, other experiments suggested that the frequency dispersion is drastically changed by the change in the interface layer and does not depend on the specific oxide[117, 118]. Defects are believed to be located within 0.8 nm of the interface. Other observations suggested that semiconductor defects such as disruption of the III-V atomic bonding cause the frequency dispersion in accumulation[119]. Interface traps may tunnel throught the thin dielectric to metal[120] and give rise

to frequency dispersion in accumulation, specifically those in the lower half of the $In_{0.53}Ga_{0.47}As$ band gap[114].

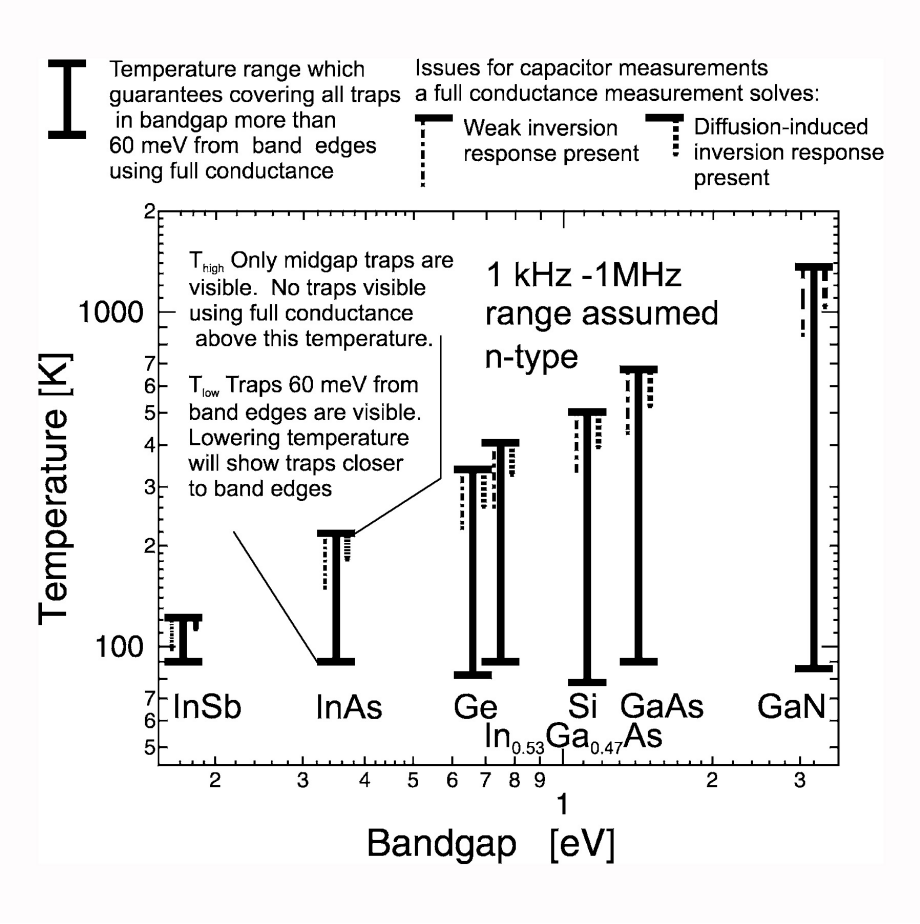

Figure 2.3: Temperature range of different semiconductors needed for extracting D_{it} across the band gap. Reprinted with permission from [111]. © 2008 IEEE

2.4 Interface Trap Densities (D_{it}) Extraction

High trap densities (D_{it}) at the interface between gate dielectrics and the III-V channel cause inefficient Fermi level response or even Fermi level pinning. These behaviors inhibit control over charge carriers in the MOSFETs channel, causing bad subthreshold slopes (SS) and low drive currents. In very-large-scale integration (VLSI) for MOSFETs applications, D_{it} must be sufficiently small in order avoid degradation of the SS. In Si MOSFETs, the SS is below 100 mV/decade. The SS of a planar long channel inversion mode MOSFET is given by:

$$SS = ln(10)\frac{k_B T}{q}\left(\frac{C_{ox} + C_{dep} + q^2 D_{it}}{C_{ox}}\right) \tag{2.1}$$

where k_B is Boltzmann's constant, T is the temperature, q is the elementary charge, and C_{dep} is the semiconductor depletion capacitance. For quantum well accumulation mode III-V MOSFETs, C_{dep} is significantly less than C_{ox}. Therefore, D_{it} must be less than 10% of the oxide capacitance to avoid degrading the subthreshold swing by more than 10%. As a result, for the 1 nm EOT MOSFETs, D_{it} throughtout the semiconductor band gap cannot be greater than 2.2×10^{12} eV^{-1} cm^{-2}[78]. Reliable methods for quantifying D_{it} are extremely important for the development of high-quality high-k dielectrics/III-V semiconductors interfaces.

In III-V MOSFETs, device fabrication involves elaborated steps. Every step can negatively affect the device performance. Metal-oxide-semiconductors capacitors (MOSCAPs) are normally used for separately addressing the issues with high-k/III-V interface. Methods for analyzing D_{it} at the SiO_2/Si interface using MOSCAPs structures were developed in the 1960s[121]. The quantity measured in a MOSCAP is its admittance as a function of gate bias and frequency. However, compared to SiO_2/Si

interfaces, the interpretation of the admittance response in high-k/III-V systems is less straight forward. With their variation of band gaps, low conduction band density of states, and wide range minority carrier response times, the methods for D_{it} analysis have to be adjusted. In addition, the energy distribution of the D_{it} also varies. Normally, more than one method is required to compare and contrast the D_{it} values and distributions. In this dissertation, the conductance and Terman methods are mainly used.

2.4.1 Conductance Method

Measurement of the equivalent parallel conductance can be used to estimate interface trap densities because the conductance is directly related to energy loss provided by AC signal source during capture and emission of carriers by interface traps [121]. The equivalent parallel conductance, G_p, can be extracted by

$$G_p = \frac{\omega^2 {C_{ox}}^2 G_m}{{G_m}^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{2.2}$$

where ω is the angular frequency ($2\pi f$), C_{ox} is the gate oxide capacitance, G_m is the measured conductance, and C_m is the measured capacitance.

During the measurement, the occupancy of the interface traps changes as a function of AC signal, which reaches a maximum when the interface traps are at resonance with the applied AC signal ($\omega\tau = 1$). Consequently, the maximum normalized parallel conductance peak, $\left(\frac{G_p}{A\omega q}\right)_{max}$, where A is the device area and q is the elemental charge can be used to estimate D_{it} values[121],

$$D_{it} \approx 2.5 \left(\frac{G_p}{A\omega q}\right)_{max} \tag{2.3}$$

The estimated D_{it} values are reliable when $C_{ox} > qD_{it}$. When $C_{ox} < qD_{it}$, D_{it} is underestimated because the measured impedance is dominated by C_{ox}[122].

This method assumes a constant capture cross section on the semiconductor surface. Thus, for different semiconductor compounds, the constant capture cross section can vary because of different types of traps and energy levels inside the band gap[123]. The trap energy level can be refered to as the energy difference to the majority carrier band edge (ΔE), which can be estimated from its relationship to the frequency at $\left(\frac{G_p}{A\omega q}\right)_{max}$. The frequency dependence is related to the characteristic trap response time, $\tau = 2\pi/\omega$. It describes the time needed for a captured charge to be released by a trapping state at energy level E. The trap response time is given by the Shockley-Read-Hall statistics of capture and emission rates[124, 125],

$$\tau = \frac{exp(\Delta E/k_B T)}{\sigma \upsilon_{th} D_{dos}} \tag{2.4}$$

where σ is the capture cross section of the trap, υ_{th} the average thermal velocity of the carriers, D_{dos} the effective density of states of the majority carrier band, k_B the Boltzmann constant, and T the temperature. CV and conductance-voltage measurements have to be performed at different temperatures in order to extract the D_{it} across the $In_{0.53}Ga_{0.47}As$ bandgap.

With the $In_{0.53}Ga_{0.47}As$ parameters taken from ref.[126] and the assumed capture cross section σ of 1×10^{-16} cm^2, the characteristic trap frequency can be calculated from equation 2.4 for different temperatures as a function of energy difference between the majority carrier band. This is shown in Figure 2.4. The frequency range is 100 Hz to 1 MHz. The data for σ of $In_{0.53}Ga_{0.47}As$ is assumed due to the lack of measurement reports. The reported values are in 7×10^{-15} to 5×10^{-17} cm^2 range[122]. It is noted that errors can appear, but they are expected to be small. Errors arise in

low temperature measurements since the D_{it} response is not as pronounced as those at higher temperature. Consequently, the D_{it} values close to the band edges are less reliable compared to those near midgap. The plot indicates that low temperature measurements are required to determine the D_{it} values close to the band edges. Room temperature measurement can only be used for extract the near midgap D_{it} values in this frequency range (< 1 MHz).

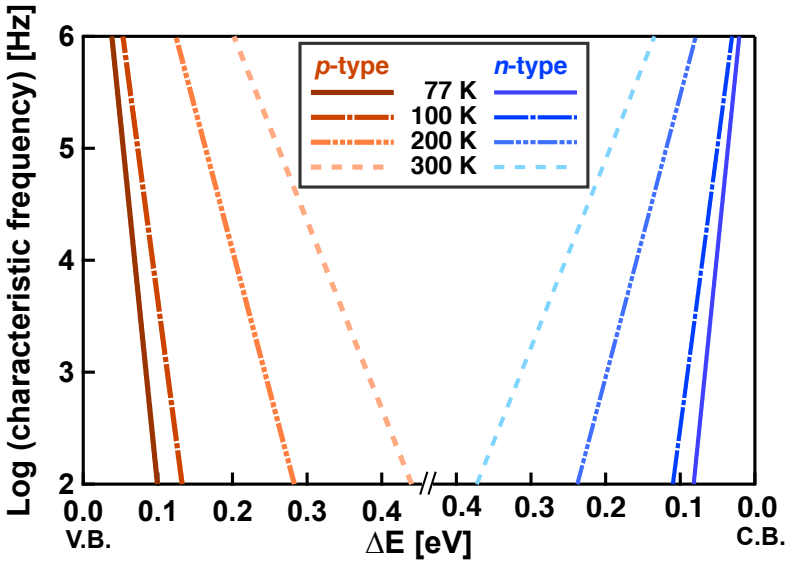

Figure 2.4: Characteristic trap frequency of $In_{0.53}Ga_{0.47}As$ as a function of energy difference between the majority carrier band and the trap energy level

In addition, C_{ox} is an important variable for conductance method. It cannot be estimated from accumulation capacitance as in Si due to the low conduction band density of states in III-V semiconductors materials. Calculating C_{ox} can also be complicated when there is interfacial layer presented. Normally, C_{ox} is determined from,

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t} \tag{2.5}$$

where ε_0 vacuum permittivity (8.854×10^{-14} F/cm), ε_{ox} effective dielectric permittivity, and t oxide thickness. TEM thickness series can be used to determine ε_{ox}. The

correct C_{ox} is important for equation 2.2. If an overestimated C_{ox} value is used, G_p/ω and $\left(\frac{G_p}{A\omega q}\right)_{max}$ will be too low, causing D_{it} and band bending to be underestimated.

2.4.2 Terman Method

The Terman method is a high-frequency CV based technique used to estimate D_{it}. A high-frequency ideal CV curve is required for comparison of stretch-out in the experimental curve. For n-$In_{0.53}Ga_{0.47}As$, the ideal CV curve cannot be calculated classically like Si because the Fermi level moves deep into the conduction band. Nonparabolicity of the lowest conduction band valley (Γ) and higher lying conduction band valleys, X and L, also need to be taken into account. A detailed study to calculated ideal CV curves is shown in refs.[122, 127]. The correct semiconductor parameters are needed for the simulation of the ideal CV curve, especially band parameters and doping concentration of the semiconductor. Using incorrect doping concentration can drastically change the D_{it} distribution. For $In_{0.53}Ga_{0.47}As$, the valence band has a larger density of states. Thus, the parabolic band approximation by a Boltzmann distribution function is sufficient. The high-frequency CV curve needs to be measured at sufficiently high frequency to avoid the ac contribution from the interface traps. The basic assumption is that the only contribution of D_{it} is in the stretch-out with gate bias. The stretch-out $\left(\frac{d\psi_s}{dV_g}\right)$, where ψ_s the semiconductor band bending and V_g the applied gate bias, is obtained from comparison with the ideal CV curve and yields for quantification of the D_{it}[128],

$$D_{it}(\psi_s) = \frac{C_{ox}}{q}\left[\left(\frac{d\psi_s}{dV_g}\right)^{-1} - 1\right] - C_{dos}(\psi_s). \tag{2.6}$$

During the comparison step, the best possible match is made between the measured high-frequency CV curve and the ideal CV curve. The correct C_{ox} is also

required for this process to avoid error in D_{it} extraction. Flatband voltage shift and an estimated D_{it} value are used for the estimation of the stretch-out. The accumulation capacitance and depletion capacitance should match as much as possible to achieve a close estimation of D_{it} distribution. When the measured depletion capacitance does not reach the ideal minimum capacitance (slope of CV curve is zero), it is an indication of a pinned Fermi level (the semiconductor is never fully depleted). Since the D_{it} distribution is extracted from the slope of the CV curve, the Terman method is not applicable anymore. Band bending can be extracted as a function of gate bias to see how efficient the Fermi level moves. It is expected for the experimental band bending to reach below -0.4 eV to indicate unpinned Fermi level for $In_{0.53}Ga_{0.47}As$.

In summary, it is noted that the D_{it} extraction is reliable in the middle of the band gap range by conductance method when $C_{ox} > qD_{it}$[122, 129], but a complete theoretical description of the CV of high-k/III-V interfaces is still lacking. Terman method can cause error when other traps states instead of interface traps are presented. Particularly, the contribution of D_{it} to the capacitance in accumulation (C_{acc}) appears to be non-negligible even at 1 MHz[129], due to the fast response of traps near or in the conduction band, as described by

$$\frac{1}{C_{acc}} = \frac{1}{C_{ox}} + \frac{1}{C_{D_{it}} + C_S}, \tag{2.7}$$

where C_S and $C_{D_{it}}$ are the semiconductor and interface state capacitances, respectively. When C_{ox} is high, the contribution to C_{acc} from $C_{D_{it}}$ becomes more significant. In addition, it is believed that the D_{it} in the conduction band can be high[22]. This precludes determination of the D_{it} from CV-based methods, which assumes that the only contribution of D_{it} to the high-frequency CV is a stretch-out. Thus, with care-

ful consideration, these two techniques should be used separately to quantitatively determine the D_{it} distribution.

2.5 X-ray Photoelectron Spectroscopy (XPS)

XPS is a chemical analysis technique that utilizes electron spectroscopy to identify chemical species on the surface of a samples. An x-ray beam radiates at an angle onto the sample surface. The kinetic energy and number of electrons emitted are measured simultaneously from within the top ∼10 nm of the samples surface, which is generally called XPS spectra. The analysis depth varies with material depending on the electron escape depth. With the known energy of x-ray, XPS spectra is used for determining the binding energy of electrons. The atomic concentration of an element can be calculated from the number of measured electrons, which is represented by core level peak. After accounting for differences in the relative sensitivity factors and measured area of the characteristic core level peaks, a ratio of chemical species (film stoichiometry) on the surface can be revealed. In addition, specimens can be tilted to provide a shallower analysis and depth profiling. The system is also equipped with an Ar ion gun for cleaning surface contamination. For our experiments, scans were run using monochromatic Al Kα radiation. This technique can be used for III-V semiconductors surface analysis of oxides, which are presented in various bonding configurations.

In the data analysis, surface aliphatic hydrocarbon peak (C 1s) is set to 285.0 eV and used for determining the chemical shift and calibrating binding energy. Since our samples are non-conductive, charge compensation has to be applied during the measurement. For this reason, samples are placed on a glass slide before mounting onto the standard wafer sample holder to make the sample insulate evenly. The detection limit of the XPS is normally about one part per thousand. However, some other factors can prevent the detection of some smaller concentration materials. Carbon contamination on the surface of the sample is one of the issue. Ar etch can be run to

decrease the carbon contaminant to about a quarter of its original peak intensity. In the analysis, the peaks do not usually correspond to the binding energy position suggested by a software because the fitting data are from metal states. If there is more than one kind of materials to fit a peak, additional database is needed to confirm on the likeliness of the state of material.

In our studies, N is difficult to detect because of the Ga Auger signal interfere with N 1s peak. Other strong peaks are also overlap, in this case between $In_{0.53}Ga_{0.47}As$ substrate and HfO_2. As 3d and Hf $5p^{1/2}$ peaks overlap at around 40 eV binding energy as shown in Figure 2.5. The presence of the Hf $5p^{1/2}$ peak is not straight-forward to add to the As 3d peak fitting. Errors can occur by fitting arsenic oxides peaks to this peak area. However, the oxide components should appear at higher binding energy than metal-metal components, in this case InAs and GaAs. Therefore, fitting the As-oxide component at lower energy than As $3d^{5/2}$ is inaccurate. In this case, by looking further to lower energy, we know that there is Hf 5p peak with $\Delta_{Hf\ 5p}$ of 7.2 eV, which send Hf $5p^{1/2}$ signal overlapping onto As 3d peak. Thus, it can be concluded that no As-oxide component is present in this sample.

Other peak overlapping issues also appear in the Ti components analysis on $In_{0.53}Ga_{0.47}As$. The As Auger and In loss signals overlap with Ti $2p$ peaks. These overlapping peaks deviate the background in the range of Ti $2p$ peaks from the standard models. A signal from the $In_{0.53}Ga_{0.47}As$ substrate with similar high-k-oxide thickness, but without Ti is needed for background subtraction of these low-intensity overlapping peaks. If no subtraction is made, the analysis will overestimate the amount of Ti and inaccurately determine the types of Ti components in the film. In this case, the signal of an $In_{0.53}Ga_{0.47}As$ substrate sample with $\sim$1 nm, post-annealed Al_2O_3 film was used for the background subtraction.

As a result of the low film thickness required for typical XPS analysis, the oxi-

dation from atmospheric condition can induce discrepancies in the *ex-situ* analysis. Some studies use a cluster tool with deposition and analysis techniques to avoid the issues with the oxidation. On the other hand, considerable caution can be carried out to draw conclusions between correlations of physical characterization results and those obtain electronically. The analysis from *in-situ* studies might argue for a better understanding of the film interface during and after the oxide growth. On the other hand, *ex-situ* studies after device fabrication can provide a direct analysis to the measured MOSCAP devices. For the studies in this dissertation, post-annealed high-k gate stacks were used for interface chemistry analysis in the same condition as the samples used for electrical measurements.

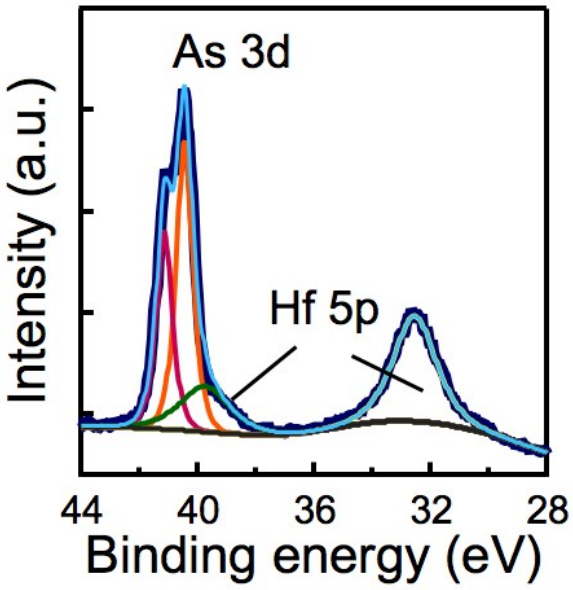

Figure 2.5: XPS spectra of 1.5-nm-thick HfO_2 with nitrogen plasma+TMA pre-deposition treatment. Thin lines are fitted peaks. Reprinted with permission from [130]. © 2013 AIP Publishing LLC.

2.6 Annealing Conditions

Annealing may reduce defects. Before oxide deposition, vacuum pre-annealing in ALD chamber has been reported to reduce the native oxides of GaAs surface[131]. Furthermore, post-oxide deposition anneal has been used widely. The main parameter for annealing is the temperature. It has to be below the III-V decomposition temperature, but sufficiently high to be effective. The high temperature is for removing excess oxygen and water. The temperature should be higher than the oxide deposition temperature in order to densify the oxide. The high temperature anneal, especially in hydrogen environment, is normally used for passivating electronically-active defects in the oxide/III-V interface, reducing midgap D_{it}[132, 133, 134]. It was also found that hydrogen can effectively remove carbon-related carrier traps and passivates negative fixed charge in the Al_2O_3[135]. In addition, post metal deposition annealing is shown to reduce damages from the metal deposition in the high-k oxide/$In_{0.53}Ga_{0.47}As$ gate stack[136]. Other annealing conditions have to be considered. The ramping rate to the annealing temperature should be low ($\sim$10 °C/min) to avoid issues with thermal expansion of the substrate and oxides. Duration of the anneal is also important. Annealing experiment for optimizing annealing time is required. Longer anneal does not necessarily benefit the gate stack quality than the shorter anneal.

2.7 Effects of Gate Metals Deposition

A few studies have looked into the effect of device processing after high-k oxide deposition. For example, in terms of metal deposition techniques, e-beam evaporation causes more damage comparing to thermal evaporation. The damage was found in the III-V quantum well layers as deep as 50 nm below the surface. It is shown by smaller quantity of the photoluminescense spectra of the e-beam evaporation comparing to the spectra from the thermal evaporation in Figure 2.6. The metalization damage was found to depend on deposition method, deposition rates, and different metal sources[137].

Another report shows the same conclusion as the study on the quantum well layers. The capacitance-voltage characteristics of HfO_2 dielectrics on n-$In_{0.53}Ga_{0.47}As$ MOSCAPs are shown in Figure 2.7. The frequency dispersion in negative bias range of the sample with Pt electrode deposited by e-beam evaporation in Figure 2.7 (a) is more pronounced than the sample with Ni electrode deposited by thermal evaporation in Figure 2.7 (b), indicating higher midgap D_{it} response. The damage from the e-beam evaporation is efficiently removed by annealing in forming gas as shown in Figure 2.7 (c) where the frequency dispersion in negative bias region decreases significantly. The e-beam evaporation can strongly degrade the device performance as shown by large frequency dispersion in negative bias region, representing large midgap D_{it} response. On the other hand thermal evaporation does not induce much damage, and thus, the post metal-deposition annealing is not needed.

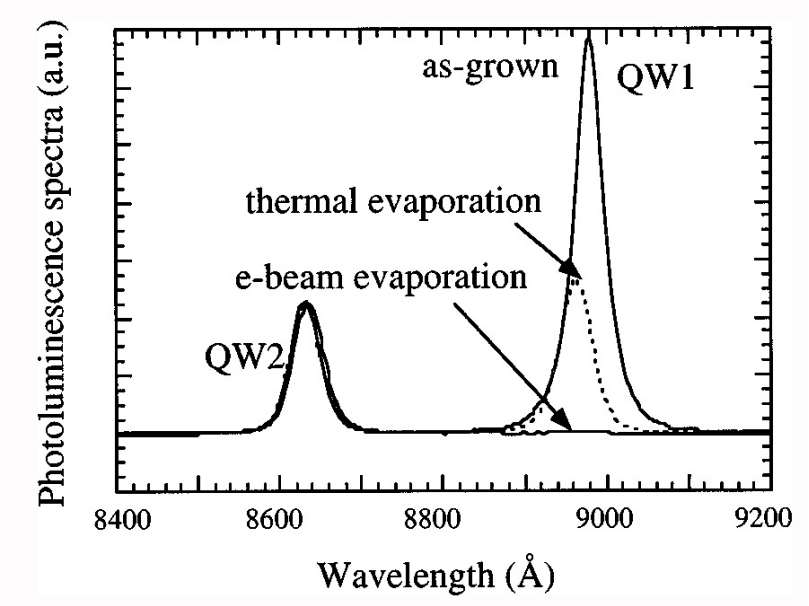

Figure 2.6: Photoluminescence spectra of 10 nm of Au deposited on InGaAs/GaAs quantum well samples with thermal evaporation of e-beam evaporation at 0.2 nm/s deposition rate. Reprinted with permission from ref. [137]. © 1998 AIP Publishing LLC.

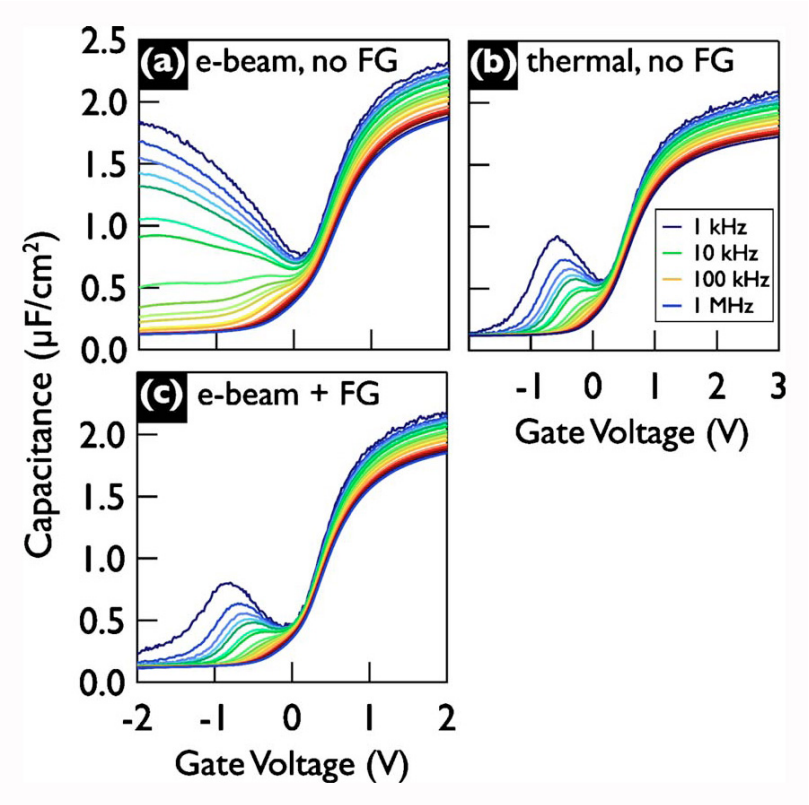

Figure 2.7: Capacitance-voltage curves of HfO_2 dielectrics on n-$In_{0.53}Ga_{0.47}As$ MOSCAPs measured as a function of frequency at room temperature with (a) e-beam deposited Pt electrode, (b) thermal evaporated Ni electrode, and (c) same sample in (a) after forming gas annealing at 400 °C. Reprinted with permission from ref. [136]. © 2011 AIP Publishing LLC.

For the results mentioned, they also suggest that the very large midgap D_{it} is to some extent the effect from damage by device processing. Thus, it is best to avoid additional damages from the metal deposition. The effect of the damage on the III-V structure is significant. The details of the fabrication have to be considered when processing the devices.

In summary, the process for achieving high quality interface high-k/III-V semiconductors needs to be focused on optimizing the pre-oxide deposition cleaning. In terms of oxide deposition, many precursors can be selected for high capacitance density MOSCAPs. For this study, TMA, TEMAH, TEMAZ, and TDMAT are selected for deposition of Al_2O_3, HfO_2, ZrO_2, and TiO_2, respectively. In terms of characterization of trap state density, capacitance-voltage curves at different frequencies are used for qualitatively analyze the midgap D_{it} response. For quantitative measure of midgap D_{it}, conductance and Terman methods are utilized for comparing D_{it} values and distributions in the bandgap. For chemical analysis, XPS is used for studying the chemical components of the interfacial layer in order to determine the effectiveness of the pre-deposition plasma treatments. In addition, the importance of annealing and metal deposition conditions are emphasized.

Chapter 3

Pre-oxide Deposition Treatment Techniques

3.1 Effects of Different Wet-Cleaning Chemicals

Wet-cleaning is a typical pre-oxide-deposition treatment step that has been widely used to remove native oxides from the III-V semiconductors. Specific conditions are required for different III-V channels. A study of four different wet chemical treatments on n-$In_{0.53}Ga_{0.47}As$ is shown in Figure 3.1. CV characteristics of ∼4 nm of $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs with 5 cycles of hydrogen+TMA plasma cleaning after pre-deposition wet-clean of 10 % HCl for 2 min, BOE for 3 min, 29 % NH_4OH for 2 min, or 20 % HF for 3 min are shown in Figure 3.1(a)-(d), respectively. As a result, the sample cleaned with BOE for 3 min shows the smallest frequency dispersion in the negative bias region, indicating the lowest midgap D_{it} response. Further investigation

for chemical analysis by XPS of the interface was performed on the gate stacks with different wet pre-treatments. Figure 3.2(a)-(d) show XPS signals of Al 2p, As 3d, In 3d, and O 1s, respectively. There is only a slight shift in the O 1s signal, but no significant difference in intensity between the four different treatments within the resolution limit. However, the conclusion can be made from the CV characteristics that BOE cleaning results in the smallest midgap D_{it} response.

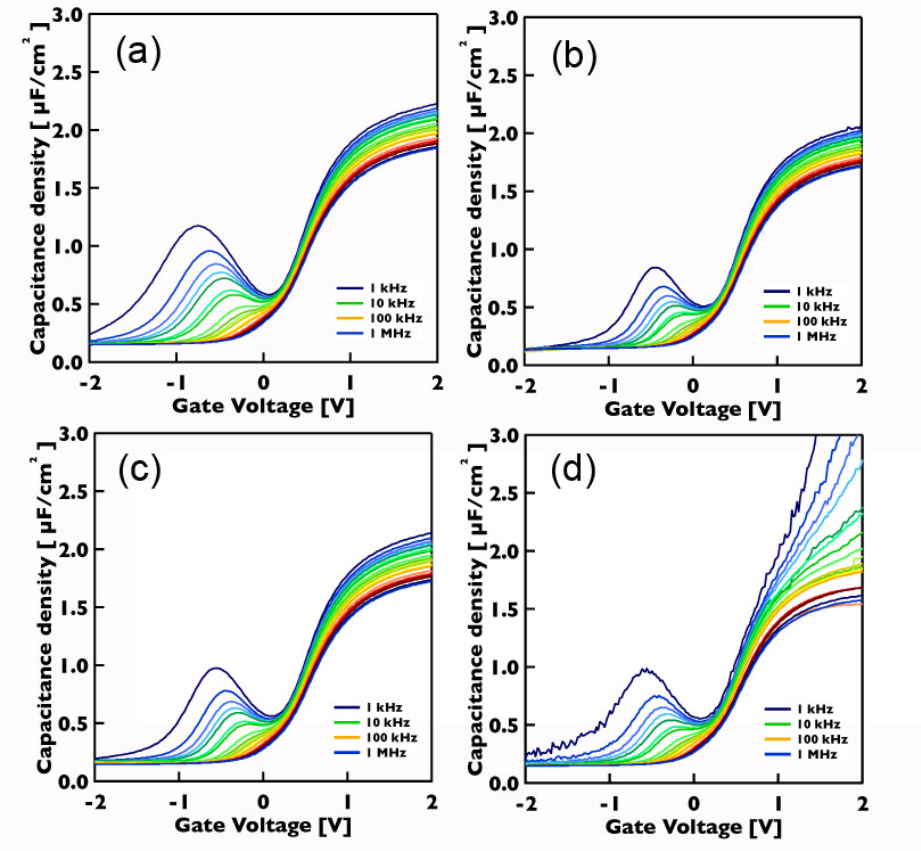

Figure 3.1: CV Characteristics as a function of frequencies of ∼3 nm of Al_2O_3/ $In_{0.53}Ga_{0.47}As$ MOSCAPs with cycles of hydrogen+TMA plasma cleaning after pre-deposition wet-clean of (a) 10 % HCl for 2 min; (b) BOE for 3 min; (c) 29 % NH_4OH for 2 min; and (d) 20 % HF for 3 min

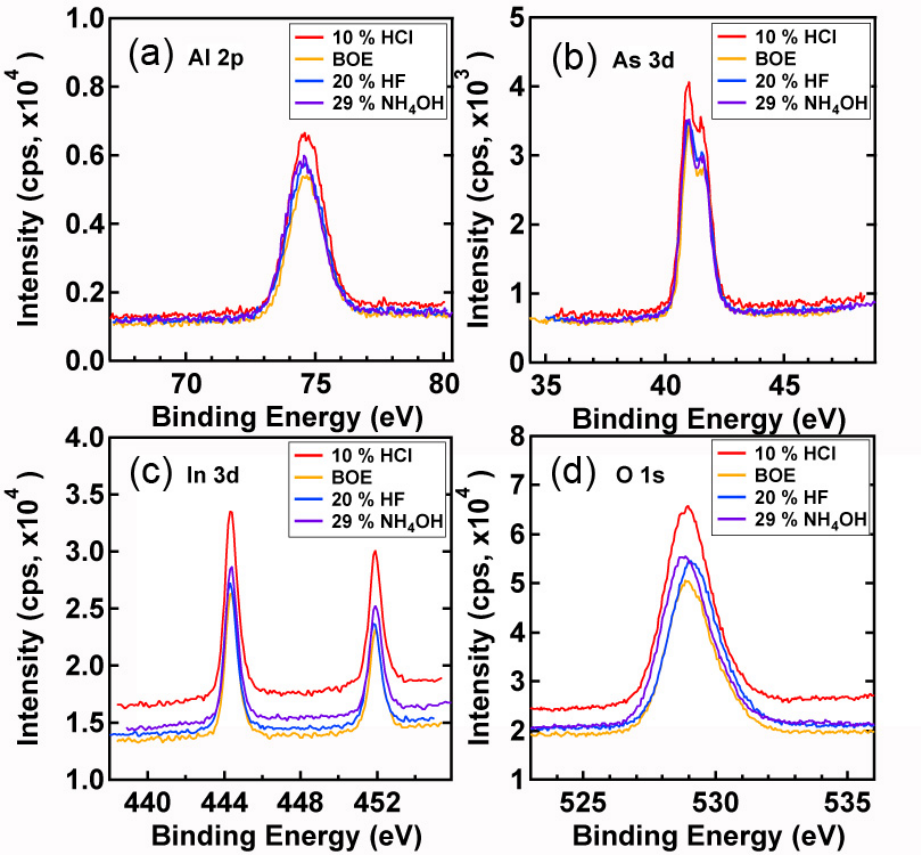

Figure 3.2: XPS signals of (a) Al 2p; (b) As 3d; (c) In 3d; and (d) O 1s from ∼4 nm of $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs with cycles of hydrogen+TMA plasma cleaning after pre-deposition wet-clean of 10 % HCl for 2 min, BOE for 3 min, 29 % NH_4OH for 2 min, or (d) 20 % HF for 3 min

3.2 Influence of Plasma

ALD *in-situ* pre-oxide deposition treatments with cycles of hydrogen or nitrogen plasma and TMA have been reported [78, 85]. It is shown that this technique provides high-quality interface between high-k materials and $In_{0.53}Ga_{0.47}As$ by accommodating highly scaled dielectrics (sub-nm thickness) with low interface traps densities (in the low 10^{12} $cm^{-2}eV^{-1}$). With optimized conditions, this technique improves interface properties, especially reducing midgap D_{it}, independent of the specific dielectric. Optimized conditions of plasma are required for each type of plasma species. Since the III-V substrates are sensitive to plasma conditions, one of the subsequent studies on the effect of number of plasma+TMA cycles to the interface is shown in ref.[138]. It is found that for a large number of plasma cycles, damage occurs to the semiconductor surface as seen from the major increase in the frequency dispersion for negative bias of the CV curves. In this study, it is also suggested that too few numbers of cycles is insufficient for cleaning the defects which are responsible for the midgap D_{it} response. The plasma cycles are believed to remove the native oxides such as In-, Ga-, and As-oxides and others sub-oxides from the III-V semiconductor surface.

Furthermore, the increase of the number of plasma+TMA cleaning cycles also increases the thickness of the interfacial layer as shown in Figure 3.3. Figure 3.3(a), 3.3(b), and 3.3(c) represent HAADF/STEM images of $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with 7, 10, and 13 cycles of nitrogen+TMA plasma cleaning, respectively. The interfacial layer thickness increases from 1.76 nm for 7 cycles to 2.81 nm for 13 cycles, which is almost a 60 % increase. The additional thickness is believed to be a result of an additional oxidation from subsequent oxide deposition cycles. The HfO_2 layers thickness also grows from 4.01 to 4.59 nm, which is likely due the better nucleation and wetting behavior on the thicker interface layer. However, this increased interfacial

layer thickness gives a negative effect on scaling EOT. Figure 3.4, shows CV curves of the MOSCAPs samples from Figure 3.3. The accumulation capacitance density decreases as the interfacial layer and oxide layer increase from 7 to 13 cycles (from Figure 3.4(a) to Figure 3.4(c), respectively). The CV curves are all well-behaved with small frequency dispersion in the depletion region, indicating low midgap D_{it}. It is noted that the slightly higher number of cleaning cycle is not detrimental to the D_{it}. The frequency dispersion response is still low even for 13 cycles of plasma cleaning cycles. Thus, closely optimizing the number of plasma cycles is essential for controlling EOT and midgap D_{it}.

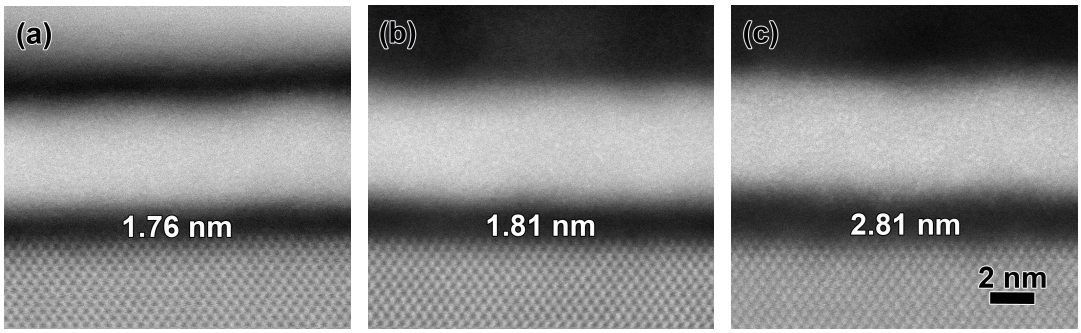

Figure 3.3: HAADF/STEM images of $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with nitrogen+TMA plasma cleaning (a) 7 cycles; (b) 10 cycles; (c) 13 cycles

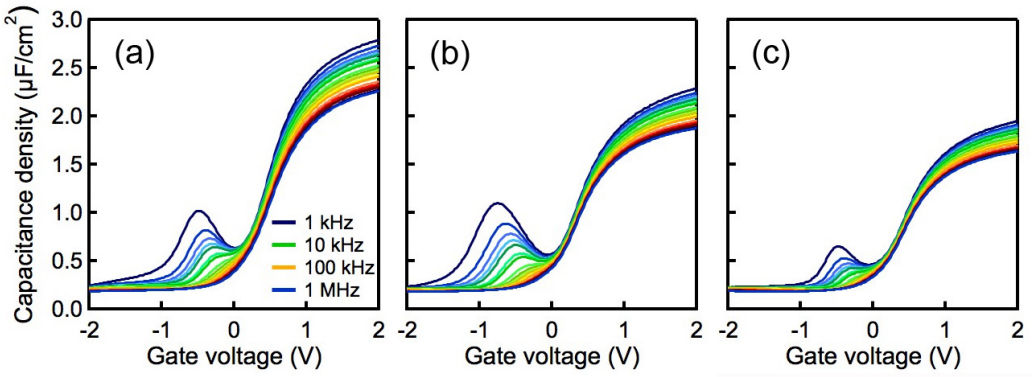

Figure 3.4: CV characteristics as a function of frequencies of $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with nitrogen+TMA plasma cleaning (a) 7 cycles; (b) 10 cycles; (c) 13 cycles

Table 3.1: Details of Nitrogen Plasma + TMA Surface Cleaning Recipes

Recipe	set-up	plasma	pump	TMA	purge		plasma	pump	
A	(10 s	2 s	—	40 ms	—		2 s	2 s)	× 7
B	(5 s	2 s	5 s	40 ms	7 s)	× 9	2 s	4 s	

A detailed study has been completed for nitrogen plasma+TMA alternating surface cleaning steps in order to achieve further EOT scaling, D_{it} reduction, and understand the mechanisms of the interfacial layer. These surface cleaning mechanisms control gate stack properties. The treatment influences interface chemistry and surface morphology of the stacks, which affect their electrical properties. In this study, two slightly different in-situ ALD nitrogen plasma+TMA cleaning procedures are compared for deposition of HfO_2 on $In_{0.53}Ga_{0.47}As$. Both recipes make use of nitrogen inductive coupled plasma (ICP) pulses with 100 W of power at 20 mTorr and 300 °C. Main differences between the two recipes are a pump step after nitrogen plasma and a purge step after TMA pulse, and total number of cycles. Details of each plasma recipe are shown in Table 3.1, which are referred to as Recipe A and Recipe B. Samples subjected to Recipe A were exposed to more nitrogen plasma comparing to Recipe B due to the total time of plasma.

Figure 3.5 shows CV curves and conductance maps measured from ∼4 nm HfO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAPs, which were cleaned with Recipe A and Recipe B. The measured accumulation capacitance densities in both cases are similar, greater than 2.5 $\mu F/cm^2$, corresponding to sub-nm EOT (Figure 3.5(a) and Figure 3.5(b)). The high dispersion in accumulation at lower frequencies curves encounter leakage artifacts from large MOSCAPs gate area. However, measured leakage current at 2 V for 1 MHz curve is less than 2 mA/cm^2. This is not an issue for MOSFETs, which have smaller gate area. Under negative bias, the frequency dispersion is much less for the gate

stacks subjected to Recipe B surface cleaning comparing to that of Recipe A. This characteristic indicates smaller midgap D_{it} response.

The measured conductance maps confirms the observation from the CV characteristics (Figure 3.5(c) and Figure 3.5(d)). The normalized conductance peaks values, $\left(\frac{G_p}{A\omega q}\right)_{max}$, are 4 times less in the gate stack cleaned by Recipe B shown in Figure 3.5(d) than the values shown for Recipe A (Figure 3.5(c)). The D_{it} value around midgap for the gate stack with Recipe B pre-treatment is low, in mid 10^{12} $cm^{-2}eV^{-1}$ range. The movement of the normalized conductance peaks also indicates how efficient Fermi level moves around midgap as a function of gate bias. The Fermi level is unpinned in both cases. Both samples show efficient band bending as more than two order of magnitude in frequency changes as the peaks values shift between 0 to -1 V. In addition, the narrow trace for the sample treated by Recipe B in Figure 3.5(d) suggests that band bending movement is large with respect to the change in gate bias. Thus, Recipe B surface cleaning is more effective in cleaning the midgap D_{it} that the conditions form Recipe A. This result emphasizes the sensitivity and importance of plasma conditions on the III-V substrates even with small changes in the step details.

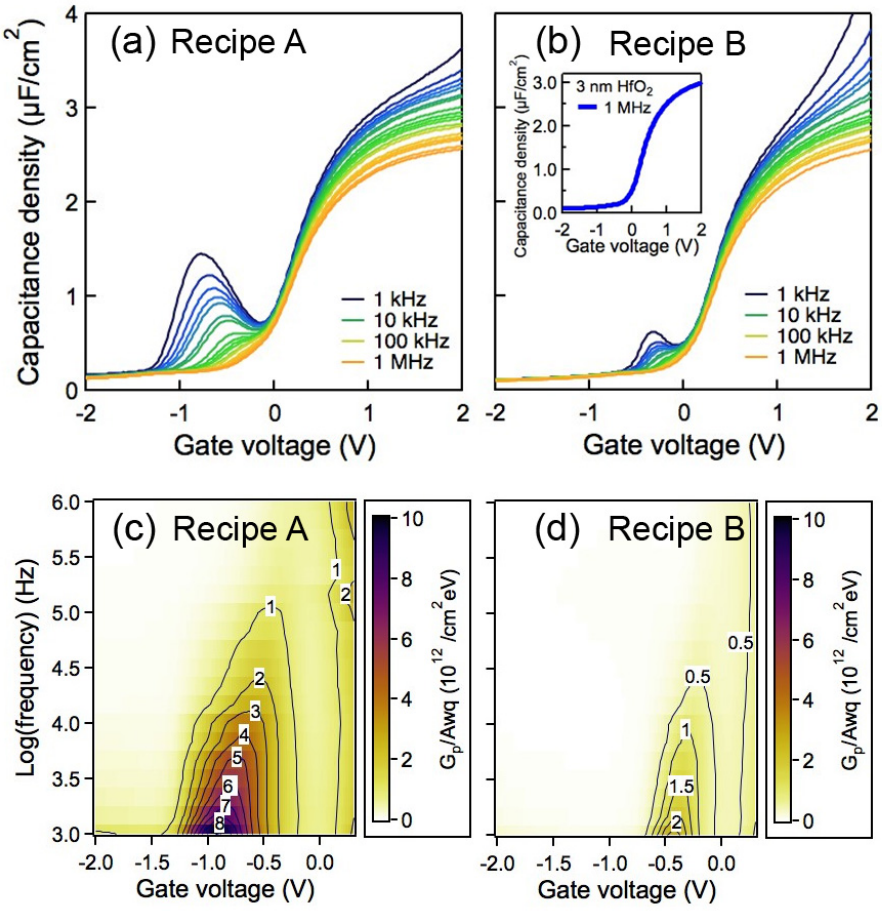

Figure 3.5: Electrical characteristics of ∼4-nm-thick $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with pre-deposition treatment (a) and (c) Recipe A, (b) and (d) Recipe B. Inset in (b) shows CV curve at 1 MHz from 3 nm HfO_2 with cleaning recipe B. Reprinted with permission from [130]. © 2013 AIP Publishing LLC.

Low D_{it} values can be used to evaluate subthreshold swing as mentioned in equation 2.1. The optimized nitrogen plasma+TMA pre-treatment (Recipe B) is implemented in III-V MOSFETs by S. Lee *et al.*[17], and it shows an exceptional performance. For example, the results from an InAs quantum well MOSFETs (schematic shown in Figure 3.6) subjected to Recipe B clean and HfO_2 deposition is shown in Figure 3.7 [17]. For a 40-nm long gate-length (L_g) with undoped vertical spacer, peak transconductance (g_m) of 2.5 mS/μm is measured. The minimum subthreshold swing (SS_{min}) is 86 mV/dec at V_{DS} = 0.5 V. For 1-μm L_g, the SS_{min} at V_{DS} = 0.1 V is 66 mV/dec, which is close to the theoretical value (60 mV/dec). The EOT for these gate dielectrics is estimated to be about 0.8 nm with D_{it} of $\sim 3 \times 10^{12}$ cm^{-2}eV^{-1}. In addition, gate leakage shown in Figure 3.7(c) is negligible ($\sim$low 10^{-10} A/μm), which emphasized that the leakage issues shown in the MOSCAPs data is not a concern for small transistor devices.

The effectiveness of Recipe B cleaning with HfO_2 gate stack is also proven in tunneling field-effect transistors (TFETs). Figure 3.8 shows cross-section schematic and TEM image of a staggered-gap $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ TFET[139]. The improvement in the high-k gate stack due to cleaning process allows high drive current and low subthreshold slope in the staggered-gap TFETs. Figure 3.9 shows transfer characteristics (I_{DS}-V_{GS}) of the TFETs and their subtreshold swings with DC and fast IV measurement[139]. The TFETs with 3 nm HfO_2 gave the SS_{min} of 97 mV/dec at V_{DS} = 0.05 V in DC IV measurement (Figure 3.9(b)). The fast IV measurement minimizes the trap response, which improve switching slope (Figure 3.9(c)). The SS_{min} decreases to 64 mV/dec by this fast IV measurement as shown in Figure 3.9(d). These two results are strong evidence for the high-quality interface formed by using Recipe B pre-treatment on III-V semiconductor surfaces. The low SS_{min} values are direct indications for low midgap D_{it} values that also appear in low frequency

dispersion in the depletion of CV curves and low $\left(\frac{G_p}{A\omega q}\right)_{max}$ values in the conductance map of MOSCAPs data.

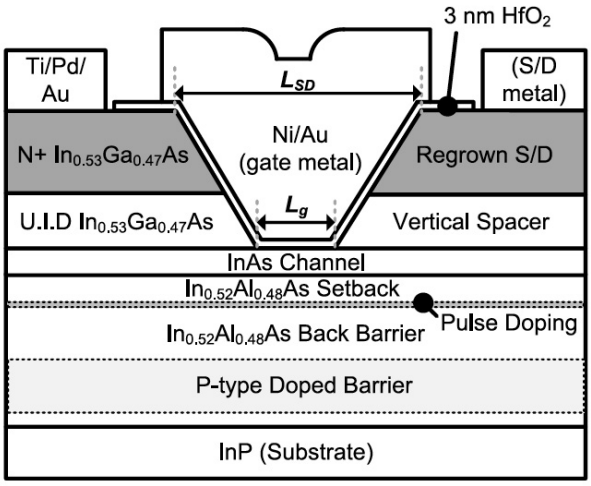

Figure 3.6: Cross-section schematic of an InAs quantum well MOSFET with ∼3-nm-thick HfO_2 as gate oxide with pre-deposition treatment Recipe B. Reprinted with permission from [17]. © Copyright 2014 IEEE

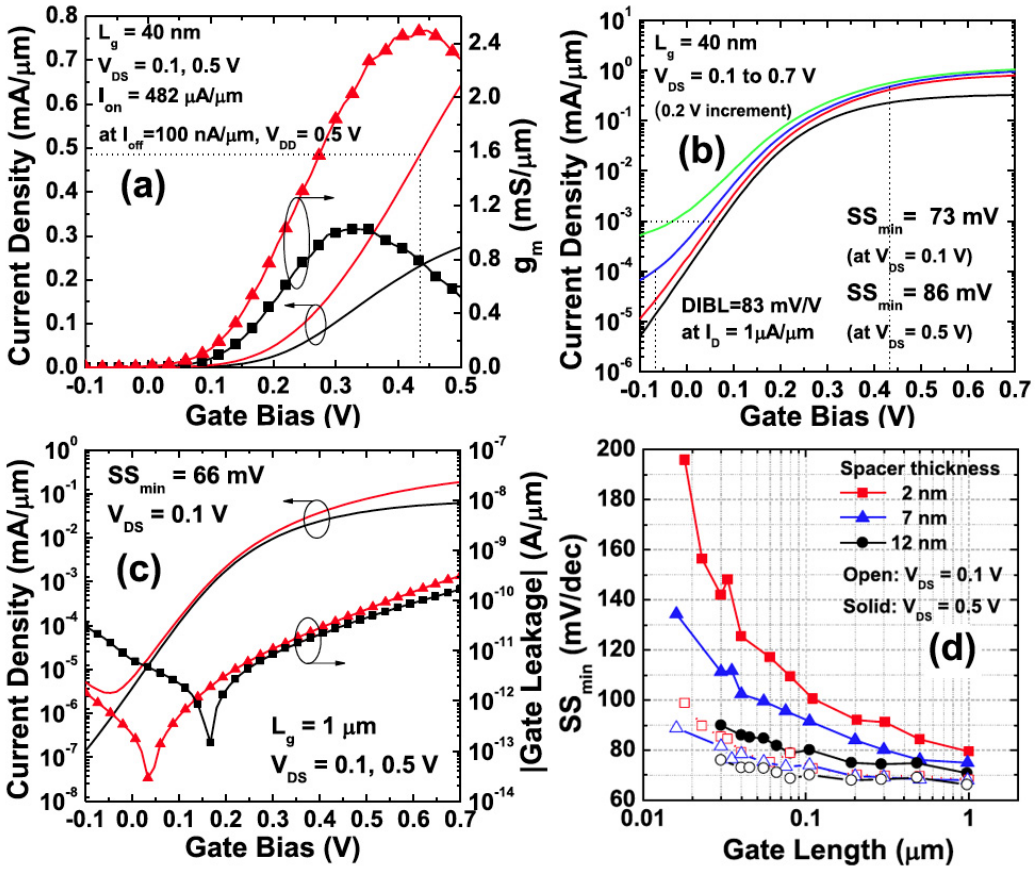

Figure 3.7: Electrical characteristics of ∼3-nm-thick HfO_2/InAs MOSFETs with pre-deposition treatment Recipe B. (a) I_D-V_{GS} and g_m vs. gate bias, (b) $\log(I_D)$-V_{GS} vs. gate bias, (c) $\log(I_D)$-V_{GS} vs. gate bias plot for a long channel device (1 μm) and its gate leakage, and (d) SS_{min} vs. L_g at V_{DS} = 0.1 and 0.5 V for different spacer thickness deveices. Reprinted with permission from [17].

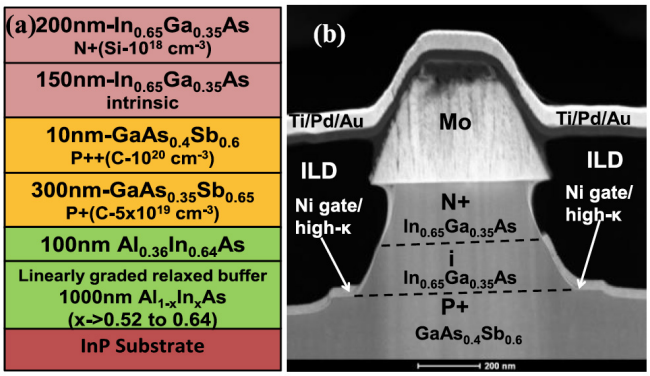

Figure 3.8: (a) Cross-section schematic of the staggered-gap TFET layer structure. (b) Cross-section TEM image of the fabricated staggered-gap TFET with HfO_2 as gate oxide with pre-deposition treatment Recipe B. Reprinted with permission from [139]. © Copyright 2015 IEEE

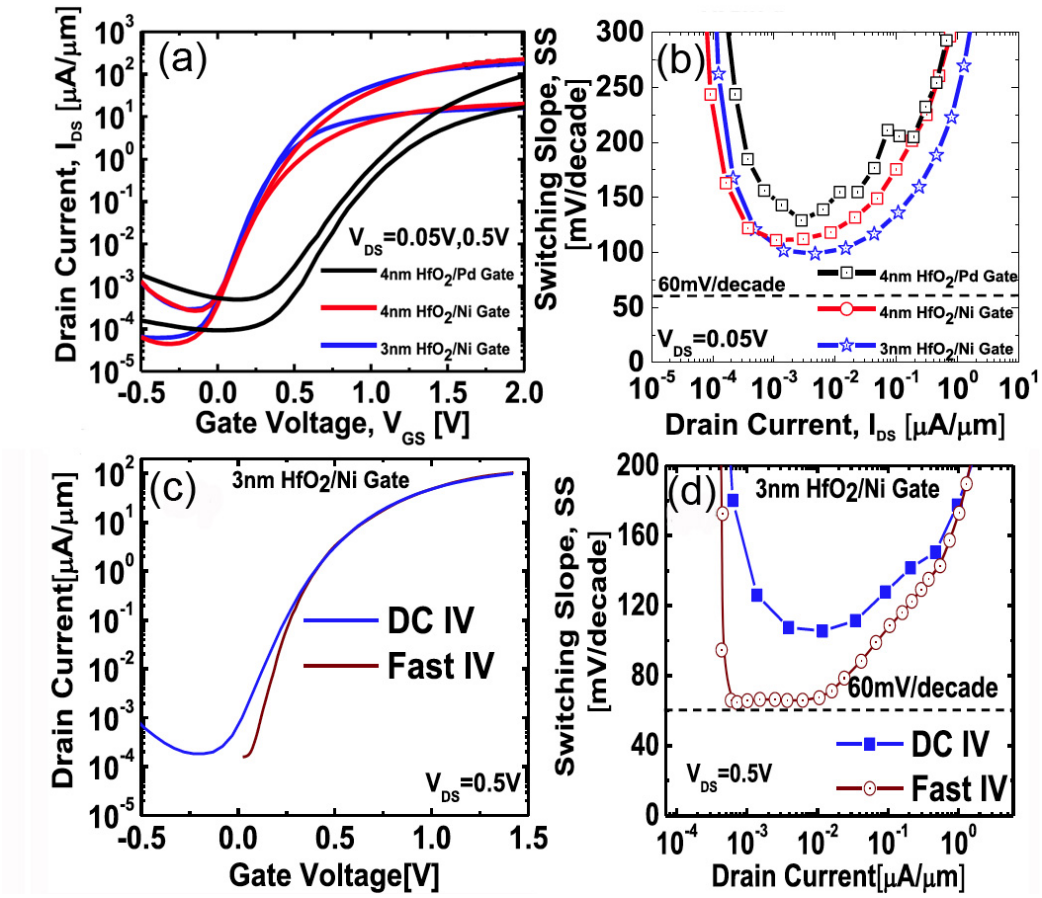

Figure 3.9: Electrical characteristics of $HfO_2/In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ TFETs with pre-deposition treatment recipe B. (a) transfer characteristics of TFET with different gate stacks at T = 300 K and V_{DS} = 0.05 V and 0.5 V, (b) SS as a function of drain current showing improvement with thermal gate metal evaporation and EOT scaling, and (c-d) Transfer characteristics and SS improve with fast I-V measurement. SS_{min} of 64 mV/decade is achieved at V_{DS} = 0.5 V. and its gate leakage. Reprinted with permission from [139]. © Copyright 2015 IEEE

It is important to understand the reasons behind the improvement in the electrical characteristics from the plasma treatment. Surface morphologies can influence the electrical properties and provide insights into growth mechanisms. AFM and SEM images were records from the surfaces of HfO_2 films subjected to Recipe A and Recipe B as shown in Figure 3.10. The surface of the sample cleaned with Recipe A has rough features with some islands up to 10 nm high (Figure 3.10(a)). On the other hand, the sample cleaned with Recipe B (Figure 3.10(b)) has a smoother surface with smaller features less than 2 nm high. Similar features are also represented in the SEM images. In Figure 3.10(c), the film reveals large voids suggesting poor coverage. This voids can be notice throughout the surface of this film. This damage possibly comes from high plasma exposure, which contributes to surface roughening. On the other hand, the sample with Recipe B cleaning has a smooth and uniform surface. The better coverage is likely due to the additional pump and purge steps in Recipe B. Additional time seems to yield a more uniform distribution of nucleation centers. The improved nucleation also leads to further scaling of the overall EOT. Thinner high-k films yield lower EOT. Due to enhanced coverage of III-V semiconductor surface, improved electrical properties are presented (Figure 3.5). In this case, a $\sim$3-nm HfO_2 gate stack can be directly deposited onto $In_{0.53}Ga_{0.47}As$, resulting in capacitance density of 3 $\mu F/cm^2$ at 1 MHz with low midgap D_{it}, shown in the inset of Figure 3.5(b).

Since TMA and nitrogen are used in the pre-deposition cleaning treatment, it is important to know their presence in the gate stacks. XPS can be used for determining chemical compositions in the interface layers between the $HfO_2/In_{0.53}Ga_{0.47}As$. Analysis from samples subjected to Recipe A and Recipe B are shown in Figure 3.11. From the survey scan (not shown), it is found that both films contain 0.2 atomic percent of Al. Figure 3.11(a) and 3.11(b) shows Al 2p peaks at 73.8 eV from Recipe A and

Recipe B, respectively. The peaks indicate fully oxidized aluminum oxide. The Al 2p peaks deconvolved into two components Al $2p^{1/2}$ and Al $2p^{3/2}$, with full width half maximum (FWHM) of ∼1.2 eV and 0.6 eV separation. Figure 3.11(c) and 3.11(d) shows As 3d and Hf 5p peaks. The As 3d peak is fitted with three components, which are As $3d^{3/2}$, As $3d^{5/2}$ peaks with FWHM of 0.65 eV and $\Delta_{As\ 3d} = 0.7$ eV, and Hf $5p^{1/2}$ peak with FWHM of 2 eV. The fitting of this peak is complicated by the overlapping of the Hf $5p^{1/2}$ as mentioned earlier in Chapter 2. Careful consideration of the energy peak splitting of Hf 5p was taken into account. Since there is no other peak appearing at higher energy than that of the As $3d^{3/2}$ peak, it is concluded that there are no detectable arsenic oxides or sub-oxides in the interfacial layers. This result emphasizes that fact that D_{it} is lowered by the elimination of As-oxides, As suboxides, and As-As bonding components.

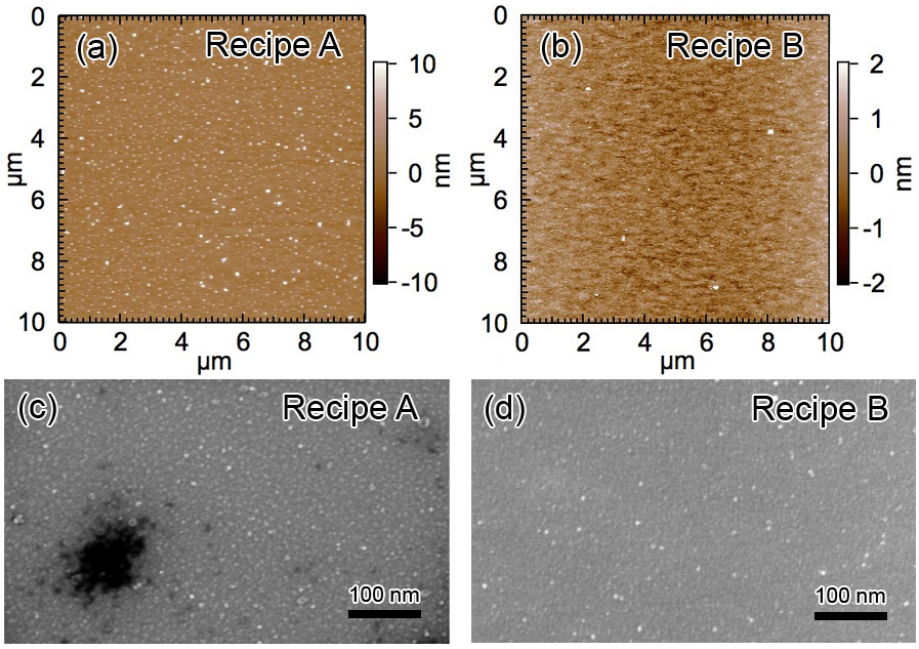

Figure 3.10: Surface morphologies of ∼4-nm-thick $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with pre-deposition treatment (a) and (b) AFM images, (c) and (d) SEM images. Reprinted with permission from [130]. © 2013 AIP Publishing LLC.

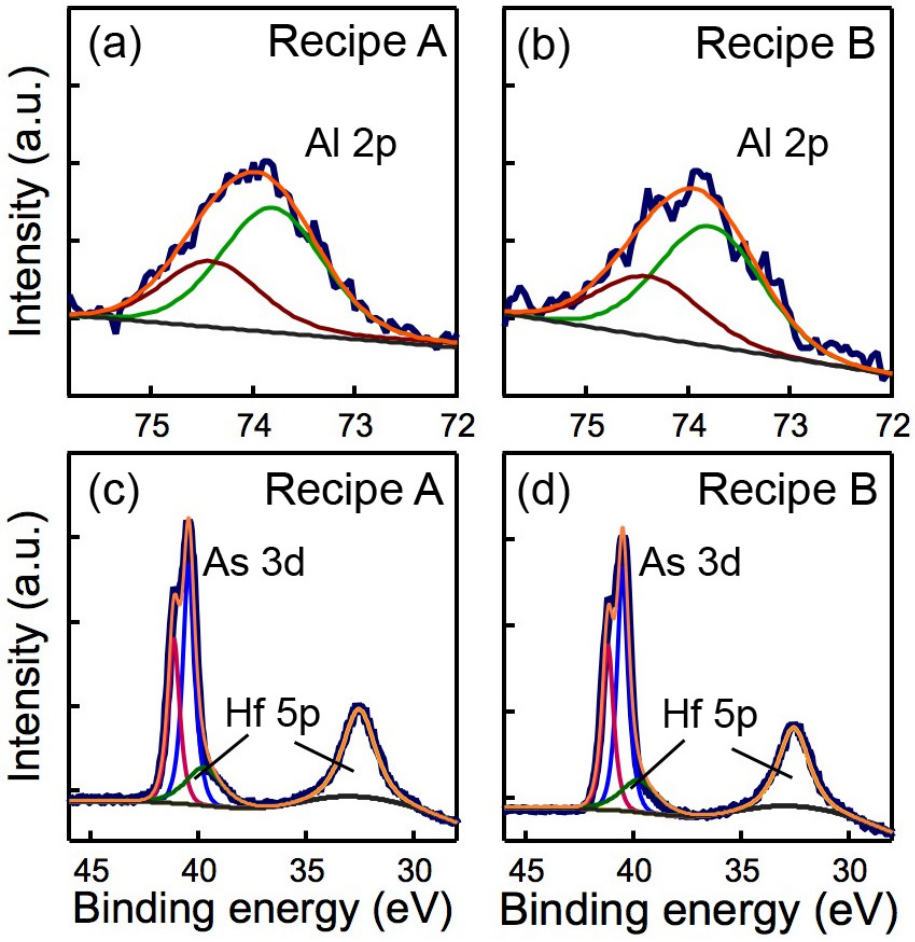

Figure 3.11: XPS spectra of ∼1.5-nm-thick $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with nitrogen plasma+TMA pre-deposition treatments Receipe A and B. (a) and (b) Al 2p peaks, (c) and (d) As 3d and Hf 5p peaks. Thin lines are fitted peaks. Reprinted with permission from [130]. © 2013 AIP Publishing LLC.

A nitrogen component was also detected by XPS in both samples with a very weak signal. However, the nitrogen signal is too small to present here. Thus, secondary ion mass spectrometry (SIMS) is used to determine the presence of nitrogen at the interface. SIMS signal can provide more information on the spatial distribution of the chemical species than XPS. 3 kV cesium beam detects negatively charged fragment at mass 41 (dark blue square symbol), identified as AlN^- at the O/As interface as shown in Figure 3.12(a) and 3.12(b). This presence of this mass is not associated with hydrocarbon species, $AlCH_2^-$, because hydrocarbon profile drops down monotonically from the surface showing a different path than mass 41. Moreover, with a 2 kV oxygen beam, positively-charged mass at 27 was detected at $HfO_2/In_{0.53}Ga_{0.47}As$ interface region on both samples and identified as Al as shown in Figure 3.12(c) and 3.12(d). These results confirm the presence of an oxygen-rich AlO_xN_y interfacial layer detected by XPS.

Both XPS and SIMS show no difference in the interfacial chemistry between the two cleaning recipes. In this experiment, no other In and Ga oxides can be analyzed because of the weak signals and overlapping with Hf peaks. This result implies that both techniques are not sufficiently sensitive to the detection of defects atomic origin. Other techniques such as electron spin resonance might show more sensitivity; however, it is usually more difficult for the III-V semiconductor than Si. There are many components to take into consideration and potentially give low signal by overlapping peaks. Furthermore, the electrical results and physical morphology suggest that complete coverage of interfacial layer is critical in passivating defects on III-V surfaces. Thus, optimizing the cleaning process early and increasing nucleation can reduce the D_{it}.

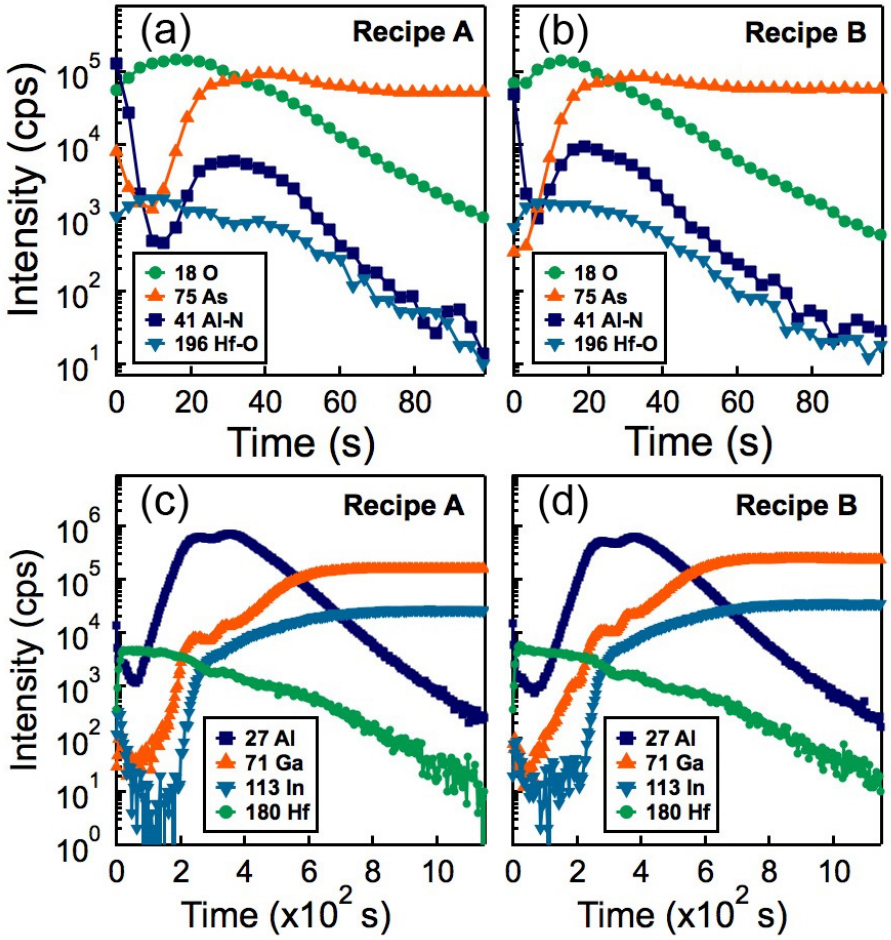

Figure 3.12: SIMs spectra from cesium beam [(a) and (b)] and oxygen beam [(c) and (d)] of ∼1.5-nm-thick $HfO_2/In_{0.53}Ga_{0.47}As$ with nitrogen plasma+TMA pre-deposition treatments (a) and (c) Recipe A, (b) and (d) Recipe B.

In conclusion, an effective passivation layer for the $In_{0.53}Ga_{0.47}As$ can be created by the assistance of nitrogen plasma and TMA cycle cleaning in *in-situ* ALD. The interfacial layer consists of mostly Al_2O_3, with small amount or nitrogen. The process prevents the formation of undesirable As-oxides and As-As bonding, which help reducing the midgap D_{it} response. The high quality surface allows the growth of thinner high-k HfO_2 film directly on $In_{0.53}Ga_{0.47}As$, resulting in high capacitance density MOSCAPs. The process is compatible with transistor fabrications and yield exceptionally high device performances that is not limit to $In_{0.53}Ga_{0.47}As$. This technique opens the door to other III-V surface passivations. Consequently, this procedure should be suitable for deposition of other high-k dielectrics without increasing D_{it} such as ZrO_2. Higher dielectrics constant oxides provide a path to further scale the EOT.

Chapter 4

Scaling the Equivalent Oxide Thickness

4.1 Scaling of the High-*k* Oxides

HfO_2 and ZrO_2 are two of the most attractive candidates as a suitable gate dielectrics for achieving high capacitance density CMOS gate stacks due to their high dielectric constant and large band offset with $In_{0.53}Ga_{0.47}As$. Both HfO_2 and ZrO_2 have an at least four times higher dielectric constant than SiO_2. The dielectric constant for HfO_2 and ZrO_2 in our studies was determined to be 17 and 23, respectively. The calculation took the interfacial layer capacitance and semiconductor capacitance into consideration as described in Ref.[130] and [117], respectively. The accurate dielectric constant values are important for reporting the D_{it} values around midgap from the conductance map. The overestimation of oxide capacitance will make $\left(\frac{G_p}{A\omega q}\right)_{max}$

appear too low.

Direct deposition of HfO_2 and ZrO_2 on $In_{0.53}Ga_{0.47}As$ has been a challenge due to poor wetting. In the previous section, it has been shown that *in-situ* ALD nitrogen plasma+TMA pre-cleaning cycles allows us to achieve high quality interface between HfO_2 and $In_{0.53}Ga_{0.47}As$, with low D_{it} and low EOT. In this section, the same pre-deposition treatment is applied to the $In_{0.53}Ga_{0.47}As$ surface before ZrO_2 deposition. This same treatment allows us to achieve even lower midgap D_{it} and lower EOT with the ZrO_2 gate stack.

The increase in capacitance density and lower midgap D_{it} by using ZrO_2 as the gate stack can be seen in Figure 4.1(a). The capacitance density reached 3.5 $\mu F/cm^2$ at 1 MHz, comparing to $\sim$2.5 $\mu F/cm^2$ from HfO_2 with approximately the same thickness. A small CV hysteresis of 0.2 V at 1 MHz is shown in Figure 4.1(b). The grey symbols in Figure 4.1(a) show the issue from gate leakage artifacts, where $G/A\omega$ value becomes higher than the capacitance density. The measured capacitance above these symbols are not a reliable measure of the capacitance density at low frequencies. This behavior represents phase error from the instrument, when the phase angle of the admittance (I/V ratio) is small. However, it is noted that the leakage current density is less than 0.04 A/cm^2 at 1 V shown in Figure 4.1(c). This value is not an issue for MOSFETs, which have a much smaller area than MOSCAPs, because it is orders of magnitude less than the Si roadmap specifications. In terms of midgap D_{it} response, the frequency dispersion in negative bias is small, indicating low midgap D_{it} values.

Consequently, the conductance map in Figure 4.1(d) shows that the $\left(\frac{G_p}{A\omega q}\right)_{max}$ are low near the midgap (low 10^{12} $cm^{-2}eV^{-1}$), which also suggests that the midgap D_{it} values is small. The movement of the peaks is also efficient as the $\left(\frac{G_p}{A\omega q}\right)_{max}$ peak shifts more than two orders of magnitude in frequency as the gate bias is changed from -0.25

to -0.75 V, indicating large movement of the Fermi level past midgap. The ZrO_2 gate stack was also used in MOSFETs fabrications by S. Lee *et al.*, which results in further reduction of midgap D_{it} (ref.[140]). The schematic of the MOSFETs is similar to the structure shown in Figure 3.6 except the HfO_2 is replaced by ZrO_2 and thinner InAs channel. The SS_{min} of 61 mV/dec is a record for the InAs/$In_{0.53}Ga_{0.47}As$ MOSFET at $V_{DS} = 0.1$ V for $L_g = 1$ μm as shown in Figure 4.2. The SS_{min} is close to the theoretical value at 60 mV/dec. Sub-40-nm L_g devices have high peak g_m value of $>$ 2 mS/μm due to high gate-channel capacitance. The 25 nm-L_g devices also perform comparable to or surpassing 20-25 nm L_g Si FinFETs[141] and nanowire FETs[142]. These results indicate very high quality high-k dielectric and III-V semiconductor interface.

The interface chemistry of this ZrO_2/$In_{0.53}Ga_{0.47}As$ gate stacks was studied. A HAADF/STEM cross-section image by Jack Zhang and XPS spectra are shown in Figure 4.3. The ZrO_2 film in Figure 4.3(a) is uniform and appears amorphous. The interface layer shows dark contrast indicating a low-atomic number film formed during the nitrogen+TMA pre-cleaning treatment. As shown earlier in the HfO_2 gate stacks, the film contains Al, O, and a small amount of N. Here, similar results are detected as shown by the XPS spectra in Figure 4.3(b)-(f). The Zr 3d peak is fitted with Zr $3d^{5/2}$ at 182.6 eV, consistent with ZrO_2 as shown in Figure 4.3(b). The Al 2p peak is fitted at 74.2 eV, indicating Al is fully oxidized. For As 3d, the peak is fitted with two components, at 41.1 eV and 41.8 eV, deriving from $In_{0.53}Ga_{0.47}As$ with FWHM of 0.7 eV. No As-oxides, As suboxides, or As-As bondings is detected, which is similar to what shown earlier in HfO_2/$In_{0.53}Ga_{0.47}As$ interface.

The earlier study on HfO_2 gate stack could not be used to determine the presence of In or Ga oxides due to the overlapping of Hf peaks. However, since there is no overlapping peaks in this study with ZrO_2 film, more qualitative and quantitative

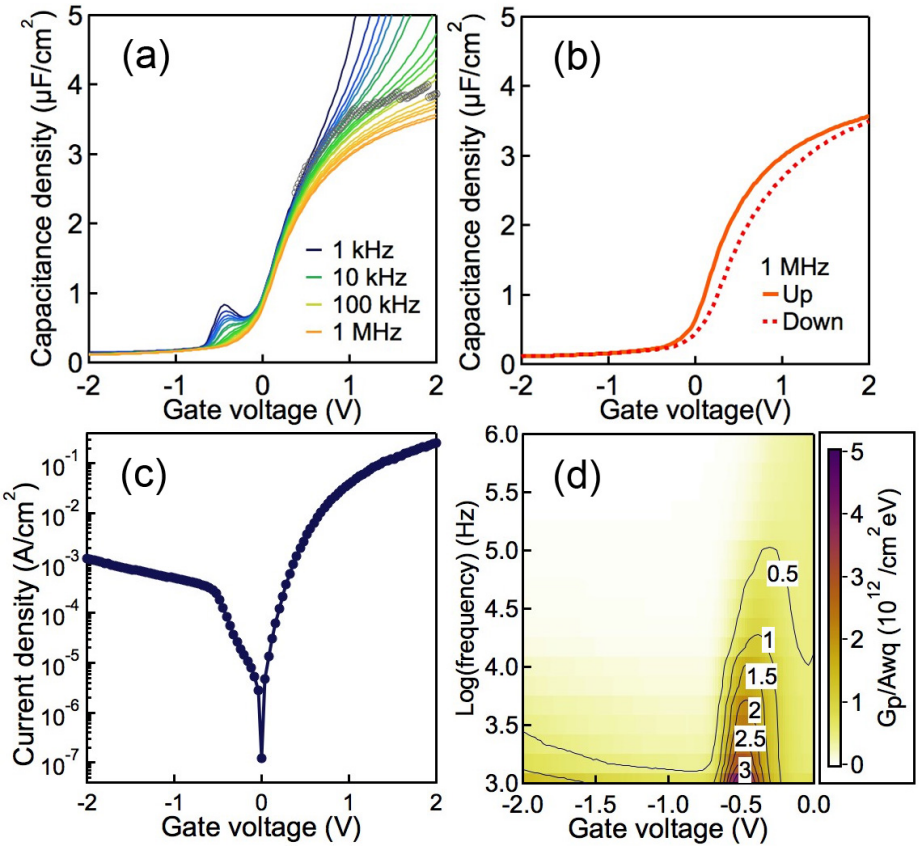

Figure 4.1: Electrical charateristics of ∼4 nm $ZrO_2/In_{0.53}Ga_{0.47}As$ MOSCAP with nitrogen plasma+TMA pre-deposition. (a) CV curves as a function of frequency. Grey symbols indicate where $G/A\omega$ value becomes higher than the capacitance density. (B) CV hysteresis at 1 MHz. (C) Current-voltage characteristics between -2 V to 2 V. (d) Normalized parallel conductance maps, showing $\left(\frac{G_p}{A\omega q}\right)_{max}$ as a function of gate bias and frequency. Reprinted with permission from [117]. © 2014 AIP Publishing LLC.

experiments can be done on these In and Ga components. As a result, In_2O_3 can be detected at higher binding energy components for In $3d^{3/2}$ and In $3d^{5/2}$ as shown in the shaded area in Figure 4.3(e). Similarly, Ga_2O_3 is also detected. The survey scan and the high-resolution peak of In and Ga were used to quantify the amount of In_2O_3 and Ga_2O_3 to be at approximately 0.2 at. % (12% of In is oxidized) and 0.5 at. % (27% of Ga is oxidized), respectively.

According to more information of In- and Ga- oxides, additional insights can be

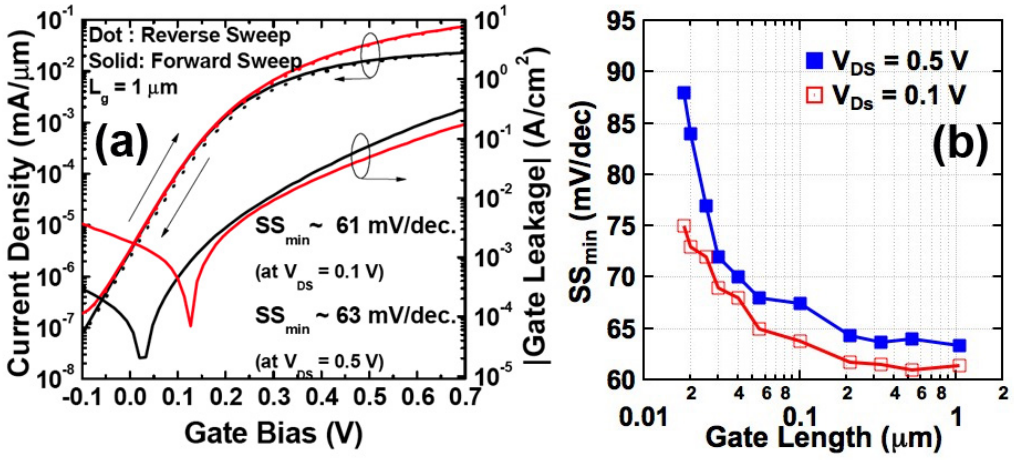

Figure 4.2: Electrical characteristics of ∼3-nm-thick ZrO_2/InAs MOSFETs with pre-deposition treatment recipe B. (a) $\log(I_D)$-V_{GS} vs. gate bias plot for a long channel device (1 μm) and its gate leakage, and (b) SS_{min} vs. L_g at V_{DS} = 0.1 and 0.5 V. Reprinted with permission from [140]. © Copyright 2014 IEEE

gained about the interface from the HAADF/STEM image in Figure 4.3(a). The top interface on $In_{0.53}Ga_{0.47}As$ appears brighter than the rest of the layer, which indicates the presence of In-oxides close to $In_{0.53}Ga_{0.47}As$ interface due to its higher atomic number than Al-oxide. Consequently, it is suggested that the bulk of the interface layer is mostly Al-oxide. It is likely that there is excess oxygen in the cleaning process since the increase in number of the cleaning cycle increase the thickness of the interfacial layer as described in the earlier section.

In summary, *in-situ* ALD nitrogen plasma+TMA cleaning cycles can provide a high quality interface for scaled ZrO_2 on $In_{0.53}Ga_{0.47}As$. The evidence for exceptional electrical characteristics by this treatment can be found in MOSCAPs with low midgap D_{it} response and MOSFETs with low SS_{min}. The chemical analysis also confirms that the absence of As-oxides, As sub-oxide, and As-As bond is related to the reduction of D_{it}. The small amount of In_2O_3 and Ga_2O_3 does not seem to be detrimental to the midgap D_{it} response. This pre-deposition plasma cleaning technique

provides an opportunity to further scale down high-k gate stacks on III-V semiconductors. The majority part of the interfacial layer is Al_2O_3. For further scaling down of the gate stack, Al_2O_3 has to be scaled. It is possible to adjust the plasma precleaning process by using different metal-organic precursors that could replace the Al_2O_3 with a higher-k dielectric. One example is Ti precursors, which ideally can form an interfacial layer consisting of high-k TiO_2.

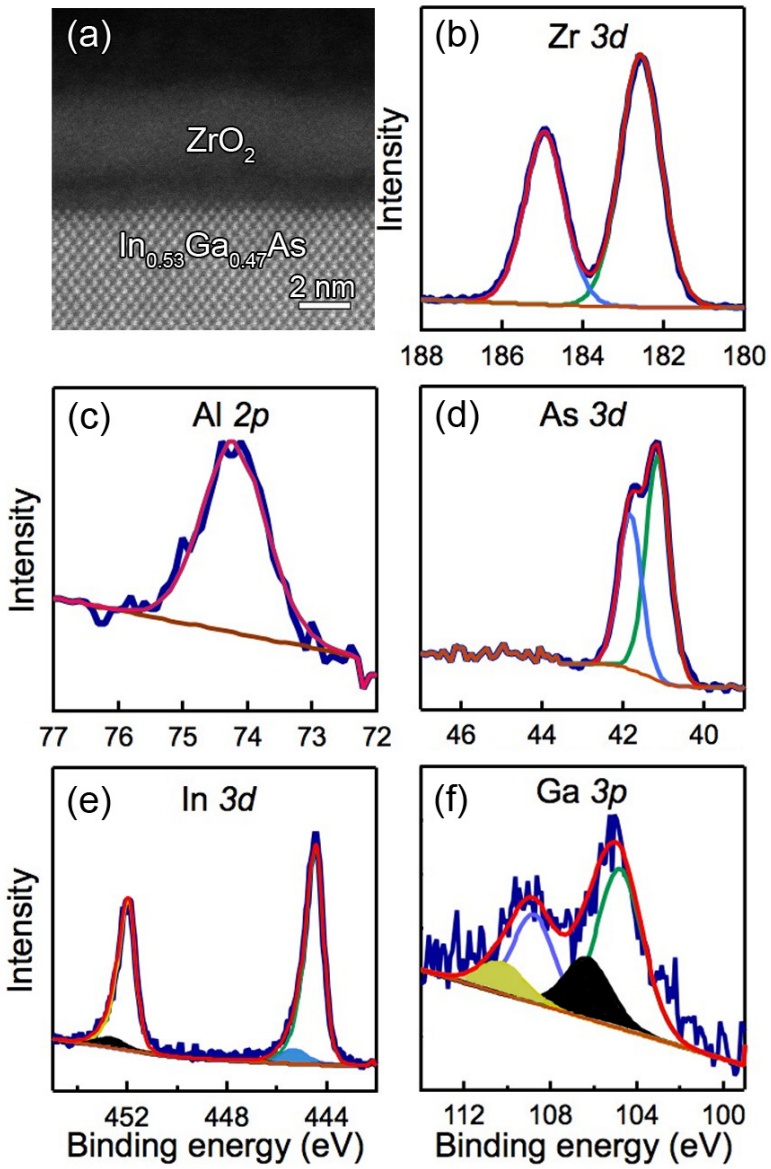

Figure 4.3: (A) HAAD/STEM cross-section images of 400 ∘C forming-gas annealed $ZrO_2/In_{0.53}Ga_{0.47}As$ interface. (b)-(f) XPS of ∼4 nm ZrO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAPs. (b) Zr 3d peaks; (c) Al 2p peak; (d) As 3d peaks; (e) In 3d peaks; and (f) Ga 3p peaks. Thin lines are fitted peaks. Reprinted with permission from [117]. © 2014 AIP Publishing LLC.

4.2 Scaling of the Interface layer

Crystalline TiO_2 can have a dielectric constant as high as 170 in the rutile phase[105]. Its dielectric constant is one of the highest among binary oxides. However, most of the TiO_2 grown by vapor phase techniques produces anatase structure, which has k value around 30-40. It can possibly be post-annealed a high temperature to achieve a higher-k state structure (> 700 °C), but this is not compatible with III-V transistor processes. In the following section, a Ti precursor is intentionally use for replacing Al_2O_3 in the interface layer in order to help scale down the EOT. The process is similar to the nitrogen+TMA cycles describe earlier, except the TMA is replace by Tetrakis(dimethylamido)titanium (TDMAT). In addition, a hold step is also added to allow the distribution of precursor since the vapor pressure of TDMAT is lower than that of TMA.

By using similar pre-treatment steps described earlier, cycles of *in-situ* ALD of nitrogen plasma+TDMAT are used to create a surface passivation layer consisting of Ti-oxide. Figure 4.4 shows XPS data with In 3d and Ti 2p peaks for two samples of $ZrO_2/In_{0.53}Ga_{0.47}As$ with 9 and 4 cycles of nitrogen plasma+TDMAT pre-cleaning treatment. This comparison is used to confirm the presence of Ti in the film. ZrO_2 is chosen here to avoid the issue of Hf peaks overlapping with In, Ga, and As peaks. The samples were annealed in forming gas for 15 min at 400 °C. The thin lines are fitted to measured data. At 451.9 and 444.3 eV for In $3d^{3/2}$ and In $3d^{5/2}$ peaks, respectively, are fitted and consistent with InGaAs [143]. Due to the overlapping of As Auger and In loss signal to the Ti 2p peaks, signal from $\sim$1 nm $Al_2O_3/In_{0.53}Ga_{0.47}As$ sample without Ti was used for extracting the real signal from Ti 2p peaks. It is noted that uncertainty exists in the fitting of these Ti peaks. Low intensity peaks of As Auger at 461 and 468 eV were removed from this background subtraction. The Ti $2p^{3/2}$

peaks appears at 458.7 eV, consistent with TiO_2 bonding. With similar confidence, an additional set of peaks at 457.1 eV and 463.3 eV could also be fitted corresponding to Ti^{3+}. These peaks could be associated with a sub-oxide and/or some Ti-N or Ti-O-N bonding. It is difficult to detect N in these XPS studies due to the interference from N 1s-Ga Auger signals. Comparison between the two samples shows that the sample with 9 cycles of the pretreatment contain higher amount of Ti than the film with 4 cycles pretreatment as shown by the greater ratio of Ti:In in the interface with 9 cycles pretreatment (0.92 vs. 0.65). A higher binding energy component indicating the presence of In_2O_3 is detected at 452.8 and 445.3 eV as shown in the shade area of the In 3d peaks. The amount of In_2O_3, quantified from the survey scan and the high-resolution, is approximately 0.3-0.4 at.% of the overall interface region. No Ga-oxides, As-oxides, As suboxide, or As-As bonding could be detected. Therefore, the interface is mostly TiO_2 with small amount of In_2O_3 and nitrogen.

Electron microscopy was used to investigate the interface. Figure 4.5 shows HAADF/STEM cross-section images (by Jack Zhang) of ∼4 nm HfO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAPs interfaces, subjected to (a) 9 cycles; (b) 6 cycles; (c) 4 cycles; and (d) 2 cycles of the nitrogen plasma+TDMAT pre-deposition treatment. All images show an amorphous interface between HfO_2 and $In_{0.53}Ga_{0.47}As$. The darker contrast indicates this layer contains a low-atomic number material than HfO_2 film. It is likely to be TiO_2 as suggested earlier by the XPS results (Ti has lower atomic number than Hf). The HfO_2 layer shows small crystallinity as seen by wormlike-contrast in the images. The thickness of the HfO_2 is relatively constant as well. The images show that the amorphous Ti-O interface layer remains relatively constant even though the number of precleaning cycles changes. This result is opposite to the effect from nitrogen plasma+TMA pretreatment cycles shown in Figure 3.4. This result from nitrogen plasma+TDMAT pretreatment cycles indicates that self-limited growth has occurred.

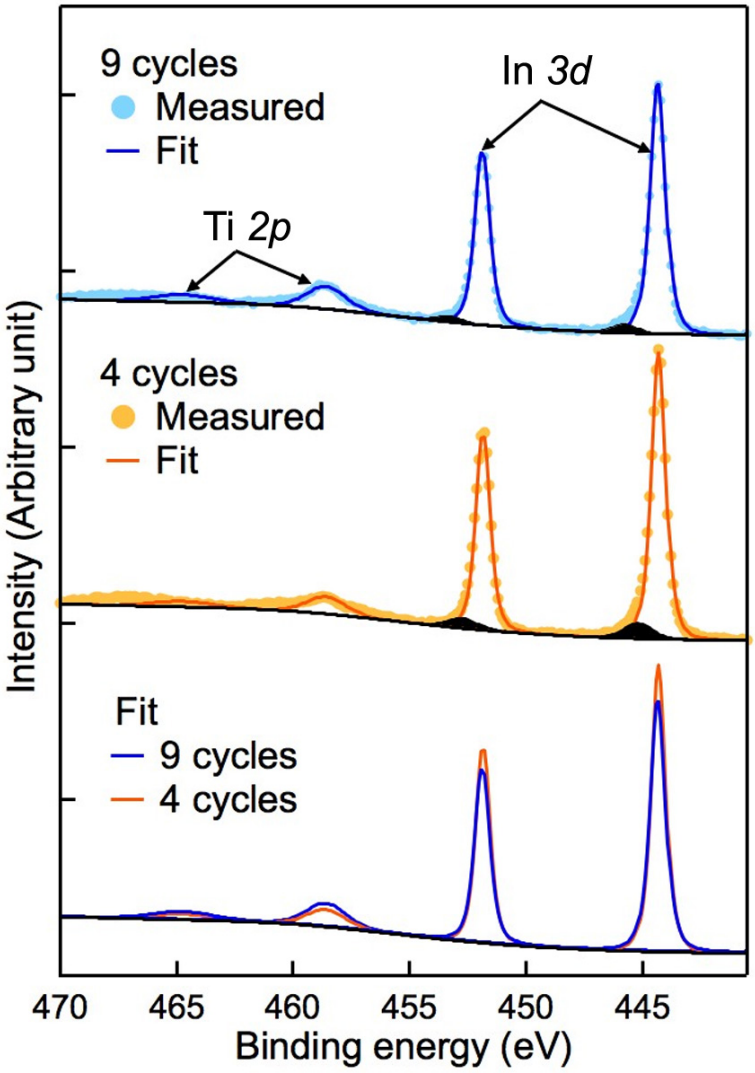

Figure 4.4: Ti $2p$ and In $3d$ XPS spectra of ∼1 nm ZrO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAPs subjected to 9 and 4 cycles of nitrogen plasma+TDMAT pre-treatment. The black shaded areas indicate peaks associated with In_2O_3. Thin lines are fitted peaks. Reprinted with permission from [108]. © 2014 AIP Publishing LLC.

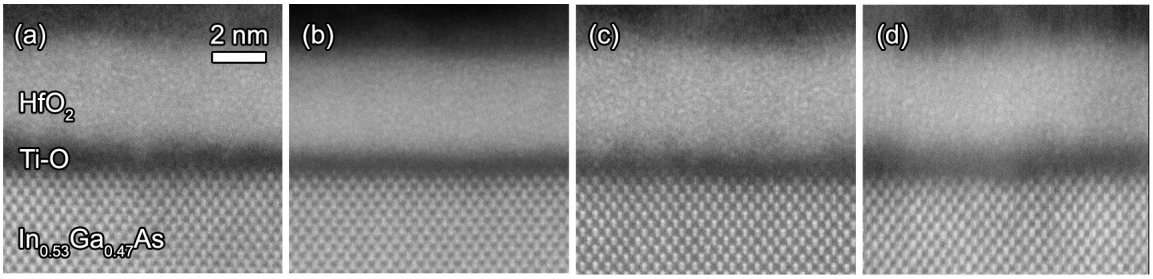

Figure 4.5: HAADF/STEM cross-section images of ∼4-nm HfO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAPs interfaces, subjected to (a) 9 cycles; (b) 6 cycles; (c) 4 cycles; and (d) 2 cycles of the nitrogen plasma+TDMAT pre-deposition treatment. All samples were annealed in forming gas at 400 °C after HfO_2 deposition. The TEM foil in (b) is thicker, so the contrast was adjusted for better comparison with the thinner foils. Reprinted with permission from [108]. © 2014 AIP Publishing LLC.

The electrical properties of these films were characterized. Figure 4.6 shows CV curves of the ∼4-nm $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs samples shown in STEM images from Figure 4.5. With the same oxide thickness, the accumulation capacitance density increases as the number of nitrogen plasma+TDMAT cycles increases. This increase is related to the higher Ti content in the film as detected from the XPS. At low frequencies, the capacitance density suffers leakage artifacts. It is represented by black circles, indicating where $G/\omega \geq$ C. The measured capacitance values above these circles are unreliable due to the instrument artifacts mentioned in earlier section.

The frequency dispersion in depletion also varies with the number of pretreatment cycles. The low frequency dispersion hump in negative bias region indicates small midgap D_{it} response. This behavior suggests that the optimized number of pretreatment for midgap response is around 4-6 cycles. On the other hand, the frequency dispersion in accumulation decreases as the number of pretreatment increases. This dispersion is particularly low for a scaled gate stack on III-V semiconductors with such a high capacitance density. The origin for the frequency dispersion in accumulation is still under debate in the community[36, 115, 114, 118]. Nonetheless, this low frequency dispersion in the accumulation from this pretreatment emphasize the im-

portance of the surface cleaning process to the electrical properties of the interfacial layer.

At 1 MHz, the accumulation capacitance density reaches 4.5 μF/cm^2 for the samples with 9 cycles of pretreatment (Figure 4.6(a)). The capacitance density for other samples are also exceptionally high. The higher capacitance density can be reached by optimizing the pretreatment and the high-k oxides gate stack. For example, CV curves of $\sim$ 1 nm HfO_2/$\sim$ 3 nm ZrO_2 bilayers gate stacks with 6 cycles of nitrogen plasma+TDMAT pretreatment is shown in Figure 4.7(a). The accumulation capacitance density reaches 5.3 μF/cm^2 at 2 V and 1 MHz. This capacitance density is much higher that other gate stacks, where the largest reported values are around 3 μF/cm^2. The dashed line in Figure 4.7(a) indicates a CV hysteresis of 0.06 V around flatband at 1 MHz. This hysteresis is very small, and decreases if the bias is swept in a smaller range. This behavior indicates that the charge trapping in the oxide is small. In addition, the CV curve shows a finite slope at negative bias, which indicates deep depletion. It is one of the indicators that the Fermi level is not pinned and able to move to the lower half of the bandgap[144].

Figure 4.7(b) shows HAADF/STEM cross-section image (by Jack Zhang) of the same MOSCAP in Figure 4.7(a). All the layers look smooth and uniform. The interfacial layer thickness (labeled Ti-O) is about 0.5 nm which is thinner that the stacks shown in Figure 4.6. The change in interfacial layer thickness and the incorporation of ZrO_2 result in a higher capacitance density. It is noted that the gate stack with only ZrO_2 results in high leakage characteristics. Thus, HfO_2 layer is kept in between to minimize the issue.

CV curves show small frequency dispersion in both depletion and accumulation regions. Compared to the frequency dispersion in accumulation of gate stacks with Al-O interface, the Ti-O interface gives smaller dispersion at high capacitance density.

Figure 4.7(c) shows a measure of the frequency dispersion in accumulation, expressed in terms of the coefficient α of a power law fit to the frequency dispersion ($C_{acc} = Af^{\alpha}$, where C_{acc} is the accumulation capacitance density at +1 V from flatband, A is a constant, and f is the frequency). It compares gate stacks of the same high-k oxide, but with different interfacial layers. The frequency dispersion of HfO_2 dielectrics and the bilayer MOSCAP, with Al-O and Ti-O interface layers are compared as a function of the maximum capacitance density at 1 MHz. For the Al_2O_3 interface, α increases as the accumulation capacitance density increases. On the other hand, for the Ti-O interface, α decreases as the accumulation capacitance density increases. The higher accumulation capacitance density results from higher Ti content in the interface by subjected to more pretreatment cycles as mentioned earlier. It is noted that the $\sim$ 1 nm HfO_2/$\sim$ 3 nm ZrO_2 bilayers gate stack with 6 cycles of nitrogen plasma+TDMAT pretreatment, which has the highest capacitance density, has similar dispersion values as the HfO_2 gate stack with 6 cycles of the same pretreatment.

The small frequency dispersion under depletion in Figure 4.7(a) indicates that this $\sim$1 nm HfO_2/$\sim$3 nm ZrO_2 bilayers gate stack with 6 cycles of nitrogen plasma+TDMAT pretreatment has a small midgap D_{it} response. A quantitative measure of D_{it} can be estimated by the the normalized parallel conductance peak values shown in Figure 4.8(a). Near midgap, the D_{it} values are in the 10^{12} cm^{-2} eV^{-1} range, which is similar to the Al-O interface gate stacks. The efficient movement of the normalized parallel conductance peaks also emphasizes that the Fermi level is unpinned at midgap. The large two orders of magnitude shift indicates large band bending with respect to gate bias. For the same MOSCAP, Figure 4.8(b) shows leakage current as a function of gate bias. The leakage current density is small as the measured value is 5 mA/cm^2 at 1 V. This value is still below the limit specified by the international technology roadmap for semiconductors. Overall, the nitrogen plasma+TDMAT pretreatment provides a

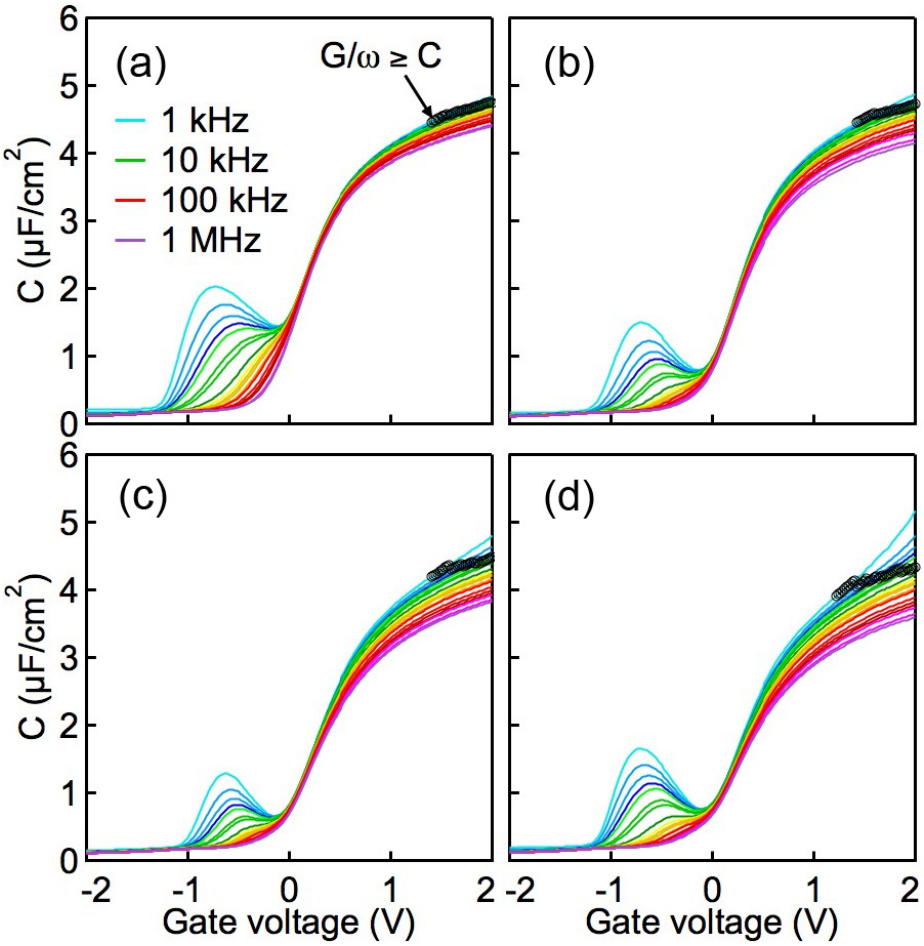

Figure 4.6: CV characteristics of ∼4-nm HfO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAPs interfaces, subjected to (a) 9 cycles; (b) 6 cycles; (c) 4 cycles; and (d) 2 cycles of the nitrogen plasma/TDMAT pre-deposition treatment. All samples were annealed in forming gas at 400 °C after HfO_2 deposition. The black circles represent where $G/\omega \geq$ C. Reprinted with permission from [108]. © 2014 AIP Publishing LLC.

quality interface that allows various superior electrical characteristics comparing to the nitrogen plasma+TMA pretreatment.

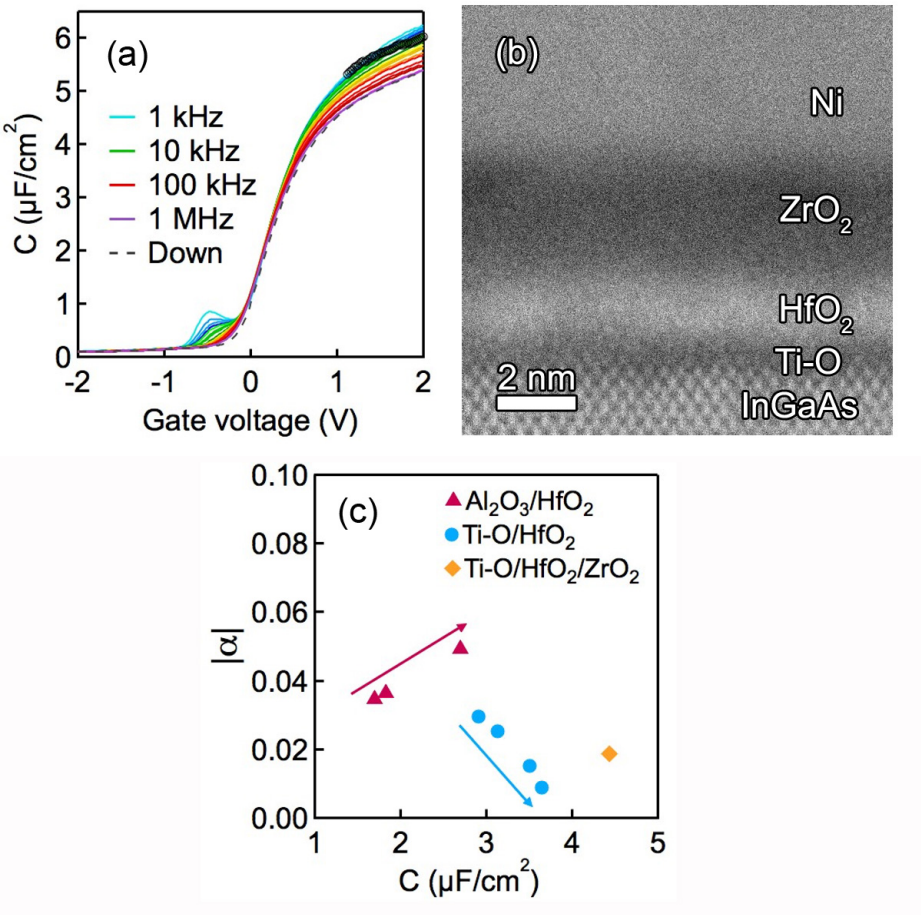

Figure 4.7: (a) CV characteristics as a function of frequency and (b) HAADF/STEM cross-section image of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ∼3 nm ZrO_2/∼1 nm HfO_2 subjected to 6 cycles of nitrogen plasma+TDMAT pre-treatment. The dashed line in (a) shows downward (positive to negative voltage) sweep at 1 MHz. The black markers indicate where $G/\omega \geq$ C. (c) Power law coefficient α of a power law fit of the frequency dispersion ($C_{acc} = Af^{\alpha}$) at +1 V from flatband for $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with nitrogen plasma/TMA pre-treatment, and $HfO_2/In_{0.53}Ga_{0.47}As$ and $ZrO_2/HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with nitrogen plasma+TDMAT pre-treatment as a function of the 1M Hz accumulation capacitance density at +1 V from flatband. Reprinted with permission from [108].

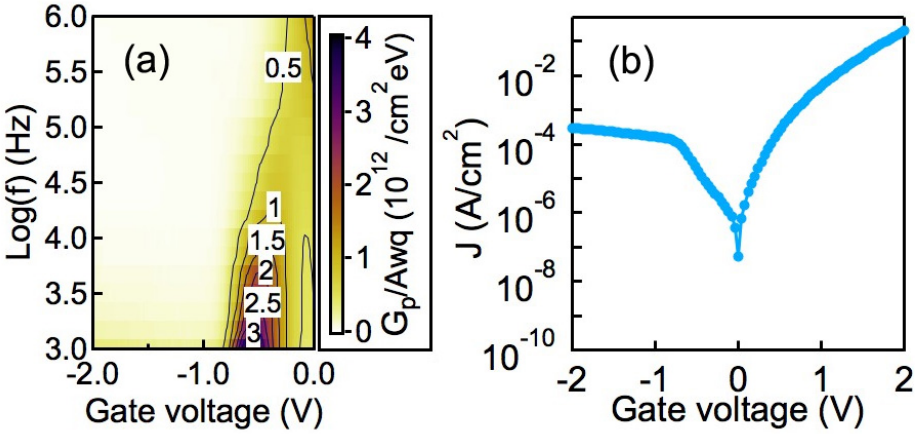

Figure 4.8: (a) Conductance map and leakage of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ∼1 nm HfO_2/∼3 nm ZrO_2 subjected to 6 cycles of nitrogen plasma+TDMAT pre-treatment. (a) Normalized parallel conductance maps, showing $\left(\frac{G_p}{A\omega q}\right)_{max}$ as a function of gate voltage and frequency. (b) Current-voltage characteristics between -2 V and 2 V. All measurements are at room temperature. Reprinted with permission from [108]. © 2014 AIP Publishing LLC.

The leakage current density of different gate stacks can be compared. Figure 4.9(a) shows comparable leakage current density between the HfO_2 on Al-O and Ti-O interfaces, both of which are lower than the ZrO_2 gate stack with Al-O interface. All of the HfO_2 films regardless of their interfacial layers show comparable leakage current density. They also have lower leakage current density than the ZrO_2 film with Al-O interface. The gate stacks with Ti-O interface shows relatively low leakage current, counterintuitive to what normally expected due to the low conduction band offset between TiO_2 and $In_{0.53}Ga_{0.47}As$[106, 145]. A possible explanation will be described later.

The leakage data can be described by direct tunneling[146, 147]:

$$J = \frac{q^3}{16\pi^2\hbar\phi_{ox,eff}} E^2 \times exp\left(-\frac{4\sqrt{2m^*}{\phi_{ox,eff}}^{3/2}}{3\hbar q} E \left(1 - \left(1 - \frac{V}{\phi_{ox,eff}} \right)^{3/2} \right) \right), \quad (4.1)$$

where q, $\hbar$, and E are the elementary charge, the reduced Planck constant, and the electric field, respectively. The fit parameters were the effective barrier height $\phi_{ox,eff}$ and the effective mass m^*. The image-force-induced barrier lowering was included according to

$$\Delta\phi = \sqrt{\frac{Eq^3}{4\pi\varepsilon_0\varepsilon_{ox}}}, \quad (4.2)$$

where the effective dielectric permittivity, ε_{ox}, was estimated to be $\sim$40 for the amorphous Ti-O and the fitting range was between 0 and +0.7 V.

This model describes the leakage data well, as shown in Figure 4.9(b) for 4 nm HfO_2 with 9 cycles of nitrogen plasma+TDMAT pretreatment. This model is used for extracting $\phi_{ox,eff}$ and m^* for $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAP with different number of nitrogen plasma+TDMAT cycles. As the number of nitrogen plasma+TDMAT pretreatment cycles increases, $\phi_{ox,eff}$ values decreases from 2.06 to 1.93 and m^* increases

from 0.17 to 0.2. The changes in the values of these parameters offset each other. As a result, the leakage current density of the MOSCAPs remains constant for different interface layer conditions (both Ti-O and Al-O interfaces). As mentioned earlier, the low leakage current density on the Ti-O is unexpected due to the much lower conduction band offset to $In_{0.53}Ga_{0.47}As$ (0.6 eV)[106, 145] compared to the offset between Al_2O_3 and $In_{0.53}Ga_{0.47}As$ (2.2 eV)[148]. Much higher leakage current would have been expected for scaled Ti-O interface MOSCAPs. However, the extracted barrier height suggested values close to 2 eV, which explained why the measured leakage current is low.

The proposed explanation for the low leakage current density for Ti-O interface layer is the presence of a large interface dipole. Evidence of the dipole can be found from the shifts in flat band voltage (V_{FB}). According to:

$$\frac{V_{FB}}{q} = \phi_M - \chi_S - \phi_F - \frac{Q_f}{qC_{ox}} + \phi_D, \tag{4.3}$$

where ϕ_M is the effective work function of the metal, χ_S the affinity of the semiconductor, ϕ_D the potential drop due to a dipole layer, Q_f fixed charge, and ϕ_F is the Fermi energy, given by

$$\phi_F = \frac{E_g}{2} - k_B T ln\left(\frac{N_D}{n_i}\right), \tag{4.4}$$

where E_g the band gap, k_B is the Boltzmann constant, T the absolute temperature, and N_D and n_i the doping, and intrinsic carrier concentrations.

In this system, $\phi_M = 5.15$ eV (Ref. [149]), $\chi_S = 4.5$ eV, and $\phi_F = 0.06$ eV at 300 K, which gives $(\phi_M - \chi_S - \phi_F) = 0.59$ eV. The fixed charge at the interface can be extracted from the slope of a plot of V_{FB} versus oxide thickness and an estimate for ε_{ox} (Equation 4.3), as shown in Figure 4.10 (a). The positive fixed charge for this system is estimated to be 1×10^{13} cm^{-2}, which is about an order of magnitude

higher than the fixed charge at the HfO_2/SiO_2 interface[150]. However, the linear dependence of V_{FB} on the oxide thickness indicates that the influence of the fixed charge is small. The intercept value is smaller than $(\phi_M - \chi_S - \phi_F)$, indicating that the interface dipole is negative. A negative dipole serves to increase the effective barrier height[151, 152](the positive end of the dipole points to the semiconductor). The extracted values of the dipole and the calculated V_{FB} for the MOSCAP samples with 2, 4, 6, and 9 cycles of nitrogen plasma+TDMAT pretreatment are shown in Figure 4.10(b). V_{FB} is shifted to more negative bias as the Ti content in the interface layer increases. Thus, ϕ_D becomes more negative. The effect of the negative dipole increases the barrier height more than the effect of the decrease in Figure 4.9. As the effective barrier height increases, lower leakage current density can be expected, as shown in Figure 4.10(c).

In conclusion, the nitrogen plasma+TDMAT pretreatment provides a high quality interface comparable to the nitrogen plasma+TMA pretreatment, but yields much higher capacitance density. This advantage results from the presence of the high-k TiO_2 in the interface layer. The modified chemistry in the interface lowers the frequency dispersion in the accumulation significantly, comparing to Al-O interface. The results show that the region within the thickness of interfacial layer is the origin of the frequency dispersion. It is in agreement with the modeling of the frequency dispersion[119]. The absence of As-oxide and As-As bonding confirms the origin of defects involving with the frequency dispersion, within the XPS detection limit. Consequently, with suitable engineering designs, this nitrogen plasma+TDMAT pretreatment technique is promising for developing high performance III-V transistor devices.

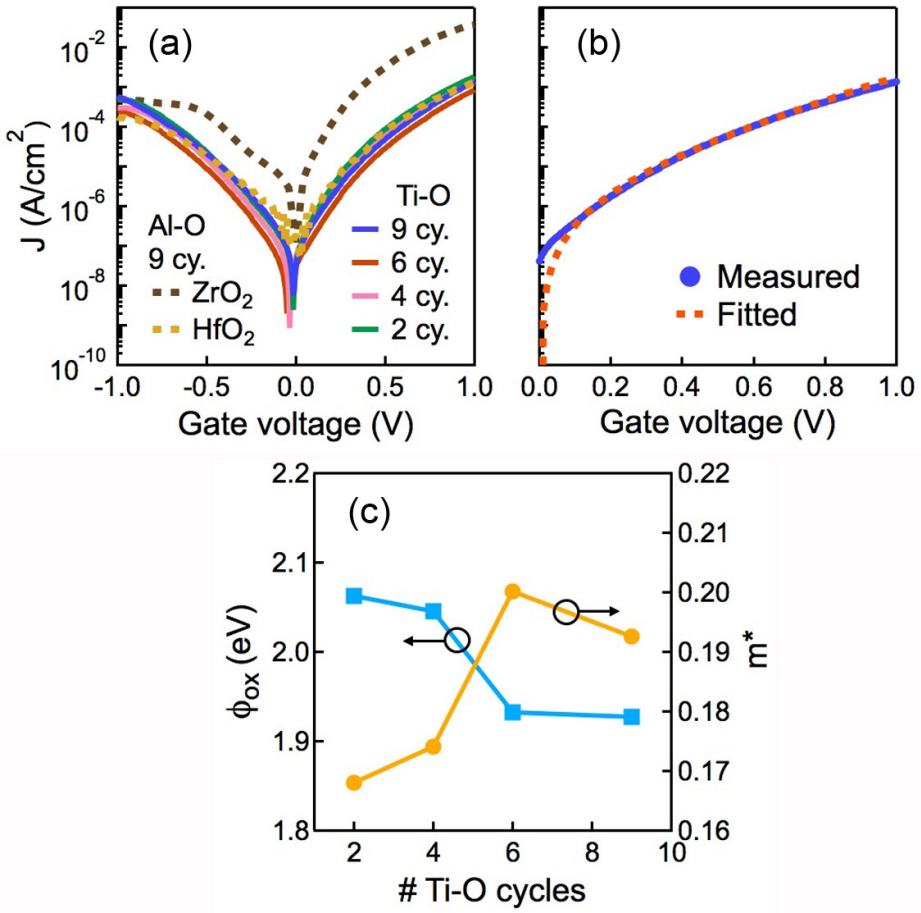

Figure 4.9: (a) Current-voltage characteristics of $In_{0.53}Ga_{0.47}As$ MOSCAPs with either ∼4 nm HfO_2 or ∼4 nm ZrO_2 dielectrics subjected to 9 cycles of nitrogen plasma+TMA pre-treatment and ∼4 nm HfO_2 samples subjected to 9, 6, 4, and 2 cycles of nitrogen plasma+TDMAT pre-treatment. (b) Comparison of measured (solid) and fitted (dashed) current-voltage characteristics between 0 V and 1 V of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ∼4 nm HfO_2 sample subjected to 9 cycles nitrogen plasma+TDMAT pre-treatment. (c) Effective barrier height ϕ_{ox} and the effective mass m^* as a function of the number of nitrogen plasma+TDMAT pre-treatment cycles. Reprinted with permission from [108]. © 2014 AIP Publishing LLC.

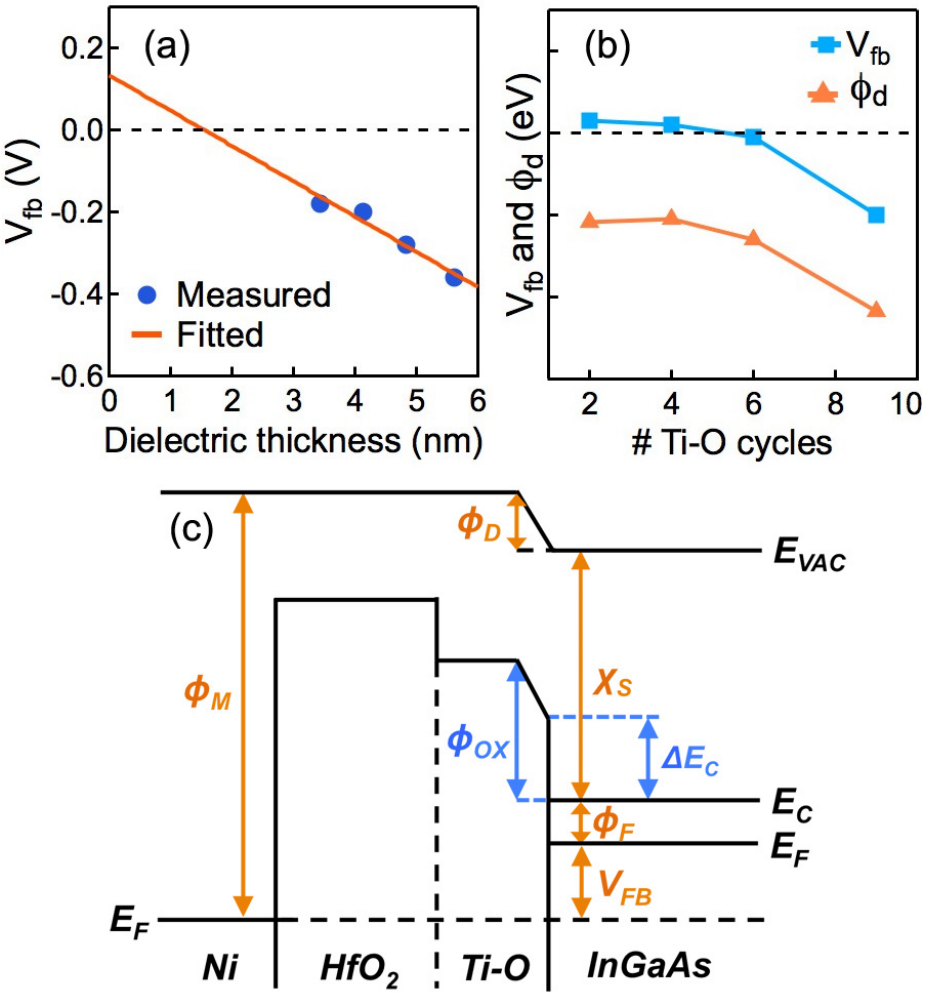

Figure 4.10: (a) Flat band voltage as function of HfO_2 thickness of $In_{0.53}Ga_{0.47}As$ MOSCAPs subjected to 9 cycles of nitrogen plasma+TDMAT pre-treatment. The line represents is a linear fit to the data. (b) Flat band voltage and calculated dipole value as a function of the number of cycles of nitrogen plasma+TDMAT pre-treatment for ∼4 nm $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs. (c) Schematic energy band diagram at flat band of MOSCAP with HfO_2/Ti-O/$In_{0.53}Ga_{0.47}As$ dielectrics showing the effect of an interface dipole on the effective barrier height. The fixed charge is not shown. Reprinted with permission from [108]. © 2014 AIP Publishing LLC.

Chapter 5

High-k Oxides on p-type $In_{0.53}Ga_{0.47}As$

5.1 Pretreatment Conditions for High-k Oxides on p-type $In_{0.53}Ga_{0.47}As$

Knowledge of band engineering brings attention to highly scaled p-channels for III-V semiconductors due to the ability to create high barriers for reducing leakage[153]. Many studies have focused on comparing n- and p-type GaAs. Pashley *et al.* show that Fermi-level pinning behavior on p-type GaAs(001) are controlled by intrinsic surface defects such as step edges and missing unit cells, as opposed to kink sites from self compensation mechanism of acceptors on n-type GaAs(001)[154]. They conclude that the Fermi level of p-type GaAs(001) will be pinned in lower half of the band gap, where the energy position depends on the doping level[155]. In addition, Hinkle *et al.* show that there was no dectable photoelectrochemical reaction among n- and p-type Al_2O_3/GaAs gate stack, but there is a dramatic difference in the frequency dispersion

in accumulation. It is suggested that the disparity of frequency dispersion for n- and p-type GaAs is due to the difference in electron and hole trap time constants[156]. For $In_{0.53}Ga_{0.47}As$, since the valence band density of states is higher than the conduction band density of states; thus, the accumulation capacitance of p-type channel should achieve higher values than those of n-type. To our knowledge, higher accumulation capacitance density on high-k/p-type $In_{0.53}Ga_{0.47}As$ MOSCAP over that with n-type counterpart has not been reported, which is likely because high quality interface between high-k and p-$In_{0.53}Ga_{0.47}As$ has never been achieved.

Different plasma surface cleaning conditions than what have been optimized for n-type $In_{0.53}Ga_{0.47}As$ are needed for p-type $In_{0.53}Ga_{0.47}As$. One of the examples is shown in Figure 5.1 for $\sim$ 2 nm HfO_2/$\sim$ 2 nm ZrO_2 bilayers/n- and p-$In_{0.53}Ga_{0.47}As$ MOSCAPs subjected to 9 cycles of nitrogen plasma+TDMAT pre-treatment. This surface passivation is optimized for n-type samples and have been confirmed to yield high quality for high-k oxide/$In_{0.53}Ga_{0.47}As$ interfaces as shown in previous sections. The high-k oxide film is deposited onto both n- and p-$In_{0.53}Ga_{0.47}As$ substrates simultaneously. The n-type sample in Figure 5.1(a) shows steep slope and low frequency dispersion in accumulation and depletion, which indicates low midgap D_{it} response. The capacitance density reaches accumulation around 5 $\mu F/cm^2$ at 1 MHz and 2 V. On the other hand, the p-sample (Figure 5.1(b)) shows much lower accumulation capacitance (< 2.5 $\mu F/cm^2$ at 1 MHz and 2 V) with larger frequency dispersion in accumulation. It indicates that the Fermi level for p-type sample is pinned at midgap. Even though these two samples were subjected to the same pre-treatment cycles and oxides deposition, the p-type sample performs much worse electrical characteristics. This result suggests that p-type substrate needs different pre-treatment conditions than the n-type substrate. It also indicates that the defects can be in different energy levels of the band gap for n- and p-type channels.

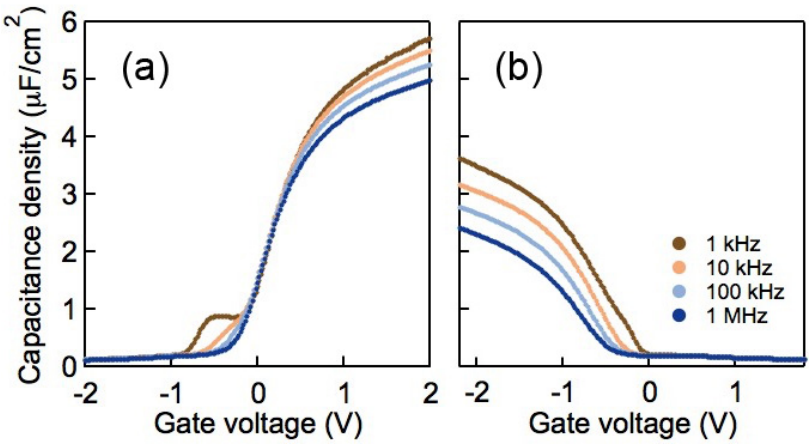

Figure 5.1: CV characteristics of $\sim$ 2 nm HfO_2/$\sim$ 2 nm ZrO_2 bilayers on (a)n-; (b)p-$In_{0.53}Ga_{0.47}As$ MOSCAPs subjected to 9 cycles of nitrogen plasma + TDMAT pretreatment.

Many plasma+metal precursor conditions were explored for achieving high-quality high-k/p-type $In_{0.53}Ga_{0.47}As$ interface, including adjusting number of plasma cycles, plasma duration, deposition temperatures, different types plasma gases (N_2, H_2, and O_2), and different precursors (TMA, TDMAT, and TDMAS). The conditions that have been tested are shown in Appendix B. So far, the most promising pretreatment for p-type $In_{0.53}Ga_{0.47}As$ is the nitrogen plasma+TMA cycles, which can be referred to as Recipe A in section 3.1. The results and analysis are shown here.

Figure 5.2 shows CV characteristics of 6 nm HfO_2/n-type (left column) and p-type (right column) $In_{0.53}Ga_{0.47}As$ MOSCAPs subjected to 12 cycles of nitrogen plasma+TMA pretreatment with the same conditions as Recipe A. Samples were measured in the dark in Figure 5.2(a) and 5.2(b) and under direct 40 W white light in Figure 5.2(c) and 5.2(d). All of the CV curves present well-behaved characteristics. The frequency dispersion in depletion in Figure 5.2(a) and 5.2(b) indicates small midgap D_{it} response. In Figure 5.2(c) and 5.2(d), capacitance values are reaching plateau at large depletion bias (negative gate voltage for n-type and positive gate voltage for p-type). This behavior indicates that the minority carriers are able to

response faster to the change in the gate voltage compare to when the capacitors are measured in the dark. Since the exchange of minority carrier generation between the bulk and the semiconductor surface region has a certain time constant, the rise in capacitance density is more pronounced at low frequencies where the charges are able to follow the AC voltage modulation. This is an indication that the Fermi level is not pinned at miggap for both n-type (left column) and p-type samples.

Comparing accumulation characteristics on n-type substrate with those on p-type substrate, the hole accumulation on p-$In_{0.53}Ga_{0.47}As$ has higher capacitance density value than electron accumulation on n-$In_{0.53}Ga_{0.47}As$ (1.77 $\mu F/cm^2$ and 1.64 $\mu F/cm^2$ at 1 MHz, respectively). This behavior agrees with the fact that the valence band has higher density of states the conduction band in $In_{0.53}Ga_{0.47}As$. This is another experimental evidence showing that these gate stacks have high-quality interface, which allows the Fermi level to move across the band gap and unpin at the midgap of $In_{0.53}Ga_{0.47}As$. The difference in the capacitance density indicates that the semiconductor capacitance has significant effect on the measured capacitance due to small effective mass and low density of states of III-V channel materials[157].

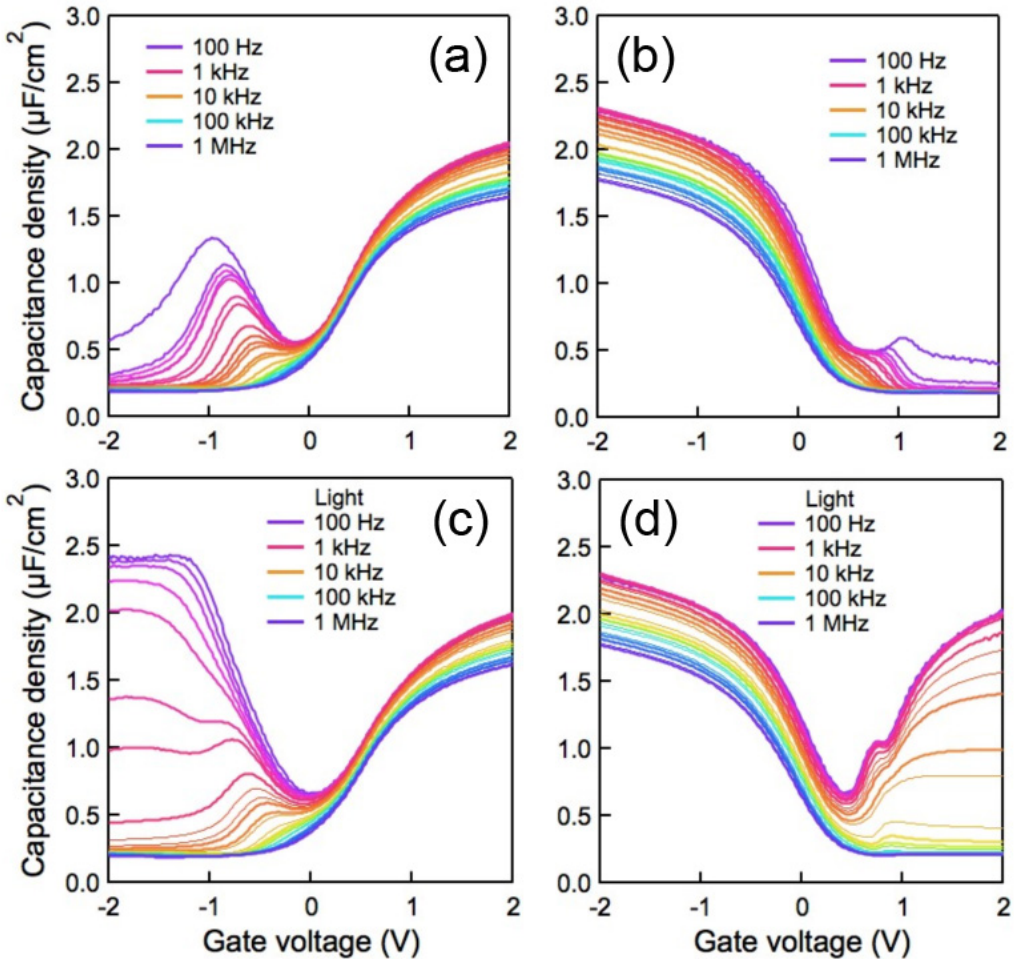

Figure 5.2: CV characteristics of $\sim$ 6 nm HfO_2 on (a) and (c)n-$In_{0.53}Ga_{0.47}As$; (b) and (d)p-$In_{0.53}Ga_{0.47}As$ MOSCAPs subjected to 12 cycles of nitrogen plasma+TMA pretreatment (similar to Recipe A). (c) and (d) show MOSCAPs measured with light.

This difference in accumulation capacitance for n- and p-type channels is also shown for different dielectrics. The CV data and conductance maps for MOSCAP with 1.1-nm-Al_2O_3/4.5-nm-HfO_2 bilayer dielectrics are shown in Figure 5.3. The data shown in Figure 5.3 are from n-type (left column) and p-type (right column) $In_{0.53}Ga_{0.47}As$ channels, respectively. The CV curves (Figure5.3(a) and Figure 5.3(b)) exhibit well-behaved characteristics. Capacitance densities reach accumulation in both n- and p-type channels. The frequency dispersion in the depletion region is small, indicating unpinned interface and low midgap D_{it} [122, 112]. Accumulation capacitance density on n-type substrate (Figure 5.3(a)) in lower than those on p-type substrate (Figure 5.3(b)) (1.7 μF/cm^2 and 1.5 μF/cm^2 at 1 MHz, respectively).

The conductance map (Figure 5.3(c) and Figure 5.3(d)) shows the normalized conductance peaks. The $\left(\frac{G_p}{A\omega q}\right)_{max}$ values can be used to estimate the D_{it} near midgap[111]. The movement of conductance peaks indicates how efficient the Fermi-level moves as a function of gate bias[158]. By tracing the maximum of normalized conductance in Figure 5.3(c) and Figure 5.3(d), the peak moves vertically across the map. This efficient movement of the conductance peak indicates the Fermi level can move more than half of the band gap. The D_{it} values are in the low 10^{12} cm^{-2} eV^{-1} range, approximately proportional to $\left(\frac{G_p}{A\omega q}\right)_{max}$ multiply by a factor of 2.5[121].

These experimental results emphasize that fact that we have obtained reasonable high-quality interfaces for HfO_2 and Al_2O_3/HfO_2 bilayer gate stack in both n- and p-type $In_{0.53}Ga_{0.47}As$ channels with the nitrogen plasma+TMA surface treatment mentioned earlier. This improvement allows further studies of the physical nature of $In_{0.53}Ga_{0.47}As$ by comparing different behaviors of n- and p-type $In_{0.53}Ga_{0.47}As$ channels.

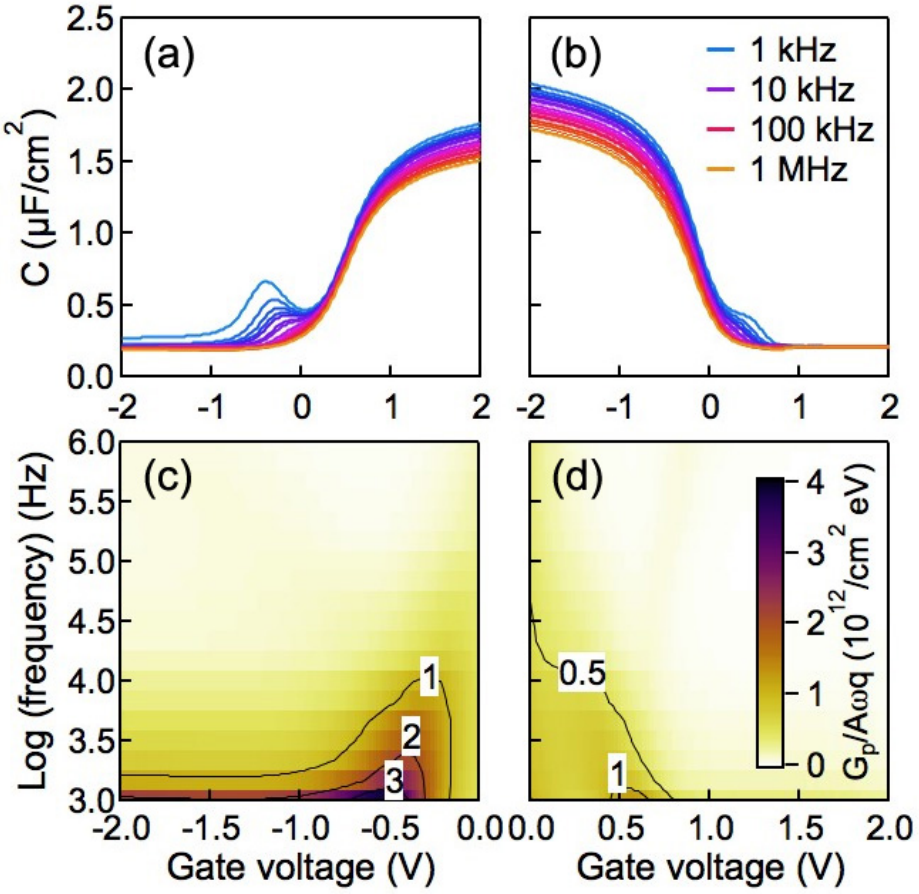

Figure 5.3: n (left column)- and p (right column) $In_{0.53}Ga_{0.47}As$ MOSCAPs with 1.1-nm-Al_2O_3/4.5-nm-HfO_2 bilayers (a) and (b) CV characteristics as a function of frequency; (c) and (d) Normalized parallel conductance map, showing $\left(\frac{G_p}{A\omega q}\right)$ as a function of gate voltage and frequency

5.2 Comparisons of D_{it} Analysis by Terman Method for High-k Oxides on n- and p-type $In_{0.53}Ga_{0.47}As$

For further analysis, Figure 5.4 shows a comparison between high-frequency simulated and 1 MHz experimental CV curves, and extracted band bending from the Terman method for the bilayers MOSCAPs shown in Figure 5.3. The $In_{0.53}Ga_{0.47}As$ band parameters are calculated from estimated values in ref. [126] to construct a high frequency ideal CV curve. The data are from n-type (left column) and p-type (right column) $In_{0.53}Ga_{0.47}As$ channels, respectively. The model includes nonparabolicity of the lowest conduction band and higher conduction band valleys for n-type model. The effect is noticeable in the second upturn in accumulation region of the ideal curve in Figure 5.4(a). On the other hand, the classical approximation is appropriate for p-type due to its large density of states.

For this comparison, C_{ox} is estimated to be 2.1 $\mu F/cm^2$. The C_{ox} values are in good agreement with the dielectric constant estimated from thickness series (Al_2O_3 = 8 ± 1 and HfO_2 = 17 ± 2) and physical thickness measured in TEM. From the simulation, flatband capacitance is 0.78 $\mu F/cm^2$ and flatband voltage is 0.45 V and -0.24 V for n- and p-type stacks, respectively. It is noted that the second upturn in n-type accumulation region never appears in the measurement even for higher capacitance density gate stacks. By using this C_{ox}, the ideal curve intersects with the measured curve more than once for n-type channel as shown in Figure 5.4(a). This behavior results in more crossover points in band bending between 1-2 V in Figure 5.4(c) and negative D_{it} values in the conduction band as shown in Figure 5.5, extracted from the Terman analysis. Although using higher number of C_{ox} for n-type data here would raise the simulated capacitance density and bring D_{it} values to positive numbers, the new C_{ox} will be overestimated for p-type Terman analysis

and the conductance method. It is also logical to use the same C_{ox} value for both n- and p-type analysis because the dielectrics were deposited simultaneously. Using too high C_{ox} will underestimate D_{it} values. In addition, the C_{ox} is already confirmed with thickness series.

Considering the negative bias region of n-type sample in Figure 5.4(a), the ideal depletion capacitance does not reach the minimum values, indicating pinned Fermi level. However, these results are not consistent with to band bending versus gate bias shown in the Figure 5.4(c). In the negative bias region, Figure 5.4(c) shows that the band bends more than 0.4 eV, which is more than half of $In_{0.53}Ga_{0.47}As$ band gap. In addition, Figure 5.3(c) shows efficient peak movement, indicating effective band bending. It is noted that the dopant concentration of the $In_{0.53}Ga_{0.47}As$ channel is confirmed with Hall measurement. The possible explanation for this error could be from ideal semiconductor capacitance density values. The Fermi level can move deep into the conduction band of $In_{0.53}Ga_{0.47}As$ for large C_{ox} due a small conduction band density of states. This problem appears for scaled gate stacks. Thus, appropriate values for higher band valleys are needed. These behaviors (capacitance density values crossover and negative D_{it} from Terman analysis) are similarly observed in the 6-nm-HfO_2/n-type $In_{0.53}Ga_{0.47}As$ gate stack when C_{ox} of 2.3 $\mu F/cm^2$ in used in Terman method (not shown here). It is clearly noticed that there are issues with Terman method when used for analyzing scaled gate stacks on n-type $In_{0.53}Ga_{0.47}As$ channel.

The Terman analysis for p-type samples are also carried out similarly to their n-type counterparts. However, as shown in Figure 5.4(b), the ideal CV curve is higher than the measured curve in hole accumulation region. There is no extra crossover point between the two curves after the transition from depletion to accumulation. The value of gives out an ideal curve that matches well with the measured curve.

Therefore, the simulated D_{it} values do not become negative. The measured band bending curve in Figure 5.4(d) bends efficiently along the slope of the ideal curve. It is also important to note that the ideal CV curve assumes that there is no trap response to the AC signal due to the extremely high frequency. Thus, trap capacitance does not contribute to the total capacitance.

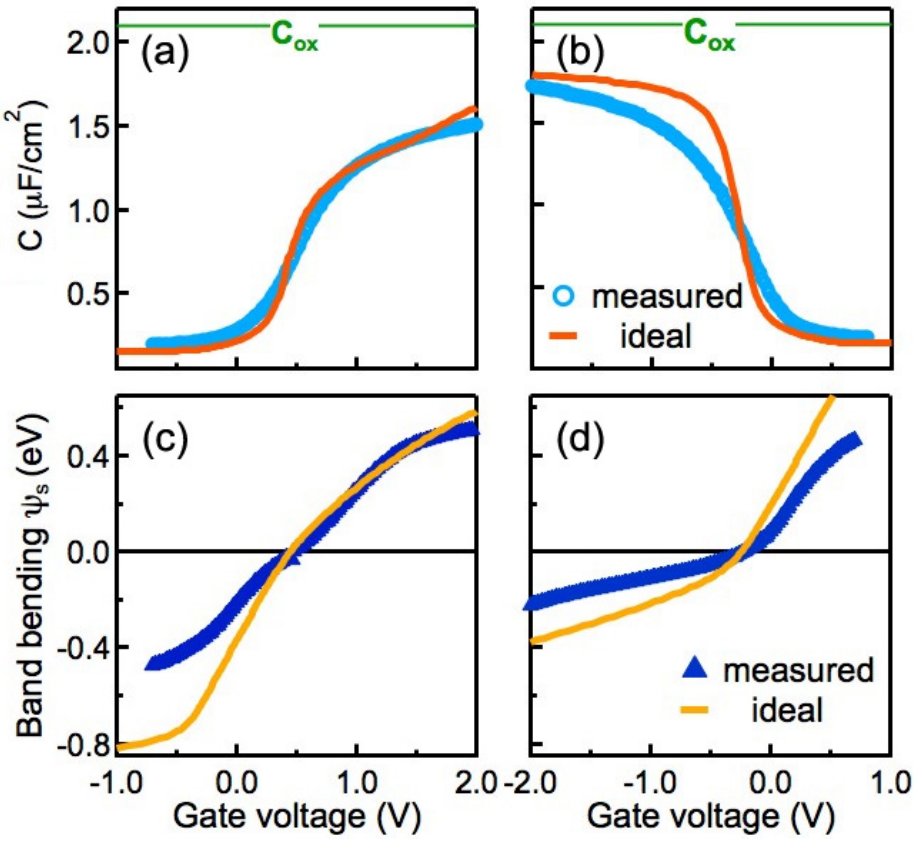

Figure 5.4: Comparison of experimental 1 MHz CV of 1.1-nm-Al_2O_3/4.5-nm-HfO_2 bilayers on (a) n- and (b) p-type $In_{0.53}Ga_{0.47}As$ MOSCAPs with calculated high frequency ideal CV. Comparison of experimental and ideal band bending, Ψ_s, and gate voltage by Terman method of (c) n- and (d) p-type $In_{0.53}Ga_{0.47}As$ MOSCAPs.

Another disagreement from the Terman method simulation of n- and p-type samples is shown in Figure 5.5. Here, D_{it} distribution is plotted against trap level position in the band gap for the bilayers MOSCAPs in Figure 5.3 from the Terman method and conductance method [127, 159]. Vertical dashed lines represent the conduction

band and valence band of $In_{0.53}Ga_{0.47}As$. From the Terman method, negative D_{it} values are extracted in the conduction band result from the crossover in n-type CV ideal and measured curves shown earlier. The D_{it} distributions from the Terman method on both n- and p-type samples display "V" shape with minimum values at different energy levels.

Comparing the minimum D_{it} position within the band gap, the lower half of the band gap shows a value of 2.2×10^{12} cm^{-2} eV^{-1} at 0.46 eV below the conduction band. This value is extracted from the D_{it} distribution of p-type sample. In the upper half of the band gap, the minimum value of 6.6×10^{12} cm^{-2} eV^{-1}, extracted from the D_{it} distribution of n-type sample, is shown at 0.23 eV below the conduction band. The higher D_{it} value for n-type arises from the fact that minimum depletion capacitance does not reach the ideal values in the Terman method. When the slope of the high-frequency CV curve in the depletion approaches zero, the Terman method is not applicable.

Considering at midgap (0.375 eV below the conduction band edge), the D_{it} value for n-type data are about three times higher than the value of p-type samples. They are found to be 5.1×10^{12} cm^{-2} eV^{-1} for p-type sample and 1.9×10^{13} cm^{-2} eV^{-1} for n-type case. The results suggest that the pre-treatment and oxide deposition may not affect the same way between n- and p-type substrate. Comparing the D_{it} distribution close to the midgap, the results from the Terman and conductance method show the same trend from both n- and p-type channels. The D_{it} values from the Terman method is higher than the D_{it} from the conductance method because D_{it} determined by the Terman method is sensitive to slow traps, while the conductance method only probes fast traps with short response times. It has been addresses as a limitation of the conductance method that for the interface with high interface trap capacitance density, the D_{it} is underestimated because the measured impedance is dominated by

oxide capacitance[122].

The results suggest that the D_{it} profile might simply be different for the two cases. The discrepancy cannot come from the oxide growth since the oxides were deposited at the same time on n- and p-type samples. For comparison, D_{it} distributions for the ∼6 nm HfO_2 MOSCAPs displays similar result (not shown). We found negative D_{it} values in the conduction band. The D_{it} distributions from the Terman method for n- and p-type samples show "V" shape within the $In_{0.53}Ga_{0.47}As$ bandgap. The minimum D_{it} positions within the band gap do not agree. The D_{it} values at midgap of n-type are almost an order of magnitude higher than p-type sample. The same conclusions can be drawn from both systems.

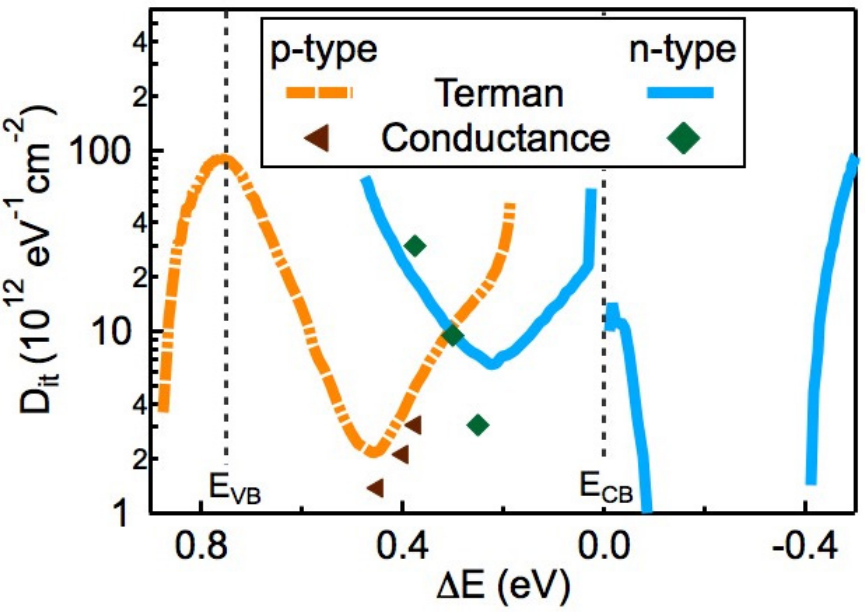

Figure 5.5: Comparison of experimental 1 MHz CV curve of the 1.1-nm-Al_2O_3/4.5-nm-HfO_2 bilayers on (a) n- and (b) p-type $In_{0.53}Ga_{0.47}As$ MOSCAPs with calculated high frequency ideal CV. Comparison of experimental and ideal band bending, Ψ_s, and gate voltage by Terman method of (c) n- and (d) p-type $In_{0.53}Ga_{0.47}As$ MOSCAPs.

In summary, the higher accumulation capacitance densities on high-k/ p-type/ $In_{0.53}Ga_{0.47}As$ than n-type samples are presented by using the novel nitrogen plasma+ TMA surface pretreatment[85]. Furthermore, differences in D_{it} distributions between n- and p-type $In_{0.53}Ga_{0.47}As$ are shown, which were consistent between the Terman method and conductance method. Based on the results from these analysis, they suggest that the Terman method has issues when applied to scaled gate stacks on n-type channel. The comparisons show differences in n- and p-type analysis are from the nature of semiconductors. The difference are density of states in the conduction band and valence band, capture cross sections of electrons and holes, and energetic asymmetries in the D_{it} distribution, which cause variation to the time constant of electron[156]. Further experiment is needed to explain physical reasons that cause these differences in the n- and p-type channels. The $In_{0.53}Ga_{0.47}As$ band parameters have to be reestimated. It is necessary to find the optimized pretreatment conditions that is specifically designed for the p-type III-V substrates for the subsequent high-k deposition.

Chapter 6

Summary and Outlook

6.1 Dissertation Summary

This section summarizes the research findings in this dissertation for the high-k/III-V semiconductors, with emphasis on surface passivation techniques. The goal for this research is to achieve highly scaled high-k/III-V gate stacks with low interface trap density that is compatible with transistor applications. The introduction to this dissertation discusses complementary metal-oxide-semiconductors (CMOS) technology based on III-V semiconductors, material challenges, and state-of-the-art surface passivations. Basic understanding of atomic layer deposition (ALD) is introduced to provide insights for high-k oxides deposition and the optimization process for scaling their thickness.

Chapter 2 describes experimental details for standard MOS capacitor fabrication and the characterization techniques. Metal-organic-precursors for ALD used in this research are introduced and the important details for *in-situ* plasma ALD are emphasized. Both electrical and chemical characterization techniques are needed to gain full understanding of the interface traps on the III-V semiconductors. Frequency dis-

persion behaviors of capacitance versus voltage curves with different frequencies are used for qualitatively determining the midgap interface trap density response. For quantitative measures, the conductance and Terman methods, are used for approximately extracting interface traps densities, D_{it}. For the chemical characterization, XPS and SIMS can be used to study the chemistry of the interfacial layer to further improve the device performance. The limitations of these techniques on III-V system are explained. In addition, the importance of annealing conditions and gate metal depositions are discussed.

In Chapter 3, the novel *in-situ* ALD surface pre-oxide deposition treatment techniques for n-type/$In_{0.53}Ga_{0.47}As$ are reported. These techniques provide high-quality interface for high-k oxides on $In_{0.53}Ga_{0.47}As$ with low midgap D_{it} and low leakage current. The techniques consist of alternative cycles of hydrogen or nitrogen plasma + metal organic precursors, including TMA and TDMAT. It is found that the number of plasma cycles and plasma power needs to be optimized specifically for different III-V substrates. The cycles of plasma is believed to remove native oxides, especially the As-oxides and sub-oxides from the III-V semiconductor surfaces, which are the origins for high trap density.

The optimized *in-situ* ALD nitrogen plasma+TMA pretreatment was used for scaling the HfO_2/n-$In_{0.53}Ga_{0.47}As$ gate stacks to sub-nm EOT thickness. The MOSCAP data shows high accumulation capacitance density of 2.5 $\mu F/cm^2$ at 1 MHz and 2 V, and D_{it} in mid 10^{12} $cm^{-2}eV^{-1}$ range. The low D_{it} values are confirmed by the low SS_{min} values of MOSFETs and TFETs, which were approaching 60 mV/dec. Furthermore, the leakage current density is low. The conductance peak movement suggested unpinned Fermi level at midgap. These optimized condition result from short plasma dose, which gives less damage to the semiconductor, and the longer pump and purge steps for better nucleation. The better nucleation is confirmed by the increase in

nucleation density, the smooth surface (< 2 nm roughness), and the good coverage of the HfO_2 film shown by SEM and AFM images. The analysis of the interface chemistry reveals Al_2O_3 and small amount of nitrogen. There is no native oxide detected, as well as As-oxide or suboxides.

Furthermore, this nitrogen plasma+TMA surface cleaning was used for further scaling of the high-k oxide. In the report, HfO_2 was replaced by ZrO_2 due to the higher dielectric constant of ZrO_2. As a result, the accumulation capacitance density reached 3.5 μF/cm^2 at 2 V and 1 MHz. The minimum midgap D_{it} value is in the low 10^{12} cm^{-2}eV^{-1} range. The SS_{min} for InAs/$In_{0.53}Ga_{0.47}As$ MOSFET is a record value of 61 mV/dec. The leakage current density is slightly higher those of HfO_2 gate stacks, but still under limit of the International Technology Roadmap for Semiconductor. The interface chemistry analysis indicates similar results to the HfO_2 gate stack, but with additional data. Since there is no overlapping peak of Zr to In and Ga like in Hf, the amount of In_2O_3 and Ga_2O_3 was quantified to be approximately 0.2 at.% and 0.5 at.%, respectively. These oxides are not detrimental to the midgap D_{it} response. There is no As-oxides, As sub-oxides, and As-As bond detected. In addition, from HAADF/STEM image, the bulk interfacial layer is mostly Al-oxide, with the presence of In-oxides close to $In_{0.53}Ga_{0.47}As$ surface.

The interfacial layer can also be scaled. The TMA precursor was replaced by TDMAT, which results in TiO_2 in the interfacial layer instead of Al_2O_3. TiO_2 increases the dielectric constant of the interfacial layer, which yield higher capacitance density in the MOSCAPs. The modified interface chemistry from Al_2O_3 to TiO_2 leads to lower frequency dispersion in accumulation. With the optimized conditions for surface pretreatment and high-k deposition, the capacitance reached 5.3 μF/cm^2 at 2 V and 1 MHz curve for $\sim$ 1 nm HfO_2/$\sim$ 3 nm ZrO_2 bilayers gate stack with 6 cycles of nitrogen plasma+TDMAT pretreatment. The minimum midgap D_{it} value

is in the low 10^{12} $cm^{-2}eV^{-1}$ range, similar to those of Al-interface gate stacks. The interfacial layer shows self-limited growth by presenting constant thickness with the increase in the pretreatment cycles. A higher number of pretreatment cycles yields higher Ti amount incorporated into the layer, resulting in higher capacitance density. The interfacial layer is mostly TiO_2, with a small amount of In_2O_3 and nitrogen. No Ga-oxides, As-oxides, As suboxides, or As-As bonding are detected. The unexpected presence of dipole layer in the interface helps maintain barrier height between oxide and semiconductor, retaining low leakage current density in the MOSCAPs.

In addition, high-k deposition on p-type $In_{0.53}Ga_{0.47}As$ was studied. Higher accumulation capacitance density for gate stacks with nitrogen plasma+TMA pretreatment on p-type $In_{0.53}Ga_{0.47}As$ compare to n-type samples were observed. The higher accumulation capacitance density is expected due to the higher density of states near the valence band than the conduction band in $In_{0.53}Ga_{0.47}As$. However, it is rarely seen because of the high D_{it}. The conductance method indicated unpinned Fermi level at midgap and low D_{it} in both n- and p-type samples. The Terman method presented some issues for the n-type samples analysis, resulting in negative D_{it} values in the conduction band. The problem arose when the gate stack is highly scaled. Different *in-situ* ALD surface passivation conditions were tested. It is concluded that p-type $In_{0.53}Ga_{0.47}As$ needs different optimized conditions than n-type substrate.

6.2 Future work

To further improve the III-V device performance, the interface chemistry of high-k gate dielectrics/III-V substrates need to be understood. XPS and SIMS present some limitations in detection limits for oxidation states of the gate stacks with III-V semiconductors. Synchrotron radiations are one of the available methods to study the oxidation states of the III-V substrates. It can enhance surface sensitivity by tuning photon energy, which can separate the binding energies that are very close together such as In 4d and Ga 3d peaks. This creates possibility to accurately identify the origin of the interface states. In addition, electron spin resonance spectroscopy (ESR) can be used to study the component of semiconductor bondings from the unpaired electrons. For III-V semiconductors, antisite defects and dangling bonds can be detected in ESR such as As^{+}_{Ga}, In and Ga dangling bonds. More studies can be done on $In_{0.53}Ga_{0.47}As$ to gain more understanding on the energy of the defects.

Moreover, XPS can be used to determine the band offset between TiO_2 and $In_{0.53}Ga_{0.47}As$ interface of both n- and p-type substrates. It can be used to focus on finding the effective band offset with different number of nitrogen plasma+TDMAT pretreatment cycles. Combining this XPS results with the dipole information on the p-type $In_{0.53}Ga_{0.47}As$ substrate, the results can provide more insights on the effect of the dipole on the band structure and further analysis on D_{it} near the band edges.

In addition, more research on the fundamental properties of the III-V materials has to be done to achieve more accurate band gap parameters. These parameters are needed for simulating the high-frequency ideal CV curve for the Terman method, as well as calculating the energy distribution of trap response time for the conductance method. Especially for the Terman analysis, the band parameters for the higher band valleys are important for the highly-scaled gate stacks. In addition, optimization of

surface cleaning on p-type $In_{0.53}Ga_{0.47}As$ is needed for achieving highly-scaled gate stacks. The *in-situ* plasma ALD nitrogen plasma+TMA can be used to achieve high quality interface between high-k oxide and p-type $In_{0.53}Ga_{0.47}As$. Additional experiments can be done to study contribution of dipole on p-type $In_{0.53}Ga_{0.47}As$. It can provide more information on the difference in oxide capacitance when comparing the fitting between n- and p-type substrates.

Appendix A

Forming Gas Anneal Protocol

A.1 Procedure for Annealing in Quartz Tube Furnace

Forming gas: 5% H_2 95% N_2

Additional precautions:

- Wear a fire retardant lab coat.
- Only start flowing gas in when the furnace is cool.
- Turn on the forming gas before loading samples.
- Use plastic gloves inside heat-proved gloves when handling end cap of glass tube.
- Keep the forming gas flow when unloading.

Procedures

1. Check the fume hood following the fume hood usage guide. Always work with the sash at or below the level of the red arrow sticker.

2. Turn on the main switch of the furnace and check the temperature.
3. Only continue if the furnace is cool.
4. Turn on the forming gas by,
   (a) Turn on the main cylinder valve
   (b) Turn on the gauge valve
   (c) Check the forming gas is not empty
   (d) Adjust the flow meter to ∼5 on the scale
   (e) Wait for 5 min.
5. Remove furnace end cap.
6. Using plastic gloves, load samples on to the center of a glass carrier and use a glass rod to push to carrier to the center of the tube.
7. Replace the furnace end cap.
8. Adjust temperature controller of the furnace to the desire temperature. (The ramping rate is 10 °C/min.)
9. Start timing.
10. After the time is done, adjust the temperature controller to the minimum (10 °C).
11. Wait until the temperature read below 60 °C.
12. Using heat-proved gloves, remove the end cap and pull the boat back from the center using the glass rod.

13. Replace the end cap and wait 5 min to allow wafers to cool down before they are exposed to air on removal from the furnace.

14. Remove the end cap and unload the carrier and the wafers.

15. Replace the carrier and the end cap.

16. Turn off the forming in the reverse order:

    (a) Adjust the flow meter to 0 on the scale

    (b) Turn off the gauge valve

    (c) Turn off the main cylinder valve

17. Turn off the main switch of the furnace.

18. Record the use in the logbook.

Appendix B

Test Conditions for Optimizing Pretreatment of *p*-InGaAs

B.1 Optimizing Pre-Treatment Conditions for *p*-Type InGaAs

n is n-type InGaAs, p is p-type InGaAs, and α is accumulation dispersion.

Table B.1: Tested Pretreatment Conditions for p-InGaAs

Recipe	**Plasma type**	**Precursor**	**no. cycles**	**High-k**	**no. cycles**	**t_{ox}** (Å)	**Note**
B	N	TMA	9	HfO_2	40	38	higher C_{acc} n, high α
B	N	TMA	9	ZrO_2	40	38	higher C_{acc} n, high α

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Table B.1 – Tested Pretreatment Conditions for *p*-InGaAs

Recipe	**Plasma type**	**Precursor**	**no. cycles**	**High-k**	**no. cycles**	**t_{ox} (Å)**	**Note**
pn1 (B)	N	TMA	13	HfO_2	50	47.9	slightly higher C_{acc} p, high α
pn2 (A)	N	TMA	13	HfO_2	50	51.8	similar C_{acc}, thicker film
pn3 (A)	N	TMA	13	HfO_2	50	53.81	similar C_{acc}, thicker film
pn4 (B)	N	TMA	15	HfO_2	50	50.02	similar C_{acc}, high α
pn5 (A)	N	TMA	15	HfO_2	50	58	similar C_{acc}, thick film
pn6	N+Ar 20 sccm	TMA	15	HfO_2	50	50.37	similar C_{acc}, high α (similar to pn4)
pn7	N:H 20:5	TMA	15	HfO_2	50	50	higher C_{acc} n, high α (bad p)
pn8	N 3 s	TMA	9	HfO_2	50	53.1	similar C_{acc}, high α (similar to pn4)

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Table B.1 – Tested Pretreatment Conditions for *p*-InGaAs

Recipe	**Plasma type**	**Precursor**	**no. cycles**	**High-k**	**no. cycles**	**t_{ox}** (Å)	**Note**
pn9	N 5 s	TMA	9	HfO_2	50	48.5	higher C_{acc} n, high α (bad p)
pn10 (B)	N	TMA	9	Al_2O_3/ HfO_2	3/40	40.52	higher C_{acc} n, high α
pn11 (B)	N	TMA	9	Al_2O_3/ HfO_2	3/35	36.04	higher C_{acc} n, high α
pn12 (B)	N	TMA	9	Al_2O_3/ HfO_2	5/45	47.78	slightly higher C_{acc} n
pn13 (B)	N	TMA	9	Al_2O_3/ ZrO_2	5/45	46.61	higher C_{acc} n, high α (bad p)
pn14	N (after) 400 W	TMA (before)	3	HfO_2	50	45.47	higher C_{acc} n, high α

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Table B.1 – Tested Pretreatment Conditions for *p*-InGaAs

Recipe	**Plasma type**	**Precursor**	**no. cycles**	**High-k**	**no. cycles**	**t_{ox}** (Å)	**Note**
pn15	N (after) 250 W	TMA (before)	5	HfO_2	50	46.04	higher C_{acc} n, high midgap D_{it}, pinned both type, high α p
pn16	N	TDMASi	9	HfO_2	50	46.87	higher C_{acc} n, high α
pn17 (B)	N	TMA	9	HfO_2	50	46.86	$(NH_4)_2S$ wet clean 10 min, bad n, higher C_{acc} n, ok p, high α
pn18	N	TDMASi	20	HfO_2	50	44.53	low C_{acc}, high α
pn19	N	TDMASi	14	HfO_2	50	43.66	higher C_{acc} n, high D_{it}, high α

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Table B.1 – Tested Pretreatment Conditions for *p*-InGaAs

Recipe	**Plasma type**	**Precursor**	**no. cycles**	**High-k**	**no. cycles**	**t_{ox} (Å)**	**Note**
pn20	H 3 s	TMA	9	HfO_2	50	43.78	higher C_{acc} n, high D_{it}, high α
pn21	H 3 s	TMA	9	HfO_2	50	46.24	higher C_{acc} n, high D_{it}, high α
pn22	N	TDMASi	5	HfO_2	50	41.75	lost n, high α
pn23	O (after)	TDMASi (before)	3	HfO_2	50	42.44	high D_{it} n, lost p
pn24	N 2 s	TMA	13	HfO_2	50	61.65	T_{dep}=200°C, higher C_{acc} n
pn25	N 2 s	TMA	9	HfO_2	50	54.44	T_{dep}=200°C, higher C_{acc} n
pn26	N	TDMASi	11	$Hf0_2$	50	44.03	higher C_{acc} n, high α
pn27	N	TMA	11	HfO_2	50	55	T_{dep}=200°C, similar C_{acc}

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Table B.1 – Tested Pretreatment Conditions for p-InGaAs

Recipe	**Plasma type**	**Precursor**	**no. cycles**	**High-k**	**no. cycles**	**t_{ox}** (Å)	**Note**
pn28	N	TMA	9	HfO_2	45	49.93	T_{dep}=200°C, higher C_{acc} n, high α
pn29	N 4 s	TMA	5	HfO_2	45	48.13	T_{dep}=200°C, higher C_{acc} n, high α
pn31	N	TDMAT	13	HfO_2	45	47.56	High D_{it}, higher C_{acc} n, high α
pn32	N	TDMAT	15	HfO_2	50	47.47	High D_{it}, higher C_{acc} n, high α

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