Integrated Multi-spectral Non-Mechanical Light-Detection-and-Ranging Beam Steering Devices and Systems Using Optical Phased Array

By

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ABSTRACT

Optical phased arrays (OPAs), by controlling the phase and/or amplitude of optical emitter structure (e.g., grating coupler, 45-degree vertical coupler), have been widely used in applications such as light detection and ranging (LIDAR), imaging, and free-space communication systems. OPAs in the mid-wave infrared (MWIR) and long-wave infrared (LWIR) regime, therefore, will be a good candidate for realizing thermal or gas-sensing, LIDAR with a lower level of turbulence. Here, based on our previous work, we propose an integrated non-mechanical OPAs-based beam steering system using a germanium-silicon optical platform. In the functional device part, we utilize vertical germanium via emitter and grating emitter arrays at MWIR and LWIR, respectively. Also, considering the fabrication complexity, we are now demonstrating a phase-change-material (PCM) assisted grating emitter to realize MWIR beam steering. Besides, we collaborated with AIM Photonics, demonstrating a large-scale lateral emitter array by foundry-based fabrication.

For the light source part, Quantum Cascade Lasers (QCLs) are the only electrically pumped semiconductor light sources that can operate at room temperature over the entire MWIR/LWIR spectral range. We collaborate with other research groups and a commercial company to grow QCL wafers We design the III-V material QCL laser integration part with the germanium-silicon platform, to guarantee the good mode transition between III-V mesa and germanium waveguide. The integrated process will rely on the emerging micro-transfer-printing technology. We have already made some testing preparation work for this fabrication process.

Acknowledgments

Special thanks to Professor S. J. Ben Yoo for his guidance and support.

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The simulation work of Ge vertical emitter design is conducted by Yi-Chun Ling and is based on Mathias Prost and Semih Cakmakyapan's foundation. Thermal simulation of integrated laser/waveguide structure is conducted by Dr. Jay Kim. Many thanks to them.

Many thanks to Yichi Zhang and Yi-Chun Ling for their patience during our corporation. I learned a lot from them.

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CONTENTS

Chapter 1

Introduction

Optical beam steering technology has broad application prospects in many directions, including free-space optical communications (FSOC)[1], imaging[2], and light-detection-and-ranging (LIDAR)[3]. Most traditional beam-steering devices and systems rely on the optomechanical movement of mirrors and lenses. These systems are expensive, relatively slow, which limits their use to static, ground-based deployment. Recently, people make efforts to miniaturize such systems by using micro-electromechanical mirrors (MEMS) and liquid-based-based devices and technology[4]. However, these technologies still have a limitation on scanning and tuning speed. Considering these background, solid-state optical beam steering based on optical phased arrays (OPAs), with advanced photonic integrated circuits (PICs) design, draw researchers' attention and they have great potential in enabling fast, reliable, and cost-effective devices and systems. Figure 1 shows a conceptual OPA-based beam-steering device using grating emitters[5].

Current OPA-based beam steering devices are mainly focused on visible light and optical communication band[6], [7], [8], [9], Extending the working range into the MWIR/LWIR can make such beam-steering devices attractive for FSOC, remote sensing[10] and navigation applications, with lower sensitivity to atmospheric turbulence and scintillation [11], [12]. On the other hand, the longer wavelength will help to relax the half-wavelength pitch requirements of adjacent emitters in a phased array, for sidelobe-free beam steering and reduction of fabrication complexity[13]. In such MWIR/LWIR PICs design, germanium (Ge) is considered a good

candidate because of its large transparency window, compared with other materials, from 2 μm to 14 μm[14]. Besides, compared to silicon, also a low-loss material at MWIR/LWIR, Ge has the advantage of the larger refractive index, thermo-optic coefficient[15], and higher carrier mobility[16]. It means Ge-based devices could achieve smaller footprints and better performance when integrated with electronic parts.

In our previous work, we demonstrated a proof-of-concept beam steering device using germanium-silicon (Ge-Si) PICs with grating emitter arrays around 4.6 μm wavelength[17]. Here, in Chapter 2, we describe the several directions we are working on to realize the new OPA-beaming steering devices at MWIR/LWIR. Section 2.1 is the background introduction of the OPA-based beam steering device principles. In Section 2.2, we provide the plan to demonstrate the MWIR OPA-based, electronically controlled beam steering device by using three-dimensional (3D) vertical Ge via emitter arrays. Its advantage is that we can put an active transistor matrix to independently control the phase of each emitter and expand the beam steering angle greatly, though the fabrication process is relatively complicated. We also collaborated with AIM Photonics, trying to demonstrate a large-scale emitter array by using foundry-based fabrication technology, which is shown in Section 2.3. On one hand, we could utilize the fabrication resource provided by the foundry, exploring the mass production possibility on this function beam steering device. On the other hand, we also need to make some compromises on the customized design, due to the material platform provided by the foundry. Meanwhile, we also make efforts on the traditional two-dimensional (2D) beam steering device. In Section 2.4 and 2.5, we introduce the PCM-assisted MWIR 2D grating emitter beam steering device, and the traditional thermo-optical phase-tuned LWIR 2D grating emitter beam steering device,

respectively. The traditional 2D grating beam steering relies on tuning the light source wavelength and the phase of each emitter simultaneously and the beam steering angle range will be seriously limited. However, its advantage is the fabrication process flow is relatively mature. We could use this relatively easy demonstration as the foundation for our future work. In this chapter, I mainly contributed to the design of the MWIR vertical emitter beam steering devices fabrication process, the design, and layout of foundries-based MWIR beam steering devices, the design and test fabrication of PCM-assisted MWIR beam steering devices, and the test fabrication of the LWIR beam steering devices.

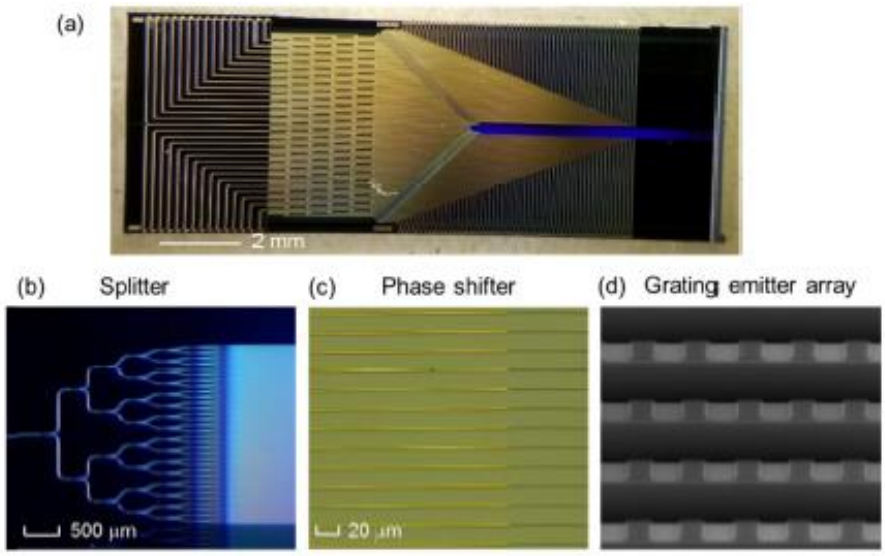


Figure 1. Schematic of an OPA photonic integrated circuit (PIC) based on grating emitters for two-dimensional beam steering[5].

The future application scenarios (e.g., autonomous-drive navigation, remote-sensing) typically require the beam-steering devices to be compact and light source alignment-free. Therefore, we hope to integrate the light source and amplifier part with our functional beam-steering emitter array in the same photonic integrated circuit (PIC). In MWIR and LWIR, the quantum cascade laser (QCL) is undoubtedly the best candidate for our devices, since it is the only electrically

pumped semiconductor light source that can operate at room temperature over the entire mid-IR and long-IR spectral range[18], [19], [20], [21]. In Chapter 3, we investigate the hybrid III-V laser and Ge waveguide structure in our integrated systems. To make sure the good mode transition happens, multiple-layer tapers are used in the integrated structures on both laser material layers and the Ge layer. The mode existing in the laser core region and Ge waveguide region are analyzed. Besides, we propose the micro-transfer-printing, one of the state-of-the-art fabrication technologies[22], to bond our QCL region on top of the Ge waveguide part. In this chapter, I mainly contributed to the design, simulation, and layout of the hybrid laser-waveguide structure, also with the test fabrication steps for the transfer-printing-based QCL device.

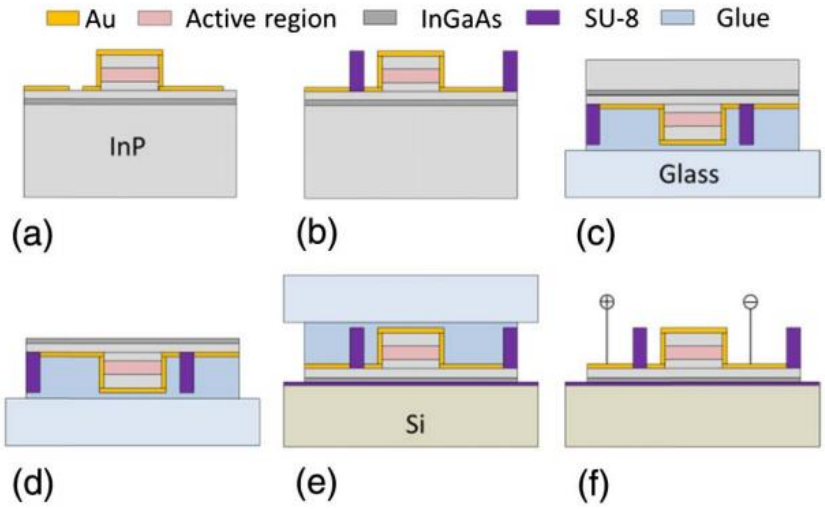


Figure 2. Example transfer-printing process for fabrication of integrated laser-waveguide structure[22]

Chapter 2

OPA-based beam steering devices in MWIR and LWIR

2.1 OPA-based beam steering device principles

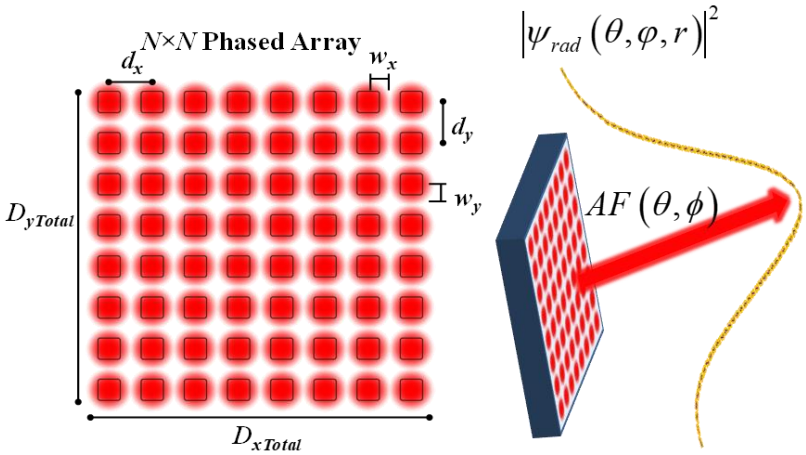


Figure 3. Schematic of an $N \times N$ phased array of emitters with mode size w_x and w_y, array pitch d_x and d_y, and total size $D_{xTotal} \times D_{yTotal}$. The output beam profile is determined by the product of a single element radiation pattern Ψ_{rad} and array factor AF.

Optical phased arrays (OPAs) can enable non-mechanical beam steering through the phase control of each emitter. Figure 3 illustrates the design of an emitter aperture with mode size w_x and w_y, and the arrangement of an emitter array with a pitch d_x and d_y. The radiation pattern Ψ_{rad} for single emitter can be determined by

$$\Psi_{rad}(\theta,\varphi,r) \propto \frac{e^{ikr}}{r}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\Psi_0(x,y)\,e^{ik\sin\theta(x\cos\phi+y\sin\varphi)}dxdy \quad (1)$$

Ψ_0 is the normalized radiation pattern. Then the array factor AF can be calculated:

$$AF(\theta,\phi) = \frac{sin\left[\frac{\pi N d_x}{\lambda}(sin\,\theta - sin\,\theta_0)\right]}{sin\left[\frac{\pi d_x}{\lambda}(sin\,\theta - sin\,\theta_0)\right]} \times \frac{sin\left[\frac{\pi N d_y}{\lambda}(sin\,\phi - sin\,\phi_0)\right]}{sin\left[\frac{\pi d_y}{\lambda}(sin\,\phi - sin\,\phi_0)\right]} \quad (2)$$

N is the number of emitters and the emitter array is along the axis (θ_0, ϕ_0). The θ_0, ϕ_0 here is the axis of the emitting beam steering direction along with *x* and *y* of the phased array plane, respectively. The total field of the array is equal to the product of the radiation pattern Ψ_{rad} for a single element and the array factor AF. Therefore, the total pattern can be controlled via the single element pattern Ψ_{rad} or AF. While designing an OPA, we need to consider the requirements for the total field of view (TFOV), instantaneous field of view (IFOV or beam width), and sidelobe suppression. Here, the TFOV, which is the largest angle that OPA can steer to, is limited by the appearance of sidelobes, and the IFOV is inversely proportional to the number of emitters N.

Figure 4 shows one example of two far fields for beam steering, comparing two situations where the emitter pitch is (a) greater than half of the wavelength and (b) less than half wavelength, as the phase difference between adjacent emitter is tuned to 0, 0, 5π, and 0.9π, respectively. When the emitter pitch is greater than half wavelength, the occurrence of unwanted sidelobes will limit the TFOV and waste energy.

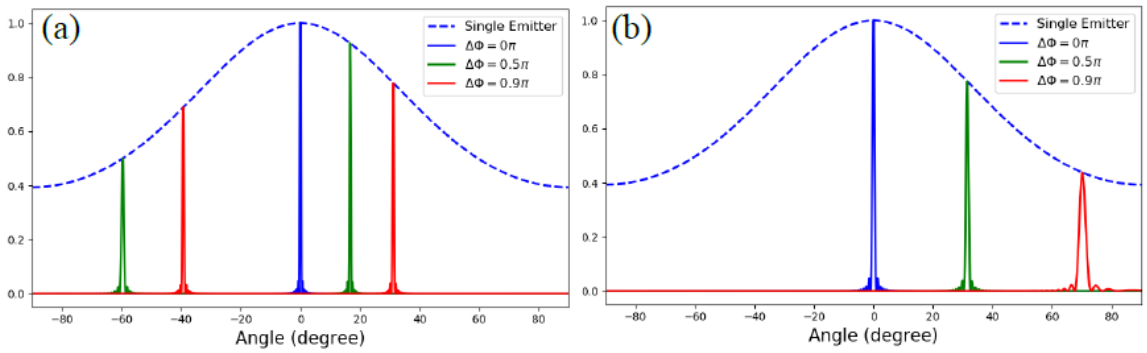


Figure 4. Simulated angular intensity distribution in the far-field for the phased array with N=128, $w_x = w_y = 1$ μm, and (a) $d_x = d_y = 4.5$ μm and (b) $d_x = d_y = 2.2$ μm as the phase difference $\Delta\phi$ between adjacent emitters is tuned to 0, 0,5π, and 0.9π at the wavelength of 4.6 μm.

2.2 MWIR beam steering devices using vertical emitter

Inspired by our previous work on MWIR grating-emitter-based beam steering devices[17] and U-shaped vertical optical coupler[23], we propose a new design of MWIR beam steering devices based on 3D Ge 45-degree vertical emitter arrays. Figure 5 shows the schematical illustration of our target large-scale OPA, integrated with the electronic control units. In each row of the array, the light propagated in the bus waveguide will be gradually coupled to the 45-degree Ge via, emitting the light vertically upward. In this phased array, each emitter is contacted with a control line and a data line, and the array will be contacted with a large-scale active electronic active transistor matrix. By control the current injected into each vertical emitter, theoretically, we can achieve individual phase control for each element in the OPA.

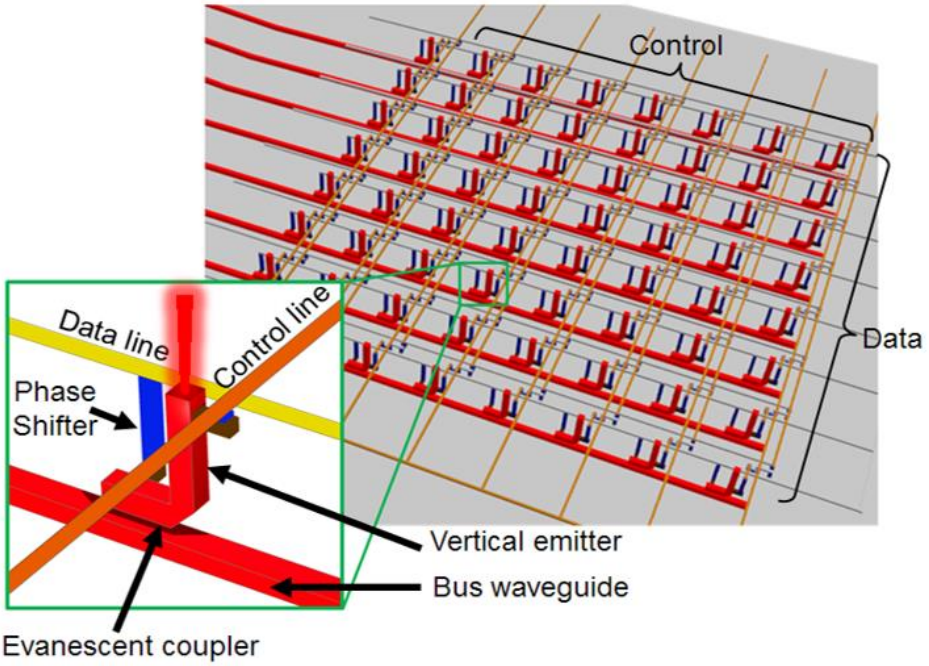


Figure 5. Schematical illustration of large-scale OPA using Ge vertical emitters, realizing individually phase tuning.

In traditional 2D beam steering OPA using grating emitters, the steering angle along the grating direction (beam propagation direction) will rely on input light wavelength tuning. In our design, due to the independently tuning of each 3D vertical emitter, we do not need the wavelength tuning and the beam steering angle will be expanded greatly.

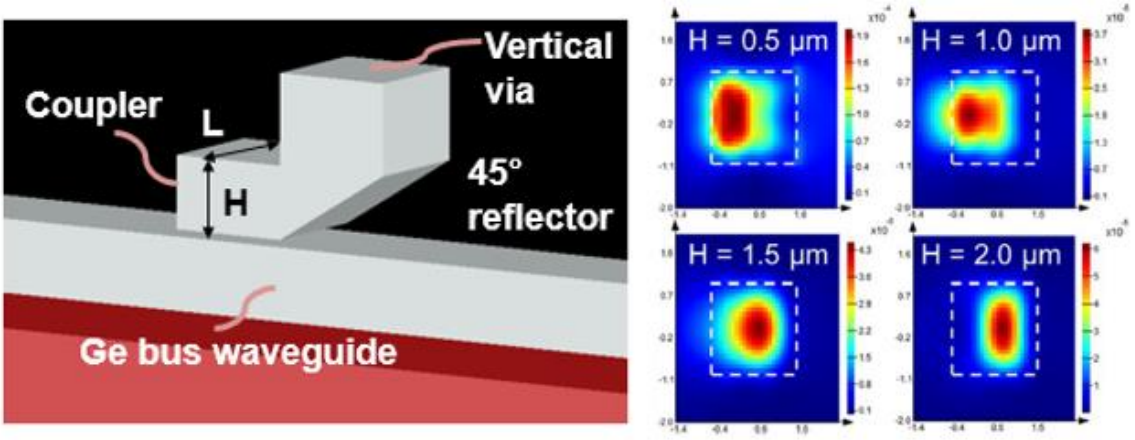


Figure 6. Left: 3D model of single Ge vertical emitter at MWIR. Right: emitting upward mode profile under different coupling waveguide height.

Figure 6 shows the upward emitting mode under different evanescent coupler heights. The width in the lateral dimension, L, is 2 μm. We can see when the H is 2 μm, the mode will be confined well in the vertical via. Figure 7 shows a row of vertical emitters design and the coupling efficiency dependence on coupler length and gap.

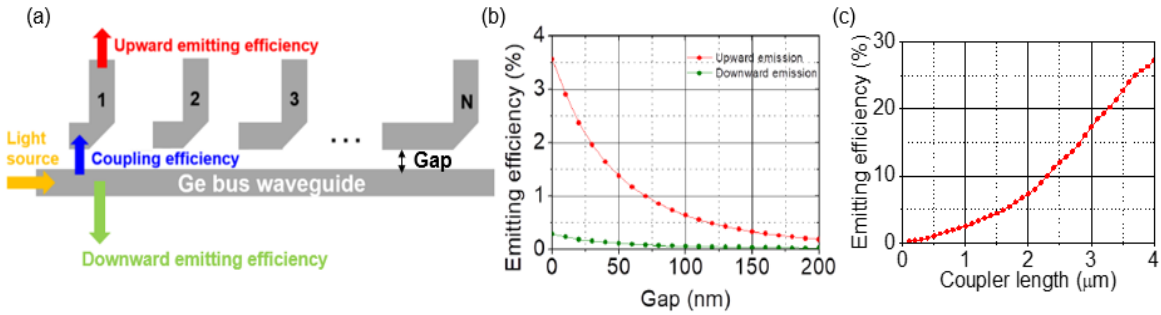


Figure 7. (a) Layout of the power feeding network where the optical power in the bus waveguide is uniformly coupled into N vertical emitters through evanescent waves; (b). Emitting efficiency as a function of the gap between coupler and the bottom bus waveguide; (c) Coupling efficiency as a function of coupler length for the vertical emitter.

Figure 8 shows the field intensity distribution of a whole uniform power-feeding system with 32 vertical emitters. ΔL in the figure means the difference on the emitter coupler length. From the side view, the light propagating inside the bus waveguide is fed into each vertical emitter and gradually decreases along with the emitter array as we expected. The top view also demonstrates a very uniform emission from all 32 elements.

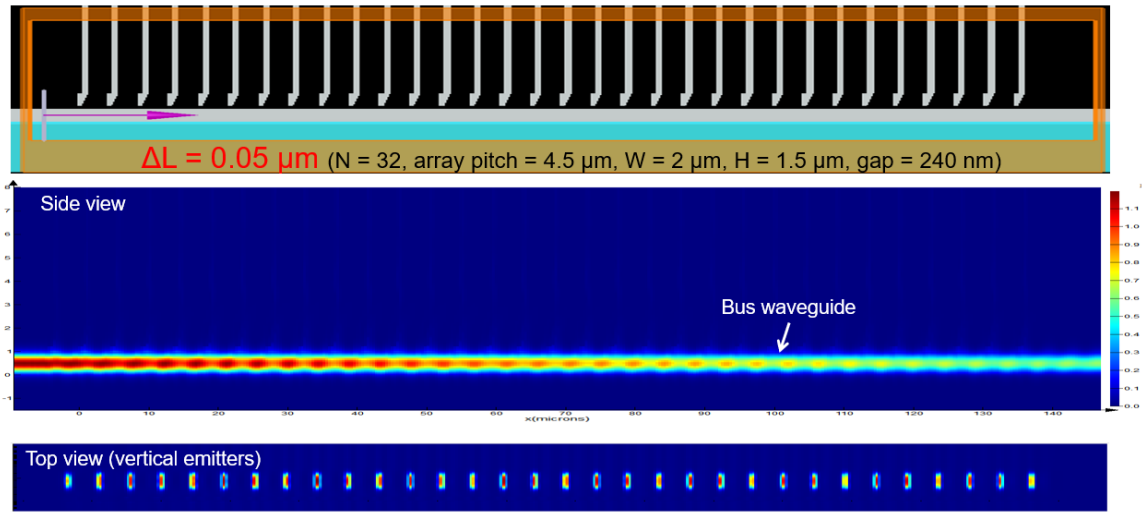


Figure 8. FDTD simulation model of a row of 32 vertical emitters, along with side and top view of the 2D field intensity distribution for the whole power-feeding network system.

Based on our vertical emitter and uniform power emitting system design, we propose a fabrication process of the 3D vertical emitter array structure, which is shown in

Figure 9. The fabrication starts with the two silicon wafers with crystalline Ge layers. (1) The Ge- on-silicon wafers will receive silicon nitride layer deposition to balance the stress and reduce the bowing of the wafers. This is because the Ge-on-Si wafer suffers from a high bowing induced by the stress from the Ge layer growth. During this step, we deposit plasma-enhanced chemical vapor deposition (PECVD) SiN at the backside of the wafer to balance the stress. (2) The pre-alignment mark (PM) is then patterned on top of the wafer by lithography and etching. (3) After the fabrication of the bottom waveguide layer, (4) high-density plasma chemical vapor deposition (HDPCVD) SiN is deposited on top of the Ge followed by a CMP. (5) The second Ge layer is fabricated on top of another Ge on Si wafer. (6) A PM and a reversed PM are patterned on wafer II for guiding the alignment before and after the wafer bonding, respectively. (7) After the fabrication of the waveguide layer on the wafer II, (8) a 45-degree slope is fabricated on top

of the waveguide block using a tilted ion-beam-etching and vertical ion-beam-etching. (9) Then HDPCVD SiN is deposited and planarized for wafer bonding. (10) Wafer bonding will bond the two wafers with silicon nitride layers facing each other, and the silicon substrate of the wafer II will be removed by lapping and then chemical selective etching. (11) HDPCVD SiN deposition and CMP achieve planarization. (12) The vertical via patterning and etching will open windows for Ge emitters. (13) Ge chemical-vapor-deposition allows filling Ge into windows open in SiN to form vertical Ge emitters. (14) An inverse etcher is performed before CMP because of the low polishing rate on the Ge layer. (15) The metal via 1 etching, (16) metal deposition, (17) Metal via 2 etching, and (18) metal deposition completes the 3D OPA fabrication. A thermal phase shifter made of metal will be fabricated on top of the Ge waveguide to enable phase tuning when the current is applied.

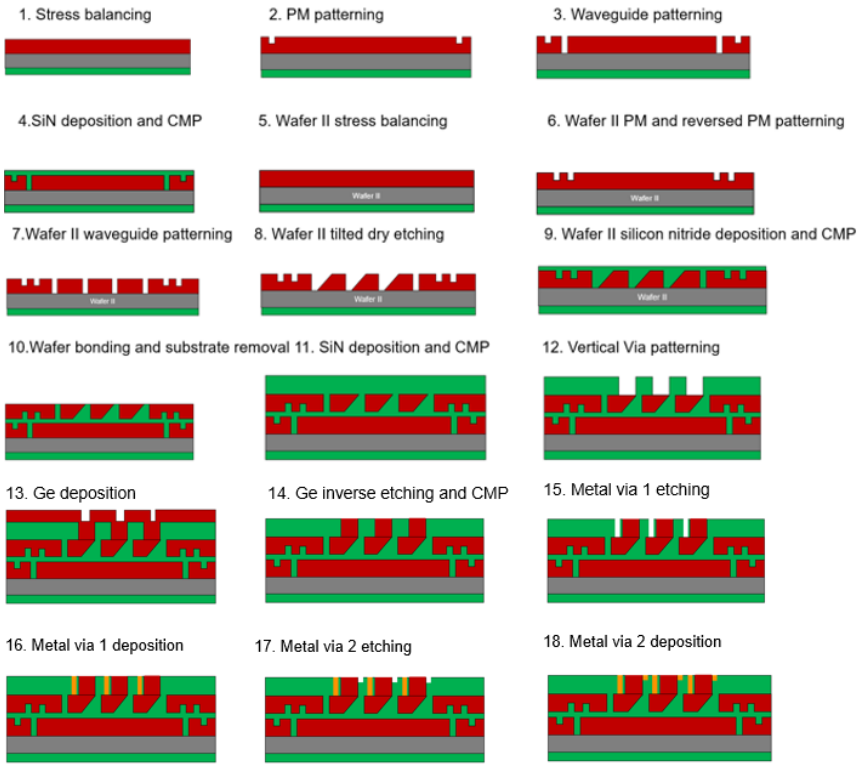


Figure 9. The fabrication process for the Ge vertical emitter structure

Considering the process possibility, based on our fabrication experience, we develop a backup plan for the 3D vertical emitter structure. The process flow is shown in Figure 10 (a). Here, the small ladder shape reflectors fabricated by 45-degree ion beam etching or focused beam etching reflect a certain proportion of energy to the top of the chip. Step 1-4 PM and waveguide layer patterning in the new 3D OPA are the same as those of the previous 3D OPA. The ladder shape reflector is patterned by 2 steps of etching. First, a rectangular etching trench is etched using traditional plasma etching. Then the 45-degree slope is fabricated using 45-degree ion beam etching or focused beam etching. Vertical vias are then fabricated before the reflector to guide the reflected wave. Figure 10 (b), (c) shows successfully fabricated 45-degree reflectors on Ge-on-Si waveguides using focused-ion-beam etching at 45 degrees.

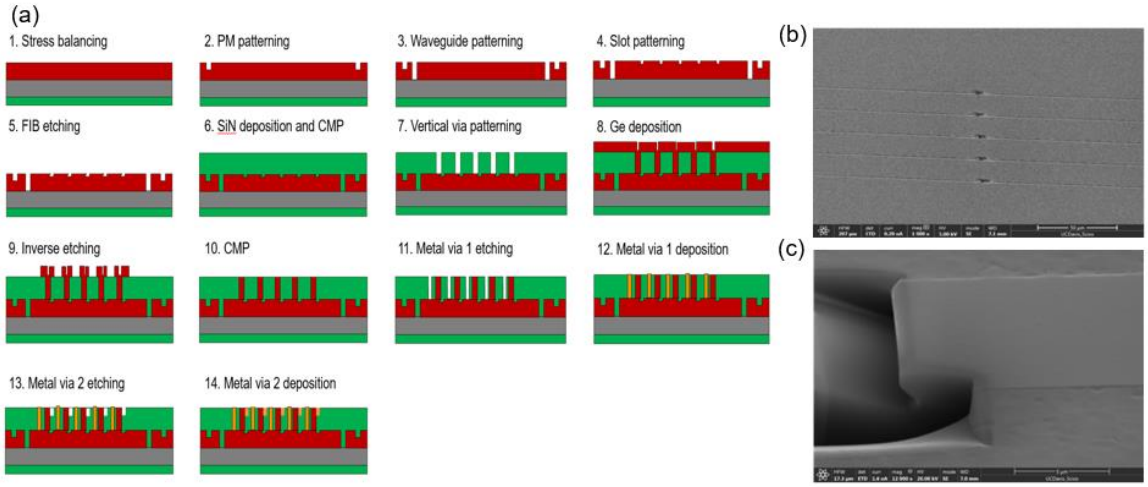


Figure 10. (a) The fabrication process of the backup simplified the new 3D vertical structure OPA. (b), (c) 45-degree reflectors etched by focused-ion-beam etching on Ge on Si waveguides.

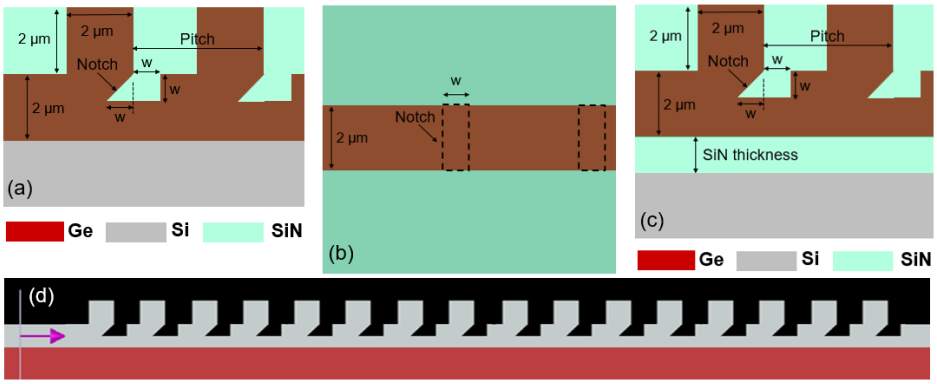


Figure 11. (a) The side view and (b) the top view of the layout for a single layer waveguide array. (c) The side view of the layout with the SiN layer. (d) The layout of a power feeding network using a single layer waveguide array.

Figure 11 illustrates the schematic of a Ge single-layer waveguide array on Si substrate. Here, a notch structure with a 45-degree-angle is utilized to feed the light into a via structure on the top. In the simulation, a transverse magnetic (TM) polarized 4.6 μm light source was applied to characterize the optical properties of the designed structure. Due to the low index contrast between the Ge and the Si layers, we also simulate another design with a SiN layer as shown in Figure 11 (c), which can increase the index contrast to improve the upward emitting efficiency. In the following discussion, we simulated a row of vertical emitters to check the global behavior of the system as shown in Figure 11 (d).

For a reasonable simulation time, we limited the number of elements to 16. After considering the arrangement for the phase control circuit and the fabrication constraints, we set the pitch for the single waveguide array to 10 μm and the notch width to 200 nm. The reason the notch is larger than the wavelength is that we also need to consider the crosstalk and the fabrication complexity. A 2 μm via length was chosen as the same as the previous design. Figure 12 (a) and (b) shows the simulated results for the field intensity distribution. To further improve the upward emitting efficiency, we put a SiN layer under the Ge layer to increase the index contrast and investigate

the change of the emitting efficiency. Figure 12 (c) and (d) shows that the downward emitting light can be significantly eliminated, and we can achieve 32.76 % upward emitting efficiency while the downward emitting efficiency is 18.77 %.

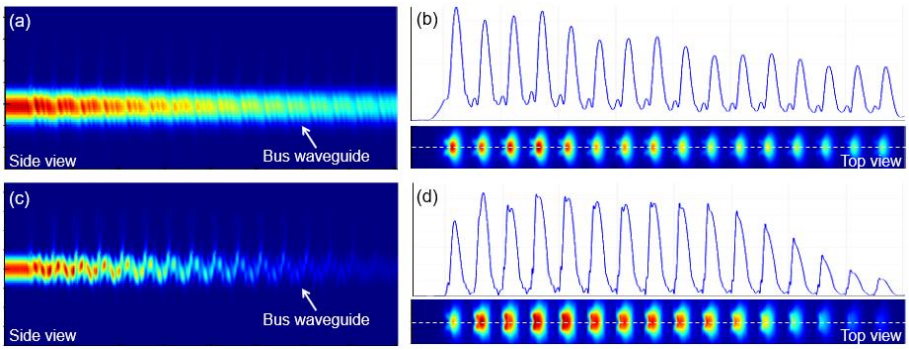


Figure 12. Two-dimensional field intensity distribution for the whole power-feeding network system. (a) The top view and (b) the side view without the SiN layer. (c) The top view and (d) the side view with the SiN layer

2.3 Foundries-based lateral emitter beam steering devices in MWIR

When we explore the proof-of-concept OPA beam steering devices using Ge 45-degree vertical emitters, we also collaborate with AIM Photonics, using the mature fabrication resources in the foundry to demonstrate the individually-phase-controlled emitter array in MWIR. Figure 13 shows the layer information we get from the AIM foundry and the mode support situation of the Ge waveguide, including the propagation and bending loss of the Ge waveguide dependence on waveguide width.

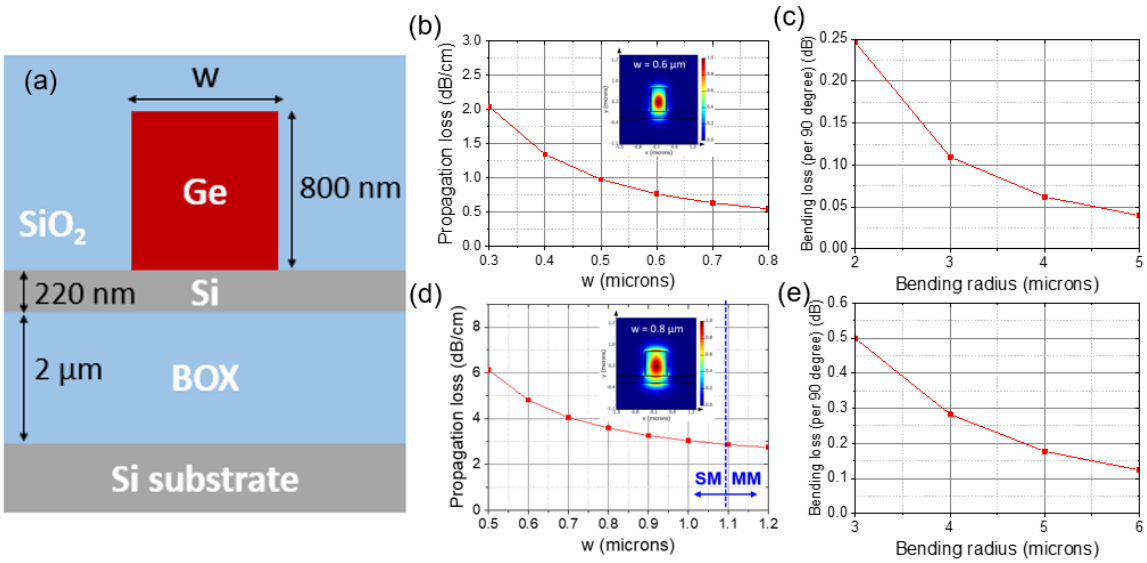
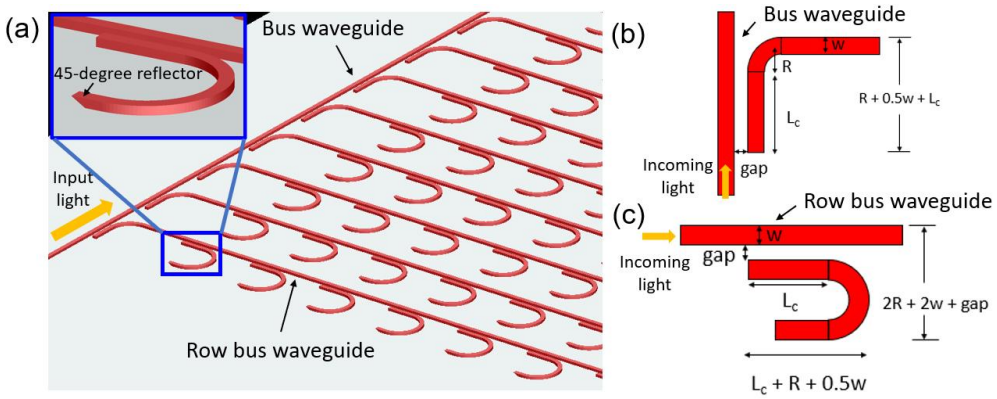


Figure 13. (a) Single-mode waveguide design based on AIM Photonics Foundry Ge and Si layer thickness. (b) Propagation loss dependence on width of the Ge waveguide at $\lambda = 3.8$ µm (inset: 2D mode profile when W = 0.6 µm). (c) Bending loss as a function of the bending radius of the Ge waveguide at $\lambda = 3.8\ \mu m$ when W = 0.6 µm. (d) Propagation loss dependence on width of the Ge waveguide at $\lambda = 4.6$ µm (inset: 2D mode profile when W = 0.8 µm). (e) Bending loss as a function of the bending radius of the Ge waveguide at $\lambda = 4.6$ µm when W = 0.8 µm.

Based on the layer thickness in the AIM foundry Ge/Si platform, we propose the large-scale (128 by 128) OPA lateral emitter array using Ge 45-degree reflector. Figure 14 shows the diagram of the whole emitter array and the corresponding bus-to-row waveguide and row-to-unit emitter coupling region.



(d)

Parameter	Value ($\lambda = 3.8\mu m$)	Value($\lambda = 4.6\mu m$)
w	0.6	0.8
gap	0.5	0.75
R	2.0	4.0
Lc	Depends on row/column index	

Figure 14. (a) Schematical illustration of the large-scale (128 by 128) OPA lateral emitter array using Ge 45-degree reflector. (b) Bus-to-row waveguide coupler design illustration. (c) Row-to-emitter-unit coupler design illustration. (d) Parameter sets of evanescent coupler design in (b) and (c) for uniform power-feeding to each emitter at λ=3.8 and 4.6 μm.

The coupler length varies as the different row and column index, to achieve uniform power feeding to each emitter, which is shown in Figure 15. As the index on each row/column increases, the beam intensity propagating will decrease gradually by splitting power to the previous row waveguide or emitters. Then the coupler length needs to be longer compared with previous ones. The coupling efficiency for a single evanescent coupler will increase to compensate for the decreasing power propagating in the bus/row waveguides.

Ultimately, we still want to achieve the individual control of phase in each emitter element in this 128-by-128 OPA. In this foundry-based design, we will use a bipolar junction transistor (BJT) to control the injection current to each emitter. Figure 16 gives the schematic diagram of the BJTs along with the emitter array. Part of the germanium layer will be doped as the load resistance used in the electronic circuit. Part of the silicon layer will be doped by different layers

and types to form the BJT structures. Figure 17 shows the lateral emitter unit connected with the detailed BJT structure and the mask layout of the whole 128 × 128 lateral-emitter-based OPA.

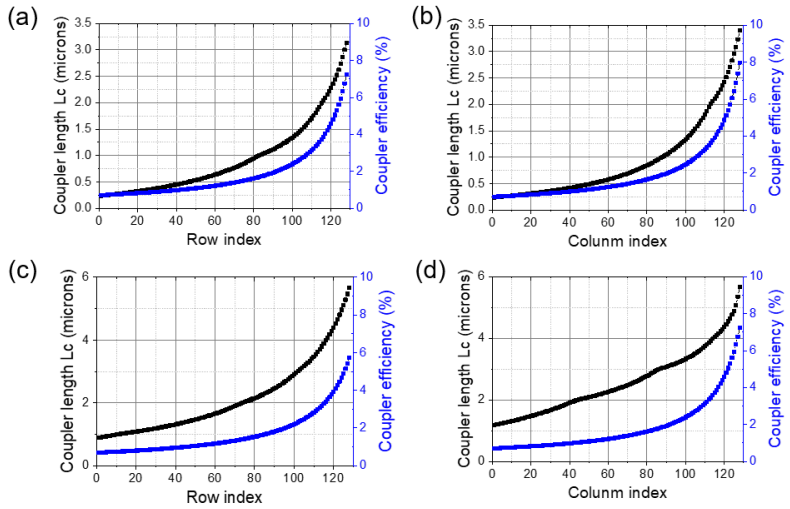


Figure 15. The coupling efficiency (Blue), and coupler length for the (a) bus-to-row couplers and (b) the row-to-unit couplers in the 128×128 OPA at λ = 3.8 μm, and the same dependence on row/column index at λ = 4.6 μm.

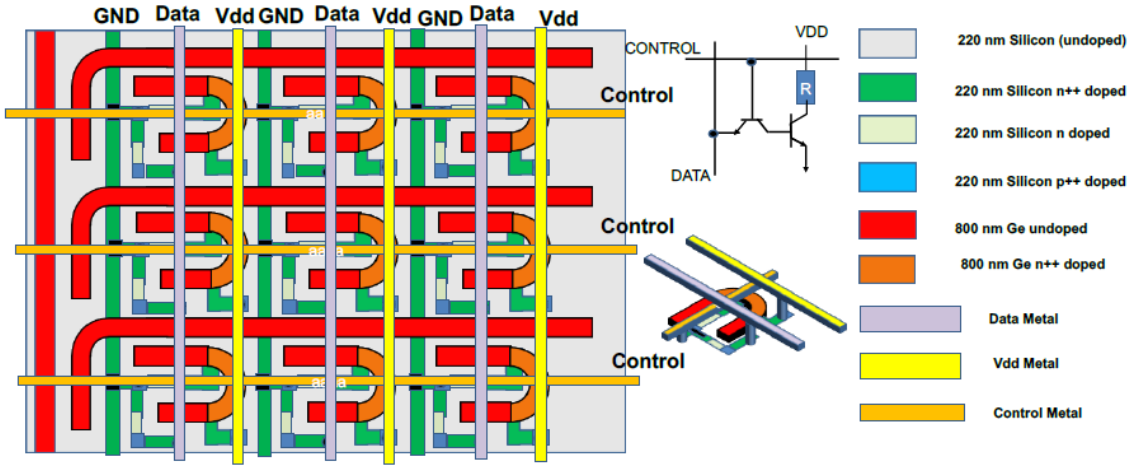


Figure 16. Schematic diagram of 128 × 128 emitter array based on AIM Photonics PDK with bipolar junction transistors

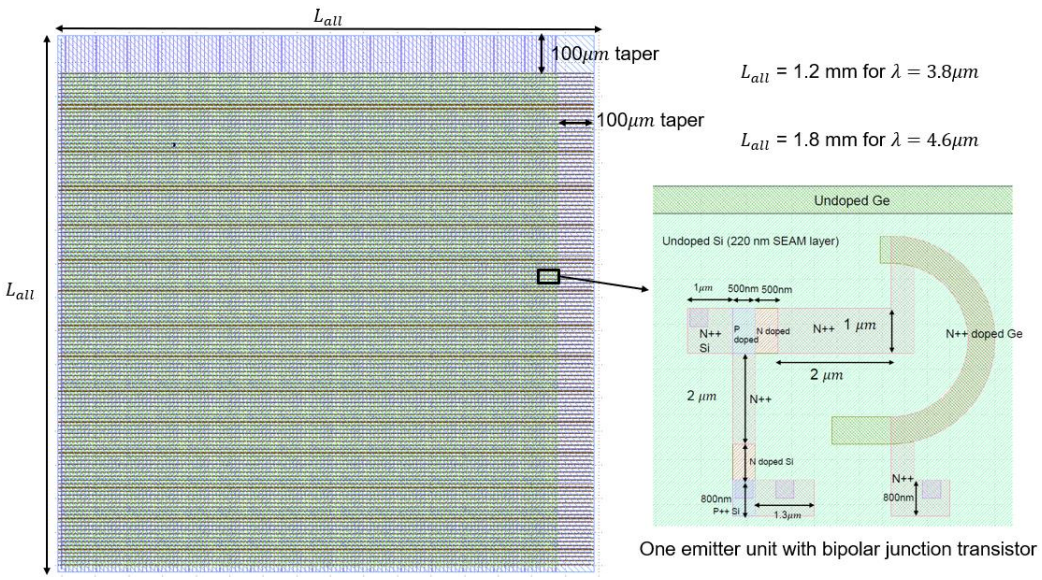
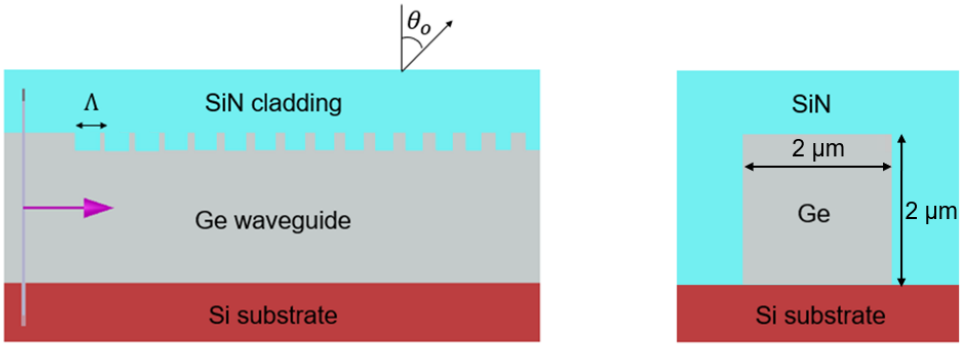


Figure 17. 128 × 128 Lateral-emitter OPA mask layout based on AIM PDK with transistors and one unit with BJT detailed parameter at λ=3.8, 4.6 μm.

2.4 PCM-assisted MWIR beam steering devices

Optical phase change materials (O-PCMs), such as GeSbTe(GST) , GeSbSeTe(GSST)[24], are good candidates to realize the solid-state phase change function. Principally, the main beam lobe steering relies on the controllable phase change of each optical antenna. From this perspective, we come up with the idea to use PCMs as phase shifters. In this plan, we still try to utilize the 2D grating MWIR structures, our demonstrated technology, to realize the beam upwards emission. Then we will fabricate amorphous silicon (A-Si) unit blocks on the grating structure, used to heat the PCM material plated on the wafer surface in the final step (collaborated with a research group in Massachusetts Institute of Technology). Figure 18 shows the parameters of the grating emitter used in the PCM-based beam steering devices. The output angle is set around 15 degrees. Figure 19 shows the general fabrication process flow of the PCM-assisted MWIR beam steering

devices. In Figure 19, step1 to step 4 is to reduce the high wafer bowing caused by the Ge layer growth, by depositing PECVD silicon nitride in the wafer backside. Then in step 5 and step 6, we do the stepper lithography machine (ASML300) PM and Ge waveguide layer fabrication. The waveguide design we still follow our successful experience in the previous demo[17], the width and height of the Ge waveguide are both 2 μm. For grating used for emitting light vertically, previously we used the SiN layer on Ge waveguide[17]. This time we will do a shallow etching on the Ge layer to form a grating structure since the SiN will be used in the following structures as cladding material. In Figure 19, from step 8 to step 12 we will finish the patterning of undoped and doped A-Si for future electrical heating up the phase change material to realize the phase shifting. Then the metal conductor will be connected to the doped Si part from step 13 to step 20. Finally, we will collaborate with MIT research group to deposit PCM on the grating emitters and A-Si islands' location.



Grating length = 2 mm

Etching depth (nm)	Grating width (μm)	Wavelength (μm)	n_{eff1}	n_{eff2}	Duty cycle	n_{eff}	Output angle	Period (μm)
60	2	4.6	3.777768	3.770752	0.5	3.77426	14.9	1.308

Figure 18. Grating emitter design for the PCM-MWIR beam steering devices

Figure 19. Fabrication process flow of the PCM-MWIR beam steering devices

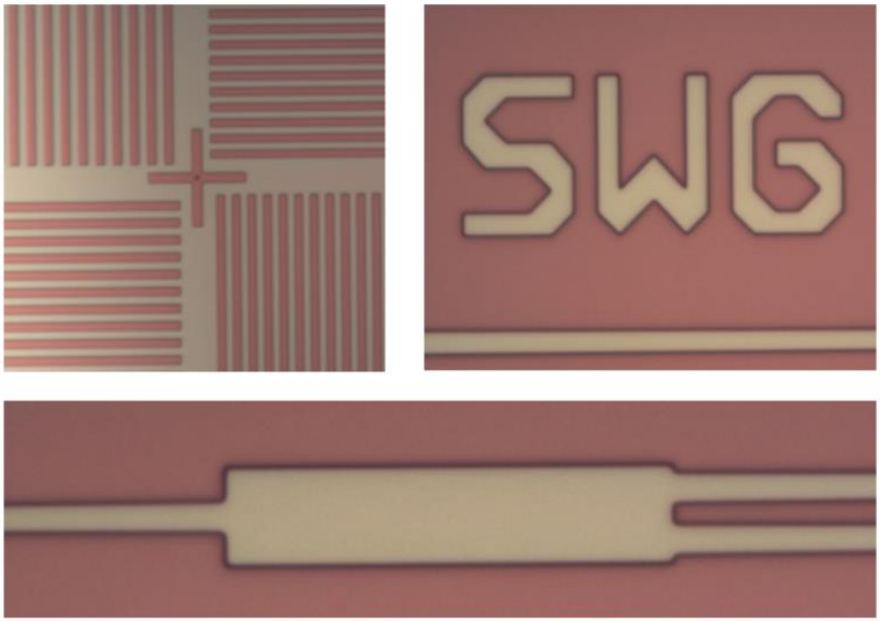


Figure 20. Microscope images of stepper PM, straight Ge waveguide, and Ge MMI after lithography

Figure 20 shows the microscope images of different structures during the fabrication process of the PCM-assisted MWIR beam steering devices, including the stepper PM, the straight waveguide of Ge layer, and Ge MMI.

2.5 LWIR beam steering devices

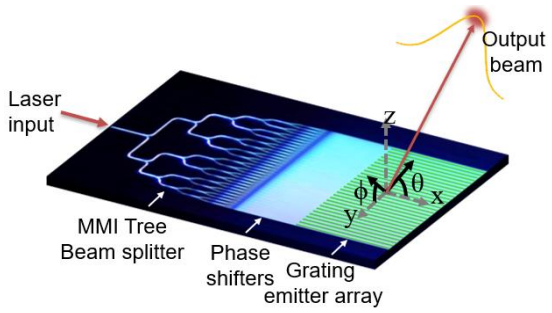


Figure 21. 2D OPA-based beam steering devices using grating emitter[17]

For a proof-of-concept demonstration of the first OPA beam steering for LWIR, we decide to use a grating emitter array, similar to that in our MWIR work[17], which is shown in Figure 21. What is different is that we choose CaF_2 as our dielectric cladding material due to its low material loss in LWIR and it is also doable for the cladding deposition to have more space for multi-layer integration and metal crossing above the waveguides. Based on what is shown in Figure 21, the LWIR device design can be decomposed into several subtasks: design of single-mode Ge-on-Si waveguide, multimode interferometer (MMI) power splitter, phase shifters, and grating emitter. Figure 22 shows the eigenmode simulation results of the Ge waveguide in LWIR ($\lambda = 8.25$ μm). To make sure good TM mode confinement and the single-mode behavior, the overall size of the Ge waveguide is chosen as 3 μm ×3.5 μm.

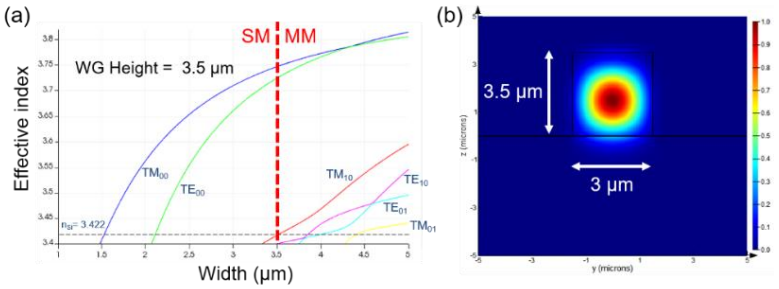


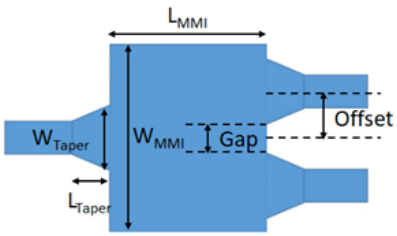
Figure 22. Variation of the effective index with waveguide width when waveguide height is 3.5 μm. (b) Simulated TM mode profile at $\lambda = 8.2$ μm.

Like our previous design in MWIR, we explore the best parameter set of MMI in LWIR to feed the light to the 128-channel Ge grating emitter. In our real layout and experiments, we will use the multi-staged cascaded MMI trees as the beam splitter for power feeding. Figure 23 shows a single MMI design for 3dB splitting and FDTD simulation results. Here are two different designs presented to accommodate process fabrication variation. The larger gap is the priority, but a trade-off will be made for a compact design to allow tight integration.

(a)

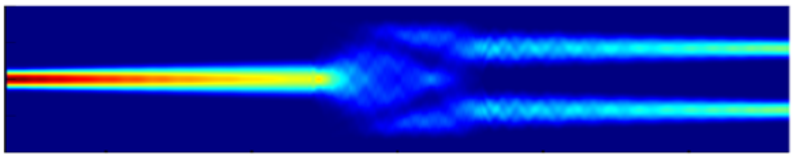
W_{MMI} (μm)	16	19
L_{MMI} (μm)	59.2	84.2
Offset (μm)	4.2	5.0
W_{Taper} (μm)	5.6	5.0
L_{Taper} (μm)	150	150
Gap (μm)	2.8	5
Transmitted relative power (%)	49.47	49.35
Total loss (dB)	0.05	0.06

(b)



(Ge ridge 3 x 3.5 μm², TM mode)

(c)



(d)

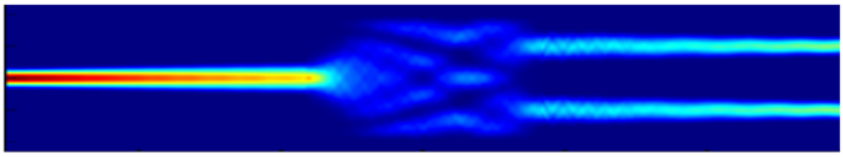
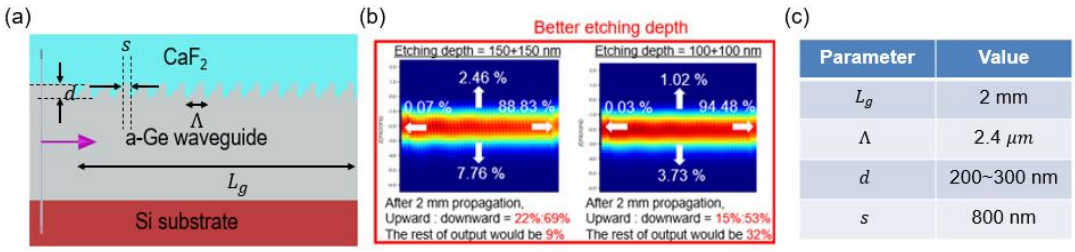


Figure 23. (a) MMI design parameter table for 3 μm × 3.5 μm ridge waveguide platform at 8.25 μm wavelength. (b) Schematic of an MMI structure. Beam propagation simulation of MMI 3dB power splitting for (c)W_{MMI} = 16 μm and (d) W_{MMI} = 19 μm.



Parameter	Value
L_g	2 mm
Λ	2.4 μm
d	200~300 nm
s	800 nm

Figure 24. (a) Grating coupler design with CaF_2 cladding and staircase-shaped grating. (b) FDTD simulation results on power propagation for grating coupler (100 μm length). (c) Parameter set of final optimized structure.

Figure 24 shows the grating emitter design for beam upward emission. To enhance the vertical coupling efficiency, a stair-cased grating structure (two-layer etching) is used. The optimized etch depth for this LWIR Ge grating with CaF_2 cladding is between 200 (100+100) ~ 300 (150+150) nm. The pitch is around 2400 nm and each step length is 800 nm. After propagating a 2-mm-long grating length, we could achieve the upward emission efficiency of around 20% and the diffraction angle of the output beam is around 15 degrees.

Based on the stair-cased grating structure in our emitter design, we propose the corresponding fabrication plan, which is shown in Figure 25.

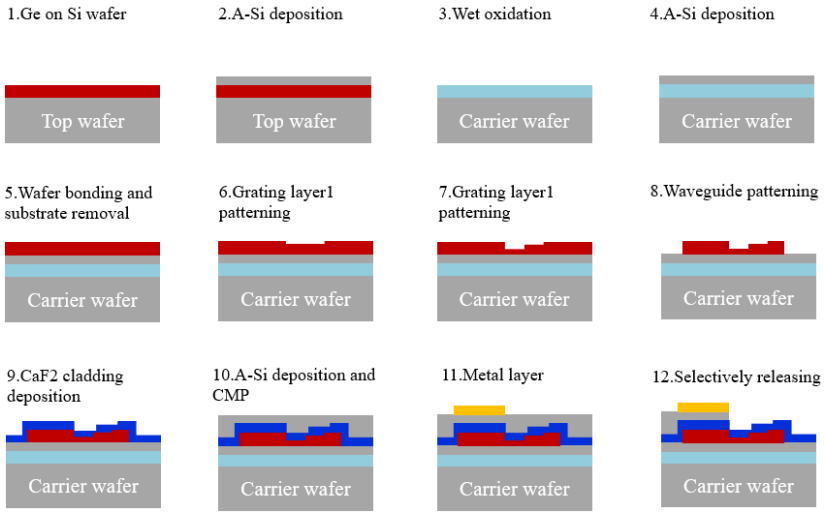


Figure 25. The fabrication process plan for the 2D LWIR device

From step 1 to step 5, we prepare the Ge-on-SOI wafer. The oxide layer above the substrate is important because it serves as a heat-insulating layer, considering the thermal issues in our future characterizations (when injecting current and producing heat). Steps 6 and 7 contain the lithography and etching of two grating layers we mentioned before. Step 8 is the fabrication of the waveguide layer. Step 9 deposits the low-loss CaF2 cladding process to insulate the metal from the Ge waveguide. Step 10-12 deposits amorphous silicon, the metal layer, and selective release to complete the 2D PEPA for LWIR. Following this process flow, we have done some test structure fabrication. Figure 26 shows the SEM photos of the staircase-shaped grating structure.

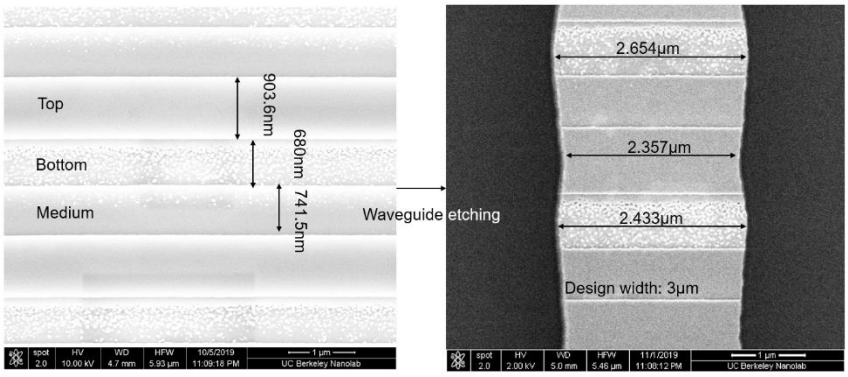


Figure 26. SEM photo of the staircase-shaped grating structure (left) and grating region after etching of the waveguide layer (right).

Chapter 3

Quantum Cascade Laser (QCL) Integration

3.1 Hybrid laser-waveguide integrated structure

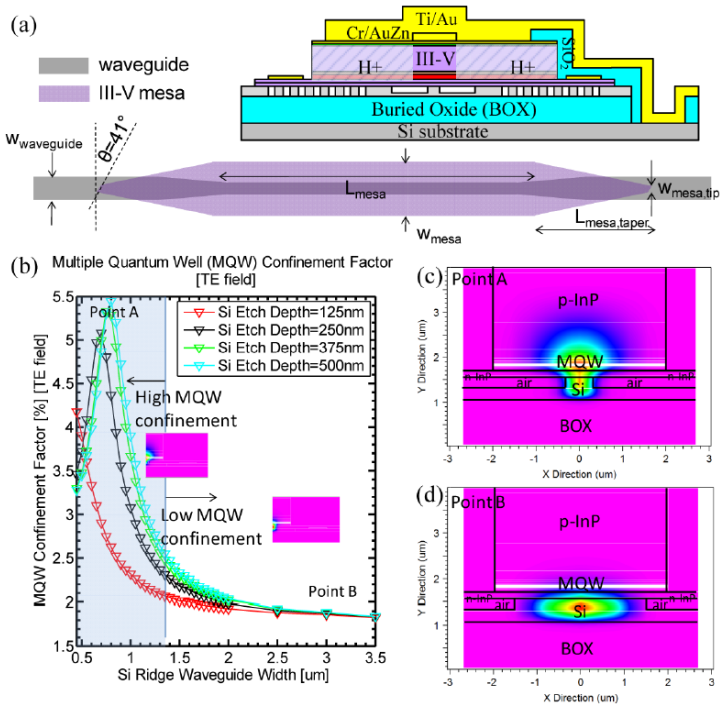


Figure 27. (a) Cross-section and top view of hybrid SOA with III-V taper regions, (b) MQW confinement factor vs. silicon waveguide width, (c) 2-D mode-profile indicating high confinement region Γ_{MQW} = 5.1%, and (d) low confinement region[25].

We propose to integrate the QCL structure, along with the amplifier (SOA) part with the Ge waveguide, based on the successful experience of demonstrating efficient chip-scale III-V/silicon hybrid optical amplifiers[25]. Figure 27 shows the hybrid SOA with III-V taper regions in our previous work. In Figure 27, in the region where mode transition from III-V material to Ge

waveguide, we deploy negative taper (decrease the width gradually) in III-V material and positive taper (increase the width gradually) in the Ge region, to push the mode down smoothly, and vice versa. This time for our QCL structure, we use a similar way. For the light source part. On one hand, we collaborate with the University of Central Florida (UCF) to design QCL wafers for the fabrication of our integrated structures (3.8 μm and 8.2 μm center wavelength). Figure 28 and Figure 29 show the InP-substrate QCL wafer structure provided by UCF at MWIR and LWIR, respectively. On the other hand, we order QCL wafers from a commercial company (4.6μm center wavelength). Figure 30 shows the structure provided by ThorLabs.

Layer	Material	Thickness (μm)	Doping (/cm^3)
top-contact	InGaAs	0.2	uid
top-clad	$Al_{0.95}Ga_{0.05}As$	0.8	Si: 8.0E+18
top-clad	GaAs	1.2	Si: 1.0E+17
top-clad	$Al_{0.4}Ga_{0.6}As$	1.5	Si: 3.0E+16
Core	AlInGaAs	1.0875	---
Grading	AlInGaAs	---	---
bottom-clad	InP	0.75	Si: 3.0E+16
Etch Stop	InGaAs	0.1	Si: 3.0E+16
Buffer	InP	3.0	Si: 3.0E+16
Substrate	InP	---	Si: 1.0E+17

Figure 28. The detailed structure of 3.8 μm center wavelength QCL wafer provided by UCF

Layer	Material	Thickness (μm)	Doping (/cm^3)
top-contact	InGaAs	0.2	uid
top-clad	$Al_{0.95}Ga_{0.05}As$	1.0	Si: 8.0E+18
top-clad	GaAs	2.0	Si: 5.0E+16
top-clad	$Al_{0.4}Ga_{0.6}As$	4.0	Si: 2.0E+16
Core	AlInGaAs	1.864	---
Grading	AlInGaAs	---	---
bottom-clad	InP	1.0	Si: 2.0E+16
Etch Stop	InGaAs	0.1	Si: 2.0E+16
Buffer	InP	3.0	Si: 2.0E+16
Substrate	InP	---	Si: 1.0E+17

Figure 29. The detailed structure of 8.2 μm center wavelength QCL wafer provided by UCF

Layer	Material	Thickness (μm)	Doping (/cm^3)
top-contact	InGaAs	0.1	Si: >1.0E+19
top-clad	$Al_{0.95}Ga_{0.05}As$	1.5	Si: 8.0E+18
top-clad	GaAs	1.5	Si: 5.0E+16
top-clad	$Al_{0.4}Ga_{0.6}As$	2.0	Si: 2.0E+16
Core	AlInGaAs	1.6461	---
Grading	AlInGaAs	0.0239	---
bottom-clad	InP	0.75	Si: 2.5E+16
Etch Stop	InGaAsP	0.1	Si: 4.0E+16
Buffer	InP	4.5	Si: 4.0E+16
Substrate	InP	350	Si: 3.0E+18

Figure 30. The detailed structure of 4.6 μm center wavelength QCL wafer provided by ThorLabs

Figure 31 shows the perspective view, side view, top view, and cross-section view of the integrated III-V mesa and Ge structure at the mode pushing-down region, with a center wavelength at 3.8μm. The parameter of detailed structures of each material layer is also labeled in the corresponding location. Figure 32 shows the FDTD simulation result, the side view of E-field intensity distribution, representing mode transition from III-V mesa to Ge region. The simulated result shows the power transfer efficiency is nearly 95%. The reflection of the III-V mesa area is suppressed to 0.02%. Figure 33 shows the cross-section 2D electrical field intensity distribution at a different location along the optical mode propagation direction, which indicates the smooth mode transition from the upper III-V material part to the bottom Ge/Si passive waveguide part.

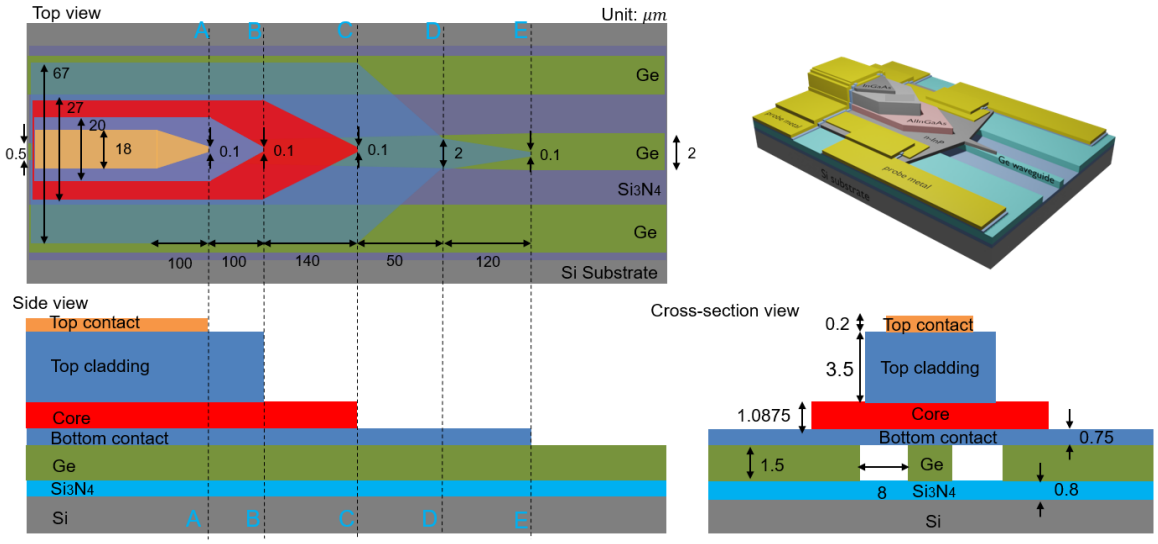


Figure 31. MWIR Hybrid SOA and waveguide structure at λ=3.8 μm: Top view, side view, cross-section view, and perspective view of the integrated structure.

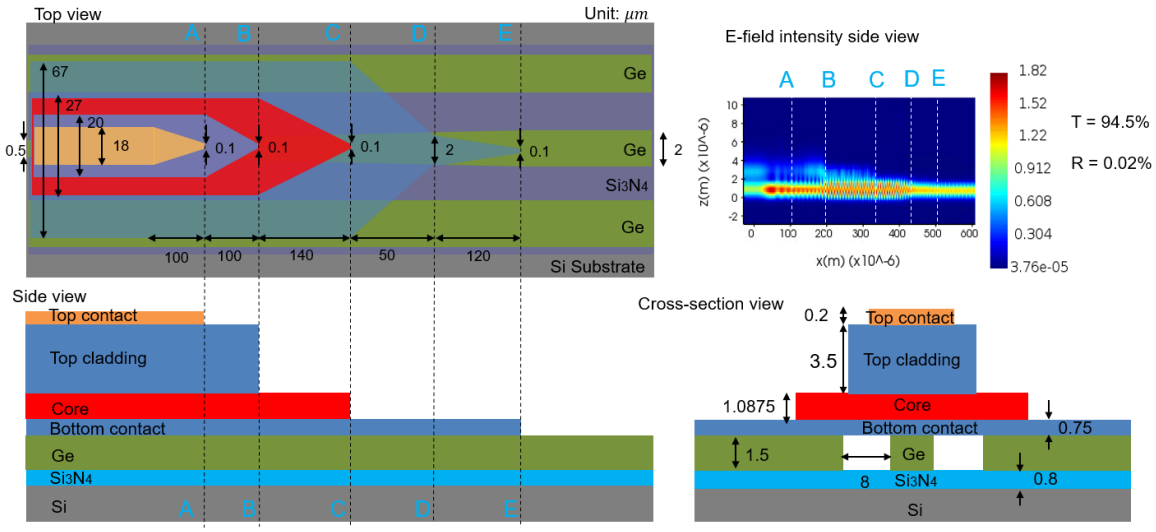


Figure 32. Three views of the hybrid structure and side view E-field intensity distribution, λ=3.8 μm

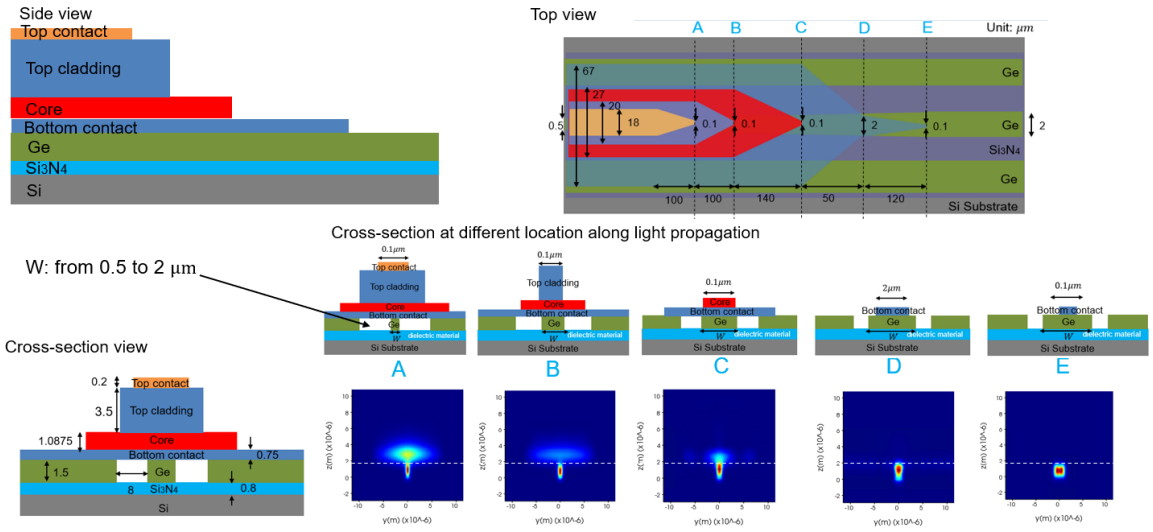


Figure 33. λ=3.8 μm, three views of hybrid structures and cross-section 2D E-field intensity distribution indicating the power transfer from III-V material to Ge region at different beam propagation locations by 3D FDTD simulation.

Figure 34, Figure 35, Figure 36, and Figure 37 show similar structures in another two wavelengths. When the center wavelength is 4.6μm, the power transfer efficiency from the III-V region (layer structure provided by ThorLabs company) to the Ge waveguide region is around 90% and the reflection is 0.02%. When the center wavelength is 8.2μm, the power transfer efficiency

from the III-V region (layer structure provided by UCF) to the Ge waveguide region is around 92% and the reflection is 0.02%. The design of the integrated structure shows the smooth mode transition in both wavelengths.

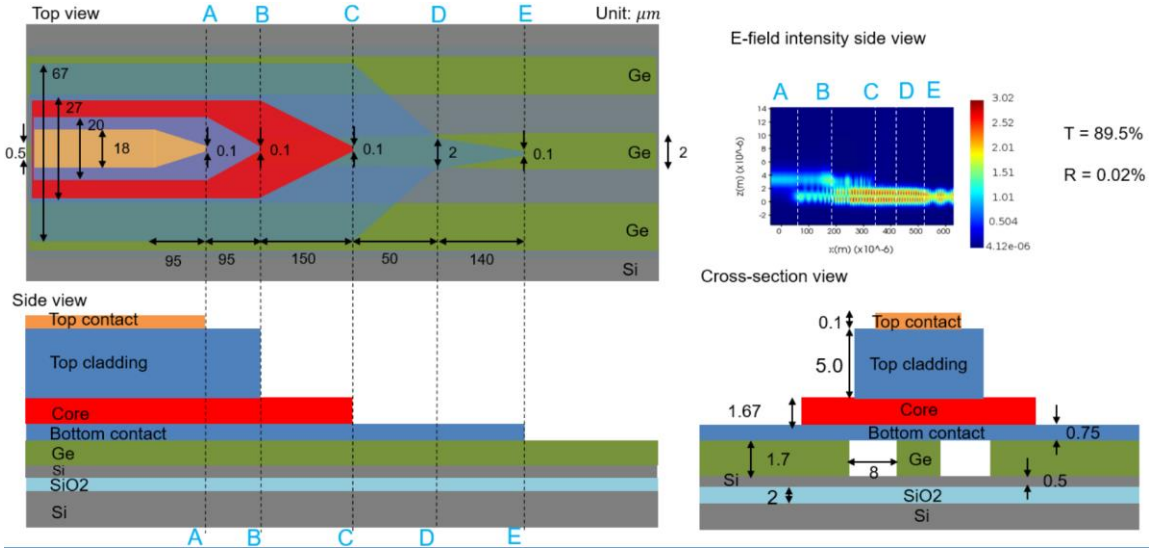


Figure 34. Three views of the hybrid structure and side view E-field intensity distribution, λ=4.6 μm

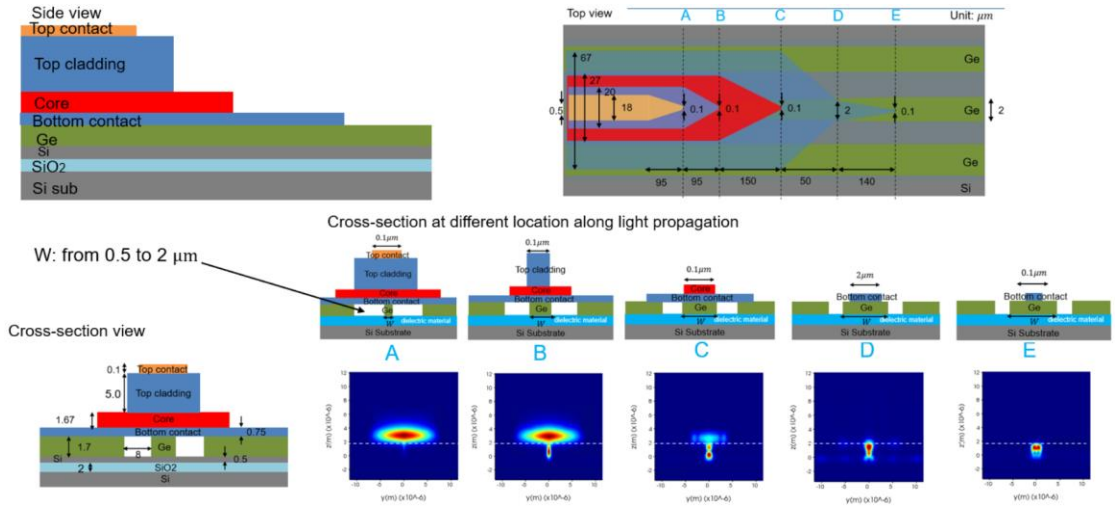


Figure 35. λ=4.6 μm, three views of hybrid structures and cross-section 2D E-field intensity distribution indicating the power transfer from III-V material to Ge region at different beam propagation locations by 3D FDTD simulation.

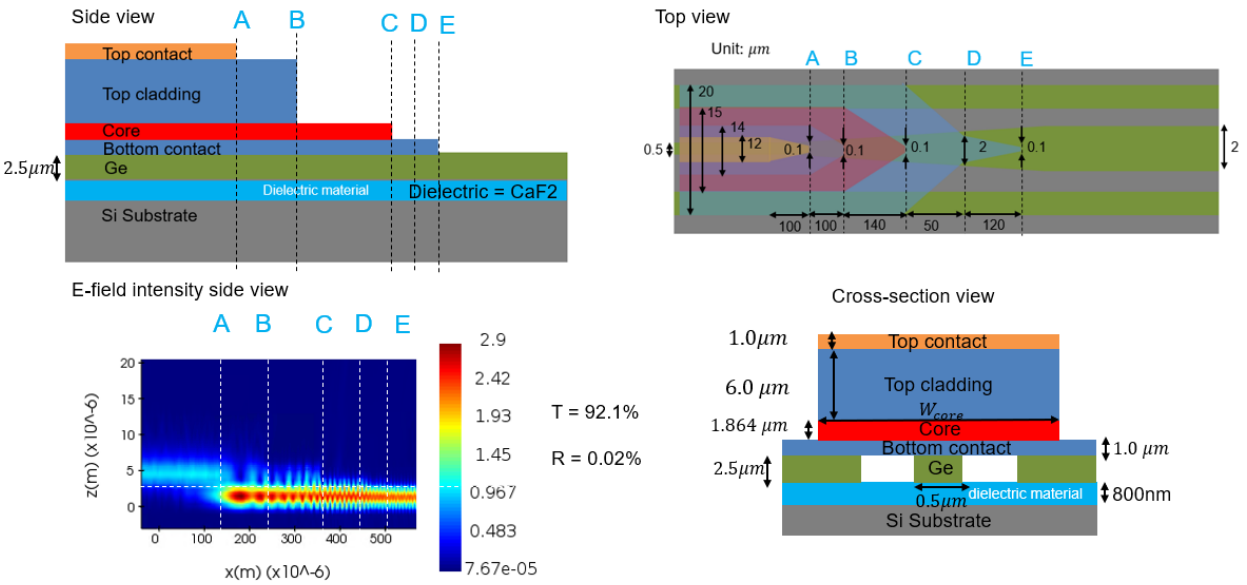


Figure 36. Three views of the hybrid structure and side view E-field intensity distribution, λ=8.2 μm

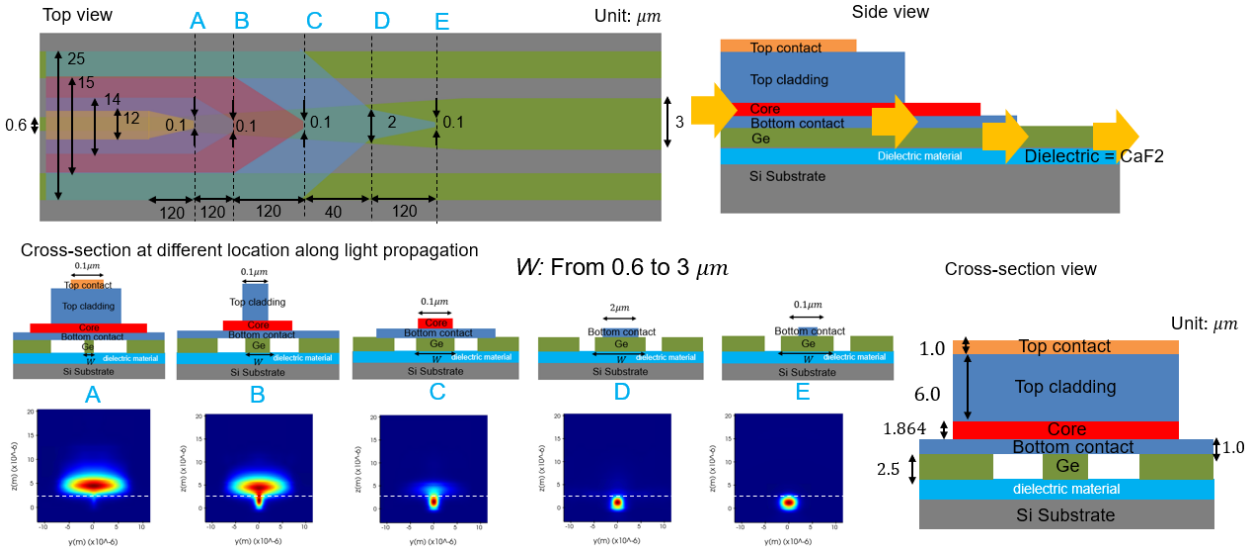
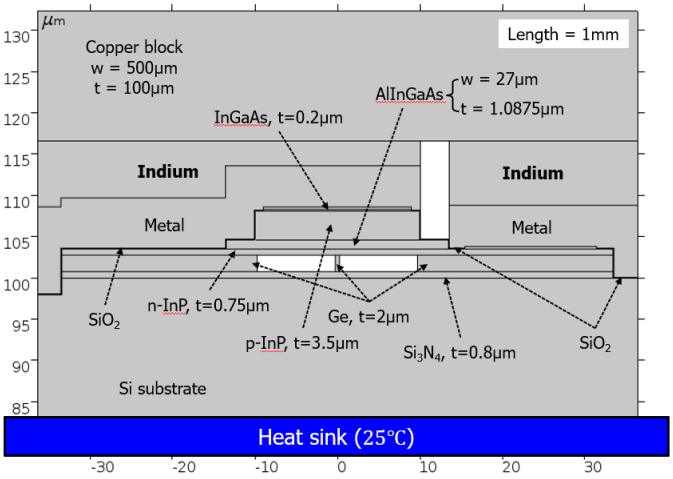


Figure 37. λ=8.2 μm, three views of hybrid structures and cross-section 2D E-field intensity distribution indicating the power transfer from III-V material to Ge region at different beam propagation locations by 3D FDTD simulation.

We also consider the thermal dissipation for our III-V/Ge-Si hybrid structure. Figure 38 and Figure 39 show the 2D thermal simulation model and the results of the integrated III-V laser/Ge-

Si waveguide structure (e.g., 3.8 μm center wavelength design). If we put our integrated device in the metal block (e.g., Copper), the thermal dissipation will be improved. Before bonding the whole structure to the copper block, the source temperature is around 92ºC, which is unacceptable. After bonding, the source temperature is lowered to be around 74ºC. Also, if we use the Si_3N_4 instead of SiO_2 as the passivation layer material, the heat transfer situation will be better. The target working temperature of our laser is around 50ºC, which needs further optimization.



Material	Thermal conductivity, W/(m·K)
Si	131
InP	68
SiO_2	1.38
Si_3N_4	25
Ge	60
Metal (Au)	310
Copper	400
Indium	81.8

Figure 38. 2D thermal simulation model of integrated III-V laser/Ge-Si waveguide structure and thermal property of the material in the structure

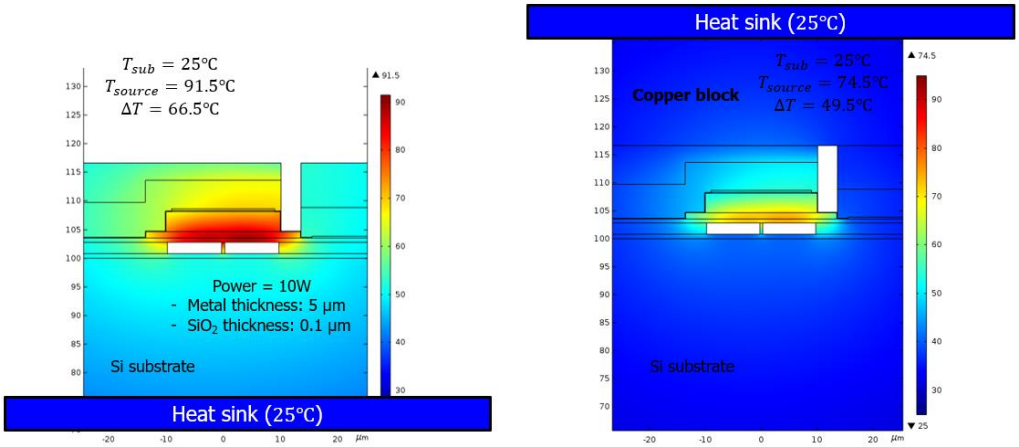


Figure 39. 2D thermal simulation results, the laser active region temperature with heat sink bonded to Si substrate (left) or Cu block (right)

3.2 Transfer-printing technology for QCL laser integration

Considering the real fabrication tolerance and difficulty, usually, the integrated structure proposed in our design will be divided into the fabrication of III-V (laser) structure and silicon photonics device structure (Ge waveguide). Then researchers can deploy integration methods, such as direct wafer-bonding[20] to form the hybrid structure as targeted. In the recent decade, a new technology called ‘transfer printing’ appeared and drew researchers' attention[18]. Figure 40 shows the transfer-printing technology that can be used for this QCL-waveguide integration structure. By using transfer-printing, materials or devices can be selectively removed from their source wafer and transferred to a new substrate in a massively parallel way, making use of structured elastomeric polydimethylsiloxane (PDMS) stamp. One advantage of using this method is that dense arrays of different devices realized on their source wafer can be selectively picked and printed on the target substrate, with high yield (99.9% and higher) and high alignment accuracy (achieving 1500nm misalignment out the device array to a Ge/Si wafer). Recently, the wafer-scale integration of GaAs lasers on silicon wafers with excellent performance has been demonstrated[26].

Figure 41 shows the fabrication process flow for the hybrid QCL and Ge/Si waveguide region. It starts from the wafer-bonding to form the Ge-on-Insulator-on-Si wafer. Then, the Ge waveguide patterning, the transfer-printing of QCL wafer coupons, proton ion implantation for isolation, top metal contact formation, III-V mesa etching, and lower metal contact formation will be conducted in order, to complete the hybrid III-V/Ge QCL-on-Si structure fabrication.

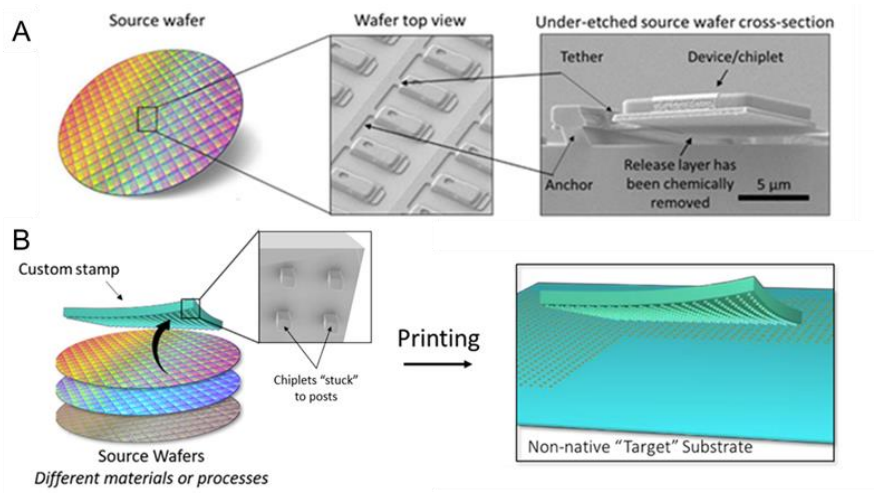


Figure 40. Micro-transfer-printing technology offers both flexibility and high throughput. Source wafer (A, left) and SEM of micro-chiplets, top view (A, center) and side view (A, right) after the chemical under-etch process, B: Sectioned materials (or devices) are removed from their native substrate with a custom, viscoelastic PDMS stamp and transferred to a new target substrate[26].

Especially, the fabrication of transfer-printing coupon (each small block of III-V material in the hybrid integration structure) is the key point in the process flow. Figure 42 shows the cross-section view of the III-V coupon prepared for transfer printing. For the III-V laser wafer, the top-contact, top-cladding, active quantum wells, and bottom cladding layers, also with some part of the etch stop layers, are planned to be dry-etched by Inductively Coupled Plasma - Reactive Ion Etching (ICP-RIE) tools, to form the trench. Then the whole block will be covered and protected by the photoresist (S1828). Then the patterned wafer will be dipped with wet-etchant to do the lateral etching on the whole etch-stop layer. Finally, the coupon blocks (III-V material device structure) are hung over the InP substrate, except some parts are still connected by the photoresist. Then we can use elastomer stamp (such as PDMS) to attach the III-V coupons and 'print' the devices to our target wafer substrate.

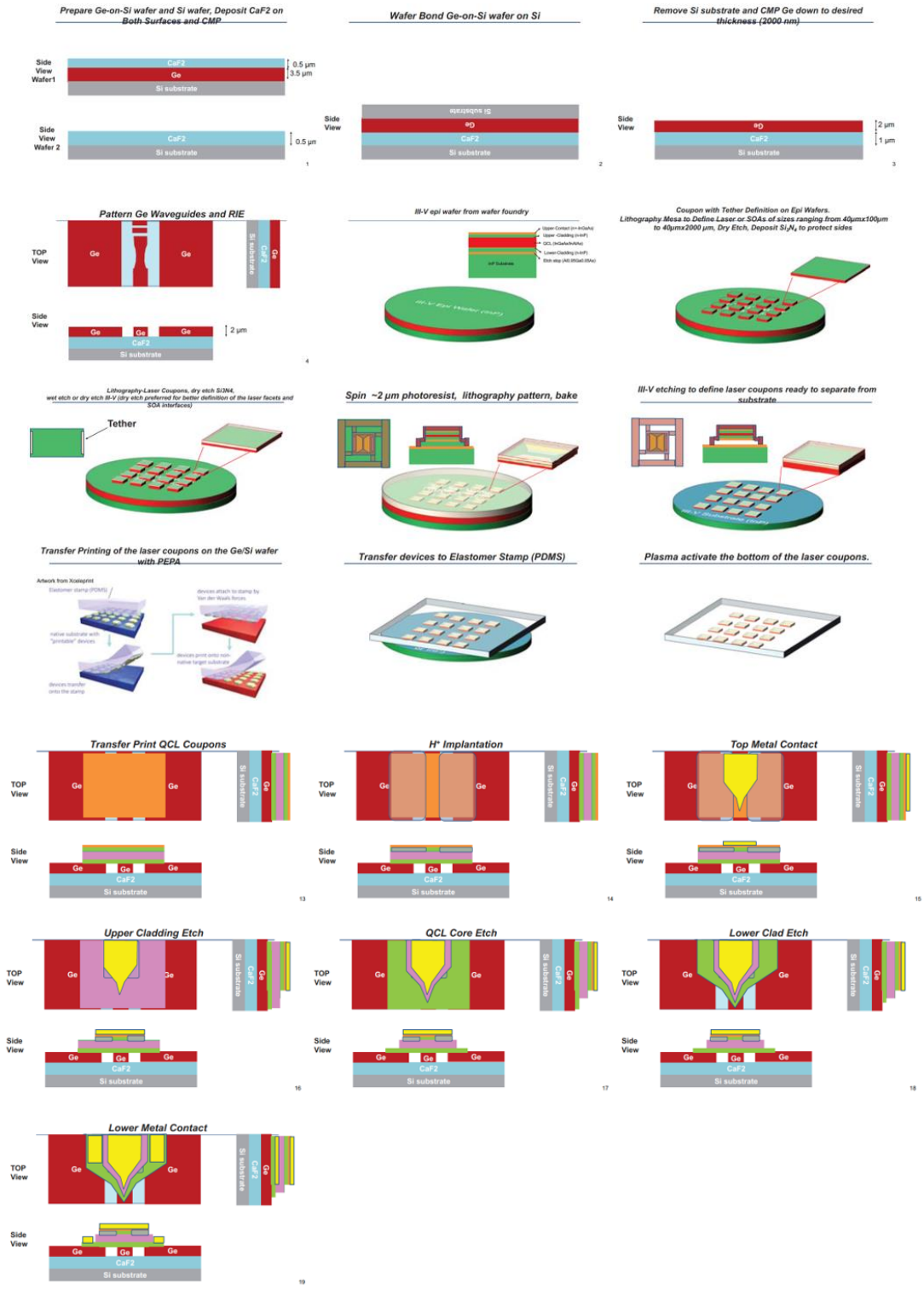


Figure 41. Hybrid III-V/Ge QCL on Si wafer fabrication process

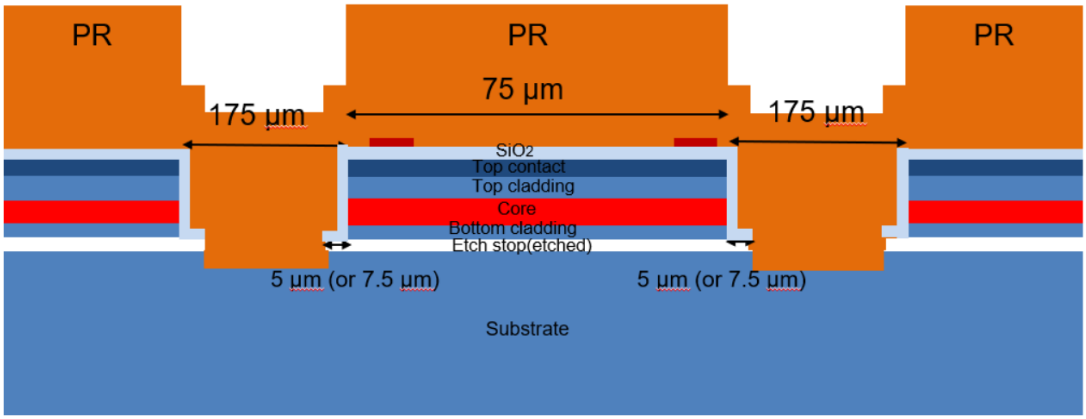


Figure 42. Transfer-printing-based III-V coupon cross-section structure

Following the general fabrication process steps described above, the mask layout design was shown from Figure 43 to Figure 45.

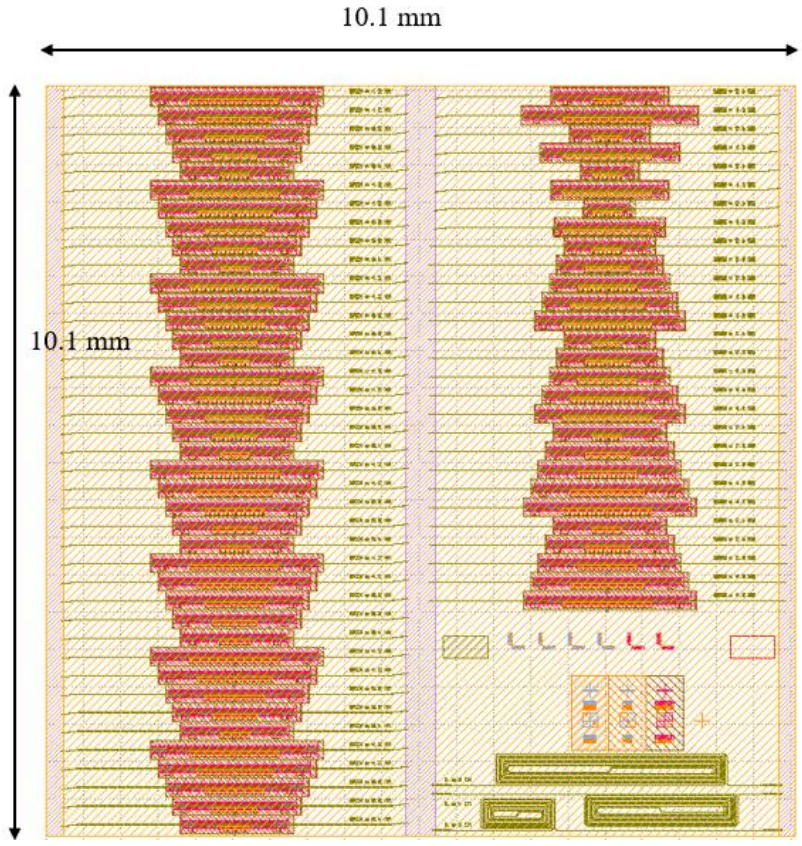


Figure 43. Transfer-printing SOA mask layout (QCL MWIR)-array

Figure 43 shows the transfer-printing SOA/laser array mask layout, generally, it consists of the target wafer structures (passive Ge/Si waveguide layers) and source wafer ones (III-V InP-based gain block and mode converter structure). Figure 44 shows one single component of the hybrid III-V coupon structure. The tether and the surrounding grating structure will assist to form the separate coupon of each III-V mesa, then help to transfer it from the source wafer substrate to the target wafer surface. The quarter-circle mark on the top/bottom side of the tether will be used to align the tether to locate the target wafer waveguide region accurately. For the layout of the passive Ge-waveguide and III-V to Ge mode transition part, some strategies are used to improve the device performance. For example, in Figure 45, the end of the taper structure of the III-V mode transition part is designed as an angled tip to reduce optical energy loss and light reflection. For the same purpose, the output facet of the Ge waveguide is tilted for 7 degrees to minimize the interface reflection. On the two sides of the Ge waveguide, two wide Ge pedestals are put to hold the III-V SOA/laser coupon.

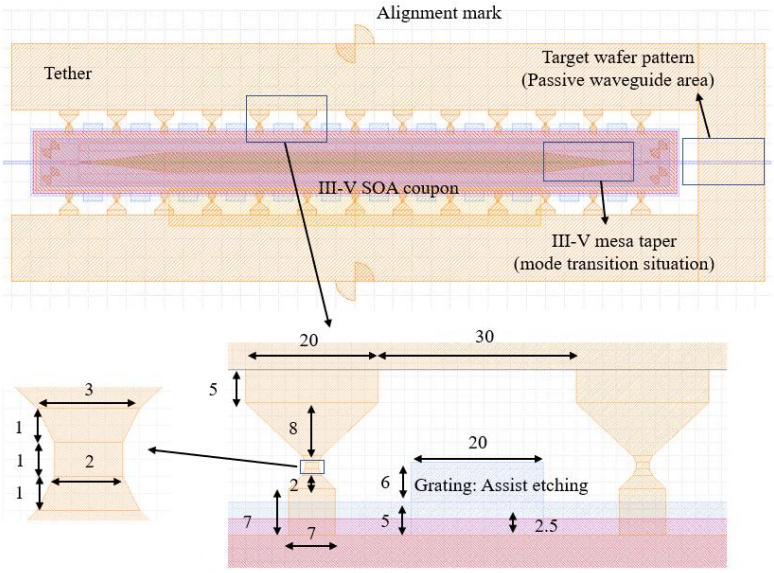


Figure 44. Transfer-printing SOA mask layout (QCL MWIR)-single component

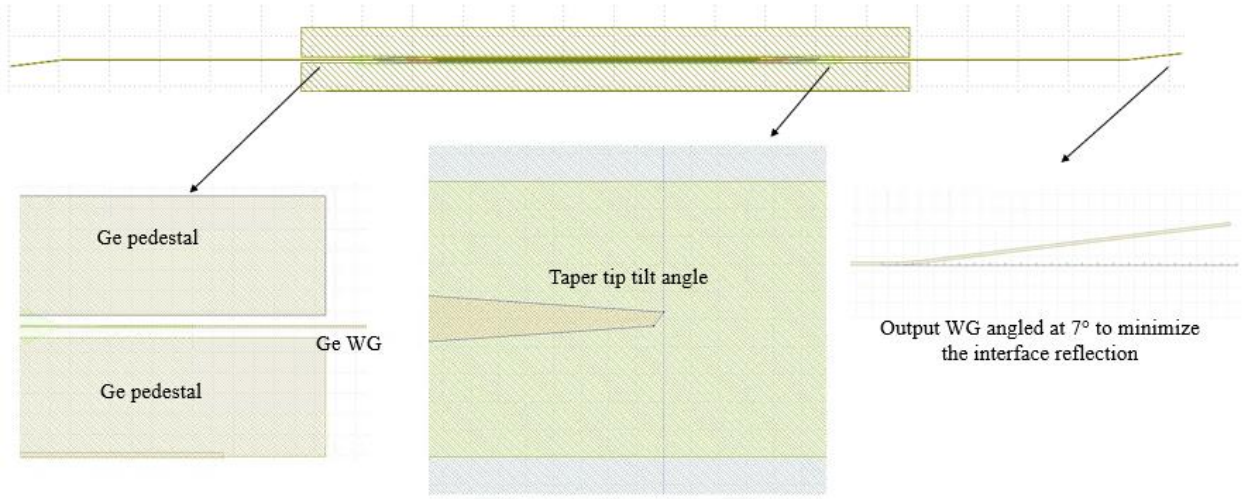
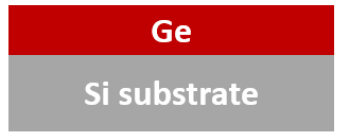


Figure 45. Transfer-printing SOA mask layout (QCL MWIR)-passive Ge waveguide

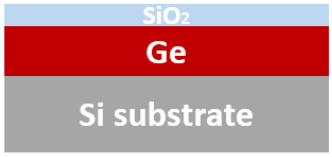
3.3 Transfer-printing wafer test fabrication

Fabrication steps of transfer-printing lasers including two main parts: the source wafer fabrication and the target wafer. In our integrated structure, the target wafer is the Ge/Si-based passive waveguide wafer. And the source wafer is InP-based Epitaxial growth Quantum Cascaded Laser wafer. In our planned process flow, the target wafer fabrication includes the formation of Ge-nm on-dielectric-on-Si structure and Ge waveguide layer fabrication. In our real operation and experiments, the Ge-on-dielectric-on-Si structure needs process calibration and

test. Then we apply the Ge waveguide layer fabrication on the Ge-Si wafer first. Figure 46 shows the general process.

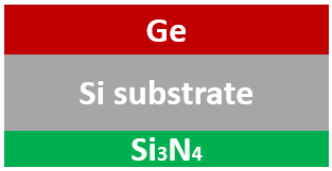


Step1: wafer preparation

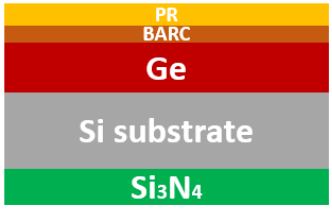


Step2: SiO_2 deposition

Step3: Si_3N_4 deposition



Step4: SiO_2 removal

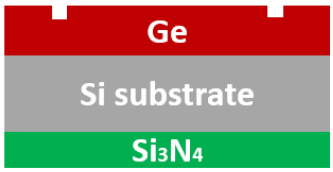


Step5: PR and BARC coating

Step6: P-mark lithography and development

Step7: BARC etching

Step8: Ge P-mark etching

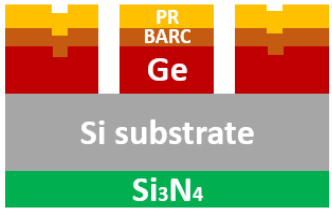


Step9: PR and BARC removal

Step10: PR and BARC coating

Step11: Ge WG layer lithography and development

Step12: Ge WG layer BARC etching



Step13: Ge WG layer etching

Step14: PR and BARC removal

Figure 46. Preliminary fabrication process flow of Ge-Si target wafer for transfer-printing

Figure 47 shows the quart-circle transfer-printing alignment marks and Ge waveguide structure under the microscope.

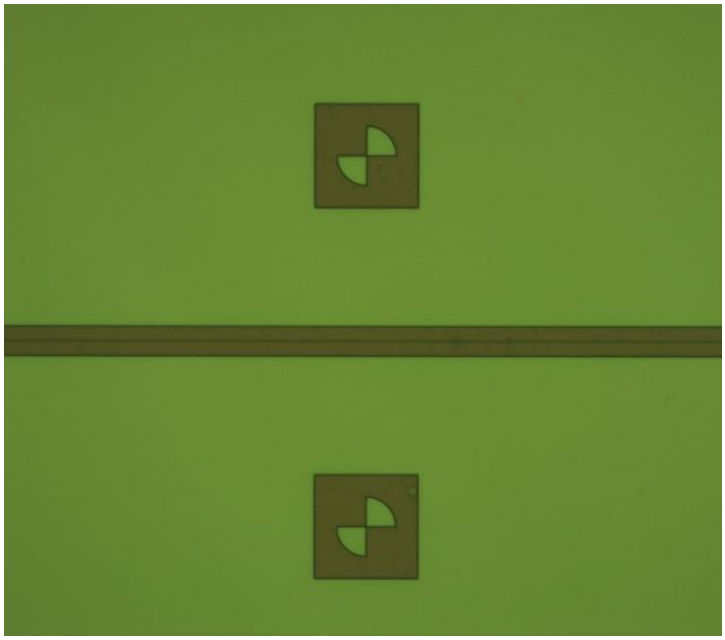


Figure 47. Ge-Si target wafer structure microscope image after lithography

For the source wafer fabrication, we also do some preliminary calibration work. Figure 48 shows the SEM photos of InP with SiO2 hard-mask structure (the III-V SOA/laser coupon block). The SiO_2 used here is deposited by the HDPCVD tool in the Center for Nano-MicroManufacturing (CNM2) at the University of California, Davis. The InP etching is conducted by the ICP-RIE tool (Oxford-ICP) in Berkeley Marvell NanoLab. The gas used for the InP etching contains Ar, CH_4, H_2, and Cl_2, the gas flow is 15sccm, 6.5sccm, 5.5sccm, 3sccm, respectively.

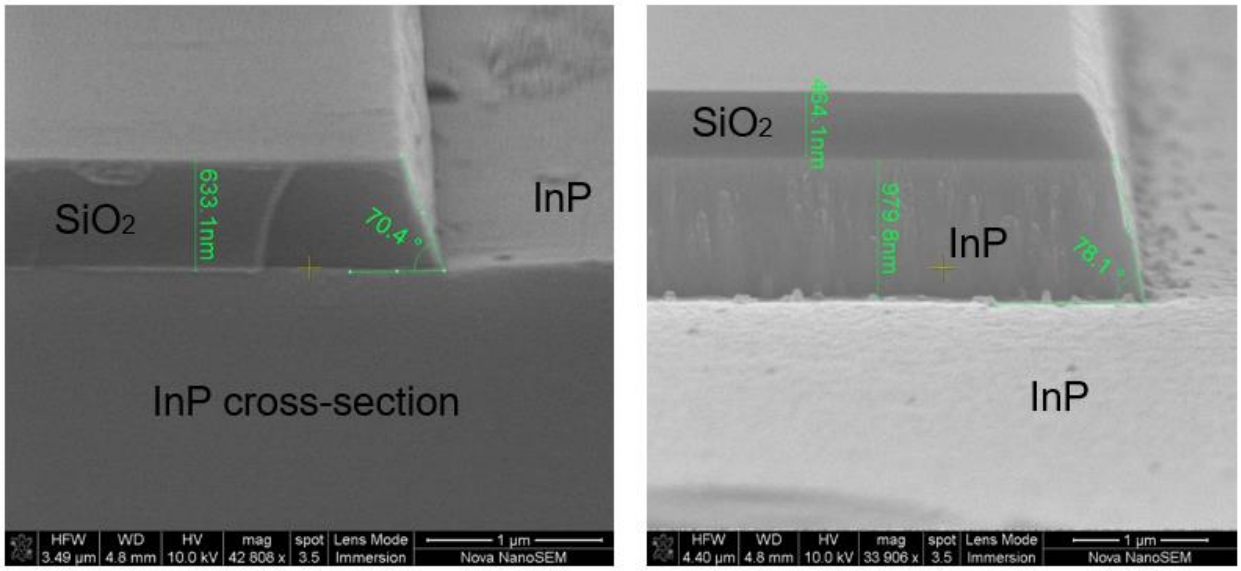


Figure 48. SEM photos of InP with SiO2 hard-mask structure (left: Photo before InP etching, right: Photo after InP etching)

Chapter 4

Summary and Outlook

4.1 Overall work summary and outlook for future

This thesis is a summary of my work in the previous three years on the project about a multi-wavelength beam steering system. With help from colleagues and the supervisor, we propose several methods, trying to demonstrate the beam steering systems at MWIR and LWIR. For the functional beam steering devices, the innovation points include the novel light emitter design, such as 45-degree Ge-based vertical via emitter, stair-cased grating at LWIR and the application of phase-change-material as the phase shifter in the OPA structure. For the light-source part, based on our mature hybrid SOA/waveguide structure, we utilize the state-of-the-art transfer-printing technology to realize the integration of III-V material and Ge-Si dielectric light propagation structure. About the outlook for the future in this direction, on one hand, in our new proposed light emitter design, we could improve our fabrication process and develop a more efficient method. For example, for the 45-degree Ge vertical via structure, currently we are trying to use FIB to form the 45-degree structure. In the future, we could try to use Reactive Ion Beam Etch (RIBE) or Chemically Assisted Ion Beam Etch (CAIBE) to increase the accuracy and efficiency of the etching step. On the other hand, for the light-source fabrication, the wet etching of the source wafer coupon to form the “printable” hung-over device is the key step. For our current laser wafer design, the etch stop layer is removed in the wet step is thin InGaAs or

InGaAsP. Currently, we plan to use the combination of phosphoric acid (H_3PO_4), hydrogen peroxide (H_2O_2), and deionized water (DI water). The composition of the wet-etching solution needs more calibration and test.

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