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Journal

IEEE Electron Device Letters, PP(99)

ISSN

0741-3106

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Publication Date

2023

DOI

10.1109/led.2023.3294722

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Characterization of Noise in CMOS Ring Oscillators at Cryogenic Temperatures

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Abstract— Allan deviation provides a means to characterize the time-dependence of noise in oscillators and potentially identify the source characteristics. Measurements on a 130 nm, 7-stage ring oscillator show that the Allan deviation declines from 300 K to 150 K as expected, but surprisingly increases from 150 K to 11 K. At low temperatures, the measured Allan deviation can be well fit using a few random telegraph noise (RTN) sources over the range of a few kilohertz to a few gigahertz. Further, the RTN characteristics evolve to reveal an enhanced role in lowfrequency noise at lower temperatures.

Index Terms—Allan deviation, CMOS ring oscillator, noise, random telegraph noise, temperature, traps

I. INTRODUCTION

Electronic circuits utilized in space applications, highenergy physics experiments, and high-performance and quantum computing often operate at cryogenic temperatures [1]– [3]. For quantum computing, there is a growing interest in developing control and readout circuitry that operates reliably at temperatures as low as 4 K [4], [5] so as to place it physically close to the qubits and reduce the impact of parasitics in the measurement pathway. Complementary metal-oxidesemiconductor (CMOS) technology is one of the most viable ways to fulfil this need for reliable low-temperature electronics due to its low cost, scalability, and ease of fabrication.

Characterization of the performance of various CMOS technologies at cryogenic temperatures [6]–[9] has been mostly limited to measurements and modeling of dc transistor characteristics. There is relatively limited work devoted to under-

Submitted on 05/03/2023. P.M. and N.P. acknowledge support under the Cooperative Research Agreement between the University of Maryland and the National Institute of Standards and Technology Physical Measurement Laboratory, award 70NANB18H165, through the University of Maryland. A.M. acknowledges support under assistance award 70NANB21H091 from the U.S. Department of Commerce, National Institute of Standards and Technology.

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standing how changes in device characteristics with temperature affect the performance of circuits [10]. Ring oscillators are basic building blocks of many digital and mixed-signal integrated circuits, particularly in applications involving timing generation or measurement [11]–[13]. Measuring their properties provides a valuable platform in understanding how low temperatures affect transient device and circuit properties.

Measurement of the temperature dependence of timing jitter or phase noise in the oscillator is as important for any practical application as characterization of parameters like frequency and power consumption [14]–[17], but appropriate measurements are lacking. Here, we report measurements of the Allan deviation [18]–[20], a time-domain stability metric, of a 7-stage CMOS ring oscillator as a function of temperature. By creating fits for the Allan deviation with white, 1/f and random telegraph noise (RTN) sources, we are able to trace how the noise signatures for devices in this process evolve with temperature. Our results highlight the use of Allan deviation measurements of ring oscillators to characterize the noise properties of devices from a few kilohertz to a few gigahertz.

II. EXPERIMENTAL SETUP

The 7-stage ring oscillator circuit was fabricated in a 130 nm bulk CMOS technology operated at voltages up to 1.5 V. It consists of seven two-input NAND gates [21] with both n-type and p-type transistors sized with a length of 120 nm and width of 8 µm. We wire-bonded the chip to an FR4 [22] printed circuit board with a temperature sensor mounted close to the chip. NP0 [23] ceramic capacitors that perform well down to 4 K, decoupled the on-board power supply. A closed-cycle refrigerator in a cryo-chamber cooled the board.

The timing noise in the oscillator output was characterized with modified Allan deviation [18]–[20], which measures the fractional frequency fluctuations in oscillators as a function of the measurement time interval. Unlike cycle-jitter or cycle-to-cycle jitter [24], Allan deviation captures the dynamics of noise accumulation. We sampled the oscillator output at 50 GHz with an oscilloscope and collected 10 ms time traces. The times at which the output waveform rising edge is at 50 % of its maximum value were used for computing the modified Allan deviation.

III. RESULTS AND DISCUSSION

We interpret the oscillator frequency and current consumption as a function of temperature, as shown in Fig. 1(a), in

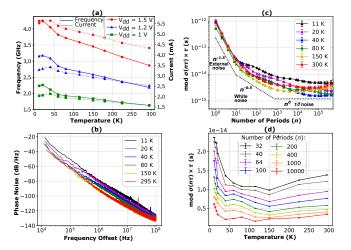


Fig. 1. Measured (a) frequency and current consumption vs. temperature, (b) phase noise power relative to carrier power measured by an oscilloscope at $V_{dd} = 1.2$ V (c) modified Allan deviation (mod $\sigma(n\tau)$) × oscillator period (τ) vs. number of periods (n) at different temperatures (d) mod $\sigma(n\tau) \times \tau$ vs. temperature at different values of n; error bars in (c) and (d) represent 95 % confidence and are determined from χ^2 statistics [18].

terms of the typical increase in both carrier mobility (μ) and transistor threshold voltage (V_t) [4], [6]–[8]. Then, the current increase from 300 K to 40 K would be due to the increased μ , and the drop in current from 40 K to 20 K would be due to the increase in V_t outweighing the effect of a larger μ . The oscillation frequency is inversely proportional to the output capacitance of each gate and proportional to the charging and discharging current. Due to the current increase, the oscillation frequency increases when cooling from 300 K to 40 K. But on cooling from 40 K to 20 K, the current decreases and the oscillation frequency increases. While gate capacitances are largely temperature independent [25], we speculate that the drain/source depletion capacitance may decrease due to incomplete ionization and higher depletion widths below 40 K, leading to an increase in frequency. The relative frequency increase at 11 K (48 %) at $V_{dd} = 1.5$ V is higher than that (37 %) at $V_{dd} = 1$ V, presumably due to the increased V_t affecting the current more at lower values of V_{dd} .

Noise sources with power-law characteristics in frequency can be identified by the slope of the Allan deviation on a log-log scale. For the smallest number of periods the Allan deviation is frequently dominated by high-frequency white noise sources external to the oscillator circuit, with a slope around -1.5, followed by contributions from noise internal to the oscillator with slopes of -0.5 from white noise and 0 from 1/f noise [18]–[20]. The Allan deviation from multiple sources is the square root of the sum of the Allan variances.

Fig. 1(c) and Fig. 1(d) show the modified Allan deviation at $V_{dd} = 1.2 V$. To compare results at different temperatures, we scale the modified Allan deviation by the temperaturedependent oscillator period and plot it as a function of the number of periods. We expect the deviations to decrease at lower temperatures for several reasons. First, The overall thermal noise in the drain current should decrease as the temperature is lowered [26]. Although the thermal noise

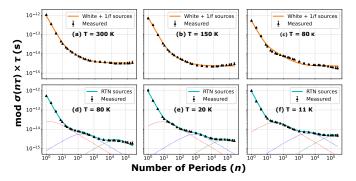


Fig. 2. Fitting measured mod $\sigma(n\tau) \times \tau$ using white and flicker noise sources in (a), (b) and (c), RTN sources in (d), (e) and (f). Dotted lines in (d), (e) and (f) show the individual contribution of each RTN source.

is proportional to the small-signal transconductance, which increases as the temperature is lowered, it only does so by 2 to 3 times for a factor of 70 reduction in temperature [7], [8], [27]. Second, the impulse sensitivity function [28] should decrease with faster rise and fall times, which can be inferred from the higher frequencies at lower temperatures in Fig. 1(a), leading to lower conversion of noise to timing jitter. Third, the 1/f noise is predicted to decrease [29], [30]. However, at 80 K, the Allan deviation is higher than at 300 K for 20 to 1000 periods and gradually becomes higher at all time scales as the temperature is lowered to 11 K. This increase is consistent with measurements on individual devices [27], [31] and fabricated CMOS LC oscillators [4] that show 1/f noise increases below \approx 150 K. The phase noise measurements in Fig. 1(b) show the same trend: phase noise at 11 K was ≈ 10 dB higher than that at 300 K. In addition to the increase in the magnitude of the Allan deviation measurements, there are also intermediary slopes that are not characteristic of white or 1/f noise.

To understand the noise increase seen in our measurements, we first fit the measured Allan deviation using a sum of lines of slopes -1.5, -0.5, and 0 for frequency fluctuations due to external, white, and 1/f noise respectively. The fitting parameters were the magnitudes of these three noise sources, and we obtained fits by minimizing the sum of relative least-squares errors. These noise sources fit the measured data well at 300 K and 150 K, see Fig. 2(a) and Fig. 2(b). At 80 K (Fig. 2(c), they give a poor fit, confirming that the noise in the circuit at 80 K is not purely white and 1/f.

We attribute the poor fit to the Allan deviation to random telegraph noise (RTN), which originates from the switching activity associated with traps and has a Lorentzian profile in the frequency domain [32]–[35]. Capture and emission of electrons by a trap results in two-state current fluctuations that linearly map to timing deviations [28]. The autocorrelation function for an RTN signal with the characteristic rate r is e^{-rt} [32]. By using this expression for the autocorrelation of a RTN signal, the contribution of an RTN source to the Allan variance is:

$$\frac{A^2}{\tau^2} \frac{4}{(rt)^2} \left(2rt + 4e^{-rt} - e^{-2rt} - 3\right),\tag{1}$$

with t the measurement time, A the RTN jitter magnitude, and τ the oscillator period. In the limit $rt \ll 1$, $\sigma^2(t) \propto rt$; when

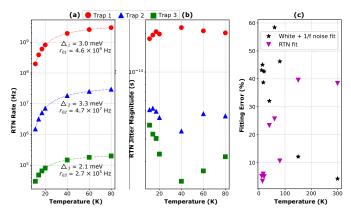


Fig. 3. Evolution of (a) trap frequency, (b) trap noise magnitude and (c) total fitting error vs. temperature

 $rt \gg 1$, $\sigma^2(t) \propto 1/(rt)$ giving the expected dependence of the Allan deviation as $t^{1/2}$ and $t^{-1/2}$ where the Lorentzian shows a $1/f^2$ roll-off and is flat, respectively.

At and below 80 K, we fit the Allan deviation with a superposition of high-frequency external noise and three RTN sources as in Eq. 1. We model the activity of traps as thermally activated and governed by $r = r_0 \exp[-\Delta/kT]$, with r_0 the trap characteristic escape rate, Δ the trap activation energy, k Boltzmann's constant, and T the temperature. The fitting parameters are temperature-independent values of Δ and r_0 for each of the three RTN sources and independent magnitudes for the three sources at each temperature. Fig. 2(d) shows the fit at 80 K obtained with RTN sources, which matches the measured data better than the fit obtained with white and 1/fnoise sources. Fits at 20 K and 11 K shown in Fig. 2(e) and Fig. 2(f) also match the measured data closely. We expect that there are contributions at all temperatures from white and 1/f sources in addition to the RTN sources but that different contributions dominate at different temperatures.

Fig. 3(a) and Fig. 3(b) show the evolution of the frequency and magnitude of the three RTN sources with temperature. Fig. 3(c) shows that at 40 K and above, there may be competing contributions from RTN, white and 1/f sources giving poor fits with all models. However, below 40 K, the RTN fits are significantly better than those done with white and 1/f noise. This indicates that at low temperatures, in a ringoscillator circuit comprised of 28 transistors, the observable noise is dominated by the switching activity of ensembles of a few distinct types of traps that emerge from the underlying defects present in these devices. As the temperature goes down, the rate r for each of the traps decreases, shifting the peak in the Allan deviation to lower and lower number of periods. The barrier heights (Δ values) in Fig. 3(a) found in our fits are consistent with the explanation offered for the increase in measured device 1/f noise due to band-tail states that act as traps at low temperatures [4], [27], [31].

The results in Fig. 3 can explain the increase in noise as the temperature decreases. At high temperatures, the band edge traps contribute high-frequency jitter that is obscured by the external noise. As the temperature decreases, the time scales at which the traps contribute decrease and come out from under the high frequency tail, increasing the noise in the region otherwise dominated by the white and 1/f noise in the circuit.

IV. CONCLUSION

Allan deviation measurements probe the noise signatures of a group of devices at cryogenic temperatures from a few kilohertz to a few gigahertz. Such measurements on a 7stage CMOS ring oscillator show non-monotonic temperature scaling, with a reduction in noise from 300 K to 150 K and a subsequent increase in noise from 150 K to 11 K. This trend is consistent with previously reported individual device measurements that have attributed the increase in noise below 150 K to uncovering of band-tail trap states.

REFERENCES

- [1] W. Kuhn, N. E. Lay, E. Grigorian, D. Nobbe, I. Kuperman, J. Jeon, K. Wong, Y. Tugnawat, and X. He, "A microtransceiver for UHF proximity links including mars surface-to-orbit applications," *Proceedings of the IEEE*, vol. 95, no. 10, pp. 2019–2044, 2007-10. doi: 10.1109/JPROC.2007.905092.
- [2] D. Braga, S. Li, and F. Fahim, "Cryogenic electronics development for high-energy physics: An overview of design considerations, benefits, and unique challenges," *IEEE Solid-State Circuits Magazine*, vol. 13, no. 2, pp. 36–45, 2021. doi: 10.1109/MSSC.2021.3072804.
- [3] B. Prabowo, G. Zheng, M. Mehrpoo, B. Patra, P. Harvey-Collard, J. Dijkema, A. Sammak, G. Scappucci, E. Charbon, F. Sebastiano, L. M. K. Vandersypen, and M. Babaie, "13.3 a 6-to-8ghz 0.17mw/qubit cryo-CMOS receiver for multiple spin qubit readout in 40nm CMOS technology," in 2021 IEEE International Solid- State Circuits Conference (ISSCC), pp. 212–214, IEEE, 2021-02-13. doi: 10.1109/ISSCC42613.2021.9365848.
- [4] B. Patra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, 2018-01. doi: 10.1109/JSSC.2017.2737549.
- [5] S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, C. Cantaloube, N. Dick, G. C. Gardner, M. J. Manfra, and D. J. Reilly, "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nature Electronics*, vol. 4, no. 1, pp. 64–70, 2021-01-25. doi: 10.1038/s41928-020-00528-y.
- [6] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE Journal* of the Electron Devices Society, vol. 6, pp. 996–1006, 2018. doi: 10.1109/JEDS.2018.2821763.
- [7] A. Beckers, F. Jazaeri, A. Ruffino, C. Bruschini, A. Baschirotto, and C. Enz, "Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing," in 2017 47th European Solid-State Device Research Conference (ESSDERC), pp. 62–65, IEEE, 2017-09. doi: 10.1109/ESSDERC.2017.8066592.
- [8] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Design-oriented modeling of 28 nm FDSOI CMOS technology down to 4.2 k for quantum computing," in 2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp. 1–4, IEEE, 2018-03. doi: 10.1109/ULIS.2018.8354742.
- [9] S.-H. Hong, G.-B. Choi, R.-H. Baek, H.-S. Kang, S.-W. Jung, and Y.-H. Jeong, "Low-temperature performance of nanoscale MOSFET for deep-space RF applications," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 775–777, 2008-07. doi: 10.1109/LED.2008.2000614.
- [10] D. Prasad, M. Vangala, M. Bhargava, A. Beckers, A. Grill, D. Tierno, K. Nathella, T. Achuthan, D. Pietromonaco, J. Myers, M. Walker, B. Parvais, and B. Cline, "Cryo-computing for infrastructure applications: A technology-to-microarchitecture co-optimization study," in 2022 *International Electron Devices Meeting (IEDM)*, pp. 23–5, IEEE, 2022. doi: 10.1109/IEDM45625.2022.10019436.
- [11] N. Kurd, J. Barkarullah, R. Dizon, T. Fletcher, and P. Madland, "A multigigahertz clocking scheme for the pentium(r) 4 microprocessor," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 11, pp. 1647–1653, 2001-11. doi: 10.1109/4.962284.

- [12] Min Park and M. H. Perrott, "A VCO-based analog-to-digital converter with second-order sigma-delta noise shaping," in 2009 IEEE International Symposium on Circuits and Systems, pp. 3130–3133, IEEE, 2009-05. doi: 10.1109/ISCAS.2009.5118466.
- [13] J. Yu, F. F. Dai, and R. C. Jaeger, "A 12-bit vernier ring timeto-digital converter in 0.13 µm CMOS technology," *IEEE Journal* of Solid-State Circuits, vol. 45, no. 4, pp. 830–842, 2010-04. doi: 10.1109/JSSC.2010.2040306.
- [14] J. Burr, "Cryogenic ultra low power CMOS," in 1995 IEEE Symposium on Low Power Electronics. Digest of Technical Papers, pp. 82–83, IEEE, 1995. doi: 10.1109/LPE.1995.482473.
- [15] H. Bohuslavskyi, S. Barraud, V. Barral, M. Casse, L. Le Guevel, L. Hutin, B. Bertrand, A. Crippa, X. Jehl, G. Pillonnet, A. G. M. Jansen, F. Arnaud, P. Galy, R. Maurand, S. De Franceschi, M. Sanquer, and M. Vinet, "Cryogenic characterization of 28-nm FD-SOI ring oscillators with energy efficiency optimization," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3682–3688, 2018-09. doi: 10.1109/TED.2018.2859636.
- [16] I. V. Vernik, T. A. Ohki, M. B. Ketchen, and M. Bhushan, "Performance characterization of PD-SOI ring oscillators at cryogenic temperatures," in 2010 IEEE International SOI Conference (SOI), pp. 1–2, IEEE, 2010-10. doi: 10.1109/SOI.2010.5641394.
- [17] R. Saligram, W. Chakraborty, N. Cao, Y. Cao, S. Datta, and A. Raychowdhury, "Power performance analysis of digital standard cells for 28 nm bulk CMOS at cryogenic temperature using BSIM models," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 7, no. 2, pp. 193–200, 2021-12. doi: 10.1109/JX-CDC.2021.3131100.
- [18] W. Riley and D. Howe, "Handbook of frequency stability analysis," 2008-07-01 00:07:00 2008.
- [19] D. Allan, "Statistics of atomic frequency standards," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 221–230, 1966. doi: 10.1109/PROC.1966.4634.
- [20] D. Allan and J. Barnes, "A modified "allan variance" with increased oscillator characterization ability," in *Thirty Fifth Annual Frequency Control Symposium*, pp. 470–475, IEEE, 1981. doi: 10.1109/FREQ.1981.200514.
- [21] T. Hoque, M. Mustapa, F. Amsaad, and M. Niamat, "Assessment of NAND based ring oscillator for hardware trojan detection," in 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWS-CAS), pp. 1–4, IEEE, 2015-08. doi: 10.1109/MWSCAS.2015.7282110.
- [22] FR4 describes a group of fiberglass epoxy resin materials that conform to National Electrical Manufacturers Association standard LI 1-1998.
- [23] F. Teyssandier and D. Prêle, "Commercially Available Capacitors at Cryogenic Temperatures," in *Ninth International Workshop on Low Temperature Electronics - WOLTE9*, (Guaruja, Brazil), June 2010.
- [24] F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 1, pp. 56–62, 1999-01. doi: 10.1109/82.749085.
- [25] R. Asanovski, A. Grill, J. Franco, P. Palestri, A. Beckers, B. Kaczer, and L. Selmi, "New insights on the excess 1/f noise at cryogenic temperatures in 28 nm CMOS and ge MOSFETs for quantum computing applications," in 2022 International Electron Devices Meeting (IEDM), pp. 30.5.1–30.5.4, IEEE, 2022-12-03. doi: 10.1109/IEDM45625.2022.10019388.
- [26] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. Wiley-Interscience, 3rd ed ed., 2007.
- [27] R. Asanovski, A. Grill, J. Franco, P. Palestri, A. Beckers, B. Kaczer, and L. Selmi, "Understanding the excess 1/f noise in MOSFETs at cryogenic temperatures," *IEEE Transactions on Electron Devices*, pp. 1–7, 2023. doi: 10.1109/TED.2022.3233551.
- [28] A. Hajimiri, S. Limotyrakis, and T. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790– 804, 1999-06. doi: 10.1109/4.766813.
- [29] E. Burstein, A. L. McWhorter, P. H. Miller, D. T. Stevenson, and P. B. Weisz, *Semiconductor Surface Physics*. University of Pennsylvania Press, 1957.
- [30] S. Christensson, I. Lundström, and C. Svensson, "Low frequency noise in MOS transistors—i theory," *Solid-State Electronics*, vol. 11, no. 9, pp. 797–812, 1968. doi: 10.1016/0038-1101(68)90100-7.
- [31] H. Oka, T. Matsukawa, K. Kato, S. Iizuka, W. Mizubayashi, K. Endo, T. Yasuda, and T. Mori, "Toward long-coherence-time si spin qubit: The origin of low-frequency noise in cryo-CMOS," in 2020 IEEE Symposium on VLSI Technology, pp. 1–2, IEEE, 2020-06. doi: 10.1109/VLSITechnology18217.2020.9265013.

- [32] M. Kirton and M. Uren, Noise in Solid-state Microstructures: A New Perspective on Individual Defects, Interface States and Low-frequency (1/f) Noise. Advances in physics, Taylor & Francis, 1989.
- [33] D. Fleetwood, H. Xiong, Z.-Y. Lu, C. Nicklaw, J. Felix, R. Schrimpf, and S. Pantelides, "Unified model of hole trapping, 1/f noise, and thermally stimulated current in MOS devices," *IEEE Transactions* on Nuclear Science, vol. 49, no. 6, pp. 2674–2683, 2002-12. doi: 10.1109/TNS.2002.805407.
- [34] K. P. Cheung and J. P. Campbell, "Non-tunneling origin of the 1/f noise in SiC MOSFET," in 2018 International Conference on IC Design & Technology (ICICDT), pp. 165–168, IEEE, 2018-06. doi: 10.1109/ICICDT.2018.8399782.
- [35] J. Campbell, J. Qin, K. Cheung, L. Yu, J. Suehle, A. Oates, and K. Sheng, "Random telegraph noise in highly scaled nMOSFETs," in 2009 IEEE International Reliability Physics Symposium, pp. 382–388, IEEE, 2009. doi: 10.1109/IRPS.2009.5173283.