UNIVERSITY OF CALIFORNIA SAN DIEGO

Recursive Switched-Capacitor Circuit Topologies for Miniaturized Power Conversion

A dissertation submitted in partial satisfaction of the
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by

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2018

The dissertation of Loai G. Salem is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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DEDICATION

To my parents

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The material in this dissertation is based on the following published papers.

Chapter 2 is based on and mostly a reprint of the following publications:

- L.G. Salem and P.P. Mercier, "A recursive switched-capacitor DC-DC converter achieving 2^N-1 ratios with high efficiency over a wide output voltage range," in IEEE Journal of Solid-State Circuits (JSSC), Dec. 2014, vol. 49, no. 12, pp. 2773-2787.

- L.G. Salem and P.P. Mercier, "An 85%-efficiency fully-integrated 15-ratio recursive switched-capacitor DC-DC converter with 0.1-2.2V output voltage range," 2014 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2014, pp. 88-89.

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L.G. Salem and P.P. Mercier, "A sub-1.55mV accuracy 36.9ps FOM digital low-dropout regulator employing switched-capacitor resistance," 2018 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2018.

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ABSTRACT OF THE DISSERTATION

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Power conversion circuits are essential components in every electronic device from laptops and cellphones to wearable and implantable devices. These circuits convert the DC voltage of the battery or energy source to the appropriate DC level or AC form required by a load. The key challenge of this class of circuits is that they often define the size and energy of an electronic system. This is since the volume-size and quality-factor of the required inductors render power conversion circuits disproportionately large and lossy to the rest of the electronic system.

This work aims to make power conversion circuits smaller without losing power efficiency by developing new circuit topologies that primarily rely on capacitors instead of inductors. The developed switched capacitor DC-to-DC and DC-to-AC converters rely on architecting the

governing current and voltage equations such that they follow efficient mathematical formulae to enable the minimum loss and/or the smallest volume size as compared to prior topologies. The developed topologies thus enable switched capacitor converters to be as efficient as the industry's flagship inductor-based solutions, however in orders-of-magnitude smaller size. Moving forward, such an approach of relying on electric instead of magnetic energy transfer enables the exploitation of fabrication-technology feature-size scaling to shrink the total electronic system size beyond what is feasible through today's technologies.

Chapter 1

Introduction

1.1 What is a Power Converter?

A power converter is a circuit that converts the level and/or form (whether DC or AC) of an input voltage to a desired target voltage while preserving the output power equal (or close) to the input power. In mechanical terms, a power converter acts as a valve that changes a fluid velocity at its ends while preserving the fluid mass (i.e. without leaking the fluid). In this sense, a linear voltage regulator is not considered as a power converter. This is since a linear voltage regulator steps down the input voltage by burning the energy of the excess voltage difference as heat in a series resistance. In mechanical analogy, this is equivalent to reducing the output fluid flow rate by creating a cut in the carrying pipe to get rid of the excess flow.

Power converters are essential elements in almost every electronic device. As discussed, they can step down/up the level of the input voltage and thus can control the amount of electric power delivered to a resistive load. This power control capability is of critical importance in present integrated circuit industry. Specifically, power management circuits control the flow of electric energy from the system battery or energy source to the supplied circuitry. This is similar to the role of the gas pedal in a vehicle where connecting the intake of the employed gasoline

engine directly to the fuel tank results in a huge waste of energy.

Additionally, power converters change the input electric power from a DC form into an AC form and vice versa. A power converter can step down/up the input DC or AC voltage to a target DC or AC voltage level at the output, respectively, in order to realize the required power control. This is essential to the functionality of the supplied load. For example, a 60 Hz power inverter converts the input DC electric power from a solar cell to an output power of alternating currents to supply home appliances. Furthermore, the amplitude of the resulted output voltage in many cases has to be precisely controlled to a target reference level. For instance, a power amplifier converts the input DC power from the supply to an output AC (or RF) power of an amplitude controlled in accordance with the input RF signal; otherwise, the transmitted power cannot be modulated according to the carried data.

1.2 Switched Inductor versus Switched Capacitor Power Conversion

Power converters employ switches and energy storage elements, i.e. inductors/transformers and capacitors to perform the required conversion. Unlike resistors, inductors and capacitors can result in a voltage drop while storing the energy of the voltage difference between the input and output ports instead of dissipating it. Additionally, an energy storage element can produce a voltage step up which cannot be achieved using a resistor. Therefore, these elements enable power converters to step down/up the input voltage while achieving high efficiency. However, as a reactive element, an inductor (capacitor) requires a change in current (voltage) in order to shuttle energy. Since typically an input DC voltage source is employed or an output DC level is required, switches are essential elements in every power converter to allow the reactive elements to store energy and release it back to the load. Unfortunately, the non-idealities of the energy storage elements as well as the equivalent on-resistance of the switches introduce power losses

and thereby degrade the output-to-input power ratio or efficiency below 100%.

1.2.1 Challenges of Switched-Capacitor Power Conversion

Most power conversion circuits in the industry rely on inductors or transformers for energy shuttling. Unlike the switched-inductor (SL) DC-DC approach, switched-capacitor (SC) DC-DC converters can achieve high efficiency only at discrete input-to-output conversion ratios. For example, a 2:1 SC is almost 100% efficient in dividing the input battery voltage (V_{BAT}) by 2 while its efficiency rapidly falls at other voltages. This drawback has plagued the capacitive approach since the early 1970's and made it impractical to use in the $40-Billion power management market despite its inherent suitability for miniaturization in CMOS processes. It stands to reason that employing more ratios, through multiple SC networks, at equidistant conversion steps could provide a semi-flat efficiency profile versus voltage, just like the inductive approach. Unfortunately, using prior SC topologies, the efficiency of the ratios of higher resolution than 2-bit falls significantly below the 2-bit linear-regulation efficiency i.e. when using a lossy resistance in series with the 2-bit networks to provide V_{out} between the fixed 4:1, 2:1, 4:3 ratios. This is because the charge-sharing loss increases almost exponentially with the resolution (N) in prior SC topologies e.g. 3-bit ratios' loss is 7$\times$ the 2-bit loss. Therefore, the SC efficiency profile versus the voltage traditionally has peaks at 3 discrete ratios with steep 30%-deep valleys in between, as a saw-tooth, which is not suitable for portable consumer applications.

1.2.2 Advantages of Switched-Capacitor Power Conversion

Present power conversion often defines the size and energy of an electronic system, where the volume-size and quality-factor of the required large inductors render power conversion circuits disproportionately large and lossy to the rest of the electronic system. In fact, power conversion circuits are becoming the bottleneck for the system size and energy in the integrated circuit

industry. With the increasing number of components inside a System-on-Chip (SoC), the required per-block power management to leash the soaring levels of chip power drives the need for the full integration of DC-to-DC and DC-to-AC conversion to avoid increased cost and limited bandwidth of the supply control. Unfortunately, on-die inductors not only occupy large area but also suffer from a large series resistance (ESR) and losses to realize a fully-integrated switched-inductor (SL) DC-DC solution with acceptable level of efficiency.

On the other hand, switched-capacitor converters have the potential to make power conversion smaller in size. Capacitors can store the same amount of energy as an inductor but in approximately two orders of magnitude smaller volume. Theoretically, the inductance of a structure is proportional to the area that the magnetic flux crosses. On the other hand, the capacitance of a structure is inversely proportional to the separation between the conducting plates. Therefore, to a first order, increasing the capacitance results in a smaller volume while increasing the inductance results in a larger one.

1.3 Developments in This Work

The key challenge of switched-capacitor (SC) power converters is that their energy conversion is only efficient at a few discrete input-to-output voltage ratios unlike the continuous switched-inductor (SL) conversion. This work addresses this challenge by developing new DC-to-DC/RF circuit topologies that enable a large number of input-to-output conversion ratios at arbitrarily small steps to reproduce the SL continuous capability without sacrificing efficiency or size.

The first part of this work is concerned with DC-to-DC conversion and introduces new SC topologies that enable a practical replacement to the bulky SL DC-to-DC conversion. Chapter 2 introduces a recursive binary topology by reproducing the recursive formula in a switched network form. Unlike prior SC topologies of divergent loss, the charge-sharing loss in the

recursive topology follows a convergent geometric binary series with N that settles at the absolute minimum loss value of 1.67× the 2-bit ratios' loss at arbitrarily high resolutions. Therefore, the topology scores the highest efficiency among prior SC topologies in integrated applications. Via the recursive topology, the higher resolution ratios can effectively fill the 30% efficiency gaps in between the 2-bit ratios, enabling semi-continuous profile like the inductive approach and hence a CMOS-compatible replacement for the SL converters. Additionally, chapter 3 develops a recursive flying-domain DC-DC converter that achieves voltage-conversion not by switching a size-consuming passive element (inductor or capacitor), but rather, by switching the load itself to achieve high power density and efficiency.

Chapter 4 is concerned with enabling capacitive DC-DC conversion for high power levels. For high power, it is more economical to implement the required capacitors as discrete elements using other technologies instead of CMOS or SOI. A baseline discrete capacitor has 25× smaller footprint, 5× smaller thickness, 21× lower cost, and more importantly, 700× lighter weight than an inductor for the same energy storage capability. It stands to reason that a competitive power management integrated circuit (PMIC) can be realized by using capacitors. However, the industry-standard SC charge-pump TPS6050x from Texas Instruments, and similar ICs from Analog Devices, Maxim Integrated among others, employs only three ratios and thus its efficiency peaks at the three ratios and rapidly falls at other V_{out} values as a saw tooth. To replicate the inductive flat-efficiency profile, 31 ratios at equidistant steps of 5-bit resolution are needed. Realizing this large number of ratios with the industry-standard topology requires 31 capacitors which occupies about 2× larger board space and a humongous assembly cost than the single inductor in the SL approach. In contrast, chapter 4 shows that by operating the switches of the various stages of a SC converter at binary-weighted frequencies instead of the traditional approach of having them all at the same operating frequency enables the smallest number of capacitors to realize a given ratio. By operating the stages at different frequencies, new switched-network phases result which impose extra Kirchhoff's Voltage Law (KVL) constraints and thereby some

capacitors can be safely removed without compromising the unique solution of the KVL system i.e. the switched network reaches a valid steady-state output voltage. Through the proposed Frequency-Scaled Gear-Train topology, only N capacitors are required for N-bit ratios. This enables a practical replacement for the traditional SL PMIC of 1.5× smaller footprint, 4× lower cost, and more importantly, 5× smaller thickness and 123× lighter weight.

The second part of this work is concerned with enabling a capacitive replacement to the contemporary inductive DC-to-AC/RF power conversion. In chapter 5, a new SC power amplifier (PA) topology is developed that can produce a large output power at a high RF voltage amplitude while employing low-voltage transistors. Current PA research endeavors to realize the required high output power by increasing the output current through size-consuming inductive transformation networks. This is because the employed PA switches cannot tolerate high voltages (HVs) in advanced CMOS fabrication technologies. Unfortunately, producing large power levels at high currents results in quadratically increasing resistive losses. Instead, the new SC topology stacks entire PA unit cells on top of each other to block higher voltages than what a single transistor can tolerate. Then, by switching the supply and ground of a stack of N-i-1 PA cells through a stack of N-i cells, for i from 0 to N-2, a 1:N DC-to-RF conversion ratio can be realized to produce a high power RF signal using low-voltage transistors.

Chapter 6 introduces SC based adiabatic clocking. Clock distribution in a modern multi-core processor often consumes more than one-third of the total power budget. For more than two decades, IBM among other companies have pursued a higher market position by reducing the dominant clock power using resonant clocking schemes. Size-consuming inductors are employed to tune-out the clock equivalent capacitance at a single target frequency. The POWER8 server processor from IBM employs 114 on-chip inductors to achieve 33% clock power reduction. Instead, chapter 6 develops a DC-to-AC topology that reduces the clock power by a factor of N across an arbitrarily wide range of clock frequencies and without using inductors. The topology sequentially charges and discharges the clock capacitance through an N-step waveform within

¡18% of the clock cycle time which reduces clock power by N×. The prototyped IC implements a 3-step clock driver and achieves 55.6% clock power reduction across 1M-2GHz without using inductors, enabling up to 200× reduction in size.

The third part of this work introduces new all-digital low dropout voltage (LDO) regulator circuit topologies. All-digital LDOs suffer from an output voltage of slow response time and low accuracy which have hindered their deployment in consumer electronics. Towards this problem, chapter 7 develops the first all-digital LDO that is faster than an analog LDO, under the same power consumption, via a new recursive LDO topology. Further, chapter 8 contributs a new class of digital LDOs that replaces the traditional programmable switch-array, the main actuator in an LDO, with a switched-capacitor bilinear resistance to regulate the output voltage. This enables digital LDOs to be as accurate as their analog counterparts, achieving a realistic digital replacement to analog LDOs.

Part I

Miniaturizing DC-to-DC Power Conversion

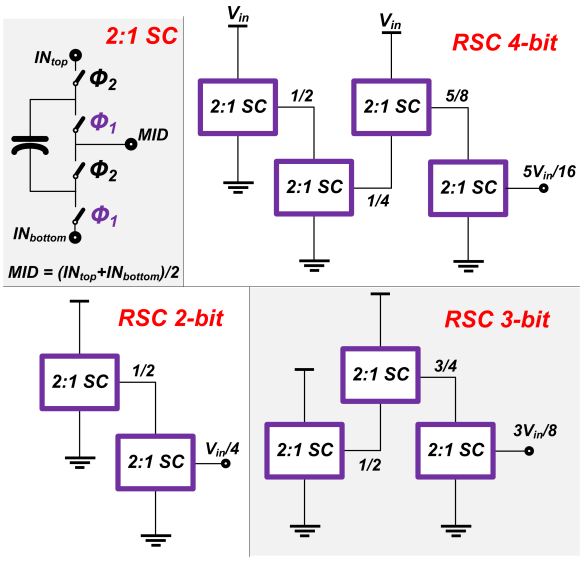
Chapter 2

Recursive Switched-Capacitor DC-to-DC Converters

2.1 Introduction

Todays digital integrated circuits achieve a balance between performance and energy efficiency through dynamic voltage scaling (DVS) of individual processing cores in accordance with performance needs. As the number of voltage domains increases in todays system-on-chips (SoCs), generation of each supply voltage must occur not only efficiently, but within a small area. While linear regulators are compact and achieve fast response times [2, 3], their efficiencies are determined by the ratio of output to input voltage, potentially limiting system-level energy-efficiency [4, 5, 6]. On the other hand, switched-inductor DC-DC converters can achieve high efficiencies, yet typically require large off-chip inductors [7] or increased packaging complexity [8, 9, 10, 11, 12], limiting their ability to power many independent voltage domains in a small volume. To simultaneously address the efficiency/size trade-off, fully-integrated switched capacitor (SC) DC-DC converters utilize high-Q capacitors available in typical CMOS processes to convert and regulate power in an energy- and area-efficient manner

[13, 14, 5, 15, 16, 17, 18, 19, 20].



(a) Examples of *Recursive* SC topology.

```
// init: IN_bottom = 0, IN_top = V_in
RBinary (V_TARGET, IN_bottom, IN_top)
{
  V_out = {V(IN_top) + V(IN_bottom)} / 2
  if (MID < V_TARGET)
    return RBinary(V_TARGET, MID,
V_in)
  else if (MID > V_TARGET)
    return RBinary(V_TARGET, 0, MID)
  else
    return
}
```

(b) *Recursive* SC topology pseudo-code generator.

Figure 2.1: The *Recursive* switched-capacitor realization of the ratios 1/4, 3/8, and 5/16, and topology pseudo-code. Each SC cell comprises two out-of-phase 2:1 SC for a well-posed SC network.

Unlike switched-inductor DC-DC converters, however, SC converters are only efficient at discrete ratios of input-to-output voltages, constricting efficient DVS operation to small supply voltage ranges. Increasing the number of reconfigurable ratios can solve this; however, doing so introduces two main challenges: capacitance utilization and relative sizing. In a fully integrated SC

converter, the achievable efficiency is limited by the amount of committed capacitance; disabling even a small fraction of such capacitance significantly lowers the efficiency. Additionally, ensuring optimal relative sizing among the constituent capacitors can improve efficiency considerably [21]. Unfortunately, the complexity of conventional topologies, including the number of necessary capacitors and reconfigurations switches, increases significantly with the number of ratios, making simultaneous 100% capacitance utilization and optimal relative sizing extremely challenging. Thus, most SC converter designs employ only a small number of ratios [22, 13, 17, 23, 24], often resulting in large efficiency drops in-between the available ratios.

This chapter presents the first demonstration of a SC converter that is reconfigurable amongst $2^N - 1$ ratios without disconnecting a single capacitor while ensuring optimal relative sizing and high efficiency across a large output voltage range. The proposed *Recursive* SC DC-DC converter topology (RSC) [25], shown in Fig. 2.1, recursively divides the delivered output charge across N 2:1 cells connected in cascade to generate N-bit ratios. By maximizing the number of input voltage and ground connections, charge-sharing losses are minimized, and in fact become a convergent geometric series with minimal additional losses incurred beyond 4-bit ratios. Given the inherently modular nature of the converter, 100% capacitance utilization is ensured by reconfiguring cell connections either in cascade (for high resolutions) or parallel (for lower resolutions), with binary slicing of the largest cascaded cell in order to enable reconfiguration amongst odd and even resolutions, all while ensuring optimal relative sizing.

This chapter is organized as follows: Section II introduces the RSC topology and discusses its theoretical performance compared with prior topologies. Section III presents architectural implementation details of a 4-bit RSC converter, while Section IV presents detailed circuit design. Experimental results of the test chip that verify the predicted performance are provided in Section V.

2.2 Recursive Switched-Capacitor Topology

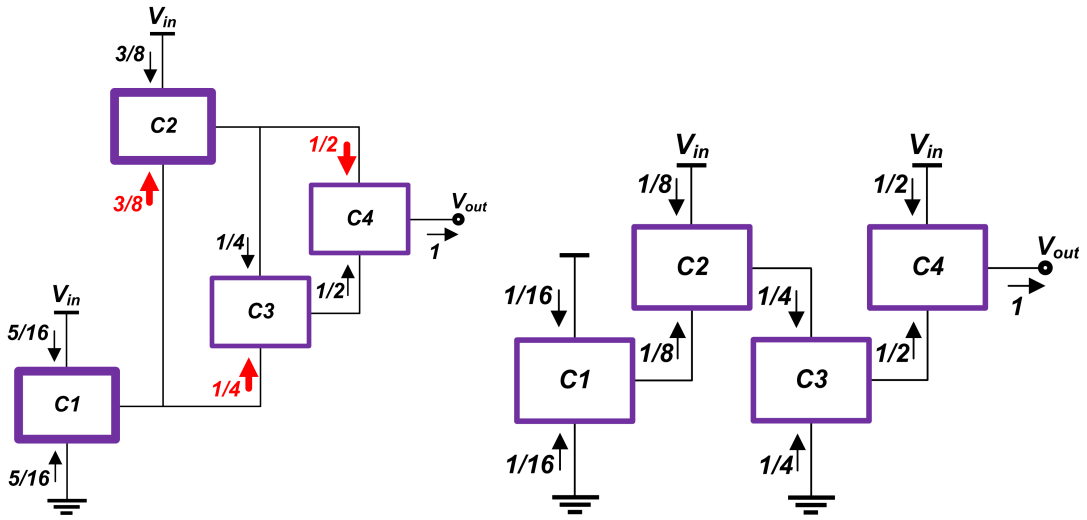
The most basic RSC building block is a 2:1 SC converter. As shown in Fig. 2.1a, a 2:1 SC can be considered as a three-port circuit that includes two input ports IN_{top} and IN_{bottom} to receive a high and low input voltages, respectively, and an output port *MID* that provides the average of the voltages at the input ports, i.e. $(IN_{top} + IN_{bottom})/2$. The 2:1 SC cell equally loads its output port current on the two input ports (IN_{top}, IN_{bottom}). The following subsections discuss how 2:1 SC building cells can be connected to realize $2^N - 1$ conversion ratios while minimizing losses.

2.2.1 Topology Definition and Steady-State Loss Analysis

Figure 2.1b shows the *Recursive* SC topology pseudo-code. Starting with a single 2:1 SC that divides the converter input voltage, V_{in}, into two intervals (0-to-$V_{in}/2$, $V_{in}/2$-to-V_{in}), the topology inserts a 2:1 SC cell in series between the previous cell output *MID* and the converter ground 0, or stacked between V_{in} and the output *MID* of the previous 2:1 cell, repeatedly, until the desired binary conversion ratio $m/2^N$ is realized, where $m < 2^N$. Figure 2.1a demonstrates examples of the ratios 1/4, 3/8, and 5/16 at 2-, 3-, and 4-bit resolutions, respectively.

The proposed topology minimizes cascaded losses by maximizing the number of input voltage, V_{in}, and ground, 0, connections. Specifically, each 2:1 stage *Ci* has at least one input port connected to either the input voltage V_{in} or the converter ground 0, and thus each stage loads half of its output charge q_i on the input supply, V_{in}, or ground, 0, instead of loading such charge on a previous cascaded stage. For example, Fig. 2.2 illustrates two different configurations that both realize an 11/16 ratio. In Fig. 2.2a, the last stage $C4$ loads half of the output charge q_{out} on the 2^{nd} stage, $C2$, which in turn loads the first stage, $C0$, with $3q_{out}/8$. The third stage, $C3$, loads the first stage by an additional $q_{out}/4$, and thus the total charge delivered by the first stage is $5q_{out}/8$. In contrast, the RSC converter employs the configuration shown in Fig. 2.2b, where the IN_{top}

of $C4$ and the IN_{bottom} of $C3$ are directly connected to the converter input, V_{in}, and the ground, 0, respectively, and therefore, the loaded charge on $C2$ and $C1$ are both reduced by $q_{out}/2$. For an arbitrary recursion depth N, each stage is loaded with a charge q_i that is divided by a binary weight of the total output charge, q_{out}, such that $q_i = q_{out}/2^{N-i}$, where i is the stage order in the cascade.



(a) Non-optimal cascading connection. (b) RSC optimal connection, minimal inter-stage loading.

Figure 2.2: Charge flow through two inter-cell connections to realize the same ratio 11/16 (a) non-optimal cascading (b) proposed RSC connection. Bold blocks are loaded with extra charge than the corresponding blocks in (b) with RSC connection. Bold arrows represent the extra loading charge.

It is known that the intrinsic loss mechanisms in a SC converter can be modeled by a finite output resistance, R_{out} in either the slow or fast-switching limit (SSL or FSL, respectively): R_{SSL}, where the charge-sharing loss dominates, and R_{FSL}, where the switches' on-resistance dominates the losses [21, 26]. In the SSL, the total energy loss through the converter can be found by adding the charge-sharing loss across each capacitor C_i, $(q_i/2)^2/C_i$, and by normalizing the charge-sharing power loss by the squared output current I_L^2, i.e. $(q_{out} f_{sw})^2$, the equivalent output resistance R_{SSL} can be calculated as:

$$R_{SSL} = \sum_{i=1}^{N} \left(\frac{1}{2^{N-i+1}} \right)^2 \frac{1}{f_{sw} C_i}, \tag{2.1}$$

where C_i is the total capacitance of the two flying capacitors per stage. The derived R_{SSL} is for a symmetric RSC, where each cell consists of two oppositely-phased 2:1 SC, which eliminates any charge-balance DC capacitor between the cascaded stages. Similarly, at the FSL, the current through each switch becomes the delivered current by that stage, which is a binary weighted fraction of the load current, I_L (i.e., $I_L/2^{N-i}$). Thus, the equivalent output resistance R_{FSL}, for a 50% duty-cycle converter clock, is:

$$R_{FSL} = \sum_{i=1}^{N} \sum_{j=1}^{4} \frac{1}{2} \left(\frac{1}{2^{N-i}} \right)^2 R_{i,j}, \tag{2.2}$$

where the summation over j accounts for the four switches per stage i, and each switch resistance $R_{i,j}$ results from two parallel switches in a symmetric RSC of eight switches. The total equivalent output resistance R_{out} at a given switching frequency, f_{sw}, occurring between the two asymptotes can be approximated by the Euclidean norm of the two limits, R_{SSL} and R_{FSL} [21]. From Eqns. 2.1 and 2.2, the RSC equivalent output resistance R_{out} only depends on N and does not change across the resolution ratios.

Allocating a larger capacitance, C_i, for each stage results in a lower voltage swing, ΔV_i, and lower charge-sharing loss, as dictated by Eqn. 2.1. Given the limited available capacitance in a fully-integrated SC converter, it is important to find the relative sizing of each stage capacitance C_i from the total available on-die capacitance C_{tot} to realize the minimal R_{SSL}. For fully-integrated capacitors with single-voltage-rating and with no stacking of switches to block higher voltages, the optimal capacitance and conductance relative-sizing match the relative charge transferred through each capacitor or switch, [21, 27, 28], and hence is binary weighted of the total available capacitance C_{tot} and conductance G_{tot}:

$$C_i = \left(\frac{2^{i-1}}{2^N - 1}\right) C_{tot}, \tag{2.3}$$

$$G_i = \frac{1}{4}\left(\frac{2^{i-1}}{2^N - 1}\right) G_{tot}. \tag{2.4}$$

With such optimal sizing, the equivalent output impedance at the two asymptotes can be found as:

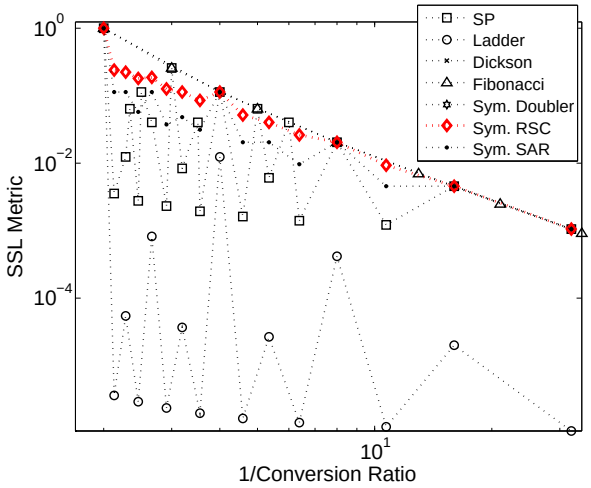
$$R^*_{SSL} = \frac{1}{f_{sw} C_{tot}} \left(1 - \frac{1}{2^N}\right)^2, \tag{2.5}$$

$$R^*_{FSL} = \frac{2}{G_{tot}} \left(1 - \frac{1}{2^N}\right)^2. \tag{2.6}$$

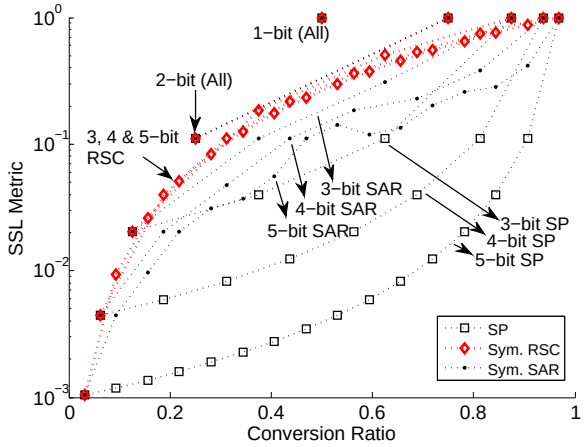
To realize the highest possible efficiency for a given silicon area, it is desired to select the SC topology that incurs the lowest charge-sharing loss, R_{SSL}, to deliver the same q_{out} and conversion ratio. The power-available from a SC converter normalized by the power-available from a 2:1 SC, using the same silicon area, can be used as a metric to compare various SC topologies in the SSL and FSL. After assigning the capacitors appropriate optimal relative sizing, the SSL normalized power-available from a topology at a conversion ratio m/n becomes $M_{SSL} = \left(m/n \Big/ \sum_i a_{c,i}\right)^2$, where $m < n$ and $a_{c,i}$ is the fraction of the output charge q_{out} that flows through the capacitor C_i.

Figure 2.3 compares five conventional SC topologies [29, 30, 31], as well as a Successive Approximation (SAR) SC converter [32] and the proposed RSC converter, using the established SSL metric, M_{SSL}, where the capacitors of each topology are assigned the optimal relative-sizing. The charge multiplier vectors of the various topologies can be found in [33] and through the analysis in [21]. The topologies are compared up to 5-bit binary conversion ratios. The SP topology M_{SSL} is also shown at the ratios 1/6, 1/5, 2/7, 1/3, 2/5, 3/7, while The *Fibonacci* topology M_{SSL} is shown for the *Fibonacci* series ratios 1/21, 1/13, ... , 1/2. All topologies, with the exception of the Ladder topology, have the same M_{SSL} at the minimum and maximum

conversion ratios within each resolution, e.g. 1/2, 1/4, 1/8, 1/16, 1/32 and 3/4, 7/8, 15/16, 31/32, respectively. As shown in Fig. 2.3b, Due to the binary division of the output charge across the various stages, the RSC cascading loss converges to an upper limit, $1/(f_{sw}C_{tot})$, at large resolutions N, without further M_{SSL} degradation. The other topologies exhibit an M_{SSL} eye opening with higher resolutions N for ratios $m_{odd}/2^N$, where the SSL loss becomes the summation of a divergent series.



(a) Power-available metric for the seven topologies.



(b) Power-available metric for SP, symmetric RSC, and symmetric SAR topologies.

Figure 2.3: The SSL power-available metric, M_{SSL}, for the seven topologies at binary ratios up to 5-bit resolution. The topology of the highest power-available at certain ratio incurs the lowest charge-sharing loss for a given silicon area.

Figure 2.4 shows the R_{SSL}, using a 1F total capacitance and at 1Hz switching frequency for the SP and the RSC topologies, with capacitors of optimal relative-sizing, across binary ratios up to 5-bit resolutions. The RSC normalized R^*_{SSL} saturates at an upper limit of $4\times R_{SSL}$ of a 1/2 ratio. Figure 2.5 shows the FSL optimal-voltage metric [21] for the seven topologies at the same binary ratios as previously discussed. In general for fully-integrated converters, capacitors consume most of the die area, and thus topologies that achieve the lowest SSL loss for a given silicon area (i.e., topologies with the highest M_{SSL}) are desired.

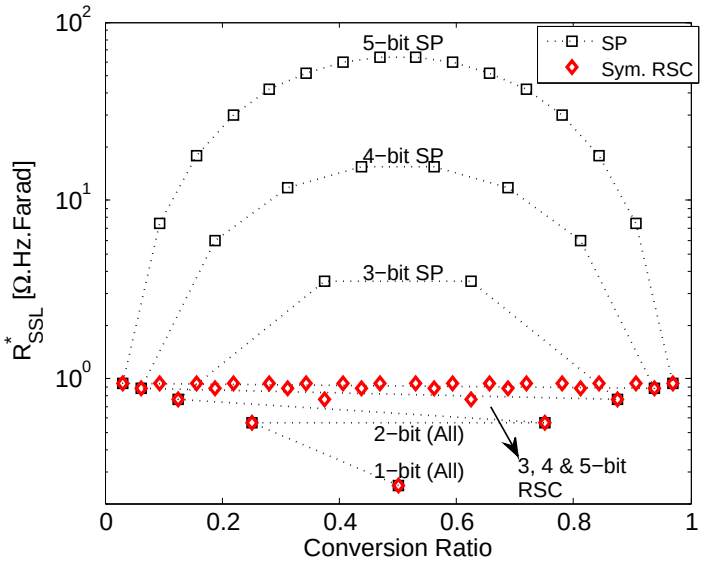


Figure 2.4: The R^*_{SSL} for the SP and symmetric RSC versus the binary ratios using a 1F total capacitance and for a SC converter operated at 1Hz.

2.2.2 Open-Loop Power Stage Optimization

After defining the optimal relative sizing of individual RSC components, it is critical to select the total switch area A_{sw} and switching frequency f_{sw} that result in the maximum efficiency for a given load I_L and input voltage V_{in}. In a fully-integrated SC, the charge-sharing SSL loss constitutes the major loss component. To decrease the SSL loss, either the available capacitance or the switching frequency, and hence switching parasitics, should be increased. In integrated

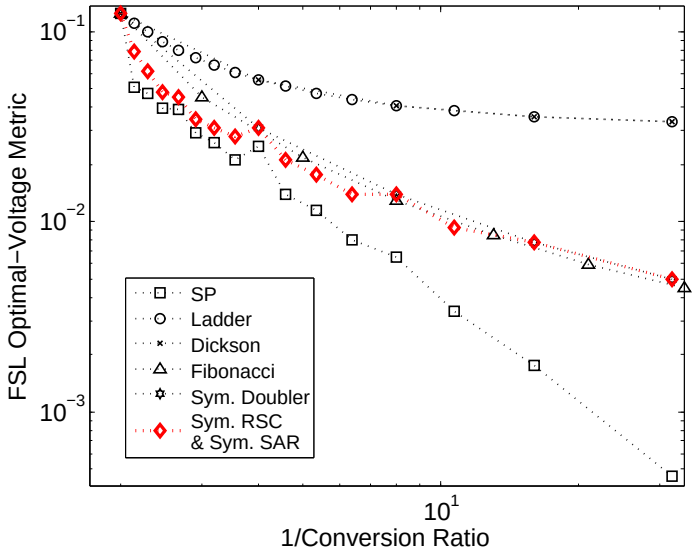


Figure 2.5: The FSL performance metric M_{FSL} of the seven topologies at binary conversion ratios up to 5-bit resolution.

converters, capacitance is not typically considered as a variable in the optimization process, and the maximum available capacitance for a given silicon area is implemented. The maximum efficiency over the design space (A_{sw}, f_{sw}) can be found by minimizing the total losses arising from the intrinsic SC R_{out}, and the switching losses that result from the power switches gate drive as well as the capacitor bottom-plate losses. The drain parasitics of the switches are treated as part of the capacitors bottom-plate parasitics.

Since a RSC consists of individual 2:1 SC cells that provide binary-weighted currents $I_i = I_L/2^{N-i}$, it can be shown that the optimal switching frequency f_{sw}^* and total conductance G_{tot}^* are given by[1]:

$$f_{sw}^* = \frac{1}{4\sqrt[3]{2}} \sqrt[3]{\frac{G_{on}}{C_{gate} V_{gate}^2} \left(\frac{I_L}{C_{tot}}\right)^2} \cdot \sqrt[3]{\left(\frac{2^N - 1}{2^{N-1}}\right)^2}, \tag{2.7}$$

[1]A simple addition of the two loss limits, R_{SSL} and R_{FSL}, is used to express the intrinsic RSC loss which overestimates the total R_{out}. A negligible bottom plate parasitics are assumed, besides the equivalent load resistance R_L is assumed to be larger than R_{out}, to obtain simple intuitive expressions. The formula for a 2:1 SC optimal switch width and frequency in [13] are used in the derivation.

$$\frac{G_{tot}^*}{C_{tot}} = 4\sqrt[3]{4}\sqrt[3]{\frac{G_{on}}{C_{gate}V_{gate}^2}\left(\frac{I_L}{C_{tot}}\right)^2}\cdot\sqrt[3]{\left(\frac{2^N-1}{2^{N-1}}\right)^2}, \tag{2.8}$$

where G_{on} and C_{gate} are the switch conductance density in S/m and the switch gate capacitance per unit width F/m, respectively. V_{gate} is the gate drive voltage, and G_{tot}^*/C_{tot} is the optimal total conductance per unit capacitance. Essentially, G_{tot}^*/C_{tot} sets the intersection point of the SSL and FSL loss components, or the SC corner frequency. The first term in Eqns. 2.7 and 2.8 depends on the technology conductance per gate drive energy loss, and the load current density per unit capacitance. The second term depends on the resolution N, where at 1-bit resolution the optimal values correspond to a 2:1 SC converter. On the other hand, with larger number of cascaded stages N, the optimal f_{sw} and total conductance density reaches an upper limit of approximately 60% above the optimal values of a 2:1 SC converter utilizing the available C_{tot}. Essentially, the allocated capacitance of the last stage at large N becomes $C_{tot}/2$ while supplying I_L load current, and thus the optimal design point shifts by $\sqrt[3]{4}$. From Eqn. 2.8, the optimal total switch area does not change from one ratio to another within a given resolution N, simplifying the implementation of a reconfigurable SC. However, a small change in the optimal total conductance results when the bottom-plate parasitics are significant, and an average total switch width across the various ratios slightly affects the optimal efficiency. The optimal total loss per unit ampere becomes:

$$\frac{P_{loss}^*}{I_L} = 3\sqrt[3]{2}\sqrt[3]{\frac{I_L}{C_{tot}}\Big/\frac{G_{on}}{C_{gate}V_{gate}^2}}\cdot\sqrt[3]{\left(\frac{2^N-1}{2^{N-1}}\right)^4}. \tag{2.9}$$

The minimum loss at the optimal design point depends on the ratio of the current density I_L/C_{tot} to the switch conductance per gate loss, and the required resolution N. However, the efficiency $(1+P_{Loss}/I_LV_{out})^{-1}$ depends on the desired ratio and increases with larger output voltages V_{out}. For arbitrarily large resolutions N, the loss per ampere in Eqn. 2.9 saturates at about 2.5$\times$ the loss of a 2:1 SC that utilizes the same available C_{tot}.

2.3 Recursive Resolution-Reconfiguration Architecture

In order to achieve the highest possible efficiency for a given silicon area, the various ratios must be realized while ensuring 100% utilization of the available on-die capacitance. Additionally, the optimal relative sizing of the constituent capacitors and switches should be guaranteed. Unlike conventional topologies, the proposed RSC topology inherently enables recursive inter-cell connection and recursive binary slicing that can simultaneously achieve both conditions with low-complexity.

2.3.1 Recursive Inter-Cell Connection

The proposed recursive inter-cell connection brings individual cells in parallel instead of disabling them when realizing lower-resolution ratios. Figure 2.6 summarizes the challenge of lowering the resolution in a 4-bit RSC. The converter consists of four 2:1 SC cells connected in succession $C1$, $C2$, $C3$, $C4$ to realize $m_{odd}/2^4$ ratios. As shown, the cells are allocated optimal binary sizing of the total available capacitance, C_{tot}, and conductance, G_{tot}. One method to realize a 1/2 ratio from the 4-bit RSC is to route the output from the first stage using an output selection multiplexer and disabling all other stages. While this will produce the correct output voltage, such an approach wastes the available capacitance in the last three cells $C2$, $C3$, and $C4$, resulting in a 14/15 (93.33%) reduction in the available capacitance for charge transfer, thereby incurring a $15\times$ penalty in R_{SSL}.

On the other hand, the *Recursive* implementation connects the four 2:1 SC cells in parallel when a 1/2 ratio is desired, as shown in Fig. 2.6, which results in 100% capacitance usage and the minimum possible ΔV for a given output charge and silicon area. Similarly, to lower the resolution from 4-bit to 2-bit, the cascade of the last two cells $C3$ and $C4$ is brought in parallel to the cascade of the first two cells $C1$ and $C2$, as shown in Fig. 2.6, ensuring optimal relative sizing, i.e. $\frac{1}{3} : \frac{2}{3}$, and 100% capacitance usage.

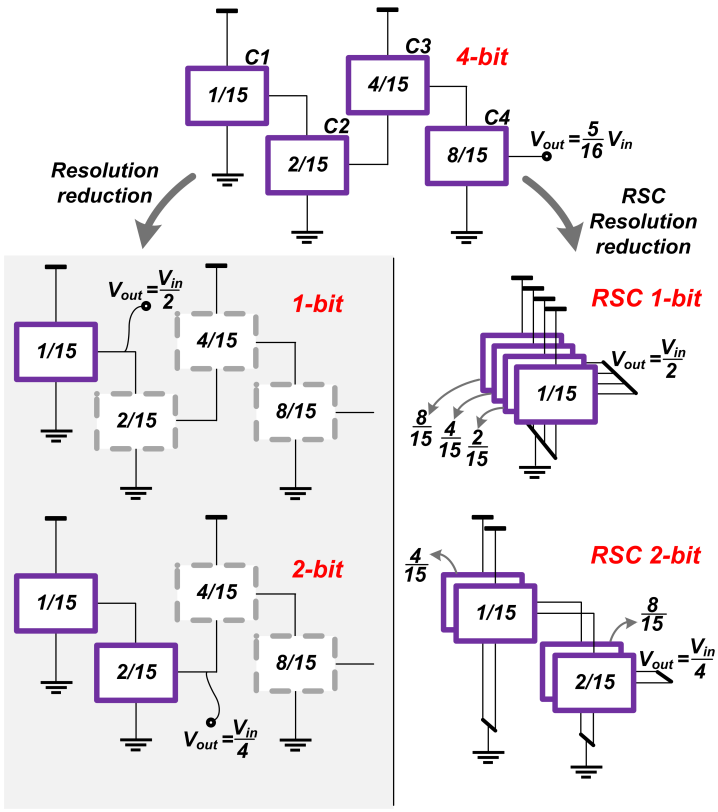


Figure 2.6: Resolution reduction from 4-bit to 1-bit and 2-bit, using output selection multiplexer (left) and recursive inter-cell connection (right). The dashed cells are disabled when realizing lower resolutions.

2.3.2 Recursive Cell Slicing

Recursive-slicing breaks down the largest cell in a cascade into binary weighted sub-cells to enable even-to-odd, and odd-to-odd, resolution reconfiguration, all while satisfying optimal sizing. For example, instead of disabling the fourth cell $C4$ to realize a 3-bit resolution in a 4-bit SC converter, which wastes more than half of the total capacitance, one or more of the four available cells is sliced to realize six cells in total, and then the resulted cells are arrange in two parallel cascades of three cells each. In general terms, it can be shown that recursively slicing the last cell in the cascade CN into $(N-1)$ binary weighted cells results in the optimal solution. Such slicing achieves the optimal relative sizing when lowering the resolution, with a minimum number of sliced sub-cells and thus complexity. The resulted binary sliced sub-cells are connected in

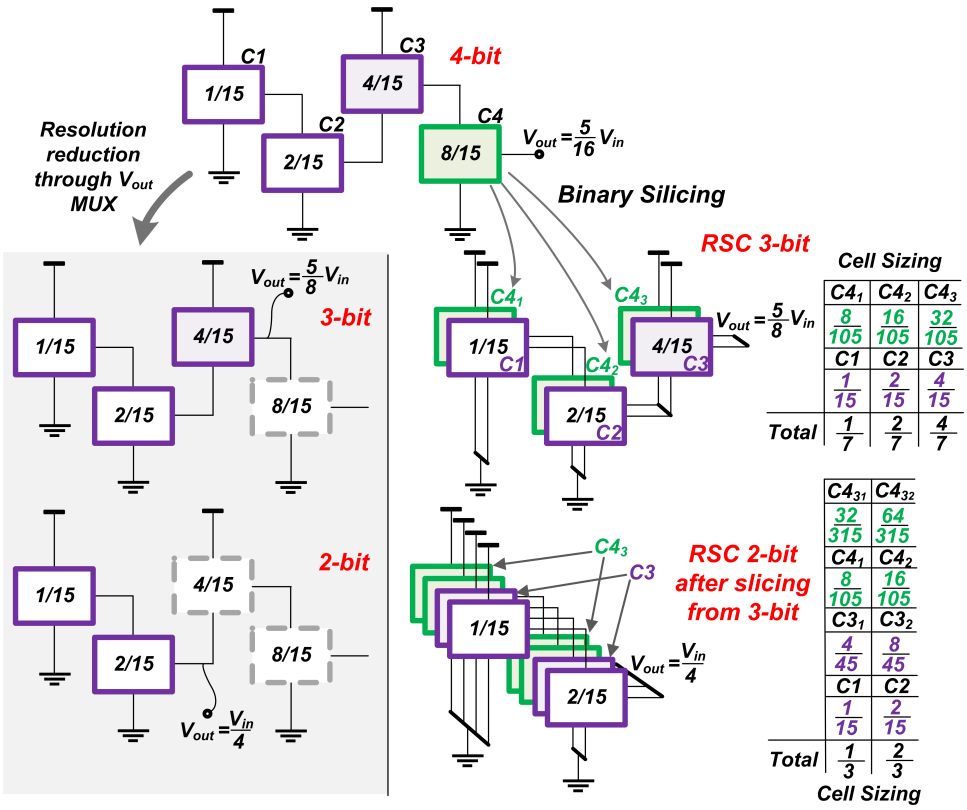


Figure 2.7: Resolution reduction from 4-bit to 3-bit and from 3-bit to 2-bit, using output selection multiplexer (left) and recursive slicing with recursive inter-cell connection (right).

cascade, while operating in parallel with the cascade of the original $(N-1)$ stages. For example, in the 4-bit converter shown in Fig. 2.7, the fourth cell $C4$ is sliced into three sub-cells of binary weights (1/7, 2/7, 4/7), and arranged in parallel to the original cascade of the stages, $C1$, $C2$, $C3$ to achieve $m_{odd}/8$ ratios.

Similarly, when lowering the resolution further from three bits to two bits for $m_{odd}/4$ ratios, the last cells $C3$ and $C4_3$, which in parallel represent the last stage in the 3-bit cascade, are each binary sliced into two sub-cells, $(C3_1, C3_2)$, and $(C4_{31}, C4_{32})$, respectively. Figure 2.7 shows the resulted eight cells sizing and connections of the topology implemented in this chapter. The relative sizing should be as close as possible to the illustrated weighting to achieve the peak performance, however the optimal efficiency is not critically sensitive to mismatches between the various charge-transfer capacitors. It should be noted that four cells are only technically needed in

order to realize all resolutions up to 4-bits; however, in order to guarantee 100% total capacitance utilization among all the possible resolutions while achieving optimal relative sizing, eight cells in total are instead employed.

2.3.3 Inter-Cell Reconfiguration Switches

This section discusses the implementation details to generate the desired ratios with a minimum set of programming switches, and hence minimum added parasitics. The required inter-cell reconfiguration switches can be divided into two main categories: switches to implement ratio-programming within a specific recursion depth N, and switches for resolution reconfiguration.

Ratio-Reconfiguration Switches

Figure 2.8 illustrates a simplified schematic of two 2:1 SC cells connected in parallel. By operating the four switches in each 2:1 cell from the non-overlapped clock phases, Φ_1 and Φ_2, the 1/2 ratio is realized. In order to realize 1/4 and 3/4 conversion ratios in a 2-bit RSC, the two cells in Fig. 2.8 are either connected in cascade or in stack through the added four reconfiguration switches r_1, r_2, r_3, and r_4. To realize a 1/4 conversion ratio, the second cell is connected between the output port MID_1 of the first cell and the converter ground, 0. This is accomplished through the three reconfiguration switches r_2, r_3, and r_4. The first cell output side (i.e., V_{out}) switches $s2_1$ and $s3_1$ are disabled and replaced by the reconfiguration switches r_2 and r_3, and hence r_2, r_3 are operated through Φ_2 and Φ_1, respectively. As a result, the first cell output charge is routed to the intermediate node V_{int} between the two cells instead of the converter output V_{out}. To cascade both cells, the second cell input port IN_{top_2} is reconfigured to the intermediate node V_{int} between the two cells instead of the converter input voltage V_{in}. The switch $s4_2$ is disabled and the reconfiguration switch r_4 is operated in its place through the same clock phase Φ_2. Similarly, to realize the 3/4 conversion ratio, the first cell charge is routed to the intermediate node V_{int} through the switches r_2 and r_3, and the reconfiguration switch r_1 is operated in place of $s1_2$. With

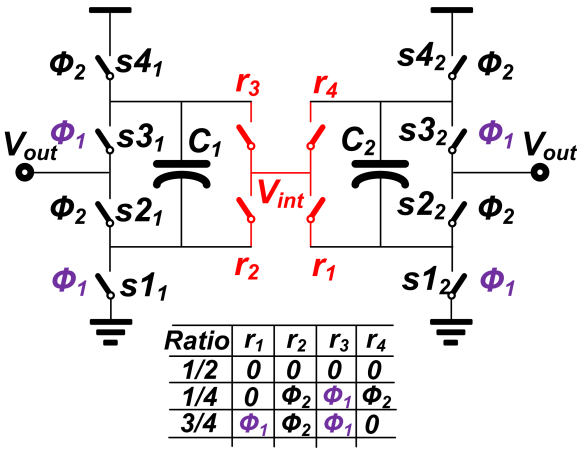


Figure 2.8: Two 2:1 SC cells interconnection through ratio-reconfiguration switches. V_{int} is the inter-cell intermediate node.

such inter-cell connection, no extra series reconfiguration switches are required.

The proposed inter-cell reconfiguration switches are scalable. By replicating the same four connections between each pair of consecutive cells in an N-stage cascade, reconfiguration among the various ratios with a resolution of $m_{odd}/2^N$ can be realized. The conductance of the right half switches, r_1 and r_4, is double the conductance of the left half switches, r_2 and r_3, for optimal binary sizing.

Resolution Reconfiguration Switches

Reconfiguration of the recursion depth (i.e., resolution) can be implemented through the same four ratio-reconfiguration switches; no additional programming switches are required. During resolution reconfiguration, the function of the reconfiguration switch pair r_2 and r_3 in Fig. 2.8 is changed from routing the cell output charge to V_{int}, to instead extracting charge from the intermediate node. Figure 2.9 illustrates the operation of the ratio-reconfiguration switches to reduce the resolution from 3-bit to 2-bit in a RSC. As shown in Fig. 2.9a, the converter connects three 2:1 cells in cascade through the reconfiguration switch blocks $R_{1,2}$ and $R_{2,3}$. The 3-bit converter employs two sub-cells $C3_1$ and $C3_2$ to realize the third cell $C3$ in the cascade, for maximum resource utilization. The reconfiguration switch pairs $(r1_{3_1}, r1_{3_2})$ and $(r4_{3_1}, r4_{3_2})$ are

operated in parallel, to connect the two sub-cells $C3_1$ and $C3_2$ as one cell in series or stack with the second cell $C2$. As shown in Fig. 2.9b, to connect the sub cells $C3_1$ and $C3_2$ in cascade, the inter-cell switches $r1_{3_1}$ and $r4_{3_1}$ are operated in place of the switches $s2_{3_1}$ and $s3_{3_1}$ in order to route the output of cell $C3_1$ to the intermediate node V_{int2}, while the reconfiguration switch $r1_{3_2}$ or $r4_{3_2}$ is operated in place of the switch $s1_{3_2}$ or $s4_{3_2}$, respectively, to realize 3/4 or 1/4 ratios. A similar procedure is followed for the reconfiguration block $R_{1,2}$ to connect the cells $C1$ and $C2$ in cascade. Finally, the second cell $C2$ output-side switches $s2_2$ and $s3_2$ are operated in place of the reconfiguration switches $r2_2$ and $r3_2$, and a 2-bit resolution is realized as shown in Fig 2.9b.

2.4 Circuit Implementation

In order to validate the performance of the proposed RSC topology, a 4-bit RSC converter that realizes 15 ratios is implemented in 0.25μm bulk CMOS process. Importantly, the RSC topology is inherently modular. Thus, design of the converter requires custom implementation of only two SC building blocks.

2.4.1 4-Bit Power Stage Block Diagram

Figure 2.10 shows the recursive block diagram of the implemented 4-bit power stage, consisting of the two basic 2:1 building blocks: boundary and transfer cells. These two building blocks are connected together to implement four reconfigurable stages: $C1$, $C2$, $C3$, and $C4$. The capacitance and conductance of the last two stages, $C3$ and $C4$, are recursively binary-sliced to achieve 100% capacitance utilization and optimal relative sizing across the various ratios at any resolution. The fourth cell, $C4$, consists of three binary-sized sub-cells $C4_1$, $C4_2$, and $C4_3$, while the sub-cell $C4_3$ is further sliced into two sub-cells, $C4_{3_1}$ and $C4_{3_2}$. Similarly, the third cell $C3$ comprises two binary weighted sub-cells, $C3_1$ and $C3_2$. The eight total cells are interconnected at four intermediate nodes, V_{int1}, V_{int2}, V_{int3_1}, and V_{int3_2}, through four reconfiguration blocks, $R_{1,2}$,

$R_{2,3}$, $R_{4_1,4_2}$, and $R_{4_2,4_3}$, along with a half reconfiguration block $R_{3,4}$.

As shown in Fig. 2.10, two reconfiguration-switch blocks $R_{1,2}$, $R_{2,3}$ are employed between the three stages $C1$, $C2$, and $C3$ to realize recursive interconnection across the various resolutions until 3-bit operation. Similarly, another two reconfiguration-switch blocks, $R_{4_1,4_2}$, and $R_{4_2,4_3}$ are used to interconnect the sub-cells of the fourth stage, $C4$, for 3-bit resolution or lower. Instead of using the typical 4-switch reconfiguration block, a 2-switch reconfiguration block $R_{3,4}$ is used to cascade the third and fourth stages, $C3$ and $C4$. The 2-switch reconfiguration block includes only the two switches that deliver charge to an intermediate node, and hence can be considered as a half reconfiguration block. Since the nodes V_{int3_1}, and V_{int3_2} should be separate when cascading the sub-cells $C4_1$, $C4_2$, and $C4_3$ to realize the 3-bit resolution, the reconfiguration block $R_{3,4}$ is further sliced into two sub-blocks, $R_{3,4_1}$ and $R_{3,4_2}$, to enable node isolation as illustrated in Fig. 2.10. The two sub-blocks $R_{3,4_1}$, $R_{3,4_2}$ have relative conductance of, $\frac{1}{3} : \frac{2}{3}$, respectively, to match the relative sizing between the sub-cells $(C4_1, C4_2)$, and $(C4_3)$. Each switch in the implemented five reconfiguration blocks is assigned the optimal binary sizing of the total available conductance G_{tot}, which matches the relative charge that it routes.

2.4.2 Reconfiguration Costs

In the implemented 4-bit converter, boundary cells extract charge from the converter input voltage V_{in}, (e.g., $C1$ and $C4_1$), or deliver charge to the converter output V_{out} (e.g., $C4_{31}$ and $C4_{32}$) across all the ratios. Therefore, these boundary cells only need an extra reconfiguration switch pair to deliver charge to a neighboring cell, or shuttle the charge from a neighboring cell to the converter output V_{out}. On the other hand, transfer cells perform charge displacement from one stage to the next, (e.g., $C2$, $C3_1$, $C3_2$, and $C4_2$). Thus, transfer cells employ four reconfiguration switches to extract the charge from one stage and deliver it to the next. Since, all the switches are binary weighted to match the relative charge shuttled through a cell, the contribution of the extra four reconfiguration switches in a transfer cell to the flying capacitor bottom-plate parasitics

matches the contribution of the original four switches of the 2:1 cell. In a boundary cell, such contribution is divided by two in relation to the original switches contribution.

In total, four cells contribute a normalize added-drain-parasitics of $1/2$, while the remaining cells add 100%. The average normalized added-drain-parasitics from the used reconfiguration switches is less than unity, or approximately 77.6% of the original switches drain parasitics. It should be noted that, in general, the drain parasitics constitute a small percentage of the gate capacitance.

2.4.3 Programmable-Port SC Boundary and Transfer Cells

In Fig. 2.10, each 2:1 SC cell is represented with a single capacitor and four switches. However, in the actual implementation, each cell includes two capacitors and eight switches to implement two out-of-phase 2:1 cells. A port state can be defined for a cell $(IN_{top}, IN_{bottom}, MID)$. A boundary cell operates in one of the four port-states: $(V_{in}, 0, V_{out})$, $(V_{in}, 0, V_{INT})$, $(V_{INT}, 0, V_{out})$, and $(V_{in}, V_{INT}, V_{out})$, where INT represents an inter-cell node. The first state is the typical case where the cell divides the converter input V_{in} by two. In the second state, the cell extracts charge from V_{in} to a neighboring cell. On the other hand, for a boundary cell to deliver charge to the output V_{out} from a neighbor, the cell input or ground ports are routed from the intermediate node, INT, instead of V_{in} or 0, which results in the last two states $(V_{INT}, 0, V_{out})$, and $(V_{in}, V_{INT}, V_{out})$.

Figure 2.11 illustrates the implemented standard boundary cell. Two 180^o phase-shifted 2:1 SC cells are used to guarantee continuous input current through the cell input port, eliminating the need for a bypass capacitance. Since the intermediate node DC level is reconfigured at binary ratios of the input voltage, a transmission gate is used to implement the switches, with the exception of the V_{in} and ground, 0, switches. The switches $M_{n1,2}$, $M_{o2,4}$, $M_{o1,3}$, and $M_{p1,2}$ are the original switches of the 2:1 SC converter which implement the typical port-state $(V_{in}, 0, V_{out})$. A pair of reconfiguration switches can be operated as output-side switches or input-side switches by controlling their driving phases. For instance, by operating the switches M_{i1}, M_{i2}, in Fig.

2.11, from the non-overlapped clock phases Φ_1, Φ_2, respectively, the switches M_{i1}, M_{i2} act as output port switches. On the other hand, by driving M_{i1} from Φ_2, and disabling M_{i2} and M_{p1}, the switch M_{i1} is operated as an input-side switch and hence the cell input port becomes connected to V_{int}. A similar explanation can be followed to connect the cell ground port IN_{bottom} to V_{int} using M_{i2}. Figure 2.12 illustrates the four states of a boundary cell and the implemented cell decoder functional-table.

The transfer cell is designed using the boundary cell as a starting point. At lower-resolution ratios, a transfer cell acts as a boundary cell and hence incorporates the same port-states of the boundary cell. On the other hand, a transfer cell requires two additional states to shuttle charge from one stage to the next. In such cases, the transfer cell input or ground port is connected to the previous cell output port, which is connected to an intermediate node denoted as V_{int} in Fig. 2.11, while the transfer cell output port is connected to the next stage input/ground port intermediate node V_{int2}. Thus, two additional port-states, $(IN_{top}, IN_{bottom}, MID)$, are required for a transfer cell, $(V_{int}, 0, V_{int2})$ and $(V_{in}, V_{int}, V_{int2})$, respectively. Figure 2.12 illustrates the additional two states and the selection signals generated from the transfer cell decoder.

2.4.4 Output Voltage Regulation

Figure 2.13a shows the overall block diagram of the implemented 4-bit RSC converter chip. Two control loops are implemented in the proposed converter: an inner fine-grain loop and an outer coarse-grain loop. The inner loop, working within a single conversion ratio, should modulate either the switching frequency, f_{sw}, or the switched capacitance (i.e., digital capacitance modulation, or DCM [5]) for fine-grain linear output voltage regulation and adaptation under load variations. Frequency modulation is chosen in this work to simplify the implementation complexity, as individual control of split sub-cells is not required in this case. The outer loop, implemented in an all-digital fashion, reconfigures the unloaded conversion ratio to minimize the range over which linear regulation is performed, thereby minimizing efficiency degradation.

Inner Fine-Grain Controller

The T flip-flop employed in Fig. 2.13a guarantees a 50% duty-cycle input clock to the non-overlap phase generator. A Strong-Arm comparator running at f_{comp} is used to provide the clock input to the T flip-flop, as shown in Fig. 2.13a. The comparator sampling clock is produced by an on-chip current-starved oscillator that is set to twice the maximum switching frequency of the power stage; since the power stage switching frequency across all the 15 ratios does not exceed $8MHz$, the current starved oscillator is set to $16MHz$ through an external bias, V_B.

Outer Coarse-Grain Controller

Coarse-grain control in reconfigurable SC converters typically switch between discrete ratios by using a resistor string to generate ratio threshold levels [32, 22]. However, a large number of ratios requires a prohibitively large resistor string, that takes into account R_{out} variation across the different ratios in order to avoid deadlock. In this work, the power stage itself is used to produce the threshold levels. By operating the SC at the maximum f_{sw} and scanning through the available ratios using binary search, the optimal ratio (i.e., the ratio that provides the required output level V_{ref} with minimum resistive voltage drop) can be located. The block diagram of the implemented binary search controller is shown in Fig. 2.14. A 4-bit shift register, that is supplied to the ratio-decoder, is used to hold the current ratio state of the SC power stage as shown in Fig. 2.13a. Once $STROBE$ is asserted, RST is triggered and the power stage is reconfigured into the $1/2$ ratio. Then, EN is asserted, initiating the binary search procedure. As a result, the CLK signal is routed directly from the on-chip oscillator, switching the power stage at $8MHz$ to provide the minimal output resistance, R_{out}.

The proposed ratio-state code, shown in Fig. 2.14, registers consecutive comparison decisions and enables a recursive implementation of the binary controller. Once the counter overflows (OVR is asserted), the 4-bit shift-register stores the present fine-grain controller comparison decision with V_{ref}. If the comparator output, $COMP$, is zero, the present power stage output is

lower than the desired level, V_{ref}, and the SC is reconfigured into a larger binary-ratio at the next resolution configuration, $(1+R_{i-1})/2$, once the comparison decision 0 is registered at the OVR edge. On the other hand, when $COMP$ is 1, the 4-bit register shifts in 1 and the power stage is reconfigured to the lower next-resolution binary-ratio $(R_{i-1})/2$, where $i-1$ is the previous search iteration.

2.5 Experimental Verification

The proposed 4-bit *Recursive* SC converter was fabricated in a 0.25μm bulk CMOS process using 0.9fF/μm^2 MIM capacitors and thin-oxide 2.5V MOS transistors; a die photo is shown in Fig. 2.13b. The RSC occupies $4.645mm^2$ for a total capacitance of $3nF$. A three-ratio $(1/3, 1/2, 2/3)$ series-parallel (SP) SC converter was fabricated using the same technology to enable normalized performance comparison with the prototyped RSC. The implemented three-ratio SP is optimized for the same current density $0.5mA/mm^2$ as the prototyped 4-bit RSC.

Figure 2.15 shows the measured efficiency of the developed RSC and three-ratio SP converters, along with the results of a numerical model developed for the RSC, three-ratio SP, and 7-bit SAR topologies, with models based on the work in [33]. In addition, an ideal LDO is included for comparison. All converters are shown for a 2.5V input voltage V_{in} and a 2mA constant load current, except for the SP which has a 1.86mA load current to ensure equal current density. The efficiency of the RSC is measured for the following 14 ratios (1/8, 3/16, 1/4, 5/16, 3/8, 7/16, 1/2, 9/16, 5/8, 11/16, 3/4, 13/16, 7/8, 15/16) over an output voltage ranging from 0.1V to 2.2V. Interestingly, the efficiency of the RSC at the 9/16 ratio falls below the RSC 1/2 ratio efficiency, since the 9/16 ratio R_{SSL} is 3.5$\times$ larger than the 1/2 ratio. The RSC and SP SC converters both achieve a peak efficiency of 85%, and the numerical models are each within 1% of measurement results across the output voltage range. The large number of ratios afforded by the RSC topology enables a 38% expanded output voltage range (0.1-2.2V in contrast to

0.2-1.6V for the SP), while achieving 6.4% and 3.5% higher efficiency at 0.79V and 1.2V output voltages, respectively, compared to the SP converter. The measured RSC also achieves 17.7% higher efficiency than an ideal LDO at 1.6V. On the other hand, the SP peak efficiencies at the 1/3 and 2/3 ratios (at 0.68V and 1.5V output voltages) exceed the RSC by 5.6% and 5.3%, respectively. The implemented RSC essentially takes the average of the three-ratio efficiency over the 0.52-to-1.6V output range, filling the gaps between the three-ratios (1/3, 1/2, 2/3) and maintaining a flatter efficiency profile. The 4-bit RSC achieves greater than 70% efficiency over the 0.9-to-2.2V output range with an efficiency improvement of 28% over the 7-bit SAR.

Figure 2.16 shows the measured and numerically-modeled efficiency given a 940Ω resistive load for the RSC and 1KΩ load for the SP in order to mimic the operation of a CMOS digital load under DVS conditions. At 0.8V and 1.2V output voltages, the three-ratio SC achieves 59% and 68.7% efficiencies while the 15-ratio RSC achieves 8% and 7.6% higher efficiencies at the same voltages, respectively. The RSC delivers a dynamic voltage operating range from 0.04-to-2.16V, which is 40.4% larger than the 3-ratio SC output range from 0.09-to-1.6V, thereby enabling wider-range DVS operation. The measured operating frequency of the RSC and SP with the external resistive load is shown in Fig. 2.17. The RSC is switched over a 45× dynamic range, from 200KHz-to-9MHz, to realize the 0.04-to-2.16V output voltage range. In contrast, the SP requires a 100× frequency dynamic range, from 100KHz-to-10MHz, to produce V_{out} from 0.09V to 1.6V.

Figure 2.18 shows the measured efficiency of the 1/2 RSC conversion ratio versus the load current at an output voltage of 1.15V . In this case, greater than 80% efficiency is achieved for load currents ranging from 30μA to 1mA. These results illustrate the primary advantage of a frequency modulation control, where the switching frequency, as well as switching parasitics loss, scales with the load current.

The peak-efficiency of the RSC and the three-ratio SP for various power/current densities are essentially identical, since both deliver the same 1/2 ratio. In DVS applications, system

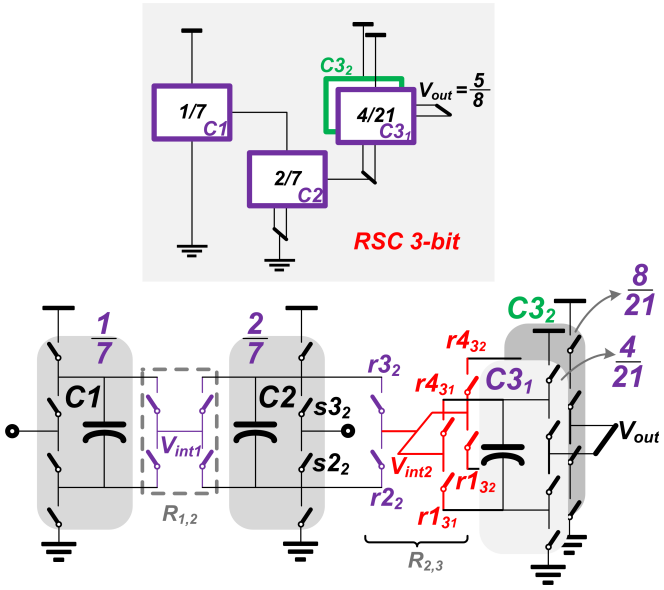
battery-life is a key parameter, and for a digital load of uniform-probability power-states, the system energy efficiency is essentially the weighted average efficiency of the converter over the output voltage range. The weighted-average-efficiency is given by $\int P(V_{out}).V_{out}\eta(V_{out})\,\mathrm{d}V_{out}$, where $P(V_{out})$ is the probability of a given power-state and the integration is over the achievable converter range. Figure 2.19 shows the measured and numerically modeled weighted-average-efficiencies across the output voltage range, plotted versus current density. As shown in Fig. 2.19a, the measured weighted-average-efficiency of the RSC exceeds the SP weighted-average by 6.9% at the same current density of $0.23mA/mm^2$. The modeled efficiency of the RSC maintains higher weighted-average efficiency across different current densities, and approaches a 2.5% higher average than the SP at $16mA/mm^2$. Note that the modeled and measured results diverge after the nominal current density of $0.5mA/mm^2$, as the model assumes optimal total switch width given the increased current density, while the fabricated chips have fixed total conductance.

Since the SP converter can only deliver voltages up to 1.6V, another weighted-average efficiency metric is calculated assuming that an ideal LDO is used to fill any efficiency gap. With an LDO, the the RSC still exceeds the SP measured weighted average by 3.3% at $0.23mA/mm^2$. At $16mA/mm^2$ and above, the LDO performance dominates the RSC and the SP efficiency and both converge to the same value. As shown in Fig. 2.19b, the RSC maintains superior performance than the SP converter at higher power densities until the LDO performance dominates.

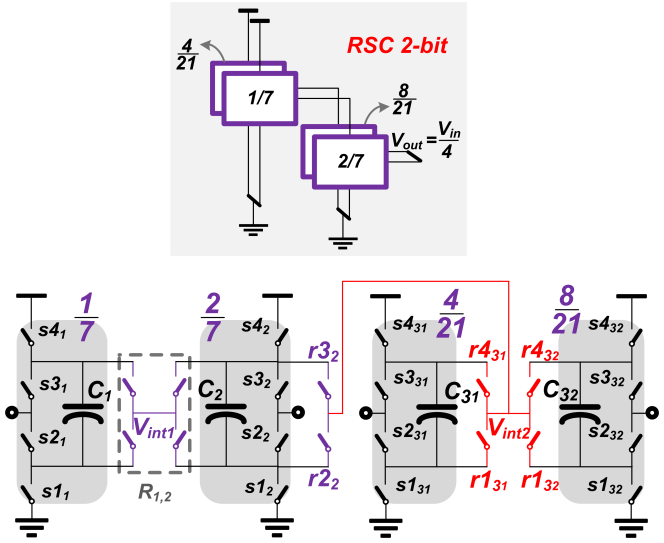
All presented numerically-modeled results employ MIM capacitors with a 1.4% bottom-plate parasitic capacitance ratio. If MOS capacitors were employed in place of MIM capacitors, the 10% bottom-plate parasitics in this technology would degrade the efficiency by 12.5% across the output voltage range for a 3nF of total flying capacitance. On the other hand, if a higher density MIM capacitance were available, for example with a MIM density of $4fF/\mu m^2$ and bottom-plate ratio of $4\times$ lower, the efficiency of both the RSC and SP converters would increase at each discrete ratio. However, due to severe linear regulation away from the nominal three ratios in the SP topology, the efficiency between these ratios only marginally improves. On the other hand,

the RSC converter has explicit ratios between these gaps, and thus the efficiency of the RSC topology at these voltages is increased. For example, with 4fF/μm^2 MIM capacitors, the weighted average efficiency of the RSC exceeds the three-ratio SP by 9% at $0.23mA/mm^2$, or by 6.8% when including an ideal LDO. In this example, the RSC and SP weighted averages converge at $60mA/mm^2$, which is 3.8$\times$ larger than the 0.9fF/μm^2 MIM capacitor case. Migrating to a more modern technology node with higher-density MIM [14, 15], MOS [23, 5, 18], Ferroelectric [22], or deep-trench capacitors [17, 19, 20] and lower parasitic switches will thus enable improved performance of the RSC over the SP topology at larger current densities.

Figure 2.20a shows the control response to a variable stair-case voltage reference, V_{ref}. The control voltage V_{ref} is changed every 500μsec with variable step sizes of 650mV maximum value. Figure 2.20b details the transient coarse controller response when the *strobe* signal is activated while the SC is initially producing a 2V output voltage. Here, the SC power stage phase clock, *clk*, is switched at the maximum frequency while the coarse controller cycles through the various binary ratios until the output reaches the desired level after 8μsec. In the third cycle of this example, the coarse controller reaches the 13/16 ratio, which cannot produce the desired level V_{ref} = 2V, given the converter R_{out}. Thus, a fourth correction cycle automatically results and the $Back-Off$ logic returns the power stage to the correct 7/8 ratio. Finally, the coarse controller hands off the regulation operation to the fine-level frequency controller where *clk* goes back to a normal frequency.



(a) 3-bit RSC



(b) 2-bit RSC

Figure 2.9: Realization of 2-bit resolution from 3-bit resolution RSC using the same ratio-reconfiguration switches.

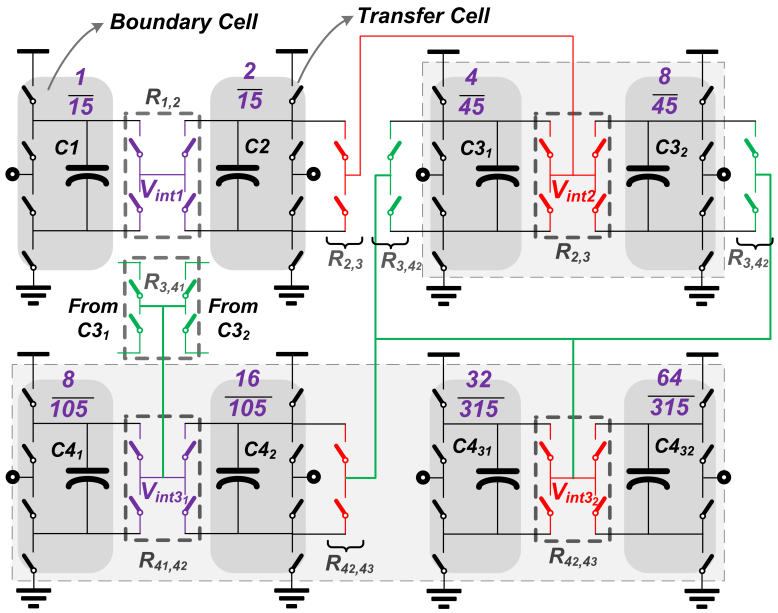


Figure 2.10: Recursive implementation block diagram of the 4-bit RSC converter. The implemented RSC comprises four stages of eight cells *Ci* and five reconfiguration switch blocks $R_{i,i+1}$.

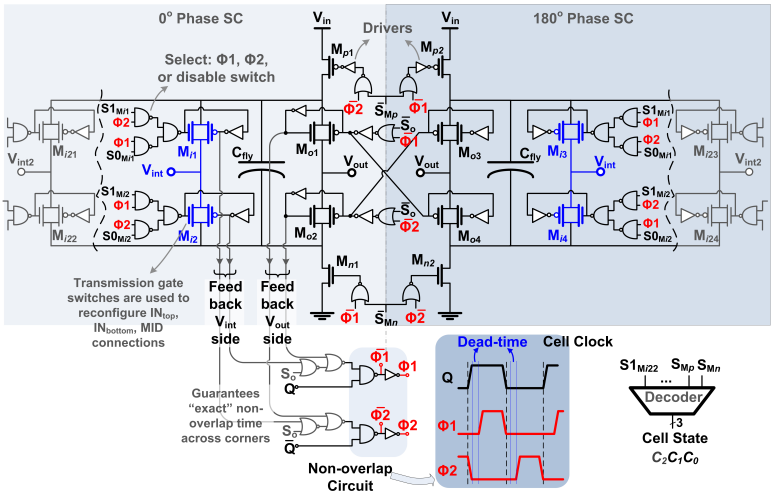
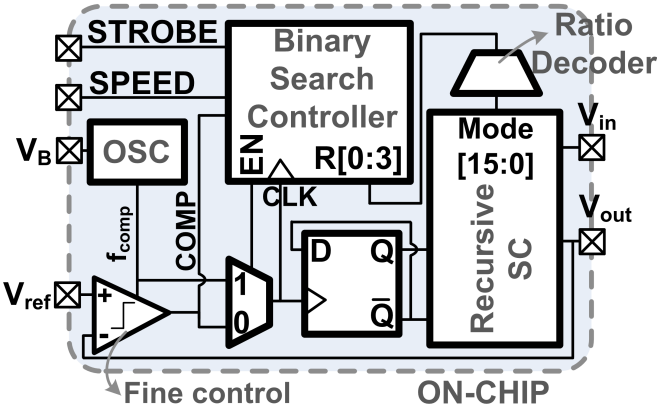


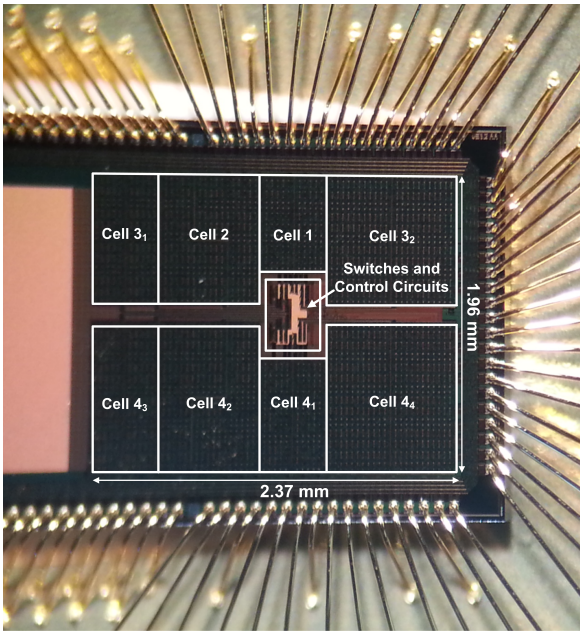
Figure 2.11: Boundary and transfer cells schematic.

	2:1 Cell State			$C_2C_1C_0$	S_o	S_{Mn}	S_{Mp}	M_{i1}		M_{i2}		M_{i21}		M_{i22}	
	IN_{top}	IN_{bottom}	MID					S0	S1	S0	S1	S0	S1	S0	S1
Boundary &Transfer Cell	V_{in}	0	V_{out}	011	1	1	1	0	0	0	0	0	0	0	0
	V_{in}	0	V_{int}	000	0	1	1	1	0	1	0	0	0	0	0
	V_{int}	0	V_{out}	010	1	1	0	0	1	0	0	0	0	0	0
	V_{in}	V_{int}	V_{out}	001	1	0	1	0	0	0	1	0	0	0	0
Transfer Cell	V_{int}	0	V_{int2}	110	0	1	0	0	1	0	0	1	0	1	0
	V_{in}	V_{int}	V_{int2}	101	0	0	1	0	0	0	1	1	0	1	0

Figure 2.12: Boundary and transfer cells decoder truth table.



(a) Block diagram of the overall RSC chip with binary search controller.



(b) 4-bit *Recursive* SC test chip photo.

Figure 2.13: *Recursive* switched-capacitor voltage regulator implementation, comprising eight cells of binary weights and two control loops.

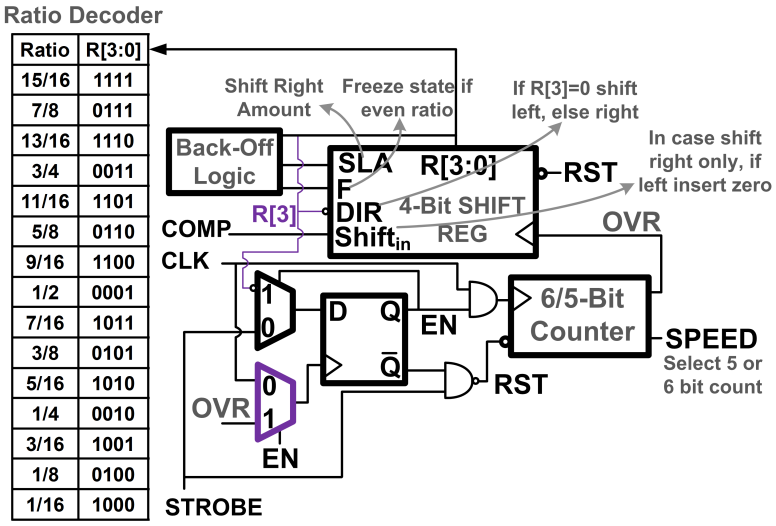


Figure 2.14: Recursive binary search controller block diagram.

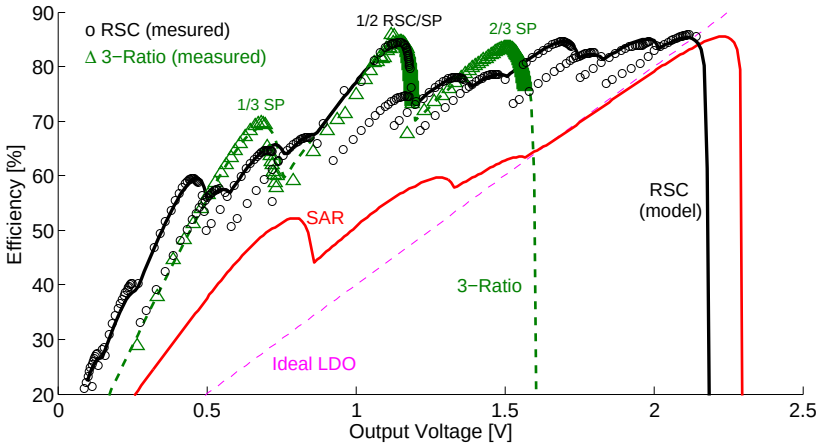


Figure 2.15: Measured and model-predicted efficiency, at 2mA fixed load current, of the fabricated 4-bit RSC versus the output voltage at an input voltage of 2.5V. The measured three-ratio efficiency is at 1.86mA current and the same input voltage.

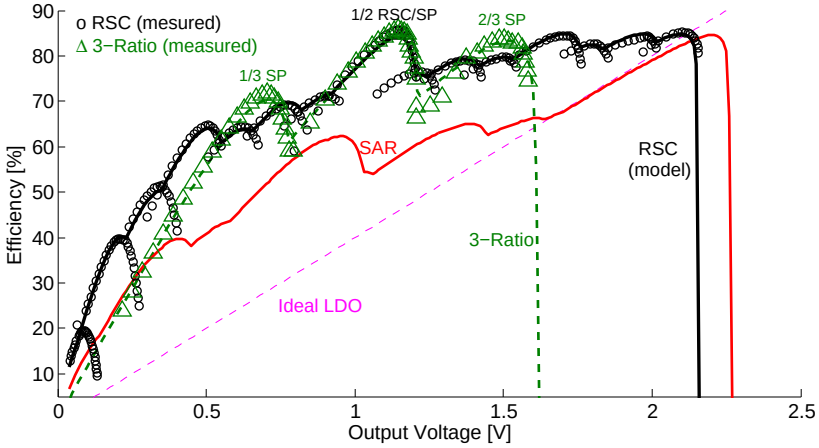


Figure 2.16: Measured and model-predicted efficiency with external resistive load, modeling a digital load under DVS operation, of the three-ratio SP and the 4-bit RSC across the output voltage, at an input voltage of 2.5V.

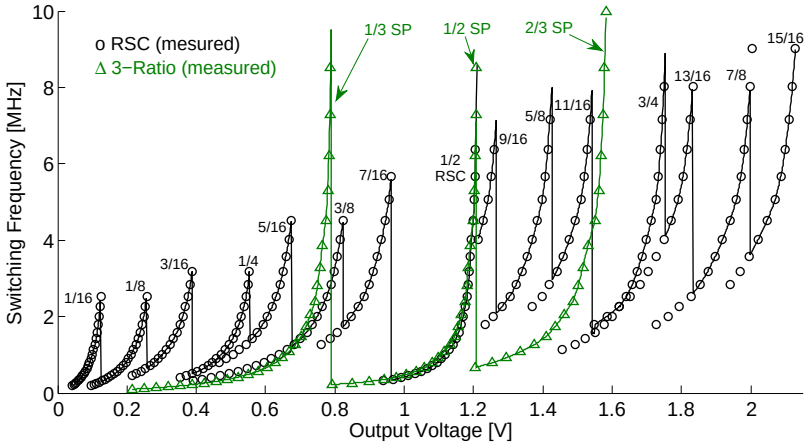


Figure 2.17: Measured RSC and three-ratio SC switching frequency f_{sw} across V_{out}, using the same external resistive load in Fig. 2.16.

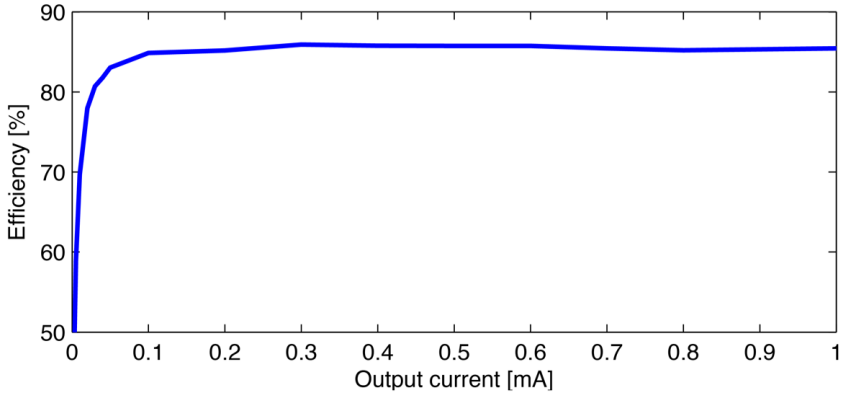
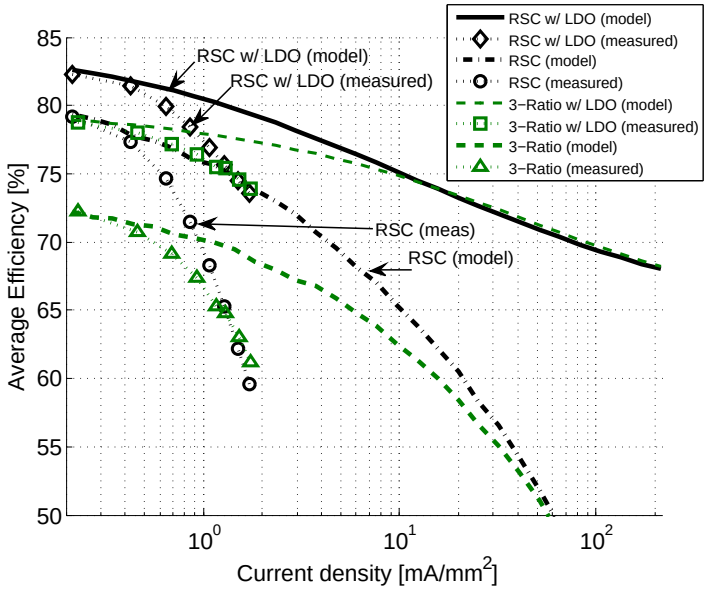
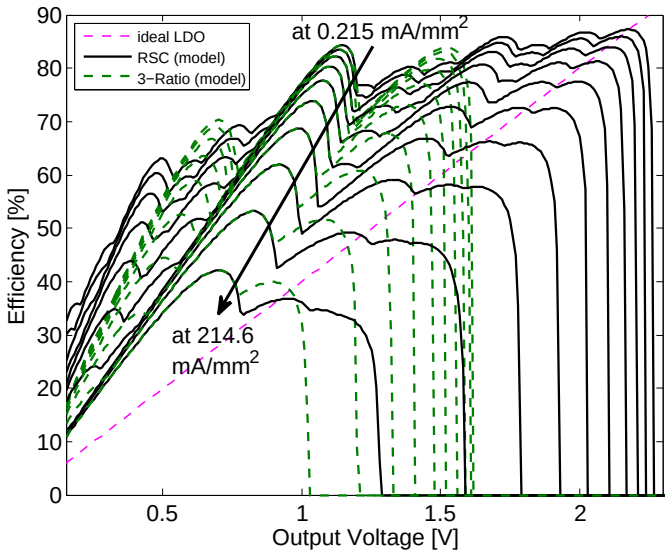


Figure 2.18: Measured RSC efficiency versus the load current at 1/2 ratio, while supplying 1.15V output voltage V_{out}.

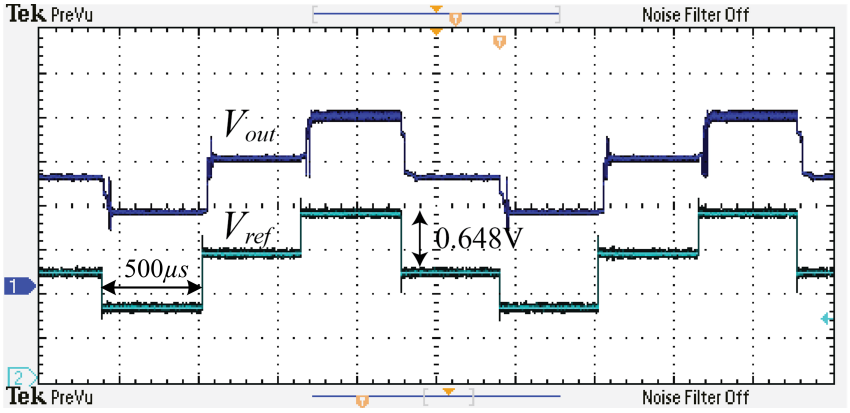


(a) Average-efficiency of RSC and SP versus current density.

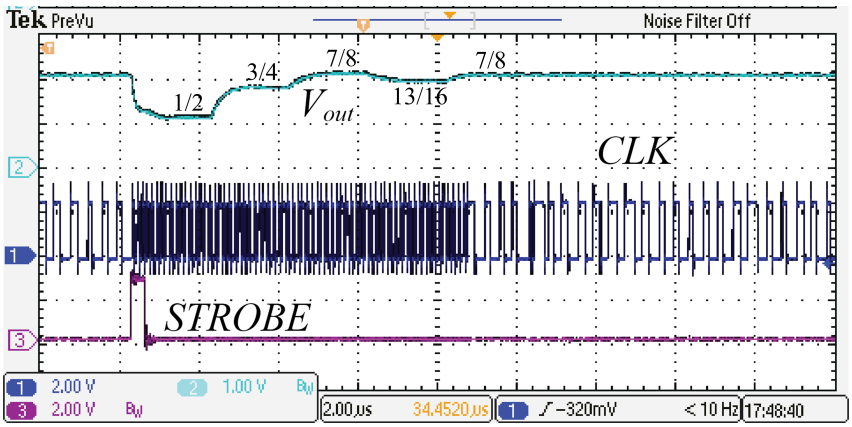


(b) Model-predicted RSC and SP efficiency across V_{out}, versus different current densities.

Figure 2.19: Measured and predicted weighted-average-efficiency versus the load current density, from 0.215-to-215mA/mm^2, for the fabricated RSC and SP in 0.25μm bulk CMOS.



(a) Measured stair control voltage V_{ref} response.



(b) Measured coarse control transient response after *strobe* activation for V_{ref} = 2V

Figure 2.20: Coarse-controller measured transient response to a stair control voltage V_{ref}. Controller transient response when *strobe* is activated while V_{ref} = 2V, showing the detailed ratio binary search operation.

Table 2.1: Comparison with Previously Published Fully-Integrated SC Converters

Work	**[22]**	**[18]**	**[32]**	**3-Ratio SP**	**4-bit RSC**
Technology	130nm	65nm	180nm	0.25μm	0.25μm
Capacitor Type	Ferroelectric	Bulk PMOS	On-chip	MIM	MIM
Chip Area $[mm^2]$	0.366	0.64	1.69	4.33	4.645
Total Capacitance $[nF]$	8	3.88	2.24	2.8	3
Topology	1, 2/3, 1/2, 1/3 step down	1/3, 2/5 SP	7-bit SAR	2/3, 1/2, 1/3 SP	4-bit RSC
V_{in} $[V]$	1.5	$3-4$	$3.4-4.3$	2.5	2.5
V_{out} $[V]$	$0.4-1.1$	1	$0.9-1.5$	$0.2-1.6$	$0.1-2.2$
Quoted Efficiency (η)	93%	74%	72%	85%	85%
Load Current @ (η)	1mA	32mA	10μA	1.86mA	2mA

2.6 Conclusion

A *Recursive* SC converter topology is presented that achieves a flattened efficiency profile over a wide voltage range by employing $2^N - 1$ ratios in an intelligent and modular manner. Compared to a co-fabricated three-ratio series-parallel converter, the proposed 4-bit RSC achieves a wider operating range and achieves a higher weighted average efficiency. To achieve high efficiency with a large number of ratios, the RSC topology maximizes the number of connections to the converter input supply and ground in order to minimize both the charge shuttled through the converter flying capacitors and the cascaded losses. Unlike conventional SC topologies, the RSC SSL loss converges to an upper limit $1/(f_{sw}C_{tot})$ and becomes fixed for arbitrarily high resolutions N. The RSC loss for large resolutions N thus saturates at approximately $2.5\times$ the loss of a 2:1 SC that utilizes the same available C_{tot}. By employing both recursive inter-cell connection and recursive slicing, all possible resolutions, N, and hence their ratios, can be realized without disconnecting a single capacitor and while satisfying optimal relative sizing of the constituent capacitors and switches, thereby ensuring high efficiency even at larger values of N. The inherent regularity and modularity of the RSC topology simplifies the implementation of arbitrarily large resolutions with 2^{N-1} possible ratios, resulting in opportunities to achieve greater than 15 ratios in future work.

2.7 Acknowledgements

This chapter is based on and mostly a reprint of the following publications:

- L.G. Salem and P.P. Mercier, "A recursive switched-capacitor DC-DC converter achieving 2^N-1 ratios with high efficiency over a wide output voltage range," in IEEE Journal of Solid-State Circuits (JSSC), Dec. 2014, vol. 49, no. 12, pp. 2773-2787.
- L.G. Salem and P.P. Mercier, "An 85%-efficiency fully-integrated 15-ratio recursive switched-capacitor DC-DC converter with 0.1-2.2V output voltage range," 2014 IEEE

International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2014, pp. 88-89.

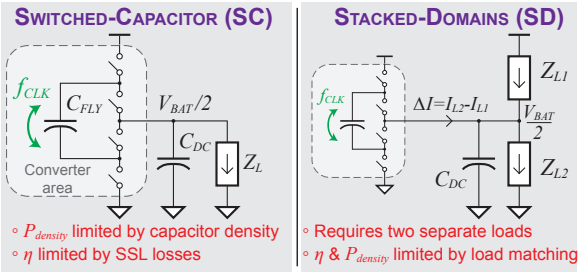
Chapter 3

Flying Domain DC-to-DC Conversion

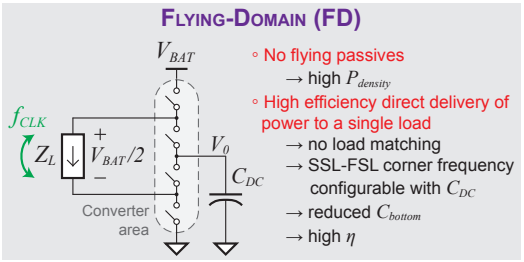
3.1 Introduction

Most modern system-on-chip (SoC) designs utilize multiple power domains to enable per-domain supply scaling commensurate with performance demands. A dedicated DC-DC converter for each power domain is required, which should ideally be integrated on-chip with minimal area overhead (i.e., high power density), feature a conversion ratio of 2:1 or larger to reduce input current and the number of required power pins, and operate efficiently.

Unfortunately, it is conventionally difficult to achieve both high power density and efficiency in standard CMOS, since passive energy storage elements used to process energy, i.e., inductors and capacitors, suffer from low-Q or high bottom-plate parasitics, respectively. For example, switched-capacitor (SC) circuits suffer from fundamental slow-switching limit (SSL) $\frac{1}{2}C\Delta V^2 f$ charge sharing losses that can be reduced by employing large flying capacitors, C_{fly} in Fig. 3.1a, in an attempt to minimize ΔV^2 [21, 27, 34]. Unfortunately, large capacitors not only occupy significant area, limiting power density, but also introduce losses from bottom-plate parasitics, which limits the achievable efficiency (e.g., $<$75% with baseline MOS capacitors) [35, 18]. Exotic capacitor options such as high density MIM [15], ferroelectric [22], or deep-



(a) Conventional integrated power delivery methods.



(b) Proposed flying-domain method.

Figure 3.1: Integrated DC-DC conversion methods.

trench capacitors [20, 36], can yield improved efficiency and/or power density, but still suffer from bottom plate losses and may not be available in all process technologies.

An alternative means to achieve high power density and efficiency is to stack voltage domains on top of one another, as illustrated in Fig. 3.1a [37, 38, 39]. This achieves implicit DC-DC conversion (at a 2:1 ratio in Fig. 3.1a) with minimal area overhead, and ideally 100% efficiency if the two loads are perfectly balanced. However, it is generally difficult to perfectly balance loads in practical applications, and thus any mismatch current must be supplied by a separate auxiliary converter, as illustrated in Fig. 3.1a, which ultimately reduces power density and efficiency to that of the auxiliary converter when only one domain is on.

To overcome the efficiency-power density trade-off in conventional DC-DC converters, this chapter presents a new class of switching converters called flying-domain (FD) power converters that do not rely on high quality passive energy storage elements to achieve high efficiency. Since C_{fly} in an SC converter is typically sized to be $>10\times$ larger than the effective capacitance of the digital load, C_L, as will be shown later in this chapter, the flying domain

concept, shown in Fig. 3.1b, replaces the flying capacitor with the load itself. This serves to: 1) significantly decrease the converter area by removing C_{fly} altogether, thereby increasing power density, and 2) scale the bottom-plate losses by $\sim C_L/C_{fly}$ (i.e., $>10\times$), thereby improving efficiency. Furthermore, the output decoupling capacitance, C_{DC}, which is nominally used to minimize ripple in SC converters, can remain tied to the DC output node of the FD converter, V_0, and can be implemented with high-density on- or off-chip capacitors without regard to bottom plate parasitics. Unlike conventional SC converters where C_{fly} defines the SSL corner frequency and hence the switching frequency that attains minimum loss, the SSL corner frequency in FD converters is defined by the larger (and more inexpensive) decoupling capacitor, C_{DC}, which sets the voltage ripple across the load yet does not switch or incur bottom-plate losses, thereby lowering the SSL corner frequency and significantly reducing charge sharing losses that plague conventional SC converters. On the other hand, it will be shown that allowing ripple in digital circuits does not adversely affect the overall system-level power consumption (when considering the implicit DC-DC converter losses), and thus C_{DC} can be alternately reduced in order to further increase power density.

This chapter presents the modeling and theory of FD conversion, and reports measurement results from prototype FD converters. Section 3.2 introduces the employed techniques to realize high-density and high-efficiency switching topology. Section 3.3 then uses graph theory to prove that the 2:1 FD concept is well-posed, and with the help of a frequency-scaled switching scheme, can enable 4:1 conversion with a valid steady-state. Section 3.4 describes details of circuits used to implement a reconfigurable 2:1 and 4:1 FD converter prototype in 0.18 μm SOI, and Section 3.5 presents measurement results. Finally, Section 3.6 concludes the chapter.

3.2 Achieving High Power Density and Efficiency via the Flying-Domain Technique

This section introduces models and analysis that show that flying the load instead of a capacitor can be advantageous in modern digital systems. To show this, it is first demonstrated that allowing ripple on digital loads does not adversely affect system-level power consumption, thereby enabling higher converter power density through reduction of decoupling capacitance. Then, an analytical model is derived to show that the flying capacitance in an SC converter is normally set to be much larger than the effective capacitance of the load itself, and thus flying the load instead of the capacitor yields reduced bottom-plate losses and overall improved conversion efficiency and power density. Furthermore, it is shown that adding decoupling can yield even further improved conversion efficiency by reducing the SSL corner frequency without a corresponding increase in bottom-plate parasitics.

3.2.1 Supply Ripple Allowance and Overall Circuit Efficiency

Switched DC-DC converters have inherent periodic output voltage variation (i.e., ripple) resulting from the switching of the constituent energy-storage elements while shuttling the charge to the output load. Typically, the clock of synchronous digital circuits, $f_{clk} = 1/T_{clk}$, operates faster than the switching frequency of the DC-DC converter, $f_{SW} = 1/T_{SW}$, as illustrated in Fig. 3.2. The maximum possible clock frequency of a digital load depends on supply voltage, for example in sub-micron CMOS with the following relationship: $f_{clk} \propto (v_{dd}(t) - V_{th})^{\alpha}/v_{dd}(t)$ [40, 41]. Since the clock of a digital load is typically not dynamically changed within the period of a DC-DC converter cycle, the maximum clock frequency as determined by the critical path delay is set by the minimum supply voltage within any T_{SW} (V_{DD} in Fig. 3.2). As a result, any periodic supply ripple $v_{dd}(t)$ above the minimum voltage, V_{DD}, nominally results in additional power consumption in the load without a return on performance (unless the clock frequency is

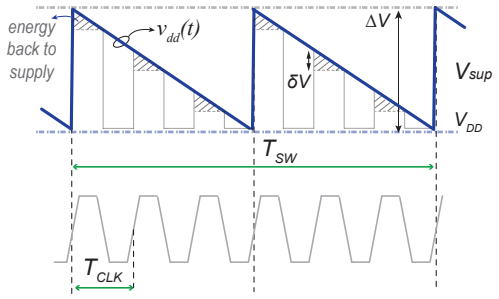


Figure 3.2: Illustration showing excess power consumption from a digital load powered by a rippled-supply.

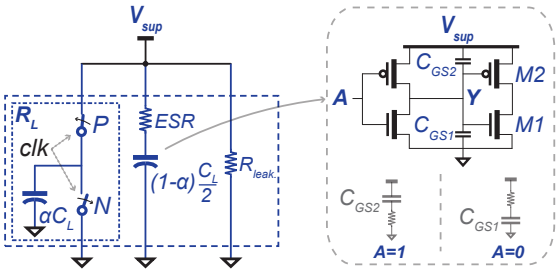


Figure 3.3: Equivalent model of a synchronous digital circuit. The origin of symbiotic capacitance is shown in the inset.

dynamically adapted to the ripple) [13, 41].

In order to evaluate the power loss caused by such periodic supply variation, a simple model of a CMOS digital circuit is employed as shown in Fig. 3.3. Here, a digital load with activity factor α is represented by a switched-capacitor resistor αC_L, an intrinsic decoupling capacitor $(1-\alpha)C_L/2$, and an equivalent leakage resistance $R_{leak.}$. At high performance levels, leakage and short-circuit currents can be neglected [40, 42, 43]. An intrinsic (or symbiotic) decoupling capacitance [44, 45] is employed in the model as illustrated in the inset in Fig. 3.3, which originates from idle gates in the vicinity of switching gates.

At maximum power, $\alpha \approx 1$, the digital load switches $2 \times N$ clock cycles within the SC DC-DC switching period. The rippled supply waveform is thus sampled on the effective load capacitance C_L at a $2 \times N$ sampling rate and the total power consumption of the logic from the rippled supply can be calculated by a backward-Euler discrete integration as illustrated in Fig.

3.2 and computed as:

$$P_L = 2f_{SW}C_L\sum_{i=1}^{N}(V_{DD}+\Delta V-\frac{2\Delta V}{T_{SW}}((i-1)T_{clk}+T_{clk}/2))^2 \tag{3.1}$$

where ΔV is the peak-to-peak supply ripple. A backward-Euler summation is used since the decreasing supply ramp time $T_{SW}/2$ is much larger than the RC time constant of the nodes within the digital circuit, and hence the loss in the logic transistors' resistance $RC/(T_{SW}/2)C\delta V^2$ is negligible, and the extra energy drawn from the supply, i.e. the bounded energy triangles in Fig. 3.2, is adiabatically returned to the supply. It can be shown that the total power consumption of a digital circuit in Eqn. (3.1) under a rippled-supply can be simplified to:

$$P_L = C_L V_{DD}^2 f_{clk} + 1/2 C_L V_{DD}\Delta V f_{clk}. \tag{3.2}$$

The first term in Eqn. (3.2) is the conventional power consumption of the digital load operating from a ripple-free supply of V_{DD}. The second term represents the extra AC power loss due to the rippled supply without any gain on circuit performance. This is since although higher supply voltage enables operation at faster clock, the valley of the supply ripple defines the circuit critical path delay and hence the maximum functioning clock speed. Therefore, from the point of view of the digital load circuit, ripple generates excess waste and should be eliminated through inclusion of a large output decoupling capacitance or a complex multi-phase DC-DC converter design.

However, this is only true when considering the load in isolation from the DC-DC converter. In order to evaluate the ripple effect on the DC-DC converter efficiency, consider the case of a 2:1 SC DC-DC converter, illustrated in Fig. 3.4a. First, consider the case where no explicit decoupling, C_D, or intrinsic decoupling, $(1-\alpha)C_L/2$, capacitance exists. As shown in Fig. 3.4b (left), during Φ_1 the odd-numbered switches are turned on, connecting C_{fly} between the input voltage, V_{IN}, and the output voltage, V_{OUT}, while the equivalent load resistance, R_L, charges C_{fly} until V_{OUT} reaches $V_{IN}/2-\Delta V/2$, as illustrated in Fig. 3.4c. On the other clock

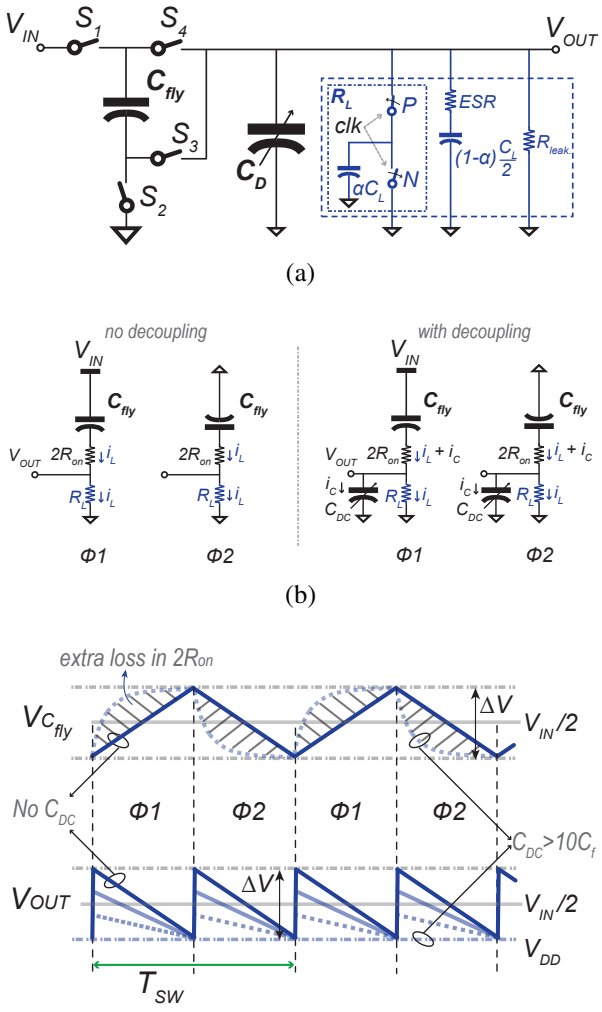


Figure 3.4: A sample 2-to-1 SC DC-DC converter. (a) Circuit topology. (b) Phase 1 and phase 2 of the voltage divider. (c) Voltage across C_{fly} and the output voltage waveforms.

phase Φ_2, the even-numbered switches are turned on, connecting C_{fly} in parallel to the output load R_L, while the charge stored on C_{fly} in the prior phase is released to the output load. In both cases, all the current that passes through the switches' on-resistance, $2\times R_{on}$, passes in the load R_L, and hence the ratio between the SC loss to the output power is $2R_{on}/R_L$, or essentially R_{FSL}/R_L, where R_{FSL} is the fast-switching limit (FSL) resistance of the 2:1 SC [21].

Now, consider the case when a decoupling capacitance (C_{DC}), comprising symbiotic capacitance, an explicit decoupling capacitance (C_D), or both, is employed, as illustrated in Fig.

3.4b (right). The presence of decoupling results in extra current through the converter switches ($2\times R_{on}$) that is not delivered to the load, R_L, and is instead sunk to ground. Interestingly, this extra loss due to the decoupling matches the reduction in the digital load *AC* power consumption due to the reduced supply ripple, resulting in a zero-sum-game from a system-level perspective. For example, as C_{DC} is further increased, the output voltage ripple decreases and more *AC* ripple power is drained to the ground and lost as heat through the converter switches instead of being dissipated in the load. When $C_{DC} > 10 \times C_{fly}$, V_{OUT} reaches a nearly fixed DC value, V_{DD}, with nearly zero-ripple, and hence the losses in the SC converter saturates to an upper bound that exactly matches the SSL loss value:

$$P_{SSL} = C_f \Delta V^2 f_{SW}, \tag{3.3}$$

while the *AC* power loss in the load vanishes. From charge conservation, the charge delivered to the output load during a complete converter switching period, $2N \times C_L V_{DD}$, matches the total charge delivered by the SC flying capacitor, $2 \times C_f \Delta V$, in Φ_1 and Φ_2. Therefore, Eqn. (3.3) can be rewritten as:

$$P_{SSL} = N \times C_L V_{DD} \Delta V f_{SW}, \tag{3.4}$$

which is identical to the *AC* loss consumed by the digital load in the zero decoupling capacitance case as expressed by the second term in (3.2). Therefore, when the performance of digital circuits are dictated by the minimum supply voltage, so long as the ripple does not exceed device voltage ratings, there is no benefit to the overall system power consumption in reducing the ripple. In fact, reducing the ripple through inclusion of a larger decoupling capacitor or multiphase interleaving serves only to increase the area or overhead power of the resulting SC converter.

3.2.2 Switching a Capacitor versus Switching the Load

The previous subsection showed that while ripple introduces additional power consumption in a digital load, elimination of ripple through inclusion of a large decoupling capacitor just shifts these losses into SSL losses of an SC converter, resulting in a zero-sum-game at the system level. In order to improve system-level power consumption, the SC converter should be operated in the FSL regime (i.e., at a higher switching frequency), which naturally decreases ripple, thereby decreasing digital load power without a corresponding increase in fundamental SC converter losses. The FSL defines the lower bound of the SC equivalent output resistance R_{out} as approximated by the Euclidean norm of the two limits $R_{out}(f_{sw}) = \sqrt{R_{SSL}^2 + R_{FSL}^2}$. In other words, the lowest possible intrinsic loss in a SC converter is limited by the ESR facing the converter charge flow. Unfortunately, increasing the switching frequency results in practical loss components resulting from power switches gate drive and drain parasitics, and top and bottom-plate flying capacitor parasitics. The total loss components in a 2:1 SC are given by:

$$\begin{aligned} P_{loss} &= I_L^2 \sqrt{R_{SSL}^2 + R_{FSL}^2} + P_{gate} + P_{Bot-cap} \\ &= I_L^2 \sqrt{\left(\frac{1}{4C_{fly}f_{sw}}\right)^2 + \left(\frac{2R_{on}}{W_{sw}}\right)^2} \\ &\quad + 4C_g W_{sw} V_{DD}^2 f_{sw} + \beta C_{fly} V_{DD}^2 f_{sw}, \end{aligned} \tag{3.5}$$

where R_{on} and C_g are a unit-width switch resistance (in Ω.m) and gate capacitance (in F/m), respectively, W_{sw} is the width of a single switch in the 2:1 power stage, and β is the ratio of bottom-plate-to-flying capacitance (e.g., ∼10% for MOS capacitors)[1]. It can be shown that the optimal switch width W_{sw}^* and switching period T_{sw}^* are given by:

$$W_{sw}^* = 2\sqrt[3]{\frac{2R_{on}^2 C_{fly}}{R_L^2 C_g}} \tag{3.6}$$

[1]Power switches' drain parasitics are included as part of $P_{Bot-cap}$.

$$T^*_{sw} = 2R_L C_{fly}\sqrt{\beta + \sqrt{2}\frac{C_g W^*_{sw}}{C_{fly}}}. \tag{3.7}$$

With these values, the minimum normalized total loss becomes:

$$\frac{P^*_{loss}}{P_L} = \sqrt{\beta + 2\sqrt{2}\sqrt[3]{\frac{2R^2_{on}C^2_g}{R^2_L C^2_{fly}}}}, \tag{3.8}$$

which matches with $<1\%$ error to a numerical model that has been shown to match measurement results to $<1\%$ [34]. Given this normalized loss, the achievable efficiency of an SC converter is $\eta = (1 + P^*_{loss}/P_L)^{-1}$.

In order to establish a relation between the required C_{fly} for a given target efficiency, Eqn. (3.8) can be manipulated to calculate the normalized flying capacitance for a given minimum normalized loss as:

$$\frac{C_{fly}}{C_L} = 4\tau f_{clk}\sqrt{\frac{2\sqrt{2}}{\left(\left(\frac{P^*_{loss}}{P_L}\right)^2 - \beta\right)^3}}, \tag{3.9}$$

where $\tau = R_{on}C_g$ can be though of as the intrinsic delay of a MOSFET. From (3.9), the minimum possible converter loss is set by the capacitance technology β (bottom-plate ratio), where $\min\left(P^*_{loss}/P_L\right) > \sqrt{\beta}$, which agrees with intuitive analysis in prior work [33, 13].

From (3.9) and values from the ITRS predictive PIDS tables [46, 47], a flying capacitor that is at least $10\times$ larger than the digital load capacitance is necessary to achieve $>75\%$ efficiency, and thus interchanging C_{fly} and C_L by switching the load itself instead of the flying capacitor results in 87.7% achievable efficiency, i.e., a 12.7% efficiency improvement when using C_{fly} as a DC capacitor. This exceeds the maximum efficiency expected from typical MIM capacitors, which have less bottom plate losses, though typically through much lower capacitive (and thus power) density.

To arrive at this efficiency improvement number, it can be shown that the equations presented in this section are applicable to FD converters, but with the decoupling capacitor C_{DC}

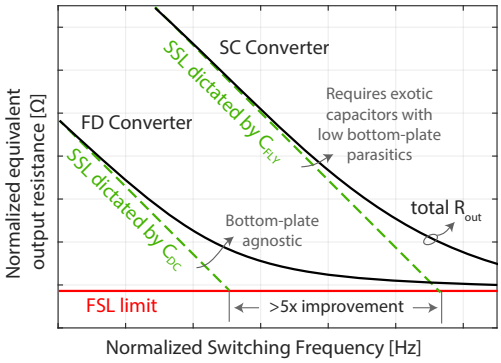


Figure 3.5: SSL-FSL corner frequencies for SC and FD circuits.

replacing C_{fly}, and β describing the ratio of bottom-plate parasitics of the load to the capacitance of the load itself. This critical distinction from SC circuits enables FD converters to have lower bottom-plate losses (when $C_{fly} >> C_L$) as observed from (3.8) with C_{fly} replaced with C_{DC}. In other words, a large and high-density C_{DC} can be employed, which sets the fundamentally achievable efficiency of the circuit, but without regard for its bottom plate parasitics (since it is not switched). Essentially, while SC converters avoid the challenge of low-Q CMOS inductors, FD converters eliminate the need for high-Q (i.e., with low bottom-plate parasitics) capacitors.

Importantly, C_{DC} also replaces C_{fly} in SSL equations, and thus in FD converters the SSL-FSL corner frequency, $1/(4R_{FSL}C_{fly})$, is set not by C_{fly}, as in SC circuits, but instead by C_{DC}. This implies that a large C_{DC}, which does not switch, can be employed to set a very low SSL corner frequency. If the converter runs at the same frequency as before (in its prior SC incarnation), SSL losses, which limit the efficiency of conventional SC converters operating at practical frequencies, can be essentially eliminated, all while reducing bottom-plate losses, for a net increase in DC-DC conversion efficiency in the FD technique. Figure 3.5 illustrates the difference in SSL corner frequencies for SC and FD circuits for the conventional case of a 2:1 SC converter employing $C_{DC} = 5 \times C_{fly}$, giving a $5\times$ improvement which results in an FD conversion efficiency of 91% given the same ITRS MOS capacitor example cited above. Furthermore, switching the load and placing the capacitor in a static state enables lower-complexity packaging solution when considering discrete SC implementations. For instance, switching large external

capacitors for 2:1 output ratio, like in [48], requires two I/O pads per flying-capacitor per load, while switching multiple loads (analogous to multi-phase interleaving, though in this case with multiple loads instead of multiple flying capacitors) around a single external decoupling cap costs only a single I/O pad.

In a bulk process, the same advantages of an FD converter can be realized, given the large bottom-plate parasitics of MOS capacitors in such technologies. The load can be placed in a separate deep-nwell and by leaving its bias floating, the deep-nwell bottom-plate parasitics can be reduced by $\sim 2\times$, as demonstrated in a recent FD power amplifier [49].

3.3 State-Space Modeling of Flying-Domain DC-DC Converters

In this section, a network-theory based analysis is followed to find the fundamental loop and cut-set matrices of an FD converter. The analysis presented in this section is based on the theory illustrated in [50, 31, 33]. A switched network can be abstracted through formulating a directed graph (digraph) to represent the topology of the switched circuit while discarding the properties of individual circuit elements, i.e. capacitors and switches. This abstract view will be utilized to derive the component voltages and charge multipliers of an FD converter, and show that the 2:1 FD topology is a properly-posed switched network with a valid stead-state output. By introducing a frequency-scaled switching technique, it will then be shown that 2^N:1 conversion ratios are possible.

3.3.1 Modeling a 2-to-1 Flying-Domain Converter

A 2:1 FD converter is shown in Fig. 3.6a, and operates by flying the voltage domain of the load itself, FD_1. The two phases of the circuit, when the odd and even numbered switches are

enabled respectively, are shown in Fig. 3.6b. To establish the digraph of the 2:1 FD converter, each component is represented by a directed branch, where the direction of each branch indicates the polarity of the component voltage or current (charge). For each phase in the circuit, a tree, T_1 and T_2, can be constructed from selected branches of each digraph, respectively. A branch in a digraph is categorized as a twig if it is contained in a tree T and a link otherwise. For each link, corresponding to a selected tree, a unique closed path, i.e. fundamental loop, can be formed by the set of twigs connecting the two endpoints of that link. For each phase, a fundamental loop matrix B^i can be established from the linearly-independent KVL equations associated with all tree links:

$$\begin{bmatrix} 1 & 1 & -1 \end{bmatrix} \begin{bmatrix} v_{FD1}^1 \\ V_O^1 \\ V_{IN} \end{bmatrix} = 0 \text{ and } \begin{bmatrix} -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{FD1}^2 \\ V_O^2 \\ V_{IN} \end{bmatrix} = 0. \tag{3.10}$$

Under no-load condition, the FD converter delivers zero current and therefore each component maintains a fixed voltage across the two phases in steady-state. In such a case, the fundamental loop matrices of each phase hold simultaneously and can be combined as:

$$\begin{bmatrix} 1 & 1 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{FD1} \\ V_O \\ V_{IN} \end{bmatrix} = 0. \tag{3.11}$$

By inspection, the rank of B in (3.11) is two. Thus, the matrix B has one degree of freedom, and the components voltages in an unloaded 2:1 FD converter can be expressed in terms of the input voltage V_{IN} by manipulating (3.11) as follows:

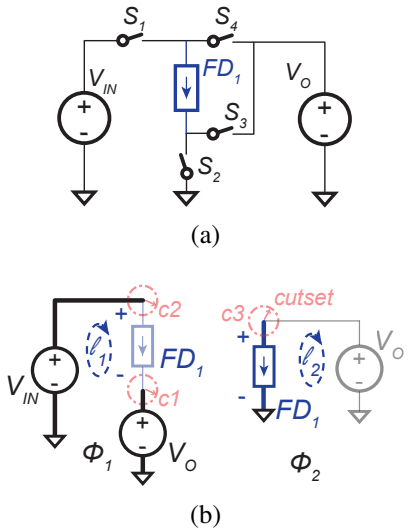


Figure 3.6: A 2-to-1 FD DC-DC converter. (a) Circuit topology. (b) Phase 1 and phase 2 of the voltage divider, twigs shown with dark lines.

$$\begin{bmatrix} B_c & b_{in} \end{bmatrix} \begin{bmatrix} v_{FD1} \\ V_O \\ V_{IN} \end{bmatrix} = 0 \text{ , thus } \begin{bmatrix} v_{FD1} \\ V_O \end{bmatrix} = \begin{bmatrix} 1/2 \\ 1/2 \end{bmatrix} V_{IN} \tag{3.12}$$

, and hence a 2:1 ratio is realized.

When a load current is drawn from the FD converter, the domain v_{FD1} and DC capacitor V_O voltages charge and discharge during each phase. In order to find the charge multipliers of each component, the fundamental cut-sets of each phase digraph (Fig. 3.6b) is examined to produce a system of KCL equations:

$$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} q^1_O \\ q^1_{FD1} \\ q^1_{IN} \end{bmatrix} = 0 \text{ and } \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} q^2_O \\ q^2_{FD1} \\ q^2_{IN} \end{bmatrix} = 0 \tag{3.13}$$

where q^i is the charge flow in a component in phase i. In order to produce a combined system of KCL equations for both phases, it can be noted that for the output decap $q^1 = -q^2$ must be true at

steady state. In addition, the total charge delivered to the load q_{FD1} during the entire clock period as well as the differential charge Δq_{FD1} relate to the charge delivered in each phase through the relation:

$$\begin{bmatrix} \Delta q_{FD1} \\ q_{FD1} \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} q^1_{FD1} \\ q^2_{FD1} \end{bmatrix} \tag{3.14}$$

By taking the inverse of (3.14), the FD_1 charge flow during each phase in (3.13) can be replaced by the total q_{FD1} and differential charge Δq_{FD1}, and hence the combined cut-set matrix becomes:

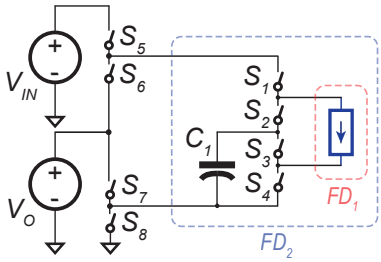
$$\begin{bmatrix} 1 & 1/2 & -1/2 & 0 & 0 \\ 0 & -1/2 & 1/2 & 1 & 0 \\ -1 & 1/2 & 1/2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} q_O \\ \Delta q_{FD1} \\ q_{FD1} \\ q^1_{IN} \\ q^2_{IN} \end{bmatrix} = 0 \text{ and } \begin{bmatrix} q_O \\ \Delta q_{FD1} \\ q^1_{IN} \\ q^2_{IN} \end{bmatrix} = \begin{bmatrix} 1/2 \\ 0 \\ -1/2 \\ 0 \end{bmatrix} q_{FD1}. \tag{3.15}$$

The rank of the combined cut-set matrix Q is four. The extra degree of freedom here is exploited to express the charge flow in each component in terms of the output charge q_{FD1} flow as shown above.

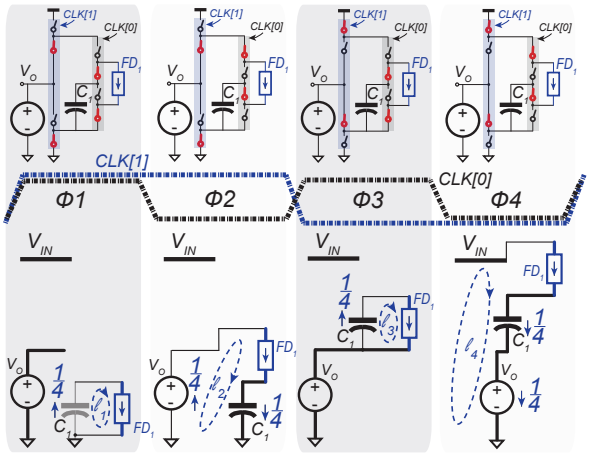
Note that both fundamental loop and cut-set matrices of the 2:1 FD converter are square and invertible, proving a properly-posed switched topology with a unique solution. Hence, the illustrated 2:1 FD converter is a valid topology that can reach a stable steady-state.

3.3.2 Modeling a 4-to-1 Flying-Domain Converter

To implement a 4:1 FD ratio, the input terminals of a base 2:1 cell, FD_1, is switched through the switches of a second flying domain converter, FD_2, as shown in Fig. 3.7a. However, operating all converter switches from a two-phase clock (which would nominally be Φ_1 and Φ_4 in Fig. 3.7b) results in a non-square fundamental loop matrix, and hence a two-phase 4:1 FD



(a)



(b)

Figure 3.7: A 4-to-1 FD DC-DC converter. (a) Circuit topology. (b) The resulted four switching phases of a properly-posed 4:1 FD converter, twigs shown with dark lines. V_{IN} is a twig in the first three phases only Φ_1, Φ_2, and Φ_3.

converter is not properly posed, as demonstrated by the 2×4 combined loop matrix:

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{FD1} \\ v_{c1} \\ V_O \\ V_{IN} \end{bmatrix} = 0. \tag{3.16}$$

Fortunately, it is possible to create a valid topology by employing additional states. This can be accomplished in a a simple and low-complexity manner by operating FD_2 at half the frequency of FD_1, as shown in Fig. 3.7b, based on prior work [51, 52]. The combined four-phase fundamental

loop matrix of the proposed multi-phase 4:1 FD converter is given by:

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 1 & -1 & 0 \\ 1 & -1 & 0 & 0 \\ 1 & 1 & 1 & -1 \end{bmatrix} \begin{bmatrix} v_{FD1} \\ v_{c1} \\ V_O \\ V_{IN} \end{bmatrix} = 0. \tag{3.17}$$

By inspection, the matrix in (3.17) has a redundant row, i.e. the first and third rows are identical. Therefore, the rank of the matrix in (3.17) is three, and hence the matrix B_c is square and invertible. This means that a 4:1 FD converter only requires three switching phases to have a unique solution and produce a properly-posed converter. However, the four-phase operation is motivated by the simpler switch driving circuitry and clock organization. In the four-phase case, in Fig. 3.7b, the component voltages in terms of the input voltage can be found from 3.17 as:

$$\begin{bmatrix} v_{FD1} & v_{c1} & V_O \end{bmatrix}^T = \begin{bmatrix} 1/4 & 1/4 & 1/2 \end{bmatrix}^T V_{IN} \tag{3.18}$$

Thus, the proposed FD converter provides a $1/4$ input-to-output conversion ratio.

Similarly, component charge flow can be found through the fundamental cut-set matrix. From symmetry, it can be noted that the 4:1 FD converter boils down to a first-stage 2:1 FD converter that is connected once in parallel to V_O, during Φ_1 and Φ_2, and then to $V_{IN} - V_O$, during Φ_3 and Φ_4, with half of the total charge delivered to the load, FD_1, in each case. Therefore, q_{C1} and q_O are balanced over the clock period of the first flying-domain, $CLK[0]$, i.e., $q^1_{C1} = -q^2_{C1}$ and $q^3_{C1} = -q^4_{C1}$, and similarly for q_O. Each component charge flow can be found as:

$$\begin{bmatrix} q_{C1} & q_O & \Delta q_{FD1} & q^1_{IN} & q^2_{IN} & q^3_{IN} & q^4_{IN} \end{bmatrix}^T = \begin{bmatrix} -1/4 & 1/4 & 0 & 0 & 0 & 0 & -1/4 \end{bmatrix}^T q_{FD1}. \tag{3.19}$$

Similarly, other binary ratios $2^N : 1$ can be realized by recursively flying the input terminals of a

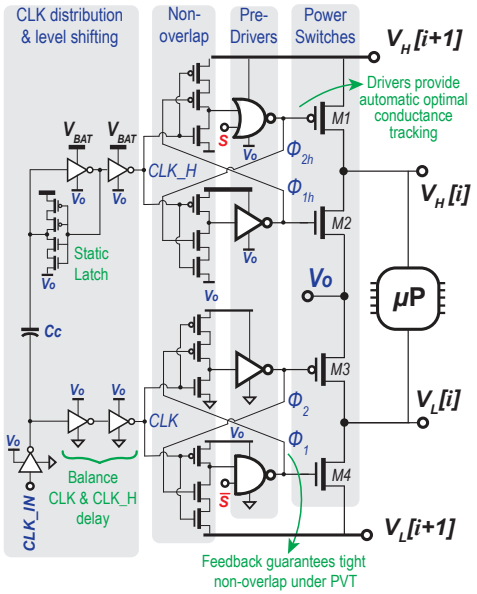


Figure 3.8: Schematic of the unit 2:1 FD power stage cell.

cell $FD[i]$ through the switches of a subsequent flying cell $FD[i+1]$, while operating the recursive N array at binary decaying frequencies $f_0/2^i$, where f_0 is the first cell switching frequency.

3.4 Circuit Implementation

This section discusses circuit implementation details of the reconfigurable FD power stage, the hysteretic control scheme, and flying level shifters [53].

3.4.1 Reconfigurable Power Stage Design

The proposed FD converter is designed in a modular fashion using a unit 2:1 cell that can be cascaded to realize additional binary ratios. The transistor-level schematic of this unit cell is shown in Fig. 3.8, and consist primarily of four power switches, M1-M4, implemented using thin-oxide transistors (1.5V max in the employed 0.18 μm SOI process). The power switches are driven by pre-drivers that operate with the same voltage range as the output ($V_0 \sim (V_H[i] - V_L[i]) < 1.5$ V). The M3 and M4 pre-drivers thus operate between $\{V_0, \text{GND}\}$, while the M1 and M2 pre-drivers

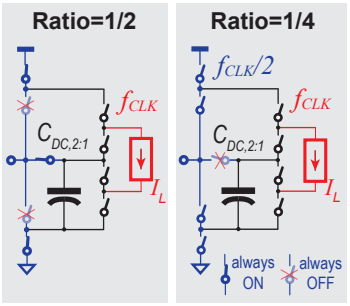


Figure 3.9: Reconfiguring the implemented FD converter between the 2:1 and 4:1 modes.

are level shifted via a 70 fF MOS capacitor (C_C) and static latch that can operate over a wide V_{BAT} range, for driving the switches between $\{V_{BAT}, V_0\}$. A static latch instead of a cross-coupled PMOS structure is selected in the level shifter to avoid level shifter output drift by the PMOS transistors leakage at low frequencies. To provide clock signals with wide frequency range ($\sim$100Hz to 300MHz) while operating down to $V_{BAT} = 0.4$ V, a 4-stacked min-sized transistors $(1/2)$ inverter is used in the level shifter to establish a weak feedback in the latch. Such weak feedback enables a small coupling capacitor C_C to change the latch state by the trigger CLK_IN inverter, while maintaining static retention against any leakage. Non-overlapping clock phases, Φ_1 and Φ_2, are then generated by 3-transistor based inverters with feedback from the power switches themselves to ensure minimal dead-time across all corners, given the wide input voltage range, and thereby eliminate any shoot-through current. According to simulations, the dead-time circuit achieves 64.8 ps and 110 ps non-overlap at FF and SS corners, respectively. A fork-based clock tree is used to distribute balanced CLK and CLK_H signals across the power stage in order to further reduce shoot-through currents.

The power stage can be recursively modularized [34] to implement a reconfigurable 2:1 and 4:1 converter as illustrated in Fig. 3.7a. In the 4:1 mode FD_2 is operated at half the frequency of FD_1 by dividing the input clock frequency using a D flip-flop. In the 2:1 mode, switches M1 and M4 (S5 and S8 in Fig. 3.7a) are permanently enabled in FD_2 via selection logic, as illustrated in Fig. 3.9. Switches S1 and S4 in FD1 Fig. 3.7a can also be permanently enabled to generate the

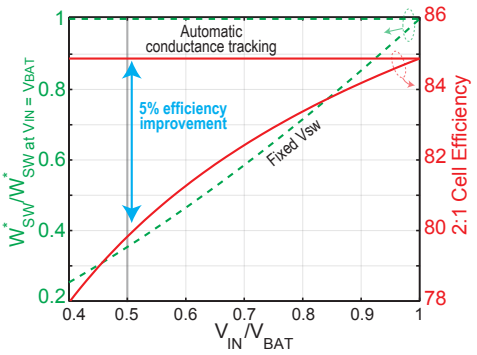


Figure 3.10: Plot of switch width (left axis, green dotted curves) and efficiency (right axis, red solid curves) with and without automatic conductance tracking.

1:1 ratio.

3.4.2 Switch-Load Voltage Matching for Optimal Conductance Tracking

When the input voltage changes or the FD converter is reconfigured between the $1/4$ and $1/2$ ratios, the optimal total switch conductance (i.e., width) could change, which would normally require enabling or disabling a portion of power switches in order to realize the optimal design point, as in similar SC implementations [35, 54], thereby limiting efficiency in ultra-low-power applications. Fortunately, the proposed level-shifting pre-driver structures described in the preceding section ensure that power switches are automatically driven by a gate voltage that is matched to the respective cell load voltage, along with the pre-driver logic circuit (for matched overhead), when the input voltage changes. By matching the respective cell switches drive voltage V_{sw} to the flying load voltage V_{FDi}, the switches R_{on} follows the same scaling trend of the load resistance R_L $(1/C_L f_{clk})$ under DVFS, where R_{on} and f_{clk} are proportional to $1/V_{FDi}$ and V_{FDi} respectively, and hence the optimal switch width W^*_{sw} from (3.6) is almost fixed as V_{BAT} or ratios change. The inherent switch-load voltage match enables direct cascading of the multi-level FD unit cells without complicated and power-consuming gate-drive-voltage conditioning circuitry, achieving a nearly optimal design point across all ratios and input voltages, as illustrated in Fig. 3.10 where a $\sim$5% efficiency improvement is observed.

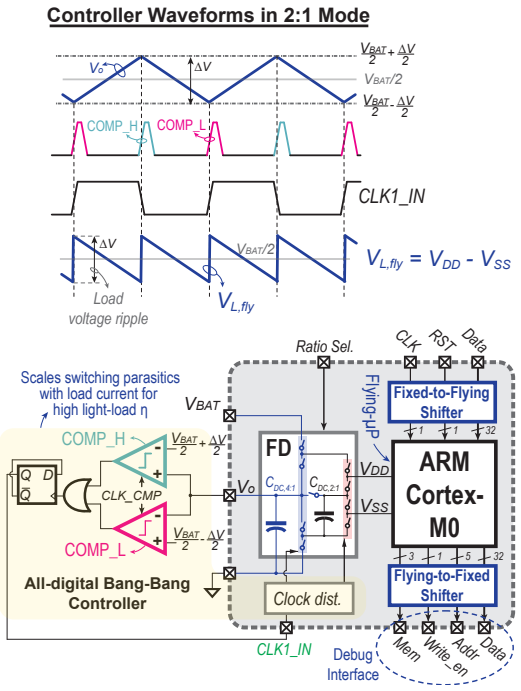


Figure 3.11: Transient waveforms of the hysteretic controller and block diagram of the reconfigurable 4:1/2:1 FD converter powering an ARM Cortex M0.

3.4.3 Hysteretic Control

The intermediate node of the FD converter, V_0, shown in Fig. 3.8 for the 2:1 converter, and Fig. 3.7a for the 4:1 converter, is a scaled value of the AC voltage across the flying domain, yet is referenced to GND. This presents an ideal fixed-domain position to sense the flying-domain voltage change in order to control the FD converter (i.e., without having to fly comparators). As illustrated in Fig. 3.11, when the load transitions between up and down positions, the flying load voltage, $V_{L,fly}$ jumps to $(V_{BAT}+\Delta V)/2$ and linearly decays to $(V_{BAT}-\Delta V)/2$ over a half cycle. Similarly, when the load is connected to the up (down) position, any capacitance at node V_0 will linearly charge (discharge) from $(V_{BAT}\pm\Delta V)/2$. Thus, the ripple across $V_{L,fly}$ and V_0 have the same magnitude (in this case ΔV), but are shaped as sawtooth and triangular waves, respectively. The FD converter, either in the 2:1 or 4:1 mode, can then be controlled via a hysteretic scheme by sensing V_0 and comparing to voltage bounds $\Delta V/2$ above and below $V_{BAT}/2$, as shown in Fig. 3.11. The proposed hysteretic approach scales switching frequency, and thus switching parasitics

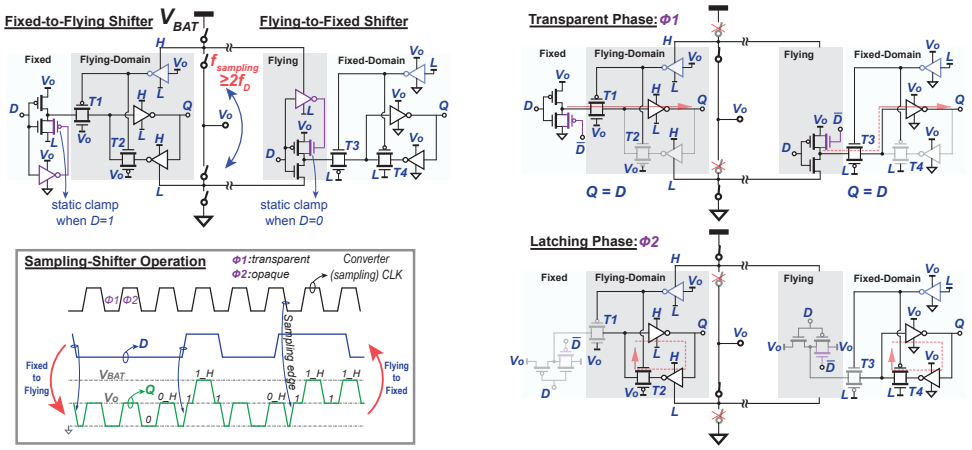


Figure 3.12: Schematic and example timing diagram of the proposed sampling level shifters.

with load current, thereby enabling high efficiency across a wide dynamic current range. Due to time limitations at design time, the hysteretic comparators were not included on-chip, and are thus implemented off-chip using Analog Devices ADCMP600 for testing purposes, though it is expected that the area and power overhead of integrated comparators will be minimal, as in conventional integrated voltage regulators. In a fully-integrated control loop, an ARM-based comparator architecture that relies on regenerative feedback latch [55] and consumes several 10s μW in 0.18 μm SOI will be employed as in prior fully-integrated SC converters [56].

3.4.4 Flying-Domain Interface Shifters

Since the digital load in an FD converter is flying with respect to the battery terminals, all I/O must be level-shifted from the normally fixed domain, $\{V_0, \text{GND}\}$ into the periodically changing voltage-state of the load, $\{V_{BAT}, V_0\}$ or $\{V_0, \text{GND}\}$. This is accomplished using area-efficient sampling level shifters for low-frequency signals, and faster continuous-time level shifters for high-speed signals.

The proposed sampling fixed-to-flying and flying-to-fixed level shifters are shown in Fig. 3.12, and consist of cascading an inverter powered between $\{V_0, L\}$, where L is the dynamic low rail of the flying domain (master stage), with a latch (slave stage) operating between the FD

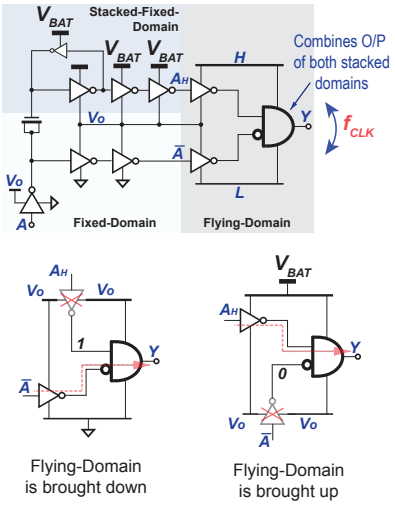


Figure 3.13: Schematic of the proposed continuous-time level shifters.

rails. When the FD is down (operating between $\{V_0, \text{GND}\}$), the master stage is transparent and the D input is passed to the slave stage output Q. When the FD is up (operating between $\{V_{BAT}, V_0\}$), the slave stage holds the data via static latch feedback. Thus, the sampling fixed-to-flying level shifter samples the input waveforms on the rising edge of the sampling clock, and thus the converter clock should be at least twice the frequency of the I/O signals, i.e., the Nyquist rate, as illustrated in Fig. 3.12. A similar operation follows for the sampling flying-to-fixed shifter, where the slave stage's rails are instead connected to the fixed domain. In either case, a static clamp transistor, as shown in Fig. 3.12, is added to the master stage to enable a low-impedance master stage output node and to prevent possible overstress of the master transistors at high voltage operation during the latching phase.

For I/O operating at a higher frequency than the converter clock, a continuous-time level shifter, depicted in Fig. 3.13, can be employed. In this case, the I/O is level shifted from $\{V_0, \text{GND}\}$ to $\{V_{BAT}, V_0\}$ using a conventional 70 fF capacitive level shifter (and weak-feedback static latch), and a combiner circuit, implemented using a CMOS AND gate, dynamically chooses either the up or down domain signals, A_H or $\bar{A}$, respectively, depending on the state of the FD load. The continuous shifter occupies 1.3× more area and consumes 1.6× more power than the

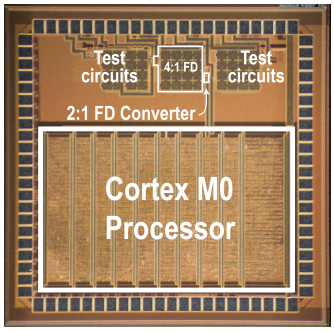


Figure 3.14: Die photograph of the test chip.

sampling shifter, and is thus only used for high speed signals when necessary.

In a typical digital processor, input conditioning and voltage level translation are required from the external high-voltage bus. The back-to-back latch (slave stage) of the proposed shifter can be infused within the high-voltage level translation buffering to minimize the overhead of the proposed shifters.

3.5 Experimental Verification

In order to experimentally verify the benefits of the proposed flying domain converter, a prototype converter was implemented and validated in a 0.18 μm SOI process. Several different versions of the converter were implemented in order to illustrate functionality and quantify performance for different load conditions: a resistive load, a cascaded inverter/ring oscillator load, and an ARM Cortex M0 processor load. In all cases, the FD converter and all its circuitry were powered via a 0.4-3 V input battery voltage, and all measurements were taken via 4-wire connections. A die photo is shown in Fig. 3.14. It should be noted that while the presented design is implemented in an SOI process, which helps to reduce bottom plate parasitics, FD converters can be implemented in bulk processes if triple-well options are available.

Figure 3.15 shows the conversion efficiency results when powering an on-chip resistive load. The load was implemented using a *p*-type unsilicided polysilicon over shallow trench

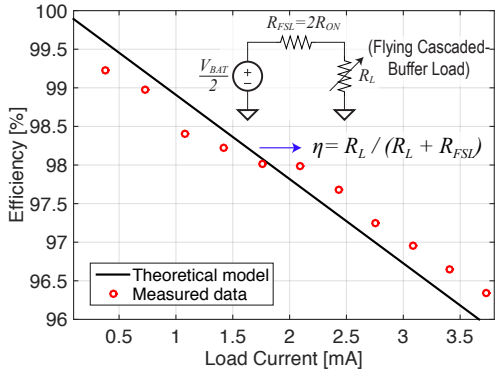


Figure 3.15: Measured efficiency of the 2:1 FD converter when powering an on-chip inverter string.

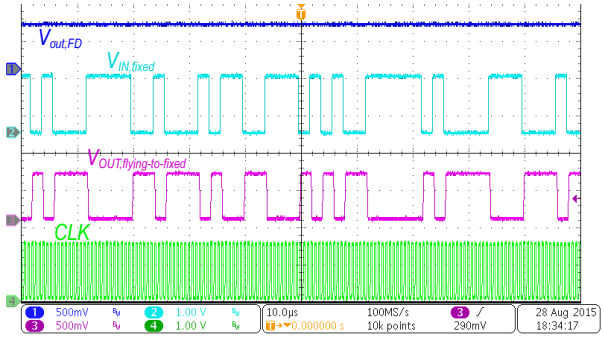
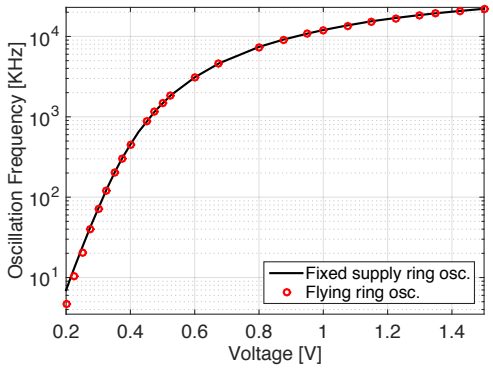
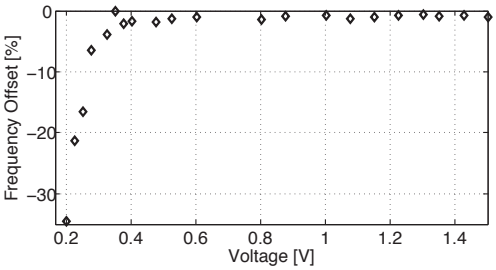


Figure 3.16: Measured input and output of the cascaded inverter chain when powered by the FD converter.

isolation resistor, with 320 Ω/□ with a minimum width of 10 μm. The implemented resistor can be probed externally through two I/O pads, and was measured using a precision multimeter to be 645.6 Ω. Careful layout was followed so that the on-chip resistor suffers from minimal top/bottom capacitance due to the I/O pads, which in fact act as symbiotic capacitance to retain state during brief non-overlap periods. The FD converter occupied 295 μm^2, including switches, pre-drivers, non-overlap circuitry, and capacitive level shifters. When powering the 645.6 Ω resistor at 1.5 V, the converter achieved an efficiency of 91.7% at a power density of 11.8 W/mm^2 (2.3W/mm^2 when including the 13.1 pF on-chip decoupling implemented using 10.7 fF/μm^2 MIM plus MOS stacked capacitance). This measured efficiency matches the results predicted from 3.8 with $<$1% error when replacing C_{FLY} in 3.8 with C_{DC} for the FD converter.



(a)



(b)

Figure 3.17: Measured frequency of the on-chip ring oscillator when powered from a conventional supply and from the FD converter (a). Measured frequency offset between the two configurations (b).

To demonstrate that the proposed FD converter can power conventional digital loads, another FD converter was designed to power a cascaded chain of inverters (of total equivalent load capacitance $C_L \sim 31$ pF) that can be driven directly from off-chip, or configured as a ring oscillator. To first validate that flying the inverters did not affect performance, and to further validate the performance of the fixed-to-flying and flying-to-fixed level shifters, the cascaded inverter load was first driven by an off-chip signal generator operating in the fixed domain ($V_{IN,fixed}$). This signal passes through a fixed-to-flying level converter, through the flying-domain inverter chain, and then through a flying-to-fixed level converter ($V_{OUT,flying-to-fixed}$). Figure 3.16 summarizes this measurement result, showing the input and output data match after a small delay and an inversion. Unlike conventional SC circuits whose efficiencies stay relatively constant at smaller currents due to the increasing SSL losses that trade-off with reduced switching frequency, the

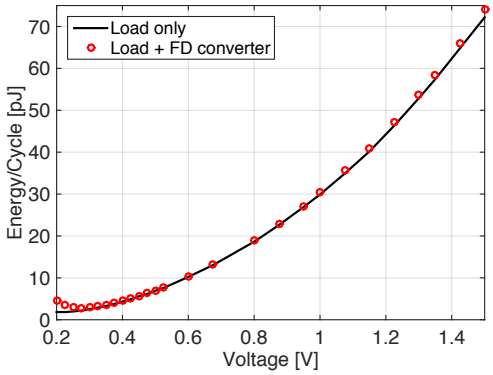


Figure 3.18: Measured energy of the ring oscillator load when powered from a conventional supply (solid line) and from the FD converter (red circles).

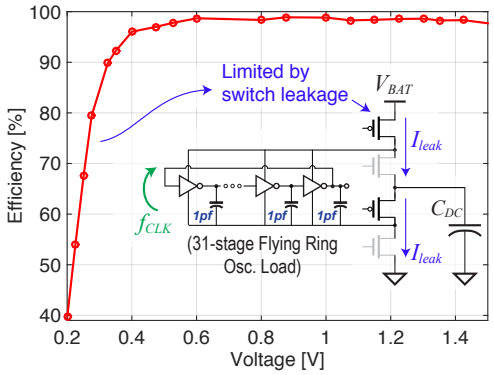


Figure 3.19: Measured efficiency of the 2:1 FD converter when powering a ring oscillator load.

efficiency of the proposed FD converter actually increases with lower load current, as shown in Fig. 3.15. This increase in efficiency occurs due to the absence of SSL losses in the employed operating range from a reduced SSL-FSL corner frequency thanks to a 10 nF off-chip decoupling capacitance (commonly used in DC-DC converter design and as decoupling to many digital loads [17, 22, 57, 58, 59]). Since SSL losses are minimal in this operating regime, the FD converter can be modeled by the converter's FSL resistance (i.e., $2R_{on}$), driving an effective load resistance, R_L, whose magnitude increases with a reduction in current. The FD converter achieves a peak efficiency of 99.2% at a current of 0.37 mA, and is within 0.4% of the simple resistive divider circuit model depicted in Fig. 3.15 for currents ranging from 0.37 to 3.7 mA ($V_{BAT} = 3$ V).

Next, the inverters were configured as a ring and powered under two different scenarios:

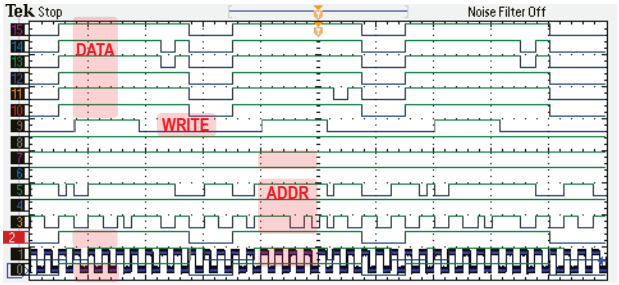
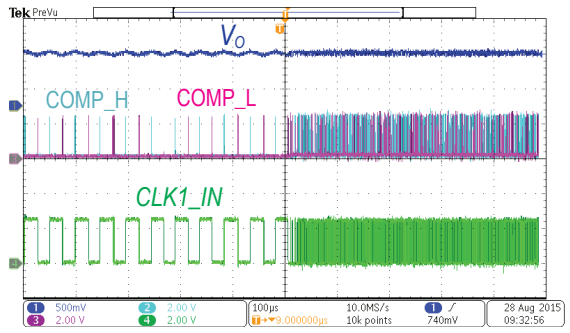


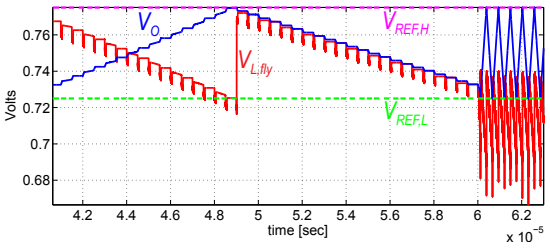
Figure 3.20: Measured debugging I/O waveforms of the M0 processor after level shifters.

via the FD converter, and via a regular power supply set to exactly half the input voltage of the FD converter. As shown in Fig. 3.17, the output frequency of the ring oscillator matched between the two cases to within 2% for output voltage ranging from 0.4 to 1.5 V with less than 50 mV_{pp} ripple. To validate the efficiency of power conversion, the energy per cycle of the ring when powered directly from a regular supply was compared to total energy per cycle consumed at the input of the FD converter. As summarized in Figs. 3.18 and 3.19, the FD converter, thanks in part to the automatic optimal conductance tracking, achieved an efficiency greater than 96% from 0.4 to 1.5 V, with reduced efficiency below 0.4 V due to power switch leakage. The FD converter in this implementation also contained switches to enable the 4:1 mode (with $C_{DC,2:1}$ = 810 pF), and at an input voltage of 1.6 V and output voltage of 0.4 V, the 4:1 FD converter achieved an efficiency of 90.5% when powering the ring oscillator with 0.014 W/mm^2 peak power density. In this implementation 4:1 power density was limited by low-density capacitance used for the inter-stage flying decoupling; higher power density can be achieved with denser capacitance, as in conventional SC converters.

To validate that the FD converter concept can power larger, more conventional digital loads, another FD converter was implemented to power a co-fabricated ARM Cortex M0 processor. The processor occupied 1.95 mm^2, and the entire processor was switched around an off-chip 10 nF decoupling capacitor. Typical values of off-chip decoupling for commercially available ARM Cortex M0 ranges from 100 nF to 10μF [58, 59]. All regular I/O were buffered via sampled level shifters, with the exception of the digital clock that employed a continuous level shifter for



(a)



(b)

Figure 3.21: Measured controller waveforms (a) and simulated voltage across flying load $V_{L,fly}$ (b) under a current step from 21.8 μA to 1 mA.

higher-speed operation. The processor consumed 3.63 mA at 1.5 V when running a checksum program at 1 MHz as measured by a conventional power supply. Figure 3.20 shows measurement results of several key debugging I/Os after level shifting when flying the entire processor as the load within the FD converter, indicating successful operation. The FD converter in this case achieved an efficiency of 90.8%, limited by the equivalent bottom-plate parasitics of the load itself.

The hysteretic controller, enabled by the fact that the internal V_O node represents the output load voltage, is validated through load step measurements in Fig. 3.21a. When stepping load current from 21.8 μA to 1 mA using a step frequency input to the on-chip cascaded buffer (V_{BAT} = 1.5 V), the employed hysteretic controller responds within $\sim$ 330 ns, and achieves a ripple lower than 50 mV$_{pp}$ at V_O. At steady-state, with the controller hysteresis is set to 50 mV, the controller maintains $\sim$ 50 mV$_{pp}$ and $\sim$ 62 mV$_{pp}$ voltage ripple across the flying domain while the cascaded chain sinking 21.8 μA and 1 mA, respectively, with the extra $\sim$ 10 mV under

1 mA load due to the brief non-overlap time, as shown in Fig. 3.21b. The voltage ripple can be reduced through a smaller hyesteresis window. The average voltage across the flying domain drops by $\sim$ 35 mV at 1 mA load, due to the internal $R_{out} \sim 35\ \Omega$, as shown in Fig. 3.21b.

A table of comparisons is shown in Table 3.1.

3.6 Conclusion

A flying-domain power conversion concept has been presented that obviates the need for large flying passives by instead flying the load circuit itself. Experimental results from a 0.18 μm test chip reveal the proposed topology can achieve upwards of 11.8 W/mm^2 power density (2.3 W/mm^2 when including on-chip decoupling) at 91.7% efficiency, while achieving upwards of 99.2% peak efficiency at 0.37 mA when a large decoupling capacitor is used. The presented theory, models, and experimental results show that the FD power conversion concept can power practical digital loads with high efficiency and power density.

3.7 Acknowledgements

This chapter is based on and mostly a reprint of the following publications:

- L.G. Salem, J.G. Louie, and P.P. Mercier, "Flying-domain DC-DC power conversion," IEEE Journal of Solid-State Circuits (JSSC), Dec. 2016, vol. 51, no. 12, pp. 2830-2842.
- L.G. Salem, J.G. Louie, and P.P. Mercier, "A flying-domain DC-DC converter powering a Cortex-M0 processor with 90.8% efficiency," 2016 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2016, pp. 234-236.

Table 3.1: Table of comparisons to prior-art SC and resonant converters achieving high power density or efficiency

	[17]	[22]	[15]	[20]	[57]	[60]	This work
Technology	45nm SOI	130nm	22nm Tri-Gate	32nm SOI	180nm HV	65nm	180nm SOI
Converter type	SC	SC	SC	SC	Resonant	SC	Flying Domain
Topology	1/2	1, 2/3, 1/2, 1/3	1, 4/5, 2/3, 1/2	2/3, 1/2	1/2	1/2, 1/3, 1/4	1, 1/2, 1/4
Flying capacitor type	Deep trench	Ferroelectric	MIM	Deep trench	MIM	MIM / MOS	N/A
Total flying capacitance [nF]	2	8	1.6	1	24.6	-	None
Vin [V]	2	1.5	1.225	1.8	3 or 6	1.2	0.4 - 3
Vout [V]	0.95	0.4 - 1.1	0.45 - 1.05	0.7 - 1.1	1.85 or 3.7	0.25 - 1.2	0.2 - 1.5
Power density of power stage [W/mm2]	2.2	0.003	0.5	3.71	N.R. / Off-chip inductors	N.R.	11.8
Power density including output decoupling [W/mm2]	N.R. / Off-chip decoupling	N.R. / Off-chip decoupling	N.R. / On-chip decoupling	3.71 (multi-phase interleaving)	0.91	N.R.	2.3
Efficiency @ peak power density	90%	92%	N.R.	90%	85.1%	N.R.	91.7%
Peak efficiency	90%	93%	84.2%	90%	89.1%	82%	99.2%
Load current [mA]	2.62	0.02 - 1	88	764	2081	0.002 - 0.6	0.37 - 3.7

N.R. = Not Reported

Chapter 4

A Switched-Capacitor Power Management Integrated Circuit

4.1 Introduction

Mobile electronic systems powered by Li-ion batteries typically employ a power management integrated circuit (PMIC) to step-down the 2.8-4.2V battery voltage. For their continuous regulation capability, switched-inductor architectures are often the preferred choice. In contrast, switched-capacitor (SC) PMICs utilize discrete capacitors that can have 7× lower BOM cost, and 8× smaller footprint than typical power inductors, yet are only efficient at discrete ratios of input-to-output.

In this chapter, a switched-capacitor (SC) PMIC is presented that achieves up to a 6.6-bit resolution with only 5 flying capacitors for inductive PMIC replacement. The flying capacitors are reused in a frequency-scaled gear train as well as charge-feedback SC topologies to attain a 2.4× reduction in capacitors number compared to prior art. In 0.25μm bulk, the PMIC operates from an input voltage of 2.5-5V, can generate an output voltage ranging from 0.2-2V, and features an average efficiency of 90.2% across the entire range and a peak efficiency of 95.5%.

4.2 Frequency-Scaled Gear-Train SC Topology

In conventional SC topologies, a bypass capacitor is required for charge balancing between the flying capacitors to enable a valid steady state output. For example, when switching two cascaded cells in a 4:1 SC as illustrated in Fig. 4.1, capacitors, C1 and C2, are stacked in $\Phi 1$ and 1/2 of the charge is delivered to V_{out}. However, without a bypass capacitor, C_{DC}, between the two cells, C1 will keep charging until V_{out} reaches 0. Another viable solution would be to have another 2:1 SC converter cell in parallel to the second cell, C2, operating out of phase. Unfortunately, in both solutions three capacitors are required. On the other hand, by switching the last cell, C2, at twice the frequency of the first cell, C1, the extra required bypass or out-of-phase capacitor is eliminated. In the proposed gear train (GT) topology, also illustrated in Fig. 1, each pair of cascaded cells is operated as in a bucket brigade: the flying capacitance of each stage does not commence gathering new charge (i.e., is switched to the next clock phase) until the flying capacitor of the following stage retrieves its charge. By eliminating C_{DC} that does not in fact contribute to the charge shuttling, the proposed topology reduces the incurred charge sharing loss for the same capacitance, e.g., 2.75× in the Fig. 1 example. For illustration, the proposed GT SC requires only 5 capacitors instead of a minimum of 7 in the highest conversion ratio topology from prior-art [31] to reach a ratio of 32:1.

Fig. 4.2 shows simplified examples of the proposed binary GT and charge-feedback (CF) SC. To realize binary modd/2^N ratios, N 2:1 SC cells are connected in cascade/stack and operated at binary scaled frequencies, $f_{N-1}/2^{N-i}$, where i is the stages order in the cascade. The proposed binary topology minimizes the inter-stage loading in the low-voltage train by maximizing the number of VINT0 and 0 connections. With 5 cascaded cells, a binary 5-bit resolution can be achieved. To further extend the achievable ratios, the ground charge of the 1st 2:1 cell is routed from the 2nd cell, enabling an additional 2^{N-1} CF ratios. In Fig. 2, up to 9 unique ratios exist in the lower 2/3 of VBAT, for a total of 24 ratios that can be generated from 5 capacitors, which

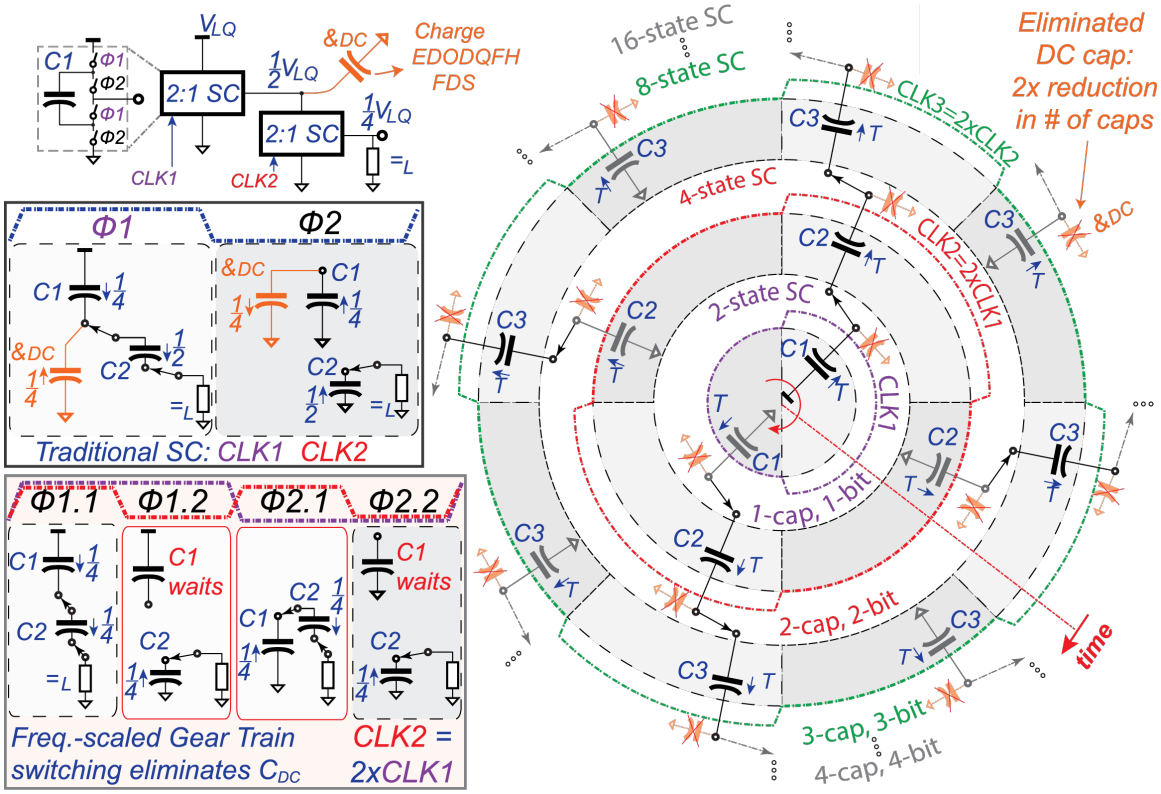


Figure 4.1: Proposed frequency-scaled gear-train switching scheme illustrating how to eliminate inter-stage decoupling capacitors for a 2× reduction in the required capacitors for binary ratios.

enables up to 6.6-bit ratio resolution that would otherwise require a minimum of 12 capacitors in a conventional binary SC [34, 56].

4.3 Circuit Implementation

The switch-level block diagram of the implemented SC PMIC is shown in Fig. 4.3. The SC enables a cascade/stack of 5 cells (schematics in Fig. 4.4) with feedback capability amongst C0 and C1. The first stage of the converter uses a boundary cell to handle the high battery voltages while enabling output voltages in the lower half of VBAT. An on-chip clock divider is used to generate the various binary scaled clock phases for each stage. Instead of disabling the last cell in a cascade when realizing lower resolutions, backward cell-disabling is proposed such that the

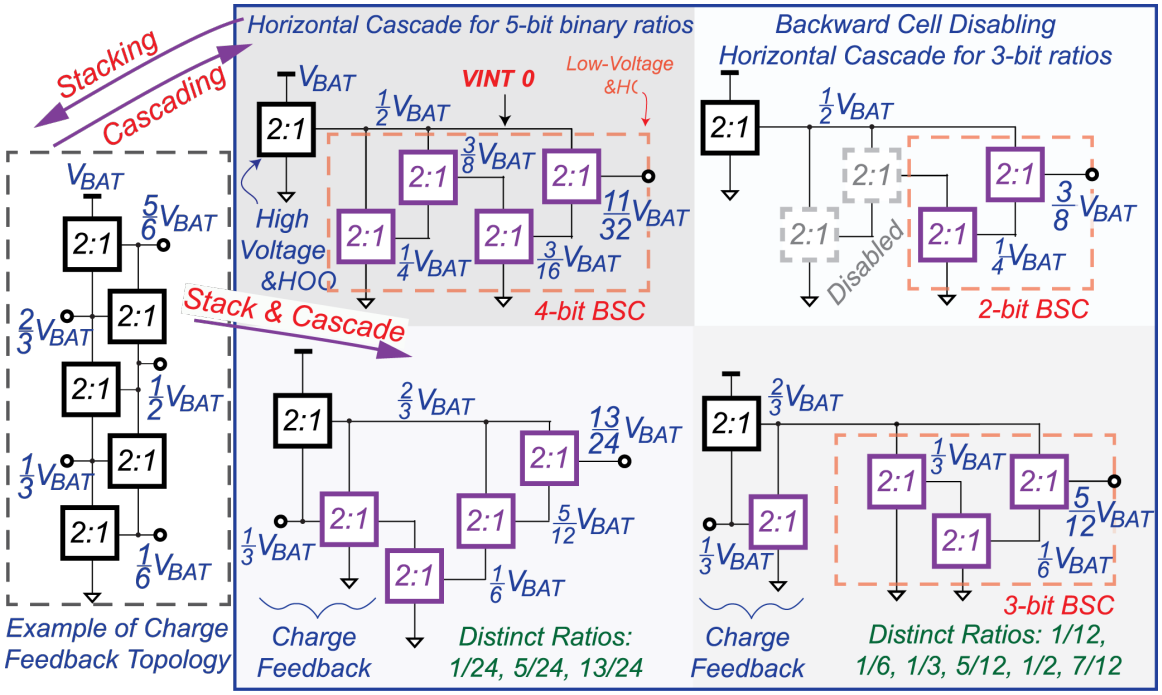


Figure 4.2: Examples of the proposed GT-binary and CF topologies. Overall, 24 distinct ratios can be achieved with 5 capacitors.

initial cells in the cascade are the ones disabled. For instance, to realize $m_{odd}/16$ ratios, cell C1 is disabled, while its driving clock is bypassed to C0. Through backward disabling, the last cell, C4, becomes the critical cell that switches at the maximum frequency and handles the largest current, localizing the packaging ESL and ESR challenges to the single capacitor of the final stage. With the proposed binary frequency scaling, the cells optimal conductance/capacitance relative sizing becomes almost identical, though with $2\times$ for the first cell. The boundary cell is capable of handling voltages up to 5V while utilizing 2.5V thin-oxide devices through deep N-well stacking, and is driven through capacitive level shifters.

4.4 Measurement Results

The SC PMIC is fabricated in a 0.25μm 5M bulk CMOS process (Fig. 4.8). Through the stacked voltage domains of the first stage, the chip can operate beyond the Lithium-ion

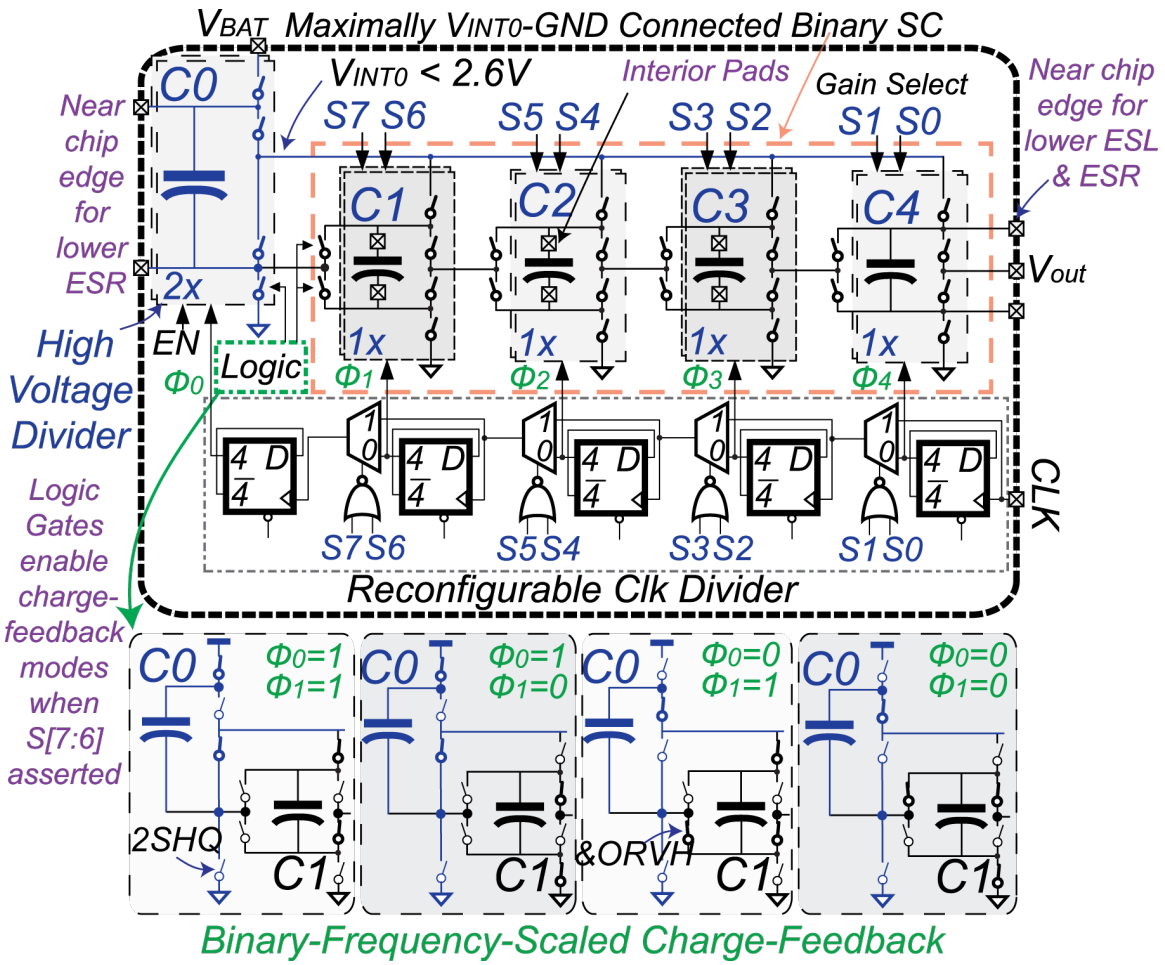


Figure 4.3: Switch-level block diagram of the implemented converter and switching states of the implemented CF.

battery range, achieving a total input range of 2.5-5V. At the same time, due to the 24 available ratios, a wide output range of 0.2-2.0V is achievable with output power up to 186mW. In this implementation, 4.7μF and 2.2μF $1\times0.5\times0.6$mm^3 SMD capacitors are used for the first and remaining stages, respectively. Figures 4.5 and 4.6 outline the measured and modeled efficiency at various Lithium-ion voltages for a DVS-modeling load resistors. The efficiency peaks at 95.5% and 91% and averages to 91.7% and 84.4% over 0.5-1.8V with VIN=3.6V at 120Ω (Fig. 4.5) and 20Ω (Fig. 4.6), respectively. Further, the proposed CF topology maximizes the utilization of the already existing 5 capacitors and realizes another 9 distinct ratios, 4 of which extend the V_{out} range by up to 35% and enable operation at a low-battery voltage of 2.8V to a V_{out}=1.46V

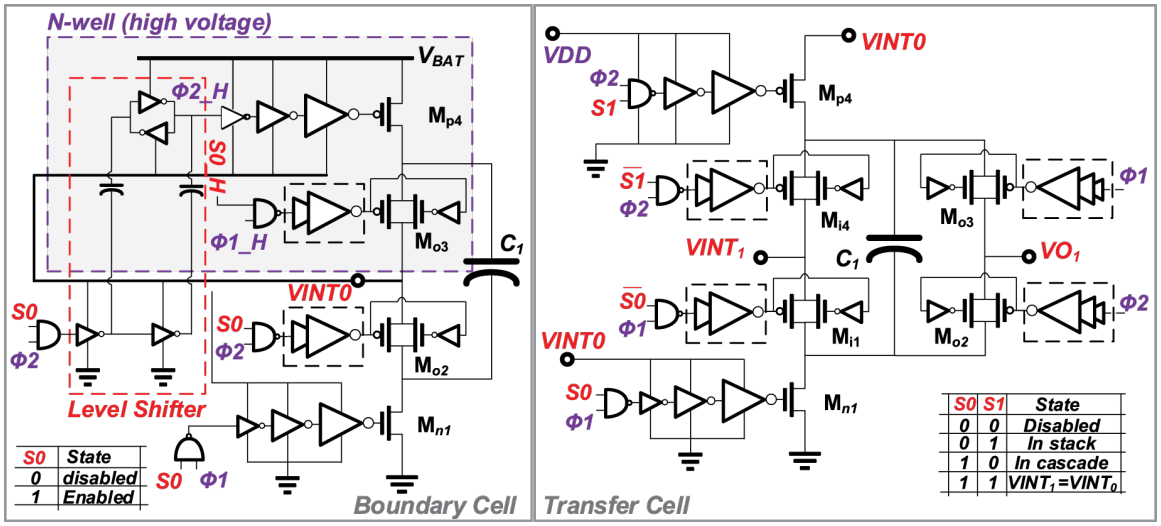


Figure 4.4: Implementation of boundary and transfer cells.

with a 20Ω load. The CF ratios help to fill the gaps between the binary ratios, with a maximum improvement of 9.5%. As shown in Figs. 4.6 and 4.7, the modeled and measured results match to within 1.5%. Compared to a modeled 3-ratio series parallel (SP) converter, a prominent topology used in present commercial charge pumps with 2 flying capacitors, the proposed PMIC with only 3 extra capacitors achieves efficiency improvements of up to 22.4% with a much wider operating range. Fig. 4.7 shows the PMIC operating at a constant load current, achieving greater than 80% efficiency down to 60μA. A table of comparison with the prior work is shown in Fig. 4.9.

4.5 Acknowledgements

This chapter is based on and mostly a reprint of the following publication:

L.G. Salem and P.P. Mercier, "A battery-connected 24-ratio switched capacitor PMIC achieving 95.5%-efficiency," 2015 IEEE Symposium on VLSI Circuits, Jun. 2015, pp. C340-C341.

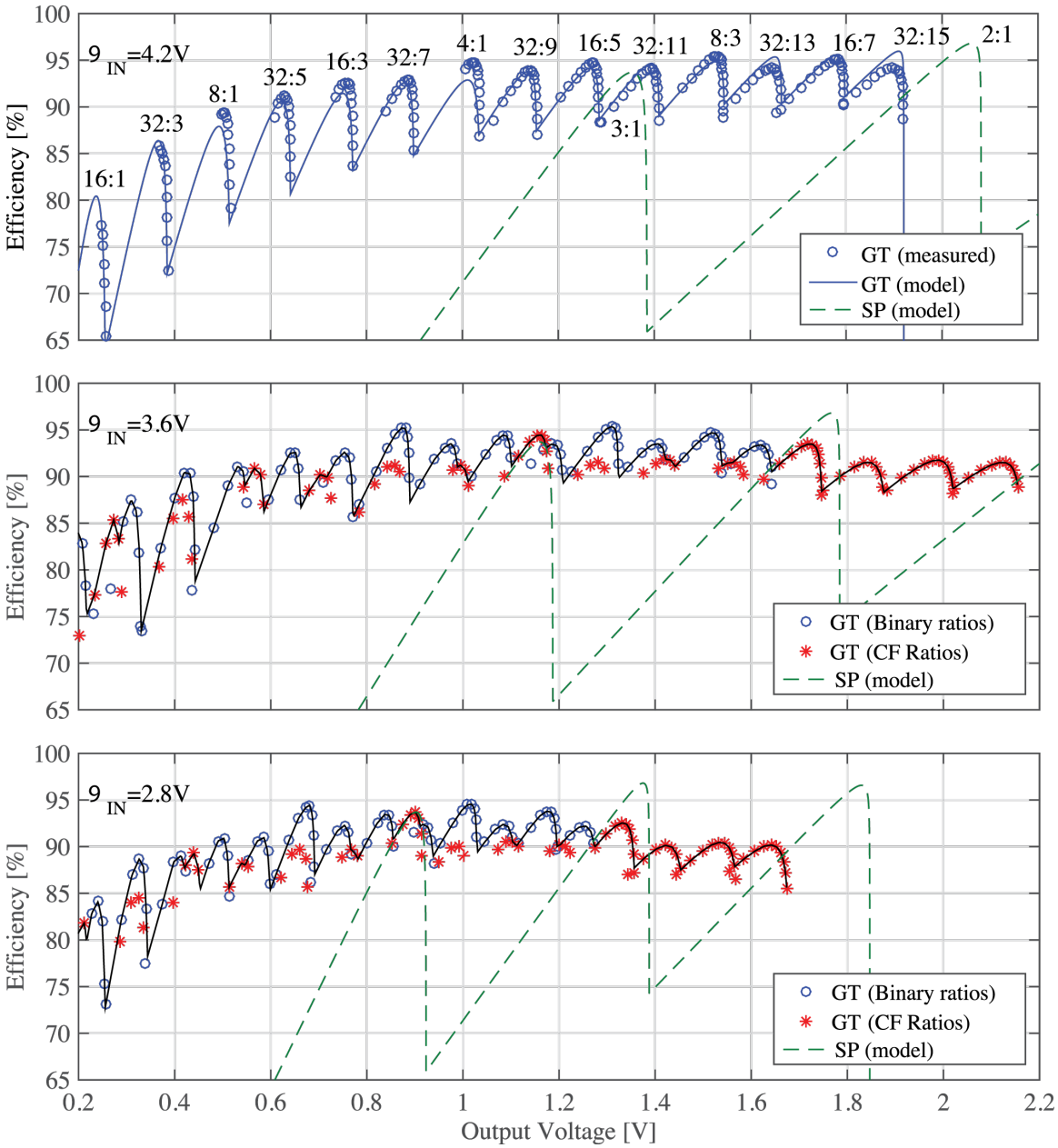


Figure 4.5: Measured and modeled efficiency curves of the SC PMIC at 4.2V, 3.6V, and 2.8V for a DVS-modeling load resistance of 120Ω.

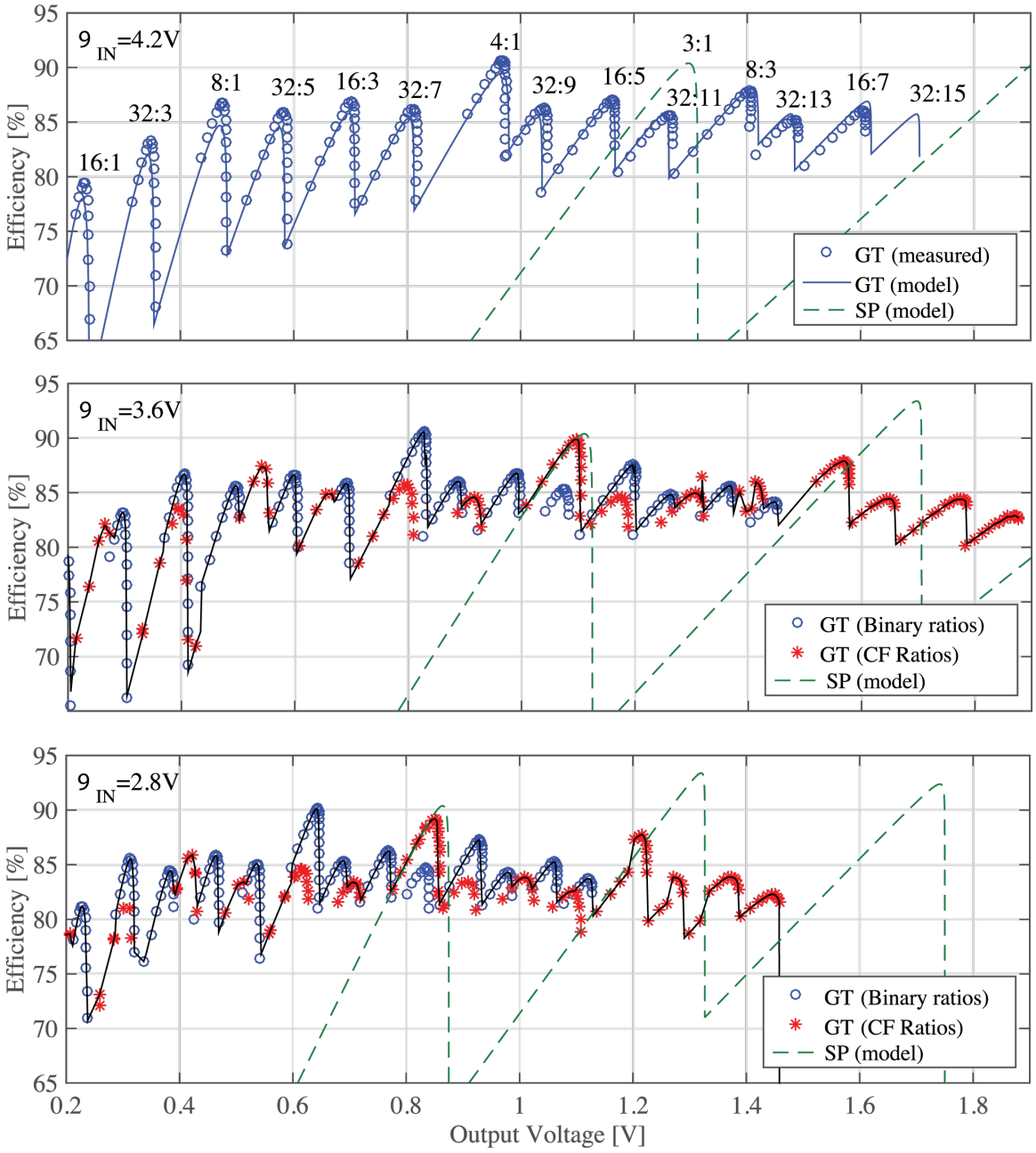


Figure 4.6: Measured and modeled efficiency curves of the SC PMIC at 4.2V, 3.6V, and 2.8V for a DVS-modeling load resistance of 20Ω.

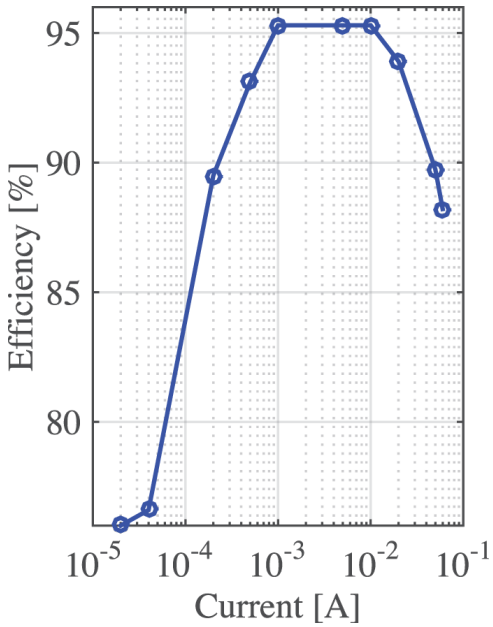


Figure 4.7: Efficiency of SC PMIC versus load current.

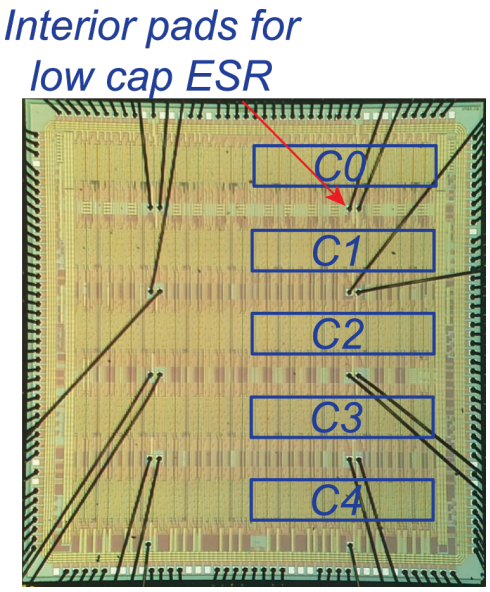


Figure 4.8: Die photo.

	V. Ng 2012	H.-P. Le 2013	S. Bandy. 2011	This Work
Technology	0.18µm HV	65nm	45nm	0.25µm bulk
Input voltage	7.5-13.5V	3-4V	2.8-4.2V	2.5-5V
Output voltage	1.5	1	0.4-1.2V	0.2-2V
Passive type	8x10µF	4 integrated capacitors	10µH inductor	1x4.7µF, 4x2.2µF
Estimated passive vol.	$20\times1.35mm^3$	-	$9\times1.3mm^3$	$2.5\times0.6mm^3$
Estimated passive cost	$0.20	-	$0.27	$0.10
Core area	$11.6mm^2$	$0.64mm^2$	$2.25mm^2$	$3.47mm^2$
Voltage resolution	7 ratios	2 ratios	5-bit DPWM	6.6-bit / 24 ratios
Topology	Dickson	2/5, 1/3	Buck	Gear Train / Charge Feedback
Peak Efficiency	92%	74.3%	87.4%	95.5%
Power handling	1.5W	162mW	100mW	186mW

Figure 4.9: Comparison with prior work.

Part II

Miniaturizing DC-to-AC Power Conversion

Chapter 5

A Recursive House-of-Cards Power Amplifier

5.1 Introduction

Design of battery-connected power amplifiers (PAs) that simultaneously achieve high output power, efficiency, and linearity in scaled CMOS is challenging, in part due to the low ($\sim$1V) breakdown voltage of thin-oxide transistors. Since most modern mobile systems utilize Li-ion batteries with voltages on the order of $\sim$4V, step-down conversion of the battery voltage via a DC-DC converter is typically required to safely drive scaled CMOS transistors. However, delivering $>$20dBm of output power to a 50Ω antenna requires $>$5V peak-to-peak swing, and thus the large battery voltage must be stepped down to drive thin-oxide CMOS transistors that perform RF waveform amplification, after which the low-voltage RF waveform is transformed back up to a higher voltage via an impedance transformation network in order to drive 50Ω with sufficient power. Converting voltages down then back up leads to cascaded losses that, in practice, limit achievable battery-to-RF efficiency of CMOS PAs to $<$30% [61]. While techniques like transistor stacking can help improve the voltage blocking capability of active PA elements

[62, 63, 64], such techniques are often employed in conjunction with linear biasing strategies (e.g., class-B) that have inherently poor efficiency.

Switched-mode PAs such as class-D amplifiers can, on the other hand, theoretically achieve high efficiency, and, importantly, leverage CMOS scaling. Since switched-mode PAs in isolation do not support amplitude modulation capabilities as required by modern spectrally-efficient communication standards, they are typically implemented in conjunction with techniques to impart amplitude modulation capabilities such as envelope elimination and restoration (EER) [65, 66, 67], outphasing [68], or pulse-width modulation [69]. Alternative switching approaches such as direct RF digital-to-analog converters (DACs) [70], digital power combining [71, 72], and switched-capacitor (SC) PA [73, 74] can be used to, in some cases with the aforementioned amplitude modulation techniques, improve efficiency or linearity. However, while switched-mode PAs leverage transistor scaling, cascaded DC-DC converter, PA, and impedance transformation network losses are exasperated as supply voltages scale downwards, making design of efficient, linear, battery-connected CMOS PAs increasingly challenging.

This chapter presents the design of a digital power amplifier that, by stacking and flying unit class-D PA cells in a switched-capacitor House of Cards (HoC) topology, enables efficient high output power generation with a direct Li-ion battery connection, all while using thin-oxide CMOS transistors. Since the PA is modular and recursively reconfigurable amongst several battery-to-RF voltage ratios, high battery-to-RF efficiency is achieved both at peak and 6dB backoff power via a voltage-mode Doherty-like capacitive power combining technique.

Initial circuit schematics and measurement results were presented in [75]. In this chapter, the proposed HoC topology is introduced and contrasted to prior-art PA approaches in Section II, while Sections III and IV provide the implementation details. Section V presents detailed measurement results, and Section VI concludes the chapter.

5.2 House-of-Cards Switched-Capacitor Power Amplifier

As described in the previous section, the design of PAs in scaled CMOS processes to provide high output power with high efficiency constitutes multiple challenges related to low transistor breakdown voltages. In this section, we discuss the design evolution of the HoC PA topology to realize high-output voltage swing while operating directly from a battery using scaled CMOS devices. A charge-recycling DC-DC conversion scheme is introduced to realize implicit high-efficiency DC-DC conversion directly from a high-voltage input power source. Then, the ladders of stacked PA cells are connected in cascade to provide efficient series power combining without any magnetics. Although described for CMOS processes, the proposed architecture is also suitable for other technologies such as BJTs, MESFETs, HEMTs, etc.

5.2.1 Implicit DC-DC Conversion via Stacked-Amplifier Charge-Recycling

Non-constant envelope modulation schemes (e.g. QPSK, QAM, OFDM, etc.) are required to provide better utilization of the available bandwidth in modern communication standards. Such high peak-to-average power ratio (PAPR) signals require a PA with high efficiency across a wide dynamic power range. Class-G supply modulation has been demonstrated to achieve high efficiency at back-off by operating a nonlinear PA from multiple supply voltage levels, typically V_{in} and $V_{in}/2$, as determined by the input envelope signal in an envelope elimination and restoration (EER) scheme [67]. The supply modulator can be implemented using a linear voltage regulator [76, 77, 66] or a hybrid design that includes linear regulator in parallel to a switching supply modulator [78, 79]. In either case, the efficiency of the employed DC-DC converter is critical to the overall efficiency of the system.

Figure 5.1a illustrates a nonlinear class-D PA when powered through a DC-DC converter to realize the 6dB back-off operation in a class-G system. The modulator typically requires off-chip or large on-chip inductors and causes cascaded losses. Instead, high-efficiency implicit

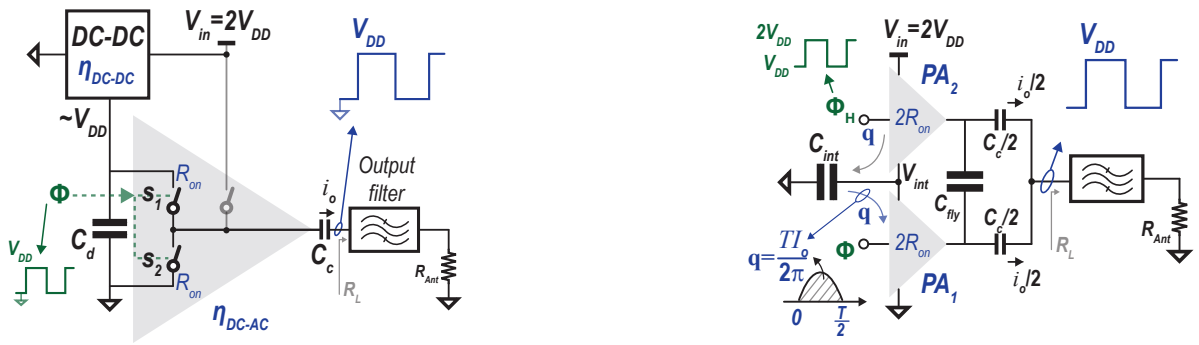


Figure 5.1: Conventional class-G operation during a 6dB back-off (a). Implicit 100% efficiency DC-DC conversion via charge-recycling PA stacking (b).

DC-DC downconversion can be realized by stacking two half-sized class-D PA cells, PA1 and PA2, each of half the PA total conductance, on top of each other while coupling their outputs through a flying capacitor C_{fly}, and operating the stack from $V_{in} = 2V_{DD}$, as shown in Fig. 5.1b. Each PA in the stack delivers half the total output power, $P_{out} = 2/\pi^2 V_{DD}^2/R_L$ [73], to the load R_L. The charge dumped by the top domain, $q = \int_0^{T/2} I_o/2\ sin(2\pi/T\ t)\ dt = TI_o/(2\pi)$, where T is the RF carrier period and $2q$ is the total output charge delivered during half the period, matches the charge absorbed by the bottom domain, thereby the intermediate node V_{int} is automatically balanced to V_{DD}. In a practical implementation, a small C_{fly} matches the switching phases for PA1 and PA2 and establishes a 2:1 SC DC-DC converter by reusing PA1 and PA2 switches to provide active regulation to V_{int}. Unlike the class-G DC-DC modulator that has to provide the total PA output power, the established 2:1 SC DC-DC sources or sinks only a small delta current due to minimal charge imbalance between the stacked domains, PA1 and PA2.

Figure 5.2 illustrates the switch-level block diagram and operation of the example 2-stack PA. The switches are controlled by the PM clock. Fig. 5.2b depicts the resulting networks during the phase when the PM clock is high (ϕ_1) and when the clock is low (ϕ_2). During ϕ_1 the odd-numbered switches are turned on, connecting the flying capacitor, C_{fly}, between the mid-level voltage, V_{int}, and ground. Consequently, capacitors C_{fly} and C_1 are connected in parallel and

charge sharing occurs to balance the voltage across C_1 to $V_{in}/2$ at steady state. During ϕ_1, R_L is AC-coupled to V_{int} and GND through the switches s_3 and s_1 in parallel, while C_{fly} holds a DC voltage of approximately V_{DD}. From Fig. 5.2b, during ϕ_1 the top PA2 charges the intermediate node V_{int} by a half sinusoid with amplitude $I_o/2$. Therefore, V_{int} jumps by $\Delta V \approx \frac{TI_o}{(2\pi)(C_1+C_2+C_{fly})}$. In ϕ_2, the even-numbered switches are on, connecting C_{fly} in parallel to C_2 in order to balance the voltage across C_2 to $V_{in}/2$. At the same time, ac-coupled R_L is brought up to V_{in} and V_{int} through switches s_4 and s_2. On ϕ_2, the charge $q = TI_o/(2\pi)$ stored on the capacitors C_1, C_2, and C_{fly} during the prior phase is released back to supply PA1, and hence V_{int} droops by ΔV.

Alternating between the two phases ϕ_1 and ϕ_2 along with the boundary condition of continuous voltage across the capacitors C_1, C_2, and C_{fly} during phase switching, enforces all capacitors voltages and V_{int} to reach $V_{in}/2$ at steady state through the imposed KVL equations, irrespective of the initial voltage level [80]. The proposed topology thereby utilizes the switches to perform simultaneous power delivery at both the DC and the RF f_o components.

The size of the capacitors C_1, C_2, and C_{fly} determines the amount of voltage ripple, ΔV, on V_{int}. For 10% ripple, C_1, C_2, and C_{fly} should be assigned equal sizes, i.e. one third, of a total on-chip capacitance of $10 \times TI_o/(2\pi V_{DD})$. In order to reduce the amount of required capacitance, an AC virtual ground is created at V_{int} in Fig. 5.2c by tying together the V_{int} nodes of two 2-stack PAs and driving them in opposite phases. Through the established differential operation, the current dumped by PA2$-$ into V_{int} cancels the current drawn by PA1 during $\phi 1$, and vice versa in $\phi 2$, and hence the required total capacitance for DC balancing is nearly zero. Practically, C_1 and C_2 should still be large enough to decouple the required gate drive charge, i.e. $C_1 = C_2 \approx 10 \times C_G$, where C_G is the total gate capacitance of PA1 or PA2. This decoupling capacitance is typically implemented using thin-oxide MOS gate capacitance. Unlike the power switch that is typically implemented using multiple parallel fingers with large area overhead for drain and source regions, the MOS capacitor can be implemented using a single transistor finger of almost equal width and length, and therefore in a denser manner. The parasitic top/bottom capacitors of the required

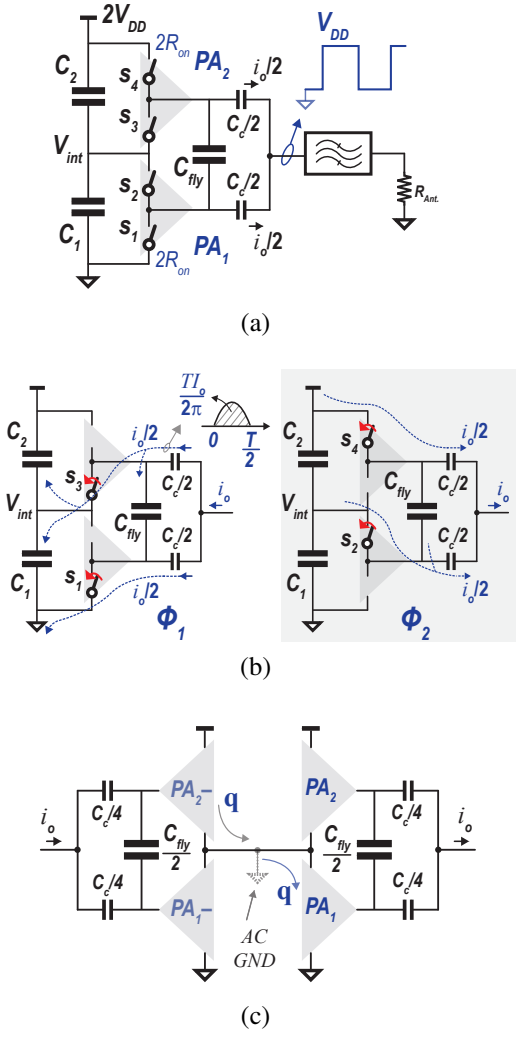


Figure 5.2: An example 2-stack PA operation from V_{in}=2V_{DD}. (a) Switch-level block diagram. (b) The resulted two switched networks of the HoC PA when the PM clock is high and low. (c) Differential operation for elimination of V_{int} capacitance.

decoupling capacitance are at a fixed voltage level relative to the ground, therefore do not result in parasitic switching losses. On the other hand, C_{fly} should be set such that $1/(\omega_o C_{fly}) < 2R_{on}$, where R_{on} is the total equivalent output resistance R_{out} of the PA, for phase-aligned AC operation.

The 2-stack differential PA topology provides three advantages for scaled CMOS technologies as compared to the representative class-G system when operating at 6dB back-off as illustrated in Fig. 5.1a. First, the proposed differential topology provides the required supply, $V_{int} = V_{DD}$, for 6dB back-off without any extra DC-DC converter. Even in a linear supply mod-

ulator, a large output decoupling capacitor C_d is required to enable a stable control loop with enough phase margin [81]. The stacking topology also enables powering the PA cells from a $2V_{DD}$ input without violating the employed thin-oxide switches breakdown voltage[1]. In addition, the stacked PA does not suffer from cascaded losses from a DC-DC converter in series with a PA as in conventional battery-connected CMOS PA approaches (e.g., the efficiency in Fig. 5.1a is $\eta = \eta_{DC\text{-}DC}\eta_{DC\text{-}AC}$). Instead, the efficiency of the 2-stack PA becomes $\eta = (1+R_{on}/R_L)^{-1}$ which approaches 100% instead of η bounded by 50% when a linear supply modulator is used. Secondly, the implicit high-efficiency switching DC-DC conversion implemented through stacking the two PA slices does not produce spurious output noise, even with the inherent 2:1 SC, where it operates at the carrier frequency f_o. On the other hand, most PAs operated from explicit DC-DC converters produce spurs at the fundamental switching frequency of the supply modulator and its harmonics. Passive filtering and postregulation through cascaded high power-supply-rejection-ratio (PSRR) linear regulators are required to circumvent the switching products from reaching the PA output, increasing cost and reducing efficiency of the overall class-G solution. Finally, by stacking 2 PA cells, the current drawn from the supply and ground grids is also reduced by a factor of 2 over the current drawn when PA cells are operated in parallel. This reduces the off-chip supply decoupling tree size and I^2ESR losses by 2 and 4 times, respectively.

The proposed implicit charge-recycling DC-DC conversion can be generalized to realize $2/\pi\, V_{DD}$ output voltage amplitude from $V_{in} = NV_{DD}$ using V_{DD}-rated thin-oxide devices. Instead of stepping the input battery voltage V_{in} down by N:1 through a lossy and bulky DC-DC converter, the proposed approach, as illustrated in Fig. 5.3, slices a nominal PA, with conductance G_{on} for a given output current driving capability i_o, into N PA cells, each with conductance G_{on}/N. Then, the approach *stacks* the N PA cells, each operating at the nominal process voltage V_{DD} while the entire stack is powered from NV_{DD}, such that the charge *discarded* by the top-most PA cell trickles down through the N-PA stack to be recycled at each level, achieving $\sim$ 100% DC-DC

[1] A startup circuit is required to ensure that the employed devices are not overstressed during power on. This is typically applied in high-voltage DC-DC converters via inrush current limiting circuitry.

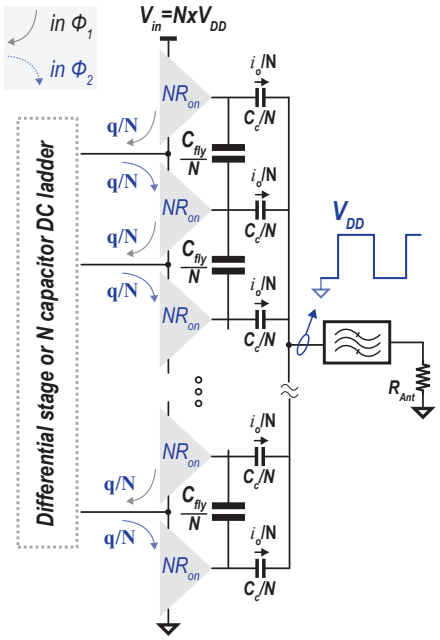
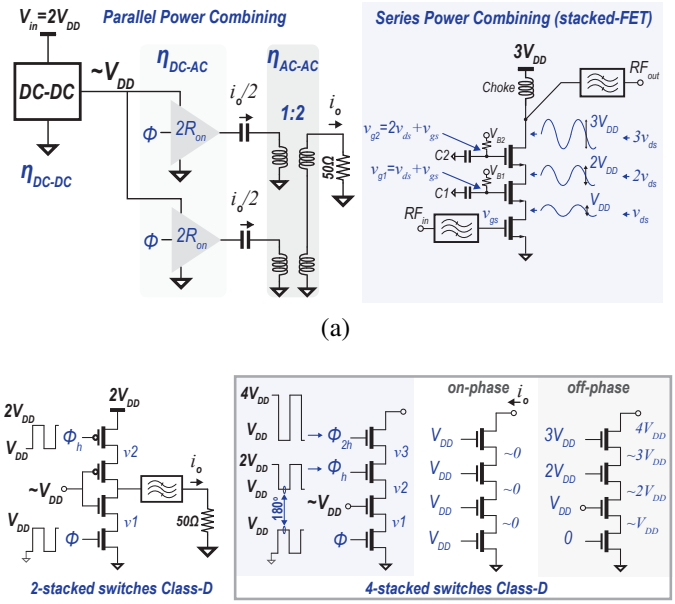


Figure 5.3: Implicit DC-DC conversion via charge-recycling. The same total DC capacitance, i.e. C_1+C_2 in Fig. 5.2, can be equally divided between the $N-1$ intermediate nodes for the same ripple amplitude as the 2-stack PA, in the case of a non-differential operation; similar explanation for C_{fly}.

efficiency. The $N-1$ flying-capacitor ladder is employed to enforce phase alignment among the stacked N PA cells and establish a properly-posed topology.

5.2.2 High-Voltage RF Signal Generation in Scaled CMOS without Magnetics

The low breakdown voltages available with deep submicron devices limit the allowed output voltage swings, and hence the achievable peak output power across a fixed load. To supply the high output power levels required by modern communication standards with thin-oxide devices, contemporary PA design schemes resort to impedance transformation networks [82, 83, 84, 85], power combining [71, 86, 72, 61], device stacking [87, 88, 62, 64], or an amalgamation of them. Figure 5.4 illustrates representative power combining and device stacking schemes, respectively. The parallel power combining schemes shown in Fig. 5.4a (left) achieves an output voltage



(a)

(b)

Figure 5.4: Prior schemes to realize high RF power using thin-oxide devices. (a) Parallel and series power combining schemes. (b) Digital device-stacked PAs.

amplitude of $4/\pi V_{DD}$ from $V_{in} = 2V_{DD}$ by placing two PA cells in parallel, powering them from a DC-DC converter outputting $\sim V_{DD}$, and having each amplifier feed a 1:1 transformer whose secondary winding is connected in series with the other PA secondary, achieving 1:2 impedance transformation. Unfortunately, on-chip transformers consume significant silicon area and suffer from high losses due to low-resistivity substrate and thin metal and dielectric layers in baseline CMOS [89, 85, 72].

An alternative means to generate high output power using thin-oxide devices is to perform series power combining by transistor stacking. Essentially, such schemes DC-connect transistors in series, while engineering the RF swing at the gate of each stacked transistor on top of the input common-source to ensure that all the transistors are operating in the safe region (i.e., without exceeding V_{GS} or V_{DS}/V_{DG} ratings), while producing high output amplitude (Fig. 5.4a, right), as in stacked-FET PA [64, 63, 62] and high-voltage/high-power (HiVP) [87, 90]. Unfortunately, such schemes typically require an array of input and output matching networks that occupy large area, degrade the overall PA efficiency, and generally limit the operational bandwidth. More

importantly, such schemes require post-fabrication trimming of the gate networks to ensure proper in-phase voltage swing at the gate and drain to avoid device breakdown. While differential topologies can create a virtual ac ground at the gate bias points, most demonstrated prototypes in prior-art assume external, up to N, ideal bias sources using lab equipment, while generating the required low-impedance high-fidelity bias voltage on chip, as in real products, is extremely challenging [91].

The stacked-transistor concept can be extended to a digital cascoded structure as illustrated in Fig. 5.4b. Stacking two devices practically requires an extra high-fidelity DC-DC source, as shown in Fig. 5.4b (left). Stacking more devices is challenging. For example, the upper two switches in a four stack cascode (Fig. 5.4b, right) have to be operated from level-shifted 180^o-phase square PM signals ϕ_h and ϕ_{2h} with V_{DD} and $3V_{DD}$ swings, respectively, in order not to violate the transistor oxide breakdown during the on-phase while not exceeding V_{DS} of V_{DD} in the off-phase. This requires perfect alignment, given the finite rise/fall times, between the PM input ϕ and the level-shifted and out-of-phase PM clocks ϕ_h and ϕ_{2h}, not to mention the complexity of generating a $3V_{DD}$ swing drive signal. Stacking N devices to realize NV_{DD}-rating cascoded switch requires $N-1$ high-fidelity biasing levels at nV_{DD} with progressively increasing gate swings, which significantly increases the cost of the solution.

To generate high RF voltages using only scaled thin-oxide CMOS transistors, a House-of-Cards topology is proposed that builds upon the stacked class-D concept presented earlier. An example 2-stack HoC is illustrated in Fig. 5.5. To achieve an amplitude of $4/\pi V_{DD}$, the supply and GND of a third PA cell, PA3, is switched with respect to the power source V_{in} rails through PA2 and PA1 switches, respectively, to provide voltage addition of the initial (PA1, PA2) ladder and PA3 outputs. The proposed topology essentially arranges the comprising PA cells in a HoC topology, where PA3 acts as a "flying-domain" [92]. During ϕ_1 (ϕ_2), in Fig. 5.5b, the odd (even) numbered switches are on, and hence R_L is connected to GND (V_{in}).

The equivalent output resistance, R_{out}, of such a PA is $2R_{on}$, where R_{on} is the on-resistance

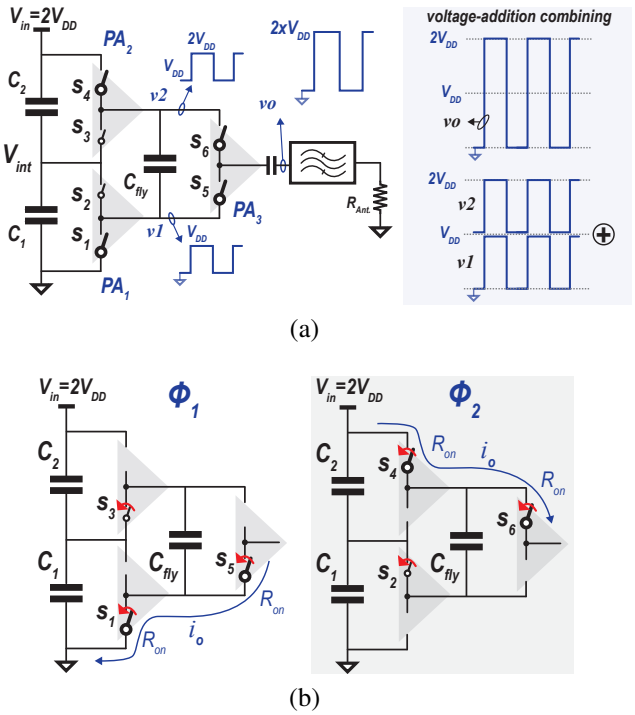


Figure 5.5: An example 2-stack HoC PA (a). Resulted phases when ϕ is high and low (b).

of the switches s_1, s_5, s_4, and s_6. The charge delivered to the output load R_L does not pass through the inner switches s_2 and s_3, which are only used to balance capacitors C_1 and C_2 using C_{fly} during transients. As a result, switches s_2 and s_3 can be made of minimal size. Essentially, switches (s_1, s_4) and (s_5, s_6) form two class-D PA cells connected in cascade, where both handle the total output current, i_o, and are therefore termed AC PA cells. Through (s_2, s_3), i.e. the DC PA cell, v_1 and v_2, are never left floating unlike what would occur in a conventional cascoded switcher, and hence the proposed HoC guarantees reliable operation without exceeding any device voltage rating, all in a self-contained solution without any bias circuitry or added complexity.

The proposed HoC topology can be generalized to simultaneously realize a 1:N voltage step up ratio and N PA power combining. The proposed topology realizes NV_{DD} swing from N AC V_{DD}-rated PA cells by flying an entire $N-i$-stacked-PA ladder through the switches of a prior $N-i+1$-stacked-PA with the $N-i$-ladder input gates clamped to the intermediate nodes of the prior ladder, recursively, until the resulted lower-stack PA is a single PA cell, as shown in Fig.

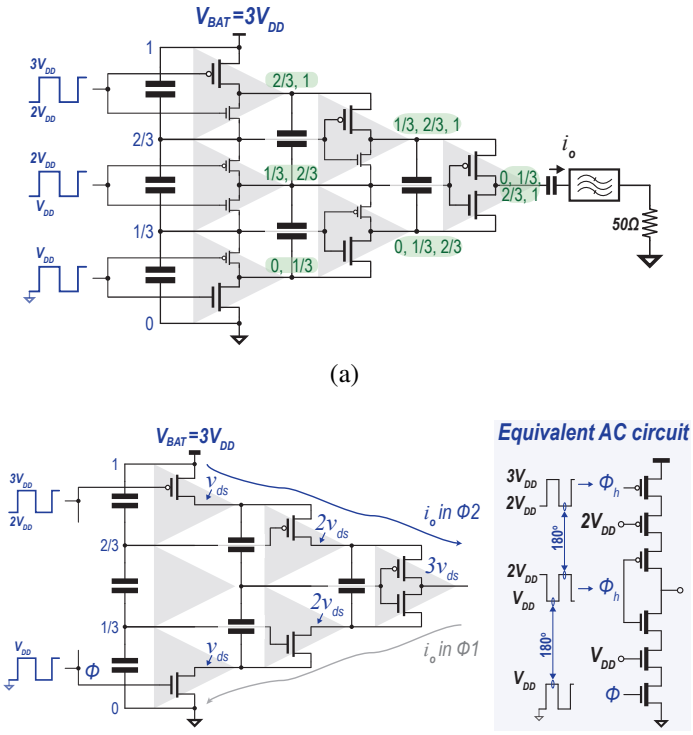
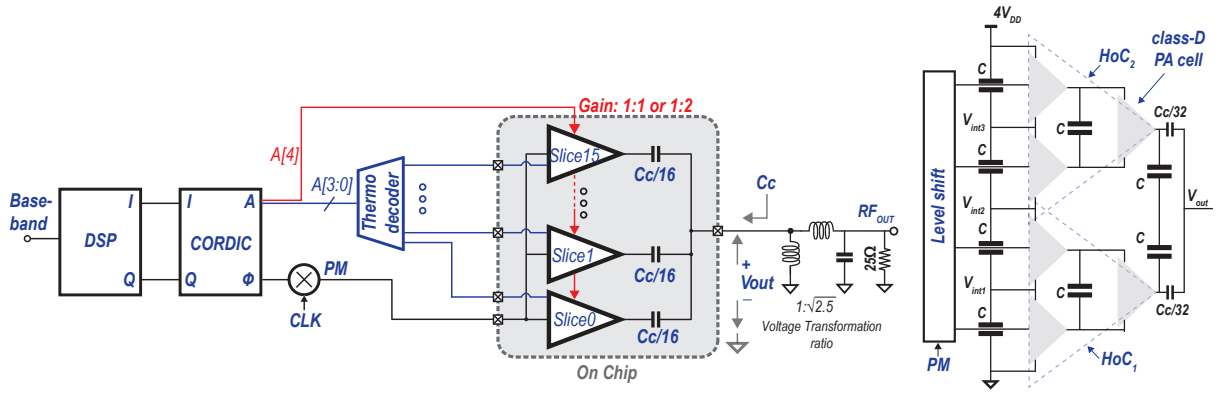


Figure 5.6: An example 3-stack HoC PA (a). Fundamental AC PA cells and their gate/drain voltages to enable aligned safe operation through the clamping capacitors while performing series power combining (b).

5.6a. The commutation of the switches permits the addition of the voltage swings of the N AC PA cells (i.e. voltage-domain combining). In addition, each flying PA-ladder provides automatic DC voltage balancing of the stacked domains of the prior ladder. Each clamping capacitor, DC or flying, is automatically balanced to $\sim V_{DD}$ at steady state. With the proposed gate connection, the cascaded PA-ladders, in Fig. 5.6a, are switched in a domino falling fashion with the annotated transient states of the intermediate nodes. As a result, the voltage swing at the gate and drain of each switch is perfectly aligned through the clamping capacitors to guarantee safe operation in a robust digital manner (Fig. 5.6b).



(a)

Figure 5.7: (a) Block diagram of a single ended HoC, actual implementation is differential. (b) Top-level schematic of an HoC Slice of the 16 slices, actual slice is differential.

5.3 Recursive HoC Amplifier Architecture

5.3.1 HoC Digital Power Amplifier Linearization

Among various digital linearization techniques [69, 68, 66, 67, 70, 93], the SC PA architecture [73, 74] has superior efficiency and linearity. A similar approach is followed in this work to linearize the non-linear HoC PA. Figure 5.7a illustrates the block diagram of the implemented 2-stack by 2-cascade recursive HoC power amplifier powered directly at V_{in}=4.8V using V_{DD}=1.2V thin-oxide transistors in 65nm. The input baseband signal is oversampled and raised-cosine filtered using a DSP to generate the in-phase (I) and quadrature (Q) signals. Using a CORDIC algorithm, the digital I and Q signals are converted into a 5-bit envelope (A[4:0]) and phase (ϕ) component. A square carrier at f_o is phase modulated by the produced phase signal through a mixer.

The generated PM clock is used to drive 16 PA slices, each sized to have conductance $G_{on}/16$, and each implementing a 2-stack 2-cascade HoC PA. As shown in Fig. 5.7b, six $V_{DD}-$rated class D PA cells are used to implement each HoC slice. Three class-D cells are arranged in a 2-cascade HoC topology to establish two $2V_{DD}$ swing PAs: HoC1 and HoC2, which

are then stacked on top of each other to block a V_{in} of $4V_{DD}$. The 16 PA slices share the same intermediate DC nodes (V_{int1}, V_{int2}, and V_{int3}), while the output of each 2-cascade HoC PA of the 32 (i.e., 16 slices, two 2-cascade HoC PAs each) is coupled to the output V_{out} through a $C_c/32$ capacitor.

Based on the required envelope amplitude, the 16 HoC slices are selectively enabled through the thermometer decoder to switch the bottom plates of a unary-sized MIM capacitor array, whose total capacitance is C_c=25pF, at f_o and a voltage swing of $2V_{DD}$. The bit $A[4]$ is employed to set the gain value of each HoC slice to one of two possible values, as will be discussed later in this section. At peak power, all HoC slices switch, while slices are gradually deactivated at backoff by connecting the bottom-plate of their C_c/32 capacitors to GND and $2V_{DD}$. A decoder is used to activate each of the HoC slices according to the envelope code, which is fetched at the desired sample rate to reconstruct the non-constant envelope RF output. An output inductive band-pass filter is used to resonate with C_c and establishes an LC impedance transformation network. As shown in Fig. 5.7a, in total two-stage LC impedance transformation network is employed to transform the 25Ω load resistance (50Ω antenna through a balun) to 10Ω (i.e. impedance transformation 1:2.5) to generate the desired 23dBm total output power. Thus, each LC matching stage should provide$\sqrt{2.5}$ of impedance transformation ratio for maximum bandwidth. However, the first LC stage is designed to provide an impedance transformation ratio of $\sim$1.8, which is a little larger than$\sqrt{2.5}$ for lower charge-sharing loss while maintaining reasonable bandwidth, as will be discussed. Therefore, the required loaded quality Q_l of the first LC matching stage is $\sim$0.88, which sets the value of C_c as 25pF at 0.72GHz for white space mobile market.

Modulating the output amplitude by controlling the number of actively switching PA slices essentially resembles a controllable capacitive voltage divider to a constant-envelope $2V_{DD}$ square wave, as shown in Fig. 5.8. Here, K is the number of unary-sized slices to enable $log_2(K)-$bit envelope resolution. As the envelope code, i, is increased, more capacitors are switched between

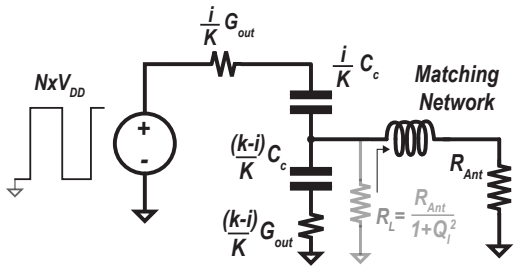


Figure 5.8: Equivalent circuit of the implemented Switched-Capacitor HoC PA.

GND and $2V_{DD}$ through an iG_{on}/k conductive path, while $K-i$ capacitors are statically pulled down through a $(K-i)G_{on}/K$ path. Since the input port of the employed matching network is inductive, the matching can be consider as high-impedance during the fast transition of the input square signal. Therefore, the output voltage V_{out} is determined by the voltage divider in Fig. 5.8 as:

$$V_{out} = \frac{2}{\pi}\frac{i}{K}2\times V_{DD}. \tag{5.1}$$

As readily seen, the series combination of the capacitor array $i(K-i)/K^2\ C_c$ must be charged and discharged once per the RF cycle, thus the array charge sharing loss P_{cs} is:

$$P_{cs} = \frac{i(K-i)}{K^2}C_c\,(2\times V_{DD})^2 f_o. \tag{5.2}$$

By employing a series inductive reactance, the series capacitive reactance $1/(\omega_o C_c)$ can be cancelled at f_o, thereby enabling a significant reduction in the employed C_c to an extent dependent on the unloaded quality of the employed inductor, Q_{ind}. Through a larger inductance L at a given R_L, a higher loaded quality factor $Q_l = \omega_o L/R_L = 1/(\omega_o C R_L)$ can be realized. This results in a smaller array capacitance, and hence the P_{cs} can be reduced, as demonstrated in [73]:

$$\eta_{drain} = \left(1+\frac{\pi}{4}\frac{(K-i)}{i}\frac{1}{Q_l}\right)^{-1}. \tag{5.3}$$

Figure 5.9 shows the drain efficiency of a SC PA with an array size of 32 unit capacitors.

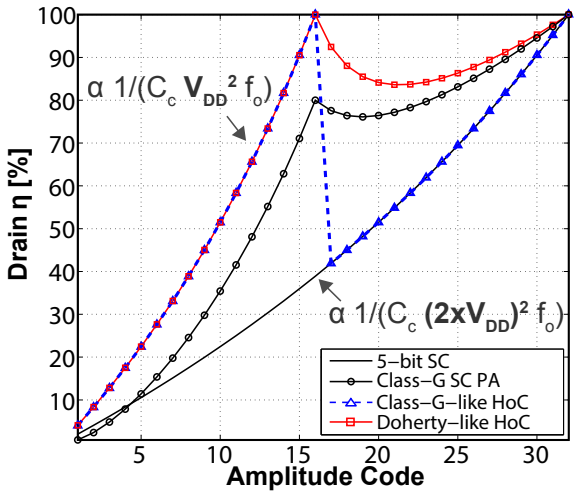
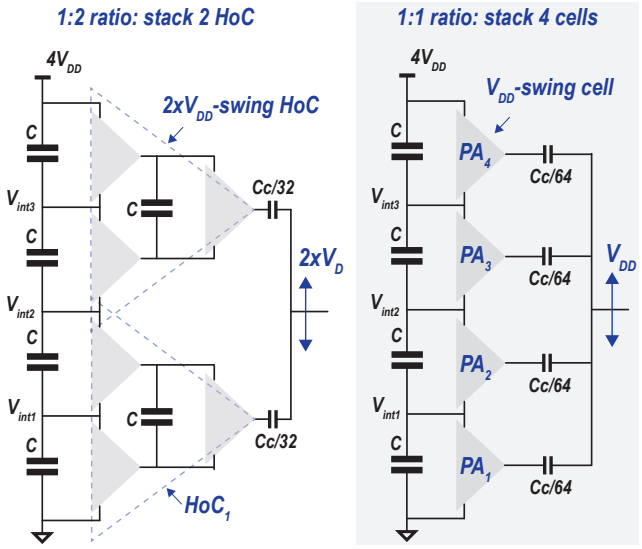


Figure 5.9: Drain efficiency of a 5-bit SC PA and a class-G-like HoC. Comparison of the drain efficiency of the proposed Doherty-like HoC (5.5) and a conventional 5-bit SC PA with two supplies V_{DD} and $2V_{DD}$ (5.6), all at Q_l of 0.5.

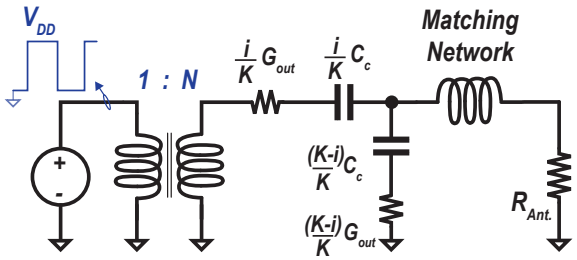
As shown, with a reasonable on-chip Q_{ind} of 10-15, the SC PA efficiency falls by 60% at 6dB back-off. Techniques are thus required to enhance efficiency at back-off.

5.3.2 Voltage-Mode Magnetic-less Swapping Doherty for High Average Efficiency

To realize high efficiency at back-off in a fully-integrated, magnetic-less, and reconfigurable approach, the proposed PA can reconfigure each PA slice, containing two stacked HoC cells (HoC1 and HoC2 in Fig. 5.10a (left)) with $2V_{DD}$ output swings, into a stack of four class-D PA cells whose outputs are capacitively coupled to provide V_{DD} output swings. In this manner, the charge-sharing losses of the capacitor array, P_{cs} in (5.2), can be scaled by the same factor as the output power at 6dB back-off (i.e., four times), and hence the HoC PA realizes a second efficiency peak at 6dB back-off that matches the peak P_{out} efficiency, as illustrated in Fig. 5.9 (class-G-like HoC). Since the overall PA supply voltage, $V_{in} = 4V_{DD}$ is not changed, the reconfigurable HoC amplifier can be considered as a solid-state RF impedance transformer that achieves two voltage



(a)



(b)

Figure 5.10: Reconfiguring the HoC slice transformation ratio from 1:2 to 1:1 to achieve high-efficiency at back-off (a). Simplified equivalent circuit (b).

transformation ratios, 1:2 and 1:1, as in Fig. 5.10b. The available two transformation ratios boost the achievable resolution by a one-bit, and thus $0 \leq i \leq 2K$.

The MSB of the envelope code, $A[4]$ in Fig. 5.7a, is used to set the transformer ratio. The remaining four least significant bits, $A[3:0]$, are used to enable fine-grain amplitude resolution. There are two ways to accomplish fine-grain amplitude modulation: Class-G-like and Doherty-like, which differ in how to utilize the inactive slices.

Class-G-like HoC back-off

At the 1:2 transformation ratio (i.e., $A[4] = 1$), $A[3:0]$ can be employed through the decoder in Fig. 5.7a to adapt the number of actively switching slices with $2V_{DD}$ swings, $i-K$, while the remaining $2K-i$ slices (where $K \leq i \leq 2K$) are statically connected low. In this case, the drain efficiency is similar to (5.3) but replacing K with $2K$. As shown in Fig. 5.9 ("Class-G-like HoC"), the HoC suffers from a discontinuous efficiency profile near the transition point in between the two transformation ratios, since all the capacitors C_c in the HoC array are switched through V_{DD} input voltage swing to produce the -6dB back-off amplitude value and therefore the PA efficiency jumps suddenly at the -6dB code to the ideal 100% value. This resembles the operation of a conventional class-G PA that operates through a 100%-efficient DC-DC converter to produce the -6dB $V_{in}/2$ supply.

Doherty-like HoC back-off

To improve efficiency at back-off, when $A[4] = 1$ the $2K-i$ inactive slices instead switch the bottom-plate of their coupling capacitors with a swing of V_{DD} rather than being static. Essentially, the input signal is amplified through two voltage-mode power amplifier paths, a *main* amplifier path with $V_{DD}-$swing and a *peaking* amplifier path with $2V_{DD}-$swing, as shown in Fig. 5.11a. The two paths are simply combined through a programmable capacitive voltage-divider network to generate amplitudes between V_{DD} and $2V_{DD}$, according to $A[3:0]$, and hence the output voltage becomes

$$V_o = \frac{2}{\pi}\left(\frac{i-K}{K}\,2\times V_{DD} + \frac{(2K-i)}{K}V_{DD}\right), \tag{5.4}$$

for $K \leq i \leq 2K$. This way, the K-capacitor array is charged and discharged through only the amplitude difference between the two amplifiers, i.e. V_{DD}, instead of $2V_{DD}$ in the old code, reducing the charge sharing losses by $4\times$, and enhancing the efficiency profile between the two ratios to exactly follow a Doherty back-off profile.

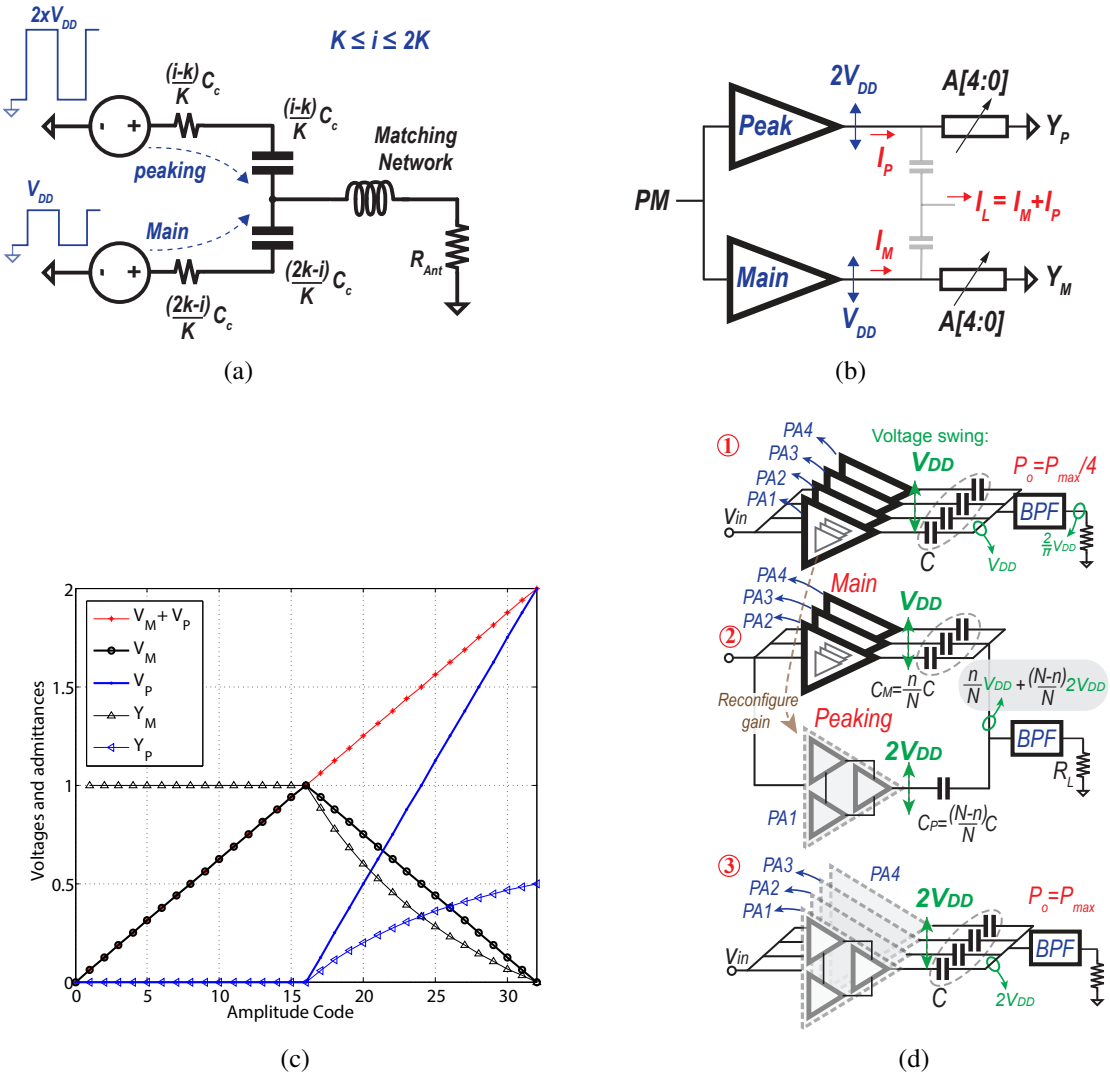


Figure 5.11: Equivalent circuit of the HoC while generating amplitudes between the two transformations ratios (a). Load-pull characteristics of the HoC for $K \leq i \leq 2K$ (b). Normalized voltages and admittances of the *main* and *peaking* amplifiers (c). (d) Swapping Doherty illustration.

The operation, to a great extent, is similar to the 2-way Doherty configuration, where capacitive load-pull of the *main* amplifier occurs. Rather than treating the two amplifiers in the 2-way Doherty as current sources, the main and peaking amplifiers are employed as voltage sources of different amplitude levels $V_M = (2K-i)/K \times V_{DD}$ and $V_P = (i-K)/K \times 2V_{DD}$, respectively. In the proposed voltage-domain combining, the load admittance, rather than impedance in current-mode Doherty, is gradually lowered once the auxiliary amplifier is on, as in Fig. 5.11b and

Fig. 5.11c. Unlike the classical Doherty implementations that disable the peaking amplifier at back-off, wasting silicon area, a "swapping Doherty" architecture is used where at back-off the peaking amplifier slices are reconfigured (i.e. swapped) to act as the main amplifier, realizing 100% resource utilization, as in Fig. 5.11d. The efficiency under such operation becomes

$$\eta_{drain|Doherty} = \left(1 + \frac{\pi}{4}\frac{(i-K)(2K-i)}{i^2}\frac{1}{Q_l}\right)^{-1}, \tag{5.5}$$

for $K \leq i \leq 2K$. To the best of our knowledge, the continuous efficiency transition through the second amplitude coding scheme was first noted in [74] in a class-G SC PA.

It is important to note that, the conventional class-G PA with multiple supplies can not achieve the efficiency profile of the Doherty configuration even with the discussed Doherty amplitude coding. This is since the secondary efficiency peak at 6dB back-off is reduced by the cascaded losses of the back-off DC-DC converter. By adding the normalized loss incurred for supplying the power of the *main* PA, the efficiency of such approach can be given by:

$$\eta_{drain} = \left(1 + \frac{K(2K-i)}{i^2}\left(\frac{1}{\eta_{DC-DC}} - 1\right) + \frac{\pi}{4}\frac{(i-K)(2K-i)}{i^2}\frac{1}{Q_l}\right)^{-1}. \tag{5.6}$$

On the other hand, through the implicit 100% DC-DC conversion, the HoC topology can realize the exact 2-way Doherty efficiency profile, as shown in Fig. 5.9, without any bulky transformer or an extra DC-DC converter.

5.3.3 Stacked-FET AM-AM and AM-PM Distortion

Unlike typical digital-to-analog (DAC) converters in mixed-signal applications, the SC RF-DAC [73] provides high output power levels, and hence requires large switches to achieve small equivalent on-state resistances. Unfortunately, the switches' gate and drain parasitic capacitance are linearly proportional to the switch width. Consequently, the minimum loss point between

the conduction and switching components is such that the switches' on-conductance i/KG_{on} is comparable to the series reactance of the capacitors $j\omega_o i/KC_c$ of the employed DAC. Therefore, not only the capacitor mismatch but, more importantly, the switch on-resistance mismatch affect the RF-DAC linearity. It is important to note that while it is relatively easy to realize capacitors' size matching within 1% accuracy in CMOS technologies, it is hard to control the transistors' on-resistance ratios and hence the DAC non-linearity is dominated by the switches' matching.

The effect of the on-resistance mismatch between the constituent switches on the DAC linearity including the code-dependent AM-AM and AM-PM distortions can be evaluated from the equivalent circuit in Fig. 5.8. As previously discussed, to realize the i^{th} code amplitude, i capacitors are switched between GND and NV_{DD} through the equivalent output conductance G_{out} of the actively switching i HoC PA slices $i/K \times G_{on}$. On the other hand, $K-i$ capacitors are statically held down through $K-i$ NMOS switches $(K-i)/K \times G_{on}$. Each switching PA slice comprises a pull-up PMOS and a pull-down NMOS paths of equivalent on-resistance of R_p and R_n, respectively. Therefore, for a 50% duty cycle input, the equivalent PA slice output resistance is essentially the average of each resistance, (R_p+R_n)/2. If perfect on-resistance matching between the PMOS and NMOS switches is realized, i.e. $R_p = R_n = R$, neither AM-AM nor AM-PM distortion would result, assuming zero capacitor mismatch. Unfortunately, such matching is almost impossible to realize which results in voltage-division ratio mismatch between the equivalent output conductance of the actively switching PA slices $i/K \times G_{on}$ and the statically enabled NMOS pull-down switches $(K-i)/K \times G_{on}$. Consequently, the amplitude-code i dependent AM-AM and AM-PM distortions result.

Assuming perfect matching between the comprising capacitors, the worst-case (peak) AM-AM and AM-PM distortion at each envelope code i due to the on-resistance mismatch can be evaluated by assuming each PMOS switch in the PA takes on the maximum possible on-resistance deviation, e.g. $\mp 6\sigma_{RP}$, while each NMOS switch approaches the opposite on-resistance extreme variation, e.g. $\pm 6\sigma_{RN}$, simultaneously, under a Gaussian distribution of the on-resistance. Thus,

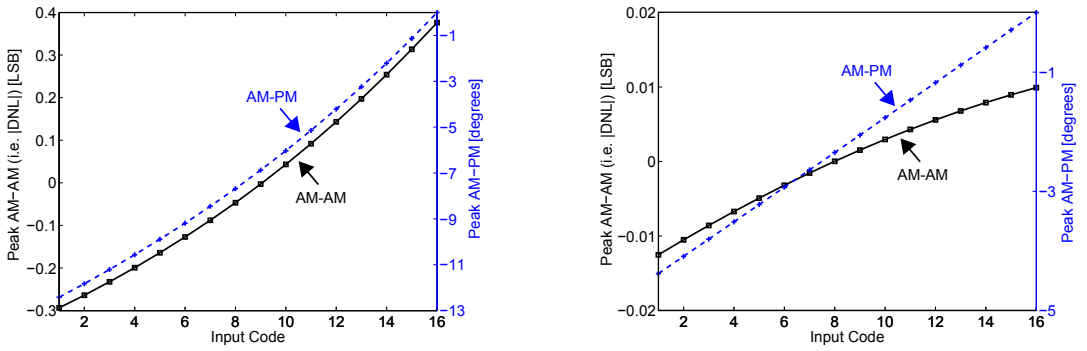


Figure 5.12: Maximum distortion value due to on-resistance mismatch in a 4-bit DAC (a) with a total conductance G_{on} of $0.1\Omega^{-1}$ and (b) with G_{on} of $1\Omega^{-1}$. Total C_c = 25pF and f_o = 1GHz.

the upper-bound on the resulted AM-AM and AM-PM distortion at each i can be evaluated analytically through the output amplitude produced through the capacitive divider network in Fig. 5.8 with the new on-resistance values. In that case, the equivalent output resistance of the actively switching PA slices becomes $i/K \times G_{on} - 1/(6\sigma_R)$, assuming the PMOS and the NMOS switches in each actively switching PA slice deviates in the same direction by $6\sigma_R$ for worst-case calculation, while the static pull-down NMOS switches approaches $(K-i)/K \times G_{on} + 1/(6\sigma_R)$, where $\sigma_{RP} = \sigma_{RN}$ for simplicity.

Figure 5.12 illustrates the calculated peak value of the resulted AM-AM and AM-PM at each amplitude code i for a $6\sigma_R$ of $25\%R$, under different values of total PA conductance G_{on}. The analytical expression derived through the capacitive voltage divider in Fig. 5.8 for the output voltage amplitude provides AM-AM and AM-PM distortion values within 10% of the schematic simulation results. As shown in Fig. 5.12, the maximum AM-AM distortion occurs at $i = 1$ and the peak code $i = 16$, where the switch on-resistance deviation is manifested in the voltage-divider expression, in either case. When the total PA conductance G_{on} is increased 10 times, the maximum AM-AM and AM-PM distortions are reduced by 37.6 times and 2.8 times, respectively. Thus, wider PA switches not only enhance the PA drain efficiency, but also improve the PA AM-AM distortion. Since the PA exhibits a mild second order nonlinearity in

amplitude and phase, a digital predistortion can be easily employed to realize higher linearity. It is important to note that if the opposite on-resistance deviation polarity is instead assumed, i.e. $i/K \times G_{on} + 1/(6\sigma_R)$ and $(K-i)/K \times G_{on} - 1/(6\sigma_R)$ in Fig. 5.8, the illustrated AM-AM and AM-PM nonlinearities in Fig. 5.12 will tilt with the opposite "negative" slope versus the amplitude code i.

On the other hand, N times FET-stacking in the proposed PA architecture results in N times larger standard deviation σ_R of the implemented switches' on-resistance under random local variations. As a result, the AM-AM and AM-PM distortions are exacerbated by more than N times, according to the model, with device stacking. Fortunately, the proposed PA not only employs unary decoded architecture but more importantly relies on multiple solid-state transformer ratios to realize higher amplitude resolutions, instead of increasing the conductance and capacitance segmentation of the employed DAC which comes at increased standard deviation in the conductance or capacitance step LSB size.

5.3.4 Recursive HoC Slice Architecture

The proposed PA architecture requires dynamic reconfiguration of individual slices between ratios to achieve Doherty-like back-off. It can be challenging to reconfigure without exceeding device ratings or wasting area, all while maintaining the same R_{out} across all reconfiguration states to avoid AM-AM distortion. Perhaps the most straightforward solution would be to implement two parallel HoC amplifiers, each configured for the 1:1 and 1:2 ratios, respectively, and enable or disable one or the other to realize each ratio as in Fig. 5.10a. However, two main drawbacks come with this approach. First, the V_{DS} device rating of the disabled amplifier can be exceeded through the high voltage output amplitude coupled through the output-side capacitor, as shown in Fig. 5.13. Furthermore, the disabled switches act as diode-connected devices, and hence loading the peaks and valleys of the output amplitude, establishing a non-linear loading and compromising the linearity. Secondly, disabling one of the amplifiers wastes almost half of

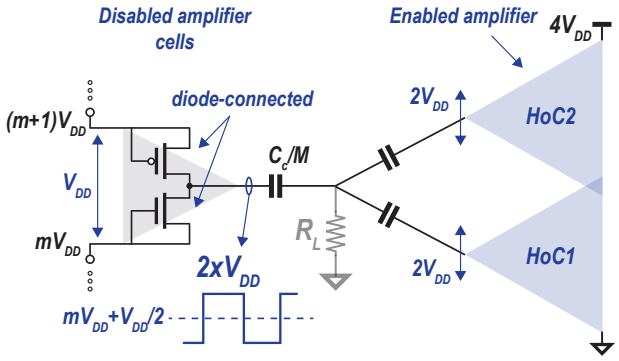


Figure 5.13: Loading of a disabled PA cell resulting in potential device voltage rating violations.

the silicon area.

To realize the high-efficiency at back-off while maintaining high linearity, a recursive reconfiguration approach is chosen in this work. Figure 5.14 illustrates the switch diagram of the implemented slice architecture used to realize the two reconfigurable transformation ratios, 1:1 and 1:2. Although six $V_{DD}-$rated class D PA cells are only technically necessary to implement each 2-stack 2-cascade HoC slice in Fig. 5.7a, twelve cells are used to permit recursive reconfiguration with fixed R_{out}, without exceeding the device ratings, and without disabling or wasting silicon area. Each recursive HoC slice is implemented through two parallel 2-stack 2-cascade HoC ladders. The intermediate nodes V_{int1}, V_{int2}, and V_{int3} are tied together in the two parallel 2-stack 2-cascade HoC ladders, while the output of each of the four 2-cascade HoC PAs is coupled to V_{out} via $C_c/64$ capacitors.

Each 2-cascade HoC comprises six switches. Each AC switch is assigned $G_{on}/2$ to realize an overall R_{out} of R_{on}. The DC switch of the two available is allocated $G_{on}/8$, as discussed previously. The four switches $s3_1$, $s3_3$, $s2_2$, $s2_4$ includes an extra helper switch, sized to be $3G_{on}/8$, to enable fixed R_{out} value across both ratios. In the 1:2 transformation ratio, all the switches are operated from the input PM clocks while the helper switches are disabled. In the 1:1 ratios, switches $s1_1$ and $s3_1$ in HoC1 are statically turned on, while $s5_1$ and $s6_1$ are operated through the PM clock, to connect the class-D PA1 permanently between GND and V_{int1}. By enabling the helper switch within $s3_1$, a fixed R_{out} (equal to R_{on}) can be realized across both 1:2

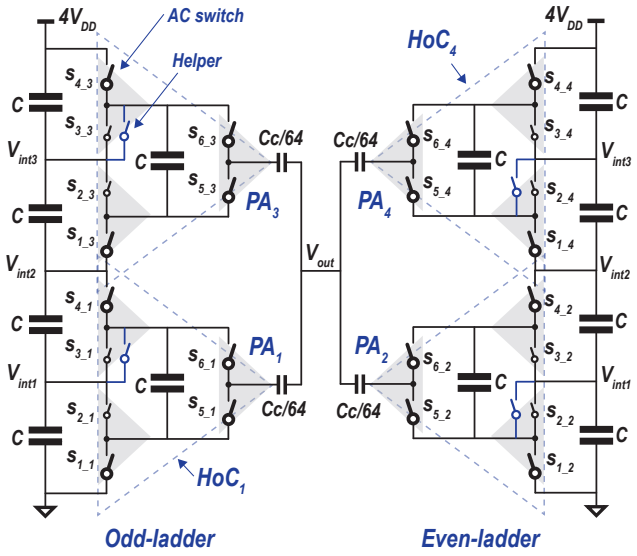


Figure 5.14: Recursive architecture of an HoC slice. The output-side stacked two DC capacitors in Fig. 5.7b are not shown for clarity.

to 1:1 ratios. Similarly, the switches ($s1_3$, $s3_3$) in HoC3, ($s2_2$, $s4_2$) in HoC2, and ($s2_4$, $s4_4$) in HoC4 are used to permanently connect PA3, PA2, PA4 at ($V_{int}2$, $V_{int}3$), ($V_{int}1$, $V_{int}2$), and ($V_{int}3$, V_{in}), respectively. This way the four $V_{DD}-$swing PA cells PA1, PA2, PA3, and PA4 are stacked on top of each other, as desired by Fig. 5.10a, while operated from V_{BAT} to enable high-efficiency at 6dB back-off.

5.4 Circuit Implementation

5.4.1 Reconfigurable Class-D PA Cell Design

The 12 class-D PA cells used to implemented an HoC slice in Fig. 5.14 are divided into three categories based on the required digital conductance programability: nominal, segmented pull-up, and segmented pull-down. The segmented configurations include an additional pull-up/down helper switch over the nominal cell. Figure 5.15a illustrates the schematic implementation of an example segmented pull-down class-D cell. The other cell configurations can be realized in a similar way. In Fig. 5.15a, a two non-overlapping clocks, ϕ_1 and ϕ_2, are generated

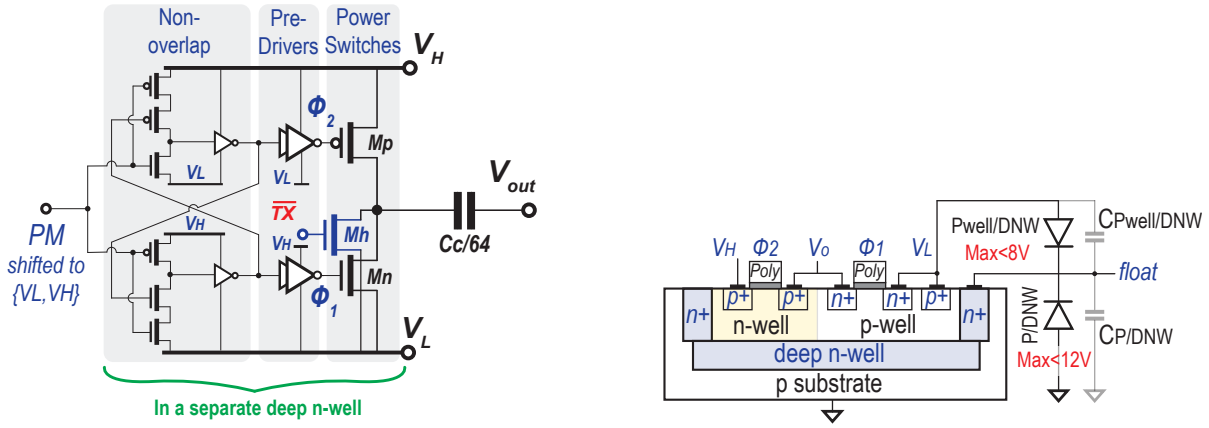


Figure 5.15: Reconfigurable class-D PA generic cell schematic (a). Placing each PA cell in a separate deep n-well (b). Floating connection enables 2× reduction in bottom-parasitics unlike the required high bias resistance used in [1].

from the received level-shifted PM signal through three-transistor inverters [92] with feedback from the opposite phase to realize minimal dead-time and eliminate any shoot-through current. Clocks ϕ_1 and ϕ_2 are provided through a cascaded chain of buffers to drive the gate capacitance of the NMOS M_n and PMOS M_p switches.

The PA conduction RMS loss stems from the load current flow through the switches' on-resistance, and hence the PA equivalent R_{out}. The second key loss component of the PA originates from the charging and discharging of the parasitic capacitance, once per the RF cycle, of the constituent power switches, which includes the gate, drain, and body parasitics; and the capacitors' top and bottom parasitics. Therefore, the total PA loss is set by:

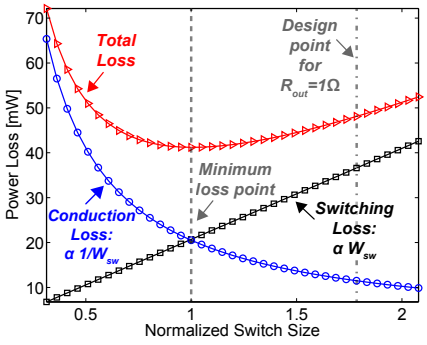
$$P_{loss} = P_{RMS} + P_{switching-transistor} + P_{switching-cap}. \tag{5.7}$$

In order to realize the maximum possible PA power-added efficiency at a given carrier frequency f_o, input voltage V_{in}, optimum resistance R_L, and for a given technology, the total PA loss P_{loss} must be minimized. Figure 5.16a shows the optimization plots of the simulated PA conduction and switching loss components associated with the PA switches, including capacitors' parasitic

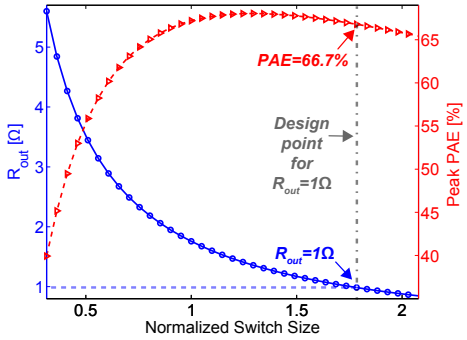
switching loss, versus the switch size in low-power 65nm CMOS. While a wider switch results in a smaller conduction loss P_{RMS}, it comes at a higher switching parasitic losses, and hence an optimal switch width can be found when both loss components are matched (Fig. 5.16a). However, as shown in Fig. 5.16b, the selected switch size for this design is almost 1.8 times the optimal point size. This is in order to realize an overall R_{out} of 1Ω for a single-ended amplifier at 65^oC to enable the PA to deliver above 23dBm of total P_{out} to the load $R_L \approx 10\Omega$ (after a small amount of impedance transformation per Fig. 5.7a) and to achieve superior linearity, given the dominance of the on-resistance mismatch on the PA distortion, as previously discussed. Thus, the selected switch sizes are 16μm for NMOS and 41.6μm for PMOS in an AC class-D cell of a matched NMOS and PMOS on-resistance. Figure 5.16c illustrates the schematic-simulated peak-amplitude PAE under the optimal switch sizing, of matched conduction and switching losses, versus f_o for an optimum R_L of 10Ω. As shown, using the employed low-power 65nm transistors of increased threshold voltage (and hence higher on-resistance) for low leakage, the peak PAE degrades with higher f_o and reaches 44% at f_o=3GHz on schematic simulations. This suggests about 24% after accounting for layout parasitics, the on/off-chip ESR, and the losses in the load transformation network as well as the employed balun including the amplitude/phase imbalance effects. Furthermore, the PA peak P_{out} gets lower as f_o is increased since the optimal switch size, in Fig. 5.16c, is reduced to realize lower parasitic switching losses.

The power switches dis/charge the top-plate of each cell's coupling capacitor, C_c, implemented between M8/M7 with a 2fF/μm^2 MIM capacitor. This way the bottom-plate capacitance is tuned out through the inductive bandpass filter, rather than being hard dis/charged through the PA cell. MIM capacitors instead of the denser MOS are used for C_c for their higher precision/linearity and, importantly, their high voltage rating of 10V. The helper transistor, M_h, is applied as a static switch through the transformation ratio control bit TX, level-shifted to the corresponding stacked-domain.

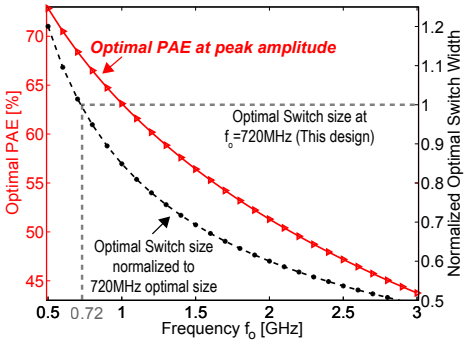
With process scaling, the substrate/drain diode's breakdown voltage gets lower. Stacking



(a)



(b)



(c)

Figure 5.16: Simulated overall loss optimization plots. (a) Conduction and switching loss components at f_o=720MHz. (b) Peak-amplitude PAE and R_{out} versus switch size at f_o = 720MHz. (c) Optimal peak-amplitude PAE versus f_o.

NMOS devices with their body tied to the p-substrate would cause the topmost NMOS in the stack to block a large drain-to-body voltage (e.g., V_{DB} of 4.8V), exceeding the breakdown voltage in deep-submicron CMOS. The implemented class-D cell is instead isolated in a separate deep-nwell

(DNW) as in Fig. 5.15b so that the substrate p/DNW diode (which has a breakdown voltage on the order of 12V) blocks the large output voltage instead of the NMOS substrate p/n+ diode. This enables stacking up to twelve class-D PA cells for a 12V maximum output voltage swing. Furthermore, this ensures fixed threshold-voltage V_{th} of the used switches during operation to ensure constant conductance and minimum distortion. To reduce switching losses, the DNW is left floating while the inner p-well is shorted to its respective flying ground to prevent latch-up. As shown in Fig. 5.15b, this effectively places the parasitic capacitors of the p/DNW and the p-well/DNW diodes in series, reducing the bottom-plate well parasitics by a factor of $\sim$2. The cell clamping capacitance (C in Fig. 5.14) is implemented in the same DNW using a thin-oxide PMOS transistor with 12.5fF/μm^2 of density and a breakdown voltage of 1.5V. The non-linearity of such capacitance does not affect the topologically-defined steady-state DC voltage across each 1.2V cell. Each cell comprises 0.6pF ($\sim$ 7.8Ω ESR at 65^{o}C) of clamping capacitance to enable automatic voltage balancing against non-fully differential signals and to provide proper decoupling for the gate drivers of the power switches. The total required clamping capacitance is 230.4pF in the present differential implementation.

5.4.2 Interfacing Level Shifters

Besides the TX signal that controls the helper switch in a static manner, an extra bit EN is employed to clock gate (i.e. PM gate) the whole HoC slice to statically hold the slice coupling capacitor low. Therefore, each recursive HoC slice in Fig. 5.14 receives two gain setting bits (EN, TX) to establish three gain states: statically holding C_c down (0, 0), switching with V_{DD} swing (1, 0), and switching with $2V_{DD}$ swing (1, 1). This requires shifting the voltage levels of the input PM clock and the enable signal of the helper switch TX to the appropriate levels needed by all twelve PA cells. Figure 5.17a shows the proposed Dickson shifter to achieve that. A fork-based clock tree is established through the depicted Dickson capacitor connection (C_{sh} = 35fF using MIM) to distribute balanced in-phase PM signals to the initial four stacked domains in each HoC ladder.

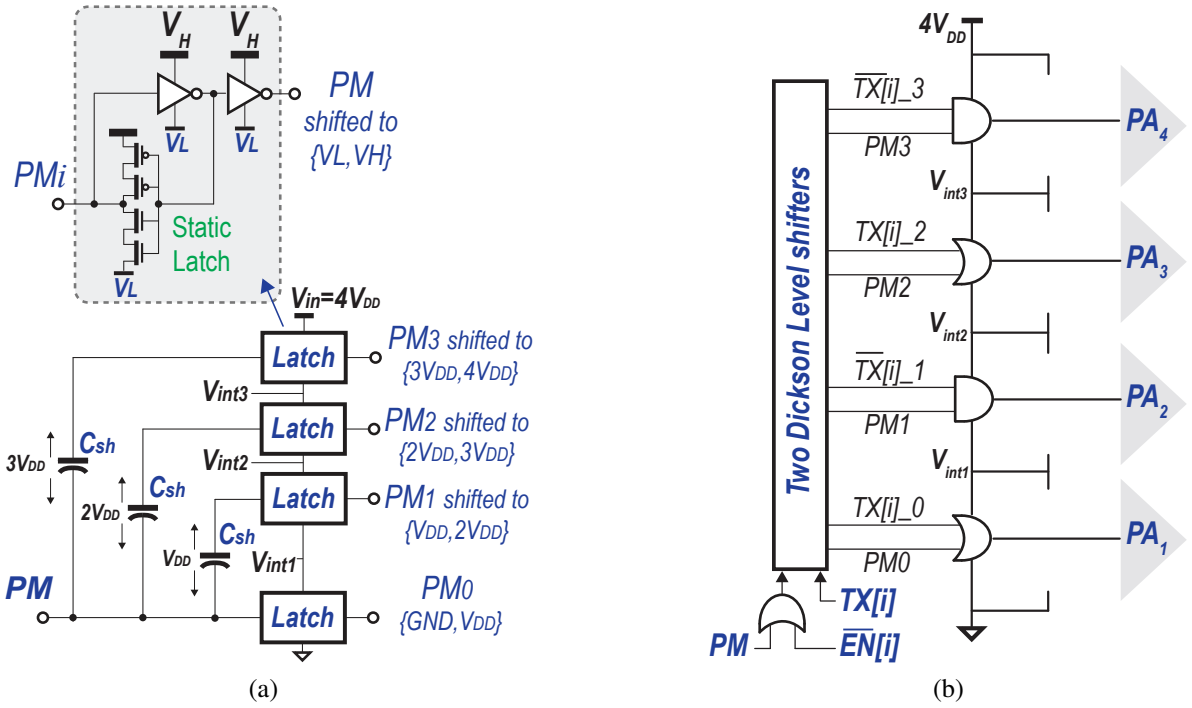


Figure 5.17: Proposed balanced Dickson shifter (a). Generating the PM clocks of PA1, PA2, PA3, and PA4 of the recursive slice in Fig. 5.14 (b).

Unlike a conventional ladder shifter which, due to the series connection of the capacitors and thereby the unequal reactances connecting the input clock to the inputs of the stacked domains can have large skew (40ps in simulation), the proposed approach achieves low skew and requires 3× less capacitance. A static latch is used to provide a low-impedance path to balance the voltage across the Dickson capacitors and enable robust operation against leakage or any coupled glitches. A 1/2-sized inverter is used in the level shifter to establish a weak feedback in the latch that is easily overridden by the triggering input PM driver, thus reducing the required capacitance. The low, V_L, and the high, V_H, supplies of each latch are provided through two consecutive voltage levels from the following list: GND, V_{int1}, V_{int2}, V_{int3}, V_{in}; as illustrated in Fig. 5.17a.

The helper enable-signal, TX, can be shifted in a similar manner for each of the four switches $s2_2$, $s3_1$, $s2_4$, and $s3_3$, where the Dickson shifter operates at the envelope sample rate. The PM input of the flying cells PA1 and PA3, in Fig. 5.14, is provided through CMOS OR gates

between (GND, V_{int1}) and (V_{int2}, V_{int3}), while the inputs to PA2 and PA4 are supplied through an AND gate between (V_{int1}, V_{int2}) and (V_{int3}, $4V_{DD}$), as shown in Fig. 5.17b. When $TX = 1$, i.e. the 1:2 ratio, the gate terminals of (PA1, PA2) and (PA3, PA4) are statically connected to V_{int1} and V_{int3}, respectively. In the 1:1 ratio, the initial four stacked PA cells in the odd-ladder are statically enabled, connecting PA1 and PA3 between (GND, V_{int1}) and (V_{int2} and V_{int3}), respectively, while the PM signals are allowed through the ORs to the gates of PA1 and PA3. A similar operation follows for the even-ladder. When the recursive HoC slice is deactivated through the EN signal received from the thermometer decoder in Fig. 5.7a, the input PM clock is gated, enabling all the NMOS switches and statically holding the output $C_c/64$ capacitors low. When reconfiguring between any two of the three states, the lead delay should be balanced by ensuring equal logic depth for the clock propagation in the 1:1 and 1:2 cases, to eliminate any AM-PM distortion.

5.5 Experimental Results

The proposed recursive House of Cards power amplifier is implemented in a low-power (LP) 65nm bulk CMOS process with nine metal layers.[2] A die photo is shown in Fig. 5.18 with the comprising 16 recursive HoC slices annotated as well as the differential three-level H-tree for balanced PM signal distribution. The occupied area is 1.2mm$\times$1mm. However, the design is loosely wired and the combined area of the individual blocks is approximately 0.83mm$\times$0.58mm to realize 5-bit amplitude resolution. However, higher resolutions can be achieved by further segmenting the same total conductance and capacitance resources to realize finer steps. The chip is directly mounted onto a Rogers 4003C PCB with 50Ω transmission lines for the input and output terminals. All PA cells are implemented with thin-oxide 1.2V transistors, and yet, thanks to the novel stacking and cascading HoC structure, the PA is directly connected to a 4.8V supply without violating any transistor voltage ratings.

[2]LP was chosen due to run availability; better performance could have been achieved in a general purpose (GP) process.

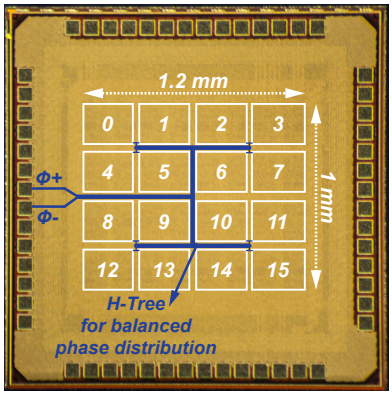


Figure 5.18: Chip micrograph.

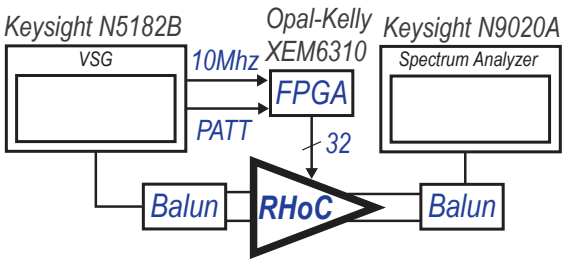


Figure 5.19: Measurement setup.

The PA testing setup is shown in Fig. 5.19. A vector signal generator (Keysight N5182B) generates constant-envelope phase-modulated RF waveforms up to 1GHz, while an FPGA (Xilinx Spartan 6) generates 32 bits of digital amplitude data (two bits to set the state of each of the 16 HoC slices) with up to 144MHz of bandwidth. The differential PA outputs are then combined via an off-chip balun and measured by a spectrum analyzer (Keysight N9020A). The large digital bus from the FPGA to the chip has up to 5ns of within-bus timing misalignment due to trace length mismatch inside the FPGA and the PCB. This limits the close-in shoulder height of the resulting spectrum to about 50dBc, theoretically. The AM and PM generated signals are frequency synchronized through a 10MHz reference signal, while the PATT trigger signal from the VSG aligns the frame start on the FPGA with a resolution of one sample.

When generating non-modulated (CW) signals, the PA was measured to generate up to 23dBm of peak power at the 1:2 ratio, while achieving a 40.3% battery-to-RF efficiency, as

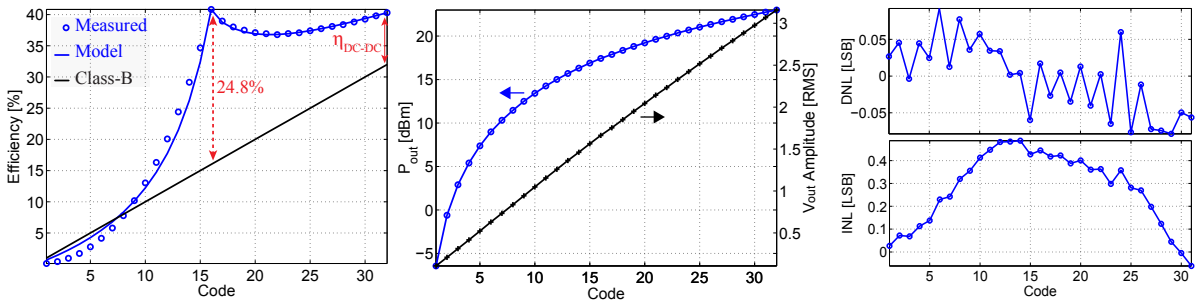
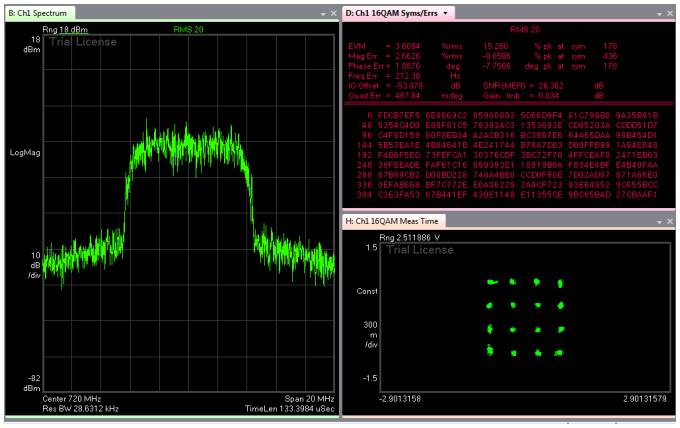


Figure 5.20: (a) Measured battery-to-P_{out} PAE, output power (P_{out}), and output voltage amplitude versus the input code of the proposed flying-domain PA with 50Ω antenna (f_o=720MHz). (b) Measured DNL and INL of the proposed PA.

shown in Fig. 5.20a. The accuracy of the off-chip matching components results in ∼90mV voltage amplitude imbalance between the differential PA channels, which, in addition to the amplitude and phase imbalance of the employed balun, serves to degrade the efficiency by 4-6% due to the non-differential DC-DC loading. A fully integrated matching can help mitigate the amplitude and phase imbalance issues. At the 1:1 ratio (6dB backoff), the PA achieves 40.8% efficiency demonstrating the elimination of cascaded DC-DC losses from the power flow. This is in fact higher than the efficiency at the peak power due in part to the linear and quadratic scaling of the gate-drive and DNW bottom-plate parasitics of the flying domains, respectively. Thanks to the magnetic-less Doherty-like structure, the PA achieves a nearly flat backoff between the two ratios. This is unlike conventional digital Doherty implementations with high-order transformer magnetics [94], [95], [96] that suffer from 8.2%, 4.9%, and 11% lower relative efficiency at 6dB back-off, and that are powered from *ideal* low supply voltages of 3V, 1.5V, and 2.4V/1.2V, respectively. Compared to an ideal class-B PA powered by an 80% efficiency DC-DC converter, the proposed PA achieves 8.3% and 24.8% higher efficiency at peak power and 6dB backoff, respectively. As shown, the measured efficiency is in good agreement with the analytical model. Thanks to the topologically-defined, KVL constrained circuit and the unary-sized array, the proposed PA achieves excellent static linearity results: less than 0.05 LSB differential non-linearity (DNL), and less than 0.5 LSB integral non-linearity (INL), as shown in



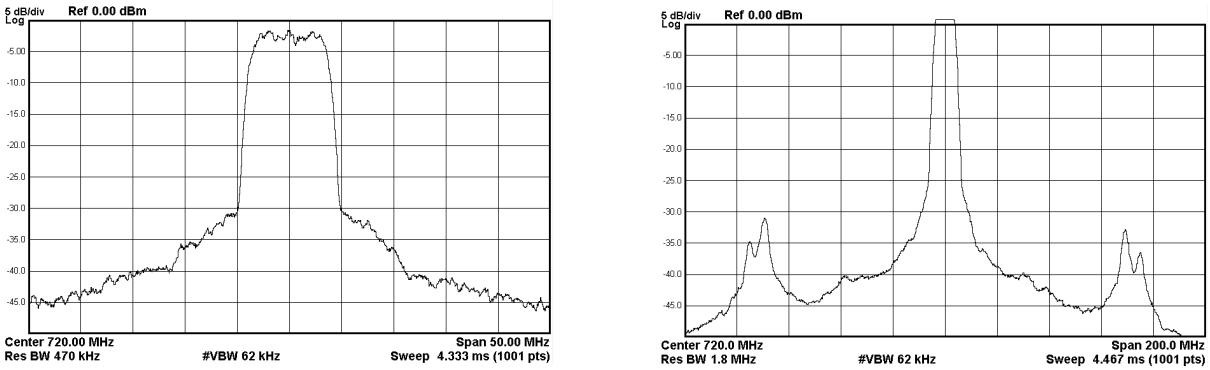
(a)

Figure 5.21: Measured dynamic characteristics of the 16-QAM signal.

Fig. 5.20b.

Figure 5.21a shows the results of dynamic tests, where a 10MHz 16-QAM signal was fed into the PA at a 72MHz envelope rate. This requires strict timing-alignment between the phase and amplitude paths, ideally with sub-ns resolution. The employed measurement setup afforded an alignment accuracy of only $\sim$13ns, which, while not ideal, was sufficient to, with the excellent linearity of the proposed circuit, achieve an error vector magnitude (EVM) of 3.6%-rms, as shown in Fig. 5.21a with the constellation diagram (bottom right) and the in-band power spectrum (left), all without employing any digital pre-distortion. Figure 5.22 shows the measured 10MHz 16-QAM signal transmitted power spectrum characteristics. While achieving -31.7dBc, the close-in shoulder height in Fig. 5.22a can be further enhanced with a better time alignment between the amplitude code and PM signal. The PA achieves an average PAE of 26.5% at an average P_{out} of 15.7dBm. The aliased artifacts in Fig. 5.22b are caused by sampling the amplitude at 72MHz, and can be reduced further through increasing the sampling frequency and/or using a higher-order filtering function. A first/second-order hold digital filter can be employed to reconstruct the continuous-time signal from the discrete samples through linear (or higher order) interpolation instead of holding each sample value for one sample interval (i.e. zero-order hold).

A transient test of a 20MHz 32-QAM modulated signal performed using a previous



(a) (b)

Figure 5.22: Measured spectrum, close-in (a) and far-out (b).

version of the developed test setup is shown in Fig. 5.23. At a 100MHz envelope rate, the PA responds to 3-bit AM codeword changes (observed to be the largest change in the signal) within 2.5ns as shown in Fig. 5.23 (bottom), implying that the maximum bandwidth of the proposed design is up to 400MHz. Generally, the implementation of the amplitude and phase modulators on-chip at high data rates is challenging and results in large area and power overheads. Table 5.1 summarizes the results of the proposed PA in contrast to prior art. The recursive house of cards PA achieves the highest power added efficiency amongst prior-art battery-connected CMOS PAs at both peak and 6dB backoff power levels.

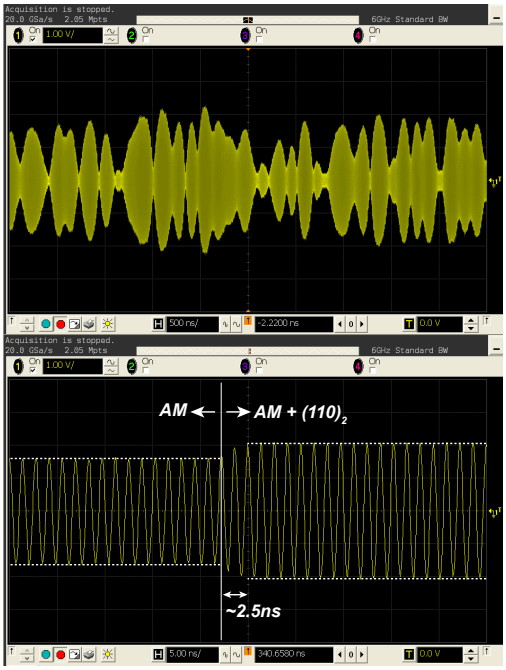


Figure 5.23: Measured time-domain output of the proposed PA with 32-QAM 20-MHz OFDM (f_o=720MHz) (top) and measured AM step response for 6-step change (bottom).

Table 5.1: Comparison with prior work

	Aoki, JSSC'02	**Nakatani, CSICS'13**	**Yoo, ISSCC'11**	**Arno, ISSCC'14**	**Hu, RFIC '14**	**Lee, ISSCC'15**	**This work**
PA technique	Power combining	Digital polar	Switched capacitor	Env. tracking	Digital Doherty	Env. tracking	**Power Inverter**
Technology	180nm	150nm	90nm	130nm	65nm	130nm	**65nm LP**
Frequency [GHz]	1.9	0.85/ 1.75	2.2	1.747	3.6	1.747	**0.72**
VBAT [V]	N/A	3.3	N/A	3.7	N/A	4	**4.8**
PA VDD [V]	1.8	N.R.	1.25/ 2.5	N.R.	3	N.R	**N/A**
Pout,max [dBm]	34.5	27.5 / 29	25.2	26.3	27.3	26	**23**
PAE @ Pout,max [%]	50	N.R.	55.2	N.R.	32.5	40	**40.3**
PAE @ 6dB backoff [%]	27*	N.R.	35.1	N.R.	22	28	**40.8**
VBAT-to-Pout @ Pout,max[%]	N/A	13.2 / 22.2	N/A	39	N/A	N/A	**40.3**
VBAT-to-Pout @ 6dB backoff	N/A	N.R. / 11.1*	N/A	N.R.	N/A	N/A	**40.8**
INL	N/A	N/A	<3 LSB	N/A	N/A	N/A	**<0.5 LSB**
DNL	N/A	N/A	<0.5 LSB	N/A	N/A	N/A	**<0.09 LSB**

5.6 Conclusion

This chapter has presented a new PA design that utilized stacked and flying class-D cells arranged in a House of Cards architecture to facilitate efficient generation of high output power, all while using low-voltage, thin-oxide CMOS transistors. Individual HoC cells were then made fully modular and reconfigurable to support different voltage conversion ratios and thus high efficiency at 6dB back-off. By capacitively combining the outputs of HoC slices operating at different ratios, the PA could be dynamically configured to deliver high efficiency at intermediate back-off levels, exactly following a Doherty back-off profile, but without requiring any magnetic components. The proposed HoC PA was implemented in 65nm LP CMOS, was operated directly at 4.8V without any explicit DC-DC converter, and was shown to achieve $>$40% battery-to-RF efficiency at both peak power and 6dB back-off, while enabling linear transmission of $>$10MHz 16-QAM signals.

5.7 Acknowledgements

This chapter is based on and mostly a reprint of the following publications:

- L.G. Salem, J.F. Buckwalter, and P.P. Mercier, "A recursive switched-capacitor house-of-cards power amplifier," IEEE Journal of Solid-State Circuits (JSSC), Jul. 2017, vol. 52, no.7, pp. 1719-1738.
- L.G. Salem, J.F. Buckwalter, and P.P. Mercier, "A recursive house-of-cards digital power amplifier employing a λ/4-less Doherty power combiner in 65nm CMOS," in Proc. IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2016, pp. 189-192.

Chapter 6

Adiabatic Clocking

6.1 Introduction

Clock distribution in modern SoCs consumes a significant fraction of total chip power. To reduce clock distribution power, resonant clocking schemes, where an inductive reactance is used to cancel the capacitive reactance of global clock networks at a given resonance frequency, f_o, have been proposed. Conventionally, such schemes are only suitable at high multi-GHz frequencies in order to be able to place the employed inductors on chip [97, 98]. Since many modern energy-efficient SoC designs optimize for clock frequencies $<$ 2GHz, with dynamic voltage and frequency scaling (DVFS) techniques bringing the core clock frequencies and the supply voltages V_{DD} to the MHz and near-threshold regimes, respectively, there is a need to develop low-power clock distribution schemes that can work across increasingly wider operating ranges. While recent work in quasi-continuous resonant clocking have been proposed to intermittently cancel global clock tree capacitance during edge transitions, such techniques require large off-chip inductors and are limited to 0.98MHz [99] and 150MHz [100], respectively, owing to the need to operate well below resonance (i.e., $\ll f_o$/10). Thus, while prior-art has shown power reduction for targeted applications, they all require large on- or off-chip magnetics, and do not meet the

MHz-to-GHz frequency-range needs of modern DVFS-enabled SoCs. To address these problems, this chapter introduces a fully-integrated adiabatic clocking scheme that efficiently synthesizes n-step clock waveforms from 1MHz to 2GHz via a switched-capacitor DC-AC multi-level inverter topology, theoretically reducing power by 1/n without using any magnetic component.

6.2 Challenges of Resonant Clocking

Fig. 6.1 illustrates prior resonant clocking techniques, including intermittent resonant clocking (IRC) [3] and quasi-resonant clocking (QRC) [4] schemes. Conventional approaches utilize an array of on-chip inductors along with per-inductor decoupling capacitor ($> 10 \times C_{CLK}$). Unfortunately, clock power increases $\sim \pm 20\%$ away from resonance (f_o), thereby limiting DVFS opportunities. On the other hand, IRC and QRC techniques can enable DVFS up to $\sim f_o/10$ by employing large off-chip inductors as in Fig. 6.1 (right). However, such approaches can have severe ringing if accurate pulse width timing is not ensured, thereby requiring power-expensive timing logic overhead, e.g., delay lock loops (DLLs). Furthermore, special gate drivers or charge pumps are required to either boost the gate drive voltage of the footer NMOS in IRC techniques, or provide a $V_{DD}/2$ gate drive for QRC footer transistor Mf, to ensure that it turns off before its drain voltage goes to $V_{DD}/2$ (which is a further device reliability issue).

6.3 Adiabatic Switched-Capacitor Driver

In contrast, clock power is reduced in the proposed approach through an adiabatic stepwise charging technique implemented using a 4-level switched-capacitor DC-AC inverter topology, shown in Fig. 6.1. In this scheme, the CLK capacitance (C_{CLK}) is step-wise charged by sequentially turning on switches s1, s2, s3, and s4, which creates a 4-level voltage staircase whose levels are set by GND, self-balanced capacitors C1 and C2, and V_{DD}. Afterwards, CLK is brought down

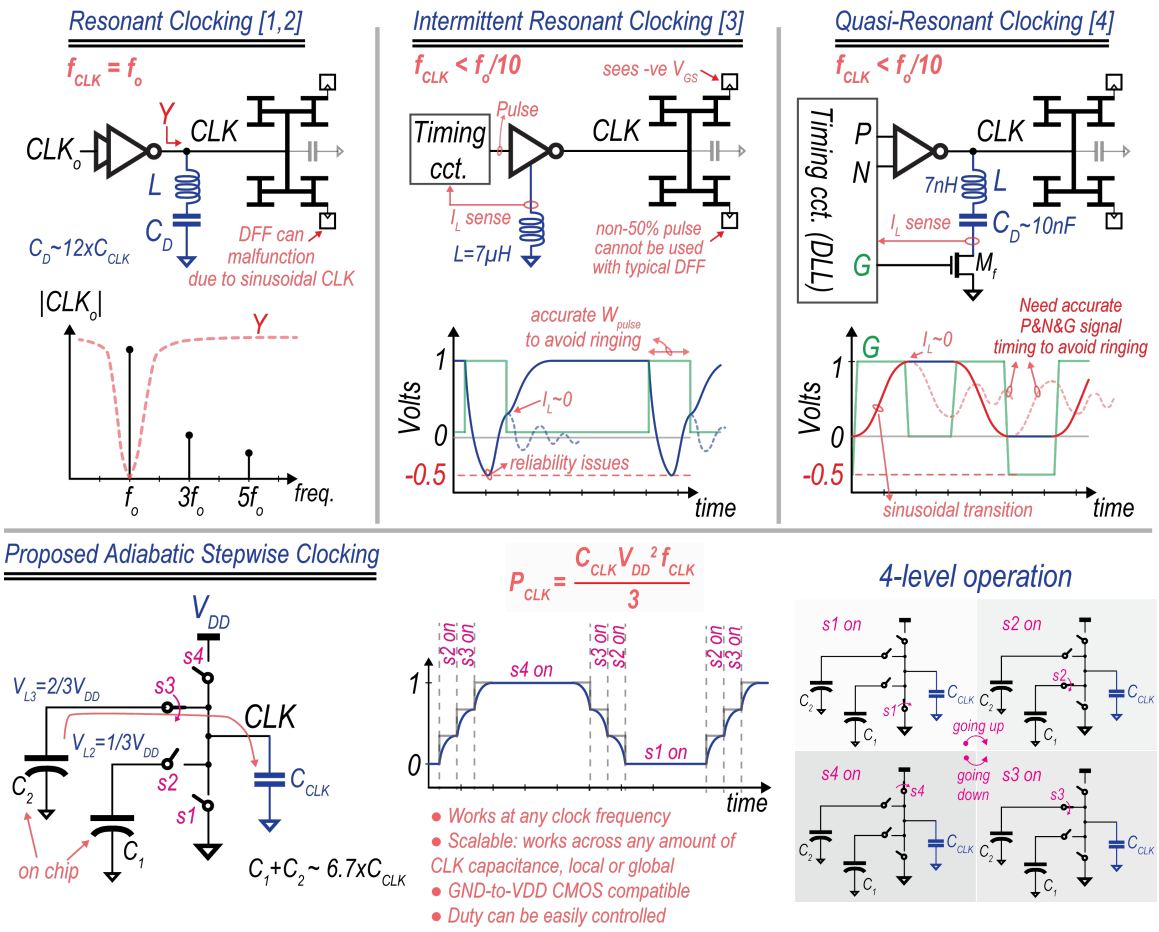


Figure 6.1: Prior inductive resonant clocking techniques (top); the proposed switched-capacitor multi-level adiabatic clocking technique (bottom).

to GND in the reverse order. Theoretically, 4-level adiabatic charging reduces CLK power by 3×. By repeating the same operation periodically at f_{CLK}, a KVL-constrained multi-phase switched network is established which inherently enforces V_{L2}=V_{DD}/3 and V_{L3}=2/3V_{DD} without any explicit DC-DC converter.

6.4 Circuit Implementation

The proposed reconfigurable 4-level inverter, shown in Fig. 6.2, is composed of two standard CMOS inverters whose outputs are tied together: an outer inverter powered between

V_{DD} and GND, and an inner inverter with a floating supply and ground at $2/3V_{DD}$ and $1/3V_{DD}$, respectively. The outer inverter is controlled by signals P and N, periodically connecting its output to V_{DD} or GND, while the inner inverter is controlled by signals Pi and Ni, periodically connecting its output to $2/3V_{DD}$ or $V_{DD}/3$. These control signals are generated by passing the input clock through a tunable-delay chain of inverters, producing three signals, A, B, and C, with equal delay times, Δt, and passing these signals through a custom House-of-Cards (HoC) timing gate (whose operation is logically represented by eight combinational gates in Fig. 6.2). To enable adiabatic charging, the switches $R_{on}/W_s w$ should be set such that the RC_{CLK} time constant, τ, is less than Δt/1.4. The 4-level inverter requires a total of $6.7C_{CLK}$ of self-balancing capacitance, which is 1.8x lower than the capacitance required in conventional resonant schemes. The 4-level inverter can be reconfigured into a 3-level inverter by overlapping pulses Ni, Pi, as shown in Fig. 6.2, coarsely decreasing the 10-90% rise/fall time from $0.8\times3\Delta$t to $0.8\times2\Delta$t; fine rise/fall time configuration can be adjusted via the tunable delay chain. The 4-level inverter can also be reconfigured into a standard 2-level CMOS inverter by disabling the inner inverter.

The actual implementation of the custom HoC timing gate, optimized to generate N, Ni, Pi, and P with non-overlapping properties in minimal area and power, is shown in Fig. 6.3. Non-overlapping pulses are inherently generated in the HoC gate since, when the leaves of the HoC tree turn on, the output pulses must wait until the common root in the tree is charged or discharged. For instance, suppose that ABC=110, thereby $\bar{N}i$=0. Then, if C transitions from 0 to 1, Cp1 and Cp2 (Cp3 and Cp4) are already discharged (charged) when the C/$\bar{C}$ edge arrives, and hence all controlling pulses (N, Ni, Pi, P) are synchronized without overlap. The HoC gate can be folded to support 4-, 3-, or 2-level timing signals via configuration bits R1 and R0.

The overall architecture of the adiabatic clocking prototype is shown in Fig. 6.3. A 4b programmable-strength reconfigurable 4-level inverter is implemented, where all 16 slices share the same VL2 and VL3 nodes, each connected to 50pF of on-chip thick-oxide capacitance. An on-chip current starved oscillator locked through an off-chip phase locked loop (PLL) is employed

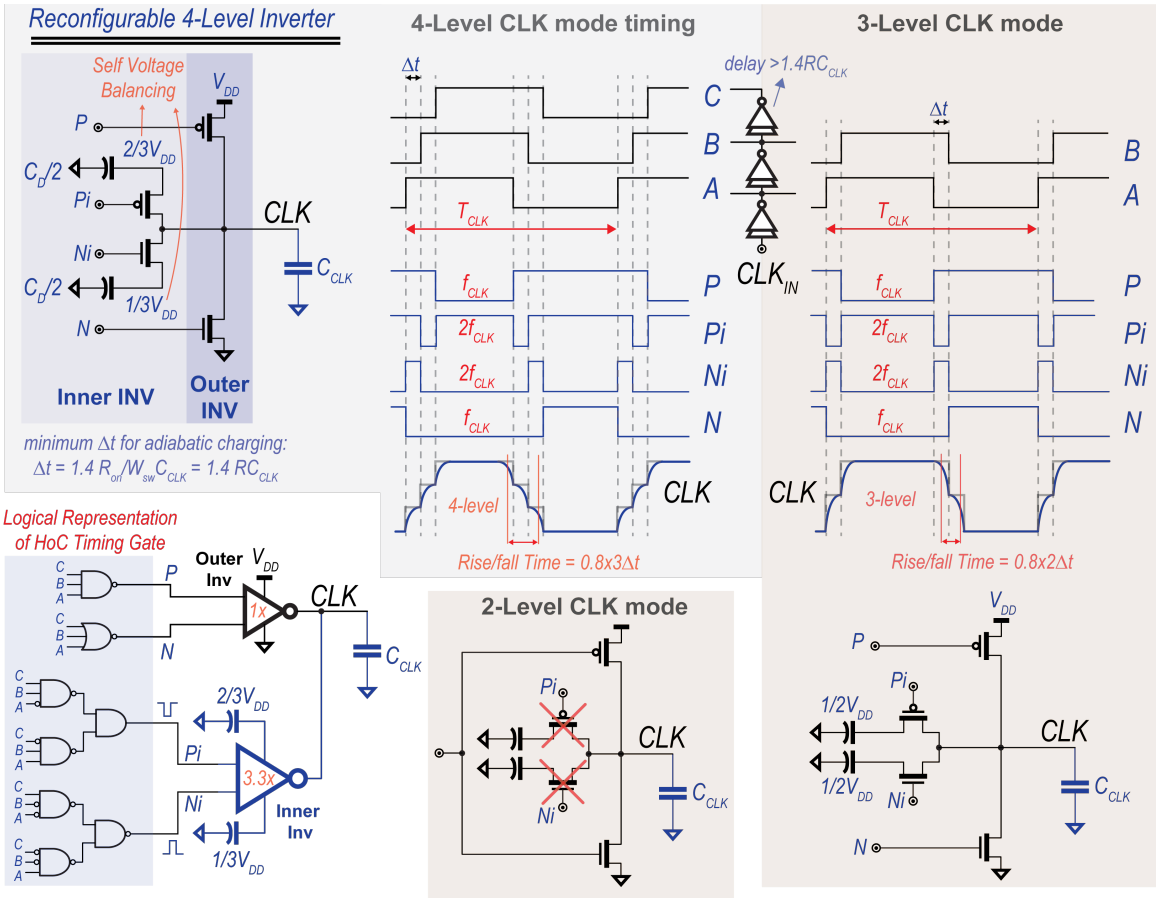


Figure 6.2: Circuit schematics and timing diagrams of the 4-level inverter, showing how it can be reconfigured into 3- and 2-level modes.

as the clock source. To ensure sufficient rise/fall time for adiabatic operation up to 2GHz, phases A, B, C are provided from the first 3 stages in the 5-stage ring oscillator such that the adiabatic CLK 10-90% (20-80%) rise/fall time is $\ll 24\%$ ($\ll 18\%$) of the CLK period. The 4-level inverter drives a 32x pipelined array of 64b MACs. Capacitance from digital logic, CLK wiring, and drain parasitics of the driver totals C_{CLK} = 15pF (2:1:1).

Fabricated in 9M 45nm silicon-on-insulator (SOI), the designed global clock distribution, spanning a load area of $550\times550\mu m^2$, takes the form of a tree-driven grid. The clock tree and grid (as well as the power distribution) occupy the top 2 ultra-thick (UT) metals M9 and M8, respectively. Each line of the 5-level H-tree is split into multiple fingers as shown in Fig. 6.3 to reduce inductance and enable rigid operation up to 10GHz. The adiabatic driver, including

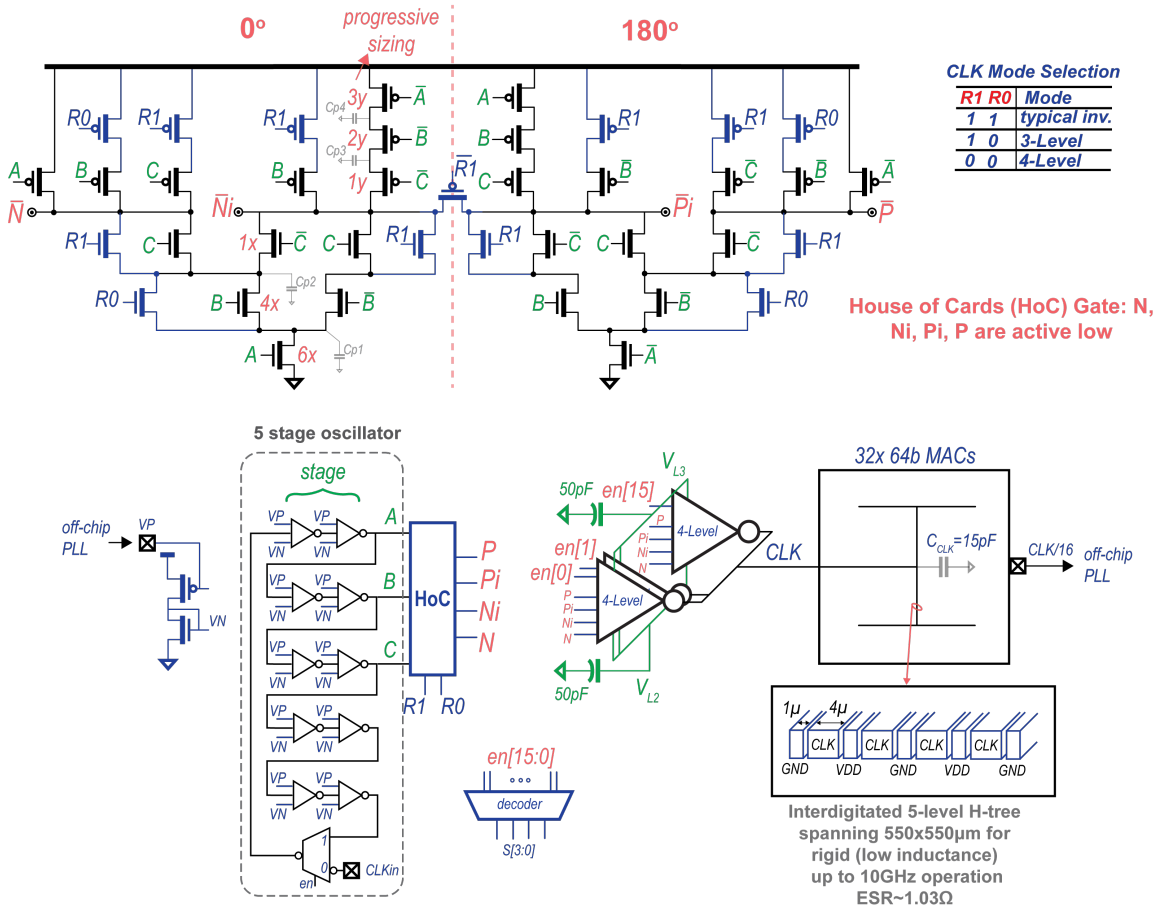


Figure 6.3: Schematic of the custom HoC timing gate (top); architecture of the implemented test chip (bottom).

self-balancing capacitors, occupies only 0.0187mm^2 ($<$ 6.2% of the load area). To quantify the improvement over conventional clocking, the driver is configured into the 2-level mode with reduced drive strength for identical rise/fall time to the 3/4-level modes, while multi-level overhead circuits are off.

6.5 Measurement Results

Measurement results at 1V in Fig. 6.4 indicate 4-level (3-level) clock power savings of at least 42% (28.4%) from 10MHz-2GHz while successfully operating a digital load, with 55.6% (45.5%) peak savings at 10MHz where adiabatic clocking overhead is minimal. At 0.4V

near-threshold operation, 4-level (3-level) clocking successfully achieves a measured power savings of at least 34.4% (22.5%) from 1MHz-267MHz. Figure 6.4 also shows the measured CLK driver energy under DVFS operation between 0.4-1V, showing above 39.4% savings across the entire DVFS range, with 46.5% peak savings. Figure 6.5 shows the measured power savings across all possible voltages and frequencies, indicating a 41.8% average savings across a 2000 times dynamic frequency range. The measured transient waveforms of the 4-level operation at 10MHz from a 1V supply is shown in Fig. 6.5, via both a common-source PMOS analog buffer (open-drain driver) biased by 25Ω (50Ω on PCB and 50Ω input of a sampling scope) for 0.75V/V gain, and a cascaded inverter chain. Figure 6.6 compares the proposed design to the state-of-the-art clocking schemes, demonstrating the widest adiabatic frequency and supply voltage dynamic ranges with the highest clock power savings, all with minimal overhead. A die photo is shown in Fig. 6.7.

6.6 Acknowledgements

This chapter is based on and mostly a reprint of the following publication:

L.G. Salem and P.P. Mercier, "A 0.4-1V 1MHz-to-2GHz switched-capacitor adiabatic clock driver achieving 55.6% clock power reduction," 2017 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2017, pp. 442-443.

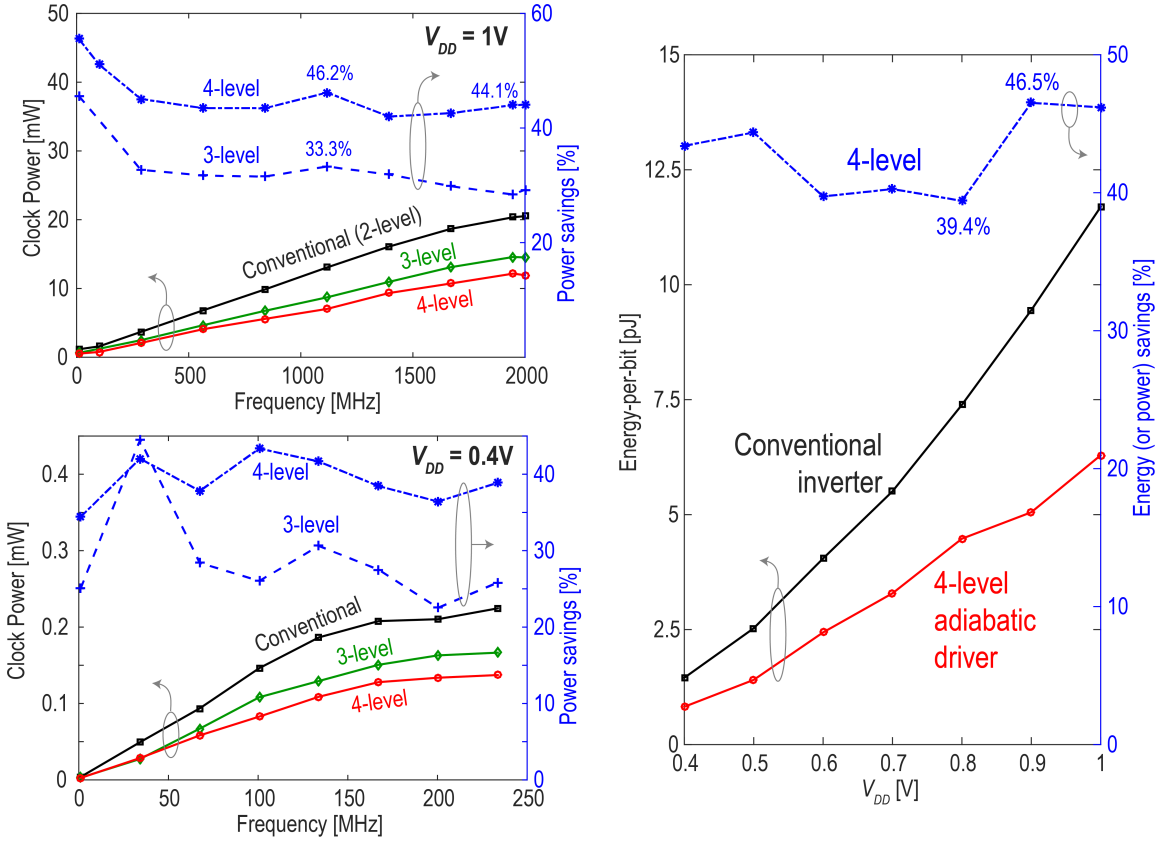


Figure 6.4: Measured clock power improvement of 4- and 3-level clocking compared to conventional clocking at 1V and 0.4V across frequency (left); measured CLK energy-per-bit improvement of the 4-level inverter across supply voltages.

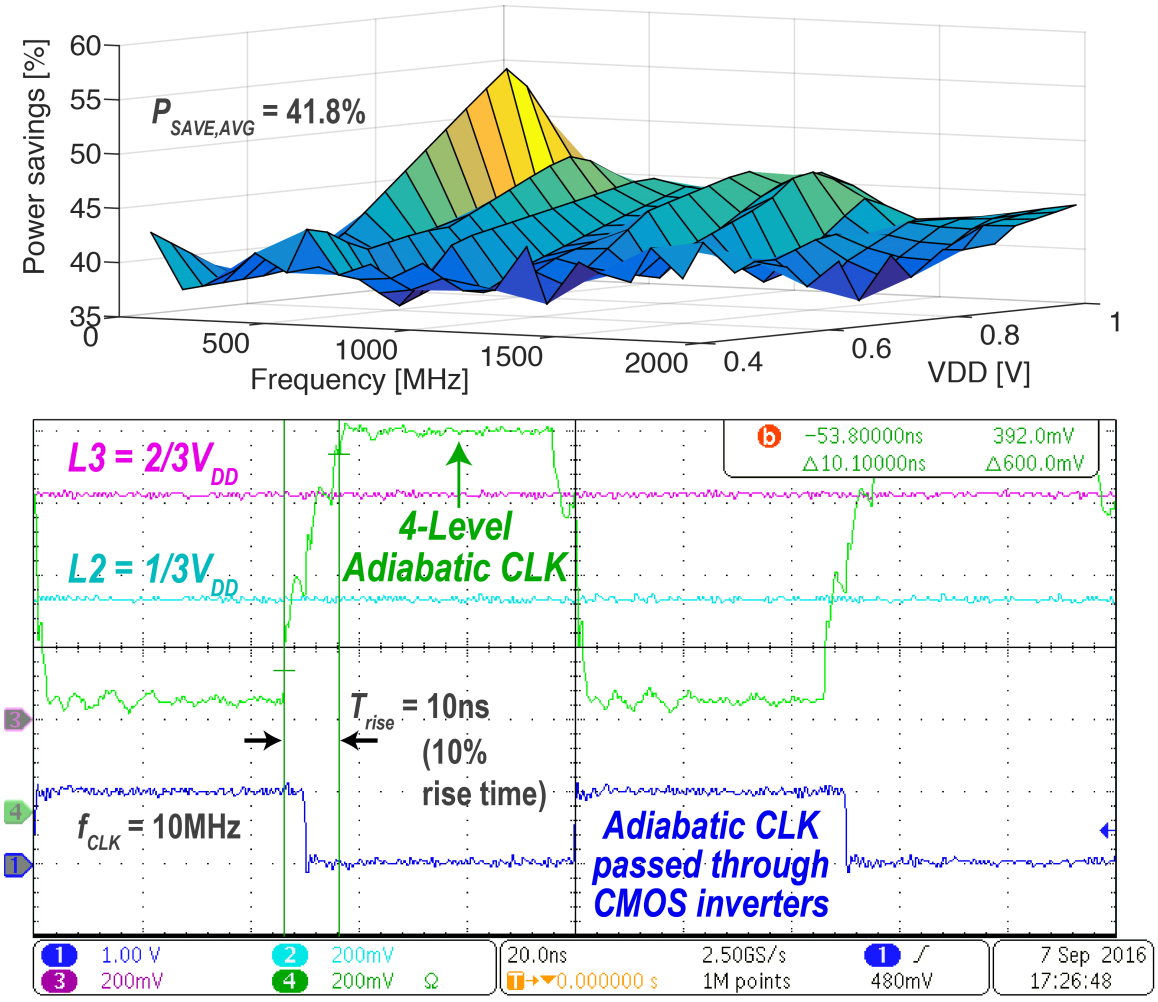


Figure 6.5: Measured power savings through 4-level clocking from 1MHz-2GHz and 0.4-1V, achieving an average efficiency of 41.8% across the entire space (top); measured transient waveforms of the 4-level adiabatic clock at (10MHz, 1V).

	ISSCC'04 [1]	ISSCC'13 [3]	ISSCC'14 [2]	ISSCC'16 [4]	This Work
Process	90nm	40nm	22nm SOI	65nm	**45nm SOI**
Power reduction methodology	LC resonance	LC resonance	LC resonance	LC resonance	**Step-wise charging**
Inductor	four 1nH per CLK sector (on-chip)	7μH (off-chip)	57 CLK sectors, each with 2 inductors from 0.3-2.5nH (on-chip)	~7nH (off-chip)	**None**
Area	N.R.	N.R.	N.R.	$0.04mm^2$ (not including inductor)	**$0.019mm^2$ (6.2% of A_{LOAD})**
Power reduction	20%	36%	25 – 33%	32 – 47%	**26.2 – 55.6% (average = 41.8%)**
Frequency range with power reduction	2.6 – 4.6GHz	0.98MHz*	2.5 – 5GHz	10 – 152MHz	**1MHz – 2GHz**
Dynamic frequency range	1.8x	N/A	2x	15.2x	**2,000x**
Voltage range	1V	0.37V**	0.75 – 1.08V (1.44x)	0.7 – 1.2V (1.7x)	**0.4** – 1V (2.5x)**
Duty-cycle control	No	No	Limited	Yes	**Yes**
Clock capacitance	7.5pF	10pF	N.R.	N.R.	**15pF**
CLK granularity	Global only	Global only	Global only	Global only	**Global + local**

* Low frequency range not reported N.R. = Not Reported
**Near-threshold operation

Figure 6.6: Comparison of the proposed adiabatic clocking scheme versus resonant clocking implementations.

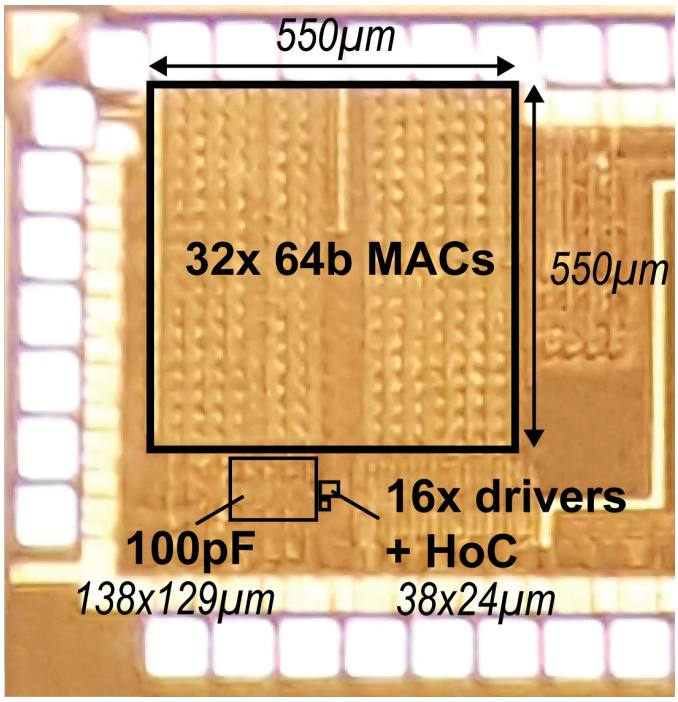


Figure 6.7: Micrograph of the fabricated chip.

Part III

Fine-Grain Power Management

Chapter 7

A Recursive Digital Low-Dropout Voltage Regulator

7.1 Introduction

Modern sub- or near-threshold SoC designs feature multiple power domains to dynamically track the maximum energy efficiency point (62mV-to-0.45V [101, 6, 102, 103, 104, 105, 106, 107]) in response to application demands. Analog low drop-out (LDO) regulators [108, 109, 110, 111, 112, 113, 114, 91] can generate such voltages in a small area with rapid response times (e.g. TR=0.65ns [91]). However, the input voltage, V_{in}, is typically brought on-chip via either a high-efficiency switching DC-DC converter or an external harvesting source, both with low-voltage sub- or near-threshold outputs (e.g., 0.5V), where analog LDOs have difficulty operating due to low voltage headroom. On the other hand, Digital LDOs (DLDOs) [115, 116, 117, 118, 119, 120, 121, 122, 123, 124], which replace a single saturated PMOS power transistor with an array of PMOS power transistors operating in the linear region, can operate down to 0.5V since less headroom is required. Most switch-array based DLDOs rely on an integral controller to linearly search (via a 1-bit ADC) for the PMOS array conductance that

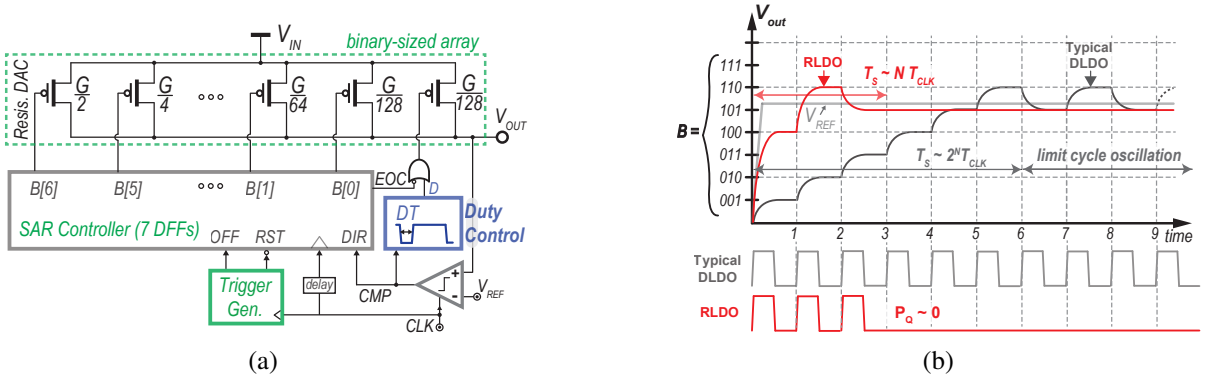


Figure 7.1: (a) Block-level diagram of the proposed RLDO. (b) Illustrative V_{out} response to a 0-to-V_{ref} step when the rate of change of V_{out} is much faster than the clock frequency, f_{CLK}, to explicitly show the binary search process.

realizes the nearest output voltage, V_{out}, to the desired target, V_{ref}. For N-bit control, linear search can take up to 2^N cycles. To expedite conversion, prior work has suggested adding a proportional term via a multi-bit ADC [120, 121]. However, the achievable response times are $44-4000$ns [120, 121], which is not sufficient for many digital loads.

Intuitively, binary search, illustrated in Fig. 7.1a, can find the required array conductance in *exponentially* shorter time, i.e., *O(N)* cycles, and therefore can enable exponentially faster response, T_R, and settling, T_S, times (Fig. 7.1b) than linear search. Unfortunately, a DLDO employing a binary search algorithm suffers from large staircase overshoots/undershoots during the N-step binary search, along with large steady-state error, as will be discussed in Sections 7.3 and 7.5. These challenges rendered binary-search control impractical as a main regulation scheme ever since the first introduction of switch-array DLDOs in [115, 116].

To enable a pragmatic binary-search-based DLDO [81], the large staircase overshoots and undershoots during binary-search steps are avoided by operating from a clock whose frequency is faster than the time-constant of the load. Since doing so nominally renders a DLDO fully-unstable due to the erroneous successive decisions, stability is obtained in the proposed design via a variable-coefficient proportional-derivative compensation scheme described in Section 7.3. To eliminate steady-state errors, a hysteretic PWM control scheme is proposed in Section 7.4 that also

enables sub-LSB load-current regulation. Additionally, loop-interruption logic is implemented in Section 7.5 to avoid large overshoot/undershoot that can result when a sudden I_L or ΔV_{in} step change occurs in the middle of the binary-search (after deciding the first few most-significant-bits (MSBs)).

7.2 Successive-Approximation Digital LDO Topology and Operation

7.2.1 SAR LDO Architecture

A conceptual 7-bit binary-search DLDO is illustrated in Fig. 7.1a. The array of 2^N equal-size PMOS fingers in barrel-based linear-search DLDOs [116, 125] is replaced with N binary-weighted PMOS switches (PMOS DAC), with a total conductance G, controlled via a SAR register. An additional switch of weight equal to the LSB is included for duty control (described later in Section 7.4).

V_{ref}-Step Transient Response

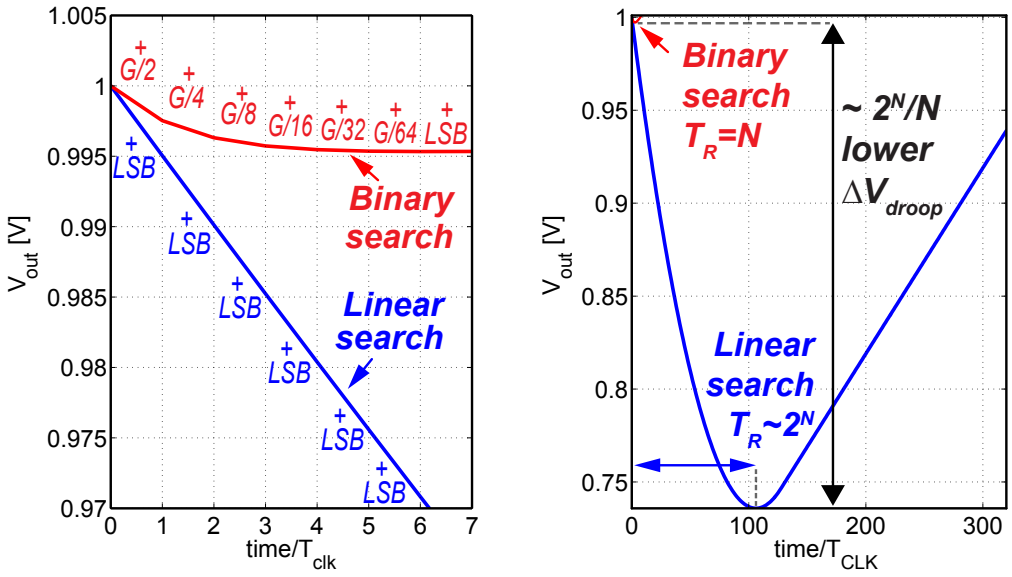
Figure 7.1b shows the transient V_{out} response of representative 3-bit linear-search and binary-search DLDOs to a 0-to-V_{ref} input reference step (only 3 bits are shown for illustrative simplicity). For illustration purposes only, f_{CLK} is set be slower than the rate of change of V_{out} in this example to allow enough time for V_{out} to settle before taking each bit-decision. Here, the PMOS array is initially turned off. At the first positive edge after V_{ref} step-increase, the comparator output goes to high, and hence under binary search the MSB switch is turned on. As a result, V_{out} starts to increase from zero initial voltage until it settles at the corresponding $G/2$ voltage level. At the following positive clock, V_{out} is still less than V_{ref}, therefore, the next MSB switch in the array is turned on which increases V_{out} to the $\frac{3}{4}G$ voltage level. At the third clock

cycle, V_{out} is larger than V_{ref}, and therefore, the SAR register turns off the second bit, $B(1)$, while simultaneously turning on the LSB.

As illustrated in Fig. 7.1b, a binary-search DLDO achieves $2^N/N$ faster settling time than baseline linear-search DLDOs. Furthermore, the SAR controller requires only N DFFs instead of 2^N DFFs for a barrel shifter, reducing control area by $2^N/N$. Along with a $2^N/N$ reduction in the number of cycles to reach V_{ref}, clock power is thus reduced by $N^2/2^{2N}$. Importantly, a binary-search DLDO does not suffer from limit-cycle oscillations as in baseline linear-search DLDOs, enabling $1/2^N$ lower quiescent current, I_Q, and hence higher current efficiency, where the entire SAR controller is clock-gated and only a single DFF is clocked during duty-control, as discussed later in Section 7.4. Prior schemes [124, 122] have been proposed to reduce I_Q of linear search, however, they come at a reduced DC accuracy, as will be discussed shortly. On the other hand, to reduce area and quiescent power in a linear-search DLDO, it is in principal possible to replace the 2^N barrel shifter by an N-bit up/down counter driving binary-sized PMOS fingers. While this modified architecture reduces the number of required DFFs, and hence quiescent power (by $2^N/N$), it results in significant periodic noise in the on-chip supply lines due to limit cycle oscillation of the binary-weighted, as opposed to unary-sized, PMOS fingers.

$I_{L,max}$-Step Transient Response

Figure 7.2a illustrates the transient V_{out} response of representative 7-bit linear-search and binary-search DLDOs to a full-range 0-to-$I_{L,max}$ load step. Compared to a baseline linear-search DLDO which turns on only a single finger (with an LSB conductance of $G/2^7$) after the load step, the SAR architecture turns on half of the total array conductance, $G/2$, after the first clock cycle. In the second clock cycle, the RLDO turns on an additional quarter of the array conductance, $G/4$, and so on in a binary-subsiding manner. The proposed SAR architecture therefore requires only N clock cycles to respond to a full load step compared to 2^N in a baseline linear-search DLDO, enabling a much smaller response time and ΔV_{droop}. However, in reality, the output voltage droop,



(a) (b)

Figure 7.2: Transient V_{out} response of a 7-bit linear-search and binary-search DLDOs to 0-to-$I_{L,max}$ load step. (a) close-in. (b) Far-out. Both LDOs have the same total array conductance, G, where $G\Delta V_{drop-out}$ matches $I_{L,max}$.

ΔV_{droop}, increases the finger current to $G/2^N(\Delta V_{drop-out}+\Delta V_{droop})$ due to linear-mode operation of the PMOS transistors, and hence the DLDO response time is a fraction, $\alpha<1$, of the simplified current-source case: $T_{R,DLDO}=\alpha_1 2^N T_{clk}$; $T_{R,RLDO}=\alpha_2 N T_{clk}$, as shown in Fig. 7.2b.

7.2.2 Performance Comparison: Speed-Power Trade-off Improvement via SAR Control

One of the main design objectives of a DLDO is to minimize the output voltage droop to a sudden load step. Nominally, consuming K$\times$ higher I_Q (e.g., via a higher f_{CLK} in an DLDO) enables K$\times$ faster T_R, and hence the speed-power product is fixed for a given architecture. Therefore, the product of T_R and normalized quiescent current is employed as a figure-of-merit

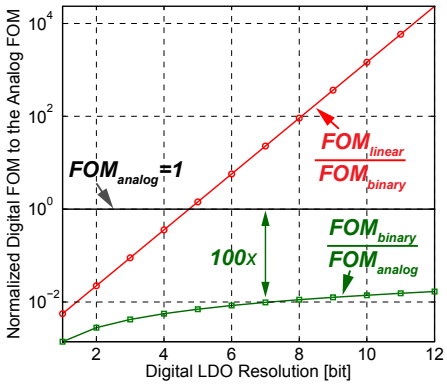


Figure 7.3: FOM of a linear-search DLDO and a binary-search RLDO normalized to the analog LDO FOM for the same process technology, $I_Q/\Delta I_L$, and C_{out} versus the required resolution N.

(FOM) [8] for a normalized comparison among various LDOs:

$$FOM = T_R\hat{I_Q} = \frac{C_{out}\Delta V_{droop}}{I_{L,max} - I_{L,min}} \frac{I_Q}{I_{L,max} - I_{L,min}}, \tag{7.1}$$

where the load step test is performed between $I_{L,min}$ and $I_{L,max}$ with a load rise/fall time less than $T_R/10$[1] and I_Q is the quiescent current incurred during the periodic load swing test and not the best case I_Q. A binary-search DLDO inherently achieves a $2^{2N}/N$ smaller (i.e., better) FOM than a baseline linear-search DLDO due to the $2^N/N$ faster response time and the reduced quiescent power afforded by the $1/2^N$ lower number of switching DFFs at steady-state. Figure 7.3 illustrates the FOMs for an analog LDO, and linear- and binary-search DLDOs.

[1] Otherwise, when the rise/fall time of the load-current swing is comparable to T_R, the measured T_R becomes the unit-*ramp* response time and not the unit-*step* response time. This invalidates the measured FOM since the output voltage droop, ΔV_{droop}, due to a unit-*ramp* current is much smaller than the droop in the unit-step current case.

7.3 Variable Coefficients Proportional-Derivative Compensation

In order to filter out the unacceptably large staircase overshoots and undershoots of the SAR conversion steps in Fig. 7.1b, it is necessary to take the SAR decisions at a faster rate than the rate of change of V_{out}. However, this can lead to erroneous successive decisions during the SAR conversion and hence an unstable response. This is why prior-art binary search architectures were not practically feasible [126, 127]; instead, prior-art SAR switching was utilized only as a mid sub-array helper DLDO [128]. In order to enable a pragmatic SAR-based LDO, a *proportional-derivative* (PD) compensation scheme is proposed to establish a multi-rate *fast-slow* control loop that observes (samples) V_{out} at a fast clock speed, f_{CLK}, to eliminate the SAR conversion overshoots and undershoots, while allowing the integrator to accumulate at a rate close to the output pole frequency, $f_c \sim f_L$ to avoid instability.

7.3.1 Stability Analysis of DLDOs using a Bode Diagram Approach

Figure 7.4a illustrates a piece-wise-linear small-signal AC model of a binary-search DLDO without PD compensation in the Z-domain. The initial load conductance, $G_L = 1/R_L$ and the initial (i.e., prior to the i^{th} iteration) PMOS array conductance, $G_p(i-1)$, in Fig. 7.4a establish the DC operating point around which the AC response to the input small-signal disturbance, ΔV_{ref}, is evaluated.

The comparator samples and quantizes the input error signal $e(t) = V_{ref} - V_{out}(t)$. At the beginning of the conversion, the SAR controller has the highest gain (via switching the MSB conductance) to facilitate a rapid response time via a large loop bandwidth. As the SAR algorithm converges, the step size at the i^{th} iteration decreases (i.e., $M(i)\times$ LSB $= G/2^i$), and thus the gain, $K(i)$, decreases in a binary subsiding manner, until the gain reaches the LSB value. For the purpose of stability analysis, the SAR register is assumed to accumulate the instantaneous error,

$M(i)e[k]$ rather than $M(i)e[i]$, to determine the number of turned-on PMOS fingers, $B[k]$.

The zero-order-hold equivalent of the output RC network, comprising $G_p(i-1)$, R_L, and C_{out}, can be found as $(1-z_L)/(z-z_L)$, where $z_L = e^{-f_L/f_{CLK}}$ is the output pole, which is determined by the ratio between the equivalent output-load frequency, $f_L = (G_L + G_p(i-1))/C_{out}$, and the DLDO sampling clock, f_{CLK}. Therefore, the open-loop transfer function of such a second-order feedback control loop is given by

$$G(z) = \frac{K(i)(1-z_L)z}{(z-1)(z-z_L)} \tag{7.2}$$

and hence $G(z)$ has two poles: the loop integrator pole on the unity circle ($z=1$), and the output pole, z_L.

It can be shown that the open-loop gain $G(s)$ of the corresponding continuous-time system using *impulse-invariance* transformation [129] of the digital LDO in (7.2) is given by

$$G(s) = \frac{\omega_n^2}{s(s+2\eta\omega_n)}. \tag{7.3}$$

Therefore, the open-loop gain $G(s)$ contains two poles, where the Z-domain poles, $z=1$ and z_L, map to, the $s=0$ and f_L, in the S-domain. Figure 7.4b illustrates the Bode diagram of a DLDO, where the integrator pole ($s=0$) asymptote intersects the 0-dB axis at $f_I = \omega_n/(2\eta)$. It can be shown that $f_I = \beta f_{CLK} \ln(M(i) \times \text{LSB} + 1)$, where β is a proportionality factor less than unity. Therefore, for a given output load frequency, f_L, increasing the sampling frequency, f_{CLK}, or the array conductance step, M, both serve to increase f_I, which shifts the magnitude plot upwards, as shown in Fig. 7.4b. This boosts the unity-gain frequency or loop bandwidth, $\omega_{GC} = \sqrt{f_L f_I}$, and hence enables a faster response time, however, at a reduced phase margin (PM) and stability as set by: $PM = 90^o - tan^{-1}\sqrt{\frac{f_I}{f_L}}$. This speed-stability trade-off sets the allowable values for the design variables f_{CLK} and M, and hence the upper bound on the achievable response time for a given design. The speed-stability trade-off becomes tighter with reduced current values: at a

fixed f_{CLK} and M, f_L becomes more dominant with smaller loads, which increases the relative separation between the two poles (f_L and f_I) and hence reduces the phase margin and eventually results in an oscillatory response at light loads, as in Fig. 7.5a.

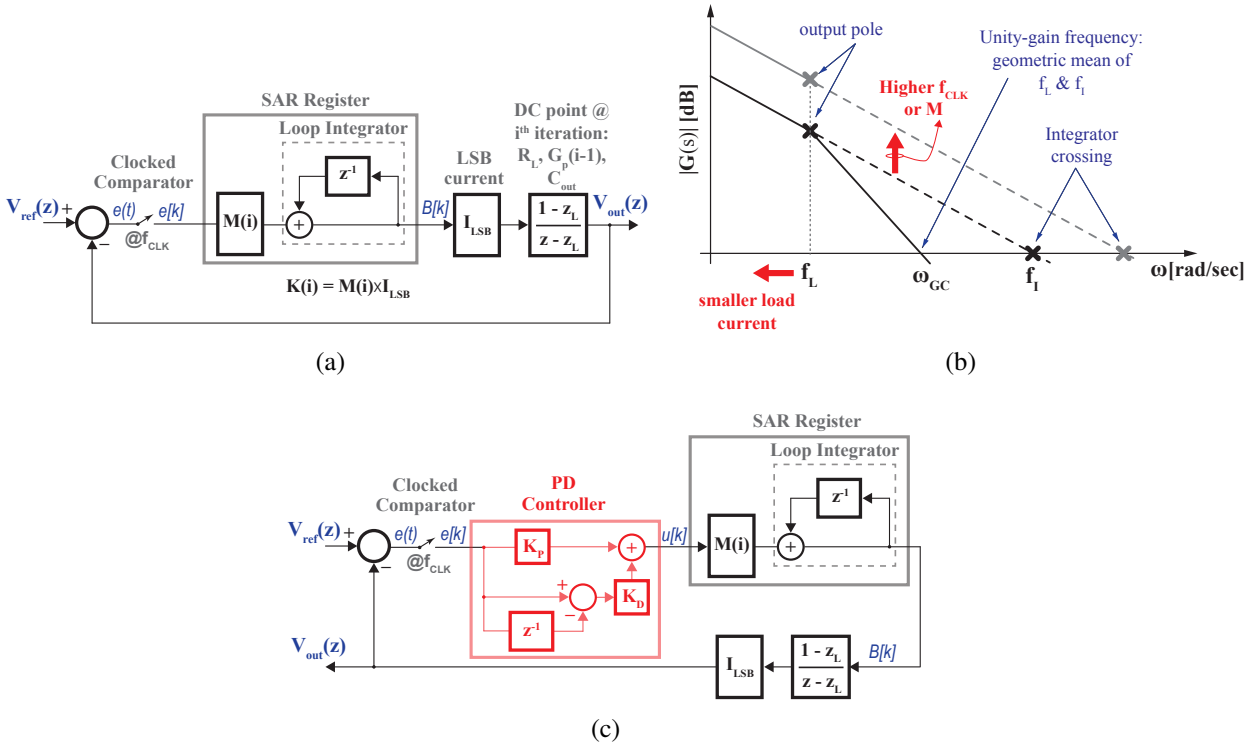


Figure 7.4: RLDO model. (a) Small-signal AC model. (b) Bode diagram. (c) RLDO with PD controller. The SAR controller acts as a variable-gain discrete-time integrator.

In theory, loop stability can be ensured by guaranteeing enough phase margin at each conversion step, i, in the piece-wise linear model. To maintain a fixed integrator asymptote crossing (f_I) and ensure stable operation, f_{CLK} should be linearly reduced, from the LSB stable clock rate, $f_{CLK,LSB}/(N-i+1)$, every iteration i. Unfortunately, in order to avoid significant overshoots and undershoots during the initial SAR conversion steps, f_{CLK} should be scaled *exponentially* the other way around in a binary increasing manner, i.e., $2^i f_{CLK,LSB}$, such that $f_{CLK,MSB}$ at the first iteration is faster than the MSB slew rate, $\text{MSB}\times\Delta V_{drop-out}/C_{out}\times 1/\Delta V_{ov}$, where ΔV_{ov} is the allowed overshoot magnitude, or $1/(2T_R)$, for $\Delta V_{ov}=\Delta V_{droop}$. Therefore, a

DLDO incorporating binary search is inherently unstable, or otherwise, provides an output with unacceptably large overshoots and undershoots.

7.3.2 Adaptive Zero Insertion through Variable-Coefficients PD Compensation

In order to enable a pragmatic SAR-based LDO, a zero is added at f_L to the open-loop transfer function in (7.3) through an adaptive *Proportional-Derivative* compensation scheme, converting the LDO into a first order system.

Proportional Derivative Control Law and Action

Intuitively, the barrel shifter in a linear-search DLDO should ideally be locked once the output voltage reverses the direction of its slope and starts to increase towards V_{ref} (e.g., after turning on three fingers in Fig. 7.6) to avoid overshoot. In other words, the loop integrator should be incremented (+1 state) only when V_{out} has a negative slope (*derivative term*) while V_{out} is less than V_{ref} (*proportional term*). Similarly, the loop integrator should be decremented (-1 state) only when V_{out} is trending upwards, i.e., with a positive slope, while V_{out} is larger than V_{ref}. Otherwise, the loop integrator value should be kept fixed (0 state). This behavior can be described by the control law of the proposed PD compensator as:

$$\textit{if } (V_{out}[k] < V_{ref}) \;\&\; (dV_{out}/dt < 0) \textit{ increment};\;\; \textit{elseif } (V_{out}[k] > V_{ref}) \;\&\; (dV_{out}/dt > 0) \textit{ decrement}; \tag{7.4}$$

The illustrated proportional-term logic in (7.4) can be implemented through the quantized error voltage, $e[k] = (V_{ref} - V_{out}[k])$, which is $+1$ when $V_{ref} > V_{out}$, and -1 when $V_{out} > V_{ref}$. The derivative term logic in (7.4) can be evaluated through the difference $(e[k] - e[k-1])$ which is equivalent to $\Delta V_{out}[k] = (V_{out}[k-1] - V_{out}[k])$. Therefore, the PD control law in (7.4) can be implemented through the addition of the aforementioned two terms as $u[k] = K_P e[k] + K_D \Delta V_{out}[k]$,

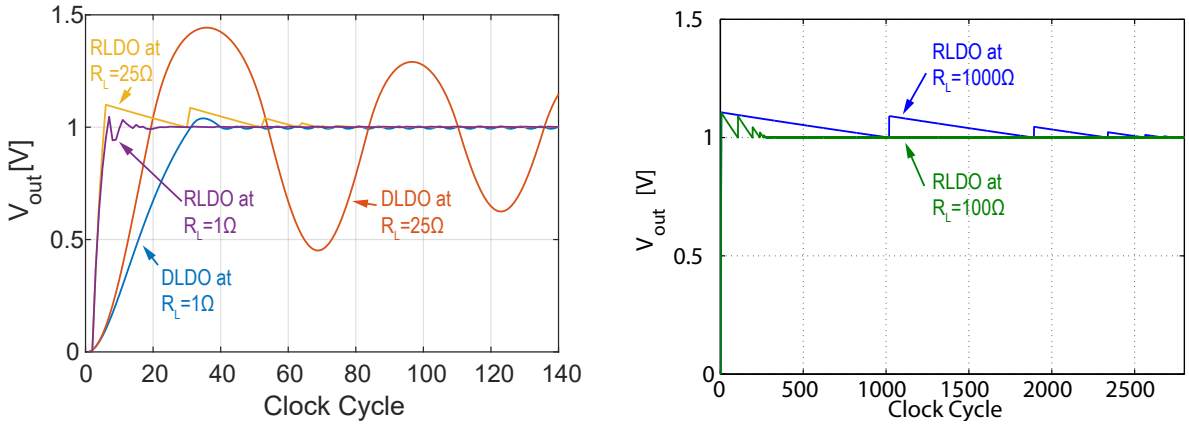


Figure 7.5: (a) Transient V_{out} simulations of a 7-bit RLDO with the proposed PD compensation, and a 7-bit DLDO at peak current $R_L = 1\Omega$ and at light current $R_L = 25\Omega$ (V_{in} =2V, V_{ref} =1V, G =5Ω^{-}1, C_{out} =1/(2π)). (b) Simulations of the PD-compensated RLDO at $R_L = 100\Omega$ and $R_L = 1000\Omega$.

Table 7.1: PD Control Action

P term	D term	PD output
$\frac{1}{2}(V_{ref} - V_{out}[k])^*$	$\frac{1}{2}(V_{out}[k-1] - V_{out}[k])^*$	$u[k]$
+1/2	+1/2	+1
+1/2	-1/2	0
-1/2	+1/2	0
-1/2	-1/2	-1

where $u[k]$ is the PD output that is provided to the loop integrator, (i.e., barrel shifter or SAR register), K_P and K_D are the proportional and derivative coefficients, and $\Delta V_{out}[k]$ is the derivative term. Table 7.1 illustrates the PD output across the possible values of the proportional and derivative terms.

Stability Improvement with PD Compensation

To illustrate the effect of the proposed PD compensation on the LDO frequency response, PD compensation is incorporated in the small-signal model in Fig. 7.4c. Using a backward-difference approximation to the differentiation operator, $de(t)/dt$, the discrete equivalent of a continuous-time PD compensator, $K_P e(t) + K_{D_C} de(t)/dt$, can be found as $K_P e[k] + K_{D_C}(e[k] -$

$e[k-1])/T_{CLK}$. Therefore, the PD compensation inserts a zero at $-K_P/K_{D_C}$ (or $-K_P/K_D \times f_{CLK}$) to the corresponding continuous-time open-loop transfer function in (7.3). Unfortunately, conventional series PD compensators have fixed coefficients (K_P and K_D) at run time. Consequently, the added zero cancels the phase lag of the output pole $f_L = 2\eta\omega_n$ only when $-K_P/K_{D_C}$ is more dominant than f_L (high currents) , limiting the achievable I_L dynamic range. On the other hand, in this work, each P and D term is individually quantized before the addition, enabling adaptation of the inserted zero with the output pole while ensuring the P and D terms have equal weights in the final output.

To illustrate the difference in the control action between the proposed and the conventional PD compensator, consider the case when V_{out} is much less than V_{ref}, yet is slowly approaching V_{ref}. In this case, the conventional PD outputs $+1$, since the D term, $\Delta V_{out}[k]$, is negative with a magnitude much less than the positive P term, $(V_{ref} - V_{out}[k])$. On the other hand, the proposed PD output is zero, since the P and D terms are quantized individually before the addition, and hence the P term is $+1$ while the quantized D term is -1.

To account for the quantization effect, an input, $e[k]$, dependent quantization gain is added to the P and D coefficients such that $K_P = k_p \times k_{Qp}(e[k])$ where $|k_{Qp} \times e[k]|$ is 1, and similarly, $K_D = k_d \times k_{Qd}(e[k])$ where $|k_{Qd} \times \Delta e[k]|$ is 1. Therefore, k_{Qp} is simply $1/|v_{out}[k]|$, where V_{ref} is set to zero under small-signal operation. The D-term difference $e[k] - e[k-1]$ can be evaluated by $(V_{out}[k-1] - V_{out}[k])$ which is equivalent to $(G_p(i) + G_L)v_{out}[k]/C_{out} \times T_{CLK}$ or essentially $f_L/f_{CLK} \times v_{out}[k]$, for sufficiently small values of T_{CLK}. Therefore, the D-term quantization gain k_{Qd} becomes $f_{CLK}/(f_L v_{out}[k])$ so that $|k_{Qd} \times \Delta e[k]|$ is 1. Consequently, the resulting zero $-K_P/K_{D_C}$ in (7.3) becomes $-f_L$, which perfectly cancels the output pole and enables a single-pole system with phase margin of 90^o, as shown in in Fig. 7.4b, irrespective of C_{out}, R_L, $M(i)$, and f_{CLK}. Figure 7.5b verifies the proposed PD compensation efficacy in realizing stable operation irrespective of I_L. In summary, inclusion of the third idle state effectively implements cycle-skipping and adapts the rate at which the integrator updates its value, $f_c = f_{CLK}/m$ for integer m,

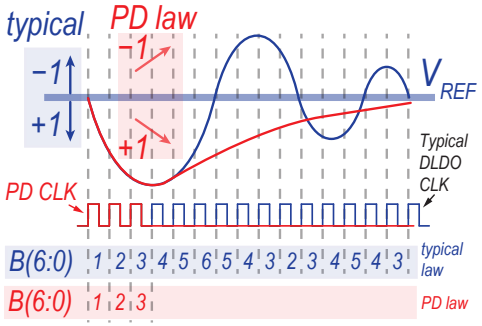


Figure 7.6: DLDO transient V_{out} response with and without the proposed PD compensator.

with the output rate, f_L, to maintain the output pole, e^{-f_L/f_c}, inside the unity circle.

7.4 Sub-LSB Hysteretic PWM Control

7.4.1 Minimum Current Limit of Linear-Search Based DLDOs

DC Accuracy Limitation

In a linear-search DLDO, limit cycling modulates the duty-cycle of the n oscillating fingers at $f_{CLK}/(2n)$ to maintain the average V_{out} close to V_{ref}. Unfortunately, such duty-cycle modulation fails to provide the desired V_{out} level, as the current of cycling on/off LSBs becomes comparable to I_L and hence gives a more pronounced V_{out} steady-state error, especially at large drop-out voltages. For instance, in a 7-bit barrel-based DLDO, the steady-state error exceeds $\pm 1\%$ V_{ref} when I_L is $2^{2.6}$ below $I_{L,max}$ for $V_{ref} = V_{in}/2$ (Fig. 7.7a).

V_{out} Peak-to-Peak Ripple Limitation

Limit-cycle oscillations result in an output voltage ripple, $\Delta V_{out,p-p}$, proportional to the number of limit-cycling fingers, n. As I_L is reduced, the output peak-to-peak ripple increases since the effect of the limit-cycling fingers on V_{out} is more pronounced at lighter loads, as illustrated in Fig. 7.7b. $\Delta V_{out,p-p}$ can be reduced by increasing the DLDO operating frequency, f_{CLK}, and

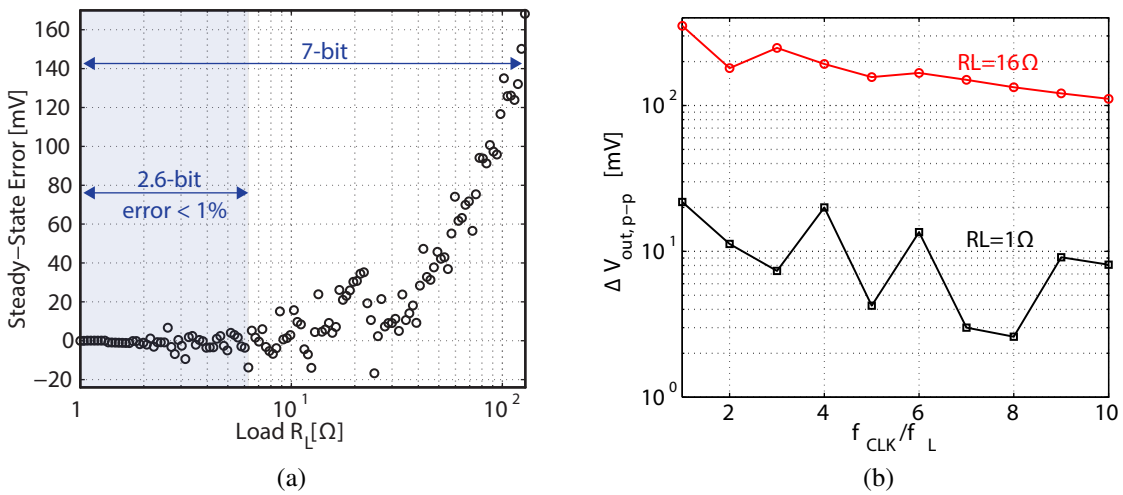


Figure 7.7: Setting-limits of digital LDOs minimum current. (a) Simulated steady-state error versus R_L at $f_{CLK} = 10 \times f_L$ and (b) simulated steady-state V_{out} ripple $\Delta V_{out,p-p}$ versus f_{CLK}/f_L of a 7-bit shifter-based DLDO with $V_{ref} = V_{in}/2$.

hence the DLDO output ripple frequency $f_{CLK}/(2n)$, beyond the output RC network corner f_L, as in Fig. 7.7b. Unfortunately, the higher f_{CLK} results in a lower damping factor η and eventually an oscillatory response, as discussed in section 7.3.1. For a 7-bit DLDO, when $V_{ref} = 0.9V_{in}$, the load current range with a peak-to-peak ripple below 50mV is limited to $2^{6.7}$.

Therefore, the LDO minimum I_L is typically limited by the acceptable steady-state error level, at large $\Delta V_{drop-out}$, and the allowable output voltage ripple, at small $\Delta V_{drop-out}$, of the limit-cycling LSB(s), and hence the resolution N, which determines both, defines the achievable dynamic range $I_{L,max}/I_{L,min}$. Unfortunately, increasing the resolution N comes with a worse transient FOM, as in Fig. 7.3.

7.4.2 Minimum Current Limit in a Binary-Search DLDO

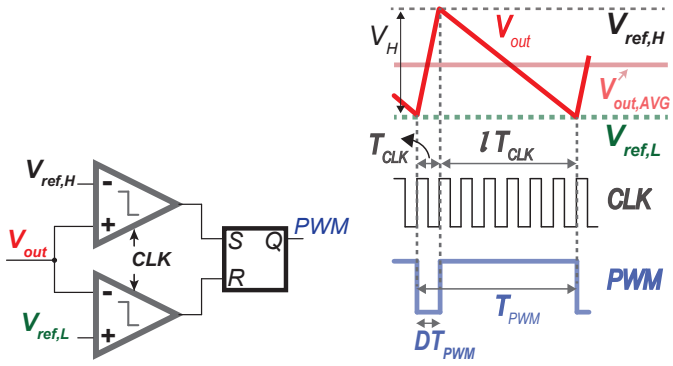
On the other hand, after the SAR conversion, V_{out} becomes within one $I_L \times$LSB of the desired target, V_{ref}. Since the RLDO does not exhibit limit-cycle oscillations, the PMOS array conductance G_p converges to $G_{ref} \pm$LSB at steady-state, where G_{ref} is the PMOS conductance

that makes V_{out} matches V_{ref} and the final V_{out} value is $V_{in} \times G_p/(G_p + G_L)$. As a result, the worst-case error becomes $\sim \pm \frac{\text{LSB}}{G_L(1+G_{ref}/G_L)} \times V_{in}$ or $\pm \frac{\text{LSB}}{G_L} \Delta V_{drop-out}$. As the load current, G_L, is reduced or $\Delta V_{drop-out}$ is increased, the worst-case steady-state error increases. Therefore, the load dynamic range $I_{L,max}/I_{L,min}$ with certain error$-\%$ becomes limited to: error$-\% \times 2^N$; e.g. $(N-6.6)$ bits range for a $\pm 1\%$ V_{ref} error. Therefore, the second challenge of the SAR LDO architecture, after its inherent instability (Section 7.3), is the limited DC accuracy that made such SAR architecture previously impractical.

7.4.3 Hysteretic PWM Control

To mitigate the accuracy problem as well as enable sub-LSB I_L regulation, a redundant LSB switch is employed while the duty-ratio, D, of its gate voltage is modulated like a lossy switched-mode buck converter. Instead of the periodic 10-70mV ripple encountered during limit-cycling in prior DLDOs [125], a dual-bound ($V_{ref,H}$, $V_{ref,L}$) hysteretic PWM controller is used to generate the redundant LSB drive signal. Once the SAR controller brings V_{out} to within the hysteretic window, the SAR controller is clock-gated and the PWM control is enabled. Here, the same SAR P-term comparators are reused, as will be discussed, to set or reset an SR latch that provides the gate voltage, *PWM*, of the redundant LSB, as in Fig. 7.8.

The average output value of a dual-bound hysteretic PWM control scheme is half of the hysteresis height, $V_H/2$, as in Fig. 7.8b. Therefore, the steady-state error in a DLDO can be eliminated by setting the hysteresis bounds at $V_{ref,H} = V_{ref} + V_H/2$ and $V_{ref,L} = V_{ref} - V_H/2$, under a high sampling rate. Furthermore, at light loads, the minimum current supplied by the DLDO can go below the LSB finger current by $I_{sub-LSB} = \frac{1}{l+1} I_{LSB}$ (7.8b), with zero steady-state error and without the ripple exceeding V_H, unlike limit-cycle oscillation. Therefore, the achievable effective-LSB, and thus the dynamic range, is extended by $log_2(l+1)$ bits. The PWM controller also limits the cycling switches to only a single PMOS finger which reduces the steady-state quiescent power.



(a) (b)

Figure 7.8: Hysteretic dual-bound controller. (a) Top-level schematic. (b) Operation.

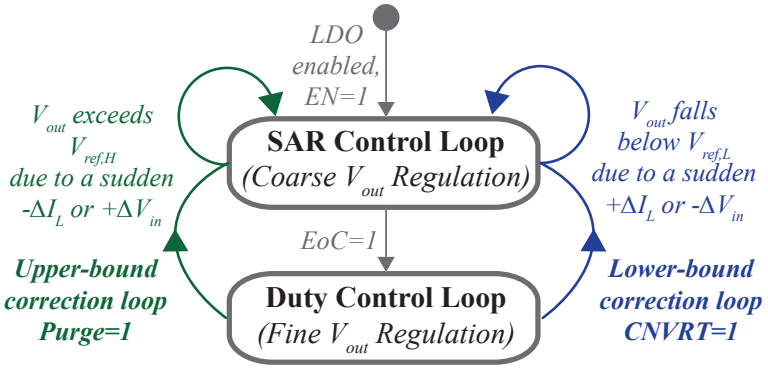


Figure 7.9: Top-level state diagram of the proposed RLDO.

7.5 Circuit Implementation

The proposed RLDO incorporates the three techniques discussed above: SAR switching, adaptive PD compensation, and sub-LSB PWM control. As shown in Fig. 7.9, once the RLDO is enabled (*EN*=1), the SAR control loop is initiated and the number of turned-on PMOS fingers is adjusted to coarsely set V_{out} to V_{ref}. Once *EoC* is asserted, the duty-cycle controller is enabled to perform sub-LSB fine regulation. If, during duty-control or SAR conversion steps, a sudden load-current ΔI_L or input-voltage ΔV_{in} step occurs that knocks V_{out} outside the control hysteresis, upper- and lower-bound correction logic restarts the SAR operation by asserting *CNV*.

Table 7.2: Truth table of PD compensator

From Block Diagram	Logic Inputs		Logic Outputs	
u[k]	e^*	ΔV^*_{out}	*INC*	*DEC*
+1	1	1	CLK	0
0	1	0	0	0
0	0	1	0	0
-1	0	0	0	CLK

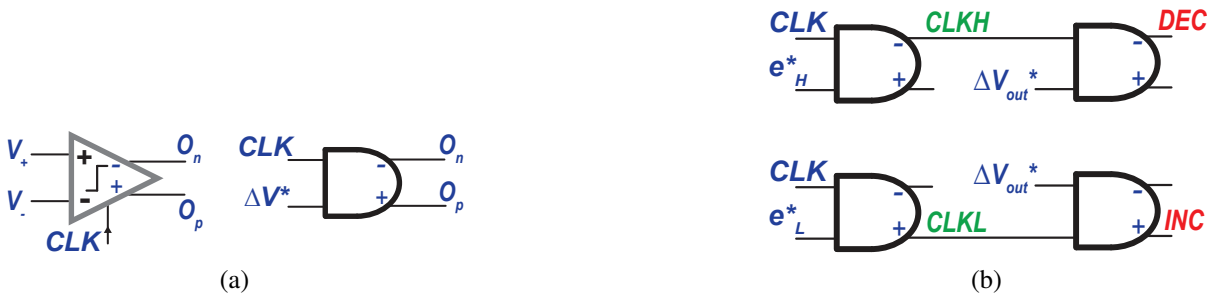


Figure 7.10: Quantized gate-level implementation. (a) Equivalence of a clocked comparator to a quantized AND gate. (b) Quantized gate-level implementation of the PD compensator truth table in table 7.2.

7.5.1 Proportional-Derivative Compensator Implementation

The PD compensator output can take on one of three values, either +1, -1, or 0; thus, two variables, *INC* and *DEC*, are used to represent the PD output state. Table 7.2 illustrates the relationship of these variables when K_P and K_D are set to 1/2. The *INC* and *DEC* signals are not static signals that take on a fixed value but rather act as pulsed signals, since they are used as clock inputs to the SAR logic in the RLDO.

A clocked sense amplifier can be considered as a differential *quantized* AND gate, as in Fig. 7.10a. Thus, when the quantized difference $\Delta V^* = \left[V_+ - V_-\right]^*$ between the input analog signals is 1, the sampling clock propagates through the positive output O_p of the proposed gate and vice versa for the negative output O_n. Figure 7.10b illustrates the quantized gate-level implementation of the truth table of the PD compensator, where $e^*_x[k]$ represents the quantized error $\left[V_{ref,x} - V_{out}[k]\right]^*$. The PD essentially acts as an XNOR gate, where it gives a true (pulsing)

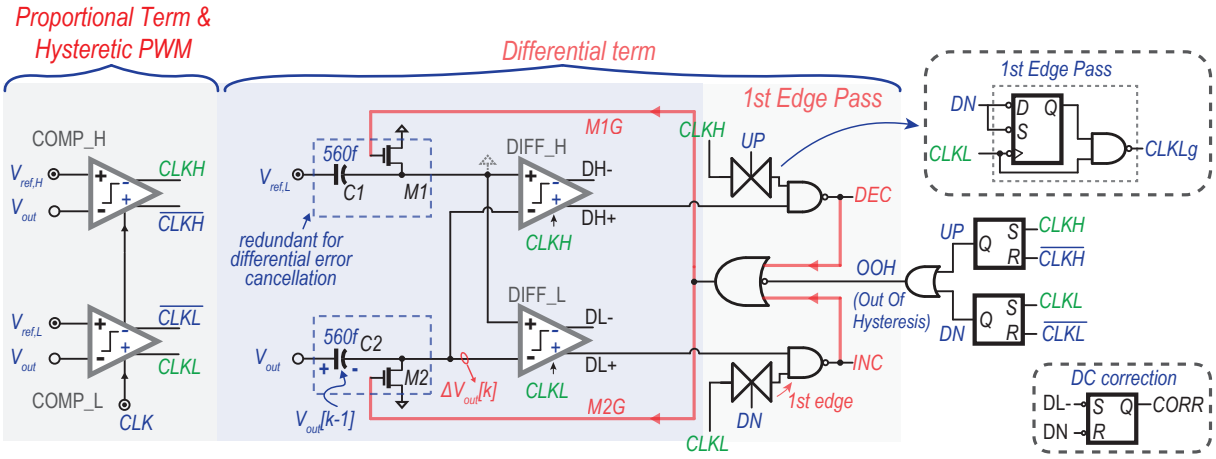


Figure 7.11: Top-level schematic of the implemented PD compensator, including PWM comparators, derivative-term comparators, and bottom-plate sampling circuitry. Insets illustrate the *1st edge pass* and *DC correction* logic.

output when the number of true inputs is even as shown in Table 7.2.

The schematic of the implemented PD compensator is shown in Fig. 7.11. The two *PWM* comparators, $COMP_H$ and $COMP_L$, implement the proportional term and thus provide the quantized errors $\left[V_{ref,H} - V_{out}[k]\right]^*$ and $\left[V_{ref,L} - V_{out}[k]\right]^*$, respectively. They establish a hysteresis where all the RLDO circuitry is disabled for minimal I_Q and V_{out} comes to a halt. The comparators $DIFF_H$ and $DIFF_L$ implement the differential term $\Delta V^*_{out}[k]$.

The derivative term $(V_{out}[k-1] - V_{out}[k])$ of the PD compensator is implemented through the bottom-plate sampling circuit illustrated in Fig. 7.11 comprised of a footer NMOS switch and a 560fF sampling capacitor. When the sampling clock *M2G* is high, the value of V_{out} is stored across the sampling capacitor. When *M2G* is low, the voltage of the negative comparator terminal becomes the difference term $(V_{out}[k] - V_{out}[k-1])$. The difference is then compared to a virtual ground through the comparators $DIFF_H$ and $DIFF_L$ to produce the quantized difference term $\left[V_{out}[k-1] - V_{out}[k]\right]^*$. A replica sample-and-hold circuit is employed to sample $V_{ref,L}$ ($\approx V_{out}$) in order to establish a virtual ground at the positive terminal of the comparators, so that errors due to charge-injection, clock feed-through, or comparator kickback noise are canceled via the inherent symmetry. The sampling switches M1 and M2 in Fig. 7.11 are enabled from

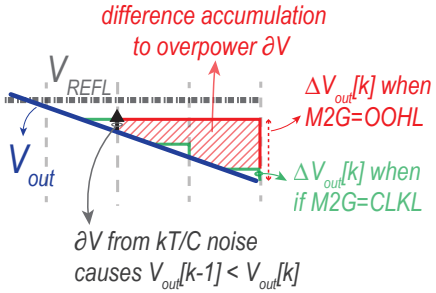


Figure 7.12: Difference accumulation to overpower KT/C noise due to a small sampling capacitor size.

INC and *DEC* instead of *CLKL* and *CLKH* so that the difference ΔV_{out} accumulates and becomes $(V_{out}[k] - V_{out}[k-m])$. Therefore, if an erroneous $DIFF_H$ or $DIFF_L$ comparison results due to kT/C noise, the difference increases until it overpowers this error, as shown in Fig. 7.12.

When V_{out} is within hysteresis, *OOH* is reset low through the two SR latches in Fig. 7.11. Thus, the footer NMOS sampling switches are statically enabled through the OR gate that propagates the complement of *OOH* to the sampling switch gate in Fig. 7.11. Once V_{out} is outside hysteresis, the rising edge of the first clock pulse *CLKL* or *CLKH* might trigger the comparators $DIFF_L$ and $DIFF_H$ when the difference $(V_{out}[k] - V_{out}[k-1])$ is small, and hence the comparison result becomes stochastic. As a result, a clock pulse might be lost, which would increase the RLDO response-time. To prevent this, the *first edge pass* logic in Fig. 7.11 allows the first clock pulse *CLKL* (*CLKH*) to pass directly to *INC* (*DEC*) irrespective of the $DIFF_L$ ($DIFF_H$) comparison result.

7.5.2 Regulation-Loop Interruption Logic

Lower-Bound Correction Loop

During duty-control, the redundant LSB current can fail to bring the output voltage above $V_{ref,L}$ if a large load-current increase $+\Delta I_L$ or a large input-voltage decrease $-\Delta V_{in}$ occurs. Therefore, lower-bound trigger logic is employed to restart the SAR search with the MSB,

$B(6)$, on and the remaining PMOS transistors off, by asserting CNV_D, created by AND-ing the redundant LSB gate signal, *PWM*, and *INC*[2]. In the worst-case, the lower-bound trigger logic takes two clock cycles to turn on the MSB switch, and hence the clock frequency is set by the required response-time as: $f_{CLK} > 2/T_R$.

To avoid artificial undershoots that may be introduced if a large $+I_L$ or $-V_{in}$ step change occurs in the middle of the SAR conversion steps after deciding the first few MSBs, a branch-prediction scheme[3] is implemented. As in Fig. 7.13a, when two consecutive *INC* edges result without any *DEC* assertion in-between during the SAR bit-cycling, the branch-prediction logic predicts that there is a disturbance, $+\Delta I_L$ or $-\Delta V_{in}$, that is large in amplitude, and therefore, the remaining unchecked l bits in the switch array may not be able to compensate for this disturbance. To verify this, the branch-prediction logic temporarily enables the remaining unchecked l bits in the SAR register by asserting *ON*, as in Fig. 7.16a where $B(2:0)$ and PWM LSB $B(-1)$ are temporarily enabled. If V_{out} exceeds $V_{ref,H}$ (i.e., *DEC*=1), then the present disturbance, $+\Delta I_L$ or $-\Delta V_{in}$, can be successfully accounted for through the remaining l bits and the SAR operation can be continued as normal. This is similar to a *branch-not-taken* in pipeline hazards terminology. Otherwise, if V_{out} is still slewing downwards below $V_{ref,L}$ despite the l bits being turned-on, then the SAR search should be restarted. This is equivalent to a *branch-taken* in pipeline design. Here, a third *INC* edge results although the l bits are turned-on, and hence the branch-prediction logic restarts the SAR search operation at $B[k] = 7'b0111111$ ($B(6)$ is on) by asserting CNV_{SAR}, as in Fig 7.16a.

Branch prediction is implemented using a 3-bit sequence detector, as in Fig. 7.13b. The *Moore* state-machine asserts its outputs, *ON*=1 and CNV_{SAR}=1, when it recognizes two and three *INC* edges in succession, respectively. The state-machine resets to its initial state when a *DEC* edge results. As shown in the inset in Fig. 7.13b, a 2-input multiplexer is used to select the

[2] *INC* pulse is produced by passing *CLKL* through *first edge pass* logic, during *PWM* control.

[3] The proposed scheme is similar to branch-prediction solutions that avoid CPU pipeline hazards in computer architecture.

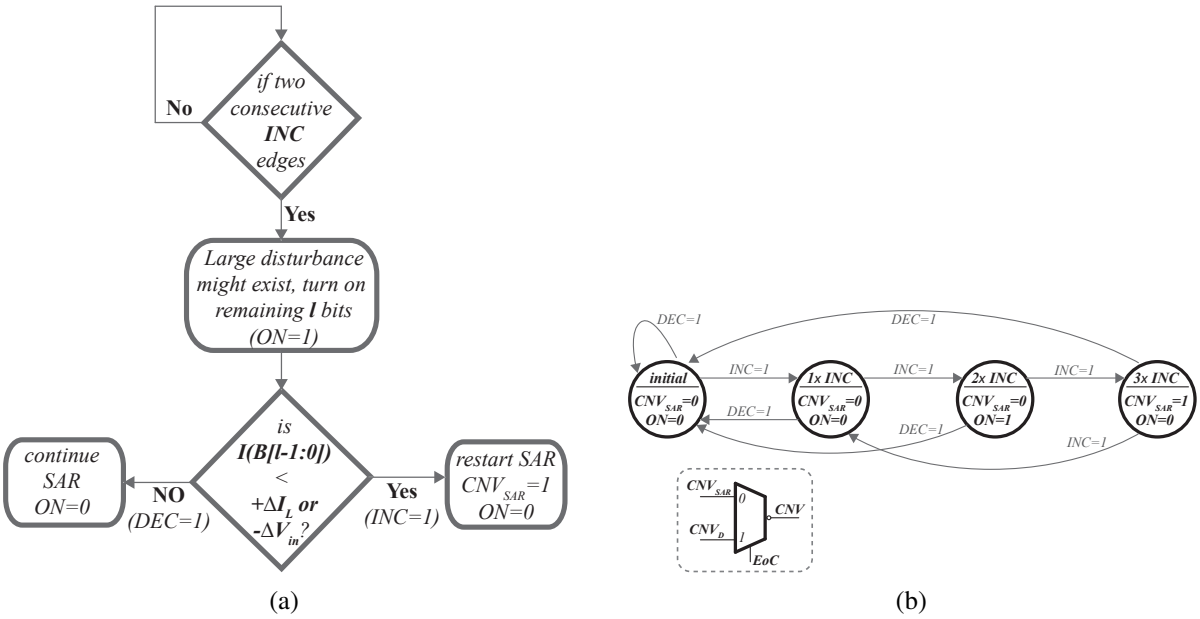


Figure 7.13: Proposed branch-prediction (a) flowchart and (b) state-diagram implementation. Inset: the SAR reset *CNV* selection based on *EoC* through an output multiplexer.

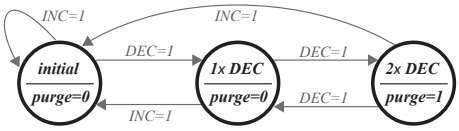


Figure 7.14: State-diagram implementation of the upper bound.

complement of either CNV_D or CNV_{SAR} as the SAR controller restart signal, *CNV*, based on the present active control loop, as determined by *EoC*.

Upper-Bound Correction Loop

During duty control, a large disturbance can make the output voltage exceed $V_{ref,H}$, even though the redundant LSB is turned off. Similarly, in the middle of the N-step SAR conversion, a sudden $-\Delta I_L$ or $+\Delta V_{in}$ can result in increasing V_{out} above $V_{ref,H}$, (i.e., overshoot), despite the turn-off of the last determined bit during SAR bit-cycling. This indicates that the already determined bits, e.g. $B(6:3)$ in Fig. 7.16b, hold the wrong value due to the unaccounted $-\Delta I_L$ or $+\Delta V_{in}$ disturbance. Such interruptions during SAR control (or PWM) should be corrected by

disabling all the switch-array PMOS fingers immediately instead of wasting time investigating the remaining bits (e.g., $B(2:0)$ in Fig. 7.16b), and increasing the V_{out} overshoot. The proposed lower-bound trigger logic is implemented through a 2-bit sequence detector, as shown in Fig. 7.14. The sequence detector asserts its output, *purge*, when two *DEC* edges occur in succession, as in Fig. 7.16b when turning off $B(3)$ is not enough to stop overshooting. On the other hand, the *Moore* machine resets to its initial state when an *INC* edge occurs. After turning off the whole PMOS switch array through the activated *purge*, the lower-bound logic restarts the SAR search operation when the output voltage, V_{out}, falls below $V_{ref,L}$ due to any $+\Delta I_L$ or $-\Delta V_{in}$ disturbance, as in Fig. 7.16b when the PWM LSB $B(-1)$ is not enough to supply the required I_L.

DC Correction Loop

PD compensation has the disadvantage that it can reduce the steady-state DC accuracy. During binary search, the PMOS DAC array is sequentially turned on, starting from the MSB, until V_{out} reverses the direction of its slope and starts to increase towards the hysteresis window after turning on *B(i)*. Since the PMOS array current depends on the drop-out voltage, as V_{out} increases, the current of the PMOS array, including the last turned-on finger *B(i)*, decreases and V_{out} can get stuck below $V_{ref,L}$ without reaching the hysteresis window.

In order to avoid such case, the next MSB switch *B(i-1)* is turned on, as an extra *safety step*, although the present bit, *B(i)*, is enough to charge V_{out} towards the hysteresis. When V_{out} is less than $V_{ref,L}$ and is increasing, the sampling clock propagates to the negative output of $DIFF_L$, $DL-$, in Fig. 7.11, which is employed to set a DC correction flag *CORR*. As a result, the next MSB in the switch array, *B(i-1)*, is temporarily turned on to provide an extra half-*B(i)* conductance in parallel to the present investigated bit, *B(i)*, to ensure the rapid increase of V_{out} towards $V_{ref,L}$ and hence avoid any possible condition of V_{out} being stuck below $V_{ref,L}$. Once V_{out} exceeds $V_{ref,L}$, *DN* in Fig. 7.11 is reset low which clears the DC correction flag *CORR*, and hence, the temporarily turned-on bit is turned back off. For instance, in Fig. 7.16a, $B(3)$ is turned

```
// initially B=7'b1111111 and i=6
BinarySearch(B(6:0),i)

  turn on B(i); //perturb phase

  //observe phase
  if (posedge DEC)
       turn off B(i);

  if (posedge INC)
     keep B(i) on;
     if i=0
       return;
     else
       return BinarySearch(B,i-1);
```

Figure 7.15: SAR backbone pseudo code.

on immediately at the next rising clock edge, via *CORR*, until V_{out} exceeds $V_{ref,L}$. A similar architecture can follow to avoid the case of V_{out} being stuck above $V_{ref,H}$.

7.5.3 Successive Approximation Controller

The RLDO's SAR logic follows a perturb-and-observe algorithm to determine the value of each bit in the PMOS switch array (Fig. 7.15). In the perturb phase, one bit in the switch array is turned on in order to test its output current value in comparison to the load current I_L. In the observe phase, the comparison result of the output voltage V_{out} with the desired target V_{ref} determines the value of the binary bit being tested through *DEC* and *INC*, coming from the PD controller to avoid oscillatory response as discussed. If V_{out} exceeds V_{ref} due to the present bit output current, *DEC* is set high, and the present bit under test is turned off. Otherwise, if V_{out} falls below V_{ref}, *INC* transitions from 0 to 1, and the present bit being tested is left on and the conversion process proceeds to the next MSB until all the bits in the switch array have been determined. Figure 7.16 shows a simulated timing diagram and response of two representative load steps.

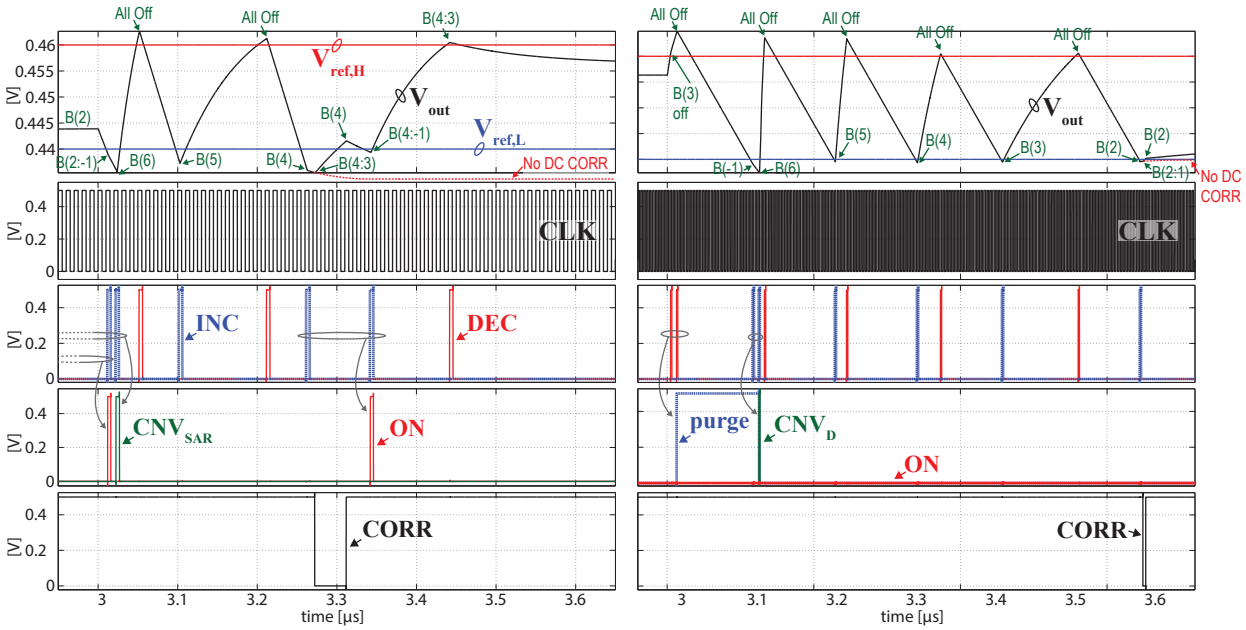


Figure 7.16: The RLDO simulated response to a periodic load swing between 40μA and 200μA within 200ps, V_{in}=0.5V, V_{ref}=0.45V, C_{out}=0.4nF, and f_{CLK}=100MHz.

7.6 Experimental Verification

A 7-bit RLDO was implemented in 0.0023 mm^2 in 65nm CMOS, including the PMOS DAC array, SAR control logic, comparators, sample and hold circuits, an on-chip load, and 0.4 nF on-chip decoupling capacitance (Fig. 7.17).

7.6.1 Transient Measurements

Mitigating the Speed-Stability Challenge in SAR LDOs

Taking SAR decisions at a faster rate than the rate of change of V_{out} (i.e., f_L) in the hope of reducing the large staircase overshoots and undershoots of binary search results in erroneous successive decisions during the SAR conversion and hence an unstable response. Figure 7.18 illustrates reliable SAR convergence despite employing a much faster clock frequency, 100MHz, than the output time constant, 411.64μs, thanks to the proposed PD compensation. Here, when I_L

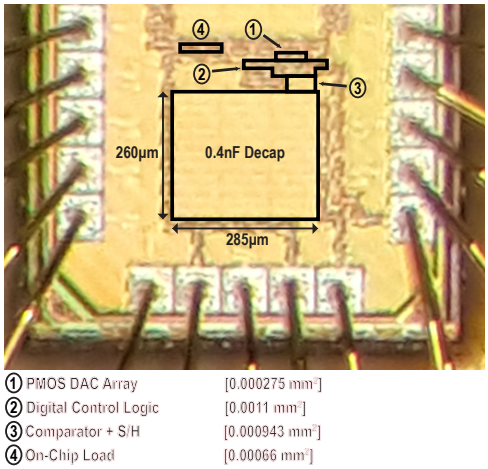


Figure 7.17: Die photo of fabricated RLDO.

is 40μA, the PWM controller tries to maintain V_{out} at V_{ref}. On the other hand, when I_L increases to 1.1mA, V_{out} starts to discharge downwards until it falls below $V_{ref,L}$ (Fig. 7.18 inset). As a result, the lower-bound trigger logic restarts the coarse binary search with $B(6)$ on and the remaining PMOS transistors off, and hence V_{out} rapidly increases until it exceeds $V_{ref,H}$. At that moment, *DEC* is activated to turn off $B(6)$ and V_{out} discharges until it reaches $V_{ref,L}$, and then binary search continues in a similar manner. The measured duration between the turn-on of the successive PMOS DAC switches is approximately 50μs, 60μs, 80μs, and 100μs, as in Fig. 7.18. Therefore, although V_{out} is sampled and observed at a high rate (100MHz) to reduce overshoots/undershoots, the SAR register is updated only at a rate close to the output time-constant, which enables stable operation. On the other hand, if the input 100MHz clock instead directly ran the SAR register, $B(6)$ would be left on since V_{out} does not exceed $V_{ref,H}$ in the following clock cycle (and rather takes $\sim$ 2μs to reach $V_{ref,H}$). This would result in an erroneous $B(6)$ decision, and the SAR operation would never converge. As shown in Fig. 7.18, V_{out} increases with binary-weighted slew rates across the successive iterations. When the SAR controller turns on $B(2)$, V_{out} settles to within the hysteresis window, and hence $B(2)$ can provide the required I_L ($I_{LSB} \sim 275\mu$A). As shown, the RLDO reaches a complete halt-state at steady-state with minimal quiescent power, where the SAR and PWM controllers are gated off. To realize below $\pm 4\%$ steady-state error, the

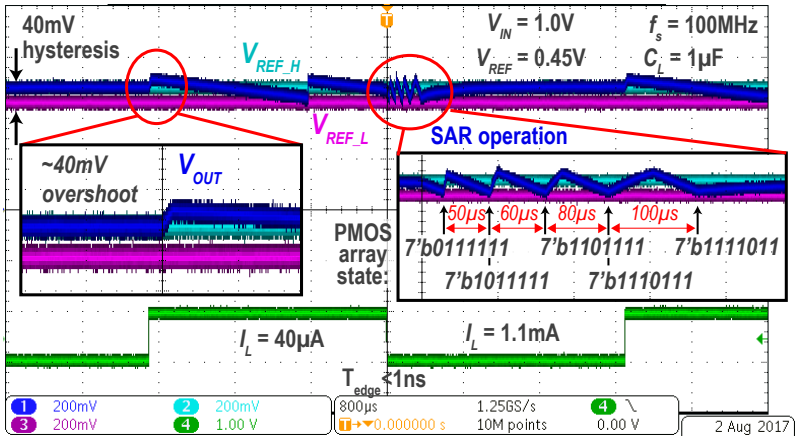


Figure 7.18: Measured transient response of the RLDO to periodic square-wave load current variation with V_{IN}=1V, V_{OUT}=0.45V, and C_{out}=1μF,.

PWM controller can be enabled once V_{out} is within the hysteresis.

The correct SAR-loop conversion is further verified at all possible I_L and V_{in} values via the measured load and line regulation plots in Fig. 7.21. Thanks to the PD compensation and DC correction loop, the LDO is able to make the correct successive decisions and reach the target V_{ref} even while employing high speed clocks ranging between 10MHz and 100MHz, all without getting stuck outside the hysteresis.

Exponential Improvement in FoM via Binary Search

Figure 7.19 shows the measured transient response of the RLDO for periodic (at 1kHz) on-chip load changes between 40μA and 1.1mA with 1ns rise/fall time. The RLDO at $V_{in} = 0.5$V maintains less than 40mV undershoot below V_{ref}=0.45V (not $V_{ref,L}$), for a quiescent current of 14μA at a clock frequency of 100MHz, thereby achieving a response time of 15.1ns and a settling time of 100ns. After the I_L step increase, the SAR operation is restarted with $B(6)$ on and the remaining bits off. For a $\Delta V_{drop-out}$ of $\sim$ 90mV, the MSB current is $\sim$ 845μA. Therefore, $B(6)$ slows down the V_{out} discharge rate until the following clock edge, after 10ns, when $B(5)$ is turned on, which reverses V_{out} direction and brings V_{out} back to within the hysteresis, and hence T_R is ideally 10ns. In contrast, a modeled 65nm shifter-based linear search DLDO with the same fan-out

capability provides 25× ($> 2^N/N$) and 13.7× slower T_R and T_S, respectively, while consuming $2^7\times$ the quiescent current. Thus, the RLDO achieves a FOM of 199.4ps at V_{IN}=0.5V, while the modeled 65nm DLDO achieves 638ns, illustrating higher than $2^{2N}/N$ FOM improvement as predicted from theory. The RLDO's measured overshoot is 62mV which demonstrates the effectiveness of the proposed upper-bound trigger logic to disable the PMOS switches of $B(6:5)$ immediately rather than waiting to check the remaining bits $B(4:0)$, after 1.1mA-to-40μA change. Afterwards, V_{out} is regulated by the duty controller to its steady-state value of 0.45V.

PD Compensation Efficacy

Figure 7.19 also shows the efficacy of the proposed PD compensation scheme − stable load step tests were performed even with a 1μF external capacitor to make the output pole, f_L, 2500× more dominant than f_{CLK} = 100MHz, which would render a baseline DLDO fully oscillatory. As shown in Fig. 7.19, the well-behaved first-order-like V_{out} response confirms the elimination of the integrator pole from the loop dynamics, as predicted from the theory in Section 7.3, thereby realizing a single pole system, and hence achieving stable operation irrespective of C_{out}, I_L, and conductance step M.

7.6.2 Steady-State Measurements

Mitigating Limited DC Accuracy in SAR DLDOs

Figure 7.20 demonstrates the efficacy of the PWM controller. At a current 20× less than I_{LSB} ($\approx 20\mu$A at $\Delta V_{drop-out} = 0.2$V), the PWM controller regulates V_{out} with $<0.2\%V_{ref}$ steady-state error (20.3-bit), all with I_L-independent peak-to-peak ripple of 20mV. Figure 7.21 demonstrates that the proposed PWM control mitigates the challenge of limited current range with acceptable DC accuracy in binary-search DLDOs, and in fact achieves load regulation with less than $\pm 2\%V_{in}$ steady-state error for a hysteresis window of ±10mV across a 20,000×

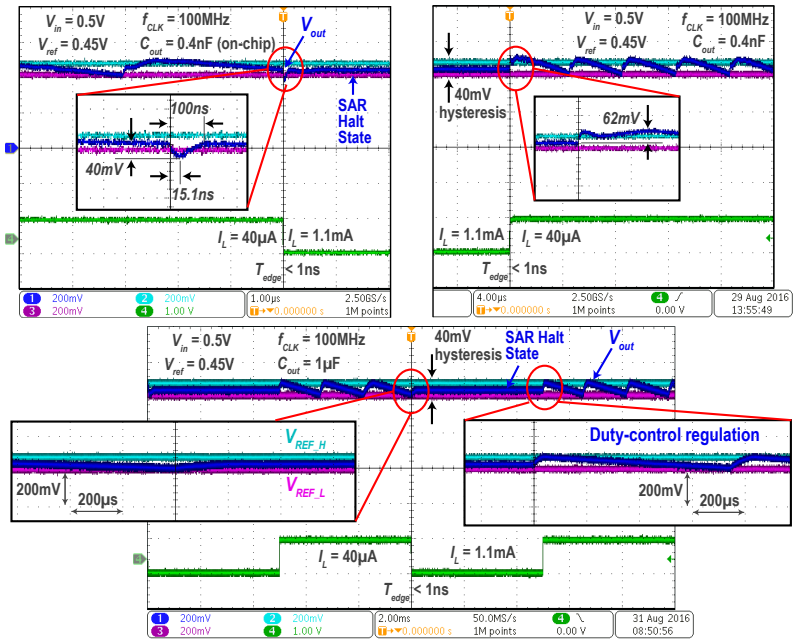


Figure 7.19: Measured transient response of the RLDO to a periodic square-wave load current variation with V_{IN}=0.5V, V_{OUT}=0.45V, and C_{out}=0.4nF (top). When C_{out} =1μF, the RLDO remains stable during periodic positive and negative load steps (bottom).

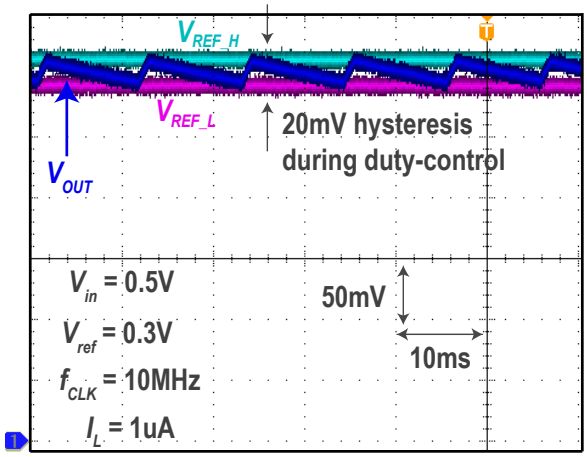
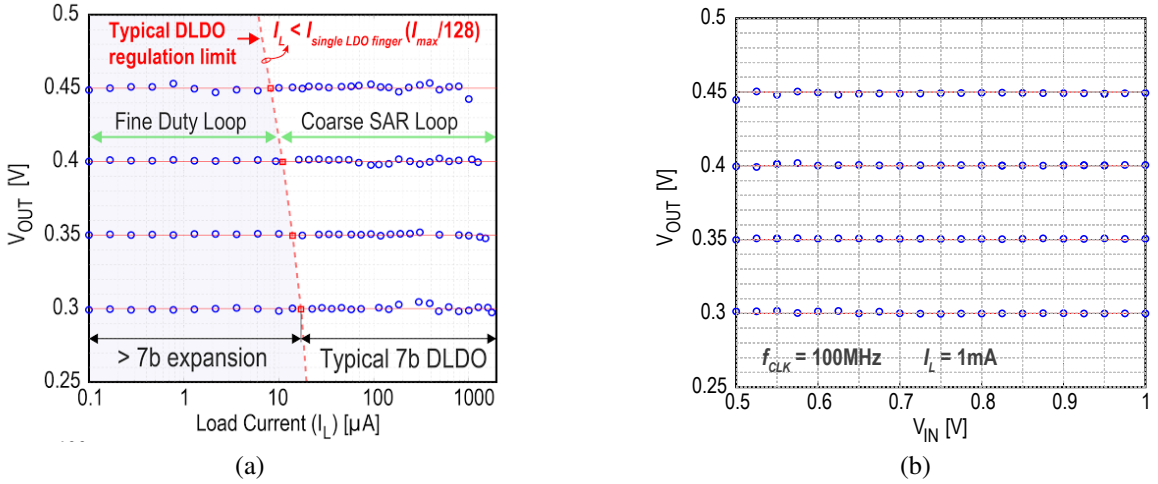


Figure 7.20: Measurement of output voltage ripple during PWM duty control.

load dynamic range (14.3-bit: from 100nA to 2mA). Without PWM control, the dynamic range would be limited to 2.64× (1.4-bit). In this design, the PWM controller is only enabled after the SAR fully converge and not within the intermediate iterations, which trades accuracy for power. Therefore, for $I_L > I_{LSB}$, the PWM controller may or may not be enabled depending on whether



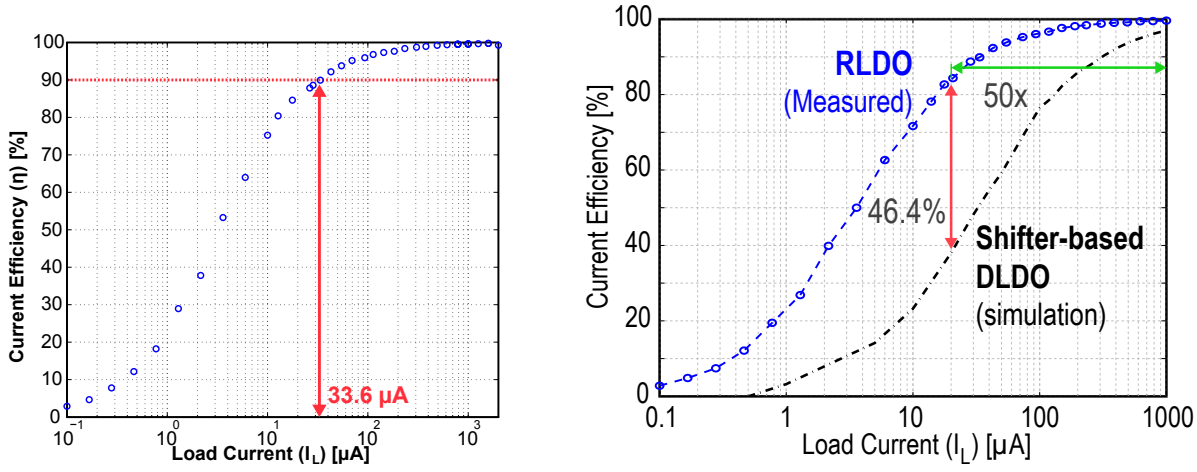
(a) (b)

Figure 7.21: (a) Line regulation measurement at a clock frequency of 100MHz and a load current of 1mA. (b) Load regulation measurement at f_{CLK}=10MHz and V_{in}=0.5V.

the SAR-halt-V_{out}-value resides within the target hysteresis or not. This enables $< \pm 2\% V_{ref}$ and $< 0.6\% V_{ref}$ steady-state error when the PWM is disabled and enabled, respectively, as in Fig. 7.21a. For $I_L < I_{LSB}$, the PWM controller is always enabled, and hence the steady-state error is $< \pm 0.6\%$, even when $V_{ref} \sim V_{in}/2$, as shown in Fig. 7.21a. In a non-PWM-modulated 7-bit DLDO, the minimum supplied current cannot go below I_{LSB} due to accuracy and ripple limitations. Fortunately, PWM control can effectively perform V_{out} regulation below the single finger current, enabling extension of the LDO effective resolution, $\log_2(I_{L,max}/I_{L,min})$, from 7b to 14.3b, with a worst-case load regulation of 5.6mV/mA. As shown in Fig. 7.21b, a line regulation of 2.3mV/V is achieved.

Exponential Improvement in Quiescent Power

Figure 7.22 verifies the exponential $(1/2^N)$ improvement in the quiescent power of the RLDO architecture over baseline linear-search designs. A peak current efficiency of 99.8% for 0.5V-to-0.3V conversion is achieved. More importantly, the RLDO achieves a current efficiency greater than 90% from 33.6μA to 2mA, a 60$\times$ load current dynamic range (Fig. 7.22a), and hence achieves the widest load range with efficiency higher than 90% as compared to 1.6$\times$ (even



(a) (b)

Figure 7.22: Measured current efficiency η. (a) At V_{in}=0.5V and V_{out}=0.3V (f_{CLK}= 10MHz), demonstrating efficiency higher than 90% from 33.6μA to 2mA. (b) At V_{in}=0.5V and V_{out}=0.45V (f_{CLK}=10MHz).

with fine-grain clock gating of the barrel-shifter [130]), 3.3×, and 10× in the prior-art (Fig. 7.23). Furthermore, as depicted in Fig. 7.22b, current efficiency greater than 84.4% is achieved across a 50× dynamic range at 0.5V-to-0.45V, exceeding a simulated barrel-based DLDO by 46.4%.

7.6.3 Performance Summary

From load regulation measurements and transient tests at various f_{CLK} frequencies ranging from 1MHz to 240MHz, the RLDO with PD compensation and PWM regulation is stable irrespective of I_L, f_{CLK}, and C_{out}. In comparison to prior-art DLDOs in Fig. 7.23, the RLDO at 0.5V achieves the fastest response (3×) and settling (11×) times, largest load dynamic range, smallest area (9.13×), and best FOM (13.8×).

7.7 Conclusion

This chapter has described a new recursive DLDO architecture that improved response time, settling time, active area, and quiescent power over conventional and augmented linear-

Design	Okuma, CICC 2010	Kim, ISSCC 2016	Nasir, TPE 2016	Lee, JSSC 2017	This Work
Process	65nm	65nm	130nm	28nm	**65nm**
Active area [mm^2]	0.042	0.029	0.114	0.021	**0.0023**
Control	Time-Driven	Event-Driven	Time-Driven	Time-Driven	**SAR/PD/PWM**
V_{IN} [V]	0.5	0.5 – 1.0	0.5 – 1.2	1.1	**0.5 – 1**
V_{out} [V]	0.45	0.45 – 0.95	0.45 – 1.14	0.9	**0.3 – 0. 45**
Load range (I_L)	10µA – 250µA (25x)	7.2µA – 3.5mA (486x)	100µA – 4.6mA (46x)	4mA - 200mA (50x)	**100nA – 2mA (20,000x)**
PMOS-Array resolution	8-bit	10-bit	7-bit	6.6-bit	**7-bit**
Effective resol. ($\log_2(I_L$ range))	4.6-bit	8.9-bit	5.5-bit	5.6-bit	**14.3-bit**
Load range with η>90%	25µA – 250µA (10x)	150µA – 500µA (3.3x)	2.9mA-4.6mA (1.6x)	N.R.	**33.6µA – 2mA (60x)**
C_L [nF]	100	0.4	1	23.5	**0.4**
Quiescent I_Q [µA] during load transient test	2.7	12.5†	221	110†	**14**
V_{droop} @ load step size for load transient test	40mV @ 0.2mA	22mV @ 0.2mA	40mV @ 0.7mA	120mV @ 180mA	**40mV @ 1.06mA**
Response time T_R [ns] for load transient test	20000	44	57	4000*	**15.1**
FOM** for load transient test [ns]	270	2.75	18.04	2.44*	**0.199**
Load step rise/fall time for load transient test††	N.R.	N.R.	N.R.	4µs*	**< 1ns**
Peak current efficiency η [%]	98.7	96.3	98.3	99.94	**99.8**
Sampling clock range	1MHz – 10MHz (10x)	200MHz	5MHz – 75MHz (15x)	N.R.	**1MHz – 240MHz (240x)**
Load regulation [mV/mA]	0.65	N.R.	< 10 across range	N.R.	**< 5.6 across range**
Line regulation [mV/V]	3.1	N.R.	N.R.	N.R.	**2.3**
Settling time [µs]	240	80	1.1	20	**0.1**

N.R. = Not Reported

† I_Q consumption during transient test was not reported, min(I_Q) is assumed

* Observed from transient plots

**FOM = C_{out} $\Delta V_{droop}/(I_{max}-I_{min})$ x $I_Q/(I_{max}-I_{min})$, P. Hazucha et al., JSSC'05

†† load rise/fall time should be < $T_R/10$ for a valid measurement

Figure 7.23: Comparison of the RLDO with prior-art DLDOs.

search-based DLDOs via the use of a successive-approximation control scheme with PD compensation. Additionally, the RLDO's dynamic load range and steady-state error performance was enhanced through duty control of an additional LSB transistor.

7.8 Acknowledgements

This chapter is based on and mostly a reprint of the following publications:

- L.G. Salem, J. Warchall, and P.P. Mercier, "A successive-approximation low drop-out voltage regulator," IEEE Journal of Solid-State Circuits (JSSC), Jan. 2018, vol. 53, no. 1, pp. 35-49.
- L.G. Salem, J. Warchall, and P.P. Mercier, "A 100nA-2mA Successive-Approximation digital LDO with PD compensation and sub-LSB duty control achieving a 15.1ns response-time at 0.5V," 2017 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2017, pp. 340-341.

Chapter 8

A Digital Low-Dropout Voltage Regulator Employing Switched-Capacitor Resistance

8.1 Introduction

Modern DVFS-enabled SoCs require nimble supply regulators that rapidly respond to abrupt load changes and offer fine resolution (e.g., 12.5mV in [131], 10mV in [132]) over large voltage and current dynamic ranges. Switch-array digital LDOs (SA-DLDOs) are a potentially attractive regulation option due to their ability to operate with low input voltages and in part to their modular digital nature and scalability. SA-DLDOs employ 2^N unary- [133] or binary-weighted [134] PMOS arrays that are modulated through a 1-bit or multi-bit ADCs to maintain the output voltage (Vout) at the desired level (Vref), as shown in Fig. 8.1 (top left). Unfortunately, while array conductance in SA-DLDOs linearly increases with equal step size (GLSB) as the code is increased, the output voltage step, vLSB, does not; in fact, vLSB is nonlinear: $\sim$ GL $\times$ Vout $\times$ GLSB. Thus, SA-DLDOs achieve a nonlinear steady-state error, $ess = Vref - Vout \sim \pm GLSB/GL \times Vdrop$, as shown in Fig. 8.1 (bottom left), that deteriorates at large dropout voltages, $Vdrop = Vin - Vout$, and at small loads, GL. As a result, the required supply step of 10mV (with $\pm$15% typical

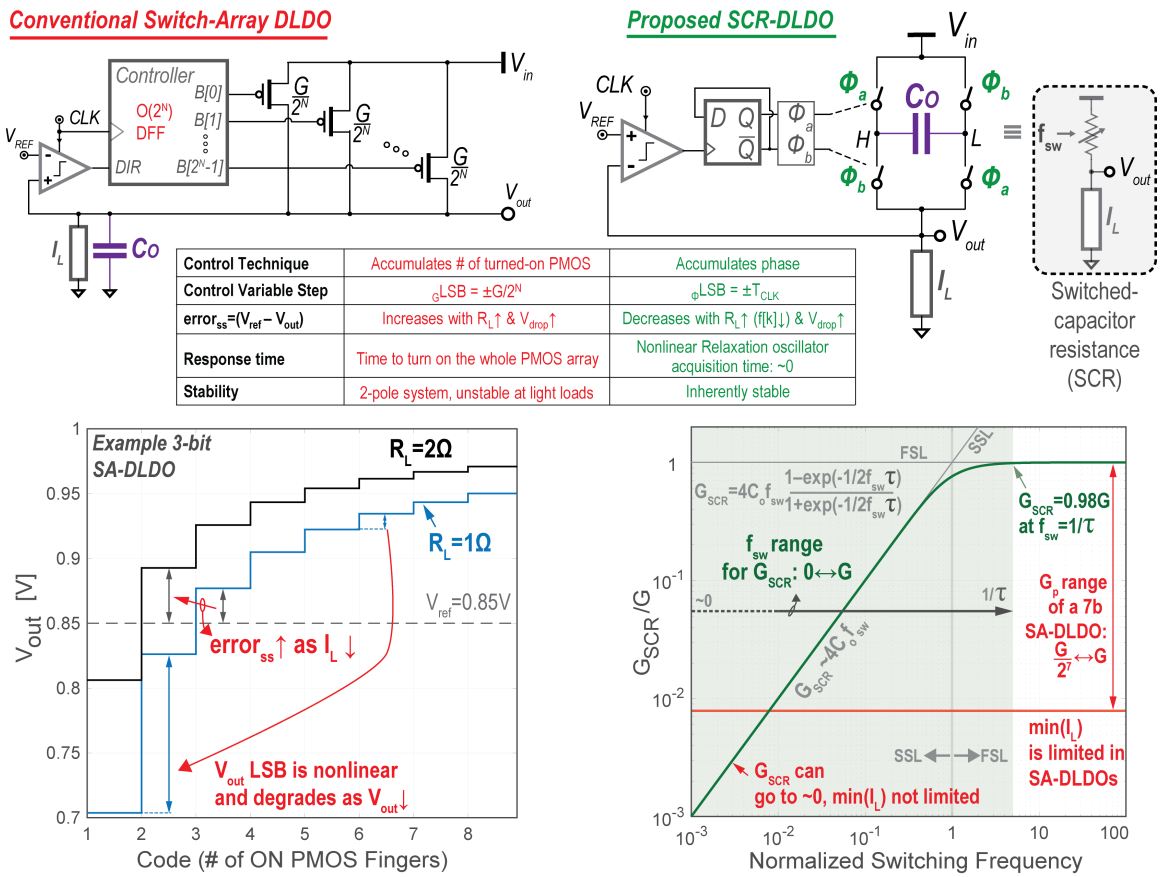


Figure 8.1: A conventional switch-array DLDO (left) and its accuracy problem (bottom left and right); proposed SCR-DLDO using a switched-capacitor resistance and its frequency-programmable equivalent conductance (right and bottom-right).

accuracy) to perform per-core DVFS over a typical 100 times load dynamic range requires an impractical 16b PMOS array resolution. Even with limit-cycle oscillations, the load range that can achieve ±1.5mV accuracy is provably limited to $2^{N-6.7}$ at Vref =Vin/2 (Fig. 8.2, top left), which would still require a 14b array resolution that, even if it were feasible to build, would come with linearly (for binary search) or exponentially (for linear search) increased response time (TR), quiescent power (IQ), and area.

8.2 Switched-Capacitor Low-Dropout Voltage Regulator

To enable industry-compliant digital replacement to analog LDOs, this work replaces the PMOS array in a SA-DLDO with a switched-capacitor resistance (SCR) that is created by switching the DLDO output capacitor Co as shown in Fig. 8.1 (top right). The SCR is then frequency-modulated through a hysteretic comparator to regulate Vout at Vref. Using two non-overlapping clocks, the top (H) and bottom (L) terminals of Co are alternately connected to (Vin, Vout) in Φ_a and (Vout, Vin) in Φ_b to charge and discharge Co by 2×Vdrop, which maximizes the charge delivered per unit capacitance. Importantly, a bilinear instead of series SCR is utilized to ensure 100% of Co is always connected to Vout despite switch commutation. In Fig. 8.1, the charge transferred, and hence the SCR equivalent conductance, GSCR, increases linearly with fsw in the slow-switching limit (SSL) region, $G_{SCR,SSL}$= 4Co×fsw, until saturating in the fast-switching limit (FSL) region, $G_{SCR,FSL}$, to its maximum value of G = 1/(2Ron) when Tsw is near the SC time-constant, τ = Co/G, where Ron is the switch equivalent on-resistance. Since GSCR can be made arbitrarily small, the SCR-DLDO can, unlike SA-DLDOs, regulate down to arbitrarily low IL.

Interestingly, placing the SCR connected to the load in feedback with a hysteretic comparator establishes a Vref-controlled relaxation oscillator which accumulates the difference ΔV = Vref - Vout to determine the oscillator period, Tsw (=1/fsw), that realizes Vout = Vref. While both SA-DLDOs and the proposed SCR-DLDO follow a search (i.e., integration) control law of the control variable, the hysteretic oscillator is nonlinear and hence abruptly finds the target fsw (i.e., with $\sim$ 0 acquisition time), enabling a response time that is limited only by comparator latency. Compared to an RLDO [134] that achieves TR=N×TCLK (Fig. 8.2, bottom right), the SCR-DLDO achieves TR $<$ TCLK for the same ΔIL and Co, where Vdrop is typically larger than Vdroop and hence the charge storage capacity of Co is amplified by the actively produced voltage swing, 2Vdrop. This, along with the efficient SCR-DLDO architecture, enables provably 2N and

2^{2N+1} better FOM over binary- [134] and linear-search [133] SA-DLDOs, respectively.

Using a clocked comparator, Tsw can only take on integer multiples of the comparator sampling clock (i.e., Tsw = k×TCLK). In this case, the minimum GSCR step within the SSL is $G_S CR, SSL$ f[k]/fCLK. Thus, the achievable Vout resolution is vLSB = Vout f[k]/fCLK, and hence ess, unlike in SA-DLDOs, actually enhances with smaller IL or larger Vdrop due to a decreasing f[k]. In the FSL region, the SCR GLSB and vLSB values can be found from the GSCR expression in Fig. 8.1 (bottom right). Throughout the SSL and FSL regions, ess is below 1mV (ENOB¿10b) across the entire Vout and IL ranges when employing an fCLK of only 4/τ (Fig. 8.2, top right). This outperforms the accuracy of a 10b SA-DLDO that not only suffers from ess=138mV (ENOB=2.9b), but that also suffers from a limited 0.65-to-0.95 Vout range at $100\times R_{L,min}$. Above all, increasing the SCR resolution via a finer TCLK actually improves TR, unlike SA-DLDOs.

It can be shown that, for the same Co and for the maximum achievable conductance in an LDO (G), fsw of the SCR-DLDO is at least 20 times lower than the required fCLK in a SA-DLDO, making the switches gate-drive losses insignificant in the overall current efficiency, η. Unlike SA-DLDOs, fsw scales with load current in proportion to the time constant of the load (CL+Co)/GL, which exponentially scales the control overhead and the gate drive losses as shown in Fig. 8.2 (bottom left), vastly improving efficiency at light loads. Since the SCR-DLDO accuracy exponentially enhances with a lower load current, the comparator sampling clock, and thus its IQ, can be linearly scaled with IL by providing fCLK directly from the frequency-scaled clock of the underlying load as shown in the measurements in Fig. 8.2 (bottom left).

8.3 Circuit Implementation

Unlike SA-DLDOs which enter limit-cycle oscillations and suffer from periodic 20-70mV ripple [133], output ripple, ΔVpp, in the SCR-DLDO can be reduced by a factor M by time-

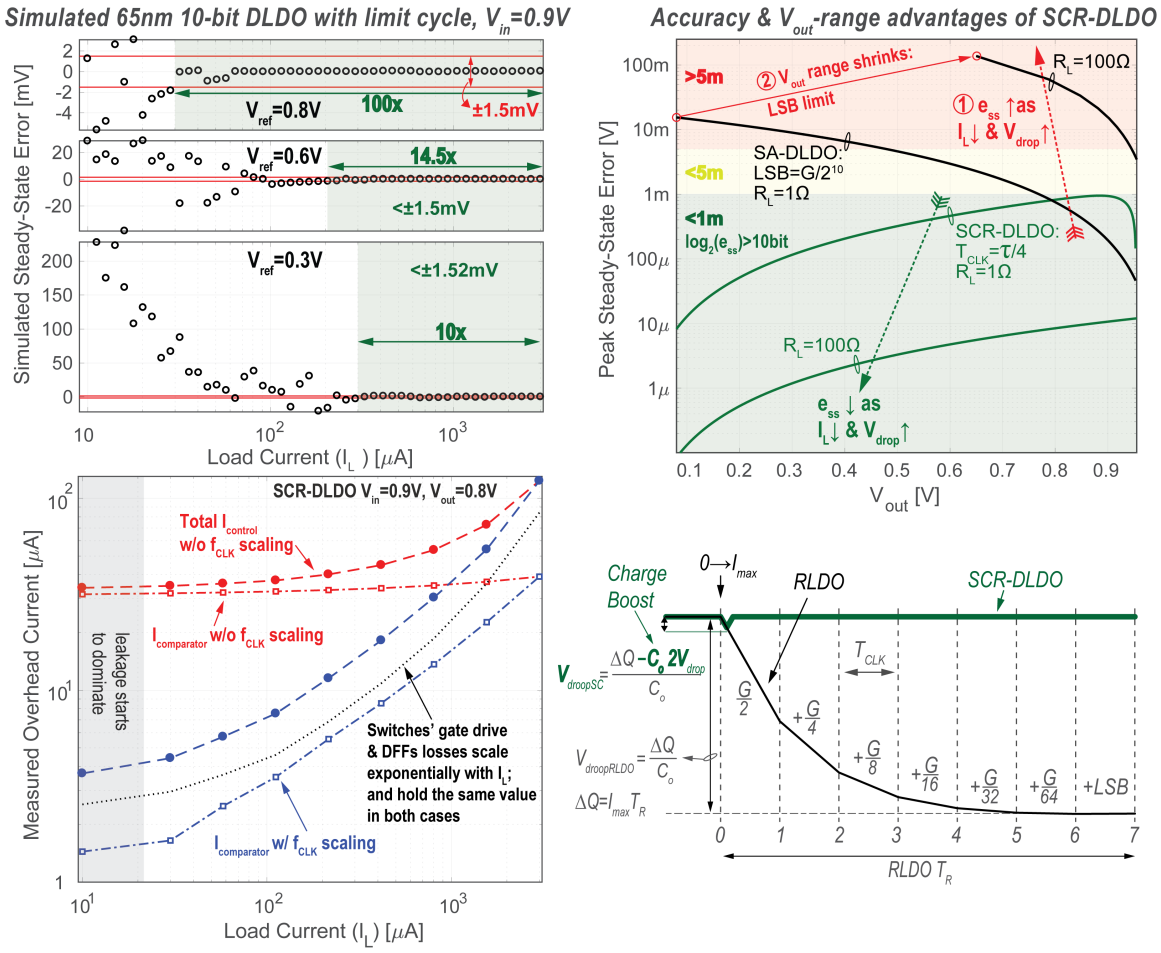


Figure 8.2: Accuracy advantage of a 1V DLDO using SCR to perform D/A conversion in the time-domain versus SA-DLDOs that achieve poor-accuracy conversion in the current-domain (top); overhead current reduction due to fCLK scaling (bottom left); fast response time advantage of the proposed SCR-DLDO.

interleaving M unit SCR cells as shown in Fig. 8.3 (top right) for M=4. Since ΔVpp nominally increases linearly with Vdrop as described by relation (1) in Fig. 8.3 (top left), the amount of capacitance that takes part in charge transfer can be scaled by a similar factor to the Vdrop increase, P, thereby canceling each other per relation (2), without affecting the load handling capability, 4Co×Vdrop×fsw. The proposed binary-ripple-control (BRC) scheme, shown in Fig. 8.3 (bottom right), divides the capacitance and conductance of each of the 4 interleaved phases into 5 binary-weighted banks that are enabled by EN[4:0] and a redundant always-on LSB bank, where EN[4:0] can be provided from an existing battery state-of-charge monitoring circuit or

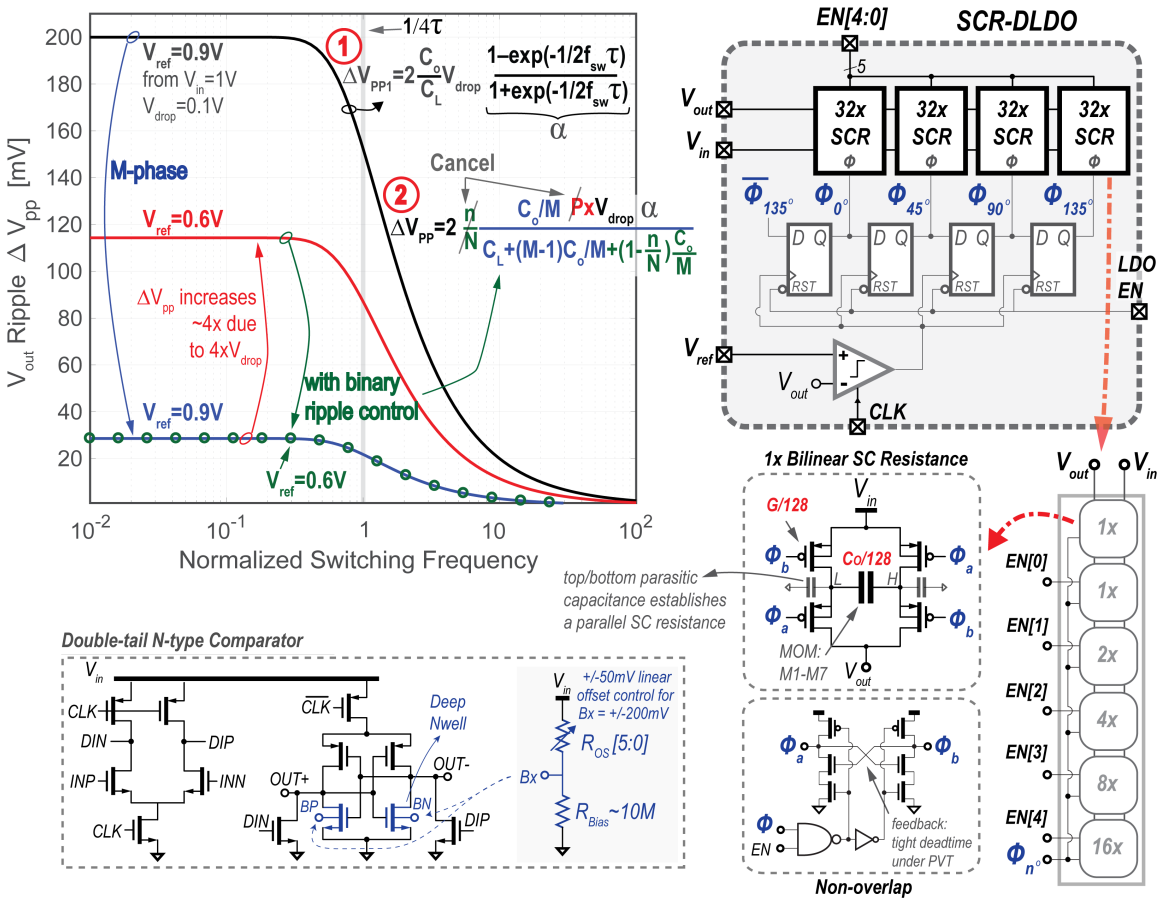


Figure 8.3: SCR ripple mitigation via the proposed binary ripple control scheme (top-left); top-level block diagram of the implemented SCR-DLDO (top-right); cell partitioning to implement binary ripple control, along with the schematics of the SCR 1x unit-cell, non-overlap circuitry, and comparator (bottom).

the switching regulator supplying Vin. The SCR-DLDO 1x unit cell, non-overlap circuit, and comparator schematics are shown in Fig. 8.3 (bottom).

8.4 Measurement Results

The proposed SCR-DLDO is fully integrated in 0.00137mm^2 core area in 65nm CMOS with Co=200pF and CL=165pF that mimics the inherent capacitance of a 3mA digital load with 5% activity. Steady-state measurement results in Fig. 8.4 demonstrate the efficacy of the SCR-DLDO in realizing high accuracy: a steady-state error of at most ±1.55mV is measured

across all desired Vout values between 0.3-0.8V over Vin corners of 0.5V and 0.9V, all over a 10A-3mA (300x) dynamic range (Fig. 8.4 left and top right). For Vin=0.9V, fCLK is set to 1GHz to enable a Tsw LSB of $\tau/4$, which would theoretically achieve $< \pm 1$mV accuracy as in Fig. 8.2. Due to the comparator frequency-dependent s-shaped offset (Fig. 8.4 left), ess grows to ± 1.55mV, which still enables up to a 174.7$\times$ accuracy improvement over a simulated 10-bit shifter-based DLDO in Fig. 8.2 (top left). Since ess enhances with lower load current, fCLK is safely linearly scaled from 1GHz down to 4MHz at 10μA to scale comparator IQ, which improves η and IL-range by 50.3% and 10$\times$, respectively (Fig. 8.4, bottom right).

Compared to the RLDO in [134], at Vin=0.5V the SCR-DLDO reduces the measured error by 2.4-4.3$\times$ for Vout ranging between 0.3-0.45V (Fig. 8.4, top right), demonstrating the accuracy advantage of SCR- over SA-DLDOs. The SCR-DLDO achieves a peak η of 99.3%, and at Vout=0.3V, operates from 1.5μA-1.75mA with $\eta >$70% (a 1,167$\times$ dynamic range), exceeding [134] by 5$\times$ and improving light-load efficiency by 37% (Fig. 8.4, bottom right). With IQ=48.4A (fCLK=1GHz), the SCR-LDO achieves a measured TR=2.48ns with Vdroop=20.5mV in response to periodic 50A-3.3mA on-chip load swings occurring within 200ps. Thus, the achieved FOM is 36.9ps, for a 5.4$\times$ improvement over prior-art (Fig. 8.6). BRC operation is demonstrated to reduce ripple from 161.3mV to 21.7mV at the worst-case voltage corner (Vin=0.9V to Vout=0.3V) across a 300$\times$ IL range (Fig. 8.5, bottom left and right) and at the worst-case current corner (Vin=0.9V with IL=10A) for Vout between 0.3-0.8V (bottom middle). A die photo is shown in Fig. 8.7.

8.5 Acknowledgements

This chapter is based on and mostly a reprint of the following publication:

L.G. Salem and P.P. Mercier, "A sub-1.55mV accuracy 36.9ps FOM digital low-dropout regulator employing switched-capacitor resistance," 2018 IEEE International Solid-State

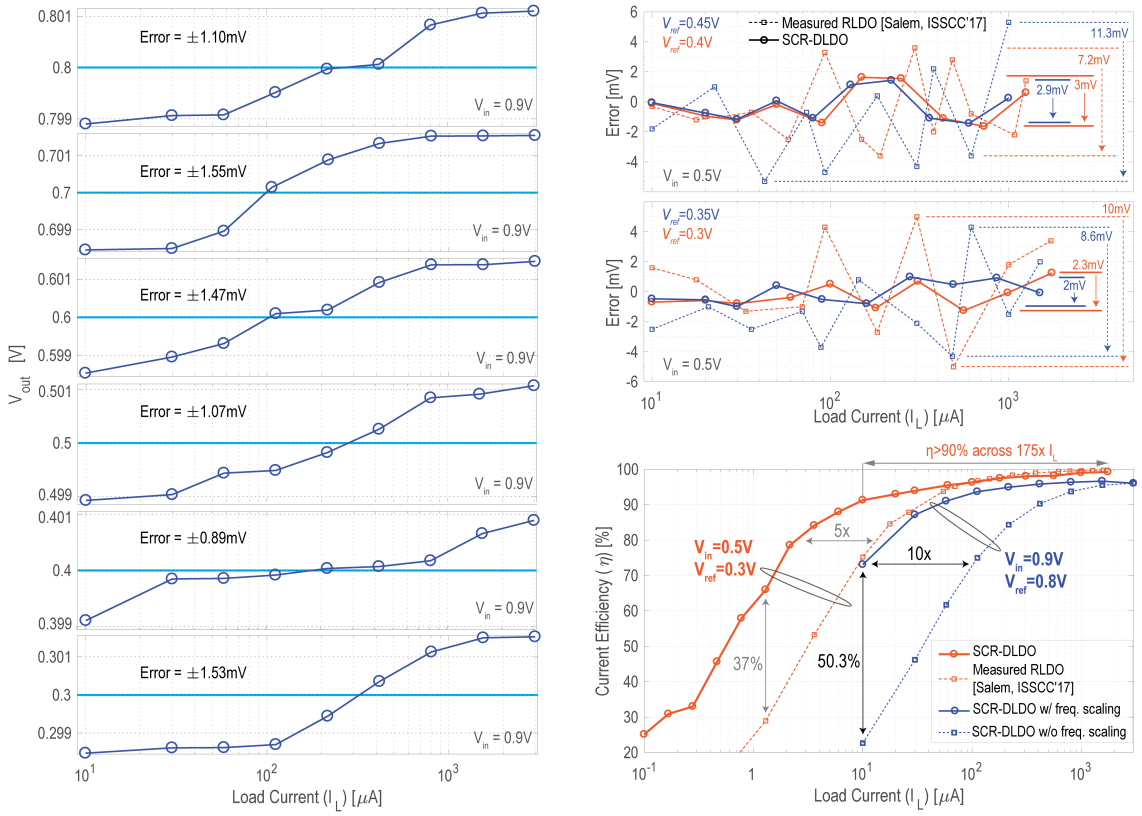


Figure 8.4: SCR-DLDO output voltage and current efficiency at corners Vin = 0.9V and Vin = 0.5V, demonstrating high accuracy and efficiency. The measured SCR-DLDO output and efficiency are compared to the measured results of a recursive DLDO.

Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2018.

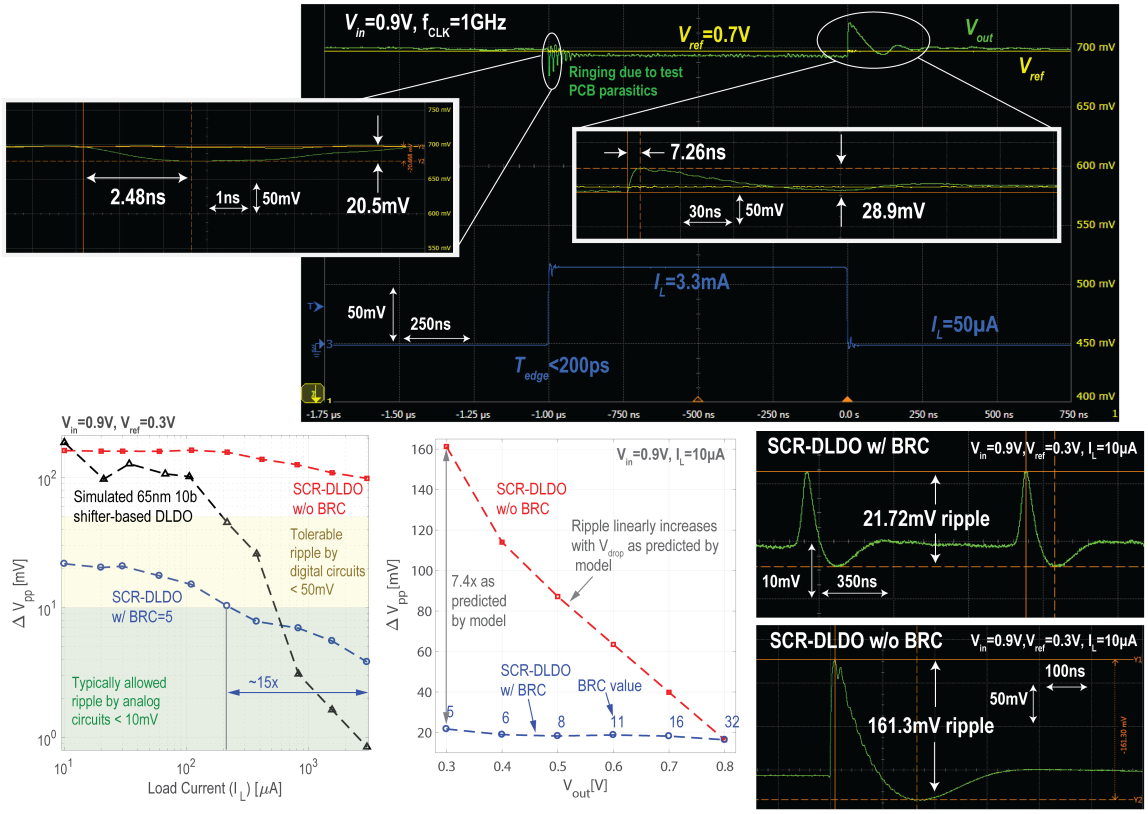


Figure 8.5: Measured dynamic response of the SCR-DLDO to an on-chip periodic load-step demonstrating 2.48ns response time at 36.9ps FOM (top). Illustration of the efficacy of the proposed binary ripple control scheme in mitigating the SCR ripple at light loads and small Vout values (bottom).

Design	Huang, ISSCC'17	Tsou, ISSCC'17	Kim, ISSCC'17	Salem, ISSCC'17	This Work
Process	65nm	40nm	65nm	65nm	**65nm**
Active area [mm^2]	0.03	0.193	0.03	0.0023	**0.00137**
V_{in}[3] [V]	0.6	0.6 – 1.1	0.45-1	0.5 – 1	**0.5-0.9**
V_{out}[3] [V]	0.5	0.5 – 1.0	0.4-0.95	0.3 – 0. 45	**0.3-0.8**
Loop Actuator	9b PMOS array	7b PMOS array	4x 7b PMOS array	7b PMOS array	**SC Resistance**
Control Loop	Barrel Shifter+Analog Assisted	PID	Event-Driven multi-bit ADC	SAR/PD/PWM	**Hysteretic Relaxation Oscillator**
Limit-Cycle Capability for Accuracy Improvement	No limit-cycle	No limit-cycle	No limit-cycle	No limit-cycle	**Not Applicable**
Load range	2m– 12mA (6x)	15mA – 210mA (14x)	14µA – 3.36mA (~100x *)	100nA – 2mA (20,000x)	**10µA-3mA (300x)**
Load range with η>90%	N.R.	N.R.	~ 10x	33.6µA – 2mA (60x)	**10µA-1.75mA (175x)**
C_L [nF]/ Total C	0/0.1	20 / 20	0.1 / 0.1	0.4/0.4	**0.165/ 0.365**
Quiescent I_Q [µA] during load transient test	N.R.	N.R.	258	14	**48.4**
V_{droop} @ load step size for load transient test	105mV @ 10mA	38mV @ 200mA	34mV @ 1.44mA	40mV @ 1.06mA	**20.5mV @ 3.25mA**
Response time[1] T_R [ns] from relation: $C_{out}V_{droop}/\Delta I$	1.05†	1000††	2.36	15.1	**2.3 (2.48 measured)**
FOM[2] for load transient test [ns]	-	0.493††	0.423	0.199	**0.0343 (0.0369)**
Load step rise/fall time for load transient test[2]	1n†	1000	N.R.	< 1ns	**<200ps**
Peak current efficiency η_L [%]	N.R.	N.R.	99.2	99.8	**99.3**
Sampling clock range	10MHz	N.R.	Not Applicable	1MHz – 240MHz (240x)	**100K-1.55GHz (15,500x)**
Steady-state error (mV)	N.R.	<150†††	<15	<5.2	**<1.55**
DC Accuracy: peak-error/V_{in}	N.R.	±13.6%†††	±1.5%	1.04%	**±0.17%**
Load regulation: worst peak-peak error/ΔI [mV/mA]	N.R.	0.8	<15	< 11.3 across range	**< 1.03 across range**

N.R. = Not Reported

[1] load rise/fall time should be < T_R/10 for a valid *unit-step* FOM measurement

[2] FOM = $C_L V_{droop}/(I_{max}-I_{min}) \times I_Q/(I_{max}-I_{min})$, P. Hazucha et al., JSSC'05

[3] Measured ranges are only depicted

† I_Q consumption during transient test was not reported. Also, the reported T_R is approximately the load rise/fall time, and hence the reported FOM is for the unit-ramp response and not the unit-step response.

†† Observed from transient measurement

††† Best-case theoretical value across the reported 15-150mA (10x) range

* For the same V_{ref}

Figure 8.6: Comparison of the proposed SCR-DLDO with state-of-the-art switch-array DLDOs illustrating the smallest area, best FOM, and highest accuracy, enabling a realistic industry-compliant digital replacement to analog LDOs for 3.1mV step DVS and adaptive voltage scaling applications.

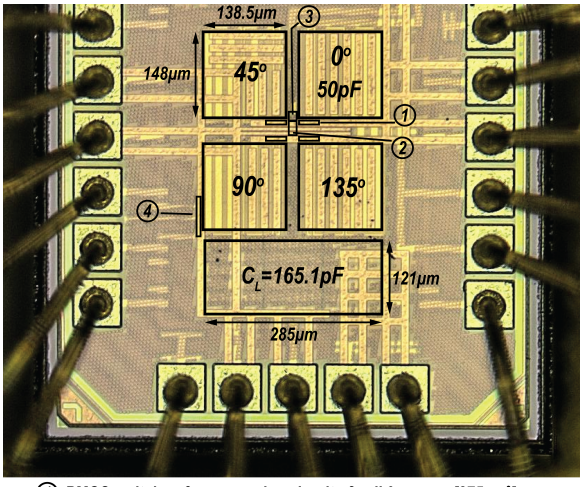


Figure 8.7: Micrograph of the fabricated SCR-DLDO chip.

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