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UNIVERSITY OF CALIFORNIA

Los Angeles

High Quality Arsenic Based III-V Semiconductor Integration on Si Using van der Waals Layered Material Buffer for Photonic Integration Applications

A dissertation submitted in partial satisfaction

of the requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Yazeed Abdullah Alaskar

ABSTRACT OF THE DISSERTATION

High Quality III-V Semiconductor Integration on Si Using van der Waals Layered Material Buffer for Photonic Integration Applications

by

Yazeed Abdullah Alaskar Doctor of Philosophy in Electrical Engineering University of California, Los Angeles, 2016 Professor Kang Lung Wang, Chair

Integration of arsenide-based III-V compound semiconductors on silicon (Si) has been the focus of significant research to integrate light sources on silicon, enabling an integrated optical solution for chip-chip interconnects in future computing systems, and to make cost-effective and efficient multi-junction solar cells on silicon substrates. The primary obstacle to success is the lattice and thermal expansion mismatches between the semiconductor compounds of interest and the silicon substrates.

In this thesis, a novel heteroepitaxial growth technique, quasi van der Waals epitaxy, promises the ability to grow high quality As-based semiconductor compounds on silicon using a twodimensional (2D) layered material as a buffer layer, where the van der Waals force is dominant between the layers, thus reducing the strain arising from lattice and thermal expansion coefficient mismatches. The main body of the thesis is structured in three parts. First, theoretical investigations of quasi van der Waals heteroepitaxial growth of arsenide-based III-V compounds on layered materials, such as graphene, Indium Selenide (InSe), Boron Nitride (h-BN) and Molybdenum Selenide (MoS_2), where the surface free energy and adsorption energies of Ga, Al, In and As are calculated using DFT calculations. Second, experimental demonstration of a novel low temperature technique for quasi van der Waals heteroepitaxial growth of arsenide based III-V compounds on graphene using Molecular Beam Epitaxy (MBE) is described. Third, using Indium Selenide (InSe) as a buffer layer due to its relatively high surface free energy and stability at high growth temperatures, a high quality and defect-free InGaAs/GaAs double heterostrucure (DH) is integrated onto a GaAs/ Si structure. The crystal quality of GaAs shows the lowest defect density of GaAs grown directly on Si to date, making it a remarkable step toward obtaining optical emitters on silicon substatres. The optical properties of this heterostructure were characterized using micro-photoluminescence (μ -PL), demonstrating room-temperature light emission out of the InGaAs/GaAs heterostructure integrated on thin GaAs on InSe/Si. Planar growth of GaAs thin films on layered materials is a potential route towards heteroepitaxial integration of GaAs on silicon in the developing field of silicon photonics.

The dissertation of Yazeed Abdullah Alaskar is approved.

Oscar Stafsudd

Dwight C. Streit

Ya-Hong Xie

Kang Lung Wang, Committee Chair

University of California, Los Angeles

2016

This dissertation is dedicated to my parents and my family

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Chapter 1 Introduction

1.1. Background

Molecular beam epitaxy (MBE) has proven to be a useful tool to grow epifilms with atomically flat surfaces and abrupt interfaces. While nearly perfect homoepitaxial growth has been demonstrated by MBE [1-3], heteroepitaxial growth is challenged by dissimilar chemical bonding, surface dangling bonds, surface states, and surface symmetry mismatch. In addition, lattice mismatch, polar-on-non-polar epitaxy, and thermal expansion mismatch add complexity to the direct heteroepitaxial growth of GaAs/Si.

1.2. Heteroepitaxial Growth of III/V Compound Semiconductors on Silicon

Integration of III-V compound semiconductors on silicon (Si) has been the focus of significant interest over the past 30 years [3-12]. Compared to Si, most III-V materials have higher carrier mobility, thus making them suitable candidates for high-speed electronic devices. But, due to its cost-effectiveness, chemical stability, and good mechanical strength, Si is still considered the best choice for large-scale integration of microelectronic circuits. III-V materials, however, have direct bandgaps, which is essential for efficient optoelectronic devices, such as light-emitting diodes, lasers and photodetectors. Therefore, the integration of III-V materials with Si microelectronics is a burgeoning field, with the goal of achieving high speed and efficient optical devices that can be fabricated at a significant performance and cost advantage using standard semiconductor fabrication techniques. Direct heteroepitaxial growth of high-quality GaAs on silicon is challenging due to the large lattice mismatch of 4.2%, large thermal expansion

mismatch of 63% and the occurrence of anti-phase domains caused by polar-on-non-polar growth [13]. These problems create stresses at the interface that negatively affect the quality of the grown films. In case of the GaAs/Si system, the resulting large strain creates a high density of dislocations, deteriorating the optical and electrical properties. Therefore, it is very critical to avoid interfacial strain in the integration of GaAs on Si to improve device performance. So far many different techniques have been considered to tackle these problems, for example thermal cycle annealing (TCA) to annihilate the dislocations [14, 15] and two-step growth to obtain a high quality buffer layer. In two-step growth, the initial interfacial layer is grown at low temperature, in which the crystallinity of the layer is poor due to the low adatom migration rate. Then, a subsequent annealing step improves the crystallinity of the layer. This technique helps to create a buffer that accommodates misfits, while the surface consists of well-oriented crystallites. Further growth at high temperature can proceed with a defect-free layer [16, 17]. Another approach is to use strained superlattices as a filter for the dislocations created at the heterointerface. In this approach, thin InGaAs/GaAs superlattices have an alternating strain, which bends dislocation lines at these strained interfaces. This bending of dislocation lines reduces the defect density in subsequent layers [12, 18-22]. A widely used approach is to use buffer layers, where these buffer layers can confine the misfit dislocations to a region underneath the active material [9, 22-25]. A well-known buffer layer for the GaAs/Si system is Ge_xSi_{1-x} , where the composition gradually varies while growing the buffer so that it is lattice-matched to both GaAs and silicon [9]. The buffer layer between the epitaxial layer and the substrate can suppress the penetration of threading dislocations to the active layer. Recently, epitaxial lateral overgrowth (ELO) from patterned areas has showed promising results due its ability to confine dislocations into the sidewalls of the growth "windows". However, thermal expansion coefficient mismatch between the barrier layer and GaAs causes some types of defects that degrade GaAs properties [7]. As a alternative approach, layered materials can be used as buffer layer for GaAs/Si systems due to their unique and promising properties, promising to open up a new route for heteroepitaxy without lattice/thermal expansion mismatch constraints [26-30]. Furthermore, this approach provides a new opportunity to utilize the novel electrical, optical, thermal and mechanical properties of such layered materials [31-37].

1.3. Quasi van der Waals Epitaxy:

Since the first demonstration by Koma in 1984 of 2D/2D material systems, e.g., selenium/tellurium and NbSe₂/MoS₂ [2], van der Waals epitaxy (vdWE) has been proven to be a useful route to heteroepitaxy, alleviating most of the aforementioned constraints [38-42]. Utilizing such a route, depositing a material with three-dimensional (3D) bonding on a two-dimensional (2D) layered van-der-Waals material promises to be a new and interesting approach to heteroepitaxy. The bonds between the 2D material / 3D substrate in this approach are weaker in comparison to the covalent bonds between a 3D substrate / 3D deposited layer. Therefore, the weak bonds between 2D / 3D layers could accommodate thermal mismatch at different substrate temperatures during the growth [30, 43-47]. Furthermore, the dislocations at the interface are not expected to propagate through the grown material due to the weak interactions at the 2D/3D heterointerface. Then, by having a suitable layered buffer layer which is lattice-matched to the grown 3D material, high quality material can be grown on top, leading to improved crystalline properties and reduced structural defects, such as dangling bonds and dislocations in the grown overlayers [38]. Different research groups have already used 2D atomic layered materials,

including graphene, hexagonal boron nitride (hBN), transition metal dichalcogenides (TMDs) and topological insulator materials, as semiconductor substrates for the growth of 3D semiconductors [26, 48, 49]. Therefore, an approach using a layered material as a buffer layer to facilitate the growth of high-quality GaAs/Si films, as illustrated in Figure 1.1, shows promise.

In this study, the integration of III-V semiconductors on 2D buffer layers is carried out using epitaxial growth by molecular beam epitaxy (MBE). Layered materials can be grown directly on the target substrates using MBE [31, 35, 38, 50] or Chemical vapor deposition (CVD) [31, 51-53], or can be mechanically transferred onto any substrate after being grown if needed [34].



Figure 1.1 (a) Atomic geometry of GaAs/ layered material /Si interface, (b) schematic view of a structure with GaAs grown on top of layered buffer layer / Si substrate.

The QvdW epitaxial growth of GaAs on Si using 2D layered materials as a buffer layer is proposed in this study. Based on our preliminary studies of GaAs growth on Graphene/Si, we concluded that the main points that need to be addressed for a successful epitaxial growth of III/V semiconductors on 2D /Si are as follows:

• Low free surface energy of layered materials.

Due to low surface energy, 2D materials exhibit a high surface tension, so deposited GaAs films will tend not to wet the buffer surface, resulting in island growth, which is empirically associated with high defect densities.

• Low adsorption energies of III/V adatoms on layered materials.

Al, Ga, In, As atoms making up the AlGaInAs material system exhibit very low adsorption energies on graphene and other layered materials, which makes it difficult for GaAs to be stable atop a 2-D layered material surface.

• Lattice mismatch between III/V and 2D material.

Although the growth of 2D materials on top of Silicon substrates is not constrained by the lattice mismatch between the grown layered material and the Silicon substrate, the growth of 3D/2D is still constrained.

1.4. Growth Kinetics and Thermodynamic considerations of quasi van der Waals Epitaxy using MBE

A better understanding of MBE growth processes and thermodynamics is needed to achieve our goal of growing epitaxial layers that result in a perfect crystal, especially in the case of quasi van der Waals Epitaxy, where 3D semiconductors are grown on van der Waal's layered materials. In this section, the effect of the interfacial energies between substrate and epitaxial thin film on the growth mode and the kinetics of growth will be studied.

1.4.1 Growth processes and kinetics:

In a typical MBE system, molecules (atoms) are evaporated from hot sources to impinge on a high-temperature surface in the path of an effusive molecular beam. Therefore, understanding the processes undergone by molecules arriving at that hot surface (substrate) is of great importance. Figure 1.2 displays the main processes in epitaxial growth. The first process is the adsorption of the molecules on the substrate. When the adtoms (Blue dots impinging the surface) arrive at the substrate, they may be either adsorbed or desorbed. The sticking coefficient (S_c) describes the probability that the arriving species will be adsorbed onto the surface.

$$S_c = \frac{N_{ads}}{N_{tot}} \tag{1}$$

where N_{ads} is number of atoms which adsorb and N_{tot} is total number of atoms impinging on the substrate. Adsorption can be physical (physisorption), where it is based on van der Waals forces on the surface. Another type of adsorption is chemical adsorption (chemisorption), which results from forming covalent or ionic bonds with the surface [54]. For III/V epitaxial grown on layered materials in this thesis, we will consider physisorption only, in the presence of van der Waals bonds in this type of epitaxy. The adsorption rate depends exponentially on the adsorption energy as follows [54]:

$$R_{ads} = A v_a \exp \frac{-E_{ads}}{k_B T}$$
(2)

where A is a constant, v_a is the adsorption frequency, E_{ads} describes the energy necessary to overcome the electrostatic potential, k_B is the Boltzmann constant and T is the substrate temperature [55]. Sticking coefficients often vary with temperature and surface stoichiometry. In the case of growth of III/V semiconductors on layered materials, the adsorption energy is low. This means it is hard for the adtoms to stick on the van der Waals surfaces, especially at high growth temperatures, and the process will result in no net growth to the system. Chapter 3 will show some DFT calculations of adsorption of Ga, In, Al and As on different van der Waals materials.



Figure 1.2: A schematic of basic processes during epitaxial growth. The two main processes of adsorption and diffusion (migration) are shown here, where the adsorbed adatoms (blue dots) diffuse on the surface until lowest-energy bonding site is found.

The second process is the diffusion or migration of the adatoms on the substrate, where adatoms (Blue dots on the surface) have the freedom to find the lowest-energy bonding site and to arrange themselves into a closely packed structure. Hence, the growth yields high quality crystals instead of the random accretion of atoms (stochastic growth). Imparting the thermal energy from

the heated surface to these molecules when they arrive at the substrate enables surface diffusion. The diffused adatoms may desorb from the surface, meet other adatoms, attach or aggregate to an existing island or step, or react at a defect site. An incorporation coefficient describes the probability that adsorbed species become incorporated into the crystal. In the case of growth of III/V semiconductors on layered materials, in general, the incorporation coefficient is high compared to conventional epitaxy due to the lack of dangling bonds on such surfaces. In the case of low thermal energies provided to the adsorbed adatoms, we see ballistic deposition in which there is little order to the system and the surface becomes rough. Thus, choosing the proper nucleation conditions in very critical for the vdW heteroepitaxial growth of III/V semiconductors on layered adatoms on the diffusion energy exponentially as follows [33]:

$$D = B a^2 K_s = B a^2 \exp \frac{-E_d}{k_B T}$$
(3)

where *B* is a constant, K_s is the site-to-site hopping rate, *a* is the effective hopping distance between sites, E_d is the diffusion energy, and *T* is the substrate temperature. From this equation, we see that the growth temperature affects the diffusion rate directly. In addition to the growth temperature, the V/III ratio has a similar impact as the growth temperature. High values shorten the migration length of the group III species because they can more easily find nucleation sites and then incorporate into the crystals.

Based on our DFT calculations of migration energies of Ga, In, Al and As on graphene, in Chapter 3, migration energies on layered materials are higher than on most 3D substrates. It is important to note here that the diffusion process affects the degree of smoothness of the grown film at a fixed growth rate.

1.4.2 Thermodynamic considerations of epitaxial growth

In MBE growth, the thermodynamic and kinetic factors determine the growth mechanisms. However, from a classical thermodynamics point of view, epitaxial thin film growth follows different growth modes according to the surface energies of the substrate and the grown semiconductor and the interfacial energy between the substrate and the grown semiconductor. Figure 1.3 displays a schematic of the three basic growth modes, Frank-van der Merwe (FM) (layer-by-layer growth mode), Volmer- Weber (VW) (island growth mode) and Stranski-Krastonov (SK) (mixed layer/island growth mode). The layer-by-layer growth mode occurs when the sum of the substrate surface free energy and the deposited film/substrate interface energy is larger than that of the deposited film. In this case, planar growth takes place by minimizing the surface energy of the grown thin film toward the bulk crystal value. In other words, the adtoms preferentially attach to the exposed part of the substrate surface rather than the already grown thin film, yielding layer-by-layer growth. On the other hand, when there is no strong bonding between the film and the substrate, island growth (Volmer-Weber (VW) growth mode) takes place. In this case the, the grown film does not wet the substrate because this will lead to an increase in the total surface energy. This growth mode is the thermodynamically favored growth mode for III/V semiconductor heteroepitaxial growth on van der Waals layered materials, where the binding force between the particles of the deposited material are stronger than the forces between the material and the substrate. As an intermediate case between layer-bylayer growth and island growth, the Stranski- Krastanov (SK) growth mode can also occur,

where the growth mode changes from layer-by-layer to island growth due to a rise in lattice mismatch biaxial strain energy that releases itself after a few layers, yielding islands on top of a strained thin film.



Figure 1.3: A schematic of the three basic growth modes. FM mode occurs when the sum of the substrate surface free energy and the deposited film/substrate interface energy is larger than that of the deposited film. In this case, planar growth takes place by minimizing the surface energy of the grown thin film toward the bulk crystal value. VW mode occurs when there is no strong bonding between the film and the substrate as in the case of growing 3D on 2D. SK mode occurs when the surface energies balnce is between FM and VW modes.

The thermodynamic approach is used to determine growth modes of thin films close to equilibrium. However, the MBE growth process is mostly a kinetic process, and thermal

equilibrium conditions can be only partially fulfilled. This occurs by not allowing the deposited ad-atoms to rearrange themselves to minimize the surface energy through limited surface diffusion or super- saturation of the deposited material, leading to large nucleation rates. In the MBE process, the growth kinetics are mainly controlled by the growth temperature, V/III ratio and growth rate where a microscopic path is taken by the system during growth to create non-thermodynamically favorable growth modes [30]. Another way to control the kinetics of the growth is to create potential reaction sites on the surface that might vary in energy. Diffusion processes are significantly affected by impurities, strain and other defects. These features tend to have an charge effect on the potential energy of the surface, and may therefore create enhanced diffusional barriers or generate favored reaction sites. Thus, miscut substrates can play a significant role in determining the growth processes and mode. In general, kinetically controlled growth has advantages and drawbacks. It helps realize thermodynamically unstable morphologies, but it might also inhibit attaining the thermodynamic equilibrium morphology, even after post-annealing of the film.

1.5. Potential Applications

Integrating III-V semiconductors on silicon substrates has been a goal for many research groups around the world to open the door for next-generation photonics. Among the potential applications, optical interconnects that are integrated on microelectronic chips must be realized to maintain the growing demand for high bandwidth, low power consumption and high speed communications for giant data centers. It has been expected that chip-to-chip bandwidth demand is likely to jump to more than 100 Gb/s in the near future. The current copper interconnect technology has reached the point where high parasitic impedance has become an obstacle to scaling for higher throughputs. Therefore, the integration of III-V materials with Si microelectronics is a burgeoning field with the goal of achieving high speed and efficient optical devices that can be fabricated at a significant performance and cost advantage using standard semiconductor fabrication techniques.

Another important application is photovoltaic devices, where integrating high quality III/V semiconductors on silicon can yield high-efficiency III-V based multi-junction photovoltaic cells utilizing cheap and large silicon wafers. Few research groups presented theoretical studies of the design of III-V multi-junction solar cells on silicon, where using silicon substrates can yield high efficiencies up to 36% by utilizing the solar spectrum more efficiently [56].

Furthermore, the concept of integrating III-V semiconductors on silicon substrates using layered materials as a buffer can be extended to other substrates as long as layered materials can be gown on to of it, opening the door to make new heterostructures. Thus, utilizing cheap flexible substrates to make novel cheap devices.

1.6. Dissertation Outline

In this thesis, a novel heteroepitaxial growth technique called quasi van der Waals epitaxy and the experimental methods used to achieve it will be described in the first and second chapters. The main body of the thesis is structured into three parts.

I. Theoretical investigation of quasi van der Waals heteroepitaxial growth of arsenide-based III-V compounds on layered materials, such as graphene, Indium Selenide (InSe), Boron Nitride (h-BN) and Molybdenum Selenide (MoS_2), where the surface free energy and adsorption energies of Ga, Al, In and As are calculated using DFT calculations.

- II. Experimental demonstration of a novel low-temperature technique for quasi van der Waals heteroepitaxial growth of arsenide-based III-V compounds on graphene using Molecular Beam Epitaxy (MBE).
- III. Experimental demonstration of the use of Indium Selenide (InSe) as a buffer layer in the growth of a high-quality and defect-free InGaAs/GaAs double heterostrucure (DH) integrated onto a GaAs/ Si structure. The crystal quality of GaAs showed the lowest defect density of GaAs grown directly on Si to date, making this a remarkable step toward obtaining optical emitters on Silicon substatres. Planar growth of GaAs thin films on layered materials is a potential route to heteroepitaxial integration of GaAs on silicon in the developing field of silicon photonics.

Chapter 2 Experimental Methods

2.1. Introduction

The experimental techniques and tools used in this research are described in this chapter. The most important tool here is the molecular beam epitaxy (MBE) system, which was used to grow our samples epitaxially. After growth, several characterization techniques were used. These included scanning electron microscopy (SEM), to check the overall morphology and quality of samples; energy dispersive spectroscopy (EDS), to monitor the sample composition ratios; atomic force microscopy (AFM), to determine the roughness of the epitaxially grown samples; transmission electron microscopy (TEM), to confirm the local quality of the grown samples; X-ray diffractometry (XRD) to check the preferred orientation direction (or axis) in the crystal and its degree of orientation; and photoluminescence spectroscopy (PL), both at room temperature and low temperatures, to characterize the optical properties of the grown samples.

2.2. Molecular Beam Epitaxy (MBE)

MBE is an ultra-high vacuum technique that is used when thin films of the highest quality and perfection are required. The MBE system used in our experiments is a Perkin (Elmer) 430 MBE system. This system is composed of three chambers, including the load-lock chamber, long buffer tube chamber, and the main growth chamber. A photograph of the entire system is shown in figure 2.1 (a), and a photo taken from the viewport of the long buffer tube is shown in figure 2.1 (b), where the molybdenum (Mo) holder is ready to be loaded into the growth chamber. The growth chamber is evacuated to UHV standards using three vacuum UHV pumps. These include

a titanium (sublimation) pump, an ion pump, and an auxiliary cryogenic pump to achieve base pressures in the order of 10^{-10} to 10^{-11} Torr. In addition to the three pumps, during growth a liquid nitrogen (N₂) cryo-shroud (77 K) internally encircles both the source flange and the growth chamber to trap contaminants onto the chamber walls, thus improving the vacuum quality in the main chamber. This vacuum range is needed to maintain a long free path on the order of 10^{8} cm during the growth process. The ultra-high vacuum conditions are necessary to maintain the extreme cleanness required for the growth environment; in addition, very stringent operating procedures and ultra-pure molecular beam sources must be used. Moreover, every time the growth chamber is opened to the atmosphere, the system should be baked for several days to outgas the moisture and other volatile contaminants that may have entered the chamber. The baking-out process should be carried out at temperatures in the range of 160- 200 °C and in such a way as to prevent any cold spots during the process.



Figure 2.1: (a) The growth chamber of Perkin-Elmer MBE 430 system. (b) Molybdenum holder in the intro-tube before loading into the growth chamber.

The growth chamber is composed of three main parts. Figure 2.2 shows the main parts of the growth chamber.



Figure 2.2: A schematic of the basic elements in the Molecular Beam Epitaxy growth chamber. The three main parts of the chamber are the substrate manipulator, source flange containing the solid-source effusion cells and the cracked As cell, and the Reflection High Energy Electron Diffraction (RHEED) apparatus that allows in-situ monitoring during the growth process.

The first part is a substrate manipulator used to manipulate the sample/holder in the chamber. A substrate heater and a thermocouple are attached to this manipulator. The substrate temperature

is one of the key parameters for the growth. Thus, proper calibration of the holder temperature must be carried out. A GaAs substrate, where oxide decomposition and different surface reconstructions take place at different well-known temperatures, is used to calibrate the growth temperature. The second part is a source flange containing the solid-source effusion cells. In this system, the effusion cells include Ga, As, Al, In, Be (p-type dopant), and Si (n-type dopant). The effusion cells contain a heater, where a thin filament of either Tantalum (Ta) or Molybdenum (Mo) is heated to the material evaporation temperature, which can be as high as 1400 $^{\circ}$ C; heat shielding, usually made of multiple Ta foils, used to confine the heat in the cell; a thermocouple to measure the material temperature; and a crucible, usually made of pyrolitic boron nitride (PBN), to hold the source material. The crucible can take many shapes and sizes depending on the cell design. In addition to effusion cells, an As cracking source is used to crack As₄ molecules into As₂ molecules by passing As₄ into a hot (900 °C) cracking zone. Each source has a high-speed mechanical or pneumatic shutter placed in front of the cell to control the growth from each cell. In the third part of the growth chamber, a Reflection High Energy Electron Diffraction (RHEED) apparatus allows in-situ monitoring of the growth process, which can provide information on the growth rate and surface reconstruction as well surface roughness (Figure 2.3). RHEED uses an electron gun to send high-energy electrons at a grazing incidence to the substrate. Because of their quantum nature and wave character, the electrons are diffracted off the surface atoms and form characteristic diffraction patterns on the phosphorescent screen on the other side of the chamber. These patterns can give valuable information of the growth morphology and surface reconstruction.

In addition, a Residual Gas Analyzer (RGA) is attached to the growth chamber to monitor the quality of the vacuum in the growth chamber and quantify the contribution of each gas species to

the background pressure. The RGA is a quadrupole mass spectrometer, where the residual gas is ionized to create ions that are accelerated through the ion source and reach the mass spectrometer; here the ions are separated by mass by the four poles, to which direct and alternating current voltages are applied, based on the mass-to-charge dependency of the ion trajectories in the electrical field.



Figure 2.3: RHEED Intensity from scattered electrons as a function of the coverage rate on the atomic surface.

2.3. X- Ray Diffractometry (XRD)

XRD is a common technique to study the structural properties of crystals An XRD system is comprised of an X-ray source, a beam conditioner to control the beam wavelength and divergence, a goniometer to manipulate the sample, a detector to measure the intensity of the scattered X-ray beam, and a collimator to limit the divergence of the measured beam [57]. As the X-rays impinge on the sample, diffracted X-rays from different crystal planes can have constructive interference by satisfying Bragg's law

$$2d \sin \theta = n\lambda$$

where n is an integer representing the order of the diffraction peak, d is the inter-planar spacing between adjacent parallel planes, λ represents the wavelength of the X-ray and θ represents the angle of scattering. Only elastic scattering where the energy (wavelength) is conserved, also called Thompson scattering, is accounted for. The resulting peaks of the diffracted X-rays represent the distribution of atoms in the crystal. In this research, different scan modes were employed to gauge the structural properties of the epitaxially grown thin film semiconductors.

- Coupled scan, resulting in a plot of scattered beam intensity versus 2θ while varying ω , where only peaks fulfilling Bragg's law are observed. Any shift of a peak from its expected position reflects the layers' strain or tilt with respect to the substrate surface.
- Rocking curve, a plot of scattered intensity versus ω keeping 2 θ constant, where the detector is fixed at a determined Bragg angle and the sample is rotated so as to vary ω . If the material is a perfect single crystal (perfect parallelism of the planes), only one set of parallel planes will generate a Bragg reflection and a very sharp peak will be observed. However, if the substrate is made of multiple crystallites slightly tilted with respect to each other, a broader peak will be observed. Such disruptions in the perfect parallelism of the atomic planes can result from dislocations, mosaicity and curvature.
2.4. Photoluminescence (PL)

Photoluminescence is a nondestructive technique to test the optical quality of grown samples by measuring the emission from radiative recombination in the material. Exposing a direct band gap semiconductor to photons of higher energy than the band gap will excite an electron from the valence band to conduction band. The created electron-hole pair has a finite momentum that undergoes energy and momentum relaxation towards the band gap minimum. A recombination process will take place by remitting the absorbed energy as photons, also called spontaneous emission, after some period of time called the carrier lifetime. The emitted photons have the same energy as the band gap of the semiconductor. These photons are measured and detected in the PL system by a sensitive photodetector. The system is equipped with an Ar laser (488 nm) for optical excitation, with a spot size of \sim 3-4 μ m. The setup includes objective lenses, a chargecoupled device camera, a monochromator and an InGaAs detector cooled by liquid nitrogen. The optical excitation is carried out in continuous wave mode with an approximate excitation power of 50 μ W. In order to perform low temperature measurements, the system is also equipped with an additional cryostat stage, which has the freedom to move along three axes. Figure 2.4 shows the PL setup used in this research. Low-temperature PL measurements are a very powerful tool to gauge the defect level in the grown semiconductors, as the effect of phonons is limited, and some type of defects have peaks in PL spectra that do not vary with temperature.



Figure 2.4: A schematic of the photoluminescence setup used. The system is equipped with an Ar laser (488 nm) for optical excitation, objective lenses, a charge-coupled device camera, a monochromator, an InGaAs detector cooled by liquid nitrogen, and a cryostat stage which has the freedom to move along three axes allowing low temperature measurements.

2.5. Scanning Electron Microscopy (SEM)

SEM is very useful imaging tool to study the overall morphology and quality of grown samples. An SEM consists of an electron gun, a lens system, scanning coils, and an electron collector. Using a focused beam of electrons to scan the sample, secondary electrons emitted by the scanned atoms make it possible to create an image showing the topology of the surface. In the SEM, there are two detection modes. The first is secondary electron imaging (SEI), where electrons are emitted from close to the surface. The second is the back-scattered electron (BSE) mode, where elastic scattering causes the electrons to be reflected from the back of the sample. In general, the SEI mode reveals better quality images, while the BSE mode can give more information about the composition of the sample.

2.6. Atomic Force Microscopy (AFM)

AFM is a very important tool to probe a sample surface. AFM can have vertical resolution down to a tenth of a nanometer and lateral resolution down to about 50 nm, making it very precise and accurate in measuring sample morphology. The AFM is equipped with a cantilever with a sharp tip with a radius of curvature of the order of few nanometers, to scan the wafer surface in both x and y directions. Based on van der Waals interactions, this tip can have attractive or repulsive forces with the surface of the sample. The tip deflection from or toward the surface can be detected by a change in a reflected laser beam that is used to accurately record the tip deflection. The final profile image shows the surface topography, where the root-mean-square (RMS) roughness values can provide a measure of the degree of smoothness of the sample surface. The AFM system used in this research is AFM, VEECO Nanoscope IIIa Multimode SPM operated in the tapping mode.

2.7. Transmission Electron Microscopy (TEM)

In this study, TEM was used to study local effects of defect propagation, dislocation, antiphase domains, stacking faults, and defect filtering and generation. In this technique, the specimen needs to be very thin, typically less than 200 nm, so electrons can be transmitted through the

sample. Therefore, the preparation of TEM samples requires tedious and painstaking effort, making it a last choice among characterization methods. In Cross-sectional TEM, the sample is glued together in a stack of wafers with the desired interface at the center. In this case, ion milling, mostly by focused ion beam, is employed to center the target interface in order to image it. The TEM system consists of a high-energy electron source, condenser lenses, and objective lenses to switch between the diffraction pattern, the sample and the sample holder. When the transmitted electrons are diffracted, a diffraction pattern (magnified image) is observed.

Chapter 3 Theoretical Investigation

3.1 Surface energy calculation and modifications

Ab-initio calculations were conducted to calculate the surface free energy of several layered materials. Surface free energy is of great interest in predicting the growth mode from a thermodynamic perspective, where it can be defined as the energy needed to create a material surface. By definition, we can expect that van der Waals materials will have lower surface free energy than 3D semiconductors, because only weak van der Waals forces are bonding the material layers. However, a relatively high surface free energy is desired for layered materials used as buffer layers, to promote layer-by-layer growth in III/V semiconductor heteroepitaxial growth.

As graphene was our first interest due its unique properties, we started by calculating its surface free energy. Detailed descriptions of all ab-initio calculations in this study are included in section 3.3. The surface energy of the substrate σ is defined as

$$\sigma = \frac{\left[E_{\text{slab}} - \sum N_i \mu_i\right]}{2A} \tag{1}$$

where E_{slab} is the total energy of the substrate calculated from first principles, μ_i the chemical potential of species *i* in the slab structure, N_i the number of particles of the *i*-th element in the slab and *A* the area of the slab.

The surface energy values calculated for single-layer and bilayer pristine graphene, multi layer graphene (MLG), Indium Selenide (InSe) and Hexagonal Boron Nitride (h-BN) are listed in table

3.1. The surface free energies of Molybdenum Diselenide (MoS_2) and Bismuth Selenide (Bi_2Se_3) with values for 3D materials collected from the literature are also listed in Table 3.1. The calculated value for the surface energy of graphene is in good agreement with prior experimental reports [58, 59].

Table 3.1: Surface free energies of different materials. The surface energy values for single-layer pristine graphene, multi layer graphene (MLG), Indium Selenide (InSe) and Hexagonal Boron Nitride (h-BN) are calculated using DFT calculation from equation (1). The surface free energies of Molybdenum Diselenide (MoS₂), Bismuth Selenide (Bi₂Se₃), GaAs (111) and Si (111) are collected from literature. InSe and Bi₂Se₃ have relatively high surface free energies. However, (Bi₂Se₃) decomposes at low temperatures (340 °C), where InSe is stable at high growth temperatures as well as having a relatively high surface energy.

| Material | Surface free energy, σ (J m ⁻²) | |
|---|--|--|
| Graphene | 0.048 | |
| Multi-layer graphene (MLG) | 0.052 | |
| Indium Selenide (InSe) | 0.149 | |
| Hexagonal Boron Nitride (h-BN) | .055 | |
| Si (111) | 1.467 [60] | |
| GaAs (111) | 1.697 [60] | |
| Molybdenum Diselenide (MoS ₂) | 0.044 [61] | |
| Bismuth selenide (Bi ₂ Se ₃) | 0.180 [62] | |

Although graphene atoms have dangling bonds only at the edges and defect sites, ideal graphene is a dangling-bond-free material, which results in both the surface energy of graphene and the interface energy between the grown film and the substrate being negligible. Hence, the growth morphology of the deposited layers can be primarily predicted by the surface energy of GaAs only [63]. Therefore, Bauer's surface energy formula for layer-by-layer growth can be simplified as

$$\Delta \sigma = \sigma_{\text{GaAs}} + \sigma_{\text{GaAs/2D interface}} - \sigma_{\text{2D-material}} \le 0$$
(2)

where $\Delta\sigma$ is the relative magnitude of the free energy, σ_{GaAs} is the GaAs-vacuum interface energy, $\sigma_{2D-material}$ is the 2D material-vacuum interface energy and $\sigma_{GaAs/2D \text{ interface}}$ is the GaAs-2D material interface. This equation clearly shows that 2D materials, such as graphene and Bi₂Se₃, in general, have much lower surface energy, as can be seen in Table 3.1, and cannot lead to a layer-by-layer growth from a thermodynamical point of view.

Furthermore, in order to study how this surface free energy can be modified if we use a gallium (Ga) or arsenic (As) pre-layer on the graphene, we included these modifications by adding gallium (Ga) and arsenic (As) pre-layers in our DFT calculations, whose details will be described in section 3.3. Figure 3.1 shows schematic structures used to calculate the surface energy of of a Ga (or As) pre-layer on graphene. With Ga and As pre-layers on graphene, the surface free energy σ is calculated to be 0.43 J m⁻² and 0.57 J m⁻², respectively. The predicted order of magnitude increase in the surface energy of the Ga (or As) pre-layer / graphene substrate compared to single and bilayer graphene suggests that this increases the wettability of the

underlying graphene substrate, thus promoting the likelihood of layer-by-layer epitaxial growth.

From Table 3.1, we see that Indium Selenide (InSe) and Bismuth Selenide (Bi_2Se_3) have relatively high surface free energies. However, (Bi_2Se_3) decomposes at the temperature of 340 °C, which is lower than the GaAs growth temperature, making it unsuitable for use as a buffer for GaAs growth. However, Indium Selenide (InSe) is stable at GaAs growth temperatures as well as having a relatively high surface energy.



Figure 3.1. Schematic illustration of supercell with two monolayers of gallium atoms coordinated on bilayer graphene, (a) isometric and (b) top views of the structure used in our calculations. (From the author's publication [26]).

3.2 Adsorption and Migration Energy

In addition to the calculations on of the surface energy, we also performed a systematic study of the adsorption and migration energies of Ga, In, Al and As atoms on graphene in order to gain a better understanding of the surface kinetics of these atoms during growth. VdW interactions were taken into account in our calculations using semi-empirical corrections to the Kohn-Sham energies obtained from DFT [64]. We compared the adsorption energies for the aforementioned elements adsorbed on the bridge (B), top (T) and hollow (H) sites (Figure 3.2) of the bilayer graphene lattice, and these results are listed in Table 3.2. The adsorption energy was calculated using the following expression

$$E_{\rm b} = E_{\rm supercell} - E_{\rm atom} - E_{\rm graphene} \tag{3}$$

where E_b is the adsorbtion energy, $E_{supercell}$ is the total energy per adatom of the 5 × 5 adatom layer on bilayer graphene, E_{atom} is the chemical potential of the adsorbed atom and $E_{graphene}$ is the total energy of the isolated bilayer graphene 5 × 5 supercell. The chemical potential of the adsorbed atoms (Ga, Al, In, As) is calculated with a single atom in a cubic supercell of length 20 Å. Only the Γ point of the Brillouin zone is sampled in this case. The resulting adsorption and migration energies for each of the elements at the most favorable adsorption sites calculated are summarized in Table 3.2.



Figure 3.2: Different high-symmetry adsorption sites investigated on the bilayer graphene supercell. The adsorption of Ga, Al, In and As atoms on the bridge (green), hollow (red) and top (blue) sites of the graphene supercell were investigated.

Table 3.2: Energy and structural properties of the most favorable adsorption sites of Ga, As, In and Al adatoms adsorbed on graphene. Equation (3) used to calculate the adsorption energies. Semi-empirical corrections to the vdW forces were applied in conjunction with the LDA functional.

| | Favored | Adsorption energy | Migration energy |
|----------|-----------------|----------------------|-----------------------|
| Atom | adsorption site | $E_{\rm b}({ m eV})$ | $E_{\rm m}({\rm eV})$ |
| Gallium | | 1.5 | 0.05 |
| Arsenic | | 1.3 | 0.21 |
| Indium | | 1.3 | 0.06 |
| Aluminum | H | 1.7 | 0.03 |
| Nitrogen | | 3.8 | 0.98 |

The calculation results in Table 3.2 using equation (3) show that both Ga and Al have higher adsorption energies compared to As, suggesting that the growth on graphene should be initiated using either Ga or Al. Despite the higher adsorption energy of Al, its lower migration energy

compared to other materials studied could lead to a tendency to form 3D islands, especially at high temperatures. Therefore, among III-As semiconductors, GaAs could be considered the most attractive material in terms of 2D nucleation on graphene. Very recently, the 2D growth of Group III nitrides on graphene was demonstrated where nitrogen (N) was used to initiate the growth, since nitrogen has both higher adsorption (3.8 eV) and higher migration energy (0.98 eV) compared to As. Nitrogen acts as nucleation sites for the 2D growth of Group III nitride films [65].

Using the adsorption energies of Table 3.2, the ratio of absorption energy to bulk cohesive energy (E_b/E_c) is calculated as another good figure of merit to determine the growth morphology of a compound semiconductor on graphene. Larger ratios will increase the probability of semiconductor adatoms sticking to graphene, and promote the likelihood of 2D growth occurring. Conversely, low ratios will lead to a 3D growth mode since the incident adatoms will tend to stick atop the semiconductor instead of the graphene layer [66]. The bulk cohesive energy (E_c) values of some relevant compound semiconductors collected from the literature are summarized in Table 3.3. **Table 3.3:** Ratios of adsorption energy to bulk cohesive energy for several binary materials, where bulk cohesive energy values are collected from the literature. Larger ratios will increase the probability of semiconductor adatoms sticking to graphene, and promote the likelihood of 2D growth occurring. The high ratio for GaN hints to the likelihood of 2D growth of GaN on graphene.

| | Bulk cohesive energy | Adsorption to bulk cohesive energy ratio |
|------------------|------------------------|---|
| Binary materials | $E_{\rm c}~({\rm eV})$ | $\frac{E_{\rm b}^{\rm III} + E_{\rm b}^{\rm V}}{E_{\rm c}}$ |
| GaAs | 6.7 [67] | 0.4 |
| InAs | 6.2 [67] | 0.42 |
| AlAs | 7.7 [67] | 0.39 |
| GaN | 2.2 [68] | 2.41 |

For binary compounds based on the III-As material system, the E_b/E_c values are very low, hinting that their 2D growth atop graphene is challenging, which agrees well with our experimental results described later. Conversely, a high adsorption to bulk cohesive energy ratio for III-N materials leads to successful 2D growth of GaN on graphene [69-72].

3.3 Calculation Details

The theoretical calculations were mainly based on 1) first-principles density functional theory (DFT) using the projector augmented wave method, 2) the generalized gradient approximation (GGA) using the Perdew-Burke-Ernzerhof (PBE) method [73], and 3) localized density

approximation (LDA) using the Perdew-Zunger (PZ) method as implemented in the Vienna abinitio simulation package (VASP) [74]. Using a semi-empirical correction to the Kohn-Sham energies [64], vdW interactions were taken into account for graphene/Ga (and As) pre-layer interfaces as well as for calculations of adsorption and migration energies of Ga, Al, In and As on graphene. A Monkhorst-Pack scheme was adopted to integrate over the Brillouin zone with a k-mesh of $9 \times 9 \times 1$. A plane-wave basis kinetic energy cutoff of 400 eV was used. All structures were optimized until the largest force on the atoms was less than 0.01 eV/Å. Calculations of the migration energy were performed using the nudged elastic band (NEB) method.

For calculations of the surface energy, repeated slab geometries were used to perform total energy calculations. The slab contained two layers of graphene followed by two monolayers of Ga atoms, one layer of InSe, one layer of h-BN, or on layer of MoS₂ depending which material is studied. InSe, h-BN and MoS₂ will be discussed in 3.5. In the case of Ga terminated graphene, Ga atoms were arranged on the graphene surface assuming that the GaAs nanostructure grows along the zinc-blende (111) direction normal to the surface. To account for the lattice mismatch between graphene and GaAs we constructed a supercell consisting of a 5×5 layer of graphene with a 3×3 layer of Ga atoms. A vacuum gap of 15 Å was introduced between neighboring slabs to avoid spurious interactions. A similar approach was used to construct a supercell with an As-terminated pre-layer on bilayer graphene. The asymmetry of the adsorbed pre-layer along the *z*-direction was considered by passivating the topmost Ga/As layer with pseudo-hydrogen atoms fractionally charged with 0.75e.

To model the adsorption energies of AlGaInAs atoms on a graphene bilayer, the adsorption was modeled using a single atom on a $5 \times 5 \times 1$ bilayer graphene sheet. Adsorption was modeled on

the bridge (B), top (T) and hollow (H) sites of the graphene lattice as illustrated in Figure 3.2. The B site is the adsorption site directly above the C-C bond of the graphene lattice, the H site is the adsorption site above the center of the honeycomb ring formed by the carbon atoms, and the T site is the adsorption site directly above a carbon atom.

To account for spurious dipole interactions between periodic images of the slab with the adsorbed adatom, self-consistent corrections to the potential and energy were applied [75]. For each calculation over an adsorption site, the adatom was relaxed along the *z* direction, and the carbon atoms in all directions, until forces on the ions were less than 0.05 eV/A.

3.4 VdW hetero-interface study

This interface energy of GaAs/graphene in J m⁻² represents the interface energy $\sigma_{GaAs/2D \text{ interface}}$ in equation (1). In this section, the interface between zinc-blende (ZB) and wurtzite (WZ) GaAs on graphene was compared using ab-initio calculations. A $4 \times 4 \times 1$ atom graphene supercell was used with a $5 \times 5 \times 1$ atom GaAs supercell. The graphene was Ga-terminated in the GaAs/graphene interface. To saturate the dangling bonds, pseudo-hydrogen atoms with a fractional charge of 0.75e were used. The binding energy, E_{binding} , was calculated using the following expression

$$E_{\text{binding}} = E_{\text{GaAs/graphene}} - E_{\text{graphene}} - E_{\text{GaAs}}$$
(4)

where $E_{\text{GaAs/graphene}}$ is the ground state energy of the GaAs/graphene heterostructure, E_{graphene} is the ground state energy of the $4 \times 4 \times 1$ graphene supercell and E_{GaAs} is the ground state energy of the GaAs supercell.

To understand the nature of the heterointerface, the binding energy between graphene and the ZB and WZ GaAs surfaces was calculated. The binding energy describes the strength of the interactions at the epitaxial interface. Table 3.4 summarizes the binding energies between the ZB GaAs (111) surface and WZ GaAs (0001) surface with graphene. The energies for a pristine interface and one with a single point defect were compared. A point defect was introduced by the removal of a single Ga atom at the Ga-terminated graphene/GaAs interface.

Table 3.4: Binding energy values of zinc-blende and wurtzite GaAs surfaces on graphene. The values are calculated using equation (4) shows that the ZB GaAs(111) phase is the preferred orientation on graphene; where the ground state energy for this configuration is 8.1 meV/C-atom lower than the energy of WZ GaAs phase on graphene. (From the author's publication [76]).

| | Binding Energy/C atom (meV) | | |
|------------|-----------------------------------|---------------|--|
| | Zinc blende GaAs (111) Wurtzite G | Wurtzite GaAs | |
| Pristine | -43.21 | -35.11 | |
| Ga-vacancy | -43.18 | -33.98 | |

Calculations of the binding energy indicated that the ZB GaAs(111) phase is the preferred orientation on graphene; the ground state energy for this configuration is 8.1 meV/C-atom lower than the energy of WZ GaAs phase on graphene. With a single point-defect at the interface, the

ZB GaAs phase remains the preferred orientation. Prior studies have demonstrated that the epitaxial relationship formed by GaAs and graphene can be affected by the orientation, strain, and defect density at the interface, among other factors [77]. A detailed calculations could elucidate which of these mechanisms governs the preferred GaAs phase when epitaxially grown atop graphene.

Because interfaces dominated by vdW forces are known to lead to turbostratically misoriented interfaces, the effect of misorientation between the graphene-GaAs interface on the binding energy was also investigated. The binding energy is maximum for the misoriented structure and minimum for the unrotated graphene/GaAs structure. The binding energies calculated as a function of rotation angle in Figure 3.3 are the same order of magnitude as the binding energy of graphene on Cu(111) surfaces, where the interactions at this interface are also dominated by vdW forces. This would suggest that the graphene-GaAs interface is also governed by vdW interactions. This binding energy in J m⁻² represents the interface energy $\sigma_{_{GaAs/2D interface}}$ in equation (1). The stronger binding energy in the misoriented structure suggests that the strain in this structure is minimized. Furthermore, this higher binding energy would also suggest that the graphene-GaAs interface is likely to be misaligned when an epitaxial interface is formed, with an unrotated interface being the least preferred orientation configuration. The energy barrier to transition from a rotated interface to an unrotated interface in the graphene/GaAs structure can be as large as 0.13 J/m^2 . For the supercells simulated, the total energy difference between the unrotated structure and the rotated structures was greater than the thermal energy $k_{\rm B}T$ at room temperature. This would suggest that the interface between GaAs and graphene may remain misaligned at 300 K and some higher growth temperatures as well.



Figure 3.3: Binding energy of the graphene/GaAs interface as a function of misorientation angle. The calculated binding energies are normalized with the planar area of the supercell used. This binding energy represents the interface energy $\sigma_{GaAs/2D \text{ interface}}$ in equation (1). This figure shows that binding energy is maximum for the misoriented structure and minimum for the unrotated graphene/GaAs structure. The energy barrier to transition from a rotated interface to an unrotated interface is 0.13 J/m². (From the author's publication [76]).

3.5 Candidate QvdWE buffer layer materials

After a detailed study of graphene as potential candidate for III/V semiconductor heteroepitaxial growth on layered materials, other van der Waals materials were considered, looking in particular for a relatively high surface free energy and high adsorption energy for III/As elements on the layered material. As wafer-scale growth of single monolayers of alternative vdW materials such as Hexagonal Boron Nitride (h-BN), Molybdenum Diselenide (MoS₂) and Indium Selenide[78] approach the same quality as graphene, we considered the possibility of using these prototypical vdW materials as a buffer layer for our quasi-vdW epitaxy approach. Adsorption energy calculations were used to determine if monolayer and bilayer MoS₂, h-BN and InSe would act as suitable buffer layers to achieve QvdWE of GaAs. For calculations of the adsorption energy of Ga, Al, In and As on h-BN, MoS_2 and InSe, a $4 \times 4 \times 1$ atom supercell of monolayer (1L) MoS₂ and monolayer and bilayer (2L) h-BN were used. For MoS₂, the 4p, 5s, 4d and 3s, 3p orbitals of Mo and S, respectively were treated as valence orbitals in the PBE functional. For h-BN, the 2s, 2p orbitals of B and N were treated as valence orbitals. Calculation details for the adsorption energy used were presented in detail in Section 3.3. Our studies of Al, Ga, As, and In adsorption on graphene shown in Table 3.2 have shown that each element binds with approximately the same binding energy onto single layer and bilayer graphene; the favored binding site on the honeycomb lattice of graphene is unique to each element. Hence, the binding energy of the defect-free GaAs surface is determined by the orientation of the Ga and As atoms above the honeycomb lattice. Table 3.5 summarizes the adsorption energy values for Al, Ga, As and In on h-BN, MoS₂ and InSe.

Table 3.5: Adsorption energies of Ga, Al, In and As on monolayer (1L) and bilayer (2L) h-BN, MoS_2 , and InSe. The favored adsorption site for each element and vdW material is listed in parentheses; for h-BN the favored site for the adatom is on top of nitrogen (TN) or on top of the boron-nitrogen bond (B), for MoS_2 the favored site is on top of the sulfur atom (T), and InSe the favored site is on the hollow between the Selenium atoms (H).

| Adsorption Energy | | | | |
|-------------------|------------|-----------|--------------|--|
| | 1L h-BN | 1L-MoS2 | 1L-InSe (eV) | |
| | (eV/atom) | (eV/atom) | | |
| Ga | 0.131 (TN) | 0.234 (T) | 2.25(H) | |
| Al | 0.135 (TN) | 0.237 (T) | N/A | |
| In | 0.067 (B) | 0.573 (T) | N/A | |
| As | 0.297 (B) | 0.527 (T) | 5.19 (H) | |

The adsorption energy at each binding site for monolayer MoS₂ and monolayer and bilayer h-BN is approximately an order of magnitude lower than the adsorption energies calculated for Ga, Al, In and As on graphene. However, the adsorption energy of Ga and As on InSe is higher than that for graphene by a factor of three. Thus, this calculation suggests that GaAs can be adsorbed (stable) on InSe surface. In chapter 5, experimental demonstration of GaAs heteroepitaxial growth on InSe will be described.



Figure 3.4: Projected density of states for Ga adsorbed on the T-site of the MoS₂ supercell, total density of states (blue), Mo states (red), S states (green) and Ga states (magenta). Inset: Schematic of $4 \times 4 \times 1$ MoS₂ supercell with Ga adatom over S atom. The low adsorption energy can be attributed to the weak hybridization of sp² orbitals of Ga with the 4d and 3p orbitals of Mo and S, respectively. (From the author's publication [76]).

The strength of the adsorption energy can be characterized by the hybridization of the adsorbed elements on the vdW buffer layer material. Figure 3.4 illustrates the projected density of states of a Ga atom adsorbed on the T-site of a monolayer MoS₂ supercell. The sp² orbitals of Ga are weakly hybridized with the 4d and 3p orbitals of Mo and S, respectively. This is evidenced by the weak overlap of the Ga orbitals with the Mo and S orbitals of the valence band in MoS₂. In contrast, strong hybridization between the sp² orbitals of Ga with the sp² orbitals of carbon in graphene results in larger adsorption energies. The adsorption of Ga, Al, In and As atoms on 1L

and 2L h-BN also results in weak hybridization with the sp^2 orbitals of boron and nitrogen, which leads to lower adsorption energies when compared to graphene. The lower adsorption energies of Ga, Al, As and In atoms on the MoS₂ and h-BN surfaces would result in these adatoms being poorly anchored during the growth process, which in turn would lead to degradation of the morphology of the GaAs film. These initial calculations suggest that MoS₂ and h-BN cannot be used as a buffer material to enable QvdW epitaxy of III-As/ 2D.

3.6 Summary:

In summary, we have reported a detailed theoretical study of MBE-grown GaAs thin films on graphene from a thermodynamic perspective, where the surface free energy was calculated for different layered materials. Among them, Ga-terminated graphene and InSe showed the highest surface free energy to promote layer-by-layer quasi-van der Waals heteroepitaxial growth. From the growth kinetics perspective, we conclude that InSe has the highest adsorption energy for As, indicating that the growth should be initiated by an As-terminated InSe surface, while Ga-terminated graphene is more likely to give thin film GaAs growth. In general, InSe and graphene are more suitable than h-BN and MoS_2 for the growth of 3D materials on 2D layered surfaces.

Chapter 4 Quasi van der Waals heteroepitaxy of GaAs on graphene/Si

4.1. Experimental Procedure

Multi-layer graphene (MLG) flakes were used as a vdWE buffer layer, and GaAs was deposited on MLG/Si (111) substrates using a Perkin-Elmer 430 MBE system as described in chapter 2. Material characterization was performed using a field emission scanning electron microscope (FESEM, JEOL, JSM-6700F), atomic force microscope (AFM, VEECO Nanoscope IIIa Multimode SPM) in the tapping mode and a double axis x-ray diffractometer (XRD, Bede D1 diffractometer equipped with a MaxfluxTM focusing graded x-ray mirror) with a monochromatic CuK α ($\lambda = 1.5405$ Å) radiation source. Raman spectra of MLG surfaces and as-grown GaAs films were collected at room temperature (RT) by using a Renishaw Raman microscope with a 514 nm excitation laser.

4.2. Graphene Quality and sample preparation

A 1 cm \times 1 cm piece of Si was first rinsed in acetone and isopropanol (IPA) for five minutes. Then, graphene flakes were mechanically exfoliated onto non-HF-treated Si by the well-known scotch-tape technique [33] as shown in Figure 4.1(a). Finally, the Si substrate with MLG was again cleaned using acetone and IPA to remove any residual organics from the exfoliation process. The corresponding microscope image is presented in Figure 4.1(b), showing the MLG flakes on the crystalline Si substrate covered with native SiO₂. Prior to GaAs growth, it is important to evaluate the quality of the exfoliated MLG layers. This was done by characterizing the crystallinity and surface morphology of MLG flakes using Raman spectroscopy and AFM, respectively. Figure 4.1(c) shows the Raman spectrum of exfoliated MLG flakes on Si, showing the main features of graphene, which are the *D*, *G* and *G'* bands. Among these bands, the main peaks are the so-called *G* and disorder-induced *D* peaks, which lie at 1580 and 1348 cm⁻¹, respectively. The integrated intensity ratio I_D/I_G for the *D* band and *G* band is less than 0.1, indicating high-quality multi-layer graphene [79]. Figure 4.1(d) shows the corresponding AFM image for the same MLG flake. The layers exhibit an atomically smooth surface morphology with a peak-to-peak variation of around 0.6 nm and a root-mean-square (RMS) roughness of 0.2 nm.



Figure 4.1: (a) Mechanical exfoliation of multi-layer graphene (MLG) flakes using Scotch-tape.(b) Optical microscope image, and (c) Raman spectrum for the exfoliated MLG. (d) AFM image

of the magnified area in (b) for the exfoliated MLG on SiO₂/Si showing an ultra-smooth surface morphology. (From the author's publication [26]).

4.3. Experimental Results

To achieve high quality epitaxial growth, the nucleation step plays a significant role and influences the film properties, morphology, homogeneity, defect densities, and adhesion. Although the influence of the substrate on nucleation behavior is well understood from conventional nucleation theory [80], there is limited understanding on the impact of the substrate on the nucleation layer growth in QvdWE using a buffer layer. To develop a detailed understanding of the nucleation and growth behavior of GaAs on Si via QvdWE, GaAs films were grown on MLG using As or Ga pre-layers, and two-step growth. These grown layers were studied using a combination of SEM, AFM and XRD in order to optimize film quality. Prior to presenting our results, a short description on the preparation for each set of growth conditions will be provided.

4.3.1. GaAs Growth on As-terminated MLG Surface

The acetone-IPA-cleaned exfoliated-MLG/Si samples were degassed at 300°C for 10 min in the buffer tube of our MBE system prior to loading into the growth chamber. The sample was exposed to As flux with a beam-equivalent pressure (BEP) of approximately 1×10^{-6} Torr. While exposed to the As flux, the substrate temperature was ramped to 400 °C to initiate growth by concurrent introduction of Ga at a nominal growth rate of 0.25 Å/s. After the growth of 25 nm of GaAs, the Ga shutter was closed and the substrate was cooled down below 150 °C in the presence of the As flux before unloading.

From a thermodynamic point of view, it is expected that the GaAs on MLG/Si system would exhibit island mode growth caused mainly by the low surface energy of graphene. From our theoretical investigations described in chapter 3, an As-terminated graphene surface will lead to approximately an order-of-magnitude larger surface energy from 48 mJ m⁻² to 570 mJ m⁻² upon sticking. However, due to their low adsorption energy (i.e., large bond distance) on graphene as we showed in Table 3.2, As atoms failed to stick to the graphene surface at high temperatures. Moreover, due to the chemical inertness of the graphene surface, the migration energies of both Ga and As atoms are low at high temperatures (Table 3.2). Thus, the diffusion length of Ga and As atoms is expected to be very high, leading to the most favorable thermodynamic growth mode. Taking this into account, the deposition of the GaAs nucleation layer was performed at temperatures as low as 400 °C to reduce the diffusion length of incident atoms on the graphene. Note that the optimal temperature for GaAs epitaxial growth is 575–600 °C [81].



Figure 4.2: Schematic cross-section views and SEM plan-view images of the surface of As-terminated GaAs grown on multi-layer graphene/Si with V/III ratios of (a) 25 and (b) 10 showing island growth and the formation of 1D nanorods, respectively. (From the author's publication [26]).

Unfortunately, even this reduced growth temperature failed to prevent the clustering of GaAs into islands atop graphene, mainly because of the low migration energy of Ga and As atoms on graphene, as mentioned previously. This leads to a poor-quality GaAs film due to island growth in the early stage of the nucleation process. Figure 4.2(a) shows an SEM image of GaAs grown at a V/III ratio of 25 on MLG/Si substrates. According to prior published data [43], we would

still expect that some grains could be epitaxial and that their orientations are sensitive to the substrate temperature.

To facilitate the nucleation process or achieve good anchoring of GaAs atoms on graphene, a second growth was performed with a V/III ratio as low as 10. A lower V/III ratio under otherwise the same growth conditions creates Ga droplets on graphene, which act as nucleation sites for the formation of GaAs nanorods (NRs) besides GaAs parasitic crystals, as shown in the SEM image in Figure 4.2(b). These NRs are present at low density on graphene mainly due to the lack of these Ga droplets. Using a Ga pre-layer (i.e. Ga-terminated surface) followed by such a low V/III ratio and a higher growth temperature would increase the number density of these NRs significantly. The length of the NRs is approximately 100 nm, which is much greater than the nominal thickness of the film. Thus, a high V/III ratio is needed to limit the diffusion of Ga and As, leading to higher nucleation density.

4.3.2. GaAs Growth on Ga-terminated MLG Surface

Since Ga has higher adsorption energy on graphene than As [65], it is expected that the surface diffusion length of Ga and As on graphene will be reduced and the density of nucleation sites for GaAs growth will be increased [82, 83]. According to the calculations in chapter 3, the surface energy of graphene is increased to 0.43 J m⁻² from 52 mJ m⁻² with the introduction of a Ga prelayer. Thus, we would expect that a further reduction of the growth temperature with a Ga prelayer to increase the wettability of the graphene surface could facilitate the nucleation process.

As part of the optimization of the 2D growth of a GaAs nucleation layer on graphene/Si substrates, a range of Ga pre-layer thicknesses was explored. Approximately two monolayers of gallium atop the graphene surface prior to growth yielded the best results in terms of the surface

morphology and material quality, as determined by SEM, AFM and Raman data. In fact, fewer or more than two monolayers of gallium yields a rough GaAs surface and low transverse-optic (TO) to longitudinal-optic (LO) Raman intensity ratio (I_{TO}/I_{LO}) [84, 85]. It should be noted that such Ga pre-layer deposition was performed at room temperature to achieve a good sticking rate of Ga atoms on graphene, as well as to prevent the Ga clustering observed to occur in highertemperature depositions. GaAs growth was begun at temperatures as low as 350 °C to avoid islanding and to enhance the nucleation process. This low nucleation layer growth temperature was optimized based on the results of several growth runs as shown in figure 4.3 and figure 4.4. The roughness of the grown GaAs increased after 350°C because the crystal start to take the thermodynamically most favorable island growth mode along with enhanced crystal quality compared to low temperatures. Note that the growth was performed with a V/III ratio of 25, but the growth rate varied under these conditions.



Figure 4.3: The full width at half maximum (FWHM) of the (111) diffraction peak (the rocking curve full width at half maximum) as a function of GaAs film growth temperature on Graphene/ Si substrate. The crystal quality enhanced at higher growth temperatures compared to low temperatures.



Figure 4.4: Root-mean-square (RMS) roughness value as function of GaAs film growth temperature on Graphene/ Si substrate. The RMS value was measured over an area of 1 μ m². The roughness of the grown GaAs increased after 350°C because the crystal start to take the thermodynamically most favorable island growth mode in the case of GaAs/ graphene.

Figure 4.5(a) shows an SEM image of GaAs grown on a Ga-terminated MLG surface at growth rate 0.25 Å/s. For the first few layers, GaAs forms widely separated islands around nuclei, and then the islands coalesce as the growth proceeds. The extremely thin Ga pre-layer was observed to have a macroscopic effect on the growth of the GaAs nucleation layer. A comparison of the surface morphologies of the structures grown with (Figure 4.5(a)) and without (Figure 4.2(a)) a Ga pre-layer shows noticeable differences. This marked difference can be attributed to a

difference in the wetting angle between MLG and islands in the overlayer, enhancing the 2D nature of growth. Bringans et al. reported that at the initial stage of epitaxy in the GaAs/Si system, a reduction of the wetting angle between the substrate and the overlayer islands could be achieved through the use of a Ga pre-layer, resulting in a smoother surface morphology [82]. In addition to the effect of Ga pre-layer, the growth rate was also observed to have a significant effect on the surface morphology in the 2D growth mode. This is demonstrated in Figure 4.5(b), where a lower growth rate of 0.15 Å/s yielded a smoother GaAs surface. Surface RMS roughnesses as low as 0.6 nm were observed, corresponding to around two monolayers of GaAs, as well as a peak-to-peak height variation of only 3 nm as measured by AFM. This smooth nucleation layer is considered to have an acceptable roughness for subsequent growth of overlayers. To our knowledge, this result is the first illustration of an ultra-smooth morphology for GaAs films on vdW material. This smooth surface could possibly be attributed to a large diffusivity (D) to deposition flux (F) ratio that allows adatoms to reach the surface potential minimum, enhancing the 2D growth of GaAs. In other words, a large value of D/F promotes growth close to the equilibrium condition, allowing the adsorbed species sufficient time to explore the potential energy surface for nucleation so that the system reaches a minimum energy configuration [84, 86]. Hence, the following well-known condition [87] for step nucleation or layer-by-layer growth is satisfied by the dimensionless parameter α

$$\alpha = \frac{Fw^2 a^2}{D} < 1 \tag{4}$$

where *a* is the in-plane lattice constant of graphene and *w* is the terrace width of exfoliated MLG.



Figure 4.5: SEM plan-view images of the as-grown structure with V/III ratios of 25 and at growth rates of (a) 0.25 Å/s, (b) 0.15 Å/s, (c) schematic cross-sectional view of the GaAs grown with Ga pre-layer on multi-layer graphene/Si, and (d) AFM image of the 1.2 μ m × 1.2 μ m region marked with a red square in (b), showing the surface morphology of the nucleation layer. (From the author's publication [26]).

The crystalline quality and the epitaxial orientation of as-grown GaAs films were characterized by Raman spectroscopy and XRD. Figure 4.6(a) shows the micro-Raman spectrum in which two GaAs Raman signature peaks corresponding to the transverse optic (TO) and longitudinal optic (LO) vibrational bands are located at 268 and 292 cm⁻¹, respectively. The presence of the forbidden but intense TO mode in the spectrum results from the defects in the nucleation layer. The crystalline quality of such a GaAs epi-layer was qualitatively evaluated by the ratio of TO and LO intensities (I_{TO}/I_{LO}), which is measured to be as high as 1.8, indicating incomplete crystallization of the GaAs.

The crystallographic orientation of as-grown GaAs films is mainly defined by the underlying graphene layer, exhibiting triangular lattice symmetry. The Si substrate will have a negligible influence on the orientation of the grown layer. Moreover, the crystalline quality of the thin GaAs film on Ga-terminated graphene was characterized by XRD omega-rocking curve scans as displayed in Figure 4.6(b). Such GaAs films are found to have broad rocking curves at the Bragg angle. The rocking curve FWHM value for the GaAs (111) plane is as high as 240 arcsec (0.065 deg), indicating that the crystal quality needs to be improved. Despite the poor crystal quality, the low-temperature grown GaAs has a strong (111) oriented fiber-texture. This is clearly an essential step towards epitaxy.

Prior reports of the x-ray rocking curves for GaAs on Si [8] show that that a FWHM value of 240 arcsec was attained by employing micron-thick GaAs films. In contrast, our approach achieved the same FWHM with GaAs film thicknesses on the order of 25 nm. The two orders of magnitude improvement in the quality of our GaAs films can be attributed to the graphene buffer layer mitigating lattice and thermal mismatch between GaAs and the underlying substrate.



Figure 4.6: (a) The room-temperature micro-Raman spectrum of the low-temperature-grown GaAs nucleation layer, and (b) the XRD omega rocking-curve scan of the GaAs(111) peak for this nucleation layer showing a narrow FWHM of 240 arcsec. (From the author's publication [26]).

4.3.3. GaAs Growth on MLG via Two-Step Growth

Two-step growth processes have already been proven to be a successful approach to depositing GaAs on Si [6, 88]. This concept could also be applied in our QvdWE, where a good-quality nucleation layer is formed at low temperature before high-temperature deposition of crystalline films. Achieving single crystalline GaAs on top of a graphene layer using a one-step growth process is challenging due to difficulties in obtaining a high-quality nucleation layer at a higher temperature. Such challenges stem primarily from the reduced adsorption and migration energies of incident atoms as well as the weak vdW forces that govern the interaction between graphene and GaAs at high temperatures.

After achieving a smooth nucleation layer of GaAs on MLG/Si (see Figure 4.5(b)), the substrate temperature was raised to 600 °C, the growth temperature of crystalline GaAs, for a second step growth at the top of the nucleation layer. The second step growth was performed at 1 Å/s and V/III ratio of 100, resulting in a film 200 nm thick. Figure 4.5(a) shows the SEM image of the GaAs after the two-step growth. We note that the clearly faceted morphology of the GaAs grains of the film indicate its untextured, polycrystalline nature, which is confirmed by the multiple diffraction peaks from (111), (200), (220), and (311) crystal planes in the XRD $\omega/2\theta$ scan as shown in Figure 4.5(b). The rough surface morphology of the GaAs after the second step growth also indicates that the underlying nucleation layer is insufficiently stable at the second-stage temperature.



Figure 4.7: SEM plan-view image of (a) 200 nm high-temperature grown GaAs on top of a 25-nm-thick nucleation layer, with Ga prelayer showing 3D cluster growth, which could be caused by the elevated temperature during the second step growth and (b) XRD $\omega/2\theta$ scan for GaAs grown by the two-step growth scheme, showing poly-crystallinity with the presence of GaAs (111), (200), (220) and (311). (From the author's publication [26]).

In order to avoid island growth during the temperature ramp-up in the two-step process, a growth was performed with a low-temperature nucleation layer as thick as 100 nm. Even this failed to prevent island formation. This suggests the GaAs/graphene interface is not stable at high temperatures. Such islanding of GaAs at high temperatures could be mainly caused by the low migration energies of Ga and As atoms on graphene, which continue to decrease with increasing temperature and are low enough for the adatoms to diffuse at low temperatures or even near room temperature. The low adsorption energy of Ga and As atoms on graphene also indicate a physical adsorption-like bonding, i.e., weak interaction between graphene and the adatoms. Moreover, the weakening of the physical vdW bonding with increasing temperature could also be a possible mechanism of island formation. High growth temperatures are required to crystallize GaAs and for the defects and dislocations to migrate in order to obtain high-quality GaAs. Unfortunately, in GaAs/graphene, the weak vdW forces that bond GaAs to graphene can be broken at high temperatures. A carefully optimized two-step growth process is essential to form a high-quality nucleation layer at low temperatures, followed by a temperature ramp-up that crystallizes the grown GaAs film.

4.4. Growth Model

Our model of the growth process of GaAs on MLG/Si is shown schematically in Figure 4.6. After the mechanical exfoliation of the MLG layer onto the silicon substrate, the QvdWE process begins either with a Ga or As pre-layer. With a Ga pre-layer, Ga atoms impinge on the room temperature MLG/Si surface to reduce the hopping rate of Ga atoms and to facilitate Ga atoms
sticking on the graphene uniformly (Figure 4.8-(ii)A). With an As-pre-layer, the MLG layer is terminated with As atoms at 400 °C. Although the Ga-terminated graphene has a lower surface energy, it is preferred over the As terminated graphene surface (Figure 4.8-(ii)B). This is because the As atoms do not adhere sufficiently to the graphene surface due to the lower adsorption energy for As compared to Ga, resulting in an island growth mode when both Ga and As are introduced for GaAs deposition at 400 °C (Figure 4.8-(iii)B). On the other hand, the growth temperature of 350 °C determined as the optimum for the approach with the Ga pre-layer facilitates GaAs nucleation on an otherwise inert graphene surface, where the diffusion length of adatoms is high. When Ga and As are introduced at 350 °C, they both react on the graphene/Si surface, to nucleate around Ga sites in islands. As the growth proceeds, the islands coalesce and eventually form a smooth film (Figure 4.8-(iii)A). This film is adhered to the graphene via vdW forces. For the small flakes characterized in our study, the strain at the interface is believed not to propagate from the interface, which limits the lattice mismatch and thermal expansion mismatch at the interface. Raising the temperature of this film to 600 °C causes GaAs to recrystallize into islands by breaking the weak vdW forces between graphene and GaAs (Figure 4.8-(iv)).



Figure 4.8: Schematic illustrations of the growth of GaAs on Si via QvdWE at different stages, (i) mechanical exfoliation of multi-layer graphene on Si substrate, (ii) growth initialization by covering the MLG surface with Ga prelayer at RT, (iii) deposition of a 2D nucleation layer at 350 °C and (iv) deposition of GaAs at 600 °C exhibiting a rough surface morphology with 3D islands due to the low adsorption and migration energies of Ga and As on graphene as presented in Table 3.2 in Chapter 3. (From the author's publication [26]).

To verify the crystalline quality of the material, the out-of-plane XRD θ -2 θ scan pattern was measured for GaAs films grown on large-area CVD graphene over a 2 θ range of 20 °- 60 °. The

graphene was grown epitaxially on Cu foil, then transferred onto the SiO₂/Si substrate [52]. As shown in Fig. 4.9(a), the θ -2 θ scan pattern is composed of zincblende (111), (200), (220) and (311) GaAs peaks with unequal intensities. Therefore, the grown GaAs film on CVD graphene is confirmed to be polycrystalline.

Pole figure measurement has been proven to be one of the most powerful XRD techniques for studying texture in thin films. The strong (111) peak at the center of the pole figure as shown in the 3D representation in Fig. 4.8 (b) indicates that the grown films are preferentially (111)-oriented along the surface normal. Also, the stereographic projection format of such a pole figure is shown as an inset in Fig. 4.8 (b). The FWHM of the surface normal peak and the degree of preferred orientation were calculated to be 1.5 ° and 2.2%, suggesting strong fiber texture in the GaAs films. In a previous study, it was reported that the (111) orientation is highly favored by the underlying graphene layer, which exhibits triangular lattice symmetry. It should be noted that the XRD θ -2 θ scan and pole figure data reported here were collected from a sample where the GaAs growth was performed on a blanket graphene layer on SiO₂/(111)-oriented silicon substrates. This clearly suggests that the silicon substrate will have a negligible influence in defining the orientation of the grown layer.



Figure 4.9: XRD analysis and pole figure of as-grown GaAs on CVD graphene, (a) HRXRD θ -2 θ scan, where the multiple peaks correspond to zincblende (111), (200), (220) and (311) GaAs. (b) The 3D pole figure of (111) GaAs, showing the preferred orientation in the grown films. The stereographic projection of the (111) pole figure is shown as an inset. (From the author's publication [76])

Selected area electron diffraction (SAED) patterns obtained from the GaAs layer in both samples contain a series of rings, which indicates the presence of a polycrystalline material. Using the diffraction pattern of the single-crystal Si substrate as a reference, the lattice plane spacings of the diffraction pattern and the relative intensity of the diffraction rings would suggest that a majority of GaAs is grown in the cubic zincblende phase. Figure 4.10 shows a high-resolution lattice image of an approximately 100 nm thick GaAs layer containing two grains in which a <110> direction is aligned close to parallel to the electron beam (see enlarged areas). The lattice fringe patterns observed are consistent with these grains being zincblende in structure, which is in good agreement with the theoretical findings in section 3.4. Defects in GaAs such as

microtwins and stacking faults were observed within some of the grains. The typical grain size observed was approximately 100 nm where the GaAs layer was between 20-60 nm thick.



Figure 4.10: Cross-sectional TEM image near the interface between GaAs film and CVD-graphene/SiO₂. Magnified TEM images of the areas in the red squares. To maximize ease of interpretation, the film growth direction is along the vertical direction of images. The corresponding SAED ring pattern is shown as an inset. (From the author's publication [76]).

4.5. Summary and conclusions

This study is a first step in the direction of achieving of high-quality single crystal GaAs on Si taking advantage of vdW epitaxy using graphene as a buffer layer. Further optimization of the growth parameters, such as use of the proper buffer material and optimization of the growth kinetics based on the results of GaAs heteroepitaxy on graphene will help us to integrate single-crystal 2D GaAs on Si. Based on our preliminary studies of GaAs growth on Graphene/Si, we have concluded that the main points that need to be addressed for successful epitaxial growth of a III/V crystal layer on 2D /Si are as follows:

• Low free surface energy of layered materials.

Due to low surface energy of 2D materials as mentioned in 3.1 of Chapter 3, 2D materials exhibit a high surface tension, so deposited GaAs films will tend not to wet the buffer surface, resulting in island growth, which is empirically associated with high defect densities.

• Low adsorption energies of III/V ad-atoms on layered materials.

Al, Ga, In, As atoms for the III-As material system exhibit very low adsorption energies on graphene as was shown in Table 3.2 of Chapter 3, which makes it difficult for GaAs to be stable atop a layered material surface, especially at high growth temperatures where the adsorption rate depends exponentially on the growth temperatures (Section 1.4.1)

• Lattice mismatch between III/V and 2D material.

Although the growth of 2D materials on top of Silicon substrates is not constrained by the lattice mismatch between the grown layered material and Silicon substrate, the growth of 3D/2D is still constrained because of the nature of covalent bonding at the 3D/2D interface plays a role in defining the quality of the grown 3D material.

Chapter 5 High-quality and defect-free GaAs on Si(111) substrates by Quasi van der Waals heteroepitaxy of GaAs/ InSe/Si

5.1. Compatibility of InSe as a buffer layer for GaAs/Si system:

Based on the results of the previous experiments on GaAs growth on graphene, an ideal vdW layered buffer material should satisfy the following: First, relatively high adsorption energy to wet the buffer, leading to layer-by-layer growth. Second, high adsorption energy for III-V elements on its surface to ensure the stability of the grown III-V semiconductor layer on top of the layered buffer. Third, the buffer layer needs to be lattice-matched to the grown III-V semiconductor, to avoid any twins caused by lattice mismatch. This is consistent with previous studies [89] where significant reductions of twin domains were observed when a lattice-matched InP (111) substrate was used to grow Bi₂Se₃, where one orientation with respect to the substrate lattice was believed to be stabilized by nucleation of the film at step edges of the substrate. Figure 5.1 shows the lattice constants of different 3D semiconductors and layered materials plotted against their energy gaps at room temperature. In addition, having the vdW buffer able to be grown on the Silicon substrate using MBE is an advantage over other methods, such as transferring layers onto silicon, to ensure cleanliness and compatibility with UHV systems used for other subsequent growth steps.

Indium Selenide (InSe) is a layered semiconductor with a crystal structure composed of units of four repeating layers of atoms, in the order Se-In -In-Se, which are called quintuple layers (QLs). Between these QLs, the bonding is of the van der Waals type. These weak interfacial bonds

make these materials fairly easy to grow using van der Waals epitaxy on many different substrates, even for large lattice mismatches or even different lattice symmetries. The lattice parameters of β -InSe are a = 4.005 Å and c = 16.64 Å with space group $P6_3/mmc$ as reported by Popovic' et al. [90]. The in-plane lattice constant matches the GaAs lattice constant, making it a suitable buffer. In addition, it has a relatively high surface free energy compared to other layered materials, as our DFT calculations showed in Chapter 3, with a free surface energy of 152 mJ/m², which is five times the surface free energy of graphene. Furthermore, the high adsorption energy of Arsenic atoms on the InSe surface facilitates the nucleation of GaAs by terminating the InSe surface with As atoms.



Figure 5.1: Lattice constants and energy gaps at room temperature of different 3D semiconductors and layered materials. Various 3D semiconductors are marked by blue stars, while layered materials are marked by red stars.

To improve the nucleation of GaAs on InSe /Si, a miscut vicinal Silicon substrate on which a sequence of steps exist was adopted. Step edges have dangling bonds, favoring strong chemical interaction. Therefore, these step edges can promote a single, substrate-lattice-aligned domain on InSe, where a step-flow growth mode takes place suitable for subsequent GaAs epitaxial growth [91]. Figure 5.2 shows the atomic geometry of the GaAs / InSe /Si (111) epitaxial structure,

where GaAs and InSe are attached to each other by a combination of van der Waals interactions and covalent bonds.



Figure 5.2: Atomic geometry of GaAs /InSe /Si (111), where GaAs and InSe are attached to each other by by a combination of van der Waals interactions and covalent bonds. The miscut of the silicon substrate imroves the nucleation of GaAs on top of InSe/Si (111).

In our growth model, GaAs epitaxial growth was performed on a tilted substrate 4 degrees off Si(111) [11, 92]. Using miscut substrates allows us to overcome the low surface free energy of layered materials that prevents epitaxial growth in layer-by-layer mode, creating step edges on the layered material by growing the InSe on the miscut silicon (111) substrate. These step edges

act as nucleation sites, which improve the nucleation and GaAs coverage on such surfaces. This can be mainly attributed to the higher surface free energy at the step edges than the terrace surface. The InSe film grows with the c-axis oriented out-of-plane, which explains why substrate surfaces with hexagonal lattice symmetries, such as the (111) surfaces of cubic crystals, are the natural choice for InSe epitaxial growth on such substrates [91].

The InSe buffer can accommodate a lattice mismatch of 4.2% with the Silicon substrate, reflecting the advantage of 2D/3D quasi van der Waals epitaxy [39, 93]. Earlier studies of Bi_2Se_3 epitaxial growth on Si:H showed that the lattice constant of the growing Bi_2Se_3 evolves with deposition coverage, with the lattice constant expanding to 4.18 A° at one quantum layer thickness before gradually coming back to the bulk lattice constant of 4.14 A°. This indicates that because of the weak vdW bonding, the growth of Bi_2Se_3 is quite tolerant of the choice of substrate [91].

5.2. Experimental procedure:

The InSe thin film was grown in ultrahigh vacuum on Si (111) substrates using a Perkin-Elmer molecular beam epitaxy (MBE) system. In preparation for InSe epitaxial growth, the Si substrates were cleaned using the well-known RCA process. Next, the substrates were immersed in a 5% hydrofluoric acid (HF) solution for 30 seconds at room temperature (RT), to etch the thin oxide layer. Next, the cleaned samples were loaded into growth chamber of the MBE system and degassed at 550 °C for 15 min to desorb hydrogen atoms on the surface. After this step, high-quality layered InSe was epitaxially grown on Si under a Se-rich beam equivalent pressure of around 5 x 10^{-2} Torr. Real-time monitoring of the growth was carried out during the growth by reflection high-energy electron diffraction (RHEED). High-purity In (99.9995 %) was

evaporated from a conventional effusion cell at 800 °C, while Se (99.99%) flux was created from a cracking cell (SVTA) at 290 °C. Two-step growth with an annealing process was employed. Initially, a 1 nm - thick InSe layer was deposited at 190 °C and annealed at 600 °C under Se flux to form a high-quality interfacial layer. Then, a 4 nm-thick InSe film was grown at 380 °C, for which the growth rate was 400 sec/nm. Fig. 5.3 (a) shows a θ -2 θ scan of an InSe film grown on Si (111) indicating the presence of a small amount of InSe at (004) peak. The corresponding AFM image with RMS value of 0.34 nm and the RHEED pattern of the surface of InSe with a thickness of 6 nm are shown in figure 5.3 (b, c). The sharp streaky RHEED lines indicate atomically flat surface morphology.



Figure 5.3: (a) X-ray diffraction (XRD) θ -2 θ scan of InSe film grown on Si (111). (b) RHEED pattern of InSe surface after the growth on Si (111). (c) AFM image of the InSe film grown on Si (111) showing an ultra-smooth surface morphology, where the steps of the silicon substrate are reflected on the InSe thin film.

The grown InSe sample was loaded immediately in the As chamber for subsequent GaAs growth. The sample was exposed to As flux with a beam equivalent pressure (BEP) of approximately 1×10^{-6} Torr. While exposed to the As flux, the substrate temperature was ramped to 590°C to degas the InSe layer, then the temperature was lowered to 575°C to initiate growth by concurrent introduction of Ga at a nominal growth rate of 0.1 Å/s. After the growth of 50 nm GaAs, the growth rate was increased to 0.77 Å/s to grow a total of 300 nm GaAs. Then, the Ga shutter was closed and the substrate was cooled down below 150 °C in the presence of the As flux.

The surface morphology of the as-grown material heterostructures was characterized by atomic force microscopy (AFM, VEECO Nanoscope IIIa Multimode SPM) in the tapping mode. The structural quality of both InSe and GaAs was determined using a high-resolution x-ray diffractometer (XRD, Bruker D8 Discover) with a monochromatic CuK α ($\lambda = 1.5405$ Å) radiation source operated at 45 kV and 40 mA. The structural characteristics of the InGaAs/GaAs multilayer structure were then investigated by cross-sectional transmission electron microscopy (TEM, Tecnai F20, operated at 200 keV). Photoluminescence spectra from InGaAs/GaAs QWs on the as-grown heterostructures were collected using a frequency-doubled diode pumped Nd:YAG laser ($\lambda = 532$ nm). The PL was collected by a 50× objective lens, and recorded by a CCD camera.

5.3. Experimental Results:

The atomic steps on the thin layered InSe surface are attributed to growth on the miscut silicon substrate, where these steps improve the nucleation process of the first few layers of GaAs due to

the increase of surface free energy at these edges. GaAs can still nucleate, as can be seen in the spotty RHEED pattern for the first three layers of GaAs on InSe. As growth continues, streaky lines appear on the RHEED pattern, indicating layer-by-layer growth. To confirm the positive effect of the step edges on the InSe surface, InSe was grown on a planar Si (111) substrate for comparison. In the later growth stages, an island pattern appeared starting with the first layers and never merged to layer-by layer growth when the growth proceeded to form a thicker GaAs layer. In this sample the GaAs exhibited some steps, which were most probably caused by the nucleation process on InSe The growth of a 500 nm GaAs film on tilted InSe/ Si (111) revealed a single-crystal GaAs layer with extraordinary quality for such thicknesses on Si substrates. This can be attributed to the strain-free interface between GaAs and InSe. The InSe layer thickness of 6 nm is considered negligible compared to the total thickness of the structure. To improve the crystal quality further, a well-known technique of using ten periods of a strained InGaAs/ GaAs superlattice after the 50 nm nucleation layer of GaAs on InSe was employed [18, 20, 21]. This strained superlattice blocks the threading dislocations caused by island nucleation in the first three layers. An XRD scan of the 500 nm GaAs grown on 6 nm of InSe shows the sole peak of GaAs (111) in addition to the Si (111) substrate peak (Figure. 5.4.a).

The crystalline quality of GaAs films can be assessed using X-ray rocking curves for the GaAs (111) reflection. The full width at half maximum (FWHM) of the reflection peak (the rocking curve full width at half maximum) depends directly on the concentration of defects in the film.



Figure 5.4: (a) X-ray diffraction (XRD) θ -2 θ scan of GaAs film grown on InSe/ Si (111). (b) Rocking curve of the (111) peak. (c) AFM image of the InSe film grown on Si (111) showing an ultra-smooth surface morphology, where the steps of the silicon substrate are reflected on the InSe thin film. (d) TEM image of the GaAs (111)/ InSe interface.

Our grown GaAs film shows a FWHM value of 74 nm, which is the narrowest value ever reported for the same thickness of GaAs grown on Silicon (Figure. 5.4.b). The average crystallite size can be calculated from the FWHM value of the XRD omega scan peak to be 543 nm based

on the following Scherrer formula [94]:

$$D = \frac{1.2\lambda}{\text{FWHM}(2\theta) \times \cos\theta}$$

where the FWHM is measured for the most prominent XRD 2 θ peak, and D is the crystallite size. In our case, the dominant peak is GaAs (111) at around $2\theta = 27.3^{\circ}$. The AFM image at figure 5.4 (c) shows a root-mean-square (RMS) roughness value of 0.6 nm and the TEM image (figure 5.4 (d)) shows the local quality of the GaAs/InSe interface.

The optical quality of the GaAs layer was characterized using photoluminescence measurements at room temperature. The room temperature emission of this thin GaAs film integrated directly on Silicon was successfully demonstrated, with a FWHM value of 44.15 nm, indicating a sharp band-to-band radiative recombination emission. Figure 5.5 shows 300 K PL spectra of 500 nm GaAs grown on InSe/ Si (111) and an undoped GaAs (111) substrate as a reference. The unstrained energy gap of GaAs was taken from the main PL peak at 870 nm, which is due to the band-to-band transition for the GaAs substrate. A minimal redshift by 5 nm can be seen in the PL peak of GaAs / InSe/ Si (111), exhibiting a slight energy-gap shrinkage for the GaAs epilayer grown on InSe/ Si (111). This biaxial tensile strain in GaAs epilayers on Si can be attributed to the thermal expansion mismatch between GaAs and Silicon [95]. However, in our case the slight strain might be due the thermal expansion mismatch between GaAs and InSe, leading to a reduction of the band gap and a slight split in the valence band.



Figure 5.5: Photoluminescence (PL) spectrum at 300 K of planar 500 nm GaAs grown on InSe/ Si(111). A peak with FWHM value of 44.15 nm is presented in red, indicating a sharp band-toband radiative recombination emission. The peak is red shifted by 5 nm due the thermal expansion mismatch between GaAs and InSe. PL of GaAs(111) substrate is presented in black as a reference.

5.3.1. GaAs growth optimization:

To optimize the growth temperature of the GaAs initial layer on InSe /Si (111), the room temperature photoluminescence (PL) signal was used to find the conditions giving the minimum FWHM signal and the maximum intensity. Figure 5.6 shows that the GaAs initial layer grown at 575 °C shows the maximum intensity as well as the minimum FWHM of 21 nm. Optimizing the

initial layer is crucial for further growth steps to ensure a high quality nucleation layer. The In_x GaAs superlattice structure used in this heteroepitaxy was optimized to have In composition x= 0.1. The FWHM of the PL signal decreased and the PL intensity increases as the growth temperature increases mainly because the improved crystallization of GaAs at higher temperatures in the range of (550- 600) °C.



Figure 5.6: The full width at half maximum (FWHM) and intensity of GaAs thin film photoluminescence signal as a function GaAs initial layer growth temperature on InSe/ Si (111) substrate. The FWHM of the PL signal decreased and the PL intensity increases as the growth temperature increases mainly because the improved crystallization of GaAs at higher temperatures in the range of (550- 600) °C.

The in-plane quality of GaAs epitaxial film was evaluated by performing in-plane XRD rocking curve measurement. The FWHM of both in-plane and out-of-plane rocking curves were measured for different growth temperatures as displayed in figure 5.7. This measurement shows the GaAs growth temperature of 575 °C shows the minimum FWHM of both in-plane and out-of-plane rocking curves. Therefore, 575 °C was used as an optimum growth temperature of GaAs on film grown on InSe/ Si (111). It is noticed that the FWHM of out-of-plane XRD rocking curves have higher values for all growth temperatures indicating an inferior quality in the in-plane directions caused mainly by dislocations in this direction.



Figure 5.7: The out-of-plane and in-plane FWHM of the diffraction peak (the rocking curve full width at half maximum) as a function GaAs film growth temperature on InSe/ Si (111) substrate.

5.3.2. Our result compared to literature studies on heteroepitaxial growth of GaAs on Silicon

Using this novel buffer layer of InSe, we were able to achieve the best rocking curve FWHM ever reported for GaAs films grown directly on Si substrates. Figure 5.8 summarizes available experimental data from the literature in addition to our recent breakthrough. It is important to note that the dislocation density decreases with increasing film thickness and our GaAs film was only 500 nm thick, which is significantly thinner than other results.



Figure 5.8: Literature survey of the full width at half maximum (FWHM) of the (004) X-ray rocking curve versus film thickness for GaAs films on Si substrates. Our result is marked in red, showing the best result so far for direct integration of GaAs on Silicon. Reproduced from reference [8]. The references in the legend are from the original source in [8].

5.4. Integration of InGaAs/GaAs double heterostrucure (DH) onto GaAs/ Si (211) structure:

Bulk-terminated Si (211) is a stepped surface with a primitive cell of 9.41 A° in the [$\bar{1}$ 1 1] direction and 3.84 A° in the [0 $\bar{1}$ 1] direction [96]. Figure 5.9 illustrates the bulk-terminated (211) surface as a (111) + (001) step. Si (211), as a high-index crystallographic plane, has been conventionally used for epitaxial growth of III-V and II-VI compound semiconductors [97, 98]. In comparison experiments growing GaAs (211) versus GaAs (100) both homoepitaxially and heteroepitaxially on Si substrates, the (211) morphology, although better than that of (100)-oriented growth on Si substrates, was inferior to (100) growth on GaAs substrates [99]. High-Miller-index surfaces are interesting for several reasons. First, they exhibit combinations of bonding configurations which do not normally occur simultaneously on any given low-Miller-index surface. Second, the planes parallel to the interface contain equal numbers of cation and anion atoms, thus assuring a charge-free interface [100]. Last, step arrays on the Si (211) surface promote step flow growth by providing nucleation sites at the step edges and limiting the migration of the adatoms. This step flow growth mode can be enhanced by As passivation, which results in the reduction of twins in GaAs growth [101-103].



Figure 5.9: Bulk-terminated Si (211). (a) Schematic view of step planes. (b) Bulk-terminated Si (211): white balls make up the (111) plane; dark grey balls make up the (001) plane. Reproduced from reference [96].

From a surface energy point of view, Chadi's total-energy calculations for the (111) and for ideal and relaxed (211) surfaces show that the surface energy of the (111) surface is appreciably lower than that of the (211) surface. The surface energy is calculated to be 1.2 (eV/unit area) for the (211) surface as compared to a value of 1.06+0.06 CV/unit area for the (111) surface [100]. From the 3D/2D/ Si (211) perspective, the inherently stepped surface in the (211) orientation can provide nucleation sites and increase the coverage of GaAs on the layered material, Indium Selenide in our case, and limit the migration of Ga and As adatoms on the InSe surface.

Because layered InSe nucleates on the (111) orientation out of the c-axis plane, the growth of InSe is expected to be in narrow stripes following the (111) steps in the Si (211) substrate, with the high tilt angle of 19.47° making the dangling bonds of such layers exposed, which means a higher surface free energy to promote layer-by-layer growth. These edges of exposed dangling bonds are passivated by Arsenic for GaAs growth in the next heteroepitaxy process. Using Si

(211), GaAs quality and uniformity was superior to our previous results on Si (111).

The GaAs film, as characterized by AFM in figure 5.10, exhibits atomically smooth surface morphology. The peak-to-peak variation is only 4 nm with a root-mean-square (RMS) roughness value of 0.4 nm, which is lower than other reported values obtained on nominal Si substrates [17, 55].



Figure 5.10: AFM image of GaAs thin film grown on InSe /Si (211) showing an ultra-smooth surface morphology. The film has a RMS roughness value of 4 Å for an area of 1 μ m².

The crystalline quality of a GaAs thin film grown on InSe/ Si (211) was characterized by XRD omega-2 theta scans. The GaAs grown on the layered buffer on Si (211) exhibits single-

crystalline characteristics, as illustrated in figure 5.11. The sole XRD peak of GaAs is the (422) peak, and the (211) peak is absent.



Figure 5.11: X-ray diffraction (XRD) θ -2 θ scan of GaAs film grown on InSe/ Si (211). The GaAs grown on the layered InSe buffer on Si (211) exhibits single-crystalline characteristics, where the sole peak of GaAs (422) can be seen.

The crystalline quality is superior, as confirmed by the rocking curve FWHM value for the GaAs (422) plane as low as 424 arcsec as displayed in figure 5.12. This FWHM value is only 2.61 times that of a GaAs (211) substrate used as reference in this measurement. The superior surface morphology and crystalline quality from the GaAs / InSe/ Si (211) samples could be attributed to the low threading dislocation and defect densities [104].

These results were achieved by increasing the nucleation sites of GaAs on lattice-matched InSe by using a high-Miller-index Si (211) substrate. Since the nucleation is initiated by As termination on the InSe surface, the nucleation was predominantly homogeneous. Based on the high nucleation rate and the high density of nuclei, quick coalescence took place to form a continuous thin and single-crystalline GaAs layer on the InSe /Si (211) substrates. On the other hand, the GaAs film grown on the InSe /Si (111) substrate required thicker deposition to achieve coalescence, which is confirmed by the time evolution of RHEED patterns.



Figure 5.12: Experimental results for the GaAs(422) rocking curves of GaAs/InSe/Si(211) in black and GaAs substrate reference in blue. Si(211) substrate is shown in black at (88.1 degrees).

The surface morphology of the as-grown material heterostructures was characterized by atomic force microscopy (AFM, VEECO Nanoscope IIIa Multimode SPM) in the tapping mode. The structural quality of both InSe and GaAs was determined using a high-resolution x-ray diffractometer (XRD, Bruker D8 Discover) with a monochromatic CuK α ($\lambda = 1.5405$ Å) radiation source operated at 45 kV and 40 mA. The structural characteristics of the InGaAs/GaAs multilayer structure were then investigated by cross-sectional transmission electron microscopy (TEM, Tecnai F20, operated at 200 keV).

In our InGaAs/GaAs double heterostructure (DH) grown onto the GaAs/ Si (211) structure, three InGaAs/GaAs double heterostructure (DH) quantum wells of different thicknesses of (2.5, 5, 10) nm with the same Indium composition of 10% integrated onto the GaAs / InSe/ Si (211) substrate were used. Each QW was sandwiched between Al_{0.3}Ga _{0.7}As/GaAs barriers to improve the carrier confinement in the quantum well. Finally, the growth was terminated with the deposition of a top GaAs barrier layer grown at 590 °C. The initial GaAs layer was grown at 575°C with a very low growth rate, whereas further GaAs growth steps were carried out at 590°C and a growth rate of 1 Å/s with V/III ratio of 100. The InGaAs growth temperature was 480°C, while the V/III ratio was kept high to avoid the Indium migration process [105]. A higher Arsenic equivalent pressure is necessary to suppress migration of Indium adatoms, yielding a smoother morphology [106]. Figure 5.13 shows the EDX mapping of the planar InGaAs/GaAs quantum well structure grown epitaxially on InSe/ Si(211).



Figure 5.13: EDX mapping of planar InGaAs/GaAs quantum well structure grown epitaxially on InSe/ Si(211). Three InGaAs/GaAs double heterostructure (DH) quantum wells are of different thicknesses of (2.5, 5, 10) nm with the same Indium composition of 10 %. Every quantum well was sandwiched between Al_{0.3}Ga $_{0.7}$ As/GaAs barriers to improve the carrier confinement in each quantum well.

5.5. Growth model:

Our model of the growth process of GaAs on InSe /Si (211) is shown schematically in Figure 5.14. Using quasi van der Waals epitaxy to grow high quality InSe buffer that lattice matched to GaAs can reduce the dislocations at GaAs/InSe interface. On the other hand, high quality InSe can be grown on Si via QvdWE despite the 4% lattice mismatch with silicon because the strain at the interface is believed not to propagate from the interface, which limits the lattice mismatch and thermal expansion mismatch at the interface (Figure 5.14-a). Si Si (211) substrate with has two faces one of them is 8.8 Å in the (111) origntation, making less than a nanometer steps. Thus, having more control on growth kinatics and limit the high diffusion rate

of GaAs adatoms on latered InSe (Figure 5.14-(I)B). Because layered InSe nucleates on the (111) orientation out of the c-axis plane, the growth of InSe is expected to be in narrow stripes following the (111) steps in the Si (211) substrate. InSe thickness is less than 6 nm so the steps of S (211) will be reflected on the surface of InSe (Figure 5.14-(II) B). As the InSe/ Si(211) is exposed to high As overpressure at 575 °C , as exchange of atoms on top surface between Se and As is possible since the chemical properties of Se and As are quite similar. Thus, Ga and As adatoms can be adsorbed even at high growth temperatures. Both the high V/III ratio of 100 and the steps on InSe surface can limit the high diffusion rate of Ga and As adtoms on layered InSe. Therefore, GaAs can nucleate at the edges at growth temperatures of 575 °C that is suffecint to crystalize GaAs as in figure 5.14-(III)B. As the growth proceeds at growth temperature of 575°C, GaAs coalesced into smooth thin film as in figure 5.14-(IV)B.



Figure 5.14: (a) Atomic geometry of GaAs /InSe /Si interface where the lattice mismatch is confined in the InSe /Si interface (b) Schematic illustrations of the growth of GaAs on Si (211) via using thin layered InSe buffer, (I) Si (211) substrate with 8.8 Å steps with (111) origntation, (II) Layered InSe growth on the the (111) orintation of the Si (211) substrate at 280 C (III) GaAs nucleation layer at 575 °C , where the substrate step edges are used to limit the high diffusion of GaAs adatoms on the layered InSe. and (IV) deposition of GaAs at 575°C exhibiting a smooth surface morphology after the coalescence of GaAs.

5.6. Characterization of the optical properties of QW structure:

Photoluminescence spectra from InGaAs/GaAs QWs on the as-grown heterostructures were collected using a frequency-doubled diode pumped Nd:YAG laser ($\lambda = 532$ nm). The PL was collected by a 50× objective lens, and recorded by a CCD camera.

Figure 5.15 shows the μ-PL spectrum at 300 K for three InGaAs/GaAs quantum well heterostructures grown epitaxially on layered InSe /Si (211). The three peaks represent strong direct band-to-band ground state optical transitions. The absence of any peaks at higher wavelengths is an indication of the superior optical property of the light-emitting medium. Furthermore, the high intensity of the peaks is an indication of the low density of crystal defects, as there is strong correlation between the PL intensity and the density of crystal defects, such as threading dislocations and stacking faults [107]. The total thickness of the structure is less than 800 nm. To the best of our knowledge, such a sharp room temperature PL signal with FWHM value of 44 nm emitted from a less-than-micron-thick GaAs/Si heterostructure has not been achieved before [108-111].



Figure 5.15: Photoluminescence (PL) spectrum at 300 K of planar InGaAs/GaAs quantum well structure grown epitaxially on InSe/ Si(211). Three InGaAs/GaAs double heterostructure (DH) quantum wells of different thicknesses of (2.5, 5, 10) nm integrated onto GaAs/ Si (211) structure. No peaks are observed at higher wavelengths, indicating superior optical quality material.

Due to the suppression of the exciton (electron) - phonon interaction at low temperature (77 K), sharper peaks for the photoluminescence bands and more defined bands with closely spaced energies can be seen. Furthermore, at low temperature, PL carriers are effectively frozen, so we should be able to see more clearly the lowest energy states. Figure. 5.16 shows the PL measurement at 77 K of our structure grown on Si. The narrow FWHM of the three peaks P1, P2

and P3 are about 13, 14 and 26 nm, respectively, due to the improvement of carrier confinement, values that are similar to or even better than other reported values for much thicker structures [112, 113]. The absence of defects peaks at low temperatures (77K) is a good indication of superior material quality of the grown heterostructure.



Figure 5.16: Photoluminescence (PL) spectrum at 77 K of planar InGaAs/GaAs quantum well structure grown epitaxially on InSe/ Si(211). Three InGaAs/GaAs double heterostructure (DH) quantum wells of different thicknesses of (2.5, 5, 10) nm are integrated onto GaAs/ InSe/Si (211) structure.

5.7. Summary and conclusions:

We successfully demonstrated that van der Waals layered materials can make the constraints of lattice and thermal expansion coefficient mismatches less dominant in heteroepitaxial growth. Having the right layered vdW material where it is lattice matched to GaAs, has a relatively high surface free energy and is stable at high growth temperatures allowed us to achieve promising results. In this work, we epitaxally grew GaAs on layered InSe /Si. This novel approach allowed us to achieve an XRD rocking curve FWHM of 74 arcsec, indicating the lowest defect density for GaAs grown on silicon compared to other techniques used to date. This single-crystal GaAs is capable of emitting a sharp PL signal with FWHM of 44 nm at room tempreture, making this work a remarkable step toward integrating optical interconnects on silicon chips. Futhermore, using high-Miller-index Silicon substates yielded better GaAs morphology, mainly due the higher surface free energy of InSe grown on top. Futhermore, a high quality InGaAs/GaAs double heterostucture was successfully demonstrated on layered InSe /Si (211) substrates. The novel growth scheme along with the use of optimized growth conditions helped realize high quality GaAs layers, leading to atomically sharp and nearly defect-free interfaces. The sharp and narrow room temperature PL signals have demonstrated the successful achievement of a single crystalline and high quality optical medium, making this a remaarkable step toward integrating light emitters on Silicon substates.

Chapter 6 Conclusions and Future Work

6.1. Extending the GaAs/InSe model to any arbitrary substrate: Muscovite Mica as a demonstration.

Following our successful growth scheme of using a layered-structure buffer layer to integrate GaAs on top of Silicon, it is possible in principle to grow layered materials on top of a wide variety of substrates. Based on the experimental results and optimization detailed in chapter 5, GaAs can be grown on any substrate as long as a good quality buffer of InSe can be grown on top of that substrate. This is because the van der Waals epitaxy of the layered material is less constrained by lattice constant and thermal expansion coefficient matching conditions compared with conventional heteroepitaxy for non-layered materials. Other factors that need to be taken into account while choosing the right substrate is its stability at the high temperatures required for GaAs growth. Muscovite mica, with a stoichiometry of KAl₃Si₃O₁₀(OH)₂ and lattice constants of a=5.2 Å, b=9.0 Å and c=20.1 Å, is a well-known layered substrate that has been used for vdWE growth of semiconductors [93, 114]. In addition, Muscovite mica is a flexible, transparent and cheap substrate. Thus, extending our growth concept using Muscovite mica seems to be an interesting next step to extend our growth model. Figure 6.1 (a) shows a grown structure on Muscovite mica where the same optimized growth conditions for GaAs on InSe /Si (111) were used. Figure (b) shows the sample after the growth of 50 nm of GaAs, where the sample number can be seen in the background.



Figure 6.1: (a) GaAs (111) growth structure on flexible Mica substrate using layered Indium Selenide buffer. (b) A photo of the grown GaAs /InSe/ Mica Muscovite substrate, where the sample number can be seen in the background through the structure.

It is important to note here that in spite of the large mismatch between InSe and Muscovite mica, good quality InSe can be achieved, because the two materials are layered and van der Waals bonding is dominant. InSe was grown through a van der Waals epitaxy process where both InSe and mica are layered materials and the large lattice mismatch between the two materials can be overcome. The first few layers of InSe were grown at 240 °C followed by an annealing step. Afterwards, the growth proceeded at 270 °C. The RHEED oscillations illustrated in figure 6.2 are an indication of layer-by-layer growth performed at a low growth rate. The morphology of the InSe /mica sample was characterized after the growth by AFM. The RHEED oscillations were reflected in the ultra-smooth morphology of the InSe surface, as can be seen in figure 6.2 (b).



Figure 6.2: (a) RHEED oscillations during the growth of InSe on mica substrates. (b) AFM image of InSe thin film grown on mica substrate showing an ultra-smooth surface morphology. The film has a RMS roughness value of 3 Å for an area of 1 μ m².

To examine the structural properties of the grown GaAs, the sample was characterized by XRD omega-2 theta scans. The GaAs grown using the InSe layered buffer on mica exhibits single-crystalline characteristics, as illustrated in figure 6.3. The sole XRD peak of GaAs (111) is observed at 27.3°, where the full scan is shown in the inset. The achievement of integrating single-crystal GaAs on mismatched substrates is very interesting and opens a new path for integrating III-V semiconductors onto a wide variety of semiconductors without being limited by lattice mismatch constraints.


Figure 6.3: X-ray diffraction (XRD) θ -2 θ scan of GaAs film grown on InSe/ Muscovite mica. The starred peak corresponds to GaAs (111) at 27.3°. The inset shows the full scan XRD scan from 20-80.

The optical properties of our grown GaAs film were characterized using PL measurements at room temperature. Room-temperature emission of such thin GaAs integrated directly on mismatched Muscovite mica was successfully demonstrated, indicating the presence of band-to-band radiative recombination emission. Figure 6.4 shows 300 K PL spectra of 500 nm thick GaAs grown on a InSe/ Muscovite mica substrate and an undoped GaAs (100) substrate as a reference. We found that there was a minimal redshift by 5 nm for the PL peak of our grown

GaAs compared to the reference substrate, exhibiting a slight energy-gap shrinkage for the GaAs epilayer and minimal strain, which might be attributed to the thermal expansion coefficient mismatch between GaAs and InSe. However, the wide shoulder at higher wavelengths is significant, and is due to impurity-related transitions. These impurities can to be attributed to two reasons. First is the need to optimize the growth conditions of InSe and GaAs on Muscovite mica substrates. At the growth temperature of GaAs at around 575 °C, the maximum emission wavelength based on Wien's displacement law is at 3.42 µm, which less by 30 times than the Muscovite Mica substrate thickness. Thus, we expect that a slight growth temperature change of GaAs in the case of using Mica substrate versus silicon substrate based on the difference in emissivity between the two substrates. However, in the case of very thin substrates, the emissivity calculated according to their thickness does not give the same results. Such phenomena are still observed when the film thickness is lower than, or of the same order of magnitude as the wavelength of the radiation concerned [115]. Second is the lack of steps on the Muscovite mica substrate, which makes the dislocations caused by the island nucleation more predominant.



Figure 6.4: Photoluminescence (PL) spectrum at 300 K of planar GaAs grown epitaxially on InSe/ Muscovite mica. Twenty (20) periods of InGaAs/GaAs superlattice were used. No significant shift is observed compared to the GaAs substrate reference, indicating a stress-free GaAs film.

6.2. Future work

As future work, this concept of using a layered buffer to integrate GaAs on Silicon substrates can be further extended to other III/V semiconductors by finding a suitable layered material where the following conditions are satisfied:

► Lattice matched to the III/V semiconductor.

- Having a high decomposition temperature above the III/V semiconductor growth temperature.
- ▶ Having a relatively high surface free energy to wet its surface for III/V growth.
- Having high adsorption energies of III-V adatoms on the layered materiel to ensure growth stability.
- > Friendly to UHV systems to avoid any contaminations in the MBE system.

Among layered materials at figure 5.1, Tungsten Disulfide (WS₂) is lattice matched to Gallium Nitride (GaN). In addition, Molybdenum Ditelluride (MoTe₂) is lattice matched to Indium Nitride (InN), where Nitrogen adatoms have high adsorption energies on layered materials to nucleate on WS₂ and MoTe₂.

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