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Spike Neuromorphic Carbon Nanotube Circuits

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Spike Neuromorphic Carbon Nanotube Circuits

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Mechanical Engineering

by

Kyunghyun Kim

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ABSTRACT OF THE DISSERTATION

Spike Neuromorphic Carbon Nanotube Circuits

by

Kyunghyun Kim

Doctor of Philosophy in Mechanical Engineering

University of California, Los Angeles, 2013

Professor Yong Chen, Chair

The brain has a superior computation performance in comparison with supercomputers in many aspects while the brain consumes much less power (~ 20 W) than supercomputers (~ 10^6 W). This is mainly owing to synapses, which are the fundamental elements in the brain, and their properties such as spatiotemporal signal processing, memory, and learning. Therefore, it is crucial to implement an electronic device which can emulate the elementary functions of biological synapses in order to mimic the functions of the brain. In this research, two types of

synaptic transistors (synapstors) using carbon nanotubes (CNTs) are demonstrated. First, a CNT network transistor with a poly(ethylene glycol) monomethyl ether (PEG) layer in the gate is presented. It has successfully emulated the elementary functions of biological synapses with low power consumption (250 pW/synapstor). Second, a CNT network transistor with C60 molecules is shown to mimic the essential functions of biological synapses with low power consumption (2.6 nW/synapstor). A spike neuromorphic circuit (SNC) was developed by integrating CNT synapstors. The SNC has a capability of parallel signal processing, spatiotemporal correlation, learning with low power consumption. It has both excitatory and inhibitory synapses and can generate output spikes from the accumulated post-synaptic currents. The large-scale SNC with 16,384 synapstors and 16 neurons has been designed and fabricated. The power consumption of a large-scale SNC is ~ 1.8 mW. The functions of a SNC were demonstrated. The toy drone was used as a platform to interact with the SNC. The SNC dynamically processed the sensing signals from the drone and triggered actuation of the drone in real-time. The performance of the drone was improved via the learning in SNC. The SNC has a potential to have higher signal processing speed and be more efficient in power consumption than a supercomputer when the dimension of parallel signal processing exceeds ~10^9.

The dissertation of Kyunghyun Kim is approved.

Kang Lung Wang

Laurent G. Pilon

Pei-Yu Chiou

Yong Chen, Committee Chair

University of California, Los Angeles

2013

This dissertation is dedicated to my parents

who encourage me with endless love and support.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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PUBLICATIONS AND PRESENTATIONS

JOURNALS

K. Kim, C-L Chen, Q. Truong, A.Shen, and Y. Chen, "A Carbon Nanotube Synapse with Dynamic Logic and Learning", *Advanced Materials*, vol. 25, 1693-1698 (2013) , **selected as FRONTISPIECE**.

B. Cho, **K. Kim**, C-L Chen, A.Shen, Q. Truong, and Y. Chen, "Nonvolatile analog memory transistor based on carbon nanotubes and C60 molecules", *Small*, Early View (Online Version of Record published before inclusion in an issue) (2012).

C-L Chen, **K. Kim**, Q.Truong, A Shen, and Y. Chen, "A Spiking Neuron Circuit Based on A carbon Nanotube Transistor", *Nanotechnolgy*, 1-6 (2012).

Y. S. Ahn*, **K. Kim***, H. K. Park, H. T. Hahn, and Y. Chen, "Functionalized Carbon Nanotube Networks with Field-Tunable Bandgaps", *Advanced Materials*, vol. 23, 3075-3079 (2011) **(*equally contributed authors).**

J. Ryu, **K. Kim**, H. Kim, H. Hahn, and D. Lashmore, "Intense pulsed light induced platinum-gold alloy formation on carbon nanotubes for non-enzymatic glucose detection", *Biosensors and Bioelectronics*, vol. 26, 602-607, (2010).

CONFERENCES

C.-L. Chen, **K. Kim**, Q. Truong, A. Shen, Z. Li, and Y. Chen, "Hydrogen Doped Carbon Nanotube Transistor for Biological Neuron Circuit Applications," 2012 *Materials Research Society Fall Meeting, (Carbon Nanomaterials session) poster* (2012)

K. Kim, C. L. Chen, Y. S. Ahn, and Y. Chen, "Functionalized Carbon Nanotube Transistors with In Situ Field-Tunable Bandgaps", *2011 Materials Research Society Fall Meeting, (Functional Nanowires & Nanotubes session) Oral presentation* (2011)

K. Kim, C. L. Chen, Y. S. Ahn, and Y. Chen, "Nonvolatile CNT Network Devices for Analog Memory Applications", *2011 MRS Fall Meeting, (Functional Nanowires & Nanotubes session) poster* (2011)

N. Salowitz, Z. Guo, Y.-H. Li, K. Kim, G. Lanzara, **K. Kim**, Y. Chen, and F.-K. Chang, "Development of a bio-inspired stretchable network for intelligent composites", *Proceedings of the 18th International Conference on Composite Materials*, (2011)

H.K. Lee, S.I. Chang, **K. Kim**, S.J. Kim, K.S. Yun, and E. Yoon, "A modular expandable tactile sensor using flexible polymer", *IEEE International Conference on. MEMS* (2005). doi:10.1109/MEMSYS. 2005.1454011

K.S. Yun, J. Gil, J. Kim, H.J. Kim, **K. Kim**, D. Park, J.Y. Kwak, H. Shin, K. Lee, J. Kwak, and E. Yoon, "A miniaturized low-power wireless remote environmental monitoring system using microfabricated electrochemical sensing electrodes", *Transducers* (2003). doi:10.1109/SENSOR.2003.1217153

1. Introduction

1.1 Distinctive Features in the Brain

The brain has a superior computation performance in comparison with supercomputers in terms of massive parallel signal processing, learning, long-term memory, pattern recognition, and creativity while the brain consumes much less power (~ 20 W)[1] than supercomputers (~ 10^6 W)[2]. For instance, the computational power in the brain is at least estimated as more than 40 x 10^{15} FLOPS[3] (FLOPS: FLoating-Point Operations Per Second, a measure of supercomputer performance) even though there is difficulty in estimating human computational power in the measure of supercomputers. On the other side, the fastest supercomputer in the world as of November 2012, Titan[4], has the computational power of ~ 18 x 10^{15} FLOPS while it consumes 8.2 MW, which is equivalent to supply electricity for 8000 homes. Moreover, the brain has the learning capability while supercomputers, even the fastest and most powerful computational one, cannot learn; they can only do tasks which are pre-defined by human beings in the programming languages. The method of signal processing is also different – the brain processes signals in a massively parallel way, and the supercomputer does it in the combined way of serial and parallel processing. This is mainly caused by the basic devices composing the system. Briefly, the brain can do similar or better jobs than supercomputers can do while it consumes low power 6 orders below than supercomputers' power consumption. This is mainly because of brain's structure and components, which are neurons and synapses. Especially, a synapse, which is the fundamental processing element in the brain, has functions of signal processing, memory, and learning in one

element. Therefore, the brain does not need to worry about the bandwidth between the processing unit and a memory unit like supercomputers. The comparison between the brain and the supercomputer is made in Table 1.

Brain		Supercomputer
Neuron (4 ~ 100 μm) Synapse (~ 100 nm)	**Basic Device**	Si CMOS Transistor (32 nm)
~ 10^{14} synapses	**Number of Devices**	~ 200 x10^{12} CMOS transistors[5] ~ 19K (CPU+GPU)s
1 ~ 100 Hz	**Operating frequency**	1.8 / 3.2 GHz
> 40 x10^{15} FLOPS[3]	**Computational power**	~ 20 x10^{15} FLOPS
20 W[1]	**Power**	8.2 MW[2]
Learning, massively parallel signal processing	**Remarks**	Programmed, fast numerical calculation, serial/parallel processing

Table 1. Comparison between the Brain and a supercomputer.

1.2 Structure of the Brain – Neurons and Synapses

In order to understand why the brain has superior computational power than supercomputers while it consumes much less power than supercomputers, the structure and operation of the brain should be addressed. In this section, the structure of the brain will be explained briefly. In the human's brain, there are roughly 10^{11} neurons[6] and each neuron has in average more than 10^3 connections with other neurons[7]. A typical neuron is a basic cell of

composing the brain and can receive from other neurons or send signals to other neurons. Neurons in the brain signal to each other using spikes, which are short duration potential pulses[8]. Typical neurons have three functional parts: the soma (cell body), dendrites, and axon. The soma or a cell body of a neuron can generate output spikes when the potential is above the threshold value. The dendrites are branches extended from the soma. In the dendrites and the soma, a neuron can receive signals from other neurons. The axon is another branch from the soma which delivers the signal to other neurons. Between neurons, there are signaling connections which are called synapses. Biological synapses are the specialized connections between neurons for transferring signals to neurons as illustrated in Figure 1. They can process and transmit spike signals in an electrochemical way and the estimated number of synapses in the brain is about 10^{14}. With this abundance of synapses, the brain can process numerous signals, associate complicated information, and achieve complex intelligence with a help of elementary functions of synapses.

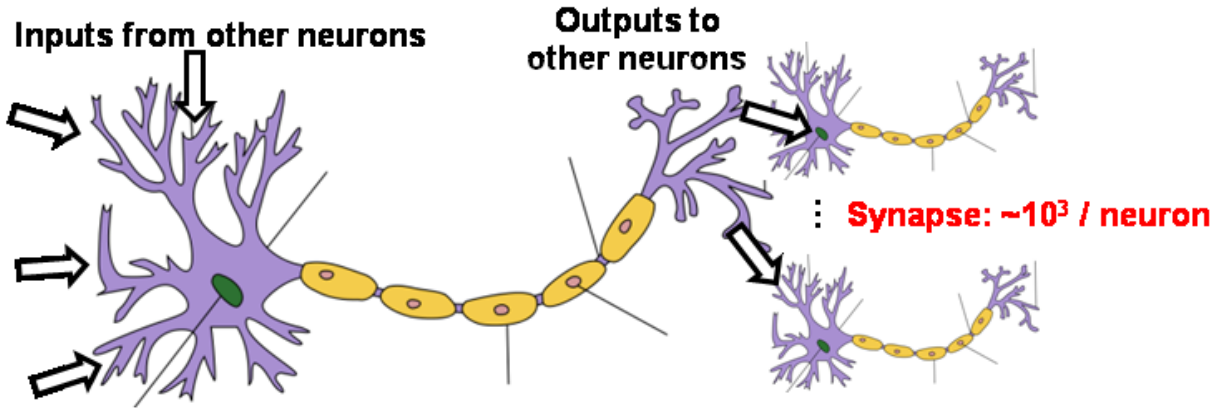


Figure 1. Structure of a typical neuron.

1.3 Operations of Neurons and Synapses

The brain's amazing power is not utilized by not only the numbers of neurons and synapses but also the functions of neurons and synapses. Therefore, it is crucial to understand the elementary functions of neurons and synapses about how they process signals and combine multiple signals into useful information. As described in the previous section, neurons and synapses handle signals in spike format and the amplitude and the duration of spikes are almost constant because both parameters are determined by the ion concentration in the brain. Whenever the spike arrives at the synapse from an input neuron (so-called a pre-synaptic neuron) to output neuron (so-called a post-synaptic neuron), the synapse generates a temporal dynamic response at the output neuron, which known as a post-synaptic potential or current[8]. The post-synaptic current can last for milliseconds to minutes depending on synapses and cause changes of the potential in the output neuron. There are two types of synapses – excitatory and inhibitory synapses. The excitatory synapse generates the positive change in the potential at the output neuron when it receives the input spike. On the other hand, the inhibitory synapse generates the negative change in the potential at the output neuron when it receives the input spike[9] as illustrated in Figure 2. The amplitude of post-synaptic current is typically referred as a synaptic weight or synaptic efficacy because spikes in the brain have almost constant amplitude and duration as described earlier. In other words, the synaptic weight means that how well the synapse can carry the spike signals from one neuron to other neuron. Shortly, there are two types of synapses which have both positive and negative synaptic weights.

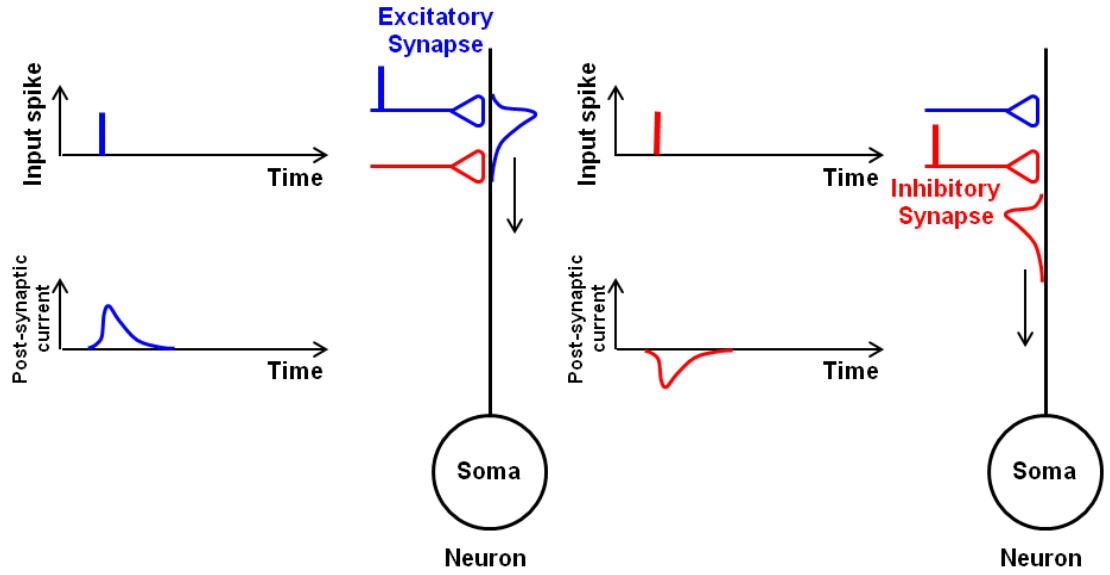


Figure 2. Excitatory and inhibitory synapses and their post-synaptic responses.

Post-synaptic currents generated from all synapses go to the soma and then will be accumulated. If the accumulated post-synaptic current is above the threshold value, then the soma generates output spikes corresponding to its level as illustrated in Figure 3. A neuron can establish spatiotemporal correlation between a set of input spikes and a set of output spikes using the accumulated post-synaptic currents from all synapses in a neuron. For instance, as shown in Figure 4, if there are a set of input spikes applied to each individual synapse at different timings, then, each input spike triggers excitatory (blue) or inhibitory (red) post-synaptic currents. All post-synaptic currents, then, are delivered to the soma, a cell body of a neuron, and accumulated. Output spikes are generated correspondingly based on the level of the accumulated post-synaptic current. There can be numerous possible forms of the accumulated post-synaptic current depending on the amplitude of post-synaptic currents of triggered synapses, timings of input

spikes, and types of synapses (Figure 4). Accompanying with described properties of synapses, there is another crucial function of synapses, which is massive parallel processing. There is no operation clock in neurons and synapses as typical CMOS IC circuit. Therefore, all spikes come and go asynchronously and trigger the post-synaptic current and output spikes. For instance, a typical neuron can process in average about 10^3 spike signals if all synapses get the input spikes almost simultaneously. Considering the number of synapses per neuron, a single neuron can generate abundant forms of the accumulated post-synaptic current and establish almost any types of correlation between input spikes and output spikes in a spatiotemporal way.

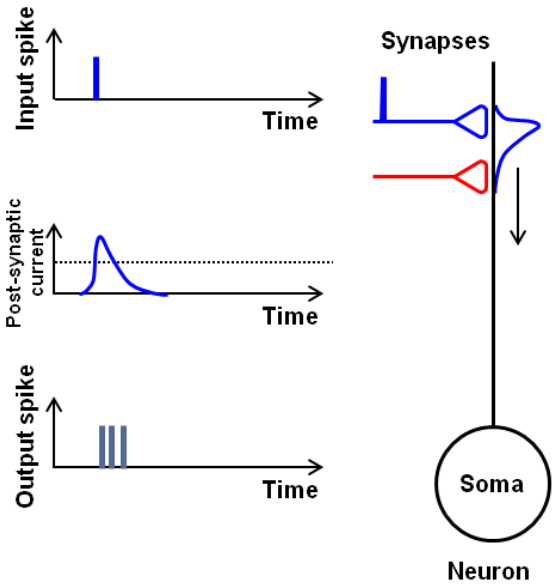


Figure 3. Generation of output spike from post-synaptic current.

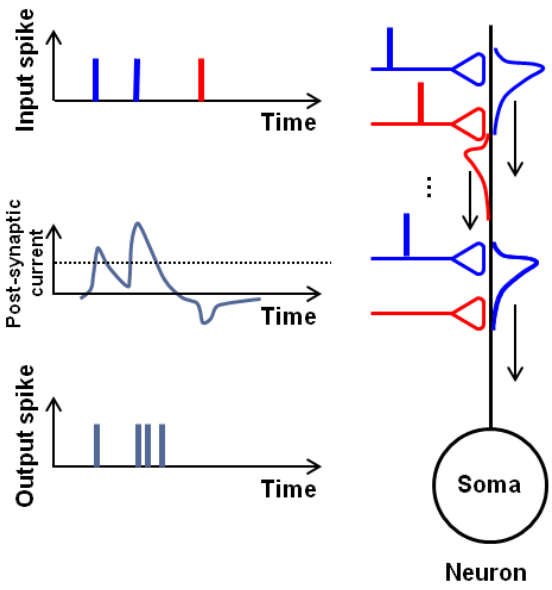


Figure 4. Spatiotemporal signal processing in a neuron.

Other critical function of synapses is synaptic plasticity[10]. The synaptic plasticity is the capability of synapses to modify the amplitude of post-synaptic current (or the synaptic weight) quantitatively and reversibly. The change may be stored for short term or long term (more than minutes to hours). The synaptic plasticity is believed as a basis for learning and memory in the brain. This tunable post-synaptic current amplitude makes the accumulated post-synaptic current more plentiful. The synaptic weight is sensitive to the relative timing of spikes in both connected neurons[11]. In other word, the synaptic weight can be either increased or decreased based on the timing difference between pre-synaptic spike and post-synaptic spike. Pre-synaptic spikes are the spikes come toward the synapse from pre-synaptic neurons like input spikes. Post-synaptic spikes are the spikes from post-synaptic neuron, which are back-propagating spikes. The STDP function is described in Figure 5. If pre-synaptic spike comes before the post-synaptic spike, then

the synaptic weight is increased and vice versa. Usually, the STDP function causes "Long-Term Potentiation" (LTP) and "Long-Term Depression" (LTD) of the synapse, which is believed to form a long term memory in our brain[12]. LTP is the strengthening of the synapse and LTD is the weakening of the synapse. Both phenomena can last from hours to days.

In short, biological synapses can 1) process and correlate spike signals in a spatiotemporally way, 2) facilitate memory and learning capability in the brain with help of synaptic plasticity while 3) consuming low power of 10^{-13} W when the spike rate is 100 Hz.

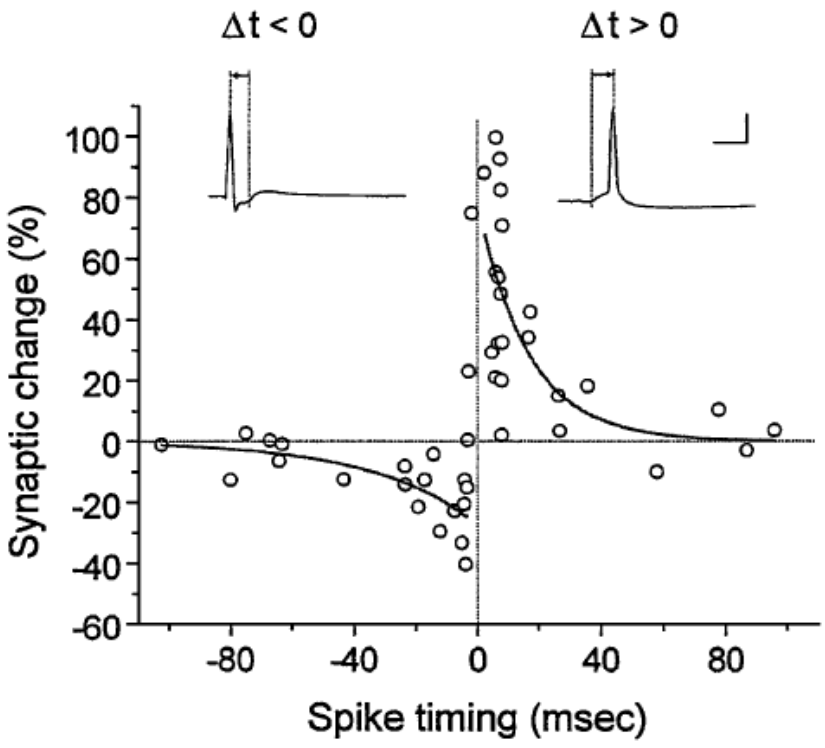


Figure 5. Spike-timing-dependent plasticity (STDP), the top pulses represent post-spikes and pre-spike is coming at t=0[11].

1.4 Cortical Simulation in a Supercomputer

As the elementary functions of synapses are revealed in micro-scale, there was a study to simulate the brain's activity in a supercomputer to widen the understanding of large scale neural networks, which is the brain. IBM supercomputer, Blue Gene, with 147,456 CPUs and 144 TB of main memory was used to simulate the neural network at the complexity level similar to cat's brain[13], which has about 1.6×10^9 neurons and 0.9×10^{13} synapses. The simulation result was 643 times slower than the cortical activity in real time while it consumed 1.4 MW power. This result vividly shows that the conventional Complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) technology is not competitive for large dimension parallel signal processing in comparison with the brain. Therefore, in order to capture the advantages of brain into a circuit, it is essential to have a novel device which can emulate the synaptic properties and build a circuit based on it.

1.5 Neuromorphic Circuit and Synaptic Devices

In the recent decades, the standard Complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) technology based on metal oxide semiconductor field effect transistor (MOSFET) has been improved drastically. To attain high performance CMOS transistors, the device feature size has kept shrinking. The famous description represents this trend is Moore's law, which is the number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately, every two years[14]. Recently, the state-of-the-art transistor has 22nm

gate length and that device is successfully integrated in commercialized products[15]. In spite of recent success in CMOS IC technology, the practical and physical limits of the transistors' scaling down will be eventually faced because of lithography limits, gate oxide leakage and so on[1]. In addition to limits of scaling down, current CMOS integrated circuit cannot do better tasks in terms of pattern recognition and intelligence such as learning. The conventional electronic circuit has difficulties when perceiving outside worlds from sensory signals when there is huge statistical variation, while the brain can easily perceive and process sensory signals. Moreover, the power consumption is the critical barrier to overcome. For instance, one of the latest central processing unit (CPU) consumes 77 W[16] and other family CPUs consume similar power[17], which is larger than the power consumption of the brain. The brain has benefits even over supercomputers as described in previous sections. If one can utilize such properties into a circuit, then, the electronic circuit can be potentially more energy efficient and more computationally powerful. To overcome existing problems of current CMOS IC technology and imbed the advantages of the brain into a circuit, new concept of emulating neural and biological architectures of the brain in the circuit is introduced which is known as a *neuromorphic circuit*. The concept of neuromorphic circuit was firstly pioneered by Carver Mead in 1990[18]. Mead have predicted the limitation of Moore's law and proposed a new direction of building electronic circuits based on brain. Most of neuromorphic researches try to 1) emulate the elementary synaptic functions in a circuit level or a device level such as spatiotemporal signal processing and synaptic plasticity, and 2) build an electronic circuit which can process signals in parallel with low power consumption. Since the first report about silicon retina based on floating gate

transistors by Mead[19], numerous researches about neuromorphic engineering have been following[20,21] to capture the brain's advantages into a circuit.

1.6 Prior Art for Neuromorphic Circuit and Synaptic Devices

As described in previous sections, emulating a synapse function is an essential process toward the implement of the neuromorphic circuit. There were three types of approaches. First one was to design analog CMOS Very-Large-Scale Integration (VLSI) circuit which can emulate the function of synapse while consuming substantial power and numbers of transistors as shown in Figure 6[22] and Figure 7[23]. As shown in Figures 6, the synaptic functions were implemented with several transistors. The synapse circuit comprises two modules. One is the receptor which sets the synapse's delay constant with low pass filter. The other is the cleft which determines its rise time with a pulse extender. The pulse extender is the interface circuit which converts from fast digital signal of 10ns duration to slow analog neural signal of several milliseconds duration. There is also a soma circuit to mimic the neuron cell body. In order to do that, the capacitor is used to set the time constant of neuron circuit. In one neuron chip, there is a 16 by 16 array of neurons with 750,000 transistors in $10mm^2$. Though each neuron circuit size is 28μm by 36μm, the chip size is fairly large considering the number of neurons. It's mainly because there are many sub-circuits to emulate neurons such as the soma, the synapse, the STDP circuit and so on. The STDP circuit comprises three sub-circuits – decay unit, integrator and SRAM. In their

neuron chip, each neuron has 21 STDP circuits. As shown in figure 6, one neuron with 21 synapses takes 190μm by 120μm area. Moreover, since SRAM is used to construct the STDP function, this neuron chip's memory is volatile. Similarly, there is substantial power consumption by numbers of transistors in second analog CMOS VLSI circuit.

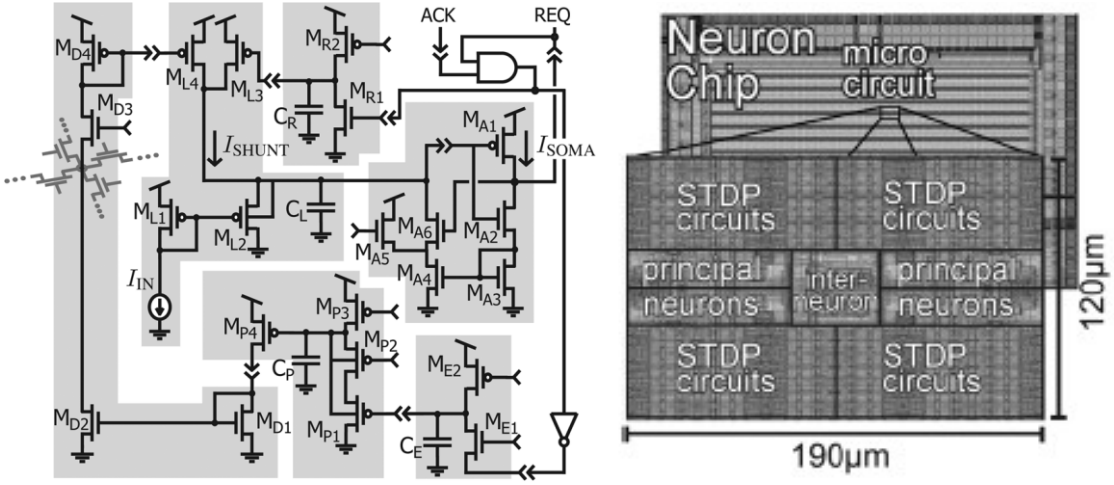


Figure 6. Analog VLSI neuromorphic circuit **(left)** circuit schematic for emulating the synaptic functions **(right)** whole chip image[22].

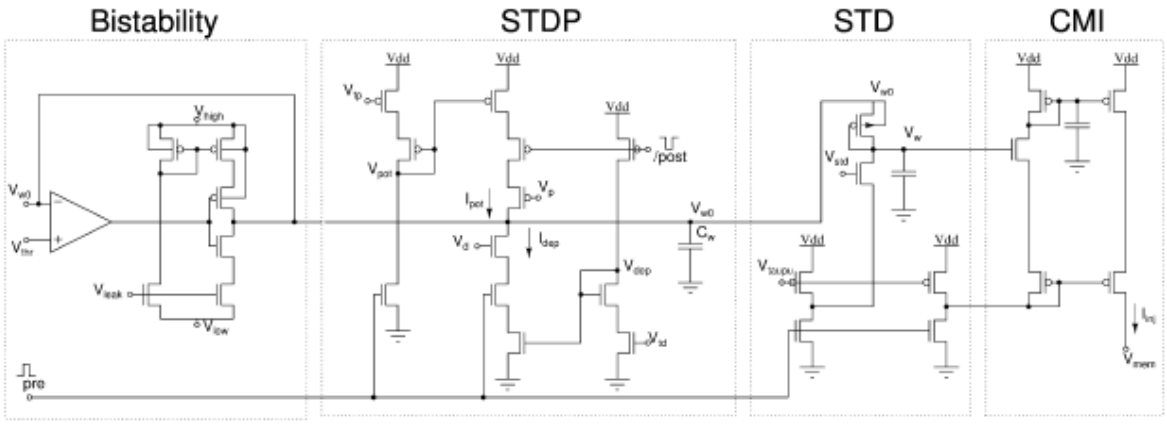


Figure 7. Analog VLSI excitatory synapse circuit[23].

The second approach was using the floating gate transistor[24,25]. By tunneling electrons toward the floating gate, the conductance of the device can be adjusted by the amount of trapped electrons in the floating gate (Figure 7)[24]. The advantages in this approach are non-volatile memory and its configurability by the amount of electrons in the floating gate. By controlling the amount of the charge, the conductance of the device can be configured in analog values so that it can emulate the synaptic plasticity in one single device. But it needs high voltage of more than 15 voltages to make tunneling happen when adjust or configure its conductance since it uses the tunneling. Also, it needs to have control 4 terminals as illustrated in Figure 7 and especially, manage all terminals to have complicated voltage functions to achieve the synaptic plasticity.

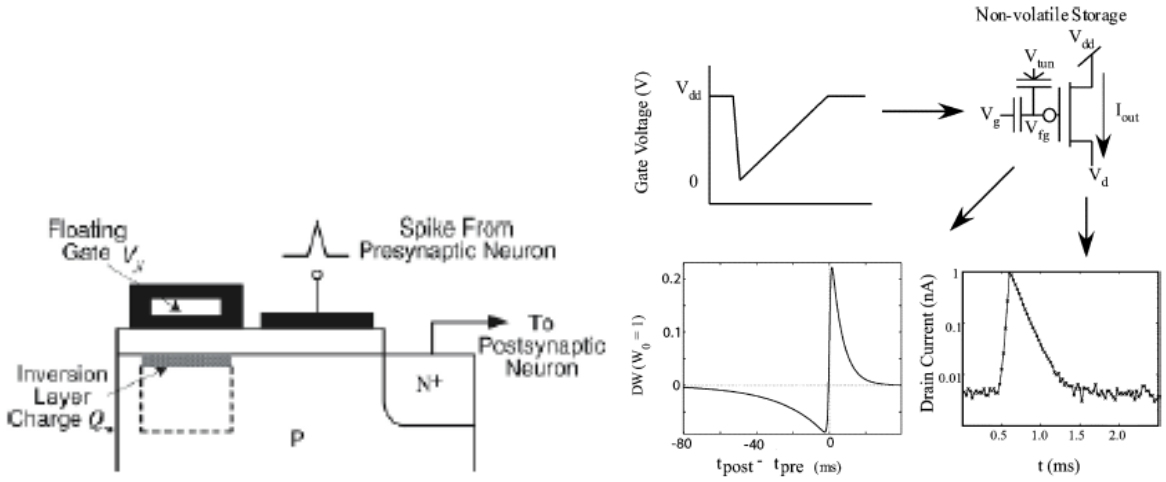


Figure 8. Floating-gate synaptic devices **(left)** using charge transfer from the floating gate[25] **(right)** using charge in the floating gate[24].

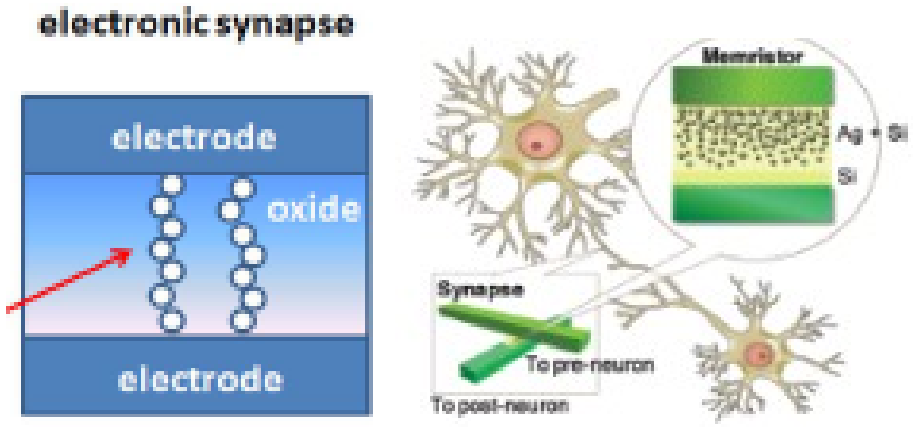


Figure 9. Resistive **(left)**[26] / memristive **(right)**[27] synaptic devices.

The last approach is using a resistive or memristor type devices to emulate the synaptic properties[26,27]. The device structures of both cases are shown in Figure 8. Both devices utilize the change of resistance for emulating the synaptic plasticity. The resistance change was made through creation or destruction of nano-scale filaments between electrodes in resistive devices, while the memristor-based device utilizes the formation of conducting filaments by Ag ions inside the device. Those devices mimic the synaptic plasticity by the change in the resistance between two electrodes. Since single device can emulate some of synaptic properties, it is easier to integrate more synaptic devices in an integrated chip. However, there is no post-synaptic response which can last for certain time period since they utilize the resistance for their synaptic weights. As a result, the short duration response, which can only last for nanoseconds, can be generated when there is an input spike and it will be difficult to have temporal correlation in spikes. In addition, the power consumption is not low. Their estimated power consumption is

about 0.3 mW/device and 1.6 μW/device, respectively. This is because of using the resistance of devices as the synaptic weights.

All previous approaches have advantages and disadvantages. The comparison is made in Table 2 for all previous approaches introduced in this section. As described earlier, it is essential to have the elementary functions of synapses in a single device such as spatiotemporal signal processing, learning, and memory with low power consumption. However, analog CMOS circuit design can successfully emulate synaptic functions but has drawbacks of power consumption and scalability. The floating gate synaptic devices have synaptic plasticity but no spatiotemporal correlation due to lack of post-synaptic current with substantial power consumption. The resistive/memristive synaptic devices are mimicking the synaptic plasticity but deficient in spatiotemporal correlation.

	Spatiotemporal correlation (post-synaptic response)	Synaptic plasticity	Power consumption per device/circuit	Scalabiilty
Analog CMOS[22]	Yes	Yes	1 μW	No
Analog CMOS[23]	Yes	Yes	1.5 μW	No
Floating gate[24]	No	Yes	4 nW	Yes
Floating gate[25]	No	Yes	2.5 μW	Yes
Resistive[26]	No	Yes	0.3 mW	Yes
Memristive[27]	No	Yes	1.6 μW	Yes

Table 2. Comparison of prior art.

1.7 Research Goal

The goal of this research is 1) to develop a novel device which can emulate the elementary synaptic properties in a single device with low power consumption (nW/device), 2) to build a spike neuromorphic circuit which is capable of parallel signal processing and learning, and 3) to demonstrate the dynamic interaction with the environment and leaning capability in real time. First goal is essential to emulate the neural network and achieve the advantages of the brain into a circuit. The synaptic devices should be able to process spike signals and trigger the post-synaptic response, a dynamic temporal response, because the spatiotemporal correlation can be obtained from it. Also, memory and learning capability in the circuit can be achieved from synaptic devices' intrinsic property of the synaptic plasticity as biological neural network do. The low power consumption is important because synaptic devices are the elementary component in a spike neuromorphic circuit. To build a spike neuromorphic circuit, it is critical to build a soma circuit in addition to synaptic devices, which can accumulate post-synaptic currents from all synaptic devices and generate output spikes correspondingly to the accumulated post-synaptic current. The configuration of a spike neuromorphic circuit will be introduced. Finally, a spike neuromorphic circuit will be used to demonstrate the capability of dynamic interaction and learning in real time. A toy drone was selected as a platform for the demonstration.

2. Synaptic Transistors (Synapstor)

2.1 Essential Properties of Synaptic Devices

In order to build a neuromorphic circuit having all the fundamental features of the brain, it is critical to have a single device with elementary synaptic properties with low power consumption as explained in the previous chapter. It is required to select essential properties for synaptic devices to have because there are many features of biological synapses and it is impossible to emulate all known properties in a single device. Therefore, in this section, the essential properties in synaptic devices will be introduced and discussed.

First, it is better to process signals in spike format. When the information is decoded into a spike format, there are advantages in terms of power consumption and use of time domain, which is basically unlimited space. Second, the post-synaptic response is required either in current or voltage. The post-synaptic response is the key response to correlate signals in space and time – spatiotemporally. The lasting time for the post-synaptic response can range from milliseconds to seconds. There will be trade-off between energy consumption and time span for the correlation. Therefore, longer or shorter lasting time of the post-synaptic response is not always good. It will depend on the applications and their operating frequency range. Third, the synaptic plasticity is necessary. The synaptic plasticity has two aspects – one is the adjustability of the amplitude in the post-synaptic response, and other is the non-volatility of the change. Simply, the synaptic weights should be able to be modified and the modification should last for long enough time to memorize the learning. Fourth, power consumption per device should be

low. To be competitive with the brain or the computer, many synaptic devices should be integrated into a single neuromorphic circuit. The power consumption or power density will be one of the key issues in such case. In this research, the target power consumption level is nW/synaptic device. Fifth, the device should have the scalability considering the large-scale integration in a neuromorphic circuit. Therefore, it is preferred to use nano-scale materials in device fabrication. Last, the compatibility with CMOS circuit is required. Eventually, the implemented neuromorphic circuit will interact with the environment in real time. It will be easier to use conventional CMOS circuits as an interface component for the environment interaction. Therefore, the compatibility can be one of essential properties for synaptic devices. Here is the list of introduced requirements of properties for synaptic devices.

- Handling spike signals
- Post-synaptic response for spatiotemporal correlation
- The synaptic plasticity
- Low power consumption: ~ nW/device
- Scalability – nano-scale material
- Compatibility with CMOS circuit

2.2 Synaptic Transistor – Synapstor

Even though synapses have two terminals (pre-synaptic neuron as an input terminal and post-synaptic neuron as an output terminal), it is not necessary to have two terminals in synaptic

devices. As seen in resistive/memritive synaptic devices, two terminal synaptic devices may suffer from power consumption and short lasting post-synaptic response due to their nature or operation. Therefore, it can be a good candidate to use three terminal devices similar with CMOS transistors. The advantages of three terminal synaptic devices are to easily generate the long-lasting post-synaptic response and conveniently design devices considering low power consumption. For example, when the input spike in a fixed format (pulse amplitude and pulse duration) is applied on the gate, the long-lasting post-synaptic current can be realized. Moreover, if the gate current is small during the input spike, the power consumption can be basically controlled by the conductance through the channel. Therefore, in this research, synaptic devices in a transistor structure are explored and studied. Synaptic transistors will be called *Synapstors* in this thesis.

2.3 Carbon Nanotube (CNT) / Poly(ethylene glycol) monoethyl ether (PEG) synapstor

2.3.1 Structure and Fabrication

As described in section 2.1, it is desirable to use nano-scale material in synapstors. In this research, carbon nanotubes (CNTs) are used as a main material for constructing a channel in synapstors. However, CNT-based devices are usually suffered by CNTs' dispersed bandgaps[28] which are made during the synthesis process. Various studies have been taken to control the

CNT bandgaps by passing high currents[29], mechanical strain[30], changing synthetic conditions[31], post-synthesis differentiation[32], and chemical functionalization[33]. Nevertheless, it is impossible to completely eliminate the bandgap variations due to their intrinsic structural disparity. In CNT/PEG synapstors, a network of randomly aligned single-walled CNTs is used as a channel to avoid such difficulty. When a randomly aligned CNT network is used in synapstors, it is easy to pattern, immune to bandgap variation of CNTs, and simple to form an electrical path[34].

First of all, the structure of a CNT/PEG synapstor is shown schematically in Figure 10a[35]. A 10 μm wide single-walled CNT network was patterned as a synapstor channel on a silicon substrate with a 100 nm thick SiO_2 layer. The CNTs in the network are self-assembled CNTs with dispersed metallic and semiconducting characteristics, which have lengths ranging between 0.2 and 2.0 μm and diameters ranging between 0.8 and 1.2 nm. Ti/Au (10 nm / 50 nm) source and drain electrodes were then interconnected with the CNT network channels. A 5 nm thick Al_2O_3 insulating layer covered the CNT channel, and a ~1 μm wide window was made in the Al_2O_3 layer to expose the central section of the CNT channel. A poly(ethylene glycol) monomethyl ether (PEG) layer with 90 nm thickness was then deposited and cross-linked by e-beam lithography, and contacted the central section of the CNT network through the Al_2O_3 window. An Ti/Al (15 nm / 85 nm) top gate electrode was fabricated on the top of the PEG layer. Finally, an electrochemical cell is integrated into a synapstor with the PEG polymer layer as an electrolyte, and the Al/Ti and CNTs as electrodes (Figure 10b).

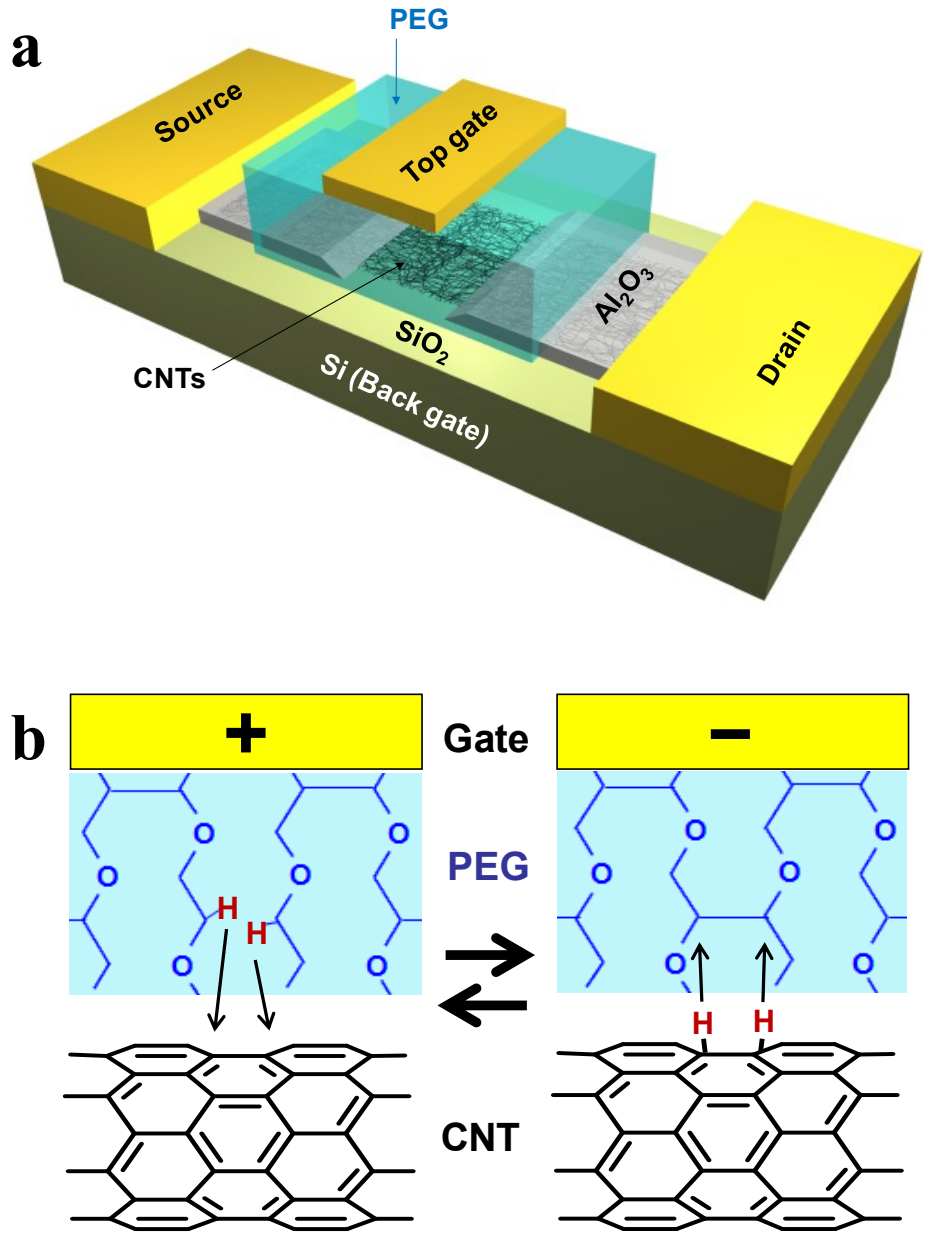


Figure 10. CNT/PEG synapstor[35] **a.** the structure of a CNT/PEG synapstor **b.** the structure of an electrochemical cell integrated into a CNT/PEG synapstor.

2.3.2 Operation Mechanism

In the PEG polymer layer, mobile hydrogen ions, or protons, can be produced and drifted with a high mobility under the external electrical field through the layer[36,37]. Such mobile hydrogen ions can react with CNTs at the channel and change the overall bandgap of CNTs. When hydrogen ions react with CNTs, the sp^2 bonding between carbon atoms at CNTs is broken and converted to the sp^3 bonding between carbon atom and hydrogen[38]; as a result, the bandgap of CNTs can be modified, which is called *hydrogenation* of CNTs. The change of bandgap can be reversibly increasing or decreasing depending on the degree of hydrogenation at CNTs[39]. When CNTs are hydrogenated, the conductance of CNTs is decreased because of increasing bandgap[40]. Contrastingly, the conductance can be increased when CNTs are dehydrogenated. Therefore, in a CNT/PEG synapstor, when a positive voltage is applied on the gate electrode with respect to CNTs, mobile hydrogen ions drift from their original positions in a PEG polymer toward CNTs, thus resulting in hydrogenation of CNTs and dehydrogenation of a PEG polymer. Oppositely, when a negative gate voltage is applied, CNTs are dehydrogenated and a PEG polymer is hydrogenated.

The source-drain current (I_{DS}) can be electrochemically configured by applying gate voltages (V_G). Most of CNT devices show p-type behavior when undoped CNTs are exposed to the environment and it is believed because of atmospheric O_2[41]. Similarly, in the control device in which the PEG polymer layer was replaced by an epoxy layer, typical p-type behavior was observed (Figure 11a). In a CNT/PEG synapstor, some of CNTs at the channel was hydrogenated during fabrication process, thus resulting in the change of the bandgap locally and showing

ambipolar behavior as shown in Figure 11b. A typical I_{DS} curve versus V_G which was measured at the room temperature with a source-drain voltage V_{DS} = 0.5 V is plotted in Figure 11b. When V_G swept from –5 V to 5 V, an "M"-shaped I_{DS}-V_G curve with hysteresis was observed. First, I_{DS} reached the minimum value of around 57 pA near V_G = 0 V, which represents the characteristics of an ambipolar CNT transistor. Therefore, both electron and hole transports can dominate I_{DS} with semiconducting CNTs under the positive or negative gate voltages. When V_G swept from 3 V to 5 V, I_{DS} was eminently reduced with negative transconductance, which indicates that CNTs were hydrogenated at V_G > 3 V. When V_G swept back from 5 V to –5 V, a "U"-shaped I_{DS}-V_G curve was observed. When V_G swept from 3.4 V to –1.8 V, I_{DS} was suppressed below 100 pA because I_{DS} in this range was the current through the hydrogenated CNTs. When V_G swept from –1.8 V to –5 V, I_{DS} was gradually increased and recovered to high values, which indicates that CNTs were gradually dehydrogenated. The redox currents through the electrochemical cell (or the leakage currents through the synapstor gate) were < 0.1 nA, and always significantly less than I_{DS} which also indicates that the power consumption during the device configuration is < 1 nW. From this current, the total amount of hydrogen ions reacted with CNTs can be estimated. The area of exposed CNTs to a PEG polymer layer is 10 μm^2 and the gate current is ~ 0.1 nA, thus resulting that the electric charge moving per area is 0.1 x 10^{-9} C/(s·μm^2). Therefore, the estimated number of protons per area and time is roughly 6.25 x 10^8 /(s·μm^2)

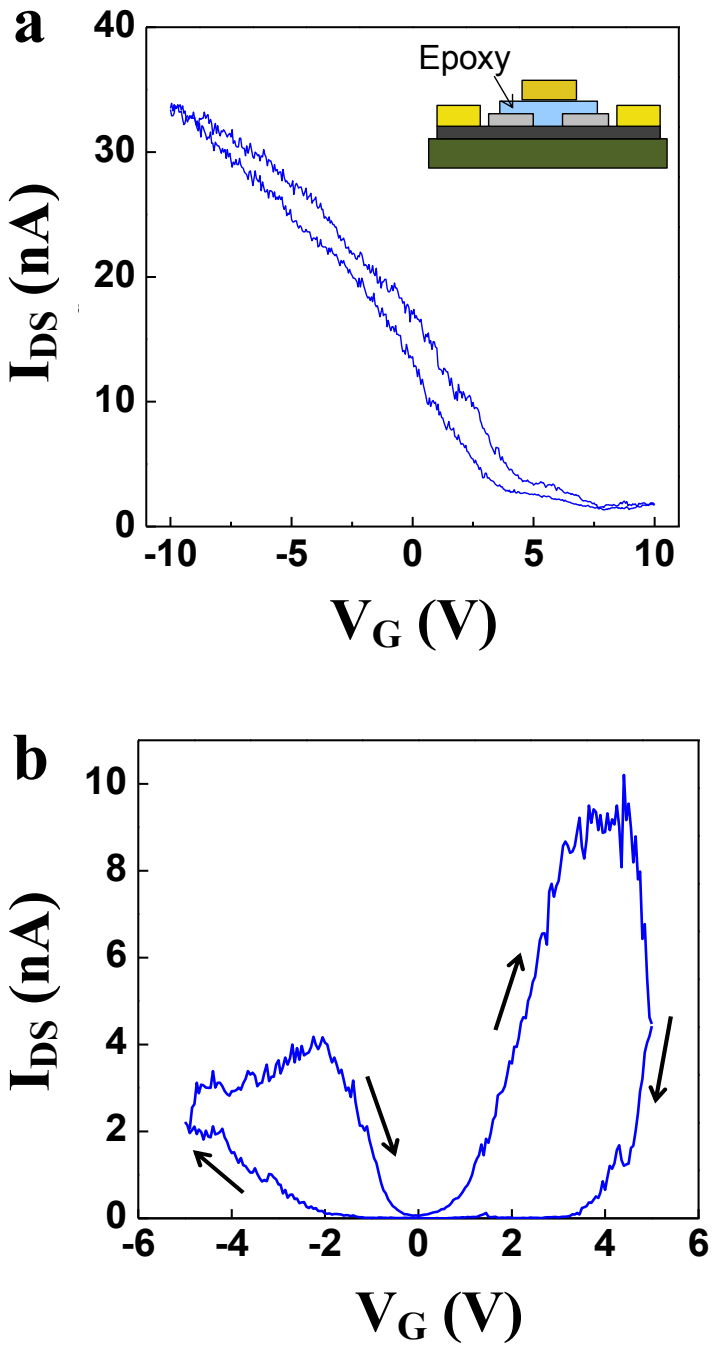


Figure 11. a. I_{DS} vs. V_G curve in a control device **b.** I_{DS} vs. V_G curve in a CNT/PEG synapstor[35].

In order to confirm the hydrogenation and dehydrogenation of CNTs at the channel of a CNT/PEG synapstor, Raman spectra from CNTs at the network in a CNT/PEG synapstor was performed. Typically, there are two peaks can be measured when Raman spectra is performed on carbon-based nano-scale materials such as CNT and Graphene. First peak is called a graphitic (G-) peak around 1590 cm^{-1} and second peak is so-called a disorder (D-) peak around 1340 cm^{-1}. G-peak corresponds to the tangential vibration of carbon atoms and represents the presence of the graphitic layers. Simply, it is related to the sp^2 bonding between carbon atoms in CNTs. D-peak is closely related to any kinds of defects in CNTs[42]. Moreover, it has been proved that the ratio between the D-peak and the G-peak ($R_{D/G}$) is increasing as CNTs are hydrogenated and vice versa[40,43,44]. It means that the CNT hydrogenation, the formation of C–H bonds on the CNT sidewalls, convert the C–C sp^2 orbital in the original CNTs to the C sp^3 orbital in the hydrogenated CNTs, which induces the relative increase in D-peak intensities in Raman spectra. To verify the hydrogenation of CNTs by Raman spectra, three different types of devices were experimented. First, pure pristine CNTs were examined by Raman spectroscopy. The pristine CNTs were deposited on a SiO_2/Si substrate and the Raman spectrum experiment was performed on it. The ratio $R_{D/G}$ was measured as 0.17. Second, the control device which has an epoxy layer instead of a PEG layer was examined by Raman spectroscopy. The measured ratio of $R_{D/G}$ was 0.20, which is slightly larger than the pristine CNTs. Finally, a CNT/PEG synapstor was examined by Raman spectroscopy. For a CNT/PEG synapstor, three states were measured – as-fabricated, hydrogenated, and dehydrogenated. An “as-fabricated” synapstor means a CNT/PEG synapstor was examined by Raman spectroscopy right after finish of fabrication without

applying any voltage pulses on the gate. A “hydrogenated” synapstor is the CNT/PEG synapstor after it is hydrogenated by applying gate pulses with the amplitude of 7 V and the duration of 1 ms. A “dehydrogenated” synapstor is similarly the CNT/PEG synapstor after it is dehydrogenated by applying gate pulses with the amplitude of −7 V and the duration of 1 ms. The ratio $R_{D/G}$ was measured 0.36 for the as-fabricated CNT/PEG synapstor. The ratio of the hydrogenated CNT/PEG synapstor was increased to 0.43, and then, decreased to 0.31 for the dehydrogenated CNT/PEG synapstor. The Raman spectroscopy results for all types of devices are shown in Figure 12. The increment in the D-peak intensity is caused by the accumulated degree of hydrogenation of CNTs, thus indicating in the formation of the C–H bonds and sp3 orbital in CNTs and consequently the enlarged overall bandgaps in a CNT/PEG synapstor. Oppositely, the decrease in the D-peak intensity is caused by the accumulated degree of dehydrogenation of CNTs, thus indicating in the rupture of the C–H bonds in CNTs and consequently the decreased overall bandgaps in a CNT/PEG synapstor.

In short, an electrochemical cell with a hydrogen-containing PEG electrolyte is integrated in the gate of a CNT/PEG synapstor to modify the CNT structures and bandgaps. CNTs in the channel can be functionalized by electrochemical hydrogenation driven by gate voltages.

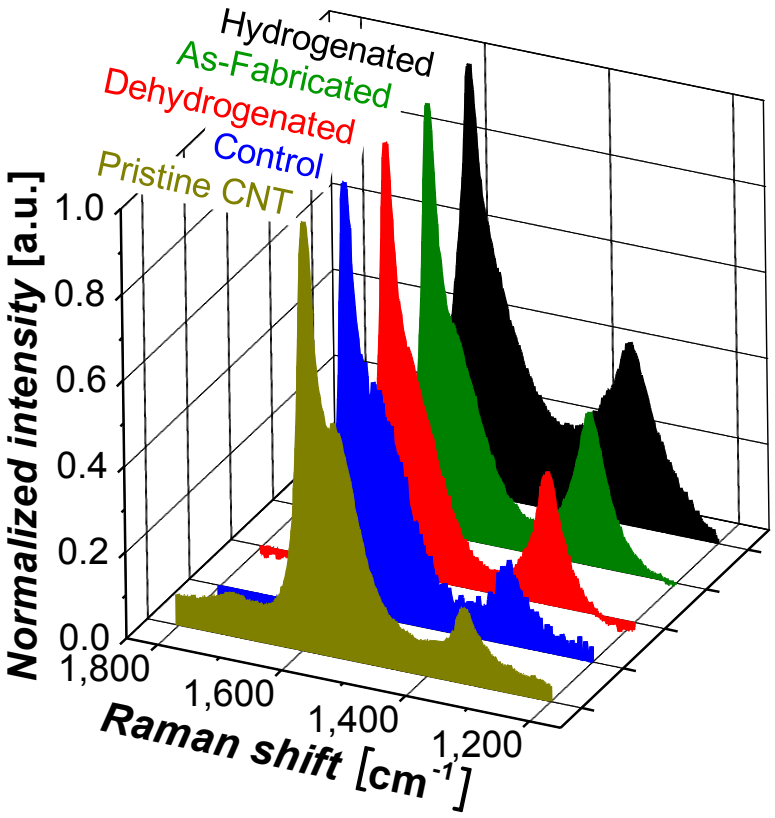


Figure 12. Raman spectroscopy of CNT networks[35]. **Pristine CNT** − Raman spectra of pristine CNTs on a SiO2/Si substrate, **Control** − CNTs covered by an epoxy layer in a control device, **As-fabricated** − CNTs covered by a PEG polymer layer in an as-fabricated device, **Dehydrogenated** − CNTs dehydrogenated by input spikes, **Hydrogenated** − CNTs hydrogenated by post-synaptic spikes. All the spectra are normalized to their graphitic (G-) peaks around 1590 cm^{-1}.

2.4 Synaptic Properties of CNT/PEG synapstors

As discussed in Chapter 1, it is crucial to emulate the elementary functions of biological synapses. In this section, the synaptic properties in a CNT/PEG synapstor will be introduced and explained[45]. To perform experiments on CNT/PEG synapstors under the condition similar to a biological synapse, a customized electronic circuit was built to achieve high electric resolution and extremely low noise and its schematic is shown in Figure 13. The drain electrodes of CNT/PEG synapstors are connected to the current-to-voltage converter to acquire the post-synaptic current (the source-drain current, I_{DS}) whereas the source electrode of a CNT synapse can be switched between the constant V_{DS} voltage (0.5 V) and post-synaptic spikes. A commercial field programmable gate array (FPGA) circuit (National Instrument sbRIO-9632) generates spikes with spatiotemporal correlations at the fixed amplitude of 3.3 V. An amplitude converter circuit transfers the amplitudes of the pre- and post-synaptic spikes with amplitudes ranging between −6 V to 6 V. The post-synaptic current was measured by an analog-to-digital converter circuit, National Instruments PCI-4472.

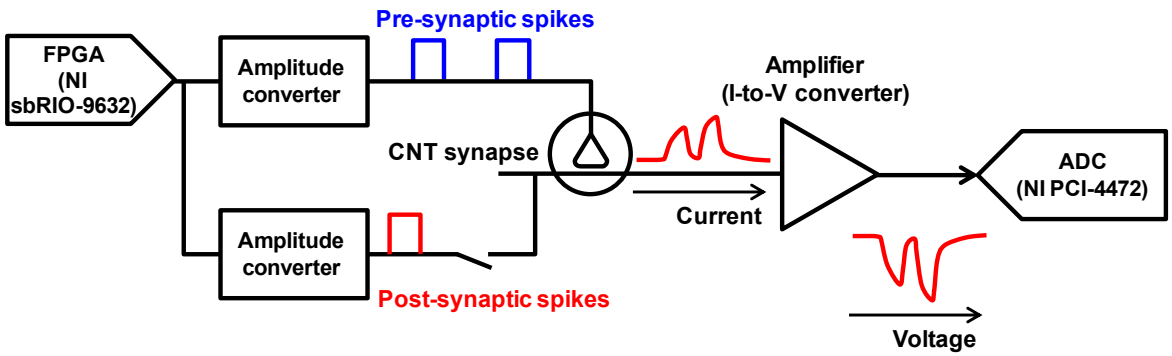


Figure 13. A schematic showing a customized testing circuit for CNT/PEG synapstors[45].

In this section, it will be shown that CNT/PEG synapstors can emulate the spatiotemporal signal processing, memory, and learning functions of biological synapses in a single device. More precisely, CNT/PEG synapstors can generate the post-synaptic current, process signals in a spatiotemporal way based on the triggered post-synaptic current, facilitate memory with long-term potentiation (LTP) or depression (LTD), and learn with spike-timing dependent plasticity (STDP).

2.4.1 Post-synaptic Current

To measure the post-synaptic current, or the source-drain current I_{DS}, from a CNT/PEG synapstor, a constant channel voltage V_{DS} = 0.5 V was applied on the source with respect to the drain. While the input spike, which is a voltage pulse on the gate with the amplitude of 5 V and the duration of 1 ms, is applied on the gate, the post-synaptic current was then measured. The post-synaptic current was amplified and converted to analog voltage signals using a customized current-to-voltage converter circuit. Analog voltage signals were then sampled to a computer by an analog-to-digital converter circuit (National Instruments PCI-4472). Typical temporal responses of a CNT/PEG synapstor by an input spike of 5 V amplitude and 1 ms duration are shown in Figure 14. The experiments were repeated for 20 times and plotted as gray lines and the average post-synaptic current was calculated and plotted in a red line. As shown in Figure 14, the input spike triggers an excitatory post-synaptic current (EPSC) above the resting current (~ 5.2 nA), which reaches a peak value (~ 22.4 nA) at the end of the spike, and gradually decays back to the resting current in ~ 23.7 ms, which is similar to EPSC in a biological excitatory synapse[46]. The synaptic weight can be defined as the amplitude of an EPSC triggered by an input spike. It

should be noted that the amplitude and the duration of input spikes in this thesis are fixed at 5 V and 1 ms, if there is no further comment.

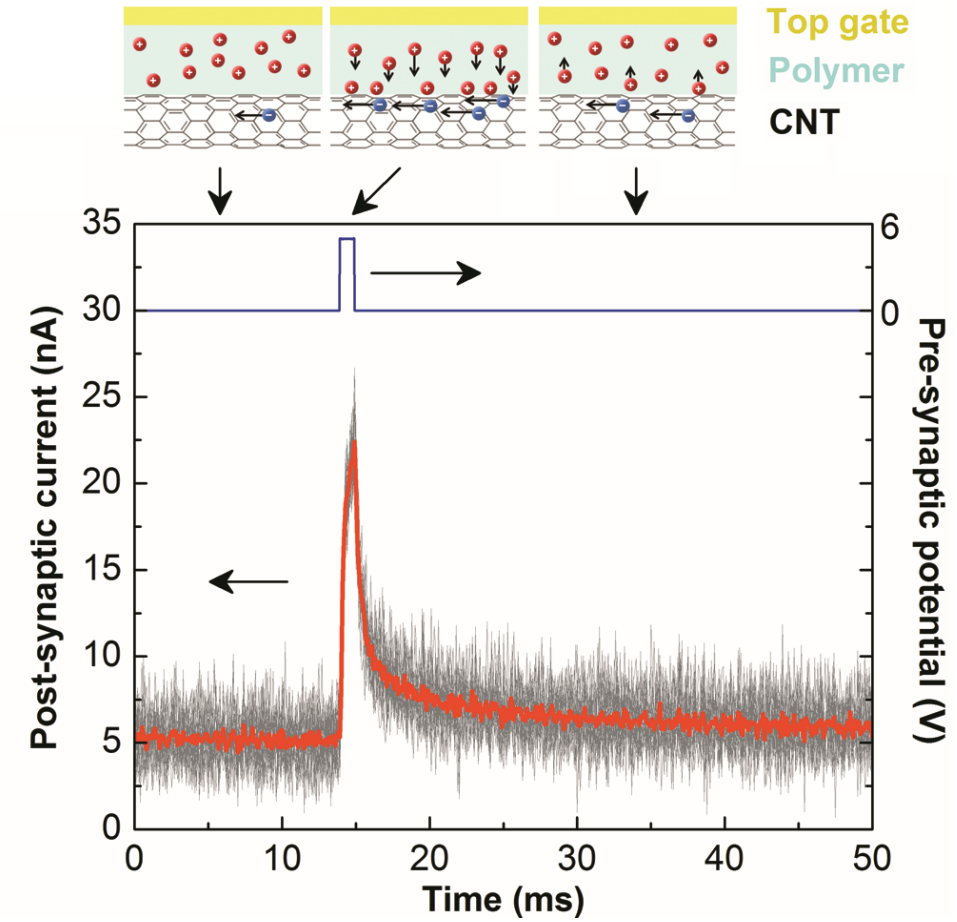


Figure 14. The post-synaptic current from a CNT/PEG synapstor[45].

The EPSC is generated by movements of hydrogen ions inside a PEG polymer layer which is triggered by an input spike on the gate. When the input spike drives mobile hydrogen ions inside a PEG polymer towards CNTs at the channel, such driven hydrogen ions can induce and accumulate the electrons in the CNTs and produce the post-synaptic current through the

CNT channel. This is because CNT/PEG synapstors have ambipolar behavior, which means that either holes or electrons can be mobile charge carriers. In CNT/PEG synapstors, the post-synaptic current was temporally increased by accumulated electrons at CNTs, which are induced by mobile hydrogen ions in a PEG layer nearby CNTs as illustrated in top insets in Figure14. Then, after the end of an input spike, the driven hydrogen ions are gradually and slowly drifted back to their equilibrium positions in a PEG layer, producing a gradually decaying current as plotted in Figure 14. As a combination of all described behaviors, EPSC can be triggered from a CNT/PEG synapstor.

It is known that there are two types of synapses, excitatory and inhibitory synapses as described in Chapter 1. The CNT/PEG synapstor can produce an excitatory post-synaptic current with a positive V_{DS} of 0.5 V. In order to make an inhibitory post-synaptic current (IPSC), a negative V_{DS} can be simply applied to a CNT/PEG synapstor. This will be discussed in details in the next chapter.

The average energy consumption for CNT/PEG synapstors to produce an EPSC also has been calculated as 7.5 pJ/spike, which is significantly lower than the energy consumption by conventional CMOS circuit (900 pJ/spike)[23] and is comparable with the energy consumption of memristors (~ 10−9 J/spike)[27,47,48] and phase-change memory (~ 10−9 ~ 10−8 J/spike)[49,50]. The average energy consumption of CNT/PEG synapstors was measured and calculated from the post-synaptic current triggered by an input spike with the amplitude of 5 V and the duration of 1 ms. The currents through the gate were 3 ~ 4 orders lower than the post-synaptic current, therefore the gate currents can be ignored in the energy consumption. The energy consumption

of the CNT/PEG synapstor per spike was derived by the integration of the power consumption of the CNT/PEG synapstors with respect to time during an EPSC. Total 115 CNT/PEG synapstors were tested and the average energy consumption was derived. If the input spike rate is assumed as 1 Hz, the average power consumption at 1 Hz input spike rate is 250 pW/synapstor, which is much less than the target power consumption of nW/synapstor in chapter1.

2.4.2 Spatiotemporal Signal Processing

To experiment spatiotemporal signal processing in CNT/PEG synapstors, two CNT/PEG synapstors were used in a simple network (Figure 15a). When two input spikes with an inter-spike interval, $\Delta t_{pre2\text{-}pre1}$, are applied at the CNT/PEG Synapstor 1 and the CNT/PEG Synapstor 2 respectively, they trigger two EPSCs (EPSC1 and EPSC2) with different amplitudes and two EPSCs are accumulated and producing a dynamic analog function of time and $\Delta t_{pre2\text{-}pre1}$ as shown in Figure 15b. When $\Delta t_{pre2\text{-}pre1} = 0$, the EPSC1 and EPSC2 are prompted simultaneously, the amplitude of the accumulated EPSC increases to the maximum value as seen at the fourth plot from the top in Figure 15b. When EPSC1 from the Synapstor 1 is triggered earlier than EPSC2 from the Synapstor 2 ($\Delta t_{pre2\text{-}pre1}>0$), EPSC1 was not affected by EPSC2 and there was slight increase in EPSC2 because of short lasting time of EPSC1; whereas EPSC1 from the Synapstor 1 is triggered later than EPSC2 from the Synapstor 2 ($\Delta t_{pre2\text{-}pre1}<0$), the amplitude of EPSC1 was increased due to EPSC2. When $\Delta t_{pre2\text{-}pre1}$ decreases further ($\Delta t_{pre2\text{-}pre1}<<0$), the increase in the EPSC1 by EPSC2 is gradually less significant as their being separated more than the lasting time of EPSC2.

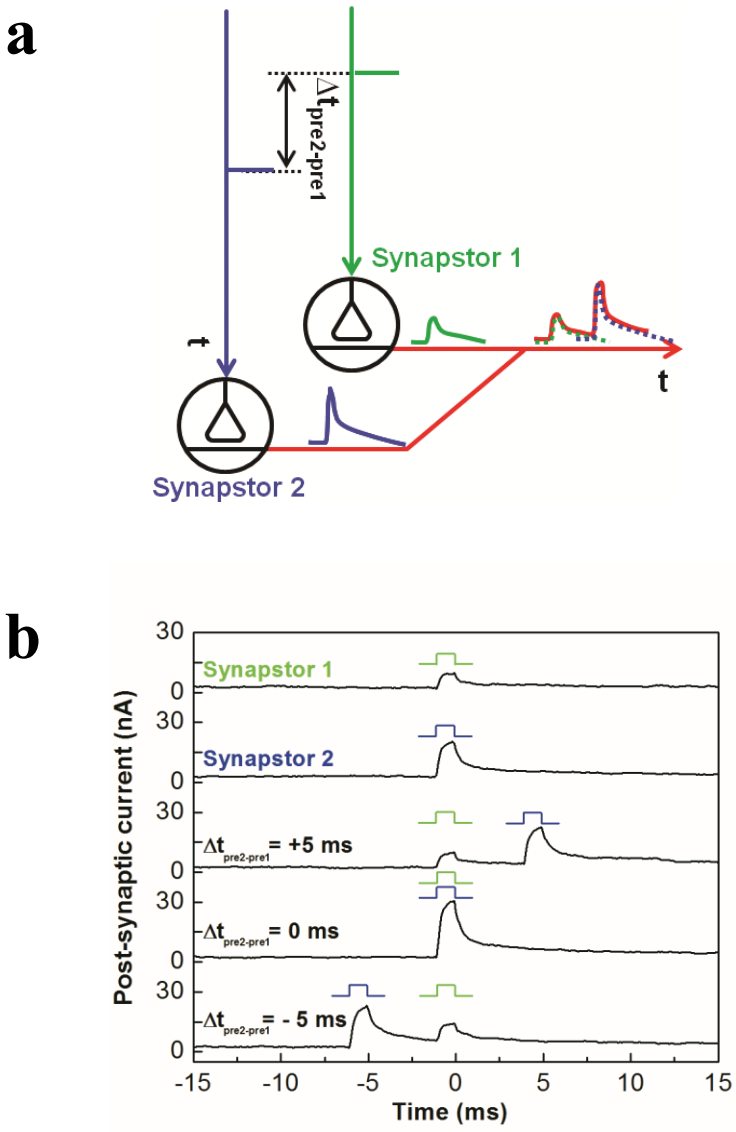


Figure 15. Spatiotemporal signal processing in CNT/PEG synapstors **a.** A scheme showing EPSC triggered by a pair of spatiotemporally correlated spikes applied through two CNT/PEG synapstors. **b.** EPSCs triggered by single and pairs of spatiotemporally correlated input spikes are shown versus time[45].

2.4.3 Synaptic Plasticity in CNT/PEG synapstors

The synaptic plasticity has been understood as the essential property for memory and learning in the brain[51,52]. Especially, the long-term plasticity is crucial for such functions because the change made through learning should be able to remain for long time to keep and utilize the learned information. The long-term plasticity (LTP) property of CNT/PEG synapstors was examined by modifying the synaptic weight, the amplitude of the post-synaptic, through the Long-Term Potentiation (LTP)/Long-Term Depression (LTD) stimulation. In this experiment, the amplitude of an EPSC was measured every 2 seconds for 16 minutes before the stimulation and one hour after the stimulation by applying an input spike to the gate as shown in Figure 16a. The relative change of the amplitude of an EPSC was then measured and calculated by comparing between the average EPSC amplitude of the first 1,000 seconds (500 data points) before the LTP/LTD stimulation was applied and the average EPSC amplitude of the last 1,000 seconds (500 data points) as seen in Figure 16b.The LTP/LTD stimulation was applied at t=0. The LTP stimulation was composed of two hundred input spikes at 500 Hz and the LTD stimulation was composed of one hundred post-synaptic spikes applied on the channel at 500 Hz. When the high frequency stimulation at 500 Hz was applied at 500 Hz, then, there was a significant increase or decrease in the amplitude of an EPSC as seen in Figure 16b. This is because the accumulated dehydrogenation and hydrogenation of CNTs at the channel changed the conductance through the channel, resulting increasing or decreasing in the amplitude of an EPSC.

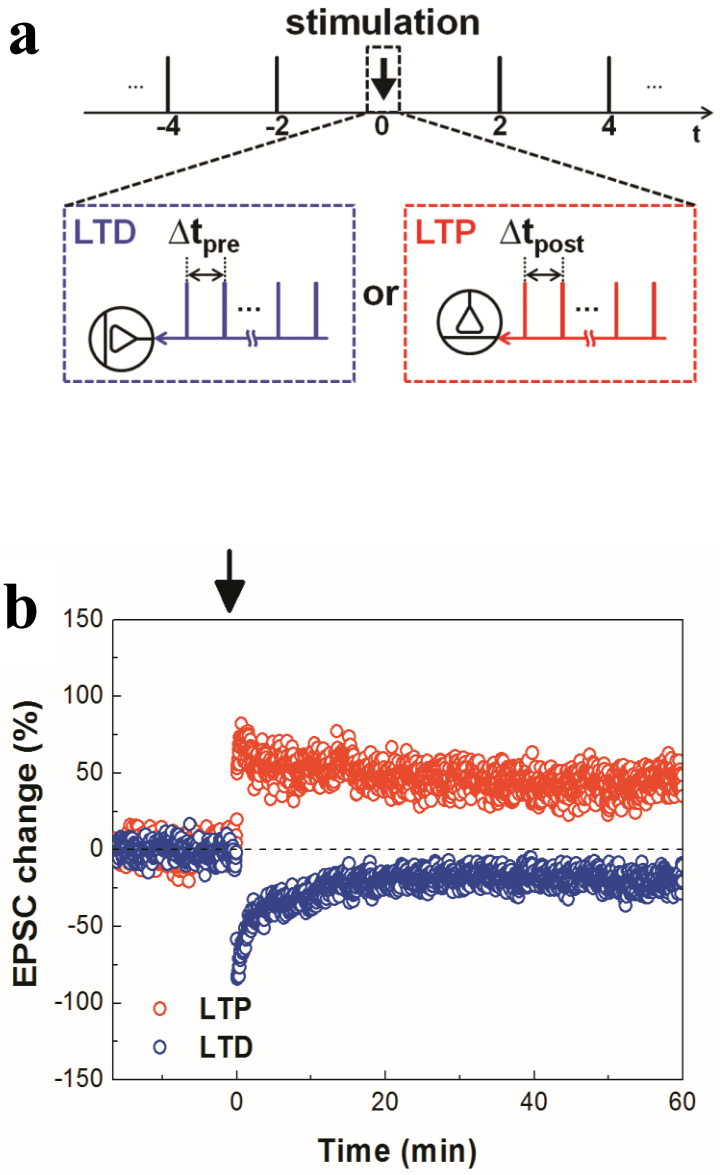


Figure 16. Synaptic plasticity in a CNT/PEG synapstor[45] **a.** The stimulation protocol to induce long-term potentiation (LTP) and depression (LTD) **b.** LTP/LTD measured in a CNT/PEG synapstor.

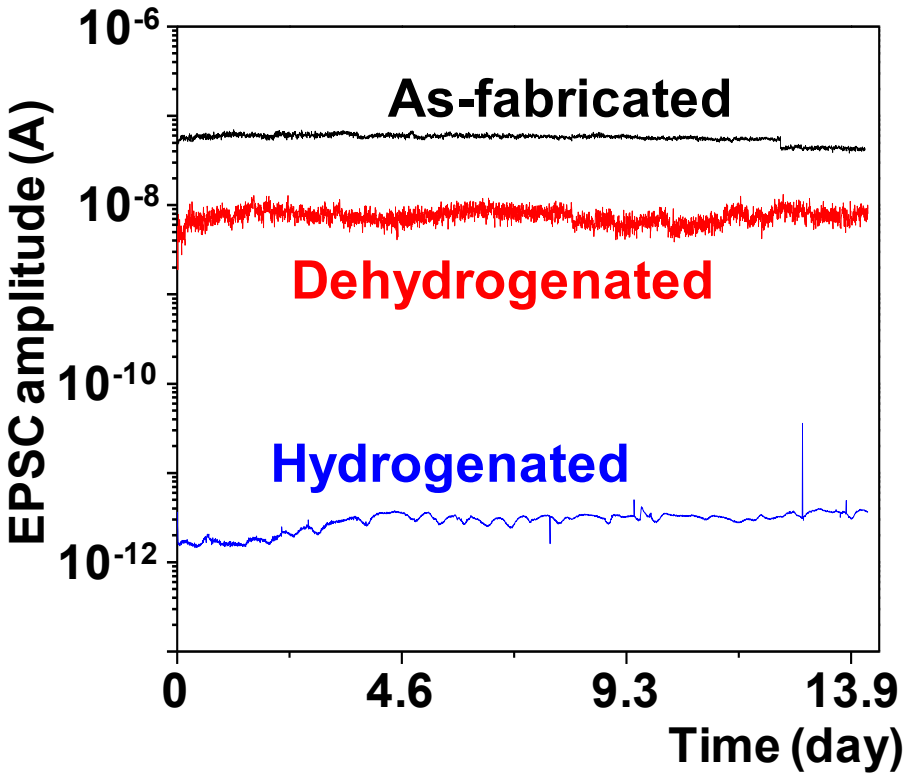


Figure 17. Non-volatile experiment in a CNT/PEG synapstor[35].

The non-volatile characteristic of CNT/PEG synapstors was further investigated by measuring the amplitude of an EPSC for two weeks. Total three CNT/PEG synapstors were tested every 5 minutes for two weeks – "As-fabricated", "Dehydrogenated", and "Hydrogenated". As-fabricated device was not applied any stimulation on it, while other two devices had sets of 7 V pre-synaptic spikes and post-synaptic spikes on them respectively. Essentially, the modification in current was remaining without significant change within two weeks, which indicates that the hydrogenated CNTs are stable, and the CNT hydrogenation is energetically favored (exothermic).

2.4.4 Learning in CNT/PEG synapstors

The amplitude of an EPSC can be modified to analog states quantitatively and reversibly as a function of numbers of spikes applied on the device and the amplitude of spikes. The modification of the EPSC amplitude is shown in Figure 18a and 18b as function of numbers of applied spikes with different amplitude of spikes. For decreasing case of the EPSC amplitude (Figure 18a), the EPSC amplitude was first adjusted to the maximum value (~ 9 nA) by applying a series of −7 V input spikes. Then, the EPSC amplitude was measured as applying a series of input spikes with a fixed duration of 1 ms, frequency of 500 Hz, and different amplitude of 3 V, 4 V, 5 V, and 6 V. For increasing case of the EPSC amplitude (Figure 18b), the EPSC amplitude was first adjusted to the minimum value (~ 2 nA) by applying a series of 7 V input spikes. Then, the EPSC amplitude was sequentially decreased as applying a series of input spikes with a fixed duration of 1 ms, frequency of 500 Hz, and different amplitude of −3 V, −4 V, −5 V, and −6 V. As seen in Figure 18, the modification rate of the EPSC amplitude can be adjusted by the amplitude of spikes and it was increased significantly when the amplitude of spikes increased from 3 V (−3 V) to 6 V (−6 V). Also, the amount of the EPSC amplitude change was increased as more spikes applied on the CNT/PEG synapstors as plotted in Figure 18. It indicates that the degree of hydrogenation or dehydrogenation in a CNT/PEG synapstor can be controlled to any analog state as a function of numbers of applied spikes and the amplitude of spikes.

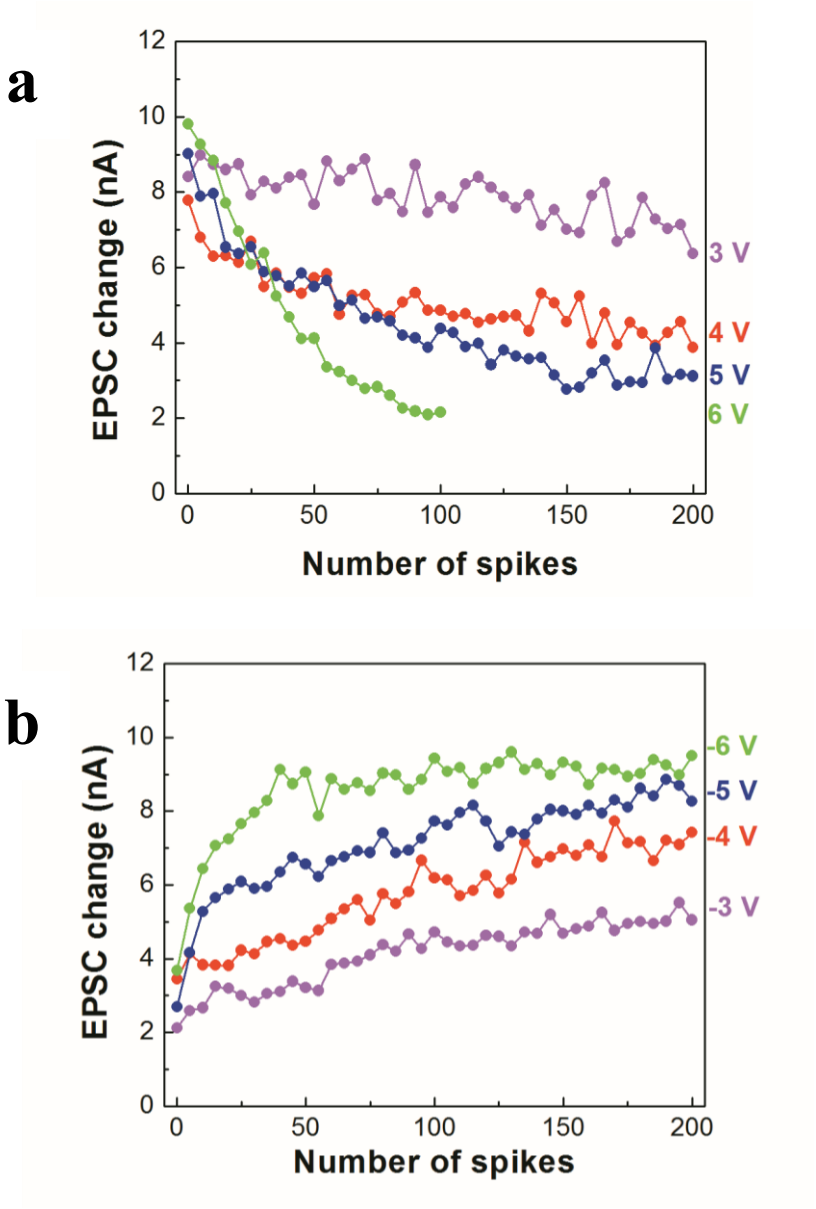


Figure 18. Learning in CNT/PEG synapstors **a.** when positive input spikes applied **b.** when negative input spikes applied on CNT/PEG synapstors.

2.4.5 Short Life-Time of CNT/PEG synapstors

As demonstrated in previous sections, the CNT/PEG synapstors successfully emulated the elementary functions of biological synapses such as the post-synaptic current, spatiotemporal signal processing, and synaptic plasticity. The CNT/PEG synapstors are operated based on dynamic interactions between CNTs and mobile hydrogen ions inside a PEG polymer layer, which is integrated into a CNT/PEG synapstor. However, there is a critical problem in CNT/PEG synapstors. The devices' properties are gradually degraded during repeated hydrogenation/dehydrogenation. Since hydrogenation and dehydrogenation processes are the chemical reactions between carbon atoms and mobile hydrogen ions, it will gradually and slowly break the structure of CNTs, resulting in significant degradation of device performance. This can be critical issue for building a spike neuromorphic circuit because the life-time of synapstors will decide the total life span of a neuromorphic circuit. Therefore, it is desirable to have a device or synapstor which can operate without chemical reactions inside.

2.5 Carbon Nanotube (CNT) / C60 synapstor

2.5.1 Structure and Fabrication

In order to avoid using the chemical reaction as a underlying mechanism in a synapstor, C60 molecules were used and integrated into a CNT synapstor. First of all, the charge carrier concentration in CNTs can be sensitively adjusted by surrounding electronic charges[53,54]. It is also well known that CNT transistors typically show p-type characteristics as discussed earlier

section. Therefore, if electrons can be provided nearby CNTs, then the conductance of CNTs can be adjusted by the amount of electrons provided. For such purpose, C60 molecules were introduced. C60 molecules, spherical fullerene molecules, have been highlighted as one of candidating materials for nano-scale electronic devices because of their strong electron affinity from their rehybridization at their molecular orbitals. As a result, electrons trapped into the C60 molecule can be stably remained[53-55]. The structure of a CNT/C60 synapstor is shown in Figure 19[56].

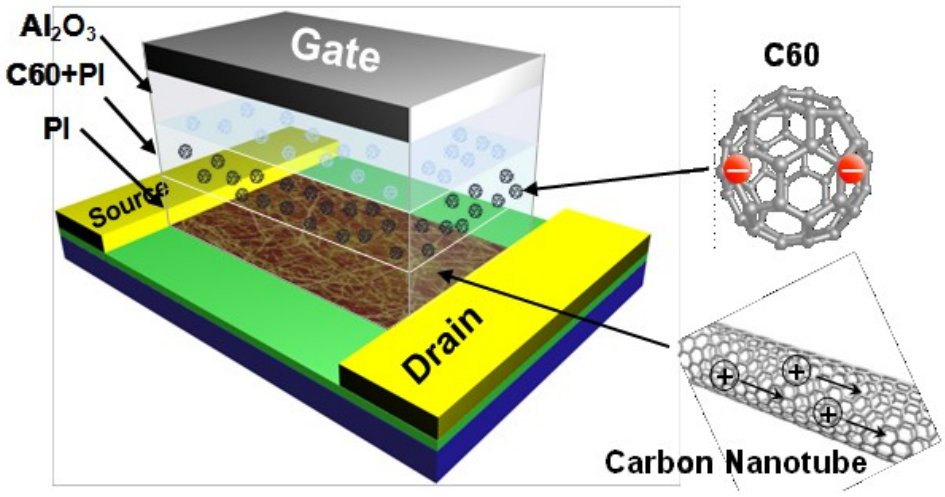


Figure 19. The structure of a CNT/C60 synapstor[56].

As CNT/PEG synapstors, the channel was fabricated by a randomly aligned CNTs network and CNTs were spin-coated using 98% semiconducting single-wall CNTs solution (IsoNanotubes-S). In contrast to CNT/PEG synapstors, for CNT/C60 synapstors, semiconducting CNTs were used because there is no chemical reaction related in this device to change the

conductance of CNTs. Then, Ti/Au (5 nm / 45 nm) source and drain electrodes were made to connect a CNT channel. The CNT channel was then patterned as having a length of 30 μm and width of 8 μm. After CNT channel definition, a polyimide (PI) barrier layer with 30 nm thickness and a second PI layer with 30 nm thickness which containing C60 molecules as a electron trapping layer were sequentially deposited on top of a CNT channel and patterned at the same time by O_2 plasma etching. For the second PI layer with C60 molecules, C60 and PI solution was made by dissolving a C60 derivative, 6,6-phenyl-C61 butyric acid methyl ester (PCBM) and PI in a 1-vinyl-2-pyrrolidinone solvent with a PCBM:PI weight ratio of 1:22. The second PI layer was deposited by spin-coating of PCBM:PI solution. An Al_2O_3 layer with 30 nm thickness was deposited on top of PI layers as a charge protection layer between the gate electrodes and C60 molecules in the second PI layer. Finally, the top gate electrode with Ti/Al (15nm / 100nm) was deposited by e-beam evaporation and patterned by conventional photolithography.

2.5.2 Operation Mechanism

Typical I_{DS}-V_G curve at V_{DS}= 0.5 V is shown in Figure 20[56]. As typical CNT transistors with exposed CNTs to the environment, a CNT/C60 synapstor is also showing p-type characteristics, which indicates that holes are the major mobile charge carrier. When V_G is swept from −6 V to 6 V, the source-drain current (I_{DS}) is significantly dropped to pA range from μA around V_G = 0 V and stay around pA when $V_G >$ 0 V. The sub-threshold swing at around $V_G \approx$ 0 V was around 460 mV/dec. When V_G starts sweeping back from 6 V to −6 V, I_{DS} starts

increasing before V_G= 0 V and exhibiting the hysteresis with counter-clockwise direction. In Figure 20, the direction of hysteresis was indicated by two arrows with black and red colors. A black arrow is I_{DS}-V_G curve when V_G was swept from −6 V to 6 V and a red arrow is I_{DS}-V_G curve when VG was swept from 6 V to −6 V. When V_G decreases to −6 V, I_{DS} is on ~ 10^7 A and staying at the similar level. This is caused by the trapped electrons inside C60 molecules at the second PI layer during positive V_G sweep. The shift of a threshold voltage was made by trapped electrons. The ratio of I_{DS} at V_G= 0 V was about 104, roughly two order difference.

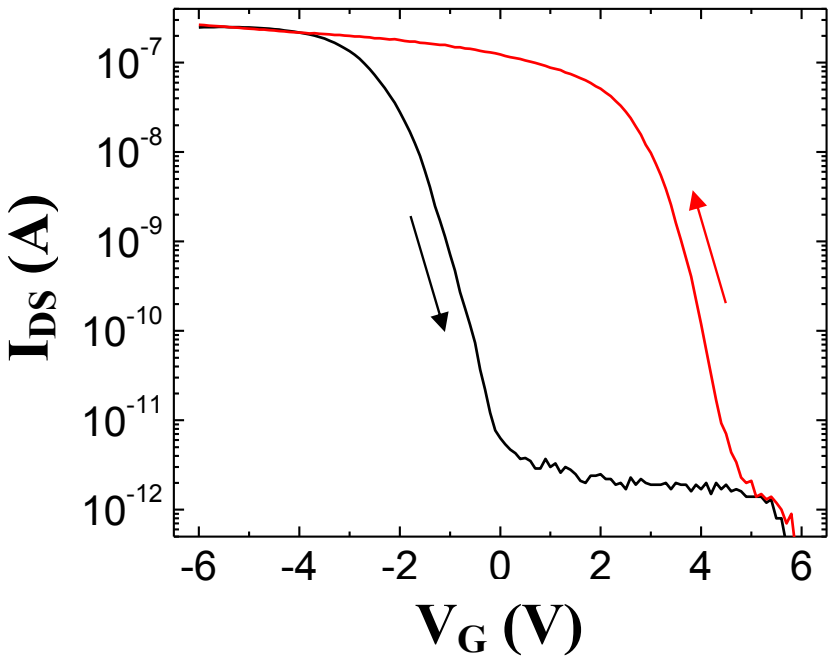


Figure 20. Typical I_{DS}-V_G curve in a CNT/C60 synapstor[56].

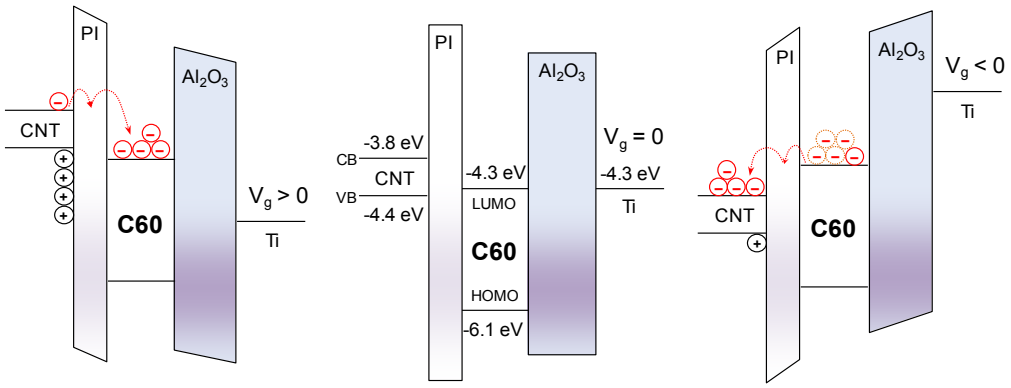


Figure 21. Energy diagram of a CNT/C60 synapstor[56].

It is more obvious and easy to understand to see the energy diagrams of a CNT/C60 synapstor as shown in Figure 21. When the positive V_G is applied on a CNT/C60 synapstor (left schematic in Figure 21), the lowest unoccupied molecular orbital (LUMO) energy level of C60 molecules in the second PI layer is reduced below CNTs' energy level, thus inducing electrons being trapped into C60 molecules via hopping tunneling through the PI layer and C60 molecules in the PI layer[57,58]. As more electrons are injected into C60 molecules, they can induce more holes as counter charges in CNTs, thus resulting in decreasing of the threshold voltage. When the zero gate voltage is applied (middle schematic in Figure 21), there is no electron injection happening because of absence of driving potential for electrons to tunnel. When the negative gate voltage is applied (right schematic in Figure 21), the highest occupied molecular orbital (HOMO) energy level of C60 molecules is above the CNTs' energy level, inducing escaping of electrons and increasing of the threshold voltage.

2.6 Synaptic Properties of CNT/C60 synapstors

Similarly with CNT/PEG synapstors, the synaptic properties of CNT/C60 synapstors have been examined such as the post-synaptic current, spatiotemporal signal processing, synaptic plasticity, and learning. The same customized electronic circuit was used, which is described in section 2.4. The configuration of an input spike is the same as one used for CNT/PEG synapstors – 1 ms duration and 5 V amplitude, when there is no additional comments.

2.6.1 Post-synaptic Current of CNT/C60 synapstors

The post-synaptic current in a CNT/C60 synapstor was measured from the source-drain current (I_{DS}) with a constant source-drain voltage V_{DS}= 0.5 V while the input spike is applied on the gate of a CNT/C60 synapstor. When the positive voltage pulse (an input spike) is applied on the gate of a CNT/C60 synapstor, electrons are attracted and injected into C60 molecules in the PI layer as explained in the previous section (however, the current drops during the pulse because the device is a p-type transistor). As a result, more holes can be induced at CNTs after the input spike, thus producing higher current level as seen in Figure 22. As time goes, trapped electrons in C60 molecules are gradually and slowly starting escaping, causing decreasing I_{DS} as function of time. Therefore, it generates an excitatory post-synaptic current (EPSC) similar to one from a CNT/PEG synapstor, while the lasting time of the post-synaptic current from a CNT/C60 synapstor is much longer (> 30 seconds). This indicates that the energy required for trapped electrons to escape is much higher than the energy for mobile hydrogen ions to go back to their equilibrium position in a PEG layer. Typical post-synaptic current from a CNT/C60

synapstor by an input spike of 5 V amplitude and 1 ms duration are shown in Figure 22. The experiments were repeated for 20 times and plotted as gray lines and the average post-synaptic current was calculated and plotted in a red line. Similarly, the synaptic weight can be defined as the amplitude of an EPSC triggered by an input spike. The average power consumption in CNT/C60 synapstors was calculated as 2.6 nW/synapstor at 1 Hz input spike rate, which is larger than the power consumption in CNT/PEG synapstors due to their long lasting time.

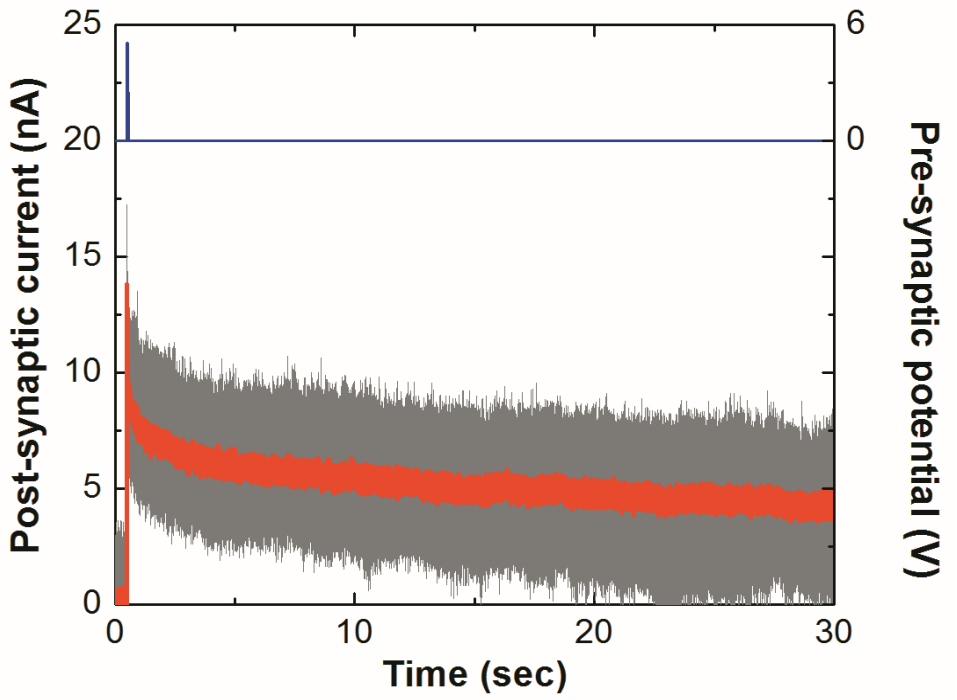


Figure 22. The post-synaptic current in a CNT/C60 synapstor.

2.6.2 Spatiotemporal Signal Processing in CNT/C60 synapstors

The spatiotemporal signal processing of CNT/C60 synapstors was experimented using two CNT/C60 synapstors as shown in Figure 23a. When two input spikes with an inter-spike interval, $\Delta t_{pre2\text{-}pre1}$, are applied at the CNT/C60 Synapstor 1 and the CNT/C60 Synapstor 2 respectively, they trigger two EPSCs (EPSC1 in green, figure 23b, and EPSC2 in blue, Figure 23 c) with different amplitudes and lasting time. Both EPSCs from two CNT/C60 synapstors can be accumulated and produce a dynamic analog function of time and $\Delta t_{pre2\text{-}pre1}$ as shown in Figure 23d, 23e, 23f. In Figure 23d, when $\Delta t_{pre2\text{-}pre1}$ is 1 second, the amplitude of EPSC2 was increased by EPSC1. As $\Delta t_{pre2\text{-}pre1}$ is increasing, or as two input spikes are separating, the amount of change in the amplitude of EPSC2 by EPSC1 was decrease as shown in Figure 23e and 23f. For instance, the amplitude of EPSC2 at $\Delta t_{pre2\text{-}pre1}$= 10 seconds (Figure 23e) is larger than the amplitude of EPSC2 at $\Delta t_{pre2\text{-}pre1}$= 30 seconds (Figure 23f). Since the lasting time of the post-synaptic current is longer (> 30 seconds) than one of CNT/PEG synapstors, there can be more correlation in time between EPSCs. Therefore, CNT/C60 synapstors can possibly correlate spikes within 30 seconds and the degree of correlation will be determined based on the separation of spikes in time, the interval between spikes. Considering the lasting time of CNT/PEG synapstors (~ ms), CNT/C60 synapstors have much longer correlation time window. However, the power consumption will be larger because of long lasting time of the post-synaptic current.

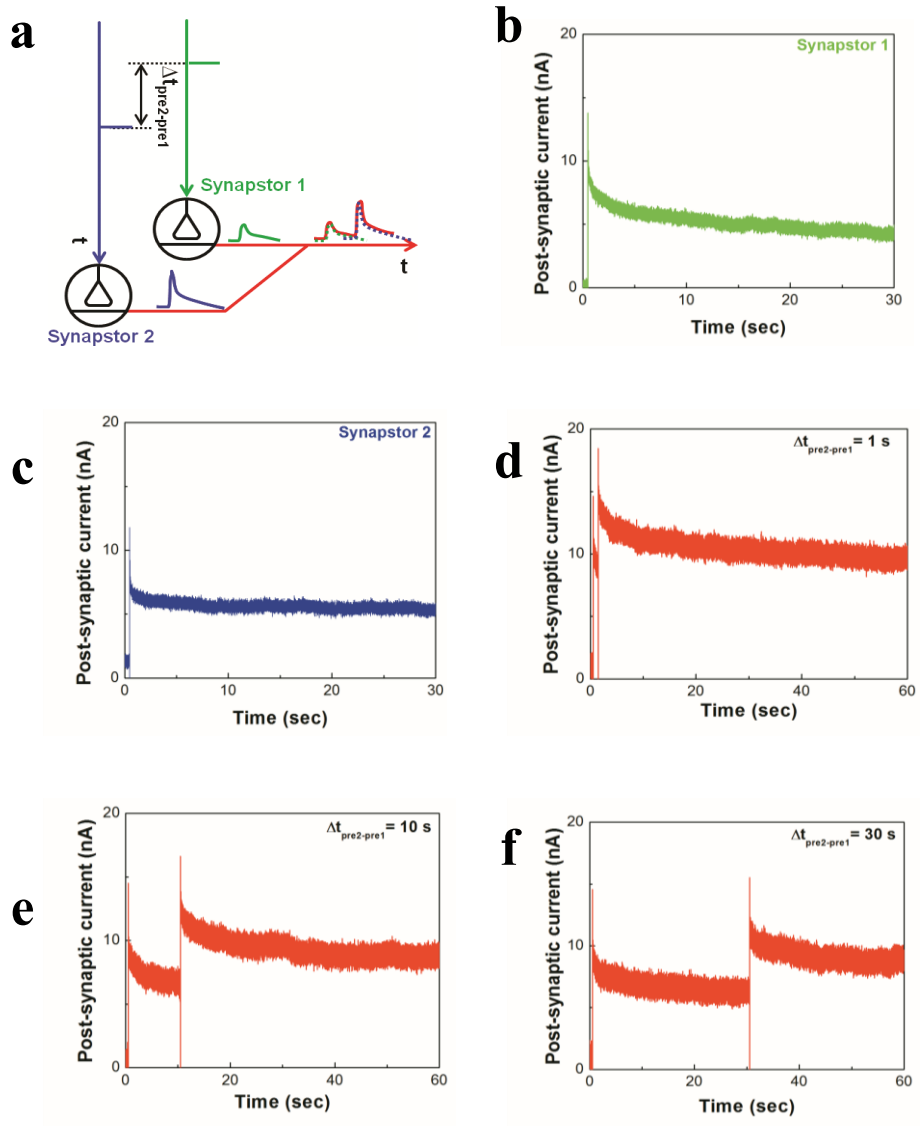


Figure 23. Spatiotemporal signal processing in CNT/C60 synapstors **a.** A schematic for spatiotemporal signal processing experiment **b.** Single EPSC from Synapstor 1 **c.** Single EPSC from Synapstor 2 **d.** The accumulated EPSC with $\Delta t_{pre2\text{-}pre1}$= 1 s **e.** The accumulated EPSC with $\Delta t_{pre2\text{-}pre1}$= 10 s **f.** The accumulated EPSC with $\Delta t_{pre2\text{-}pre1}$= 30 s.

2.6.3 Synaptic Plasticity in CNT/C60 synapstors

The synaptic plasticity in CNT/C60 synapstors was also examined. The EPSC amplitude was configured to different state as represented in different colors in Figure24. The change of the EPSC amplitude at V_{DS}= 0.5 V was measured for one week after modification. As shown in Figure 24, the modified EPSC amplitude can be remained for one week. This result implies that CNT/C60 synapstors have the synaptic plasticity and non-volatile characteristic. The non-volatile characteristic could be possibly originated from the strong electron affinity of C60 molecules in the PI layer. The modified EPSC amplitude was gradually increased or decreased as time goes and it could be induced by the leakage of electrons from C60 molecules. This leakage problem can be potentially relaxed by increasing the thickness of the PI layer or altering the insulating material.

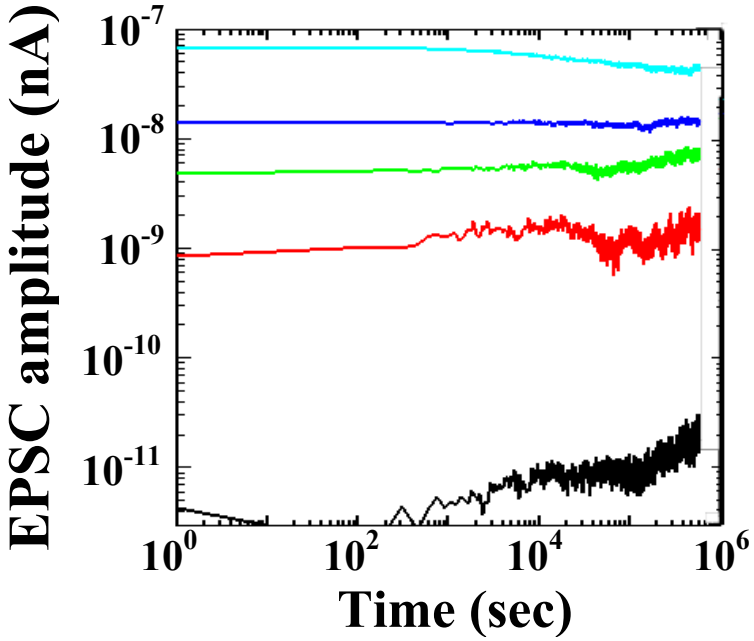


Figure 24. Synaptic plasticity in CNT/C60 synapstors.

2.6.4 Learning in CNT/C60 synapstors

The amplitude of an EPSC from a CNT/C60 synapstors can be also configured to analog states quantitatively and reversibly as a function of numbers of spikes applied on the device and the amplitude of spikes. The modification of the EPSC amplitude is shown in Figure 25a and 25b versus numbers of applied spikes with different amplitude. The duration of spikes used in this experiment was fixed at 1 ms regardless of the amplitude. For experiments of tuning with positive amplitude spikes (Figure 25a), the EPSC amplitude was first modified to its lowest value by applying a series of −8 V input spikes. Then, the change in the EPSC amplitude was measured as applying a series of input spikes with a fixed duration of 1 ms, frequency of 500 Hz (2 ms pulse interval), and different amplitude of 2 V, 4 V, 6 V, and 8 V. Similarly, for experiment with negative amplitude spikes, the EPSC amplitude was tuned to its maximum value by 8 V spikes and then, a series of input spikes was applied with a fixed duration of 1 ms, frequency of 500 Hz, and different amplitude of −2 V, −4 V, −6 V, and −8 V. As seen in Figure 25a, the EPSC amplitude was gradually increased as numbers of applied spikes increased when positive spikes applied. This is because more electrons are trapped in C60 molecules accumulatively as applied more positive spikes. The rate of the change in the EPSC amplitude is also a function of the amplitude of applied spikes – higher amplitude, faster and more change in the EPSC amplitude. Similarly, the EPSC amplitude was gradually decreased as more negative spikes applied and its rate depends on the amplitude of spikes used. It indicates that the amount of electrons trapped in C60 molecules can be adjusted to any analog state as a function of numbers of applied spikes and the amplitude of spikes.

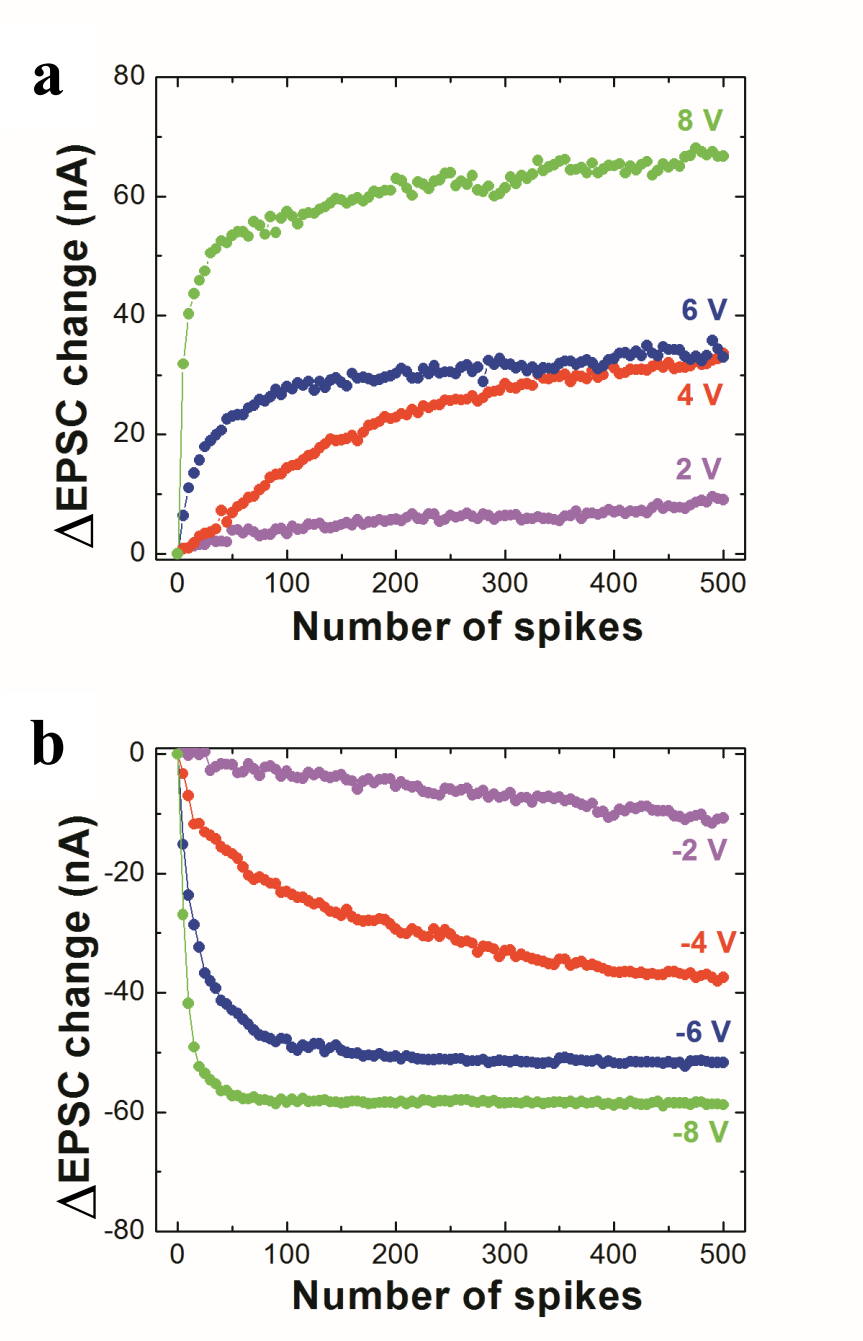


Figure 25. Learning in CNT/C60 synapstors **a.** when positive input spikes applied **b.** when negative input spikes applied on CNT/C60 synapstors.

2.7 CNT Synapstor Comparison

As introduced and demonstrated in previous sections, CNT/C60 synapstors can successfully emulate the elementary functions of biological synapses, similar with CNT/PEG synapstors, such as the post-synaptic current, spatiotemporal signal processing, and synaptic plasticity with low power consumption of 2.6 nW at the input spike rate of 1 Hz. The CNT/C60 synapstors are operated based on the change of conductance by induced hole carriers from trapped electrons inside C60 molecules. The comparison of two CNT synapstors with prior art is made in Table 3. The power consumption was calculated when the input spike rate is 1 Hz in Table 3.

	Spatiotemporal correlation (post-synaptic response)	Synaptic plasticity	Power consumption per device/circuit	Scalabiilty
CNT/PEG synapstor[45]	Yes	Yes	250 pW	Yes
CNT/C60 synapstor[56]	Yes	Yes	2.6 nW	Yes
Analog CMOS[22]	Yes	Yes	1 μW	No
Analog CMOS[23]	Yes	Yes	1.5 μW	No
Floating gate[24]	No	Yes	4 nW	Yes
Floating gate[25]	No	Yes	2.5 μW	Yes
Resistive[26]	No	Yes	0.3 mW	Yes
Memristive[27]	No	Yes	1.6 μW	Yes

Table 3. Comparison of CNT synapstors with prior art.

3. Spike Neuromorphic Circuit (SNC)

3.1 Schematic Overview

Since the properties of CNT synapstors have been discussed, it will naturally lead to build a neuromorphic circuit based on them as a next step. Before moving on the implementation of a neurormorphic circuit, the operation of biological neurons and synapses will be reviewed briefly again in this section. A biological neuron is composed of a large number of synapses and a soma, a cell body. It can transmit and process signals in a spike format. When a synapse is triggered by a spike, it generates a temporal response, called the post-synaptic current (PSC). All triggered post-synaptic current from numerous synapses will be collected and accumulated in a soma. If the potential change by the accumulated PSCs is above the threshold value, then a neuron will fire output spikes corresponding to the level of PSCs. The amplitude of PSCs in synapses can be also modified to any analog states. Therefore, a neuron can establish complex spatiotemporal correlations between sets of input spikes and output spikes by utilizing all the properties mentioned above. In order to emulate such functions of biological neurons, it is also crucial, as well as CNT synapstors, how to build a neuromorphic circuit based on CNT synapstors. The neuromorphic circuit implemented from CNT synapstors will be called as a Spike Neuromorphic Circuit (SNC) in this paper because our circuit can handle spike signals while emulating neural network properties. The schematic overview is illustrated in Figure 26a. The detail explanation will be given sequentially following the operation in a SNC.

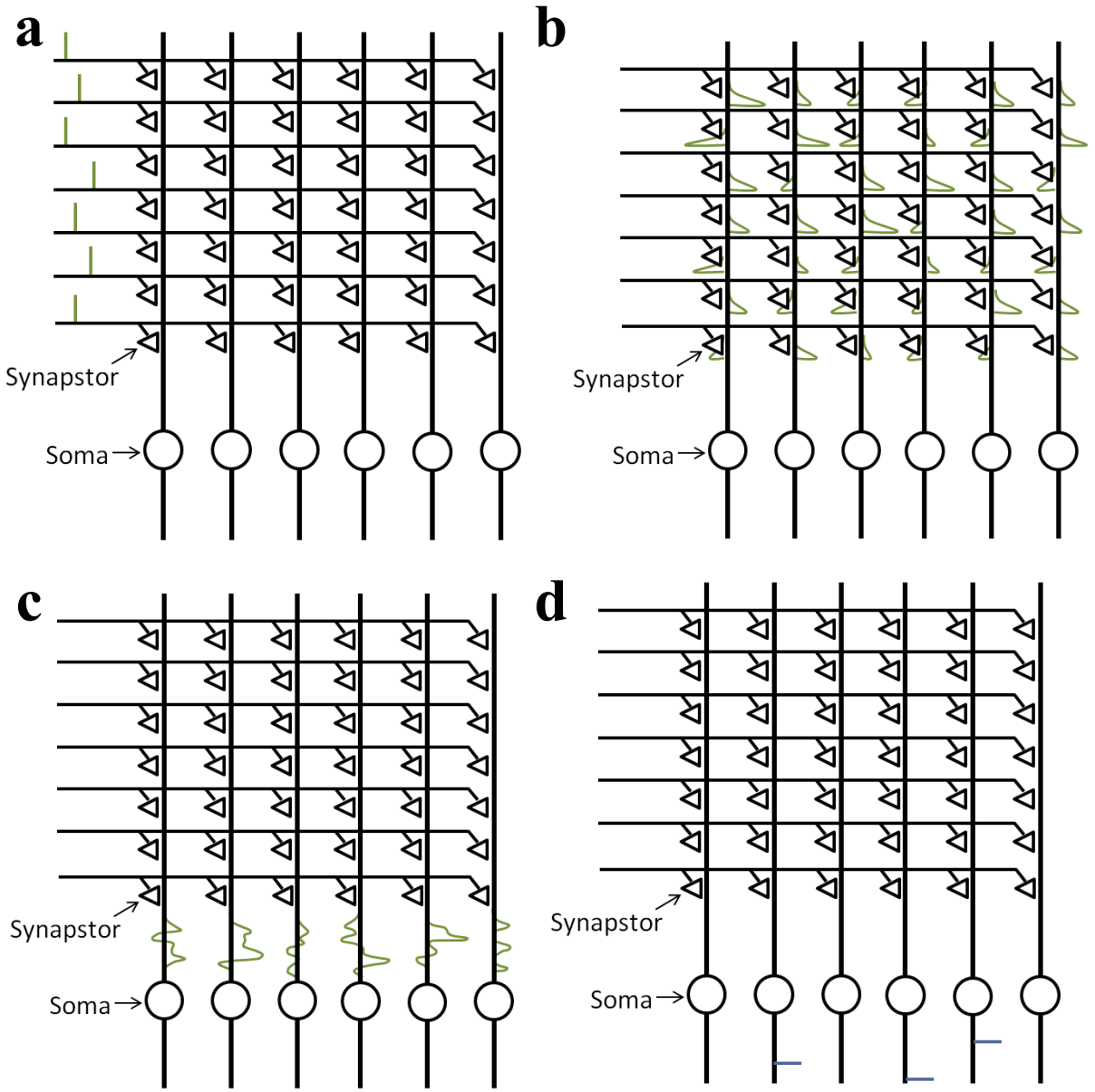


Figure 26. Spike Neuromorphic Circuit (SNC) **a.** Schematic overview of a SNC with input spikes **b.** post-synaptic currents (PSC) triggered by input spikes **c.** the accumulated PSCs generated **d.** output spikes triggered from the accumulated PSCs.

In a SNC, there is an array of CNT synapstors, in which each row of CNT synapstors will have a shared input spike channel and each column of CNT synapstors will have a shared output channel to a soma circuit as seen in Figure 26a. Therefore, an input spike on one of input channels can trigger multiple CNT synapstors simultaneously and all the post-synaptic current from CNT synapstors in a column will be collected and accumulated in a soma circuit. First, a set of input spikes will be arrived on input channels of a SNC (Figure 26a). Input spikes represent sensing signals from the external environment. The timing and the rate of spikes contain the analog information about the sensing signals from the sensors. In other words, sensors will sense the external environment, and then convert sensed information into the spikes with timing and rate. Then, each input spike will trigger the post-synaptic currents from CNT synapstors which have the input spikes as illustrated in Figure 26b. Then, all the triggered post-synaptic current will go to soma circuits in each column and produce the accumulated PSCs as seen in Figure 26c. The output spikes will be generated at soma circuits when the accumulated PSC level is above the threshold value as seen in Figure 26d. A SNC will have the following properties with the explained structure. First, it can process signals in parallel because an input spike can trigger multiple post-synaptic current and it will affect the generation of output spikes. Second, it can establish the spatiotemporal correlation between input spikes and output spikes from the post-synaptic currents of CNT synapstors. Third, it has the learning capability. The PSC amplitude of CNT synapstors can be modified to any analog states and memorized for a long time. Therefore, if the PSC amplitudes of CNT synapstors are adjusted in a correct way, then such change will create the better correlation between a set of input spikes and output spikes,

thus producing better performance eventually when a SNC interacts with the environment. Last, a SNC will consume low power intrinsically from the power consumption of CNT synapstors. The detail information about each component will be introduced in following sections.

3.2 Soma – Integrate-and-Fire (I&F) Circuit

In order to generate the output spikes based on the level of the accumulated post-synaptic currents, a soma circuit is required. There is a good candidate for such purpose, the Integrate-and-Fire (I&F) circuit[23]. For a SNC, the conventional I&F circuit was used and the schematic is shown in Figure 27.

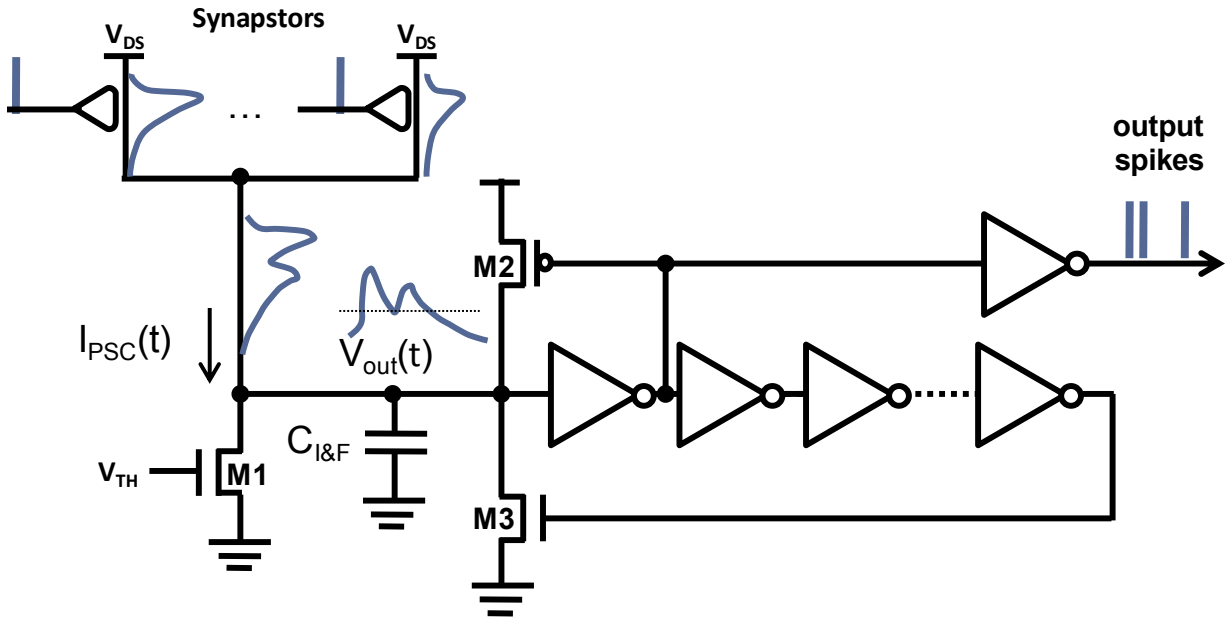


Figure 27. The schematic of an Integrate-and-Fire circuit in a SNC.

I&F circuit was built with a conventional CMOS technology and served as a soma circuit in a SNC. When CNT synapstors produced multiple post-synaptic currents by input spikes, they will be collected at I&F circuit interface (I_{PSC}). There is a leaky CMOS transistor to control the threshold current level by the bias, V_{TH}. The collected post-synaptic current will be subtracted by the leaky current and then, rest of current will go to a membrane capacitor ($C_{I\&F}$). The coming current will be integrated on the membrane capacitor and build up the corresponding voltages (V_{out}). If the voltage on the membrane capacitor is above the logical threshold of the first stage amplifier, then it will be propagated to next amplifiers. After the first stage amplifier flips its output, a p-type CMOS transistor, M2, will be turned on and provide more current to the membrane capacitor. By doing that, M2 can help I&F circuit maintain the constant pulse-width as ~1 ms. After the delay of few stages of amplifiers, a n-type CMOS transistor, M3, will be turned on, discharge the membrane capacitor to the ground and finish generating an output spike. Therefore, an output spike can be generated by operation of two CMOS transistors (M2 and M3) and amplifiers. When the output spike is generated, the membrane capacitor is reset to the ground by M3 and ready to integrate the following PSCs. The transfer function between the constant input current (I_{PSC}) and the rate of output spikes is plotted in Figure 28.If the input current, which is the accumulated PSCs (I_{PSC}), is below the threshold value (~ 5 nA), then no output spike is generated from an I&F circuit. As the input current increases from 5 nA to 40 nA, higher rate of output spikes are generated and the change of the frequency in output spikes is linearly increased as seen in Figure 28. When the input current is more than 40 nA, the output

spike frequency starts being saturated gradually. The saturated output spike frequency is about 70 Hz.

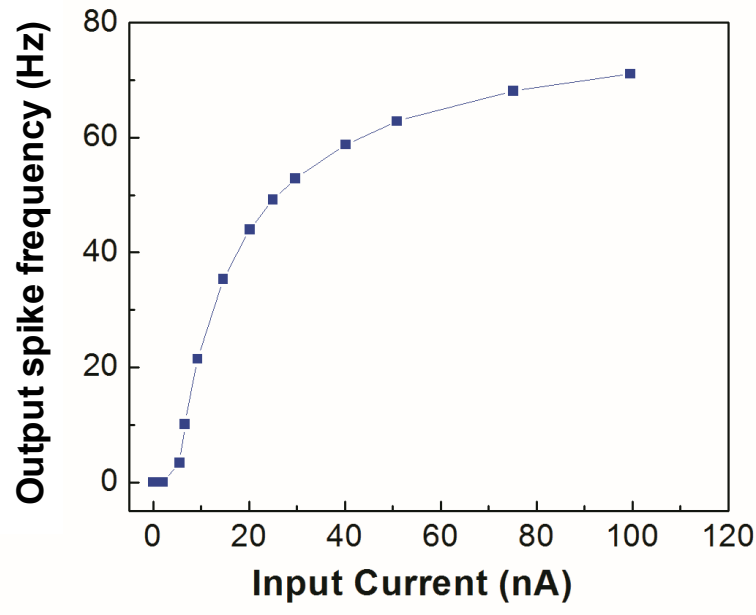


Figure 28. Transfer function of a single I&F circuit.

3.3 Excitatory and Inhibitory Synapstors in a SNC

In order to produce both excitatory and inhibitory post-synaptic currents from CNT synapstors, it is required to make two V_{DS} with opposite polarity due to their nature of operation. Therefore, two columns were introduced to produce both excitatory and inhibitory post-synaptic current, which are positive and negative post-synaptic currents respectively as shown in Figure 29. The blue horizontal lines at CNT synapstors mean the positive V_{DS} (0.5 V) and the red

horizontal lines at CNT synapstors mean the negative V_{DS} (−0.5 V). As seen in Figure 29, there are two columns of CNT synapstors in a SNC and their post-synaptic currents are collected at the end. The collected post-synaptic current is the sum of both excitatory (I_{EPSC}) and inhibitory post-synaptic currents (I_{IPSC}). The total post-synaptic currents (I_{PSC}) will then go to two I&F circuits.

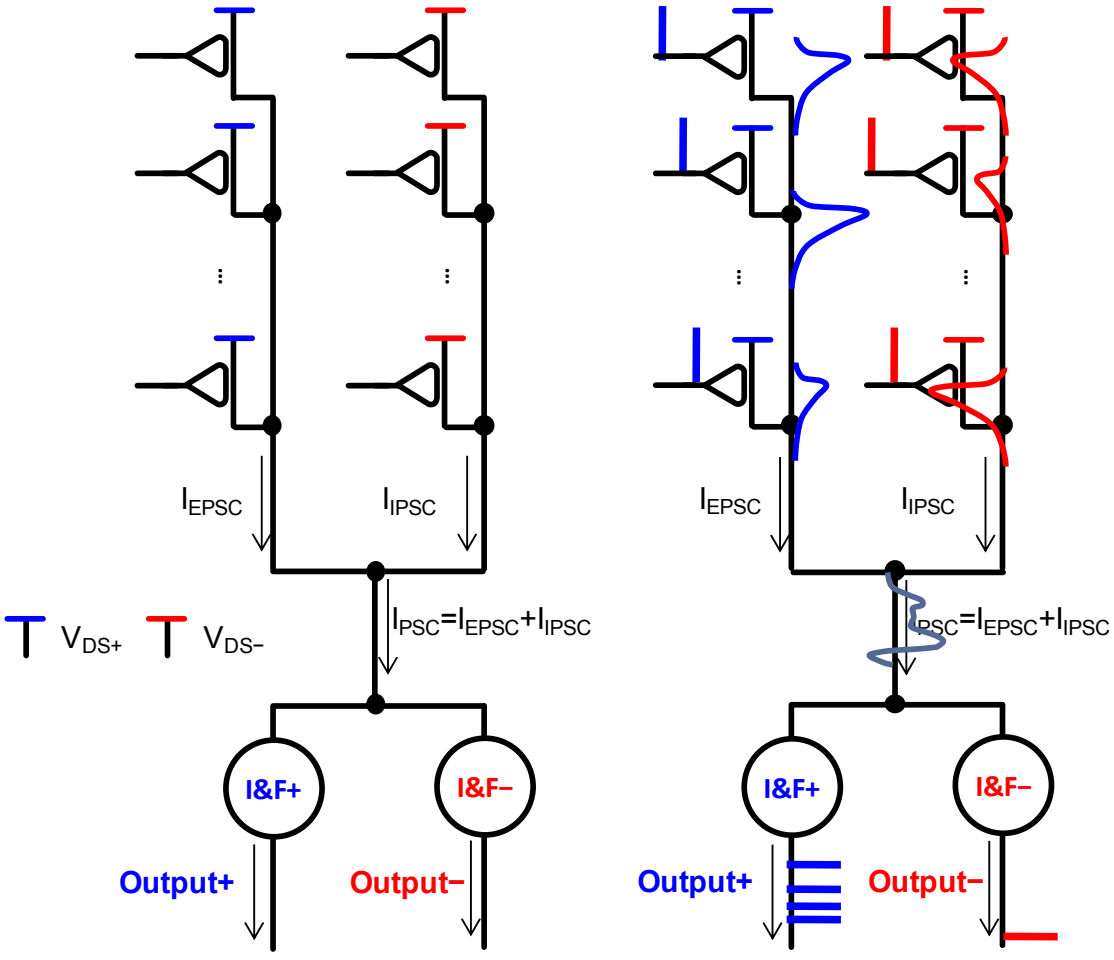
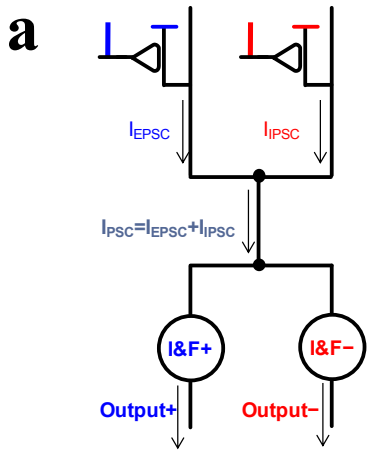


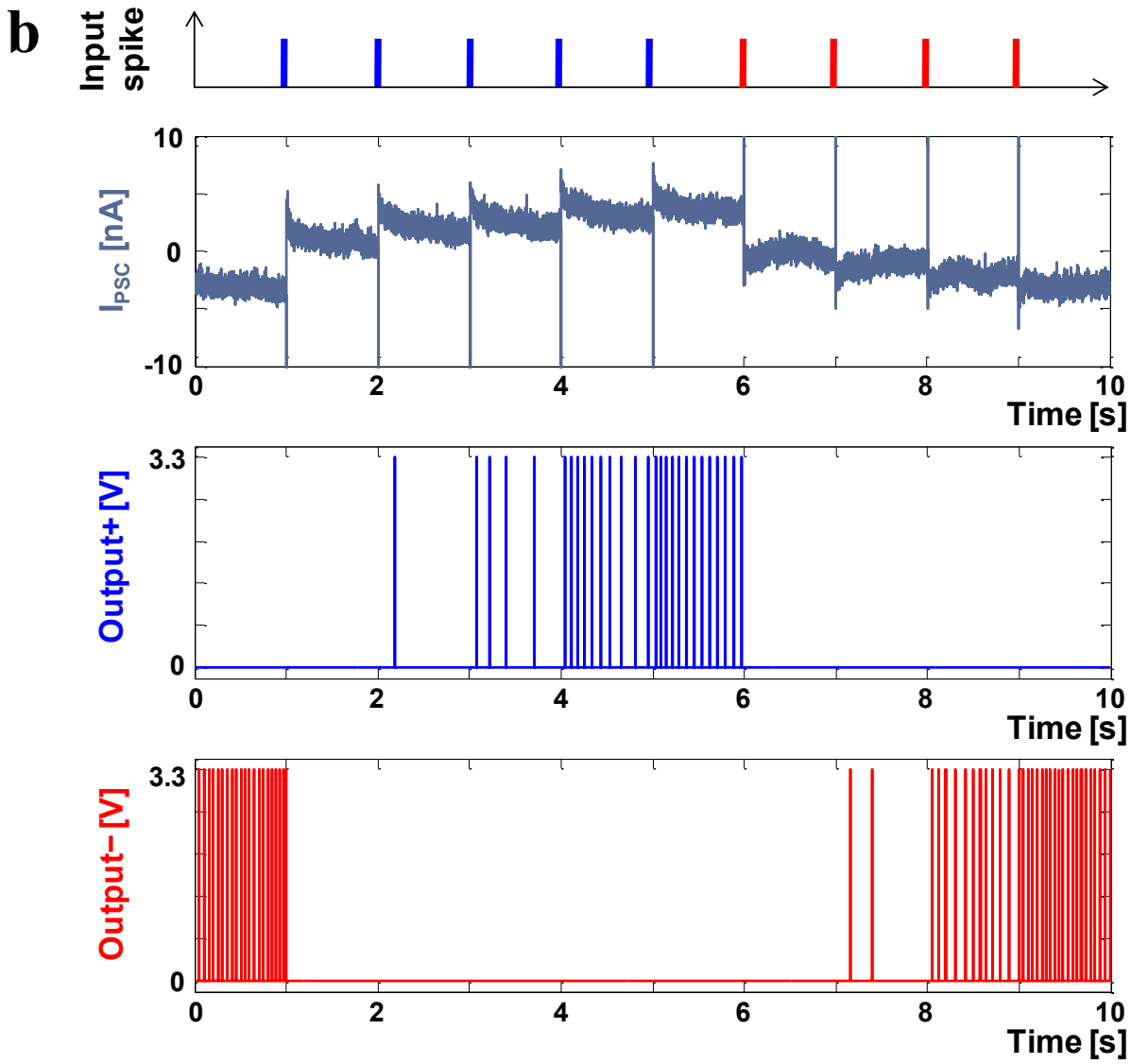
Figure 29. Excitatory and inhibitory columns in a SNC **(left)** A schematic view of excitatory and inhibitory synapstors **(right)** Operation of two columns – excitatory and inhibitory synapstors.

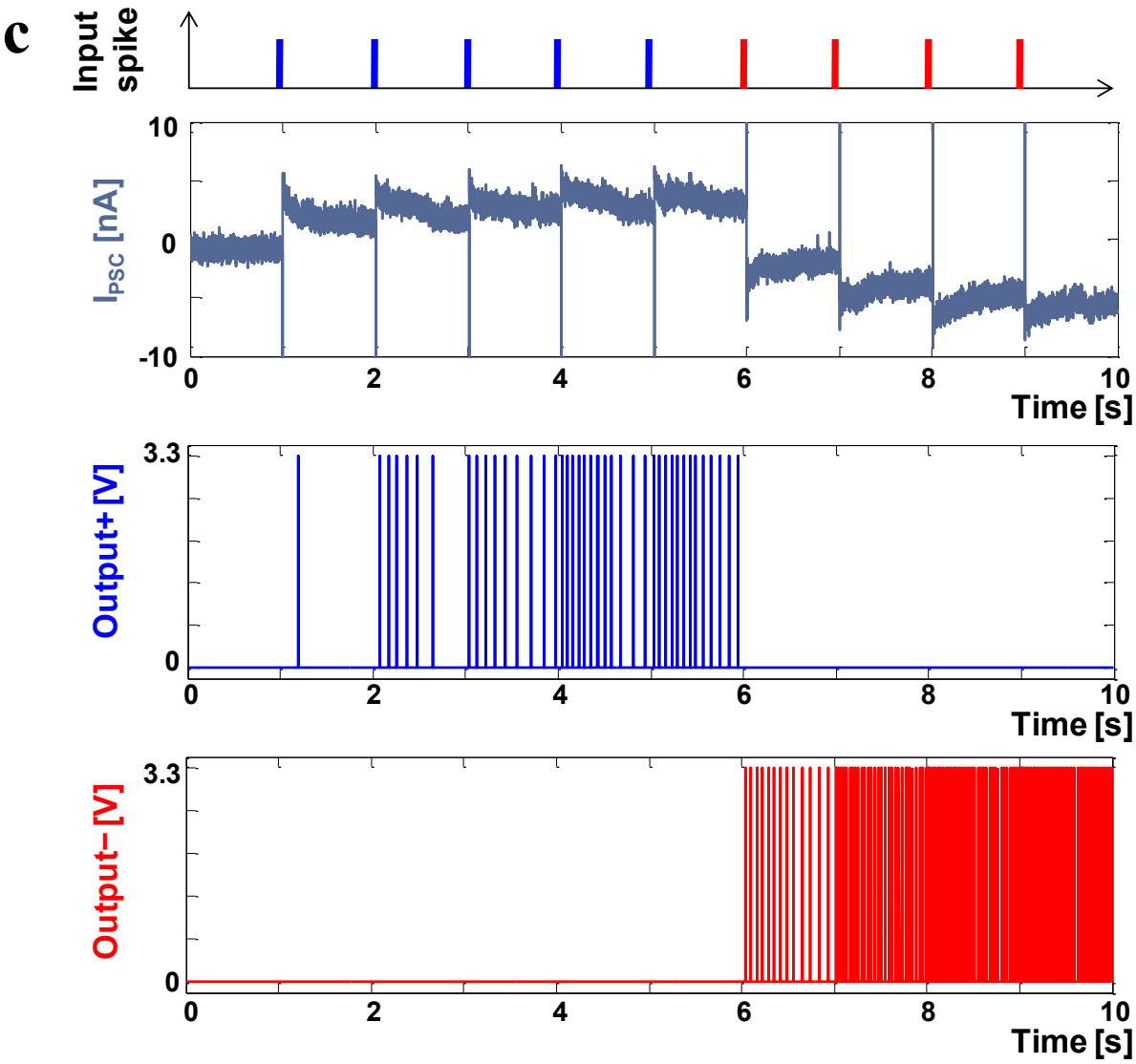
At the both I&F circuits, there is a CMOS interface circuit which can split the total post-synaptic currents into the positive portion and the negative portion and feed them to the positive and the negative I&F circuits, respectively. As the configuration of a SNC with dual columns, positive output spikes will be generated when the positive or excitatory post-synaptic current is dominating, and negative output spikes will be generated when the negative or inhibitory post-synaptic current is larger as illustrated in the right schematic of Figure 29.

3.4 Operation of Excitatory and Inhibitory Synapstors

In order to elucidate the operation of excitatory and inhibitory synapstors, the actual experiment results using two synapstor – one excitatory and one inhibitory synapstors – are shown in Figure 30. The schematic view of this experiment is shown in Figure 30a.




b
Input spike
10
0
-10
I_{PSC} [nA]
0
2
4
6
8
10
Time [s]
3.3
0
Output+ [V]
Time [s]
3.3
0
Output− [V]
Time [s]


c
Input spike
10
0
-10
I_{PSC} [nA]
0
2
4
6
8
10
Time [s]
3.3
0
Output+ [V]
Time [s]
3.3
0
Output− [V]
Time [s]

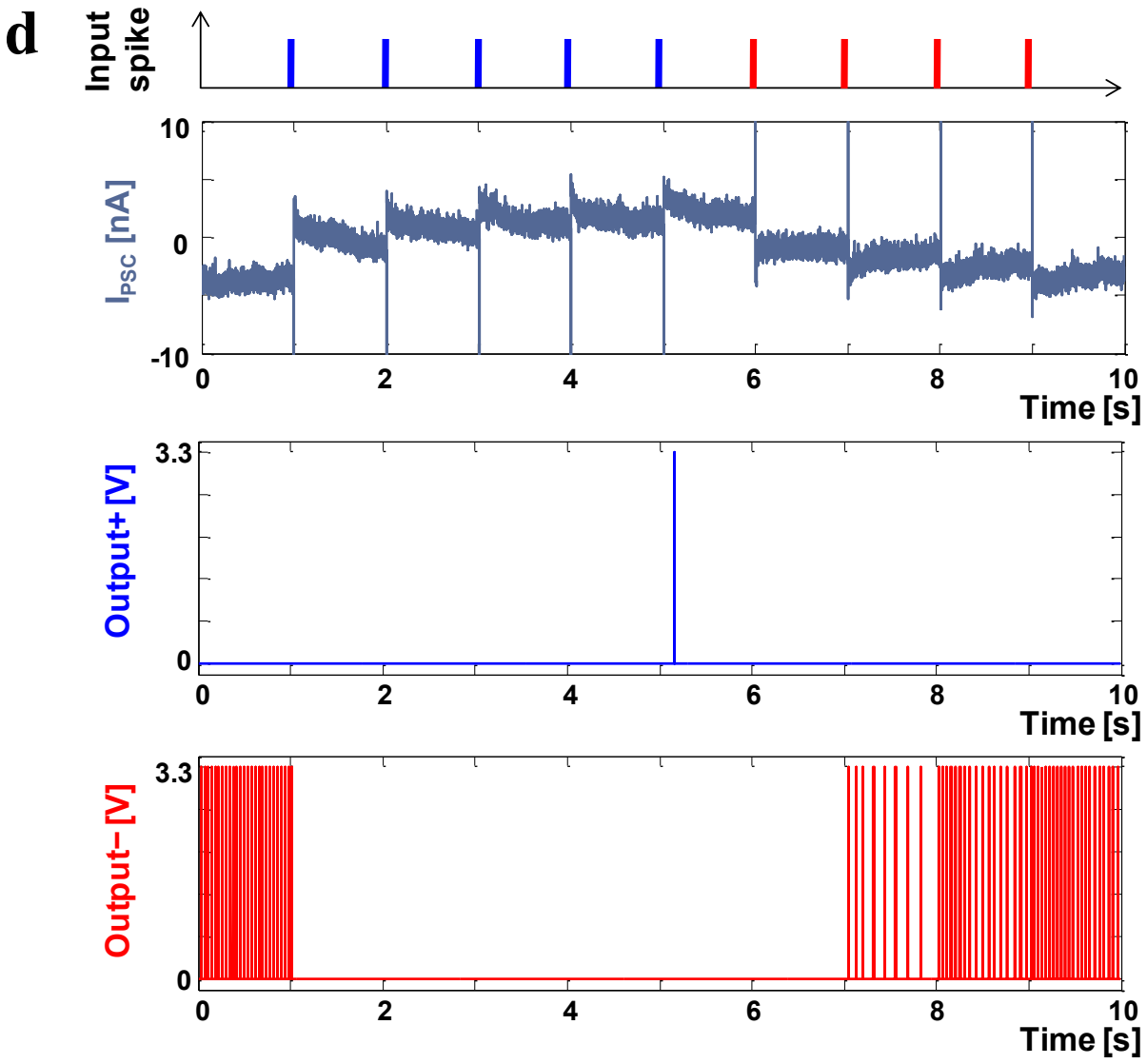


Figure 30. Experiment results of an excitatory and an inhibitory synapstors **a.** A Schematic overview of experiments **b.** I_{PSC} from a set of input spikes on both synapstors, the positive and the negative output spikes are shown before the tuning of synaptic weights. **c-d.** As synaptic weights are tuned, different correlations between input and output spikes can be generated.

The accumulated post-synaptic current (I_{PSC}) was plotted with positive and the negative output spikes in Figure 30b. On a top plot of Figure 30b, input spikes applied on an excitatory synapstor were plotted in blue lines while input spikes on an inhibitory synapstor were plotted in red lines. For experiments of Figure 30b to 30d, the same set of input spikes was applied on the same pair of synapstors, 5 input spikes on an excitatory synapstor and then 4 input spikes on an inhibitory synapstor were applied at every 1 second. As more input spikes applied on an excitatory synapstor, I_{PSC} was sequentially increased by accumulated post-synaptic currents. And positive output spikes started being generated while negative output spikes stopped being generated. In Figure 30b, less positive output spikes were generated than negative output spikes for a given set of input spikes because of the smaller synaptic weight of an excitatory synapstor than one of an inhibitory synapstor. After increasing both synaptic weights (Figure 30c), there were more positive and negative output spikes triggered. After decreasing the excitatory synaptic weight, there was only one positive output spike generated from the given set of input spikes. As clearly seen in Figure 30, a SNC with two columns of synapstors can trigger both excitatory and inhibitory post-synaptic currents, establish the complex spatiotemporal correlation between input spikes and output spikes, and adjust its spatiotemporal correlation by tuning the synaptic weights.

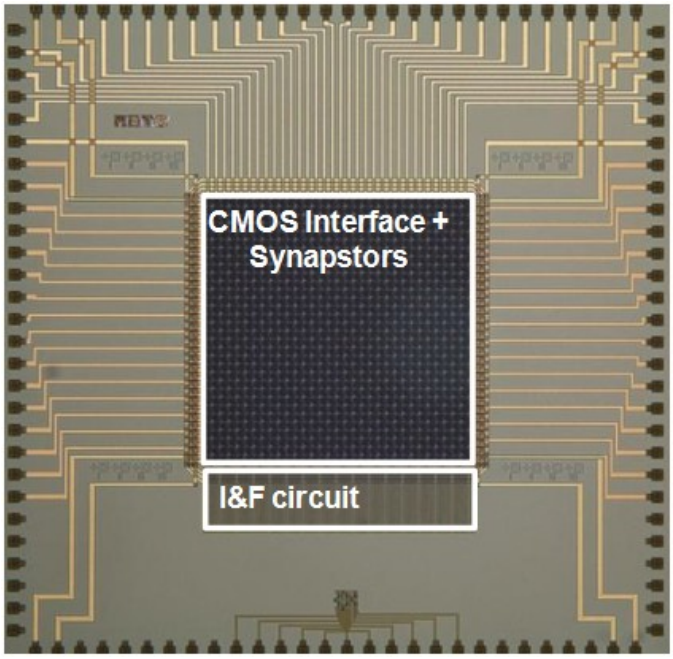
3.5 Large-Scale Spike Neuromorphic Circuit

3.5.1 Design and Fabrication

The large-scale spike neuromorphic circuit was designed and fabricated based on the structures explained in previous sections. The large-scale spike neuromorphic circuit has 16384 CNT synapstors, CMOS interface circuits for CNT synapstors, and 16 I&F soma circuits. The ratio of synapses per neuron, a number of synapstors per I&F soma circuit, is 1024, similar level with biological neurons. The fabricated chip image is shown in Figure 31a. In the center area, there is an array of static random-access memory (SRAM) like CMOS interface circuit to realize the parallel dynamic interface between a FPGA and CNT synapstors as illustrated in Figure 31b. On top of the CMOS interface circuit, CNT synapstors were integrated utilizing a post-CMOS process. There are 16 I&F soma circuits below the array of synapstors. The CMOS interface circuit and I&F circuit were design and fabricated using MOSIS TSMC 0.35 μm process with the size of 5 mm by 5 mm. CNT synapstors were fabricated between micron scale electrodes (source, drain, and gate electrodes for CNT synapstors) defined by the top metal layer (Al) where the over-glass etching was conducted at the foundry readily exposed the top metal layer. After the fabrication of CMOS chips, a reactive-ion etching (RIE) process was performed to remove the residue on top of the source, drain and gate electrodes for CNT synapstors. To provide good electrical contacts between electrodes and CNT synapstors, a thin Al_2O_3 layer, which was naturally formed, was removed by wet etching process and immediately and electroless zincation plating process was performed. Electroless zincation plating process started with immersed the chip into 1 M sodium hydroxide solution for 1 minute following by DI water rinsing and

nitrogen dry. Then, immerse the chip in zinc plating solution (zinc oxide 0.2 g/L, sodium nitrate 0.025 g/L, potassium sodium tartrate tetrahydrate 0.6 g/L, ion chloride 0.015 g/L and sodium hydroxide 40 g/L) at 40 °C for 2 minutes. The electroless plating process is a low cost deposition method which does not require an additional lithography steps and prevented the underlying aluminum from getting re-oxidized and reduced the contact resistance between CNTs and the Al electrodes. After electroless plating process, the same CNT synapstor fabrication process was performed on top of defined electrodes in the following sequence: CNT spin-coating and CNT channel definition, deposition of a PI layer, deposition of a PI:PCBM layer, patterning and etching of both PI layers, deposition and patterning of an Al_2O_3 layer, and fabrication of top gate electrodes. The image of part of fabricated CNT synapstors is shown in Figure 31c.

a



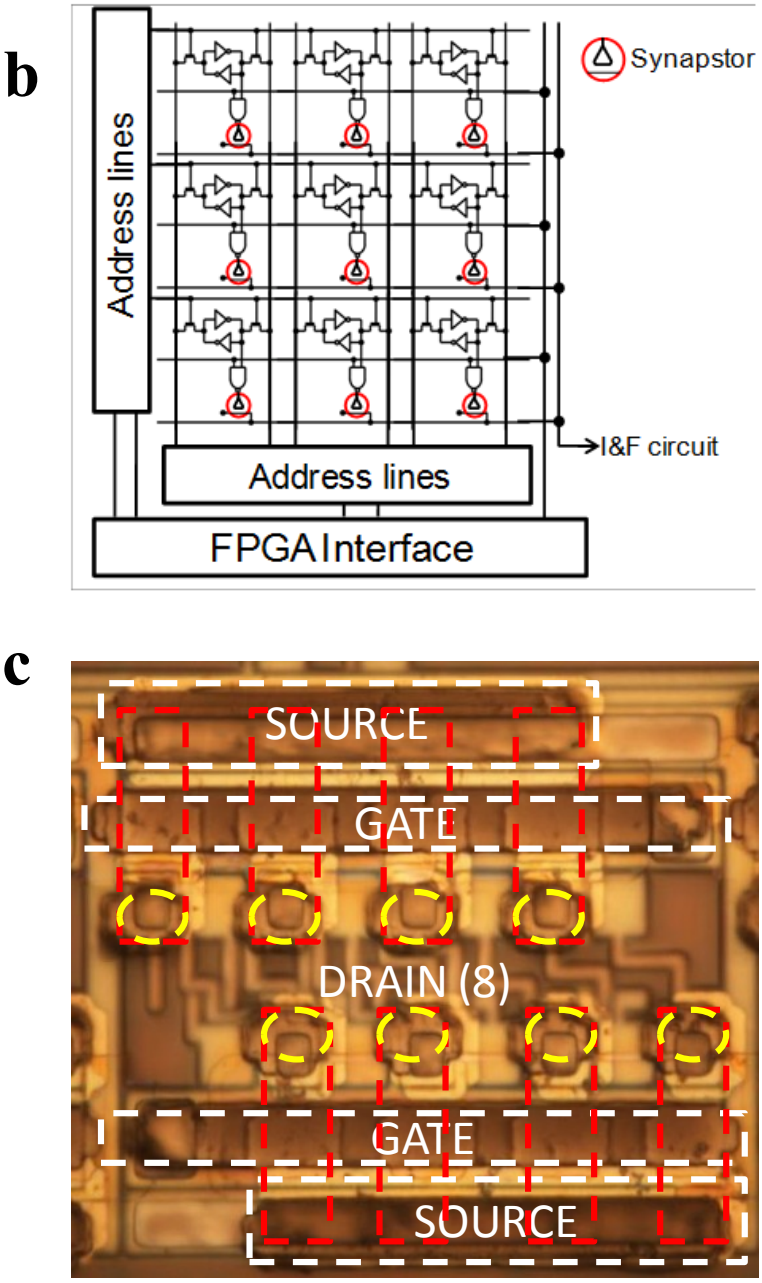


Figure 31. A large-scale spike neuromorphic circuit **a.** A full chip image of a large-scale spike neuromorphic circuit **b.** A schematic of CMOS interface circuit **c.** Image of one cell containing 8 synapstors.

3.5.2 Power Consumption in a Large-Scale Spike Neuromorphic Circuit

Power consumption is one of crucial properties for neuromorphic applications. The power consumption of a large-scale spike neuromorphic circuit was measured and estimated. First of all, the average power consumption in one CNT synapstor is about 100 nW at the input spike rate of 10 Hz (2.6 nW at the input spike rate of 1 Hz). Second, the average power consumption of one I&F soma circuit is about 10 μW at output spike rate around 100 Hz. It is slightly varying depending on the input current level to an I&F circuit. The average power consumption of 10 μW was calculated by considering the number of synapstors per I&F soma circuit and their average current. Therefore, the total power consumption of a large-scale spike neuromorphic circuit without the interface circuit can be estimated by the following equation.

$$P = 100\ \text{nW} \times N_{\text{Synapstor}} + 10\ \mu\text{W} \times N_{I\&F}$$

The total estimated power consumption in a large-scale spike neuromorphic circuit is 1.8 mW for 16384 synapstors and 16 I&F soma circuits.

4. Dynamic Interaction and Learning of a SNC

4.1 Overview

The Spike Neuromorphic Circuit based on CNT synapstors has interesting capabilities as described in a previous chapter. First, it can establish the dynamic interactions with the environment in real time. Whenever there is a set of input spikes, the output spikes will be generated as seen in Figure 32. If there are proper sensors and actuators interfacing between a SNC and the environment, the dynamic interactions in real time can be performed by a SNC easily. Second, it can learn to improve the preset performance function by modifying the SNC's transfer function from input spikes to output spikes. This is mainly originated from the synaptic plasticity of CNT synapstors. To demonstrate dynamic interaction and learning capability of a SNC, a toy drone (Parrot AR.Drone 2.0) was selected as a platform. The overall schematic view of the demonstration is seen in Figure 32.

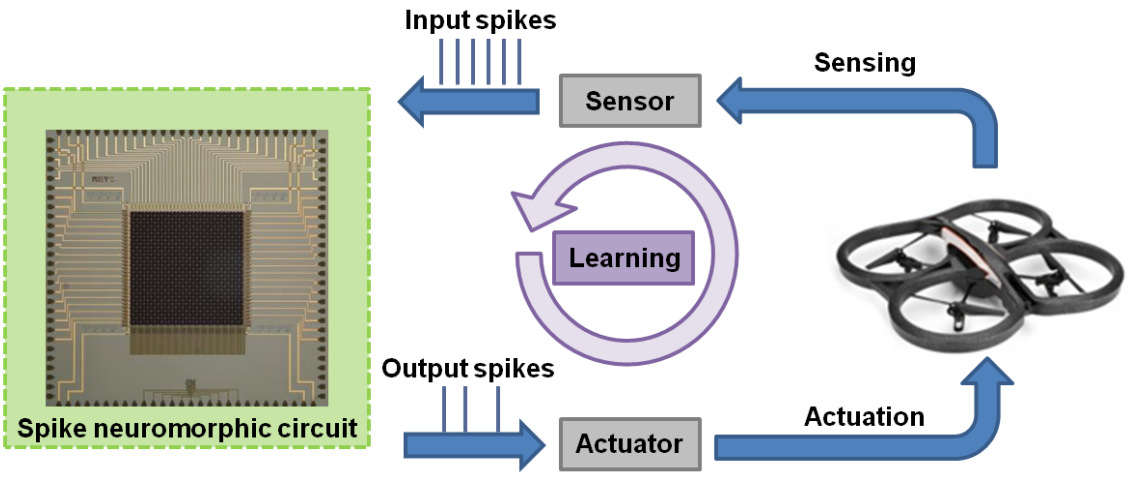


Figure 32. The overview of the demonstration of a SNC.

4.2 Experiment Set-up

The detail set-up of the demonstration will be explained and discussed in the following sections. The main idea of this demonstration is to let a SNC to interact with the environment (a drone) in real time and modify itself to improve the given performance function by learning. More precisely, there will target lights in front of a drone, and a SNC needs to learn to interact with the drone so that it can point at the target lights without any given pre-knowledge about the drone and itself. As illustrated in Figure 32, the detail information will be explained in the following order – from sensing, processing in a SNC, actuation, performance, and learning.

4.2.1 Sensing Signals from a Drone

The wide-angle lens and a camera were attached at a drone so that it can see things in front. In front of the drone, the target lights with blue lights were present and swung at every 15 seconds. The images were taken from a camera at every 50 ms and were then processed in an interface program composed by Visual Studio. The interface program filtered images, calculated the position of the target lights in images, and converted it to input spikes. Sensing signals are the information about the relative position of the target lights in the images with respect to the center line of the taken images. There are two sensing signals – X_L and X_R as illustrated in Figure 33. When the position of the target lights can be changed by either the movements of the lights or a drone, then input spikes are generated correspondingly to the relative position of the lights. As seen in Figure 33a, if the lights are moved to the left with respect to a drone, then, there will be input spikes on X_L input channel with the frequency proportional to the position.

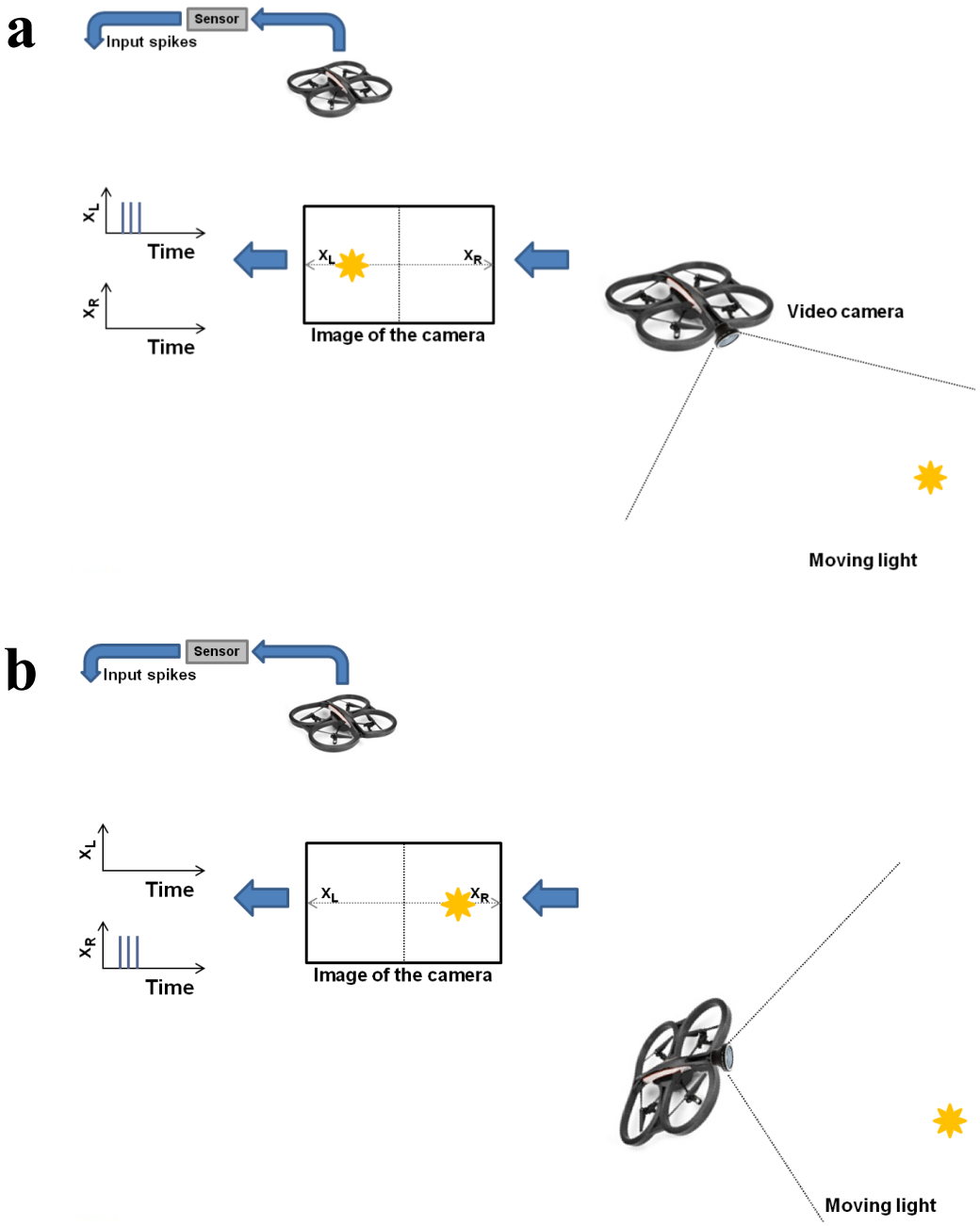


Figure 33. Sensing signals (X_L and X_R) from a drone **a.** An illustration of X_L input spikes being generated when the target lights (yellow) are in the left plane of the image by lights moving. **b.** An illustration of X_R input spikes being generated by a drone's movement.

In Figure 33b, there are input spikes on a X_R input channel because a drone is rotated to the left, causing the lights are located in the right plane of the taken image from the center line. The input spike frequency is proportional to the position of the lights.

4.2.2 Processing Signals in a SNC

When there are input spikes on input channels, which carry the information about the relative position of the target lights, they will directly go to a SNC and trigger the output spikes based on synaptic weights of a SNC. In this experiment, four CNT synapstors, two excitatory and two inhibitory CNT synapstors, were selected. Each pair of an excitatory and inhibitory synapstors has the same input spikes – X_L and X_R. Therefore, if the synaptic weights of both synapstors are the same, then, there will be no accumulated post-synaptic current (I_{PSC}) at I&F soma circuits. If one of synaptic weights is stronger than the other one, then one type of output spikes can be generated from that pair of synapstors. Therefore, a SNC should learn to modify one of the synaptic weights either increasing or decreasing in order to control a drone so that it can finally improve the performance function. The details about the learning will be discussed in the following sections. The schematic overview of processing in a SNC is illustrated in Figure 34. When input spikes are generated and fed to a SNC, CNT synapstors having input spikes will produce the post-synaptic currents. All triggered post-synaptic currents are then accumulated at I&F soma circuits and will trigger the corresponding output spikes. For instance, if I_{PSC} is positive, then positive output spikes will be generated and vice versa.

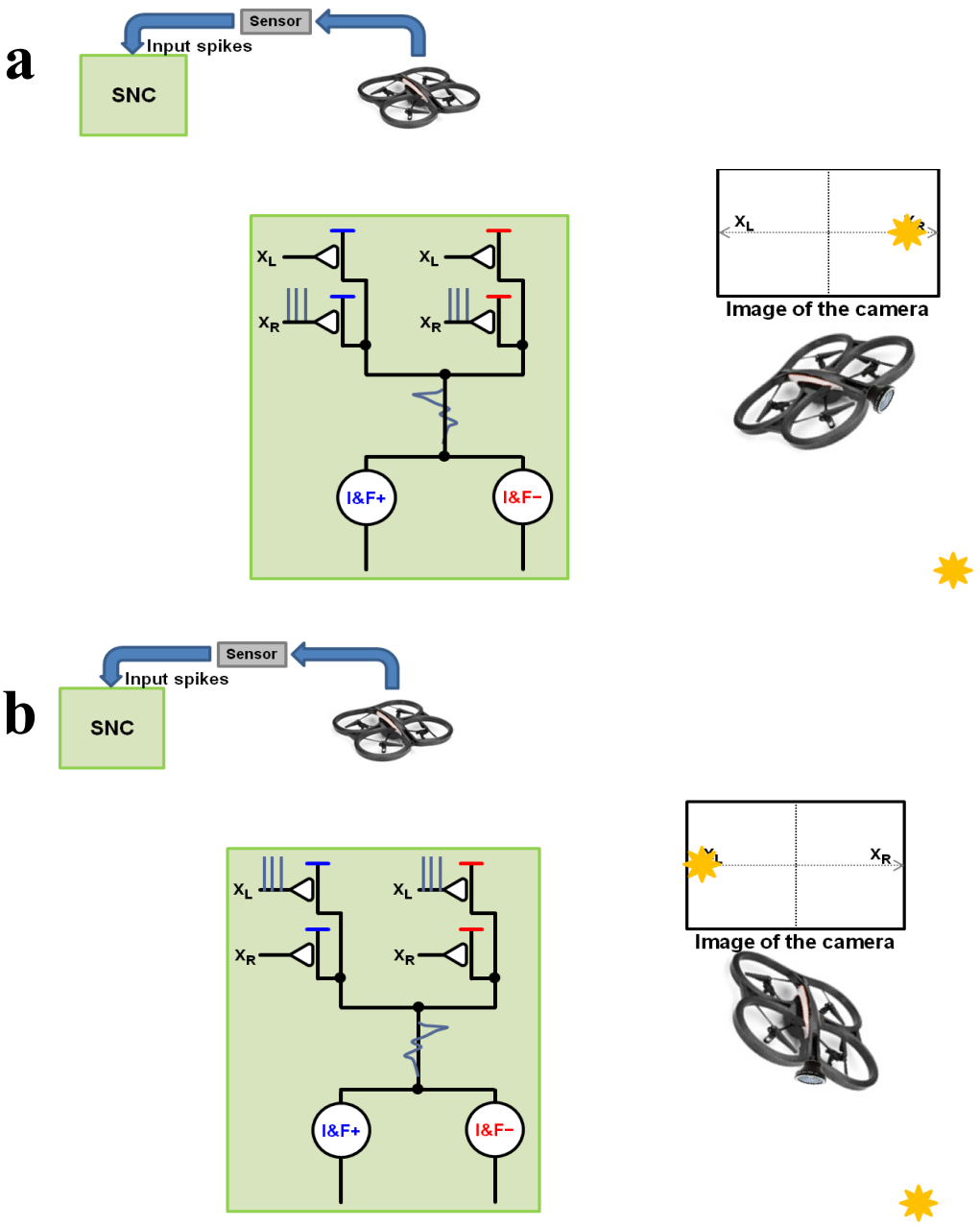


Figure 34. Processing in a SNC **a.** An illustration of X_R input spikes triggering the post-synaptic currents and the accumulated post-synaptic current. **b.** An illustration of X_L input spikes triggering the post-synaptic currents and the accumulated post-synaptic current.

4.2.3 Actuations Signals from a SNC

There are 4 possible actuations on a drone – up and down (altitude actuation), left and right (translational actuation), forward and backward, and rotation left and right. In this experiment, only rotation actuations were selected for a SNC to control. The positive output spike was assigned to rotation left (a_L), and the negative output spike was assigned to rotation right (a_R) as illustrated in Figure35. If there are positive output spikes from a SNC, 1) their rate is sensed by a FPGA board, 2) the interface program converts it to series of actuation commands to a drone, and 3) the converted commands are sent to a drone through the wireless communication. For instance, if the relative position of the target lights in the left plane of the image, then sensing program will generate input spikes to a X_L input channel with corresponding frequency as seen in Figure 35a. Assuming they can trigger the positive output spikes as seen in Figure 35a, and then triggered positive output spikes are sampled by a FPGA board, the rate of output spikes is converted to a series of actuation commands, and then converted commands are sent to a drone. As a result (Figure 35b), a drone will rotate to the left and change the relative position of the target lights in the image. Therefore, also input spikes will be diminished as the relative position is aligned to the center line of the image as seen in Figure 35b. However, this is the case with well modified synaptic weights. For instance, if X_L input spikes trigger the negative output spikes, then a drone will rotate to the right and the relative position of the target lights will be deviated more from the center line. Therefore, it is crucial for a SNC to modify the synaptic weights in the right direction through a learning process, which will be discussed in the following.

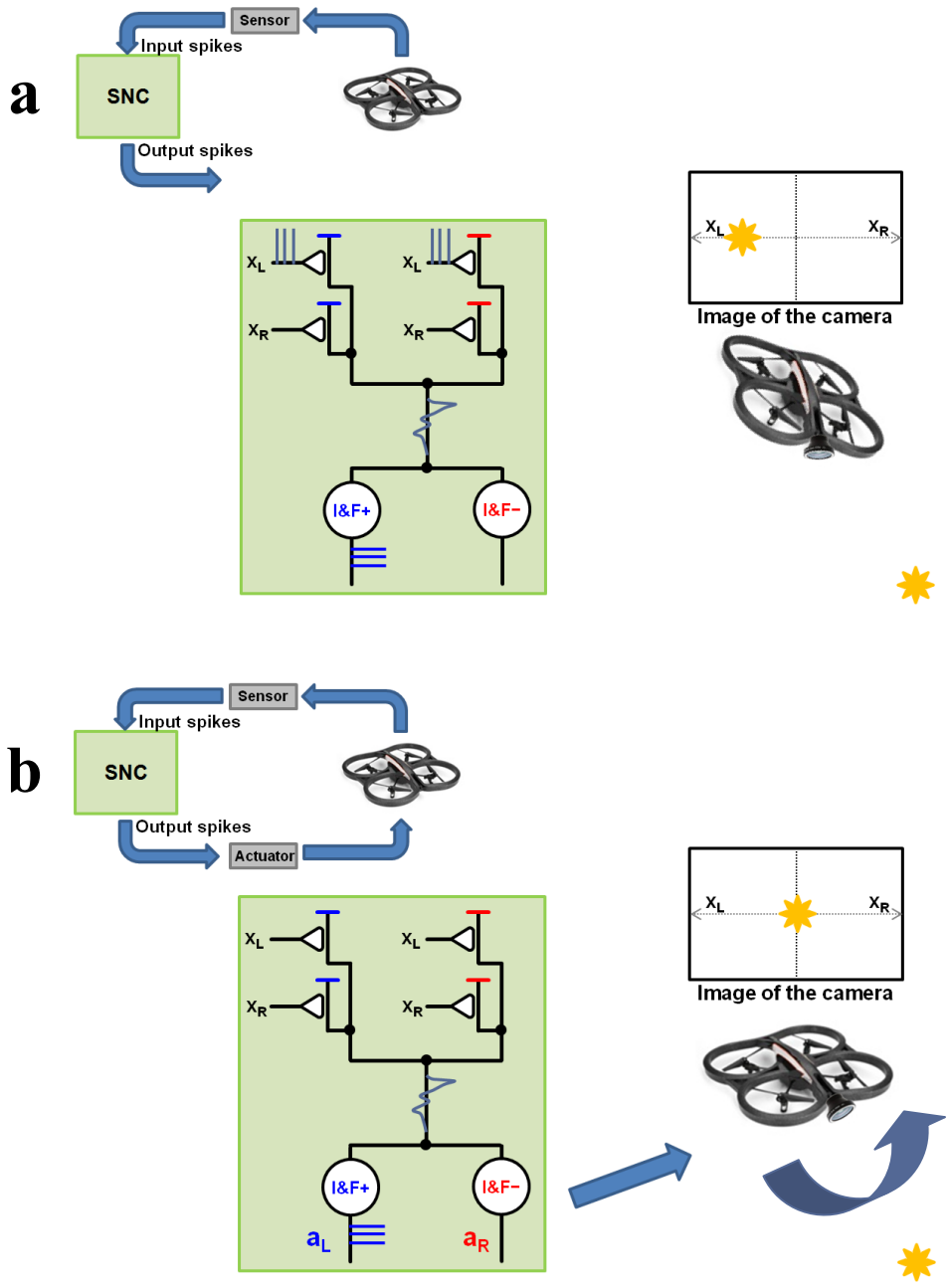


Figure 35. Actuation by a SNC **a.** An illustration of positive output spikes triggered by X_L input spikes **b.** As positive output spikes assigned to rotation left (a_L), a drone will rotate to the left, resulting in change of input spikes.

4.2.4 Performance Function of a SNC

Before the learning process is discussed, it should be explained about the performance function of a SNC. During the experiment, the performance function is measured as a following equation.

$$P = -\int_0^T x^2(\tau)d\tau$$

The performance function is the integral of square of the deviation of the target lights from the center line of the take images. In other words, the performance function is the numerical reference of how well a drone points at the target lights for given amount of time, T = 10 seconds. In this experiment, a SNC interacts with a drone for 10 seconds, and then there is a learning process for 2 seconds. The interaction and learning periods are then repeated until the end of the experiments. In other words, the learning process is performed every 10 seconds within 2 seconds.

4.2.5 Modeling and Learning in a SNC

The learning performed in this experiment will be explained in this section. The closed-loop of a SNC and a drone can be simply modeled as illustrated in Figure 36. The actuation signals, a(t), are output spikes from a SNC triggered by input spikes and CNT synapstors. There is also unexpected noise term in the actuation signals to a drone, $a_0(t)$, which is originated by coupling with other actuation signals, drift, and air turbulence. The sensing signals, x(t), are the relative position of the target lights in the image and sensed from a drone and an interface

program. Also, in the sensing signal, there is a noise term, $x_0(t)$, which is the change in the sensing signals by other actuations, drift of a drone, or the air turbulence. Let's assume that h(t) is the transfer function of synapstors which can be adjusted by learning process, and g(t) is the transfer function of a drone, which is time-invariant function.

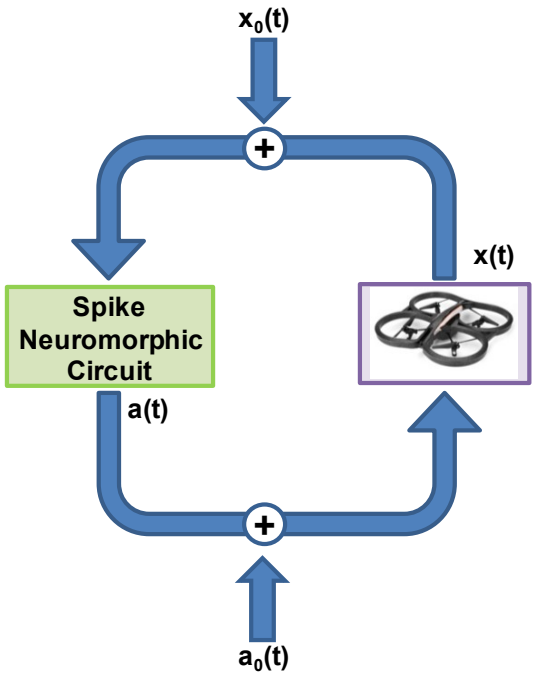


Figure 36. Modeling of dynamic interaction and learning of a SNC.

The operation of the closed-loop interactions can be described in the following equations based on the definitions aforementioned.

$$x(t) = x_0(t) + \int_0^T g(t-\tau)a(\tau)d\tau \,,\; a(t) = a_0(t) + \int_0^T h(t-\tau)x(\tau)d\tau$$

To simplify the problem, the average of sensing and actuation signals can be taken as well as linear assumption. Then, two modeling equations can be simplified as a following equation.

$$x(t) \approx x_0(t) + T^2 \bar{g} \bar{h} \bar{x}$$

The goal of a SNC is to maximize the given performance function by the learning process. In other words, a SNC needs to improve the performance function by modifying the synaptic weights and change the correlation between input and output spikes. Therefore, the change in the performance function by the change of h(t) should be positive to improve the performance function by the learning process.

$$\frac{\partial P}{\partial h} \approx -T^2 \bar{g} \bar{x} \;\rightarrow\; \Delta P = -T^2 \bar{g} \bar{x} \Delta h > 0$$

Therefore, if Δh is satisfying above equation, then, the performance function will be improved gradually. Δh used in this experiment is described in the next equation:

$$\Delta h = -\varepsilon \frac{(\Delta x)^2}{\bar{g}} \approx \varepsilon (x_N - x_0) \sum_{i=0}^{N} a_i, \;\; \epsilon > 0$$

Simply, the given learning rule is to reward (increase) the synaptic weight which has more correlation and to punish (decrease) the synaptic weight which has less correlation between sensing signals and actuation signals in a way to improve the performance function.

4.3 Experiment Results without Learning

In order to see the necessity of the learning, two different experiments were performed – first experiment without the learning process, and second experiment with the learning process. The experiment results without the learning are plotted in Figure 37. The sensing signal measured by a drone is plotted as a function of time in Figure 37a and the actuation signal from a SNC is plotted as a function of time in Figure 37b. The performance function calculated at every 10 seconds is also plotted versus time in Figure 37c. As clearly seen in Figure 37, the actuation signal kept oscillating from rotation left and right with a significant delay (~ 5 seconds). Also, when a drone pointed at the target lights by rotation left actuation (a_L), then rotation right actuation (a_R) was triggered from a SNC, resulting in huge deviation of a drone from the target lights. This is mainly caused by the unbalanced synaptic weights of four CNT synapstors. Since there is no learning process to modify them, a SNC kept doing the same operations until the end of the experiment. As more accumulation of wrong actuations, the drone was deviated from the target lights, thus resulting that the performance function at the end of the experiment was decreasing close to −300. This implies that even the oscillating actuation with a certain delay can cause huge decrease in the performance function. Therefore, it is obvious that the learning process is necessary for a SNC to improve the drone's performance function – let a drone point at the target lights under the circumstance of swinging lights and disturbance by coupled actuations, drift, and air turbulence. In the following section, it will be shown how well the learning process can improve the performance function.

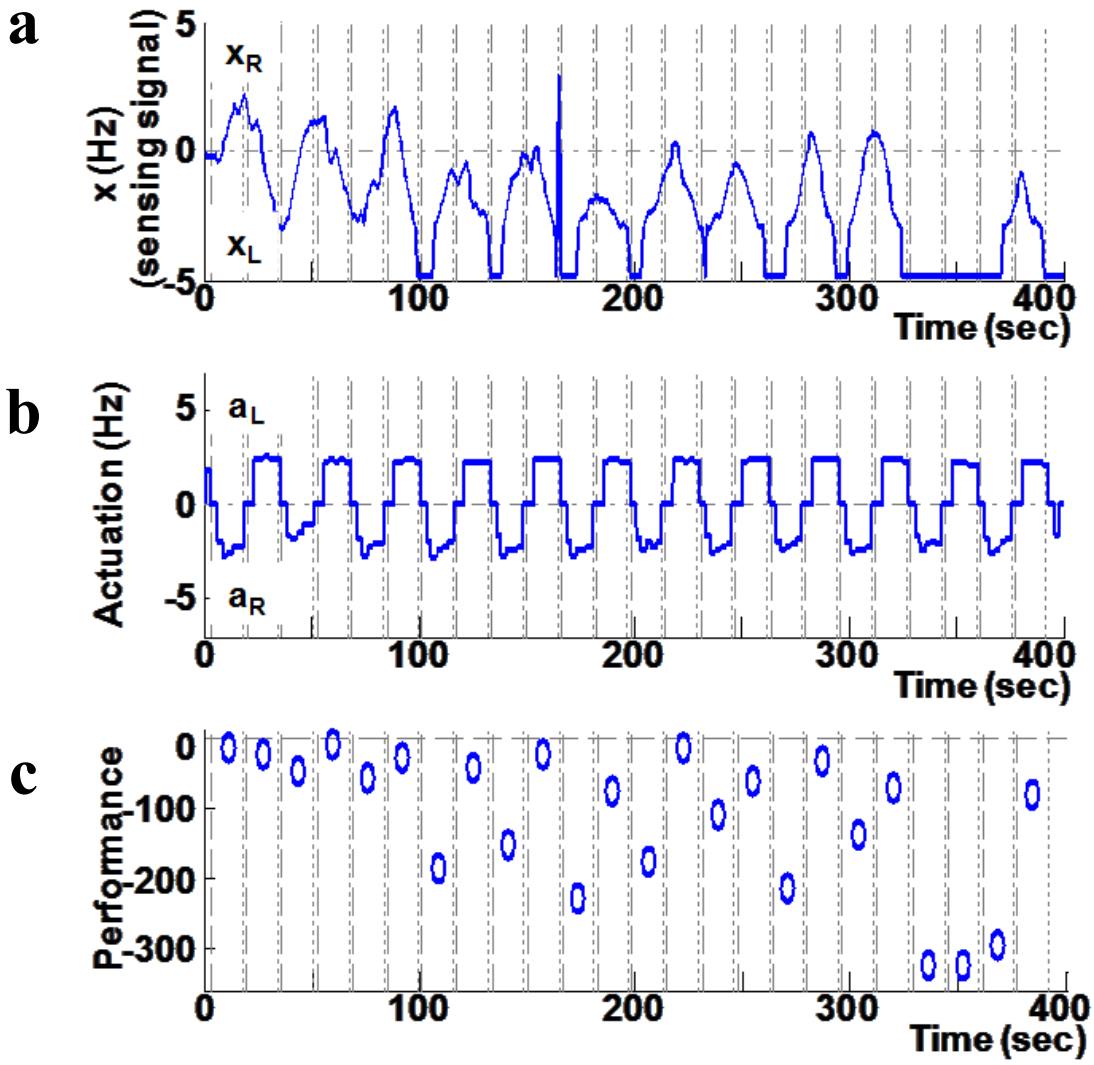


Figure 37. Experiment results without learning **a.** Sensing signals from a drone versus time. **b.** Actuation signals from a SNC versus time **c.** Performance function at every 10 seconds.

4.4 Experiment Results with Learning

The experiment with the learning process was also performed and the results are plotted in Figure 38. The sensing signal measured by a drone is plotted as a function of time in Figure 38a and the actuation signal from a SNC is plotted as a function of time in Figure 38b. The performance function calculated at every 10 seconds is also plotted versus time in Figure 38c. The learning spikes applied on synapstors are also plotted versus time in Figure 38d. Blue dots mean the number of learning spikes on CNT synapstors having X_L input channel, and red dots mean the number of learning spikes on CNT synapstors having X_R input channel. The numbers of learning spikes was determined by the equation $\Delta h = 0.03\,(x_N - x_0)\sum_{i=0}^{N} a_i$ and the frequency of learning spikes was 500 Hz, which is much higher than the frequency of input spikes (0 ~ 3 Hz). As clearly seen in Figure 37c, the performance function was gradually improved as time goes. This is mainly because the actuation signals triggered by synapstors are balanced. As a comparison between without and with learning, Figure 37c and Figure 38c can be compared. When the performance function was about −200 ~ −300 in the experiment without learning, the performance function was in the range of −20 ~ −30 in the experiment with learning in a SNC. Therefore, it is clearly shown that a SNC can improve the given performance function through a learning process by changing the synaptic weights of CNT synapstors. In summary, it is demonstrated that 1) a SNC can dynamically process sensing signals from the drone and trigger the actuation signals for the drone in real-time, 2) the performance of the drone can be improved by the learning process in a SNC.

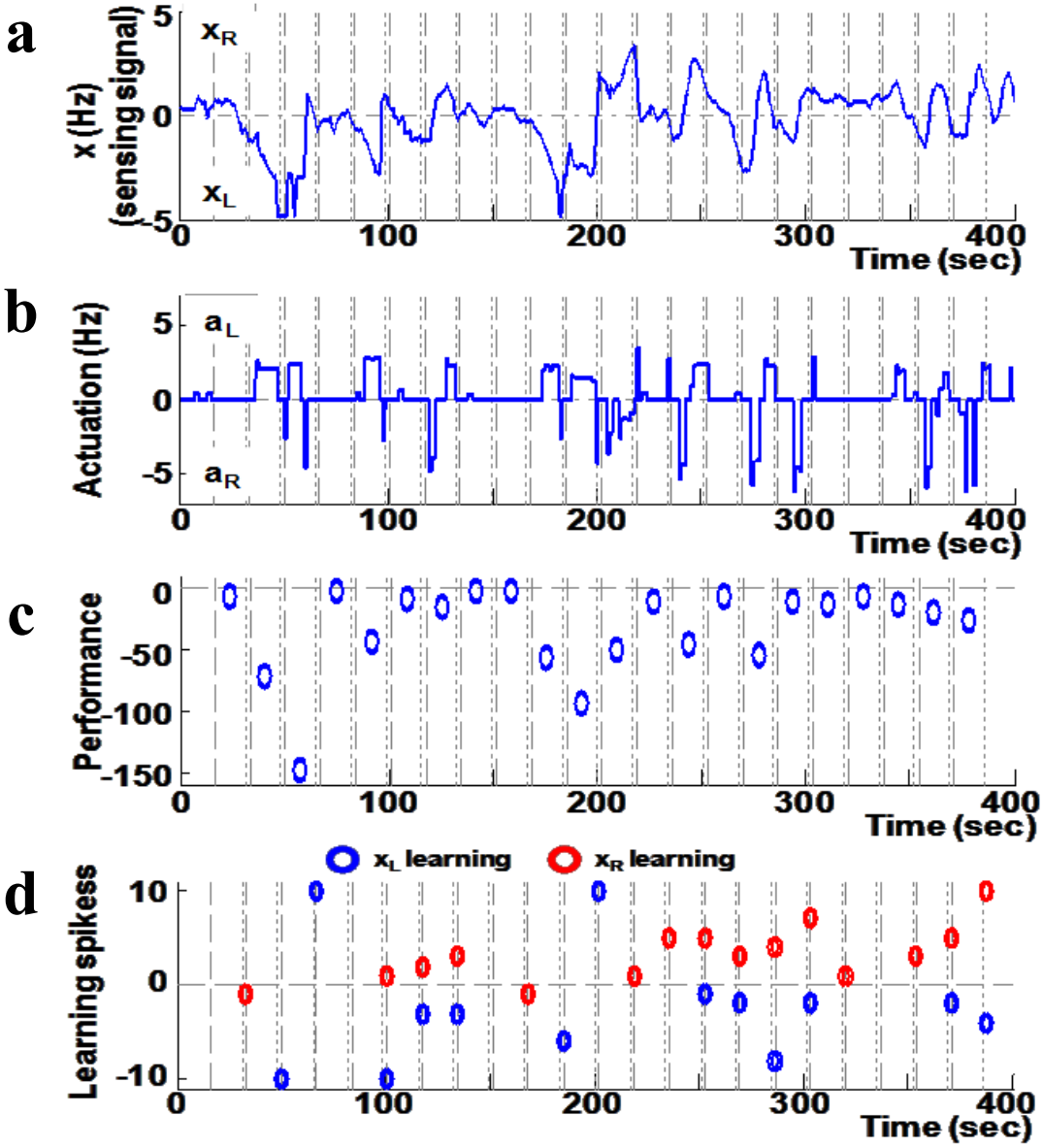


Figure 38. Experiment results with learning **a.** Sensing signals from a drone versus time. **b.** Actuation signals from a SNC versus time **c.** Performance function at every 10 seconds. **d.** The learning spikes applied on synapstors. Blue dots representing learning spikes on synapstors having X_L input channel, and red dots representing learning spikes on synapstors having X_R input channel.

4.5 Comparison of a SNC with Prior Art

As demonstrated in previous sections, a SNC based on CNT synapstors has capabilities of dynamic interactions with the environment and learning in real-time. Two representative works using other device type are chosen and compared with a SNC in Table 4. For a neuromorphic circuit based on analog CMOS design[59], it can emulate the elementary functions of biological synapses and parallel processing using peripheral Input/Output (I/O) circuit with 32 neurons and 4096 synapses. However, the numbers of neurons and synapses is limited due to the numbers of transistors required. Though the power consumption for whole chip operation is unavailable in the reference, there will be substantial the power consumption in analog CMOS design. Second reference is a neuromorphic circuit based on resistive switch devices. There was no neuron-type of circuit but only an array of 1,600 resistive switch devices. Also, the power consumption for whole chip operation is unavailable in this reference but the power consumption in one device is roughly around μW. Therefore, the power consumption will be also considerable and there will be weak spatiotemporal correlation due to the nature of resistive type devices.

Device	Number of Neurons	Number of Synapses	Synapses per neuron	Power consumption
CNT synapstors	16	16,384	1,024	1.8 mW
Analog CMOS[59]	32	4,096	4	N/A
Resistive switches[60]	N/A	1,600	N/A	N/A

Table 4. Comparison of neuromorphic circuit implementation.

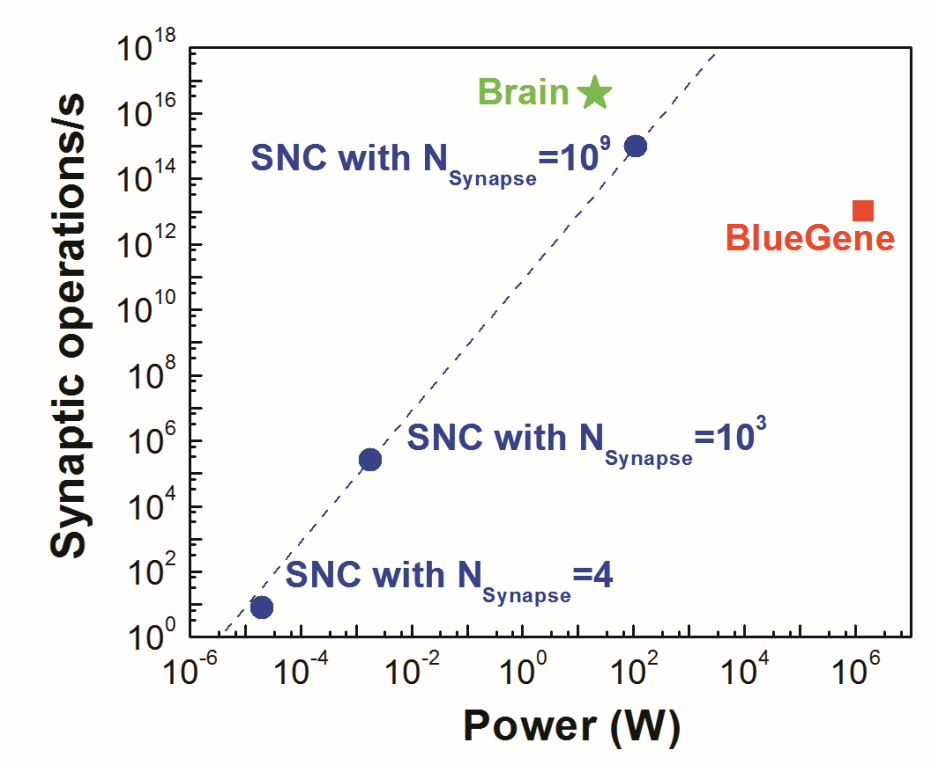


Figure 39. Estimation performance (speed) of SNCs with different numbers of synapstors against power – in comparison with the brain and supercomputer (Blue Gene).

In Figure 39, the estimated performance of SNCs with different numbers of synapses (synapstors) is plotted in the speed of synaptic operation and the power consumption space in blue dots and a blue dotted line. Blue dots were the measured performance and the blue dotted line is the estimation made by an extrapolation. The performance of the brain and the supercomputer simulation[13] was also plotted for comparison as a green star and a red square. As seen in Figure 39, SNC has a potential to have higher signal processing speed and be more efficient in power consumption than a supercomputer when the dimension of parallel signal processing exceeds ~10^9.

5. Conclusions

The brain, essentially a biological neural network, has advantages over supercomputers in power consumption, parallel processing, spatiotemporal correlation, learning, and intelligence. The neural network is composed of synapses – the fundamental component. In order to emulate a neural network by a circuit, it is crucial to realize the device which can emulate the elementary functions of synapses. Carbon nanotube (CNT) based transistors, CNT synapstors, were designed, fabricated, and tested to emulate the essential functions of the synapses. The CNT synapstors can generate post-synaptic current, process spike signals in a spatiotemporal mode, and have the memory and learning functions with low power consumption (250 pW for CNT/PEG synapstors and 2.6 nW for CNT/C60 synapstors).

A spike neuromorphic circuit (SNC) based on CNT synapstors was designed, fabricated, and tested. A SNC has the capability of parallel signal processing and spatiotemporal correlation between input spikes and output spikes. The spatiotemporal correlation can be established by utilizing the synaptic plasticity of CNT synapstors. A large-scale spike neuromorphic circuit was designed and fabricated with 16,384 synapstors and 16 Integrate-and-Fire (I&F) soma circuits. The average power consumption for a large-scale spike neuromorphic circuit is 1.8 mW.

To demonstrate the function of the SNC, a toy drone was used as a platform. A SNC formed a dynamic closed-loop interaction with the drone, and the SNC dynamically processed signals from the drone and triggered the actuation signals for the drone in real-time. The performance of the drone was significantly improved by the learning process in the SNC. A large-scale SNC can successfully emulate the massively parallel signal processing and learning

functions of a biological neural network and be potentially used for applications for speech recognition, pattern recognition, statistic inference, and other intelligent behaviors.

REFERENCES

1 Bohr, M. The new era of scaling in an SoC world. in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International.* 23-28.

2 TheGreen500.org. *The Green500 List - November 2012*, Available at: <http://www.green500.org/lists/green201211> (2012).[Accessed May 19, 2013]

3 Larry Greenemeier, S. A. *Computers have a lot to learn from the human brain, engineers say*, Available at: <http://www.scientificamerican.com/blog/post.cfm?id=computers-have-a-lot-to-learn-from-2009-03-10> (2009).[Accessed May 19, 2013]

4 Top500Supercomputersites. *TOP 10 Sites for November 2012*, Available at: <http://www.top500.org/lists/2012/11/> (2012).[Accessed May 19, 2013]

5 Anandtech. *Inside the Titan supercomputer*, Available at: <] http://www.anandtech.com/show/6421/inside-the-titan-supercomputer-299k-amd-x86-cores-and-186k-nvidia-gpu-cores> (2012).[Accessed May 19, 2013]

6 Scheff, S. W., DeKosky, S. T. & Price, D. A. Quantitative assessment of cortical synaptic density in Alzheimer's disease. *Neurobiol. Aging* **11**, 29-37, (1990).

7 Drachman, D. A. Do we have brain to spare? *Neurology* **64**, 2004-2005, (2005).

8 Llinas, R., Sugimori, M. & Simon, S. M. Transmission by presynaptic spike-like depolarization in the squid giant synapse. *Proc. Natl. Acad. Sci. USA* **79**, 2415-2419, (1982).

9 Blankenship, J. E., Wachtel, H. & Kandel, E. R. Ionic mechanisms of excitatory, inhibitory, and dual synaptic actions mediated by an identified interneuron in abdominal ganglion of Aplysia. *J. Neurophysiol.* **34**, 76-92, (1971).

10 Abbott, L. F. & Nelson, S. B. Synaptic plasticity: taming the beast. *Nat. Neurosci.* **3**, 1178-1183, (2000).

11 Bi, G. & Poo, M. Synaptic modification by correlated activity: Hebb's postulate revisited. *Annu. Rev. of Neurosci.* **24**, 139-166, (2001).

12 Cooke, S. F. & Bliss, T. V. Plasticity in the human central nervous system. *Brain* **129**, 1659-1673, (2006).

13 Ananthanarayanan, R., Esser, S. K., Simon, H. D. & Modha, D. S. The cat is out of the bag: cortical simulations with 109 neurons, 1013 synapses. in *High Performance Computing Networking, Storage and Analysis, Proceedings of the Conference on.* 1-12.

14 Schaller, R. R. Moore's law: past, present, and future. *IEEE Spectrum* **34**, 52-59, (1997).

15 Satish, D., Varghese, G., Sanjeev, J., Tanveer, K., Milstrey, R., Sanjib, S., Siers, S., Stolero, I. & Arun, S. A 22nm IA multi-CPU and GPU system-on-Chip. in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International.* 56-57.

16 Intel. *Intel Core i7-3770 Processor specifications*, Available at: <http://ark.intel.com/products/65719> (2012).[Accessed May 19, 2013]

17 Wikipedia. *Ivy Bridge (microarchitecture)*, Available at: <http://en.wikipedia.org/wiki/Ivy_Bridge_(microarchitecture)> (2012).[Accessed May 19, 2013]
18 Mead, C. Neuromorphic electronic systems. *Proc. IEEE* **78**, 1629-1636, (1990).
19 Mead, C. in *Analog VLSI Implementation of Neural Systems* Vol. 80 *The Kluwer International Series in Engineering and Computer Science* (eds Carver Mead & Mohammed Ismail) Ch. 10, 239-246 (Springer US, 1989).
20 Boahen, K. A. Point-to-point connectivity between neuromorphic chips using address events. *IEEE T. Circuits-II* **47**, 416-434, (2000).
21 Douglas, R., Mahowald, M. & Mead, C. Neuromorphic Analog VLSI. *Annu. Rev. Neurosci.* **18**, 255-281, (1995).
22 Arthur, J. V. & Boahen, K. A. Synchrony in silicon: the gamma rhythm. *IEEE Trans. Neural Netw.* **18**, 1815-1825, (2007).
23 Indiveri, G., Chicca, E. & Douglas, R. A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity. *IEEE Trans. Neural Netw.* **17**, 211-221, (2006).
24 Ramakrishnan, S., Hasler, P. E. & Gordon, C. Floating gate synapses with spike-time-dependent plasticity. *IEEE Trans. Biomed. Circuits Syst.* **5**, 244-252, (2011).
25 Chen, Y. J., Hall, S., McDaid, L., Buiu, O. & Kelly, P. A silicon synapse based on a charge transfer device for spiking neural network application. *Lect. Notes Comput. Sc.* **3973**, 1366-1373, (2006).
26 Yu, S. M., Wu, Y., Jeyasingh, R., Kuzum, D. G. & Wong, H. S. P. An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation. *IEEE Trans. Electron Devices* **58**, 2729-2737, (2011).
27 Jo, S. H., Chang, T., Ebong, I., Bhadviya, B. B., Mazumder, P. & Lu, W. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **10**, 1297-1301, (2010).
28 Avouris, P., Chen, Z. H. & Perebeinos, V. Carbon-based electronics. *Nat. Nanotechnol.* **2**, 605-615, (2007).
29 Collins, P. C., Arnold, M. S. & Avouris, P. Engineering carbon nanotubes and nanotube circuits using electrical breakdown. *Science* **292**, 706-709, (2001).
30 Minot, E. D., Yaish, Y., Sazonova, V., Park, J. Y., Brink, M. & McEuen, P. L. Tuning carbon nanotube band gaps with strain. *Phys. Rev. Lett.* **90**, 156401, (2003).
31 Bachilo, S. M., Balzano, L., Herrera, J. E., Pompeo, F., Resasco, D. E. & Weisman, R. B. Narrow (n,m)-distribution of single-walled carbon nanotubes grown using a solid supported catalyst. *J. Am. Chem. Soc.* **125**, 11186-11187, (2003).
32 Zheng, M., Jagota, A., Strano, M. S., Santos, A. P., Barone, P., Chou, S. G., Diner, B. A., Dresselhaus, M. S., McLean, R. S., Onoa, G. B., Samsonidze, G. G., Semke, E. D., Usrey, M. & Walls, D. J. Structure-based carbon nanotube sorting by sequence-dependent DNA assembly. *Science* **302**, 1545-1548, (2003).
33 Cabana, J. & Martel, R. Probing the reversibility of sidewall functionalization using carbon nanotube transistors. *J. Am. Chem. Soc.* **129**, 2244-2245, (2007).

34 Snow, E. S. & Perkins, F. K. Capacitance and conductance of single-walled carbon nanotubes in the presence of chemical vapors. *Nano Lett.* **5**, 2414-2417, (2005).
35 Ahn, Y. S., Kim, K., Park, H. K., Hahn, H. T. & Chen, Y. Functionalized carbon nanotube networks with field-tunable bandgaps. *Adv. Mater.* **23**, 3075-3079, (2011).
36 Binks, A. E. & Sharples, A. Electrical conduction in olefin oxide polymers. *J. Polym. Sci. A2* **6**, 407-&, (1968).
37 Emami, S. H., Salovey, R. & Hogen-Esch, T. E. Peroxide-mediated crosslinking of poly(ethylene oxide). *J .Polym. Sci. Pol. Chem.* **40**, 3021-3026, (2002).
38 Kim, K. S., Bae, D. J., Kim, J. R., Park, K. A., Lim, S. C., Kim, J. J., Choi, W. B., Park, C. Y. & Lee, Y. H. Modification of electronic structures of a carbon nanotube by hydrogen functionalization. *Adv. Mater.* **14**, 1818-1821, (2002).
39 Park, K. A., Seo, K. & Lee, Y. H. Adsorption of atomic hydrogen on single-walled carbon nanotubes. *J. Phys. Chem. B* **109**, 8967-8972, (2005).
40 Zhang, G. Y., Qi, P. F., Wang, X. R., Lu, Y. R., Mann, D., Li, X. L. & Dai, H. J. Hydrogenation and hydrocarbonation and etching of single-walled carbon nanotubes. *J. Am. Chem. Soc.* **128**, 6026-6027, (2006).
41 Avouris, P., Appenzeller, J., Martel, R. & Wind, S. J. Carbon nanotube electronics. *Proc. IEEE* **91**, 1772-1784, (2003).
42 Dresselhaus, M. S., Dresselhaus, G., Saito, R. & Jorio, A. Raman spectroscopy of carbon nanotubes. *Phys. Rep.* **409**, 47-99, (2005).
43 Strano, M. S., Dyke, C. A., Usrey, M. L., Barone, P. W., Allen, M. J., Shan, H. W., Kittrell, C., Hauge, R. H., Tour, J. M. & Smalley, R. E. Electronic structure control of single-walled carbon nanotube functionalization. *Science* **301**, 1519-1522, (2003).
44 Nikitin, A., Ogasawara, H., Mann, D., Denecke, R., Zhang, Z., Dai, H., Cho, K. & Nilsson, A. Hydrogenation of single-walled carbon nanotubes. *Phys. Rev. Lett.* **95**, (2005).
45 Kim, K., Chen, C. L., Truong, Q., Shen, A. M. & Chen, Y. A carbon nanotube synapse with dynamic logic and learning. *Adv. Mater.* **25**, 1693-1698, (2013).
46 Gardner, D. & Stevens, C. F. Rate-limiting step of inhibitory post-synaptic current decay in aplysia buccal ganglia. *J. Physiol.* **304**, 145-164, (1980).
47 Erokhin, V., Berzina, T., Camorani, P., Smerieri, A., Vavoulis, D., Feng, J. & Fontana, M. Material memristive device circuits with synaptic plasticity: learning and memory. *BioNanoScience* **1**, 24-30, (2011).
48 Chang, T., Jo, S. H. & Lu, W. Short-term memory to long-term memory transition in a nanoscale memristor. *ACS Nano* **5**, 7669-7676, (2011).
49 Kuzum, D., Jeyasingh, R. G., Lee, B. & Wong, H. S. Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing. *Nano Lett.* **12**, 2179-2186, (2012).
50 Bichler, O., Suri, M., Querlioz, D., Vuillaume, D., DeSalvo, B. & Gamrat, C. Visual pattern extraction using energy-ffficient "2-PCM synapse" neuromorphic architecture. *IEEE Trans. Electron Devices* **59**, 2206-2214, (2012).

51 Buonomano, D. V. & Maass, W. State-dependent computations: spatiotemporal processing in cortical networks. *Nat. Rev. Neurosci.* **10**, 113-125, (2009).
52 Cavus, I. & Teyler, T. Two forms of long-term potentiation in area CA1 activate different signal transduction cascades. *J. Neurophysiol.* **76**, 3038-3047, (1996).
53 Singh, T. B., Marjanovic, N., Matt, G. J., Sariciftci, N. S., Schwodiauer, R. & Bauer, S. Nonvolatile organic field-effect transistor memory element with a polymeric gate electret. *Appl. Phys. Lett.* **85**, 5409-5411, (2004).
54 Park, B., Choi, S., Graham, S. & Reichmanis, E. Memory and photovoltaic elements in organic field effect transistors with donor/acceptor planar-hetero junction interfaces. *J. Phys. Chem. C* **116**, 9390-9397, (2012).
55 Haddon, R. C. The fullerenes - powerful carbon-based electron-acceptors. *Phil. Trans. R. Soc. Lond. A* **343**, 53-62, (1993).
56 Cho, B., Kim, K., Chen, C.-L., Shen, A. M., Truong, Q. & Chen, Y. Nonvolatile analog memory transistor based on carbon nanotubes and C60 molecules. *Small*, Early View (2013).
57 Alagiriswamy, A. A., Narayan, K. S. & Raju, G. Relaxation processes in aromatic polyimide. *J. Phys. D: Appl. Phys.* **35**, 2850-2856, (2002).
58 Gaur, R. M. S. & Tiwari, R. K. Time-dependent charging current study in polyimide film. *J. Plast. Film Sheeting* **25**, 271-283, (2009).
59 Moradi, S. & Indiveri, G. A VLSI network of spiking neurons with an asynchronous static random access memory. in *Biomedical Circuits and Systems Conference (BioCAS), 2011 IEEE.* 277-280.
60 Kim, K. H., Gaba, S., Wheeler, D., Cruz-Albrecht, J. M., Hussain, T., Srinivasa, N. & Lu, W. A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications. *Nano Lett.* **12**, 389-395, (2012).