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UNIVERSITY OF CALIFORNIA,
IRVINE

A 53-61GHz Low-Power PLL in 65nm CMOS

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Electrical engineering

by

Razieh Abedi

Thesis Committee:
Professor Payam Heydari, Chair
Associate Professor Ozdal Boyraz
Professor Ender Ayanoglu

2017

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DEDICATION

To my parents and husband

For their supports and encouragement

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ABSTRACT OF THE THESIS

A 53-61GHz Low-Power PLL in 65nm CMOS

By

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Master of science in Electrical Engineering

University of California, Irvine, 2017

Professor Payam Heydari, Chair

A 53-61GHz low-power charge-pump PLL is presented. This integer-N type-II PLL employs a class-D V-band VCO, a divide-by-1024 chain. The first divider in the chain is an inductor-less divide-by-4 injection-locked frequency divider (ILFD). The proposed PLL is fabricated in a standard 65nm CMOS process. The PLL achieves a tuning range of 13% from 53.35GHz to 60.83GHz and a phase-noise of -85.23dBc/Hz at 1MHz offset, while consuming a minimum DC power of 50.8mW. This PLL can be used as part of the LO generation network for millimeter-wave phased-array transceivers.

INTRODUCTION

mm-wave PLLs continue to be utilized as the core circuits in LO generation networks for mm-wave wireless transceivers and vehicular radars. These applications mandate frequency generation circuits with low phase-noise (e.g., $\leq$-80dBc/Hz at 1MHz offset), low-power (e.g., ≤ 100 mW), and wide tuning range (e.g., $\geq 10\%$) [1], [2].

Satisfying these specifications is challenging at mm-wave frequencies due to inherently poor performance of constituent active and passive devices [3] - [7].

This work introduces a fundamental frequency PLL covering frequencies from 53.35-60.83GHz. The design techniques in this work leads to low phase-noise and power consumption and wide locking range, all proved to be essential for radar and wireless communication applications.

V-BAND PLL ARCHITECTURE

The system block diagram of the V-band type-II PLL-based frequency synthesizer is presented in Fig. 1. It is comprised of a class-D V-band differential VCO, a divide-by-4 ILFD, a frequency divider chain with division ratio of 256, a phase/frequency detector (PFD), a charge pump (CP), and a 3rd-order loop filter (LF).

The divider chain is based on CML-type flip-flop-based topology. Programmable PFD and loop filter are utilized to calibrate the inaccuracy due to process, voltage, and temperature variation (PVT). Two common-source buffers are used after the VCO with one buffer driving the ILFD and the other one (with an additional GSG pad) monitoring the output of the loop.

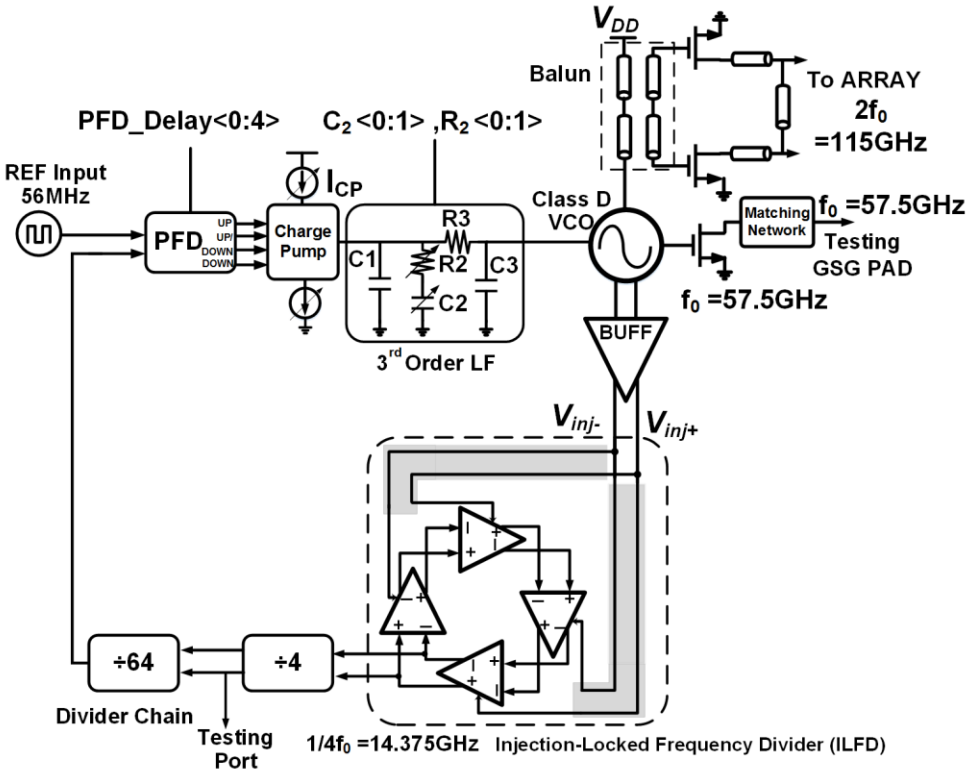

Fig. 1. Block diagram of the v-band Phase-Locked Loop

PLL BUILDING BLOCKS

Class-D V-band VCO

Low power consumption, low phase-noise, and wide tuning-range are desired for any VCO, including the ones operating at mm-wave frequencies. This work presents a class-D oscillator with relatively large voltage swing despite its operation with a low supply voltage.

Fig. 2. shows the circuit schematic of this VCO. The transformer feedback provides the required negative resistance for oscillation start-up. In addition, the mutually coupled t-lines introduce excess phase-shifts required to maximize the oscillation power at the fundamental frequency [8]. Furthermore, it also decouples the DC biases of the gates and the drains of M_1 and M_2 Most PLL loops require low K_{VCO} for the loop stability and low sensitivity to unwanted fluctuations on the VCO control lines. In this work, we have used small varactors to ensure small K_{VCO} for the VCO. However, with small varactors, tuning range is limited. At low RF frequencies, discrete tuning by switched-capacitors are often used to widen the tuning range of the VCOs. At millimeter-wave frequencies, however, switched-capacitors add significant loss to the circuit, thus degrading the phase noise. In addition to using the MOS varactors, the proposed VCO employs additional tuning mechanism to avoid switched capacitors.

The coupled t-lines allow separate bias voltages for the gate and drain terminals. The gate bias voltage is independently varied to change parasitic capacitors of M_1 and M_2, thereby introducing frequency tuning. Consequently, wider tuning range and limited K_{VCO} is achieved without any need for switch capacitors.

One way of reducing the oscillator phase noise is to increase the oscillation amplitude. The VCO in Fig. 2 operates at a supply voltage of 0.8V. Reaching high voltage swing is thus even more challenging considering that for higher oscillation amplitudes, transistors unavoidably enter their triode region for a portion of the oscillation cycle.

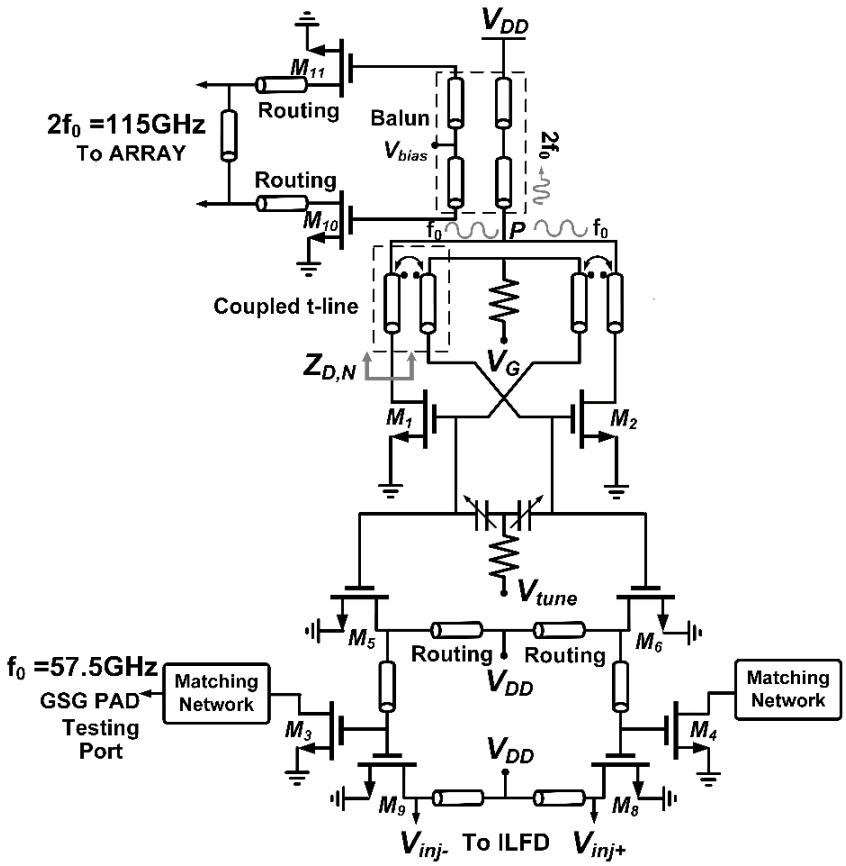

Fig. 2. Schematic of the Proposed VCO and buffers

A transistor entering different regions of operation during the oscillation cycle exhibits a time-variant nonlinear behavior. As for any nonlinear circuit, any harmonic voltage amplitudes at the gate and drain terminals may thus alter any other harmonic content of the drain current. In particular, the push-push topology of this VCO boosts the second harmonic of the drain voltages operating at node P of the cross-coupled pair

transistors. These second harmonic components can strongly affect the fundamental frequency content of drain current. This effect can be understood with the following signal flow study. Large fundamental voltage amplitude on the drain node will result in considerable second harmonic current generation due to the transistor nonlinearity, I_{21} [9]. This is illustrated on the left-side of Fig. 3. This current can create the second harmonic voltage on the drain (node P) as it flows through the drain load ($Z_{D,2}$ at the second harmonic). This voltage, in turn, induces the fundamental current, again, through the transistor nonlinearity, I_{12} which is illustrated on the right-side of Fig. 3. The boosted drain current at the fundamental frequency can further increase the drain voltage at the fundamental frequency by flowing through the drain load ($Z_{D,1}$ at the fundamental frequency). It is intuitively seen that if the voltage phasor of the second harmonic component is in-phase with the one of the first harmonic current, this reinforcement will be constructive, and a harmonic positive feedback is created [9].

At the circuit level, this can be achieved if the drain load is designed to be resistive both at the fundamental and the second harmonic frequencies. To this extent, the common drain node in Fig. 2 is a virtual ground at the fundamental frequency but not at the second harmonic. As a result, the M_1 and M_2 drain impedances at the second harmonic can be altered without affecting the drain impedance at the fundamental frequency.

The balun used at the common drain node is designed to load the drain of M_1 and M_2 by a resistive load at the second harmonic. The 22Ω load creates a 0.3V amplitude at the drains of M_1 and M_2 at the second harmonic. This balun will be used in a future phased-array system, which needs a differential feed at 120GHz.

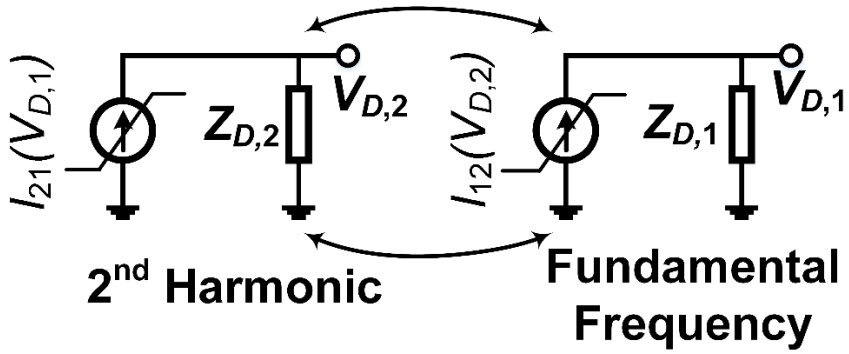

Fig. 3. Mutual harmonic translations between the fundamental frequency and the second harmonic

Eventually, our proposed oscillator has simulated oscillation amplitude of 0.92V from a 0.8V supply. This could only be achieved by exploiting the benefits of the second harmonic. As a result, better phase noise performance could be achieved, while the supply voltage and dc power consumption are kept low. The dc power consumption of the VCO varies between 10.6mW and 17.5mW for different values of V_G.

The independent control over the gate voltage is significantly helpful to engineer the amount of time the transistors spend in the triode region in one cycle of oscillation. Consequently, mutual translations between harmonics in Fig. 3. could be maximized. The constructive loop between the fundamental frequency and the second harmonic components not only has boosted the oscillation amplitude for low phase noise but also has boosted the required 120GHz power flowing into the balun for the future use in a phased-array system. This has obviated the need for additional frequency doublers. Therefore, the harmonic loop has had twofold benefits for our system.

Injection Locked Frequency Divider (ILFD)

Following the class-D VCO, the ILFD should be designed such that its locking range is sufficiently wide to cover more than just the tuning range of the VCO. This ensures that the VCO and the ILFD can still lock despite of any potential shifts in oscillation frequencies of either the VCO or the ILFD.

A ring oscillator-based ILFD (ring-ILFD) with inherently lower Q-factor compared to an LC oscillator-based ILFD (LC-ILFD) exhibits wider locking range and less output signal variation [10], [11]. In fact, in an LC-ILFD, the tank impedance drops sharply as the output frequency deviates from resonant frequency causing variation in output amplitude.

The schematic of the inductor-less ring-ILFD is shown in Fig. 4. The absence of inductors in the design leads to reduces the chip area, significantly. The ILFD is composed of 4 stages of injection buffer. The ring oscillator's free-running frequency is at ω_{free} if no injection signal is applied.

As it is shown in Fig. 4, the biasing transistor M_0 injects the injection current $I_{inj,\ \omega i}$ into the differential pair. The differential pairs act like ideal switches as the output swing is large. Therefore, the injection current $I_{inj,\ \omega i}$ mixes with the ILFD's fundamental oscillation frequency and its third harmonic. The low pass filter behavior caused by the interaction of the output impedance of each stage with the input capacitance of the following stage suppresses frequencies higher than ω_0. Therefore, the lower frequency component of the mixing product between the third and the injected signal will survive. If this frequency falls inside the valley region of the divider's sensitivity curve, it can lock to the 1/4th of the injected signal [11].

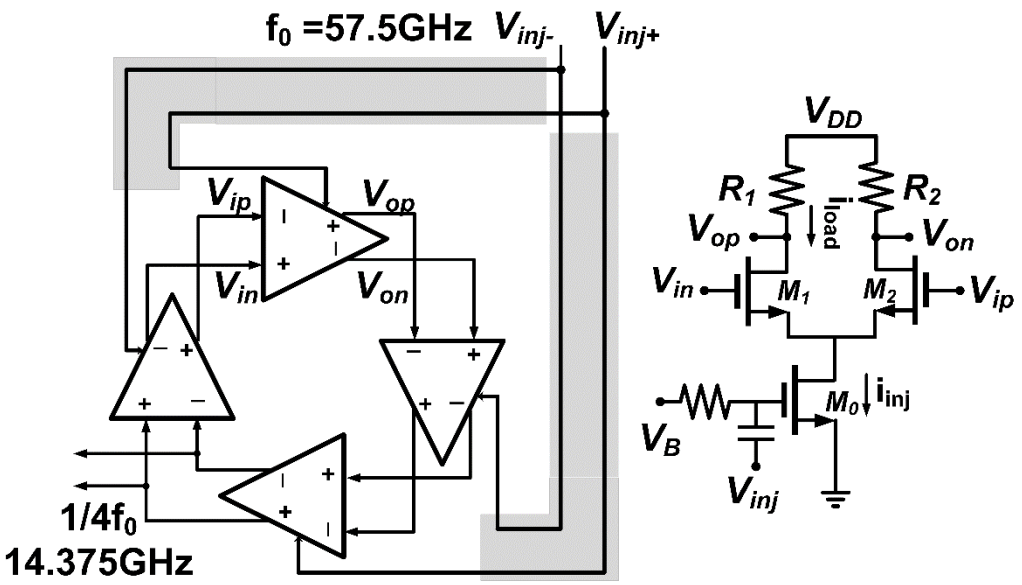

Fig. 4. Ring oscillator based injection locked divider with single tail injection

The locking range is improved in this architecture, as each injected signal bears the phase difference such that i_{inj} in Fig. 4 is orthogonal to i_{load}. The maximum locking range is achieved when multiple $i_{inj,\omega o}$ are applied with optimal phase difference. For the 4:1 frequency division, this optimal phase difference is 4xπ/4 or equivalently π. The locking range decreases or becomes even worse than the case with single injection if the optimal phase is not satisfied for the injected signals [12].

To provide the 180-degree phase shift between injected signals at around 60GHz, symmetric layout is considered. The CPW lines are used to rout the signals from the class-D VCO to the ILFD with the minimum phase error and loss. Moreover, the layout of the ring oscillator is developed in such a way as to make sure each stage has the same load at the output.

The ring shape of the compact layout of the ILFD, as it is shown in Fig. 4, leads to symmetric interconnections between each two consecutive stages. Moreover, these interconnections do not introduce any phase delay from the drain of one transistor to the gate of the next. Hence, the third harmonic components (i.e., ~45 GHz) at the gate and drain nodes reinforce themselves for even higher amplitudes, leading to an enhancement of the locking range.

By taking advantage of the compact layout of the ILFD, and maximizing the generated power by the VCO and delivered power from the injected signal to the ILFD, this structure can operate up to 61GHz which is much higher than reported ring-ILFD designs [10]-[12].

Other Loop Components

The VCO output signal is fed back through the injection locked divider, and the output frequency is scaled down to 56 MHz to be compared with an external signal source by the PFD. The biasing current of the CML dividers were scaled down based on the operation frequency.

The charge pump was designed to eliminate the region of low gain near phase lock [13]. The detector generates the "UP" and "DOWN" current pulses during each cycle even when the PLL locks eliminating the dead zone. Programmable 4-bit delay is added in the PFD to acquire optimal close-in phase noise.

The passive on-chip 3rd-order loop filter is implemented. From Fig.1, C_2 produces the first pole and together with R_1 is used to generate a zero to stabilize the loop. C_1 is utilized to smoothen the control voltage ripples. In order to further suppress reference spurs and high frequency noise R_3, C_3 are used.

Circuit simulations were done in order to choose the value of loop components and also investigate the stability of a loop which leads to the target bandwidth of 1MHz. The loop filter components value are C_1 =0.8pF, R_2=12kΩ, C_2=24pF, C_3=0.3pF. Two bits are used to modify the value of C_2 and R_2 to compensate for PVT variation. The value of C_2 and R can be chosen between 22pF, 24pF, 26pF and 10kΩ, 12kΩ, 14kΩ respectively.

MEASURMENT RESULTS

The PLL is fabricated in 65nm CMOS process. Fig. 5 shows chip micrograph of the PLL with chip core area of 0.38x0.9 mm ^{2}. The supply voltage is 1.2V except the charge pump and the PFD which operate at 2.4V to have wider tuning range (0 to 2.4V) for VCO. The supply voltage for the VCO is 0.8V. There are two GSG pads for the PLL measurement to monitor the VCO output and also the locking range of the ILFD.

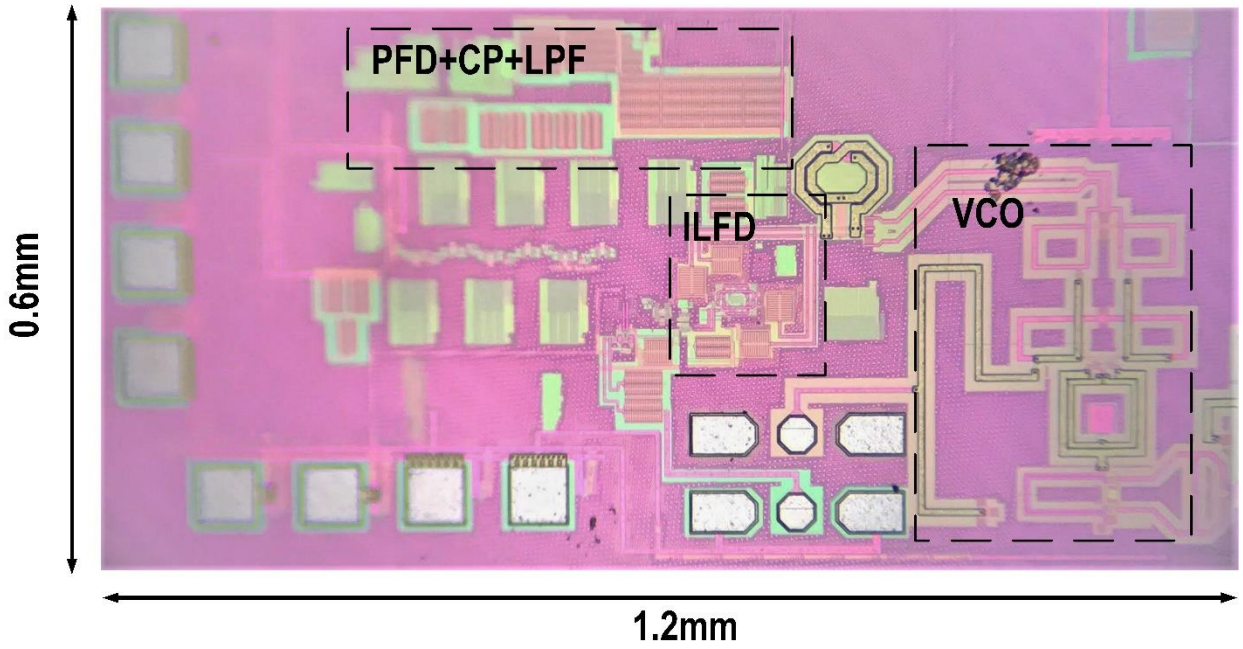

Fig. 5. die micrograph of the PLL in 65nm CMOS Process

The PLL achieves a locking range of 7.48GHz (from 53.35GHz to 60.83GHz). Spectrum analyzer, Anritsu MG3694C signal generator, and Agilent 11970V series harmonic mixer are used to measure the output spectrum of the PLL and VCO. Fig.7 shows the measured output spectrum of the locked PLL at 57.34GHz with the reference clock of the 56MHz. The output power here includes the setup loss including the

conversion loss of the mixer at 57GHz. An external Signal Generator is used as the reference for the PLL. Since the reference spurs are buried in the noise floor, the spurious is less than -37dBc.

The measured tuning range of the stand alone VCO is shown in Fig. 6. The frequency tuning range of the 13% is achieved for the standalone VCO. The ILFD has a wider locking range, and can thus cover the whole tuning range of the VCO. The locking range of the ring-ILFD is 15GHz (50 - 66GHz). Therefore, the PLL achieves 13% locking range at the center frequency of 57.5GHz.

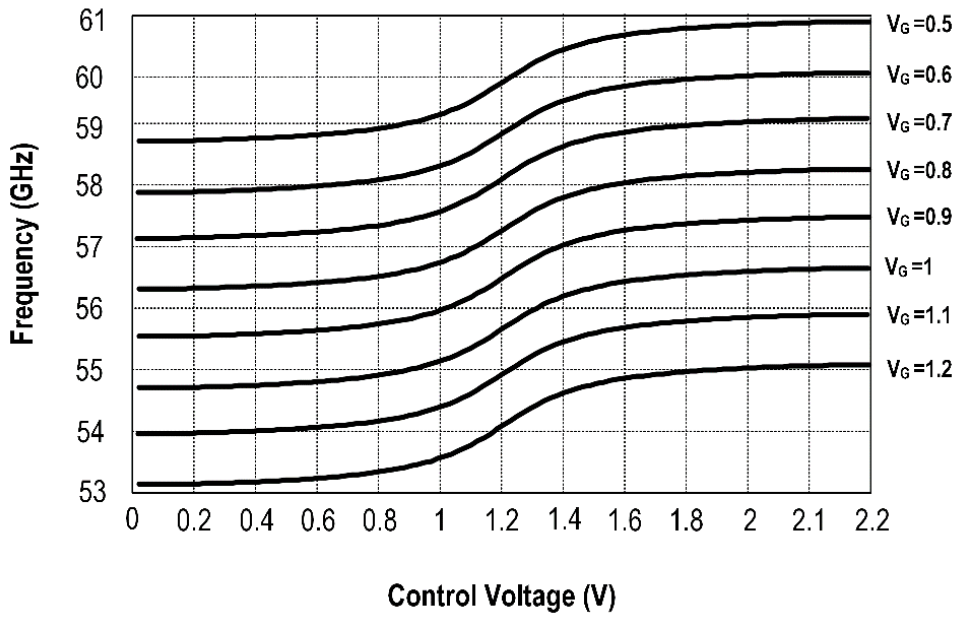

Fig. 6. Measured tuning range of the stand alone VCO

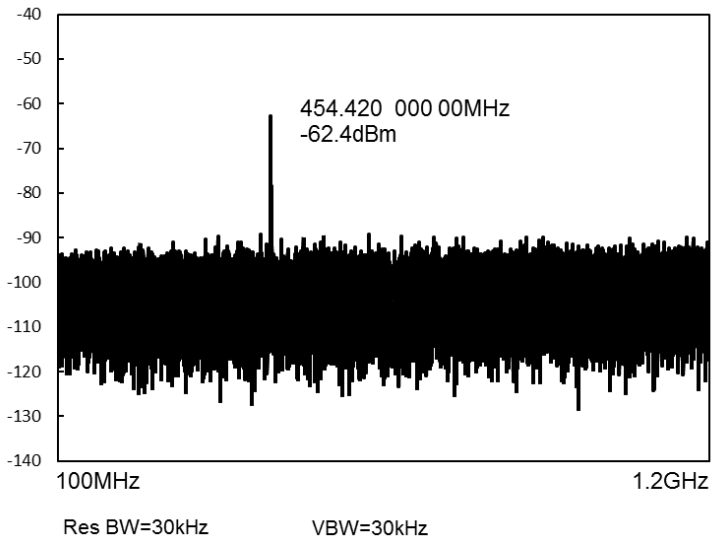

Fig. 7. Measured down converted output spectrum

The measured phase noise profile is shown in Fig. 8. For the frequency offsets beyond the loop bandwidth, the phase noise is dominated by the phase noise of the VCO which is -84.01dBc/Hz and -90dBc/Hz at 1MHz and 10MHz offset frequency, respectively. The total phase noise of the locked PLL is -85.23dBc/Hz at 1MHz offset frequency.

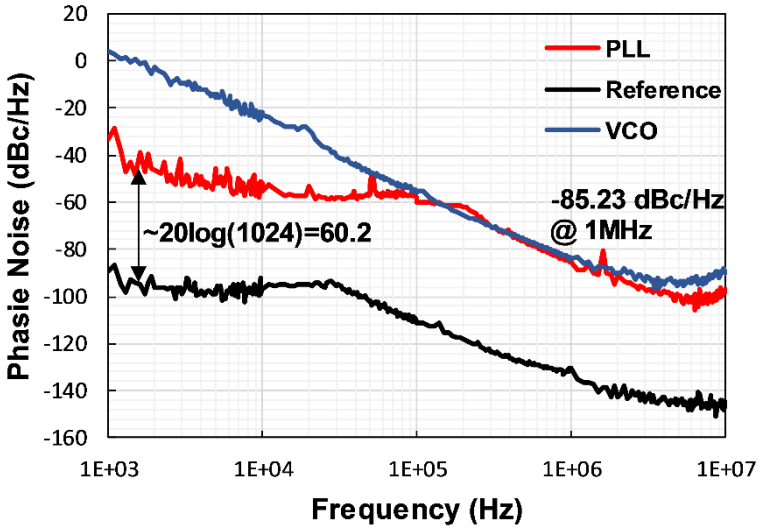

Figure 8. Measured phase noise of the V-band PLL and reference signal

Table I compares the proposed PLL with state-of-the art 60GHz fundamental PLLs. The wide locking range in [6] was achieved by adopting 3 binary-weighted digitally controlled capacitors and an A-MOS varactor. Furthermore, the coupled QVCOs in this work improved the phase noise performance. The digital fractional-N PLL presented in [7] used combination of several tuning techniques including 5-bit binary-weighted finger capacitor banks, NMOS transistors, and 2-bit switched coupled inductors to achieve the wide locking range. Several on-chip calibration techniques are used to lower the in-band phase noise and spurs caused by capacitor banks. In [3], a binary-weighted bank of varactors is employed so as to provide coarse tuning. However, the low Q factor of varactors is limiting factor for performance (i.e., output power and phase noise) improvement. Moreover, two VCOs were used to cover whole output range. In this work, wide tuning range is achieved without any need for bank of capacitors and varactors for discrete tuning. The PLL in this work achieves low phase noise and wide tuning range from a 56MHz reference signal generator with -130dBc/Hz at 1MHz offset.

Table 1: COMPARISION OF CMOS FUNDAMENTAL-OSCILLATION PLLS

[Ref.]	Technology	Frequency	PN @1MHz (dBc/Hz)	Reference Spur (dBc)	Reference Frequency (MHz)	P_{DC} (mw)	Area (mm^2)	Topology
[5]	65nm	58.5-58.9 (0.68%)	-83.5	-66	150	43	0.64	Without the capacitor bank
[4]	90nm	60.2-62.4 (3.58%)	-62.92	-36	78	106.6	1.12 ††	Without the capacitor bank
[3]	45nm	57-66 (14.6%)	-75	-42	100	78	0.82	With the varactor bank
[7]	65nm	50.2-66.5 (28%)	-88*	-59.1	100	46	0.45	With capacitor bank
[6]	65nm	58-68.3 (8.3%)	-91*	-45	135	24	0.192	With capacitor bank †††
This work	65nm	53.35-60.83 (13%)	-85.23	<-37	56	50.8-62.1†	0.34	Without the capacitor bank

†The minimum power consumption of VCO is 10.57mW. ††With Pad. ††† Uses the in- phase injection-coupled QVCO.

*The reference signal is crystal oscillator.

CONCLUSION

A V-band phase-locked loop was designed and fabricated in a 65nm CMOS process. The PLL achieves a wide tuning range and good phase noise. A class-D VCO with transformer feedback to boost the oscillation power was introduced. The wide band injection-locked divider was designed to increase the locking range of the PLL.

This PLL achieved a measured tuning range of 13% from 53.35GHz to 60.83GHz and a phase-noise of -85.23dBc/Hz at 1MHz offset, while consuming a minimum DC power of 50.8mW.

REFRENCES

[1] C. Marcu, et al. “A 90 nm CMOS low-power 60 GHZ transceiver with integrated baseband circuitry,” IEEE Journal of Solid-State Circuits, vol. 44, no. 12, pp. 3434–3447, Dec 2009.

[2] W. Deng, et al. “A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers,” IEEE Journal of Solid-State Circuits, vol. 48, no. 7, pp.1710–1720, July 2013.

[3] K. Scheir, et al. “A 57-to-66ghz quadrature PLL in 45nm digital CMOS,” in 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, Feb 2009, pp. 494–495,495a.

[4] H. K. Chen, T. Wang, and S. S. Lu, “A millimeter-wave CMOS triple-band phase-locked loop with a multimode LC-based ILFD,” IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 5, pp. 1327–1338, May 2011.

[5] Y. L. Yeh, X. Lin, H. Y. Chang, and K. Chen, “A v-band 65 nm CMOS low dc power low phase noise PLL using divide-by-three injection-locked frequency divider,” in 2016 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Aug 2016, pp. 1–3.

[6] X. Yi, et al. “A 57.9-to-68.3ghz 24.6mw frequency synthesizer with in-phase injection-coupled QVCO in 65nm CMOS,” in 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, Feb 2013, pp. 354–355.

[7] A. Hussein, et al. “19.3 a 50-to-66ghz 65nm CMOS all-digital fractional-N PLL with 220fsrms jitter,” in 2017 IEEE International Solid-State Circuits Conference (ISSCC), Feb 2017, pp. 326–327.

[8] O. Momeni and E. Afshari, “High power terahertz and millimeter-wave oscillator design: A systematic approach,” IEEE Journal of Solid-StateCircuits, vol. 46, no. 3, pp. 583–597, March 2011.

[9] R. Kananizadeh and O. Momeni, “High-power and high-efficiency millimeter-wave harmonic oscillator design, exploiting harmonic positive feedback in CMOS,” IEEE Transactions on Microwave Theory and Techniques, vol. PP, no. 99, pp. 1–15, 2017.

[10] H. Tong, S. Cheng, A. I. Karsilayan, and J. S. Martinez, “An injection-locked frequency divider with multiple highly nonlinear injection stages and large division ratios,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 4, pp. 313–317, April 2007.

[11] S. Liu, et al. “Ring oscillator based injection locked frequency divider using dual injection paths,” IEEE Microwave and Wireless Components Letters, vol. 25, no. 5, pp. 322–324, May 2015.

[12] J. C. Chien and L. H. Lu, “Analysis and design of wideband injection-locked ring oscillators with multiple-input injection,” IEEE Journal of Solid-State Circuits, vol. 42, no. 9, pp. 1906–1915, Sept 2007.

[13] C. C. Wang, Z. Chen, and P. Heydari, “W-band silicon-based frequency synthesizers using injection-locked and harmonic triplers,” IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 5, pp. 1307–1320, May 2012.