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Resonant Switched-capacitor Converters with Wide Line Regulation Range and Control Maps for PWM plus Phase-shift Modulated DC-DC Converters

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

In Electrical Engineering

by

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ABSTRACT OF THE DISSERTATION

Resonant Switched-capacitor Converters with Wide Line Regulation Range and Control Maps for PWM plus Phase-shift Modulated DC-DC Converters

By

Shouxiang Li

Doctor of Philosophy in Electrical Engineering

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Professor Keyue Smedley, Chair

Part I: Resonant Switched-capacitor Converters with Wide Line Regulation Range

The traditional switched-capacitor converter (SCC) typically comes with the shortcomings of high transient current spike, hard-switched operation and limited line regulation range. In this thesis, a family of resonant two-switch boosting switched-capacitor converter (RTBSC) and a family of Ladder resonant switched-capacitor converter (RSC) with low transient current spike, soft-switching operation and wide line regulation range are proposed. By inserting a small resonant inductor, the additional benefit of reduction of one or two bulky capacitor banks to much smaller resonant capacitor(s) is obtained. By operating above the resonant frequency, the transistors are ZVS turned on and diodes are zero-current-switching (ZCS) turned off. Most importantly, the voltage-gain range is significantly expanded. This resonant configuration is applicable to TBSC, Ladder SCC and the Dickson SCC.

However, the regulation capability of the proposed RTBSC and Ladder RSC is still a challenge at light load condition. To ease this issue, a family of step-up resonant switched-

capacitor converter (RSC) with continuously adjustable conversion ratio is proposed based on the Cuk Dual Resonance Core (DRC) concept. By adopting the on-time fixed frequency modulation, its conversion ratio can vary continuously and efficiently even at the light load condition (1/10 of the rated power). The configuration of Cuk DRC is applicable to the Series-parallel (SP) SCC, Fibonacci SCC, Voltage Doubler (VD) and Dickson SCC.

Part II: Control Maps for PWM plus Phase-shift Modulated DC-DC Converters

In this part, comprehensive analyses about the operation principle, power transmission capability, component stress and the zero-voltage-switching (ZVS) operation region for a three-level PWM plus phase-shift (PPS) modulated bidirectional push-pull converter and a family of two-level PPS modulated isolated bidirectional DC-DC converters (IBDCs) are presented. Based on the analyses, a set of control maps is established to assist converter operation and design in the low-circulating-current regions, high-power-transmission-capability regions, and ZVS operation regions. In the control maps, a circuit parameter is identified, providing a design limit to select switching frequency, leakage inductance, turns ratio and power level of the PPS modulated DC-DC converters.

PART I

CHAPTER 1: A Family of Resonant Two-switch Boosting Switched-Capacitor Converter with ZVS Operation and a Wide Line Regulation Range

1.1 Introduction

Switched-capacitor converter (SCC) has the potential to achieve small size, light weight, high efficiency and high power density for DC-DC power conversion [1]. Over the last decades, researches in this field flourished, resulted in many SCC topologies, such as conventional Ladder SCC, Dickson SCC [2], series-parallel SCC [3][4], flying capacitor multilevel dc-dc converter (FCMDC) [5]-[7], multilevel modular capacitor-clamped dc-dc converter (MMCCC) [8] and so forth. The inductor-less property makes SCC possible to be integrated on chip for milliwatt-power level applications [2][9][10], operating as the power supply for other function blocks such as EEPROM, Flash memories, mixed-signal VLSI and so forth. In addition, applications where power levels are in the range from tens of watts [3][4][11] to kilowatt-level [5]-[8][12], and even tens of kilowatts [13] were reported in the literature, demonstrating the widespread utilization of SCCs.

One major limitation for the SCCs is its limited line regulation range. If the output voltage is regulated, the input-voltage variation range is constrained by a narrow band, because the voltage gain is predetermined by the circuit structure with little adjustability [18]. Several methods were proposed to improve the line and load regulation performances. One of them is to operate the converter at a duty cycle close to 0.5 and a fixed frequency, while adopting the on-resistance control [1]. However, the smaller on-resistance is preferable to achieve higher efficiency, limiting the regulation range. Another method is to change the duty cycle of the transistors, as reported in [3][4][11]. But the switching current will be very high if the duty cycle is small, causing high EMI and power losses. One can also use frequency modulation. This method is mainly for chip-level SCCs [9] [10], whose switching frequency range can be adjusted widely in the order of Mega Hertz. A combination of two

modulation variables can also be employed to regulate capacitors' charging time and switching frequency so as to achieve the line and load regulation [14]. Moreover, [15]-[17] reported the quasi-switched-capacitor (QSC) converter, where p-type MOSFET being operated as a controllable constant current source to regulate the output. However, the precise control of the current level may be difficult [18] and the extra p-type MOSFET and the driving circuit will increase the cost and circuit complexity.

To combine the advantages of high-voltage-gain of a SCC and good output regulation of a switching-mode dc-dc converter, some hybrid converters were proposed. In [19], traditional Fibonacci SC converter and boost/buck-boost converter were coupled to obtain a good regulation. In [20], two buck converters were cascaded before and after an n-cell phase-shifted switched-capacitor (PSSC) converter [21]. Aside from the SCCs, SC cells can also be utilized in some traditional inductor-based converters to combine the voltage-lift and regulation functions. Such voltage-lift technique was employed in Luo converter to increase the output voltage gain in geometric progression [22]. The SC cell - voltage multiplier - was applied in the interleaved boost converter [23] and then extended to some other topologies [24]- [27].

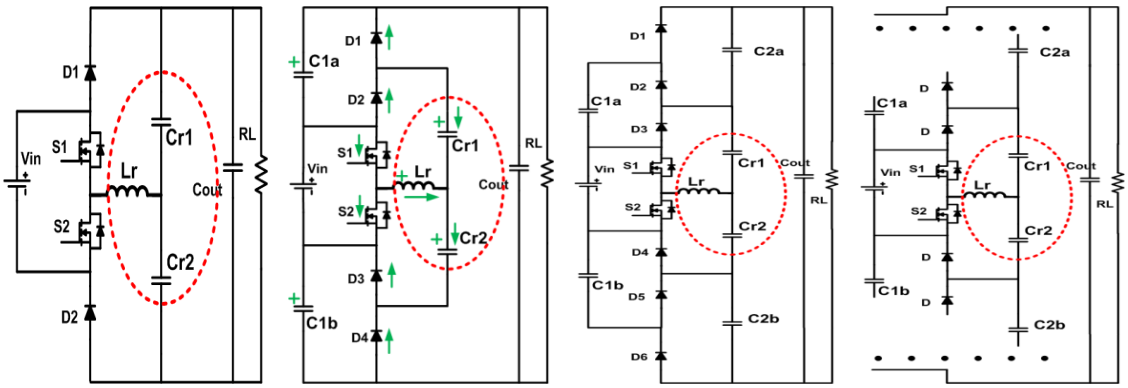
Another limitation for SC converters is the hard-switched operation, which results in switching losses [2] – [13], hindering the increase of switching frequency. Zero-current-switching (ZCS) SC converters with an inserted resonant tank were proposed in [28]-[30]. Those converters typically operate at a switching frequency lower than the resonant frequency and their resonant current is in DCM. If the resonant frequency is designed to be a much higher value, the added resonant inductor can be integrated on a chip as reported in [31]. The achieved ZCS operation improves the efficiency, however, ZVS is still preferable

for MOSFETS. Moreover, the ZCS RSCs are still bounded by the most severe limitation of inability to provide regulation against line and transient load changes [32]. Theoretically, the voltage gain in DCM is almost fixed. Therefore, the output voltage will follow any change in the input voltage and no satisfactory transient response can be achieved in case of load changes.

In [33], "sneak circuit" paths of Dickson RSCs were found at different operating frequencies, inspiring researchers to explore the characteristics of RSCs in different operation regions. In [34], the improved voltage regulation capability of a double voltage-ratio RSC above its resonant frequency was verified, revealing the significance of this operation region.

In this chapter, a family of RTBSCs with ZVS operation and a wide line regulation range is proposed. Compared to the previously proposed TBSCs [35][36], from the UCI Laboratory, only a small resonant inductor is added, while two bulky capacitor banks are replaced by two much smaller resonant capacitors. By operating it above the resonant frequency, the transistors are ZVS turned on and diodes are ZCS turned off, reducing the switching loss significantly. In addition, the voltage-gain range is expanded significantly, so that it can tolerate large input-voltage-variation if the output voltage is regulated. The different operation modes, voltage-gain curves, soft-switching regions, output characteristics and current/voltage stresses of the resonant tank for this family were analyzed in details. A 3X RTBSC prototype with maximum output voltage 150V, maximum output power 140W was built. The analysis has been verified by experimental results. The contents in this chapter have been published in paper [37].

1.2 Operation Modes and Voltage-gain Curves



(a) 2X (b) 3X (c) 4X (d) N-X

Fig. 1.1. Topologies of the proposed RTBSC family

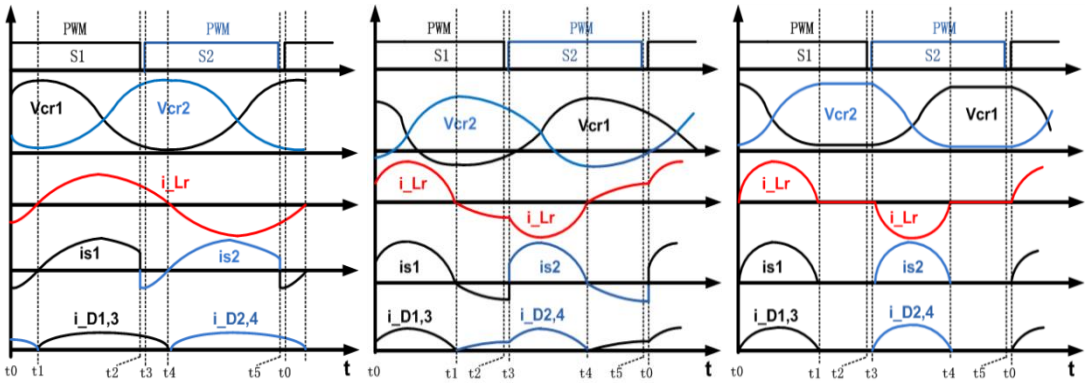
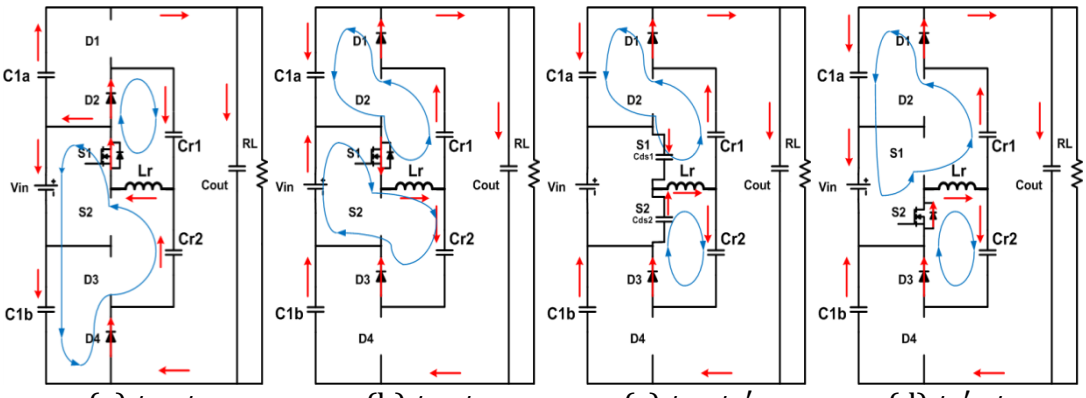
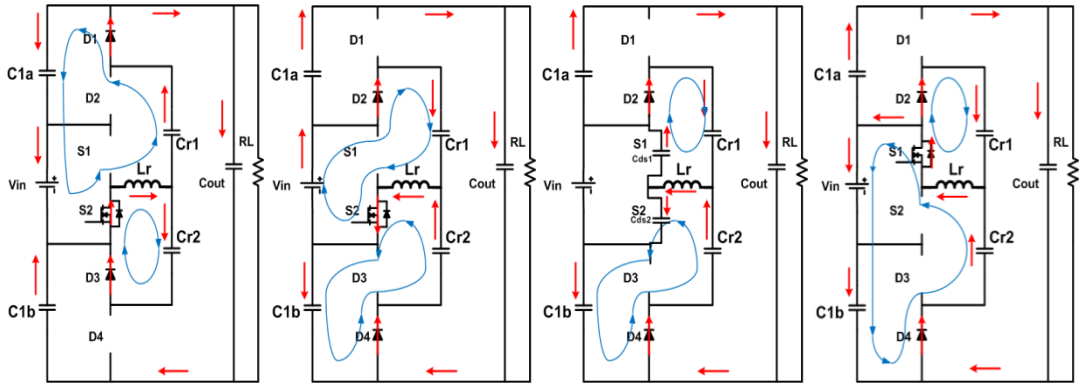


Fig. 1.2. Operating waveforms of 3X RTBSC





(e) $t_3 \sim t_4$ (f) $t_4 \sim t_5$ (g) $t_5 \sim t_5'$ (h) $t_5' \sim t_0$

Fig. 1.3. Operating states of 3X RTBSC ($CCM_{1<F<2}$)

The TBSC converter family was proposed in the Power Electronics Laboratory at UCI [35] with the advantage of only two active switches, automatic interleaved operation and low output voltage ripple. Significant improvement in voltage regulation can be achieved by inserting a small resonant inductor. Soft switching and reduction of capacitance come as added benefits.

The topologies of the proposed RTBSCs family are shown in Fig. 1.1, where the resonant tank is highlighted with the red circle, while the other part is the same as the structure of TBSC in [35]. In this part, a 3X RTBSC will be analyzed to find different operation modes and the corresponding voltage-gain curves. Then the similar analysis will be extended to N-X RTBSCs.

The topology of 3X RTBSC is shown in Fig. 1.1 (b), where $S_{1,2}$ are MOSFETs with internal anti-parallel diodes and $D_1 \sim D_4$ are power diodes. An inductor L_r and two small film capacitors $C_{r1,2}$ constitute the resonant tank, which is highlighted in the red circle. Capacitors $C_{1a,1b}$ are charge banks with much larger capacitance.

The duty cycle of S_1 and S_2 is fixed at 0.5 and their driving signals are complimentary with a short dead-time. The voltage across $C_{r1,2}$ is denoted as $V_{cr1,2}(t)$, while the voltages

across $C_{1a,1b}$ are defined as $V_{c1a}(t)$ and $V_{c1b}(t)$. The currents flowing through L_r, switches $S_{1,2}$ and diodes D_1~D_4 are represented by $i_{Lr}(t)$, $i_{s1,2}(t)$ and $i_{D1\sim D4}(t)$ respectively. The switching frequency and resonant frequency are represented by f_s and f_r. The defined positive directions are highlighted in green arrows in Fig. 1.1 (b).

For simplicity, several assumptions are made as follows. With the symmetrical structure, the capacitances of C_{r1} and C_{r2} are both equal to C_r, so the maximum (minimum) voltage values across them are both equal to $V_{cr\_max}(V_{cr\_min})$. The capacitances of C_{1a} and C_{1b} are large and equal to each other, so the voltages on both C_{1a} and C_{1b} maintained at a constant value V_c in a given switching cycle. The ESRs of all capacitors, on-resistance of switches and forward voltage of diodes are neglected. The dead-time between the complimentary driving signals is neglected.

1.2.1 Operation Modes and Voltage-gain Curve of 3X RTBSC

1.2.1.1 Operation in Frequency Region $f_r < f_s < 2f_r$

When $f_r < f_s < 2f_r$, the transistors are ZVS turned on while the diodes ZCS turn off. In addition, the voltage-gain range is widened by changing f_s within a relatively small range. Moreover, the RMS current stress is lower, which will be discussed later. Therefore the nominal operating frequency is chosen in this range. The typical operating waveforms and the equivalent circuits in different operating states are shown in Fig. 1.2(a) and Fig. 1.3. This operating mode is defined as $CCM_{1<F<2}$. Analyses of converter operation and voltage-gain curve in $CCM_{1<F<2}$ are as follows.

First, in every operating state illustrated in Fig. 1.3, the following equation is always held:

$$V_{in} + V_c = V_{cr1}(t) + V_{cr2}(t) = V_{cr1}(t_1) + V_{cr2}(t_1) = V_{cr\_max} + V_{cr\_min} \quad (1)$$

As a result, the output voltage is:

$$V_o = 2V_c + V_{in} = 2\left(V_{cr\_max} + V_{cr\_min}\right) - V_{in} \quad (2)$$

Secondly, from Fig. 1.3, both C_{1a} and the load are charged by C_{r1} during $t_1 \sim t_4$. Then all the charges stored in C_{1a} will be transferred to the load during $t_0 \sim t_1$ and $t_4 \sim t_0$, which means all the charges delivered to the load will be first stored in C_{r1} in each switching cycle. According to the charge balance of C_{r1}:

$$C_r(V_{cr\_max} - V_{cr\_min}) = \frac{V_o}{R_L} * \frac{1}{f_s}, \text{ where } R_L \text{ is the load resistance} \quad (3)$$

Thirdly, the values of V_{cr_max} and V_{cr_min} can be derived according to the KVL and KCL equations in each operating state.

$[t_1 \sim t_2]$: In this state, there are two charging loops denoted in blue arrows, as shown in Fig. 1.3(a). The KVL and KCL equations in this operating state are:

$$-L_r \frac{di_{Lr}(t)}{dt} + V_{cr1}(t) - V_c = 0 \quad (4)$$

$$C_r \frac{dV_{cr}(t)}{dt} = -\frac{1}{2} i_{Lr}(t) \; (C_{r1} = C_{r2}) \quad (5)$$

From Fig. 1.2(a), the boundary conditions are:

$$i_{Lr}(t_1) = 0, V_{cr1}(t_1) = V_{cr\_max} \quad (6)$$

Based on (1) (4) (5) (6), the resonant current and voltage are:

$$i_{Lr}(t) = (V_{in} - V_{cr\_min})\sqrt{\frac{2C_r}{L_r}} sin2\pi f_r(t - t_1), \text{ where } f_r = \frac{1}{2\pi\sqrt{2L_rC_r}} \quad (7)$$

$$V_{cr1}(t) = (V_{cr\_max} + V_{cr\_min} - V_{in}) + (V_{in} - V_{cr\_min})cos2\pi f_r(t - t_1) \quad (8)$$

$[t_2 \sim t_4]$: This interval is composed of three parts - $t_2 \sim t_3'$, $t_3' \sim t_3$ and $t_3 \sim t_4$, but the equations are the same. At t_2, transistor S_1 is turned off and then the loop current will charge the parasitic capacitance C_{ds1} of S_1 and discharge C_{ds2} of S_2 till t_2', shown in Fig. 1.3(c). The parasitic capacitance is so small, thus this interval is very short, which is

neglected in steady-state calculation. After t_2', the voltage across C_{ds2} is discharged to zero and the internal anti-parallel diode of S_2 starts conducting current, shown Fig. 1.3(d). At t_3, transistor S_2 is turned on with ZVS operation.

During $[t_2 \sim t_4]$, the KVL and KCL equations are:

$$-L_r \frac{di_{Lr}(t)}{dt} + V_{cr1}(t) - (V_{in} + V_c) = 0 \quad (9)$$

$$C_r \frac{dV_{cr}(t)}{dt} = -\frac{1}{2} i_{Lr}(t) \ (C_{r1} = C_{r2}) \quad (10)$$

From Fig. 1.2(a), the boundary conditions are:

$$i_{Lr}(t_4) = 0, V_{cr1}(t_4) = V_{cr\_min} \quad (11)$$

Based on (1) (9) (10) (11), the resonant current and voltage are:

$$i_{Lr}(t) = (-V_{cr\_max}) \sqrt{\frac{2C_r}{L_r}} sin2\pi f_r (t - t_4) \quad (12)$$

$$V_{cr1}(t) = (V_{cr\_max} + V_{cr\_min}) + (-V_{cr\_max}) cos2\pi f_r (t - t_4) \quad (13)$$

During $[t_1 \sim t_4]$, both the resonant current and voltage are composed of two different parts of sinusoidal waveforms and the overall frequency is equal to f_s if dead-time is neglected, i.e.:

$$t_2 - t_0 = t_4 - t_1 = \frac{1}{2} \frac{1}{f_s} \quad (14)$$

According to (7) (12) (14):

$$(V_{in} - V_{cr\_min}) sin2\pi f_r \left(\frac{1}{2} \frac{1}{f_s} + t_0 - t_1\right) + V_{cr\_max} sin2\pi f_r (t_0 - t_1) = 0 \quad (15)$$

Similarly, according to (8) (13) (14):

$$(V_{in} - V_{cr\_min}) cos2\pi f_r \left(\frac{1}{2} \frac{1}{f_s} + t_0 - t_1\right) + V_{cr\_max} cos2\pi f_r (t_0 - t_1) = V_{in} \quad (16)$$

By solving the set of equations (15) (16), the following expression can be obtained:

$$cos \frac{f_r}{f_s} \pi = \frac{V_{cr\_min}^2 - 2V_{in} V_{cr\_min} + V_{cr\_max}^2}{2V_{cr\_min} V_{cr\_max} - 2V_{cr\_max} V_{in}} < 0 \ (f_r < f_s < 2f_r) \quad (17)$$

Assuming $d = cos\frac{f_r}{f_s}\pi$, $k = C_r R_L f_s$ and according to (2) (3) (17):

$$M_{cr\_min} = \frac{V_{cr\_min}}{V_{in}} = \frac{(1-d)k^2+(A-d-3)k+6d+6-2A)}{2[(1-d)k^2+4d+4]} \quad (18)$$

$$M_{cr\_max} = \frac{V_{cr\_max}}{V_{in}} = \frac{(k+2)M_{cr\_min}-1}{k-2} \quad (19)$$

$$M = \frac{V_o}{V_{in}} = \frac{k[(1-d)k+2A-4d-4]}{(1-d)k^2+4d+4}$$

$$\text{where A}=\sqrt{(d^2-2d+1)k^2+(2d^2-2)k+d^2+8d+7} \quad (20)$$

However, a special scenario should be noted. The minimum voltage gain of the 3X RTBSC is 1, resulting from the structure of the TBSC converter. As a result, the voltage-gain curve maintains at 1 when (20) is smaller than 1. In this condition, equation of charge balance (3) will not be held, while (2) and (17) are still true. This operating mode is defined as $Fixed - Gain_{1<F<2}$ ($FG_{1<F<2}$). According to (2) (17), the following equations are derived:

$$M_{cr\_max} = \sqrt{\frac{1}{2(1+d)}} \quad (21)$$

$$M_{cr\_min} = 1 - \sqrt{\frac{1}{2(1+d)}} \quad (22)$$

$$M = \frac{V_o}{V_{in}} = 1 \quad (23)$$

The boundary constraint between $FG_{1<F<2}$ and $CCM_{1<F<2}$ is when equation (20) is smaller than 1.

1.2.1.2 Operation in Frequency Region $\frac{1}{2}f_r < f_s < f_r$

When $\frac{1}{2}f_r < f_s < f_r$, the transistors are hard-switched and suffer from capacitive turn-on losses and dv/dt noise, which is not practical for very high-frequency operation [38]. Typically, the RTBSC does not operate in this region. In order to make the analysis

complete, the voltage-gain curve is analyzed as well. The operating waveforms are shown in Fig. 1.2(b). This operating mode is defined as $CCM_{0.5<F<1}$

With the similar method, the equations of resonant current and voltage during $[t_0 \sim t_1]$ and $[t_1 \sim t_3]$ can be derived:

$$i_{Lr}(t) = (V_{in} - V_{cr\_max})\sqrt{\frac{2C_r}{L_r}} sin2\pi f_r(t - t_1) \tag{24}$$

$$V_{cr1}(t) = (V_{cr\_max} + V_{cr\_min} - V_{in}) + (V_{in} - V_{cr\_max})cos2\pi f_r(t - t_1) \tag{25}$$

And,

$$i_{Lr}(t) = (V_{cr\_min})\sqrt{\frac{2C_r}{L_r}} sin2\pi f_r(t - t_1) \tag{26}$$

$$V_{cr1}(t) = V_{cr\_min}cos2\pi f_r(t - t_1) \tag{27}$$

By ignoring the dead-time and charging/discharging time of the parasitic capacitances, the following equations are held:

$$i_{Lr}(t_0) = -i_{Lr}(t_3) \tag{28}$$

$$V_{cr1}(t_0) + V_{cr1}(t_3) = V_{cr\_max} + V_{cr\_min} \tag{29}$$

According to (24) – (29), the following expression can be obtained:

$$cos\frac{f_r}{f_s}\pi = \frac{V_{cr\_min}^2 - 2V_{in}V_{cr\_max} + V_{cr\_max}^2}{2V_{cr\_min}V_{cr\_max} - 2V_{cr\_min}V_{in}} \quad (0.5f_r < f_s < f_r) \tag{30}$$

Moreover, equations (2) (3) are still true in this operation region. As a result, the following formulas can be derived according to (2) (3) (30):

$$M_{cr\_min} = \frac{V_{cr\_min}}{V_{in}} = \frac{(1-d)k^2 + (B+3d+1)k - 2d - 2 - 2B)}{2[(1-d)k^2 + 4d + 4]} \tag{31}$$

$$M_{cr\_max} = \frac{V_{cr\_max}}{V_{in}} = \frac{(k+2)M_{cr\_min} - 1}{k-2} \tag{32}$$

$$M = \frac{V_o}{V_{in}} = \frac{k[(1-d)k + 2B + 4d + 4]}{(1-d)k^2 + 4d + 4}$$

where B=$\sqrt{(d^2-2d+1)k^2-(2d^2-2)k+d^2+8d+7}$ (33)

However, two special conditions should be noted.

First, the minimum voltage gain is 1. As a result, the voltage-gain curve maintains at 1 when (33) is smaller than 1. Equation (3) will not be held, while (2) and (30) are still true. This operating mode is defined as $FG_{0.5<F<1}$.

According to (2) (30), the following equations are derived:

$$M_{cr\_max}=1+\sqrt{\frac{1}{2(1+d)}} \quad (34)$$

$$M_{cr\_min}=-\sqrt{\frac{1}{2(1+d)}} \quad (35)$$

$$M=\frac{V_o}{V_{in}}=1 \quad (36)$$

The boundary constraint between $FG_{0.5<F<1}$ and $CCM_{0.5<F<1}$ is when equation (33) is smaller than 1.

Secondly, the maximum voltage gain is 3, limited by the TBSC structure. Within a certain frequency range, the gain curve will maintain at 3. In this unregulated region, the resonant current will go to DCM as shown in Fig. 1.2 (c). This operating mode is defined as $DCM_{0.5<F<1}$. The boundary between $CCM_{0.5<F<1}$ and $DCM_{0.5<F<1}$ can be derived as follows.

In $DCM_{0.5<F<1}$, equation (3) will not be held. Based on (2) (30),

$$M_{cr\_max}=\left(1+\frac{3}{2k}\right) \quad (37)$$

$$M_{cr\_min}=\left(1-\frac{3}{2k}\right) \quad (38)$$

$$M=\frac{V_o}{V_{in}}=3 \quad (39)$$

If M_{cr_min} is larger than 0, the resonant tank cannot start resonating in the reverse direction and thus the resonant current goes to DCM. As a result, the constraint of $DCM_{0.5<F<1}$ is $M_{cr\_min} > 0$, i.e.

$$k > 3/2 \tag{40}$$

1.2.1.3 Voltage-gain Curve in Frequency Region $\frac{1}{2}f_r < f_s < 2f_r$

For convenience, the above analyses about operating modes, boundary conditions and voltage-gain formulas are summarized in Table 1.1.

Table 1.1. Key formulas for 3X RTBSC

Freq.	$0.5f_r < f_s < 2f_r$			$f_r < f_s < 2f_r$	
Mode	$FG_{0.5<F<1}$	$CCM_{0.5<F<1}$	$DCM_{0.5<F<1}$	$CCM_{1<F<2}$	$FG_{1<F<2}$
Boundary	Eq. (33)<1	Eq. (33)>1 &$k < 3/2$	Eq. (33)>1 & $k > 3/2$	Eq. (20)>1	Eq. (20)<1
M_{cr_min}	$-\sqrt{\frac{1}{2(1+d)}}$	Eq. (31)	$1-\frac{3}{2k}$	Eq. (18)	$1-\sqrt{\frac{1}{2(1+d)}}$
M_{cr_max}	$1+\sqrt{\frac{1}{2(1+d)}}$	Eq. (32)	$1+\frac{3}{2k}$	Eq. (19)	$\sqrt{\frac{1}{2(1+d)}}$
M	1	Eq. (33)	3	Eq. (20)	1

In order to plot the voltage-gain curve, two parameters are defined as follows:

$$\text{Frequency Ratio: F} = \frac{f_s}{f_r}, where\ f_r = \frac{1}{2\pi\sqrt{2L_rC_r}} \tag{41}$$

$$\text{Quality Factor: Q} = \frac{Z_r}{R_L}, where\ resonant\ impedance\ Z_r = \sqrt{L_r/2C_r} \tag{42}$$

As a result, the relationships between d, k and F, Q are:

$$d = cos\frac{f_r}{f_s}\pi = \cos(\frac{\pi}{F}),\ k = C_rR_Lf_s = \frac{F}{Q}\frac{1}{4\pi} \tag{43}$$

Substituting (43) into the formulas and boundary conditions in Table 1.1, the voltage-gain curve of 3X RTBSC is plotted in Fig. 1.4.

1.2.2 Voltage Gain of N-X RTBSC

The analysis method for N-X RTBSC is similar to that in part 1.2.1.

When $f_r < f_s < 2f_r$, equation (17) is always true for all RTBSCs when $f_r < f_s < 2f_r$. The only differences are the equations of output voltage and charge balance:

$$V_o = (N-1)(V_{cr\_max} + V_{cr\_\min}) - (N-2)V_{in} \tag{44}$$

$$\mathrm{C_r}(V_{cr\_max} - V_{cr\_min}) = \frac{N-1}{2} * \frac{\mathrm{V_o}}{\mathrm{R_L}} * \frac{1}{f_s} \tag{45}$$

When $0.5f_r < f_s < f_r$, equation (30) is always true for all RTBSCs. The equations of output voltage and charge balance are exactly the same as (44) and (45).

By consolidating the above equations and the boundaries between different operating modes, the voltage-gain curve of N-X RTBSC can be obtained. For instance, the voltage-gain curves of 2X and 4X RTBSC are plotted in Fig. 1.5 and Fig. 1.6.

From these figures, it is observed that the voltage gain curve resembles a bell like shape peaked at F=1. When Q changes from low (light load) to high (heavy load) the shape of the curve becomes sharper. Regulation of output voltage can be realized at heavy load, but is compromised at light ones.

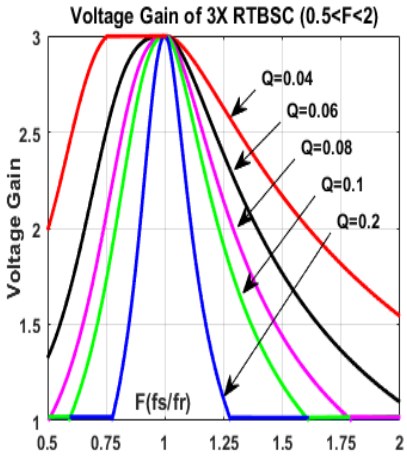


Fig. 1.4. Voltage gain of 3X RTBSC ($0.5 < \mathrm{F} < 2$)

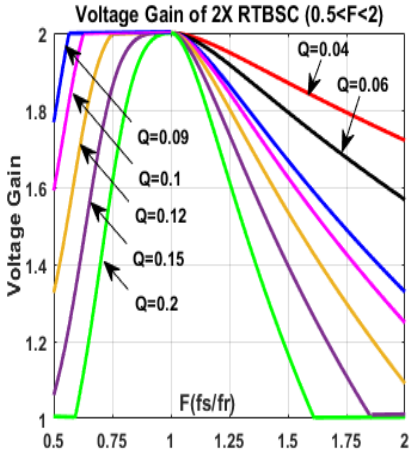


Fig. 1.5. Voltage gain of 2X RTBSC

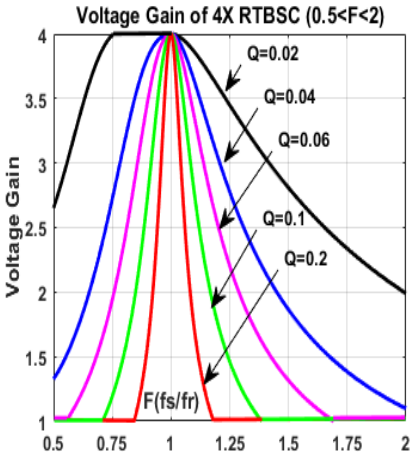


Fig. 1.6. Voltage gain of 4X RTBSC

1.2.3 Further Investigation

When $0.5 < F < 1$, with low Q, the gain curve will maintain at the maximum gain (N) over a certain frequency range, in which the RTBSC will lose regulation capability. For example, the Q is low, such as Q=0.04 and Q=0.06 in Fig. 1.6, the RTBSC will lose regulation capability completely in the range 0.5<F<1. As a result, aside from the hard-switched issue, another restriction preventing the RTBSC from operating in this region is the unregulated region.

When 1<F<2, the N-X RTBSC has higher "selectivity" than (N-1)-X RTBSC if Q is equal. For instance, when Q=0.04, the voltage-gain range of 2X RTBSC is 1.72 ~ 2. However, the voltage-gain range of 3X and 4X RTBSC is 1.56 ~ 3 and 1.14~4, respectively. If Q is low, corresponding to very light load condition, the line regulation range is limited. In order to change the voltage gain, switching frequency has to be varied a lot. This phenomenon is similar to the characteristics of series resonant converters (SRCs) [39].

1.3 Output Characteristics of RTBSCs

In this section, the output characteristics of RTBSCs will be discussed. The output characteristic curve can help to gain understanding of how to regulate the output voltage when the line voltage or load current is changing.

As mentioned in section 1.2.1, the operation switching frequency is above the resonant frequency, therefore, only modes $FG_{1<F<2}$ and $CCM_{1<F<2}$ are applicable. Furthermore, in mode $FG_{1<F<2}$, the voltage gain is fixed at 1 and the output characteristic can be represented by a straight line. Thus only the output characteristic in $CCM_{1<F<2}$ needs to be discussed.

1.3.1 Output Characteristics of 3X RTBSC

Several parameters are defined as follows:

$$\text{Current base: } I_b = \frac{V_{in}}{\sqrt{L_r/2C_r}} \tag{46}$$

$$\text{Normalized output current: } \mathrm{J} = \frac{V_o/R_L}{I_b} = \frac{M}{2\pi f_r C_r R_L} \tag{47}$$

From (47), once the input voltage and the resonant tank are determined, the value of J corresponds to the load current. In $CCM_{1<F<2}$, based on (2) (3) (17) and (47),

$$\mathrm{J} = \frac{F}{4\pi}\left(M_{cr\_max} - M_{cr\_min}\right) = \frac{F}{4\pi}\left(\sqrt{\frac{-M^2+2M+d(1-2M+M^2)+7}{4(d+1)}} - 1\right) \tag{48}$$

Referred to (48), the output characteristic of 3X RTBSC is plotted in Fig. 1.7.

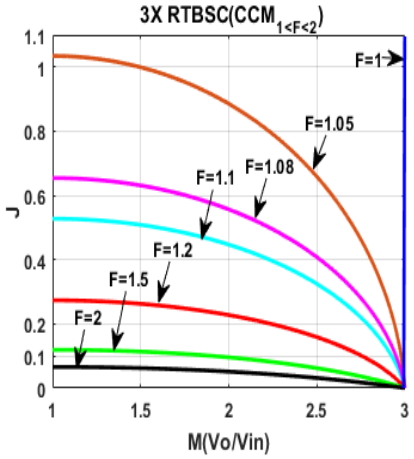


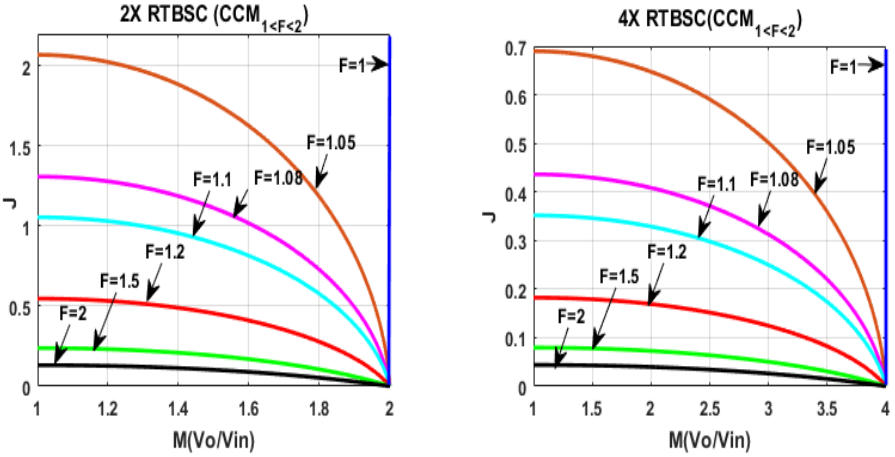
Fig. 1.7. Output characteristic of 3X RTBSC ($CCM_{1<F<2}$)

1.3.2 Output Characteristics of N-X RTBSC

For N-X RTBSC, according to (45) and (47),

$$\mathrm{J} = \frac{F}{2(N-1)\pi}(M_{cr\_max} - M_{cr\_min}) \tag{49}$$

When $1 < \mathrm{F} < 2$, the expression of (17) is always the same, while the equation of the output voltage is different, as given in (44). According to (17) (44) and (49), the output characteristic can be derived. For instance, the output characteristics of 2X and 4X RTBSCs are plotted in Fig. 1.8 (a) (b).



(a) 2X (b) 4X

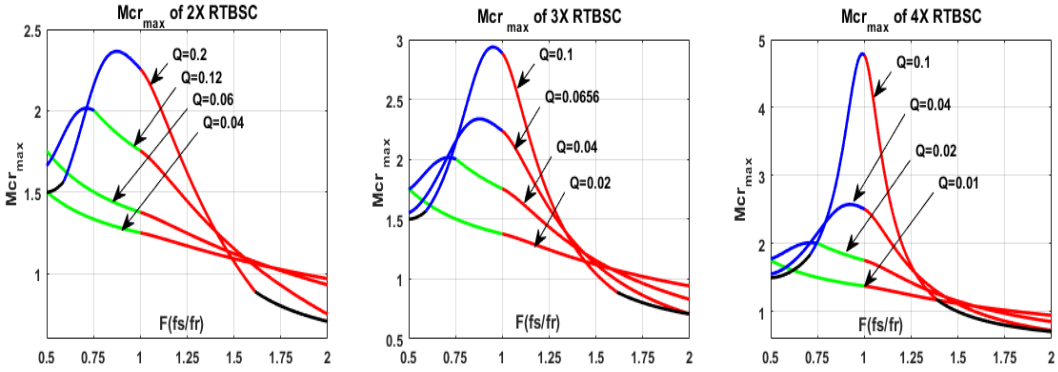
Fig. 1.8. Output characteristic of RTBSC ($CCM_{1<F<2}$)

1.4 Voltage and Current Stress of the Resonant Tank

1.4.1 Voltage Stress of the Resonant Capacitor

In this part, the normalized maximum voltage value (M_{cr_max}) of the resonant capacitor is analyzed. For 3X RTBSC, the value of M_{cr_max} in different operating modes can be obtained from Table 1.1. Considering the boundary constraints, M_{cr_max} of the resonant capacitor for 3X RTBSC is plotted in Fig. 1.9 (b). The black line, blue line, green line and red line represents M_{cr_max} in mode $FG_{0.5<F<1}$ / $FG_{1<F<2}$, $CCM_{0.5<F<1}$, $DCM_{0.5<F<1}$ and $CCM_{1<F<2}$, respectively.

Similarly, M_{cr_max} of the resonant capacitor for 2X/4X Ladder RSC is plotted in Fig. 1.9 (a) (c). The voltage stress for the resonant capacitor under different operating conditions can be obtained out.



(a) 2X (b) 3X (c) 4X

Fig. 1.9. Normalized maximum voltage value of the resonant capacitor for RTBSC

1.4.2 Current Stress of the Resonant Inductor

In this part, the normalized RMS current stress of the resonant inductor is analyzed.

For the 3X RTBSC, from Fig. 1.2(a) (b), the current waveform can be approximated to be a sinusoidal wave for simplicity, even though the practical RMS value is smaller. But it will give more design headroom for the purpose of components selections. As for the

$DCM_{0.5<F<1}$ in Fig. 1.2(c), the inductor current can be regarded as a periodic waveform composed of sinusoidal piecewise segments.

When 1<F<2, the equations of the current waveform in $FG_{1<F<2}$ and $CCM_{1<F<2}$ are same. The normalized RMS value of the sinusoidal current wave is calculated according to (7) (46):

$$J_{Lr\_rms} = \left| \frac{(V_{in} - V_{cr\_min})\sqrt{\frac{2C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}} \right| = \frac{1}{\sqrt{2}}(1 - M_{cr\_min}) \tag{50}$$

When 0.5<F<1, the normalized RMS current value of the resonant inductor in $FG_{0.5<F<1}$ and $CCM_{0.5<F<1}$ is calculated as:

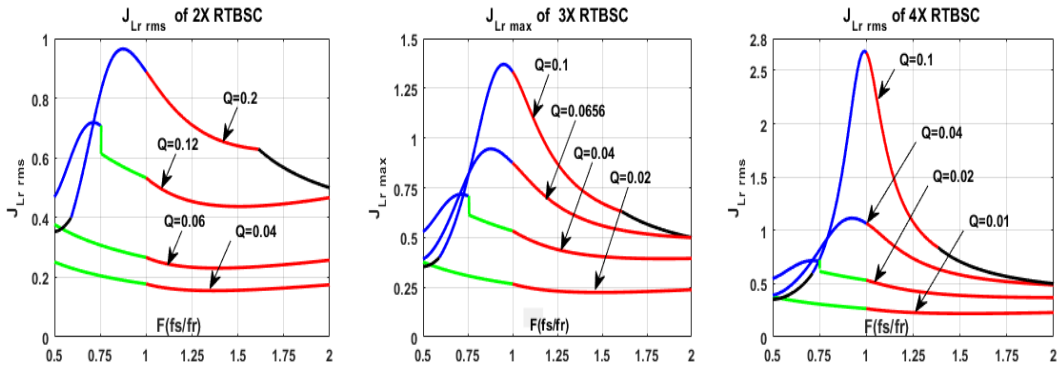
$$J_{Lr\_rms} = \left| \frac{(V_{cr\_max} - V_{in})\sqrt{\frac{2C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}} \right| = \frac{1}{\sqrt{2}}(M_{cr\_max} - 1) \tag{51}$$

In $DCM_{0.5<F<1}$, the normalized RMS current value of the resonant inductor is:

$$J_{Lr\_rms} = \sqrt{F} \times \left| \frac{(V_{cr\_max} - V_{in})\sqrt{\frac{2C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}} \right| = \frac{\sqrt{F}}{\sqrt{2}}(M_{cr\_max} - 1) \tag{52}$$

The corresponding values of M_{cr_min} and M_{cr_max} can be obtained from Table 1.1. The normalized RMS current value of the resonant inductor for 3X RTBSC is plotted in Fig. 1.10(b). The black line, blue line, green line and red line represents J_{Lr_rms} in condition $FG_{0.5<F<1}/FG_{1<F<2}$, $CCM_{0.5<F<1}$, $DCM_{0.5<F<1}$ and $CCM_{1<F<2}$. It's shown that current stress is high at high Q and 0.5<F<1, and low at low Q and 1<F<2.

Similarly, J_{Lr_rms} of the resonant inductor for 2X and 4X RTBSC is plotted in Fig. 1.10(a) (c). The current stress for the resonant inductor under different operating conditions can be figured out.



(a) 2X (b) 3X (c) 4X

Fig. 1.10. Normalized RMS current value of the resonant inductor for RTBSC

1.5 Hardware Design and Experimental Results

1.5.1 Hardware Design

In this part, a 3X RTBSC prototype with theoretical maximum output voltage 150V and maximum power 140W is designed. Typically, the operating frequency is recommended to be in the range of 1<F<2 for ZVS operation, but this prototype was designed to operate in the whole frequency range (0.5<F<2) for open loop test in order to demonstrate the validity of analyses in the entire operation range. While for closed-loop test, the converter will only operate in 1<F<2.

The highest switching frequency $2f_r$ is designed to be 150kHz, so the lowest switching frequency $0.5f_r$ and resonant frequency f_r are about 38KHz and 76KHz respectively. The resonant capacitors C_r are chosen to be two 100nF film capacitors. According to $f_r = \frac{1}{2\pi\sqrt{2L_rC_r}}$, the resonant inductor L_r is about 22uH.

In order to measure the performance of 3X RTBSC under different load conditions, two power loads -160Ω and 320Ω - are chosen. As a result, the theoretical values of Q are 0.0328 or 0.0656.

According to Fig. 1.3, the voltage stress $V_{s\_s1,s2}$ on transistor S_1 and S_2 is equal to the input voltage, i.e. $V_{s\_s1,s2} = V_{in}$. While for the voltage stress $V_{s\_D1\sim D4}$ on diodes $D_1 \sim D_1$, it's equal to the voltage across C_{1a} and C_{1b}, i.e. $V_{s\_D1\sim D4} = V_c = V_{cr\_max} + V_{cr\_\min} - V_{in} = \frac{V_o - V_{in}}{2}$. The voltage stress (normalized to V_{in}) of diodes is plotted in Fig. 1.11. Since the maximum gain of 3X RTBSC is 3, the maximum voltage on the diode is also equal to the input voltage, i.e. $V_{s\_D1\sim D4} = \frac{V_o - V_{in}}{2} = \frac{3V_{in} - V_{in}}{2} = V_{in}$. As shown, the voltage stress on transistors and diodes is low, equal to the input voltage. The voltage stress of the resonant capacitor can be figured out from Fig. 1.10(b), $V_{s\_Cr} \approx 2.4V_{in}$ when Q=0.0656.

The RMS current stress of the resonant inductor can be figured out from Fig. 1.11(b), i.e. $I_{rms\_Lr} \approx 0.95 \times I_b$ when Q=0.06256. From Fig. 1.2, the RMS current stress of $S_{1,2}$ is $I_{rms\_S1,S2} = \frac{i_{rms\_Lr}}{\sqrt{2}}$. In addition, the diode current is only half of the transistor current in every operation state, so $I_{rms\_D1\sim D4} = \frac{i_{rms\_Lr}}{2\sqrt{2}}$.

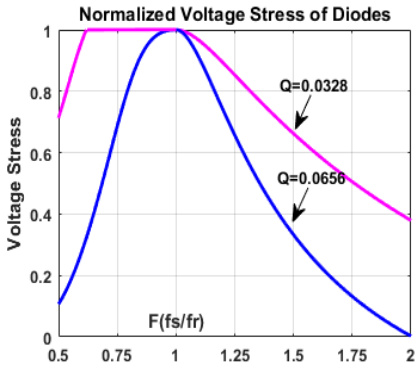


Fig. 1.11. Voltage stress of diodes for 3X RTBSC

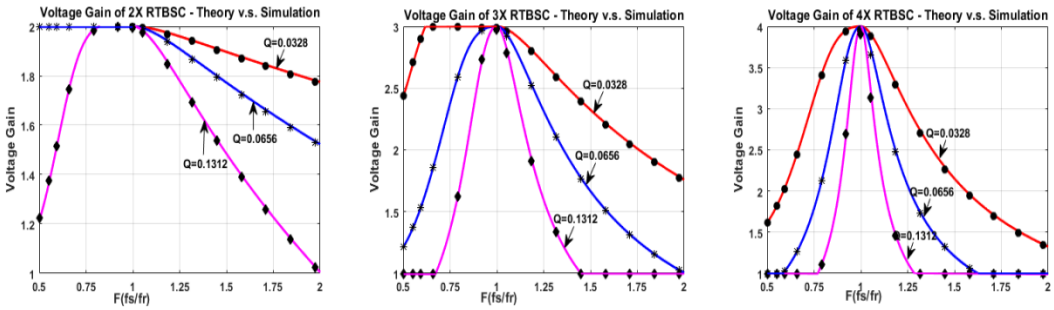
Based on the above analysis, proper components are selected and the parameters of the prototype in open-loop (OL) and closed-loop (CL) tests are listed in Table 1.2.

Table 1.2 Prototype specifications of 3X RTBSC

Power Level (Po)	<140W	C_{1a}, C_{1b}	100uF
Input (V_{in})	OL: 50V	$C_{r1,r2}$	100nF film capacitors
	CL:40~100V		
Output (V_o)	OL: <150V	L_r	22uH
	CL: 120V		
f_s	OL:38~150k Hz	f_r	76kHz
	CL:76~150k Hz		
C_{in}	100uF	$D_{1\sim4}$	MBR10100G
C_{out}	100uF	$S_{1,2}$	FDPF390N15A

1.5.2 Simulation and Experimental Results

A family of RTBSCs without parasitic elements is simulated using software Psim. The parameters of the circuit are selected from Table 1.2, and the voltage-gain curves are shown in Fig. 1.12. The solid lines represent the theoretical gain curves, while the black dots/stars/diamonds are simulation results. Seen from the preliminary comparison, the analysis matches the simulation results closely.



(a) 2X (b) 3X (c) 4X

Fig. 1.12. Simulated Voltage-Gain Curves of RTBSCs

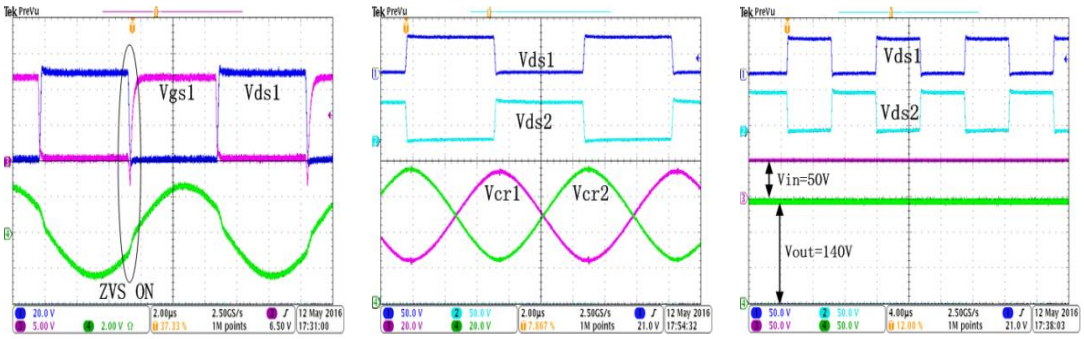
A prototype was then built. The experimental waveforms of open-loop test are shown in Fig. 1.13 ~ 1.16. In open-loop test, the input is fixed at 50V and then to measure the output voltage with different switching frequencies. Two load resistances are measured to be 163.9Ω and 322.8Ω, i.e. Q=0.064 and Q=0.0325 in practice.

In Fig. 1.13, Q is 0.0325 and f_s is 90kHz. The experimental waveforms match the waveforms of $CCM_{1<F<2}$ in Fig. 1.2(a). From Fig. 1.13(a), transistor S_1 is ZVS turned on, because the resonant current is negative when the driving signal of S_1 becomes high. Obviously, the switching noise on the drain-source of MOSFET is reduced a lot due to ZVS operation. Fig. 1.13(b) shows the resonant voltages on $C_{r1,r2}$. According to Fig. 1.13(c), V_{in} is 50V and V_{out} is 140V, thus the voltage gain is 2.8.

The boundary between 1<F<2 and 0.5<F<1 can be figured out from Fig. 1.14 approximately. The waveform of resonant current is almost a pure sinusoidal wave at 80kHz, which is the practical resonant frequency f_r.

In Fig. 1.15, Q is 0.0325 and f_s is 40kHz. The experimental waveforms match the waveforms of $CCM_{0.5<F<1}$ in Fig. 1.2(b). From Fig. 1.15(a), transistor S_1 is hard-switched turn on, while the resonant current is in CCM. Fig. 1.15 (b) shows the resonant voltages on C_{r1} and C_{r2}. According to Fig. 1.15(c), V_{in} is 50V and V_{out} is 121V, thus the voltage gain is 2.42.

In Fig. 1.16, Q is 0.0325 and f_s is 50kHz. The experimental waveforms match the waveforms of $DCM_{0.5<F<1}$ in Fig. 1.2(c). From Fig. 1.16(a), transistor S_1 is ZCS turned on, because the resonant current is in DCM. In Fig. 1.16(b), the resonant voltages on C_{r1} and C_{r2} maintain at constant values when the resonant current goes into DCM. According to Fig. 1.16(c), V_{in} is 50V and V_{out} is 137V, thus the voltage gain is 2.74.



(a) V_{gs1}, V_{ds1}, i_{Lr} (b) $V_{ds1}, V_{ds2}, V_{cr1}, V_{cr2}$ (c) $V_{ds1}, V_{ds2}, V_{in}, V_{out}$

Fig. 1.13. Operation waveforms in $CCM_{1<F<2}$ for 3X RTBSC

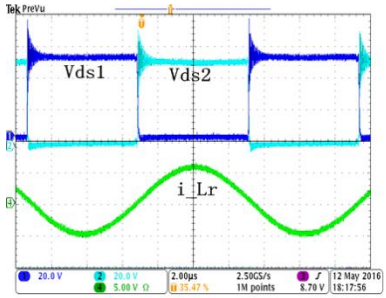
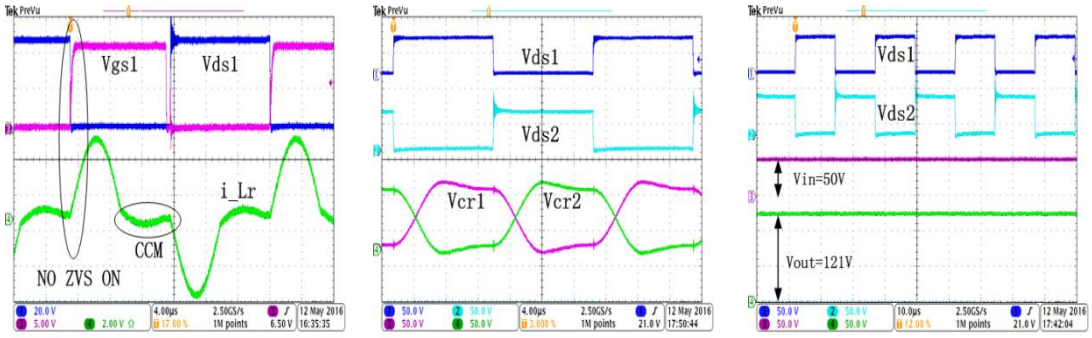
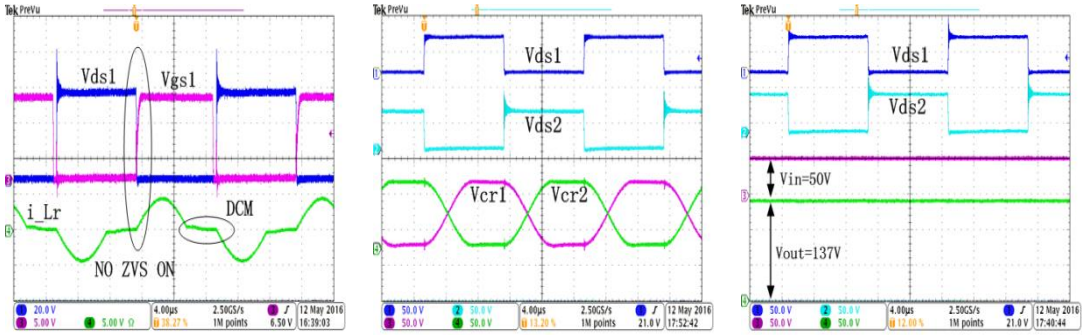


Fig. 1.14. Boundary condition for 3X RTBSC - f_s=80KHz



(a) V_{gs1}, V_{ds1}, i_{Lr} (b) $V_{ds1}, V_{ds2}, V_{cr1}, V_{cr2}$ (c) $V_{ds1}, V_{ds2}, V_{in}, V_{out}$

Fig. 1.15. Operation waveforms in $CCM_{0.5<F<1}$ for 3X RTBSC



(a) V_{gs1}, V_{ds1}, i_{Lr} (b) $V_{ds1}, V_{ds2}, V_{cr1}, V_{cr2}$ (c) $V_{ds1}, V_{ds2}, V_{in}, V_{out}$

Fig. 1.16. Operation waveforms in $DCM_{0.5<F<1}$ for 3X RTBSC

The comparison of experimental and theoretical voltage-gain curve is plotted in Fig. 1.17. The solid lines represent theoretical gain curve, while the dashed lines stand for the experimental results. From the graph, the maximum gain is about 2.84, peaking at round 80kHz which matches the boundary condition in Fig. 1.14. The deviations from the theoretical peak gain (3) and resonant frequency (76kHz) are mainly caused by ESRs, diode forward voltage, parasitic capacitance and the inaccuracy of resonant capacitance and inductance. However, the experimental curve is still close to the analysis and demonstrates the wide voltage-gain range. For Q=0.0325, the voltage gain changes from 2.84 to 1.96 by regulating f_s from 80 to 150kHz. For Q=0.064, the voltage gain changes from 2.73 to 1.2 by regulating f_s from 80KHz to 150kHz. In addition, when 0.5<F<1, the converter enters $DCM_{0.5<F<1}$ and the voltage-gain becomes almost a constant over a certain frequency range, seen from the dashed blue line. In practice, this unregulated region will be avoided by operating the RTBSC above the resonant frequency.

In Fig. 1.18, the curve of measured efficiency versus frequency is plotted. When 0.5<F<1, the transistors are hard-switched, deteriorating the overall efficiency. When 1<F<2, the transistors and diodes are soft switched, reducing the switching loss significantly. In addition, based on the analysis in section 1.4.2, the RMS current stress in 0.5<F<1 is higher, causing higher conduction loss as well. As a result, the overall efficiency below f_r is lower than that above f_r, which can be seen from Fig. 1.18 clearly. Aside from the unregulated issue, this is another reason that the RTBSC will be operating in 1<F<2.

In comparison, a traditional 3X TBSC converter was built with the same voltage level and power level. In Fig. 1.19(a), the voltage-gain curves of traditional 3X TBSC converter under different load conditions are shown. Only frequency range of 1k ~ 30kHz is shown in

details, because the capacitors are partially charged and thus the voltage-gain can be regulated in this region. After 30kHz, the voltage-gain will become almost a constant (30k~60kHz) and then start decreasing as the frequency increasing (>60kHz) due to hard-switched operation. Even in the low-frequency range, the voltage-gain range is much narrower than the proposed RTBSC. More importantly, the efficiency of SC converter is directly proportional to the voltage-gain [18], so the overall efficiency is poor when the voltage-gain is low, as shown in Fig. 1.19(b). To sum up, the traditional TBSC is more suitable for fixed-voltage-gain, low-frequency-operation and high-power-level (when conduction loss is dominant) applications. In contrast, the proposed RTBSC is more suitable for wide-voltage-gain-range, low-power-level and high-frequency-operation (when switching loss is dominant) applications. Considering the soft-switching operation of RTBSCs, by proper design of the resonant frequency to a much higher value, the component size of the RTBSC can be reduced significantly, while not sacrificing the overall efficiency or regulation range.

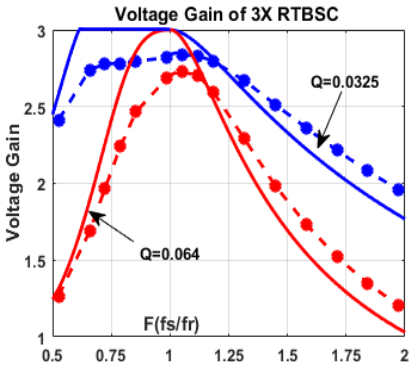


Fig. 1.17. 3X RTBSC - gain curve

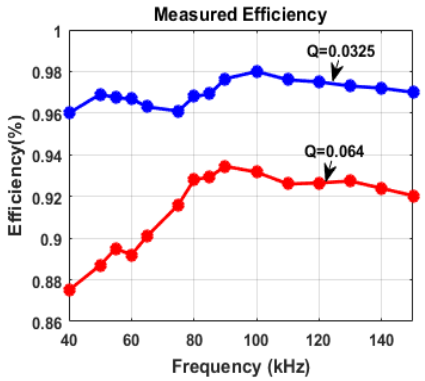
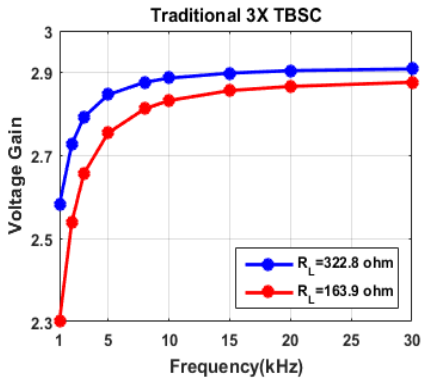
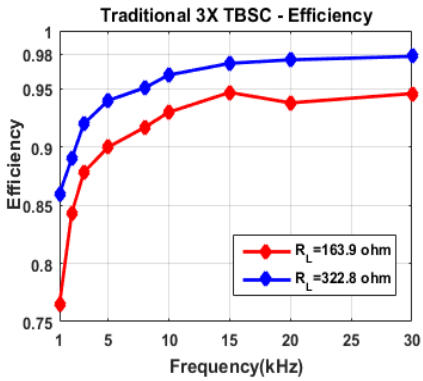


Fig. 1.18. 3X RTBSC- efficiency v.s frequency



(a) Gain curve



(b) Efficiency v.s. frequency

Fig. 1.19. Gain/efficiency curve of 3X TBSC

A voltage feedback loop is then added by TMS320F28335. In the closed loop test, the output voltage is regulated to be 120V, while the input voltage or load current is varied. The converter is ensured to be operating in $1 < \mathrm{F} < 2$ by proper selection of upper/lower limit of f_s. The practical lower limit can be obtained from Fig. 1.16, in which the current waveform is a pure sinusoidal wave, i.e. $f_r = 80kHz$. Then the upper limit is $2f_r = 160kHz$.

Fig. 1.20 shows the input-voltage range when V_{out} is regulated to be 120V. The left y axis represents the input voltage, while the right one stands for the efficiency at this input voltage value. The blue color is denoted as lighter load (Q=0.0325, $I_{load} = 0.37A$), at which the input-voltage range is 42.8~63V, but the efficiency is higher due to less conduction loss. The red color is denoted as heavier load (Q=0.064, $I_{load} = 0.73A$), at which the input-voltage range is 45 ~100V. As noted, the efficiency is well above 91%, even though the input voltage varies widely.

Fig. 1.21 shows the converter efficiency versus output power. V_{in} is 50V and V_{out} is regulated to be 120V. As shown, the peak efficiency is 98.3% at 23W and then the efficiency is decreasing to 90.7% at 140W. The estimated power loss distribution at 90W is shown in Table 1.3. In practice, the transistors can be regarded as ZVS turn-off due to its parasitic

capacitance. Therefore with soft-switching operation of transistors and diodes, switching loss is estimated to be zero and only conduction loss exists. As listed, the loss of the diodes is dominant and the loss of resonant inductor is the second highest.

Table 1.3 Power loss distribution of 3x RTBSC prototype

Device	**ESR or V_f**	**RMS Current**	**Average Current**	**Power Loss**	**Power Loss Ratio**
$s_{1,2}$	31mΩ	2.4A	-	0.36W	5.9%
$D_{1\sim4}$	0.8V	-	1.2A	3.84W	62.5%
$C_{r1,2}$	100mΩ	1.7A	-	0.58W	9.4%
L_r	100mΩ	3.4A	-	1.2W	19.5%
$C_{1a,1b}$	100mΩ	0.9A	-	0.16W	2.7%

Fig. 1.22 shows the line regulation curve and load regulation curve under the closed-loop. From Fig. 1.22(a), the RTBSC can provide line regulation against input voltage changes under different load conditions, and the output voltage can maintain at about 120V. From Fig. 1.22(b), the RTBSC can provide load regulation against load changes, and the voltage gain can maintain at about $120\text{V}/50\text{V} = 2.4$.

Fig. 1.23 shows the waveforms of load transient response. In Fig. 1.23(a), V_{in} is set to be 50V. When the load current is switched from $0.19A$ to $0.34A$ with a slew rate of $3.8 \times 10^4 A/s$, V_{out} is regulated back to 120V after about 50ms. Similarly, when the load current is switched from 0.34A to 0.19A, the regulation time is about 70ms, shown in Fig. 1.23(b).

Fig. 1.24 shows the waveforms of line transient response. In Fig. 1.24(a), the load current is fixed at 0.19A. When V_{in} is switched from 50V to 52V with a slew rate of $9.71 \times 10^2 V/s$, V_{out} is regulated back to 120V after about 70ms. Similarly, when V_{in} is switched from 50V to 48V with a slew rate of $5.22 \times 10^2 V/s$, the regulation time is about 50ms, as shown in Fig. 1.24(b).

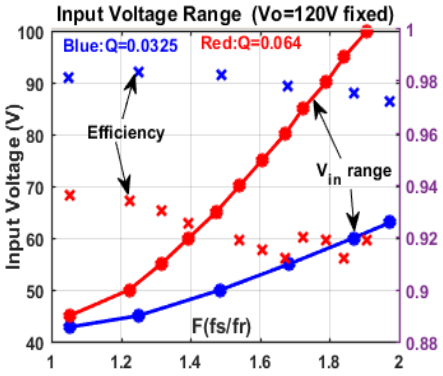


Fig. 1.20. Input voltage range

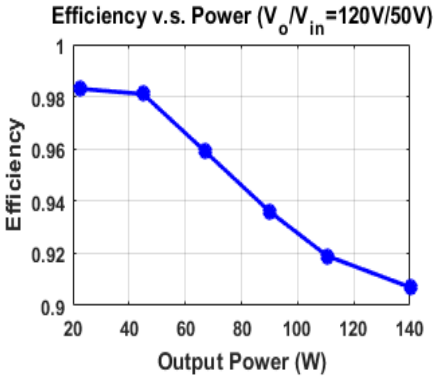
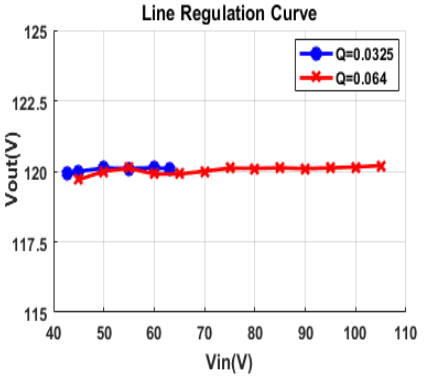


Fig. 1.21. Efficiency v.s. power



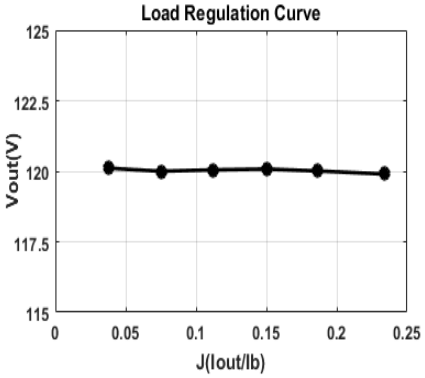
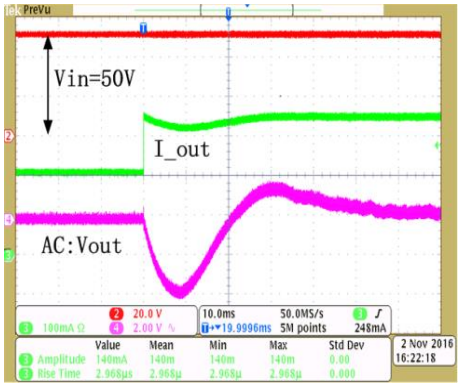
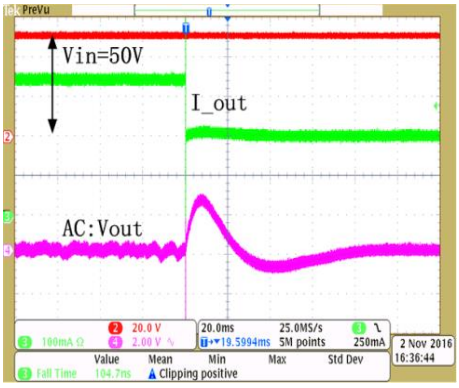


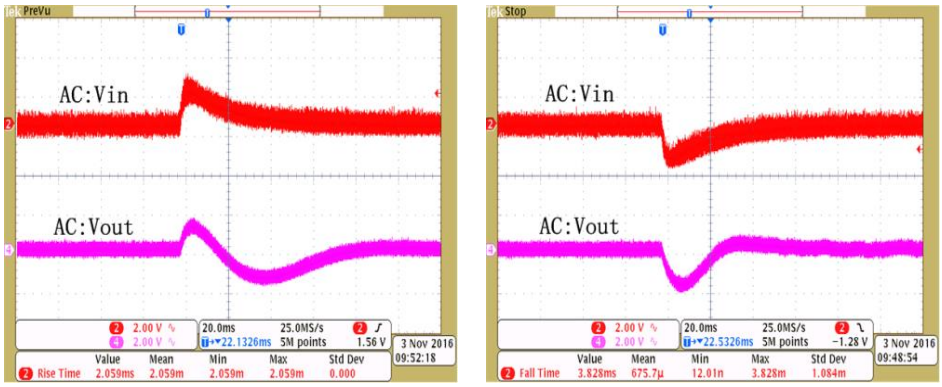
Fig. 1.22. (a) Line regulation curve (b) Load regulation curve





(a)Up loading current (b)Down loading current

Fig. 1.23. Load transient response of 3X RTBSC



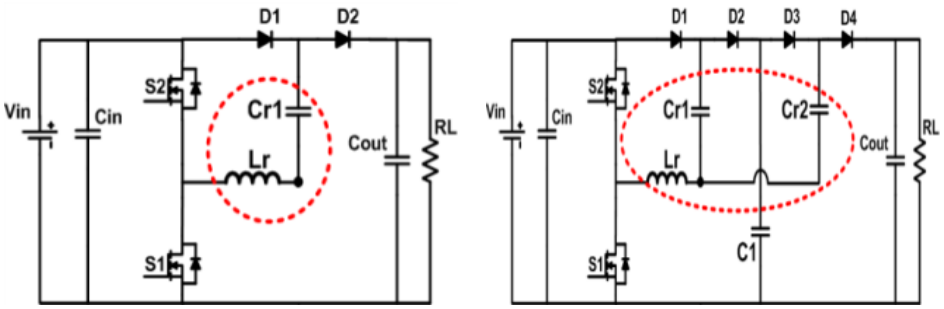
(a)Up input voltage (b)Down input voltage

Fig. 1.24. Line transient response of 3X RTBSC

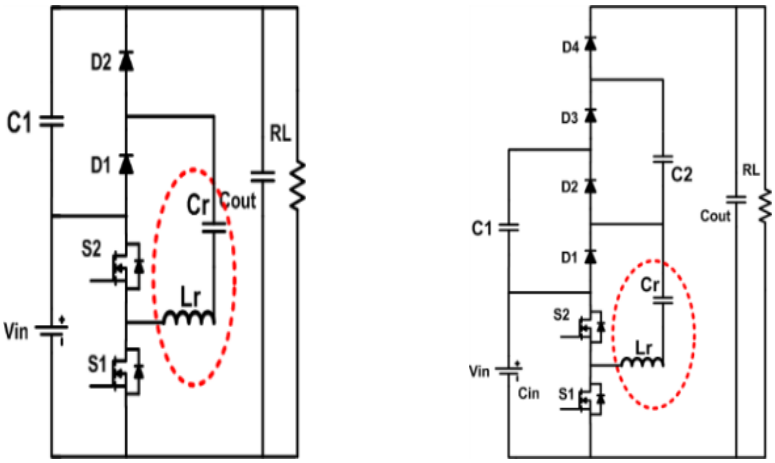
1.6 Topology Extension and Comparison

1.6.1 Topology Extension

The resonant tank and operation principle can be adapted to some other conventional SCC topologies, shown in Fig. 1.25. The resonant tank is highlighted in a red circle. The operation principle is similar to that of the RTBSCs. The continuous resonant current introduces good regulation capability and ZVS operation. The detailed analysis will be covered in our future work.



(a) 2X Dickson (b) 3X Dickson



(c) 2X Ladder (d) 3X Ladder

Fig. 1.25. Variants of Resonant Switched-capacitor Converters

1.6.2 Topology Comparison

In this part, the component counts, voltage stress (VS) and some properties of the proposed RTBSC are compared with some previous works. All converters have the maximum gain of 3 and the component count comparison is given in Table 1.4. In addition, the comparison of VS on switches, diodes, capacitors and some other properties are summarized in Table 1.5.

As shown, the proposed RTBSC has low switch counts and low to intermediate capacitor counts, which is desirable as the cost of those components is typically high . In addition, the voltage stress on all switches, diodes and capacitors is low, equal to the input voltage V_{in}. However, the output of RTBSC is floating, so the control circuit and driving circuit design will require more effort. Furthermore, the diodes of RTBSC could be replaced by active switches to achieve bidirectional power flow, and the semiconductor counts are still lower than those listed bidirectional converters [5] [7] [8] [21].

Table 1.4 Component count comparison

Topology	Gain	Switch	Floating Switch	Diode	Intermediate Cap. Banks
Dickson[2]	3	2	1	4	3
SPC[4]	3	8	4	6	4
TBSC[34]	3	2	1	4	4
[5]	3	6	5	0	2
[7]	3	12	11	0	6
[8]	3	7	5	0	2
[21]	3	12	9	0	5
RTBSC	1~3	2	1	4	2
	+ 2 small resonant Cap. and 1 resonant inductor				

Table 1.5 Property comparison

Topology	Floating Output	Power Direction	VS on Switch	VS on Diode	VS on Cap.
Dickson[2]	No	Uni.	Vin	Vin	Vin/2Vin
SPC[4]	No	Uni.	Vin	Vin	Vin
TBSC[34]	Yes	Uni.	Vin	Vin	Vin
[5]	No	Bi.	Vin	N/A	Vin/2Vin
[7]	No	Bi.	Vin	N/A	Vin
[8]	No	Bi.	Vin/2Vin	N/A	Vin/2Vin
[21]	Yes	Bi.	Vin	N/A	Vin
RTBSC	Yes	Uni.	Vin	Vin	Vin

1.7 Conclusion

In this chapter, a family of RTBSCs with ZVS operation and a wide regulation range is proposed. The resonant tank is composed of one inductor and two small capacitors for all RTBSCs. Some comprehensive characteristics of this family including operation modes, voltage-gain curves, output characteristics, voltage/current stresses of resonant tank are analyzed over 0.5<F<2. When 1<F<2, the family of RTBSC features ZVS operation and good regulation capability. In practice, the converter is ensured to be operating in this region referred to the derived gain curves and output characteristics. A 3X RTBSC prototype with peak efficiency of 98.3% was designed and built. The analysis is verified by both simulation and experimental results. The proposed converter family is suitable for wide-voltage-gain-range, high-frequency-operation and low-power-level applications.

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CHAPTER 2: Analysis and Design of the Ladder Resonant Switched-Capacitor Converters for Regulated Output Voltage Applications

2.1 Introduction

The traditional Ladder SCC with hard-switched operation is well known [1], whose line regulation capability is poor, because its conversion ratio is predetermined by the configuration. Its resonant configurations can be achieved by adding a resonant inductor and substituting a bulky capacitor bank with a much smaller resonant capacitor as shown in section 2.3. In practice, the Ladder RSC consists of two parts: series resonant inverter (SRI) and the voltage multiplier circuit. So it can be regarded as one type of "series resonant inverter fed voltage multiplier based transformer less dc-dc converter"**.**

In this chapter, the Ladder RSCs are analyzed to find the optimized operation region. It's demonstrated that, by operating above the resonance, ZVS turn-on is ensured for transistors and ZCS operation is guaranteed for all diodes, regardless of the load current. In addition, the voltage-gain range is increased significantly, which means the line regulation range is wide for regulated output voltage applications. In the closed-loop design, the instability issue of transition between DCM and CCM can be avoided. Moreover, the voltage/current stress of the resonant tank is reduced, comparing to that below the resonance. The converter operation modes, voltage-gain curves, output characteristics and the voltage/current stress of the resonant tank for the Ladder RSCs are analyzed in details. A 3X Ladder RSC prototype for a fuel injector application was designed in the optimized operation region to verify the analyses. The contents in this chapter have been published in the journal paper [2].

2.2 Nomenclature

$\boldsymbol{f_r}$:Resonant frequency;

$\boldsymbol{f_s}$:Switching frequency;

$\mathbf{C_r}$:Resonant capacitance; $\mathbf{C_{1,2,\ldots N}}$:Intermediate capacitors;

$\mathbf{L_r}$:Resonant inductance;

$\mathbf{S_{1,2}}$:MOSFETs;

$\mathbf{D_{1,2,\ldots N}}$:Power diodes;

$\boldsymbol{V_{cr}(t)}$:Voltage across the resonant capacitor;

$\boldsymbol{V_{cr\_max}}$, $\boldsymbol{V_{cr\_min}}$:Maximum and minimum values of $V_{cr}(t)$;

$\boldsymbol{M_{cr\_max}}$: Normalized maximum value of $V_{cr}(t)$;

$\boldsymbol{M_{cr\_min}}$:Normalized minimum value of $V_{cr}(t)$;

$\boldsymbol{V_c}$:Constant voltage value across the intermediate capacitors;

$\boldsymbol{V_{in}}$, $\boldsymbol{V_o}$:Input and output voltage;

M: voltage gain of V_o to V_{in};

$\boldsymbol{V_{s\_cr}}$:Voltage stress of the resonant capacitor C_r;

$\boldsymbol{V_{s\_s1,2}}$: Voltage stress of transistors $S_{1,2}$;

$\boldsymbol{V_{s\_D1,2..N}}$: Voltage stress of diodes $D_{1,2,\ldots N}$;

$\boldsymbol{i_{Lr}(t)}$: Resonant inductor current;

$\boldsymbol{i_{s1,2}(t)}$, $i_{D1,2\ldots N}(t)$:Current flowing through $S_{1,2}$, $D_{1,2,\ldots N}$;

$\boldsymbol{I_b}$:Current base;

J :Normalized output current;

$\mathbf{R_L}$:Load resistance;

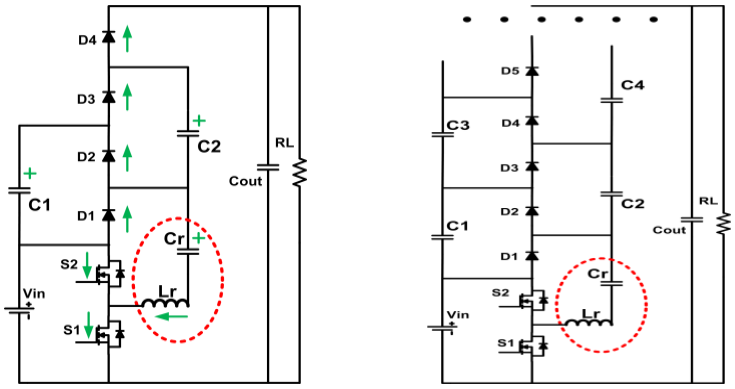
$\boldsymbol{J_{Lr\_rms}}$:Normalized RMS current value of L_r.

2.3 Operation Modes and Voltage Gain

The topologies of 3X and N-X Ladder RSCs are shown in Fig. 2.1. In this section, a 3X Ladder RSC in Fig. 2.1 (a) is exemplified to derive the voltage gain curve and then the derivation is extended to N-X Ladder RSCs.

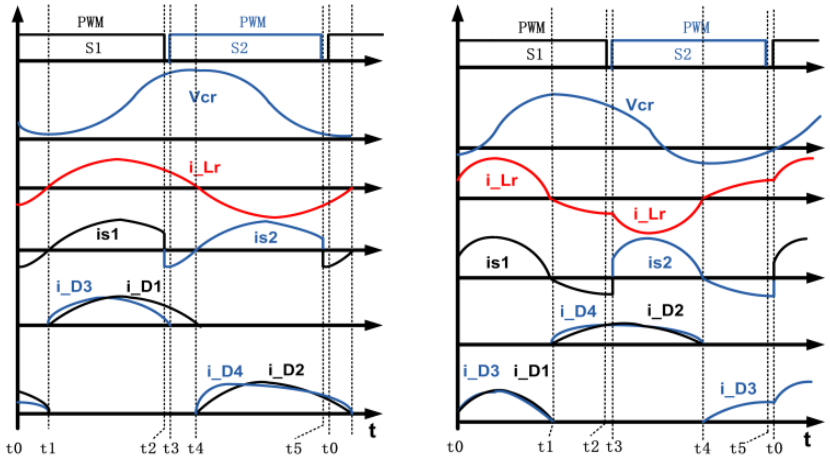
In the circuit, S_1 and S_2 are MOSFETs with internal anti-parallel diodes. The resonant tank - highlighted in the dashed circle - is composed of an inductor L_r and a capacitor C_r. Capacitors C_1 and C_2 work as charge banks with large capacitances. The duty cycle of transistor S_1 and S_2 is fixed at 0.5 and their driving signals are complimentary with a short dead-time. The defined positive directions are highlighted in green arrows as shown in Fig. 2.1 (a).

Several assumptions are made. The capacitances of C_1 and C_2 are large, so voltages on C_1 and C_2 are considered to maintain at a constant value V_c in one switching cycle. Similarly, the output voltage is regarded as a constant V_o. ESRs of capacitors, parasitic components of switches and forward voltage of diodes are neglected. The dead-time is ignored.

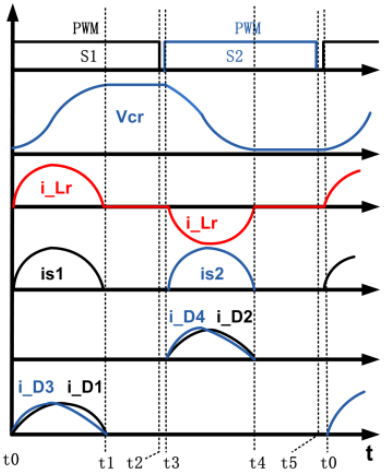


(a) 3X Ladder RSC (b) N-X Ladder RSC

Fig. 2.1. Topologies of the Ladder RSCs

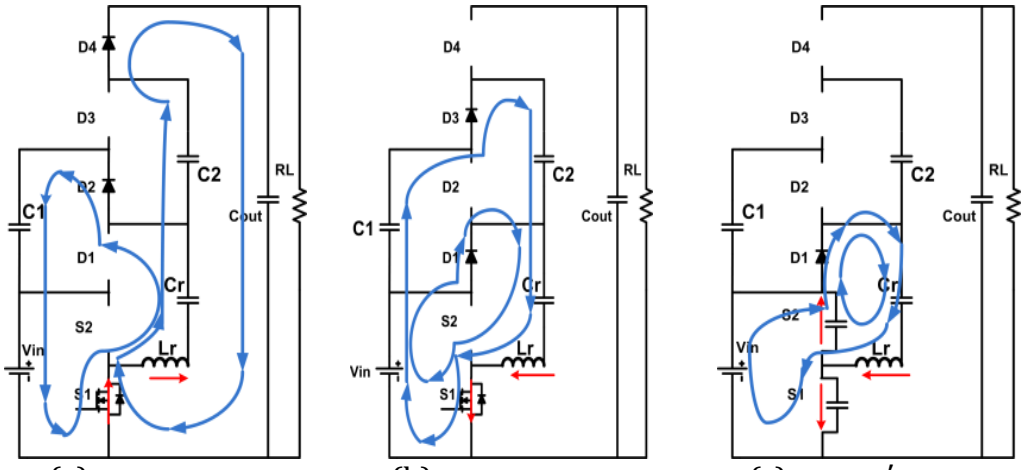


(a) $CCM_{1<F<2}$ (b) $CCM_{0.5<F<1}$

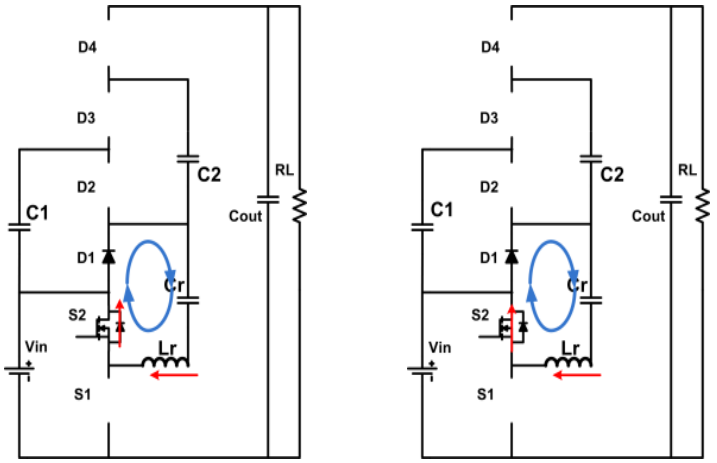


(c) $DCM_{0.5<F<1}$

Fig. 2.2. Operating waveforms in different modes – 3X Ladder RSC



(a) $t_0 - t_1$ (b) $t_1 - t_2$ (c) $t_2 - t_2'$



(d) $t_2{}' - t_3$ (e) $t_3 - t_4$

Fig. 2.3. Switching states of 3X Ladder RSC in $CCM_{1<F<2}$

2.3.1 Analysis of 3X Ladder RSC

2.3.1.1 Operation Region $f_r < f_s < 2f_r$

When $f_r < f_s < 2f_r$, the transistors are ZVS turned on and diodes are ZCS turned on/off. The output of the converter can be regulated well by frequency modulation against line or load variations. The typical operating waveforms and the switching states during the first half cycle are shown in Fig. 2.2(a) and Fig. 2.3. This operation mode is defined as $CCM_{1<F<2}$.

First, resonant current and voltage are obtained accordingly.

$[t_0 - t_1]$: Before t_0, $i_{Lr}(t)$ is negative. At t_0, transistor S_1 is turned on with ZVS operation. The diodes $D_{2,4}$ will start conducting the resonant current with ZCS turn-on as Fig. 2.3(a). In this state, there are two charging loops denoted in blue arrows.

The KVL and KCL equations are obtained as:

$$L_r \frac{di_{Lr}(t)}{dt} + V_{cr}(t) - V_C - V_{in} = 0 \quad (1)$$

$$L_r \frac{di_{Lr}(t)}{dt} + V_{cr}(t) + V_C - V_o = 0 \quad (2)$$

$$C_r \frac{dV_{cr1}(t)}{dt} = i_{Lr}(t) \quad (3)$$

From Fig. 2.2(a), the boundary conditions are:

$$i_{Lr}(t_1) = 0, V_{cr}(t_1) = V_{cr\_min} \tag{4}$$

Based on (1)-(4), the following expressions are obtained:

$$i_{Lr}(t) = -(V_{cr\_min} - V_C - V_{in})\sqrt{\frac{C_r}{L_r}} sin2\pi f_r(t - t_1) \tag{5}$$

$$V_{cr1}(t) = (V_{in} + V_C) + (V_{cr\_min} - V_C - V_{in}) \times cos2\pi f_r(t - t_1)$$

$$\text{where } f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{6}$$

$$V_o = 2V_C + V_{in} \tag{7}$$

$[t_1 - t_2]$: At t_1, $i_{Lr}(t)$ resonates to zero. The $i_{D2,D4}(t)$ becomes zero, so diodes $D_{2,4}$ are turned off with ZCS operation. Meantime, $V_{cr}(t)$ reaches the minimum value V_{cr_min}. Afterwards, $i_{Lr}(t)$ is positive and diodes $D_{1,3}$ will conduct the resonant current with ZCS turn-on as Fig. 2.3(b). With the similar method, the resonant current and voltage are obtained:

$$i_{Lr}(t) = -(V_{cr\_min} - V_{in})\sqrt{\frac{C_r}{L_r}} sin2\pi f_r(t - t_1) \tag{8}$$

$$V_{cr}(t) = V_{in} + (V_{cr\_min} - V_{in}) cos2\pi f_r(t - t_1) \tag{9}$$

$[t_2 - t_4]$: This interval is composed of two parts: $t_2 - t_3$ and $t_3 - t_4$. At t_2, transistor S_1 is turned off with ZVS operation due to the parasitic capacitance C_{ds1}, and then the loop current will charge C_{ds1} and discharge C_{ds2} till t_2', shown in Fig. 2.3(c). The parasitic capacitance is so small and this interval is very short, which is neglected in steady-state calculation. After t_2', the voltage across C_{ds2} is discharged to zero and the internal anti-parallel diode of S_2 starts conducting current, shown in Fig. 2.3(d). At t_3, transistor S_2 is turned on with ZVS operation. The loop current starts conducting through the transistor

channel. At t_4, $i_{Lr}(t)$ resonates to zero. Diode D_1 is turned off with ZCS operation. Meantime, $V_{cr}(t)$ reaches the maximum value V_{cr_max}. After t_4, the next half switching cycle starts and the operation principle is similar.

In this interval, the resonant current and voltage are:

$$i_{Lr}(t) = -V_{cr\_max}\sqrt{\frac{C_r}{L_r}}sin2\pi f_r(t - t_4) \tag{10}$$

$$V_{cr}(t) = V_{cr\_max}cos2\pi f_r(t - t_4) \tag{11}$$

At t_2, the values of resonant current and voltage derived in $[t_1 - t_2]$ should be equal to those derived in $[t_2 - t_4]$. In addition, both the resonant current and voltage are composed of two different parts of sinusoidal waveforms and the overall frequency is equal to the switching frequency if dead-time is neglected, i.e.:

$$t_2 - t_0 = t_4 - t_1 = \frac{1}{2}\frac{1}{f_s} \tag{12}$$

Based on (8)-(12), the following expression is calculated as:

$$cos\frac{f_r}{f_s}\pi = \frac{V_{cr\_min}^2 - 2V_{in}V_{cr\_min} + V_{cr\_max}^2}{2V_{cr\_min}V_{cr\_max} - 2V_{cr\_max}V_{in}} \tag{13}$$

Secondly, the expression of output voltage is derived.

Based on Fig. 2.2(a) and 2.3(b), at t_1^+:

$$V_{in} - V_{cr\_min} - L_r\frac{di_{Lr}(t)}{dt}_{|t=t_1^+} = 0 \tag{14}$$

Similarly, at t_4^+:

$$V_{in} + V_{cr\_max} + V_C - V_o + L_r\frac{di_{Lr}(t)}{dt}_{|t=t_4^+} = 0 \tag{15}$$

From Fig. 2.2 (a), the slopes of resonant current at t_1^+ and t_4^+ are opposite:

$$\frac{di_{Lr}(t)}{dt}_{|t=t_1^+} = -\frac{di_{Lr}(t)}{dt}_{|t=t_4^+} \tag{16}$$

As a result, the output is obtained based on (14) – (16):

$$V_o = (V_{cr\_min} + V_{cr\_max}) + V_C \tag{17}$$

With the expressions of (7) and (17), the following relationships can be derived:

$$V_{in} + V_c = V_{cr\_max} + V_{cr\_min} \tag{18}$$

$$V_o = 2(V_{cr\_min} + V_{cr\_max}) - V_{in} \tag{19}$$

Thirdly, the equation of charge balance on C_r is figured out:

$$C_r(V_{cr\_max} - V_{cr\_min}) = 2\frac{V_o}{R_L}\frac{1}{f_s} \tag{20}$$

For simplicity, assuming $d = cos\frac{f_r}{f_s}\pi$ and $k = C_r R_L f_s$. According to (13) (19) (20), the following equations are derived:

$$M_{cr\_min} = \frac{V_{cr\_min}}{V_{in}} = \frac{(1-d)k^2+(A-2d-6)k+24d+24-4A)}{2[(1-d)k^2+16d+16]} \tag{21}$$

$$M_{cr\_max} = \frac{V_{cr\_max}}{V_{in}} = \frac{(k+4)M_{cr\_min}-2}{k-4} \tag{22}$$

$$M = \frac{V_o}{V_{in}} = \frac{k[(1-d)k+2A-8d-8]}{(1-d)k^2+16d+16} \tag{23}$$

$$A=\sqrt{(d^2-2d+1)k^2+(4d^2-4)k+4d^2+32d+28}$$

However, a special condition should be considered. The minimum voltage gain is 1. As a result, the voltage-gain curve maintains at 1 when (23) is smaller than 1. In this scenario, equation of charge balance (20) will not be held, while (13) and (19) are still true. This special condition is defined as $Fixed - Gain_{1<F<2}$ ($FG_{1<F<2}$).

According to (13)(19), the following equations can be derived:

$$M_{cr\_min} = 1 - \sqrt{\frac{1}{2(1+d)}} \tag{24}$$

$$M_{cr\_max} = \sqrt{\frac{1}{2(1+d)}} \tag{25}$$

$$M = \frac{V_o}{V_{in}} = 1 \tag{26}$$

2.3.1.2 Operation Region $\frac{1}{2}f_r < f_s < f_r$

When $0.5f_r < f_s < f_r$, the transistors are hard-switched and suffer from capacitive turn-on losses and dv/dt noise. This operation mode is defined as $CCM_{0.5<F<1}$ and the operating waveforms are shown in Fig. 2.2(b).

Similarly, by solving the KVL and KCL equations in $[t_0 - t_1]$ and $[t_1 - t_3]$, the following expression is derived as:

$$cos\frac{f_r}{f_s}\pi = \frac{V_{cr\_min}^2 - 2V_{in}V_{cr\_max} + V_{cr\_max}^2}{2V_{cr\_min}V_{cr\_max} - 2V_{cr\_min}V_{in}} \tag{27}$$

With (19)(20)(27), the following equations can be obtained:

$$M_{cr\_min} = \frac{(1-d)k^2 + (B+6d+2)k - 8d - 8 - 4B)}{2[(1-d)k^2 + 16d + 16]} \tag{28}$$

$$M_{cr\_max} = \frac{(k+4)M_{cr\_min} - 2}{k-4} \tag{29}$$

$$M = \frac{V_o}{V_{in}} = \frac{k[(1-d)k + 2B + 8d + 8]}{(1-d)k^2 + 16d + 16} \tag{30}$$

$$\text{B}=\sqrt{(d^2 - 2d + 1)k^2 + (4 - 4d^2)k + 4d^2 + 32d + 28}$$

Two special conditions should be considered.

First, the minimum voltage gain is still 1. This condition is defined as $FG_{0.5<F<1}$.

According to (19) (27), the following equations are derived:

$$M_{cr\_min} = -\sqrt{\frac{1}{2(1+d)}} \tag{31}$$

$$M_{cr\_max} = 1 + \sqrt{\frac{1}{2(1+d)}} \tag{32}$$

$$M = \frac{V_o}{V_{in}} = 1 \tag{33}$$

Secondly, over a certain frequency range, the gain curve will maintain at the maximum gain 3, which means the regulation capability is lost. In this unregulated region - defined as - $DCM_{0.5<F<1}$, the resonant current will go to DCM as shown in Fig. 2.2 (c). The conventional ZCS RSCs are operating in this mode [3]-[5]. However, the inability to provide regulation against line/load changes eliminates the possibility for regulated output voltage applications. The boundary between $CCM_{0.5<F<1}$ and $DCM_{0.5<F<1}$ can be derived as follows.

In $DCM_{0.5<F<1}$, the following equations can be obtained:

$$M_{cr\_min} = \left(1 - \frac{3}{k}\right) \tag{34}$$

$$M_{cr\_max} = \left(1 + \frac{3}{k}\right) \tag{35}$$

$$M = \frac{V_o}{V_{in}} = 3 \tag{36}$$

If M_{cr_min} is larger than 0, the resonant tank cannot start resonating in the reverse direction and thus the resonant current goes to DCM. As a result, the constraint of $DCM_{0.5<F<1}$ is $M_{cr\_min} > 0$, i.e.:

$$k > 3 \tag{37}$$

2.3.1.3 Voltage-gain Curve

In order to plot the voltage-gain curve, another two parameters are defined as follows:

$$\text{Frequency Ratio: F} = \frac{f_s}{f_r}\text{; Quality Factor: Q} = \frac{\sqrt{L_r/C_r}}{R_L} \tag{38}$$

As a result, the relationships between d, k and F, Q are:

$$d = cos\frac{f_r}{f_s}\pi = \cos(\frac{\pi}{F})\text{; } k = C_r R_L f_s = \frac{F}{Q}\frac{1}{2\pi} \tag{39}$$

For 3X Ladder RSC, some important formulas and boundary constraints are summarized in Table 2.1 and the voltage-gain curve of 3X Ladder RSC is plotted in Fig. 2.4. As shown, when 0.5<F<1, the converter may enter $DCM_{0.5<F<1}$ and lose regulation capability in case of small Q. If Q<0.0265, the converter will be always operating in $DCM_{0.5<F<1}$ over 0.5<F<1. In the closed loop design, this may cause instability issue when the converter switches between DCM and CCM. However, when 1<F<2, the inductor current maintains continuous and no stability issue needs to be concerned.

Table 2.1. Key Formulas for 3X Ladder RSC

Freq.	**0.5<F<1**			**1<F<2**	
Mode	**$FG_{0.5<F<1}$**	**$CCM_{0.5<F<1}$**	**$DCM_{0.5<F<1}$**	**$CCM_{1<F<2}$**	**$FG_{1<F<2}$**
Boundary	(30)<1	(30)>1 F<6πQ	(30)>1 F>6πQ	(23)>1	(23)<1
M_{cr_min}	(31)	(28)	(34)	(21)	(24)
M_{cr_max}	(32)	(29)	(35)	(22)	(25)
M	1	(30)	3	(23)	1

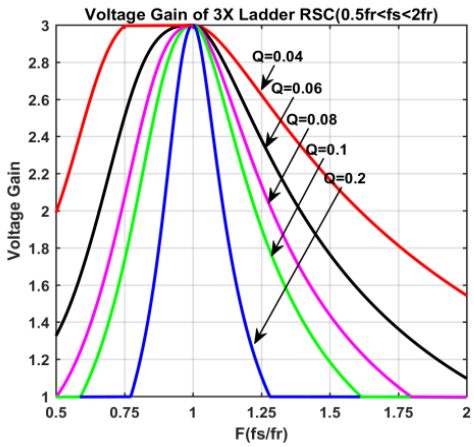


Fig. 2.4. Voltage gain of 3X Ladder RSC ($0.5 < \mathrm{F} < 2$)

2.3.2 Analysis of N-X Ladder RSC

The topology of N-X Ladder RSC is shown in Fig. 2.1(b). Since the resonant tank does not change, the resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$ is the same for all Ladder RSCs.

When$1 < \mathrm{F} < 2$, the expression of (13) is always the same. The only differences are the equations of output voltage and charge balance:

$$V_o = (N-1)(V_{cr\_max} + V_{cr\_\min}) - (N-2)V_{in} \tag{40}$$

$$\mathrm{C_r}(V_{cr\_max} - V_{cr\_min}) = (\mathrm{N}-1)\frac{\mathrm{V_o}}{\mathrm{R_L}}\frac{1}{f_s} \tag{41}$$

By solving (13)(40)(41), the voltage gain of N-X Ladder RSC when $1 < \mathrm{F} < 2$ can be derived. Note that the minimum voltage gain is 1.

When $0.5 < \mathrm{F} < 1$, the expression of (27) is always the same. By solving (27)(40)(41), the voltage gain of N-X Ladder RSC when $0.5 < \mathrm{F} < 1$ can also be derived. In addition, the minimum voltage gain is 1, and the maximum voltage gain is N. The constraint of $DCM_{0.5<F<1}$ is $0.5 < N(N-1)\pi\mathrm{Q} < \mathrm{F} < 1$.

2.4 Output Characteristics

In this section, the output characteristics of Ladder RSCs will be analyzed. A 3X Ladder RSC is analyzed as an example and then the analysis is extended to N-X Ladder RSCs.

As mentioned in the previous section, in two special conditions when the voltage gain is fixed at 1 ($FG_{0.5<F<1}, FG_{1<F<2}$) or when the converter goes into DCM ($DCM_{0.5<F<1}$), the voltage gain will not change no matter the load current or switching frequency is changing. As a result, the output characteristic in the two special conditions can be represented by a straight line and will not be discussed in this section. Only the conditions in $CCM_{0.5<F<1}$ and $CCM_{1<F<2}$ are discussed.

2.4.1 Output Characteristics of 3X Ladder RSC

At first, several parameters are defined as follows:

$$\text{Current base: } I_b = \frac{V_{in}}{\sqrt{L_r/C_r}} \tag{42}$$

$$\text{Normalized output current: J} = \frac{V_o/R_L}{I_b} \tag{43}$$

According to the definition of normalized output current,

$$\text{J} = \frac{V_o/R_L}{I_b} = \frac{M}{2\pi f_r C_r R_L} \tag{44}$$

In $CCM_{1<F<2}$ and $CCM_{0.5<F<1}$, equation (20) is always held. Based on (20) and (44),

$$\text{J} = \frac{F}{4\pi}(M_{cr\_max} - M_{cr\_min}) \tag{45}$$

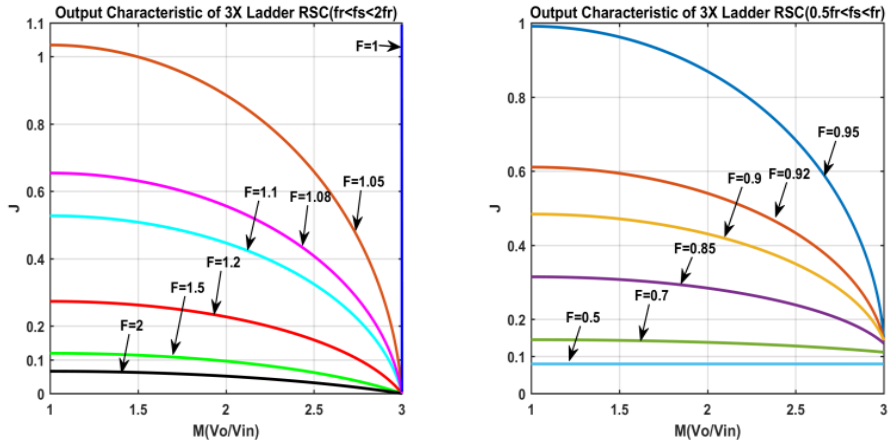
When $1 < \text{F} < 2$, according to (13)(19) and (45),

$$J = \frac{F}{4\pi}\left(\sqrt{\frac{-M^2+2M+d(1-2M+M^2)+7}{4(d+1)}} - 1\right) \tag{46}$$

When $0.5 < \text{F} < 1$, according to (19)(27) and (45),

$$J = \frac{F}{4\pi}\left(\sqrt{\frac{-M^2+2M+d(1-2M+M^2)+7}{4(d+1)}} + 1\right) \tag{47}$$

Based on (46)(47), the output characteristic of 3X Ladder RSC is plotted in Fig. 2.5. Referred to Fig. 2.5, one can know how to regulate frequency ratio (F) to maintain the voltage-gain (M) if the normalized output current (J) is changed. For example, a fixed M=2 is desired for a 3X Ladder RSC. Under J=0.9, the converter can be operating either above the resonance (F≈1.05) or below the resonance (F≈0.95). Then the load current is decreased to J=0.1, the frequency ratio should be regulated to F≈1.5 or F ≈ 0.55 to maintain the voltage gain, according to Fig. 2.5. However, one should be very careful that the converter may enter DCM if the operating frequency is chosen to be below the resonance in case of light load (small Q). Once the converter enters DCM, Fig. 2.5(b) is no long applicable. In contrast, this unfavorable scenario can be avoided if the operating frequency is chosen to be above the resonance since the converter is always in CCM.



(a) 1<F<2 (b) 0.5<F<1

Fig. 2.5. Output characteristics of 3X Ladder RSC

2.4.2 Output Characteristics of N-X Ladder RSC

For N-X Ladder RSC, the expression of normalized load current is the same as (45). According to (41) and (45),

$$\mathrm{J} = \frac{F}{2(N-1)\pi}\left(M_{cr\_max} - M_{cr\_min}\right) \tag{48}$$

When $1 < F < 2$, the expression of (13) is always the same, while the equation of the output voltage is different, as given in (40). According to (13)(40) and (48), the output characteristic curve can be derived.

When $0.5 < F < 1$, according to (27)(40) and (48), the output characteristic curve can be derived similarly.

2.5 Normalized Maximum Voltage of the Resonant Capacitor

In order to design the Ladder RSCs, a big concern is the maximum voltage value of the resonant capacitor. It directly affects the parameter selection of the converter. A 3X Ladder RSC is chosen as an example to derive its normalized maximum voltage value (M_{cr_max}) of the resonant capacitor.

By substituting (39) into the formulas in Table 2.1, M_{cr_max} in different operating conditions can be obtained. Considering the boundary constraints, the normalized maximum voltage value of the resonant capacitor for 3X Ladder RSC is plotted in Fig. 2.6. The black line, blue line, green line and red line represent M_{cr_max} in condition $FG_{0.5<F<1}/FG_{1<F<2}$,$CCM_{0.5<F<1}$, $DCM_{0.5<F<1}$ and $CCM_{1<F<2}$, respectively.

The voltage stress for the resonant capacitor can be obtained under different operating conditions. From Fig. 2.9, it's observed that the maximum voltage stress of resonant capacitor when 1<F<2 is lower than that when 0.5<F<1.

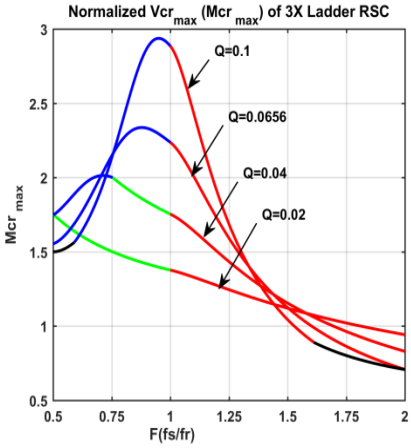


Fig. 2.6. Normalized maximum voltage of the resonant capacitor for 3X Ladder RSC

2.6 Normalized RMS Current of the Resonant Inductor

In the process of designing the Ladder RSCs, another important consideration is the RMS current value of the resonant inductor. From Fig. 2.2(a) (b), it can be assumed that the current waveform is a sinusoidal wave for simplicity, even though the real RMS value is smaller. But it will give more headroom to select the components. As for the $DCM_{0.5<F<1}$ in Fig. 2.2(c), the inductor current can be assumed as a periodic waveform composed of sinusoidal piecewise segments. A 3X Ladder RSC is chosen to derive its normalized RMS current value (J_{Lr_rms}) of the resonant inductor.

When 1<F<2, the equations of the current waveform in $FG_{1<F<2}$ and $CCM_{1<F<2}$ are same. The normalized RMS value of the sinusoidal wave is calculated according to (8) and (42):

$$J_{Lr\_rms} = \left| \frac{(V_{in} - V_{cr\_min})\sqrt{\frac{C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}} \right| = \frac{1}{\sqrt{2}}(1 - M_{cr\_min}) \tag{49}$$

Similarly, when 0.5<F<1, J_{Lr_rms} of the resonant inductor in $FG_{0.5<F<1}$ and $CCM_{0.5<F<1}$ is calculated as:

$$J_{Lr\_rms} = \left| \frac{(V_{cr\_max} - V_{in})\sqrt{\frac{C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}} \right| = \frac{1}{\sqrt{2}}(M_{cr\_max} - 1) \tag{50}$$

In $DCM_{0.5<F<1}$, J_{Lr_rms} of the resonant inductor is:

$$J_{Lr\_rms} = \sqrt{F} \times \left| \frac{(V_{cr\_max} - V_{in})\sqrt{\frac{C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}} \right| = \frac{\sqrt{F}}{\sqrt{2}} (M_{cr\_max} - 1) \quad (51)$$

According to (49)-(51) and Table 2.1, J_{Lr_rms} of the resonant inductor for 3X Ladder RSC is plotted in Fig. 2.7. The black line, blue line, green line and red line represent J_{Lr_rms} in condition $FG_{0.5<F<1}/FG_{1<F<2}$,$CCM_{0.5<F<1}$, $DCM_{0.5<F<1}$ and $CCM_{1<F<2}$.

The current stress for the resonant inductor can be obtained for different operating conditions. Seen from Fig. 2.7, the maximum current stress of resonant inductor when 1<F<2 is lower than that when 0.5<F<1.

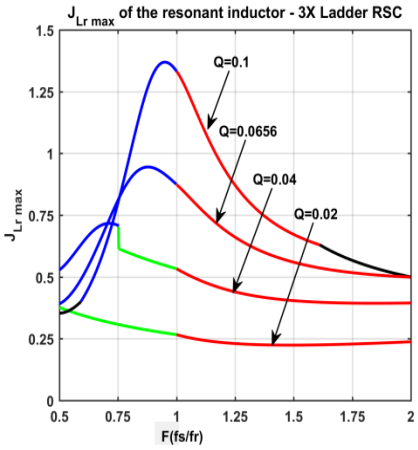


Fig. 2.7. Normalized maximum RMS current of the resonant inductor for 3X Ladder RSC

2.7 Optimized Operation Region

According to the aforementioned analysis, several advantages will be obtained by operating the Ladder RSCs above the resonant frequency (1<F<2).

(1) The transistors can be operated with ZVS turn-on and diodes can be operated with ZCS operation. The soft-switching operation makes it possible to decrease the component size by increasing the switching frequency, while not deteriorating the overall efficiency.

(2) The voltage-gain range is expanded significantly, so the output voltage will follow any change in the input voltage within a wide range, and satisfactory transient response can be achieved in case of load changes.

(3) The inductor current is always continuous, so the instability due to transition between DCM and CCM can be avoided in the closed-loop design.

(4) The voltage stress of the resonant capacitor and RMS current stress of the resonant inductor is lower.

Therefore, the Ladder RSCs are better to be operated above its resonant frequency for output voltage regulated applications.

2.8 Hardware Design and Experimental Results

2.8.1 Hardware Design

One possible application of the Ladder RSC is the Electronic Fuel Injection (EFI) for the engineering equipment. Its input voltage, which is supplied by lead acid batteries, can be varied from 30-50V. The output can be ranged from 90V to 120V for different applications of fuel injectors. The power level is typically below 150W. As a result, a 3X or a 4X Ladder RSC is a good candidate. In this part, a 3X Ladder RSC prototype with maximum output voltage 150V and maximum power 140W is designed for EFI applications.

With open-loop test, the input voltage will be fixed at 50V and then to measure the output voltage at different switching frequencies ($0.5<F<2$). Since the theoretical voltage-gain range is $1<M<3$, the output voltage is between 50-150V.

With closed-loop test, the output voltage is regulated to be fixed at 120V to meet the voltage requirement of the EFI. The converter is designed to be operating in the optimized region ($1<F<2$).

To begin with, the highest switching frequency $2f_r$ is chosen to be 152kHz, so the lowest switching frequency $0.5f_r$ and resonant frequency f_r are about 38kHz and 76kHz respectively. The resonant capacitors C_r are chosen to be 200nF. According to $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, the resonant inductor L_r is about 22uH.

In order to measure the voltage-gain curve, three power loads R_L - 640Ω, 320Ω and 160Ω - are chosen, decided by the power level (140W) of the EFI. As a result, the theoretical values of Qs are $Q = \frac{\sqrt{L_r/C_r}}{R_L} = 0.0164,\ 0.0328$ and 0.0656.

According to Fig. 2.3, the voltage stress $V_{s\_s1,2}$ of transistor S_1 and S_2 is equal to the input voltage, i.e. $V_{s\_s1,2} = V_{in}$. While for the voltage stress $V_{s\_D1,2,3,4}$ of diodes D_1 - D_4, it's equal to the maximum voltage value across C_1/C_2. As known, the maximum gain is 3, where V_c reaches its maximum value, i.e. $V_{s\_D1-D4} = V_{in}$. The voltage stress of the resonant capacitor V_{s_cr} can be figured out according Fig. 2.6, $V_{s\_cr} \approx 2.4V_{in}$.

The normalized RMS current value of the resonant inductor has been calculated in section 2.6. According to Fig. 2.7, the current stress of the resonant inductor $i_{s\_Lr} \approx 0.95 \times I_b$ (Q=0.0656). As a result, the current stress of the transistors is $i_{s\_s1,2} = \frac{\sqrt{2}}{2} i_{s_{Lr}}$, while the current stress of the diodes is $i_{s\_D1,2,3,4} \approx \frac{\sqrt{2}}{4} i_{s_{Lr}}$.

Based on the above analysis, components are selected and the specifications of the prototype are listed in Table 2.2.

Table 2.2. Prototype specifications of 3X Ladder RSC

Power Level	<140W	$C_{1,2}$	20uF
Input (V_{in})	40-120V	C_r	200nF
Output (V_o)	<150V	L_r	22uH
f_s	38-152kHz	f_r	76kHz
C_{in}	100uF	D_{1-4}	MBR10100G
C_{out}	100uF	$S_{1,2}$	FDPF390N15A

2.8.2 Experimental Results

In this part, a 3X Ladder RSC prototype was built based on the hardware design guideline. The open-loop experimental results are shown in Fig. 2.8 -2.12 and the closed-loop experimental results are shown in Fig. 2.14 and 2.15. In practice, three load resistances are measured to be 163.9Ω, 322.8Ω and 640.5Ω respectively, i.e. Q=0.064, 0.0325 and 0.0164.

From Fig. 2.8 to Fig. 2.10, Q is 0.0325 and the input voltage is fixed at 50V. In Fig. 2.8, f_s is 40kHz (0.5<F<1). In Fig. 2.8(a), transistor S_1 is hard-switched turned on with high dv/dt noise on V_{ds}, while the resonant current is in CCM. Fig. 2.8(b) shows the waveforms of resonant voltage and current, matching the waveforms of $CCM_{0.5<F<1}$ in Fig. 2.2(b)

In Fig. 2.9, f_s is 50kHz (0.5<F<1). From Fig. 2.9(a), transistor S_1 is ZCS turned on, because the resonant current is in DCM. Fig. 2.9 (b) shows the waveforms of resonant voltage and current. There exists a short period where the resonant current is zero and thus the resonant voltage is flat. This phenomenon matches the waveforms of $DCM_{0.5<F<1}$ in Fig. 2.2(c).

In Fig. 2.10, f_s is 79kHz. As shown, both the resonant inductor current and the resonant capacitor voltage are pure sinusoidal waves. So the practical boundary - resonant frequency - is 79kHz instead of 76kHz in theory. The boundary frequency could help set the lower/upper limit of the switching frequency while designing the closed loop scheme.

In Fig. 2.11, f_s is 100kHz (1<F<2). From Fig. 2.11(a), transistor S_1 is ZVS turned on, without any dv/dt noise on V_{ds}. In Fig. 2.11(b), the waveforms of resonant voltage and current match the waveforms of $CCM_{1<F<2}$ in Fig. 2.2(a). Fig. 2.11(c) shows the input current above the resonance.

The experimental gain curve is plotted in Fig. 2.12(a). The solid lines represent theoretical gain curves, while the dashed lines mean the experimental results. In the optimized operation region (1<F<2), for Q=0.0164, the voltage gain changes from 2.89 to 2.48; for Q=0.0325, the voltage gain changes from 2.86 to 1.86; for Q=0.064, the voltage gain changes from 2.77 to 1.08. In general, the experimental gain curves are pretty close to the theoretical analysis in part 2.3.1. The maximum gain is lower than the theoretical maximum gain 3 because of voltage drop on the diodes and on the parasitic resistance of the transistors.

Fig. 2.12(b) shows the measured efficiency with open loop. The peak efficiency is about 97.6% at 100kHz (Q=0.0164). The average efficiency above the resonance is 97.0%, 95.4% and 90.6% for Q=0.0164, 0.0325 and 0.064, while the average efficiency below the resonance is 94.7%, 93.4% and 89.5% respectively. In general, the efficiency above the resonant frequency is higher than that below the resonant frequency due to the ZVS operation and lower RMS current stress as analyzed

To make a comparison, a traditional 3X Ladder SC converter was built and tested. In Fig. 2.13, when the switching frequency is below 30kHz, the voltage gain can vary with the switching frequency in a relatively wide range. However, the converter efficiency is pretty low in this well-regulated region. Afterwards, the voltage gain can only change in a narrow range, even though the switching frequency is varied in a wide range from 30kHz to 150kHz. Obviously, the voltage-gain range of the 3X Ladder RSC is improved significantly within the same frequency range, while not deteriorating the efficiency.

The next step is to add the feedback loop by DSP TMS320F28335. The lower and upper switching frequency limit is set to 80kHz and 158 kHz to ensure the 3X Ladder RSC operate above the resonant frequency.

The circuit diagram of the feedback controller is shown in Fig. 2.14. The output voltage is sampled by the resistance divider followed by a RC filter and a voltage follower, which are used to eliminate the high frequency noise and influence of the following stage. A PI controller is applied to eliminate the error between the feedback signal and the reference. Then the switching frequency is varied within the lower/upper limit to regulate the output voltage.

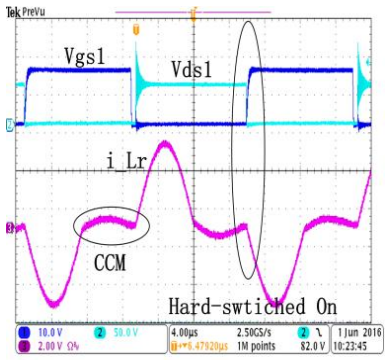
Fig. 2.15(a) shows the input-voltage range for a regulated output voltage application, whose output is regulated to be at 120V. The right y axis represents the input voltage at a certain load condition and a frequency ratio, while the left y axis represents the corresponding converter efficiency. At lighter load (Q=0.0325), the input-voltage range is 42.7-63.8V, in which the efficiency is well above 95%; at heavier load (Q=0.064), the input-voltage range is 43.9-105V, in which the efficiency is kept over 89%. For EFI applications, the input voltage is provided by several lead acid batteries in series. The typical value for 4 batteries in series is 48V. However, the batteries can be discharged to about 44V and charged to over 50V easily. As a result, the wide line regulation range of the Ladder RSCs could help ease this issue. If fewer batteries are used in series, more modular stages could be added to further boost the conversion ratio.

Fig. 2.15(b) shows the efficiency versus output power under different voltage ratios. When the voltage gain is 120V/45V=2.67, the peak efficiency is 97.7% at 22.4W and the minimum efficiency is 90.7% at 135W. When the voltage gain is 120V/50V=2.4, the peak

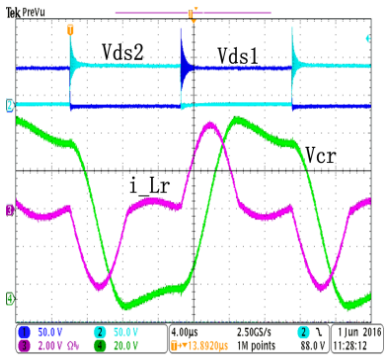
efficiency is 97.03% at 22.5W and the minimum efficiency is 90.5% at 135W. When the voltage gain is 120V/55V=2.18, the output can't be regulated to 120V at very light load, which could also be found from Fig. 2.12(a). But at heavier load, the efficiency is well above 90%.

Fig. 2.15(c) shows the line and load regulation curves of the 3X Ladder RSC. By operating above the resonance, the output voltage could be regulated at about 120V with small ripple (<2%) over wide line range or load range.

Fig. 2.16 shows the dynamic behavior of the converter. In Fig. 2.16(a), the input voltage is fixed at 50V and the load is switched from 322.8Ω to163.9Ω, while the output voltage is regulated to back to 120V after about 12ms. In Fig. 2.16(b), the input voltage is fixed at 50V and the load is switched from 163.9Ω to 322.8Ω, while the output voltage is regulated back to 120V after about 20ms. In Fig. 2.16(c), the load is fixed at 322.8Ω and the input voltage is switched from 45V to 60V, while the output voltage is regulated to maintain at 120V. The regulation time is about 70ms. In Fig. 2.16(d), the load is fixed at 322.8Ω and the input voltage is switched from 60V to 45V, while the output voltage is regulated back to 120V after about 40ms. The dynamic behaviors have proved the regulation capability of the 3X Ladder RSC against load and line changes.

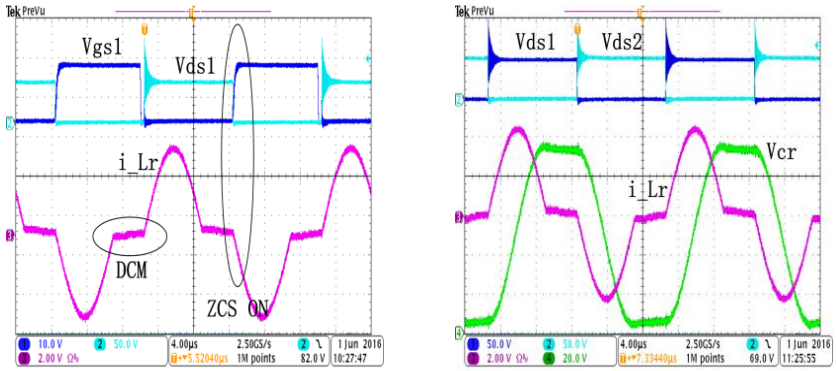


(a) V_{gs1}, V_{ds1}, i_{Lr}



(b) $V_{ds1}, V_{ds2}\ V_{cr}, i_{Lr}$

Fig. 2.8. Experimental waveforms at f_s=40kHz for 3X Ladder RSC



(a) V_{gs1}, V_{ds1}, i_{Lr} (b) $V_{ds1}, V_{ds2}\ V_{cr}, i_{Lr}$

Fig. 2.9. Experimental waveforms at f_s=50kHz for 3X Ladder RSC

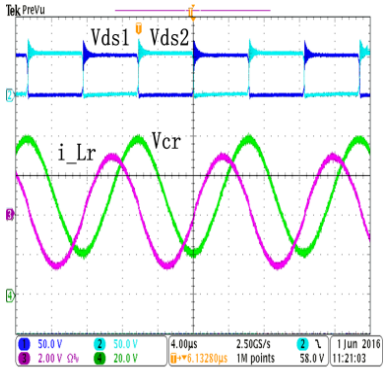
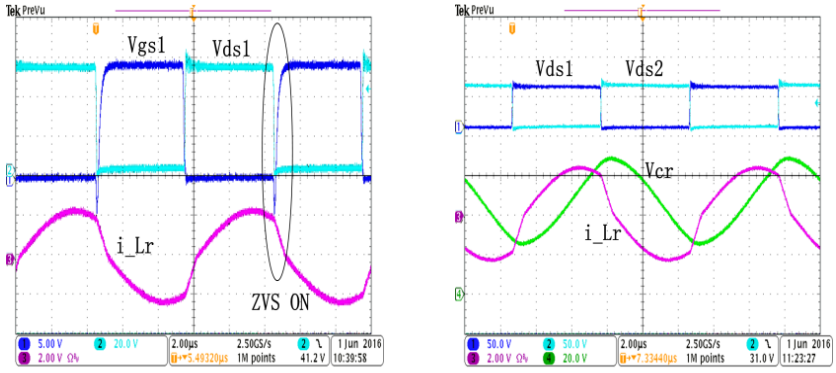
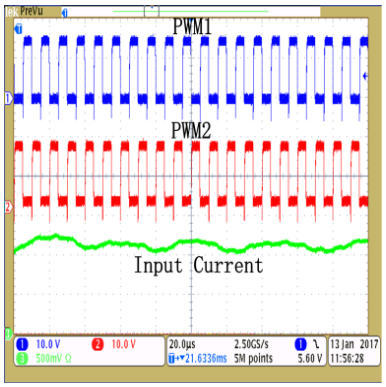


Fig. 2.10. Experimental waveforms at f_s=79kHz for 3X Ladder RSC（Boundary）

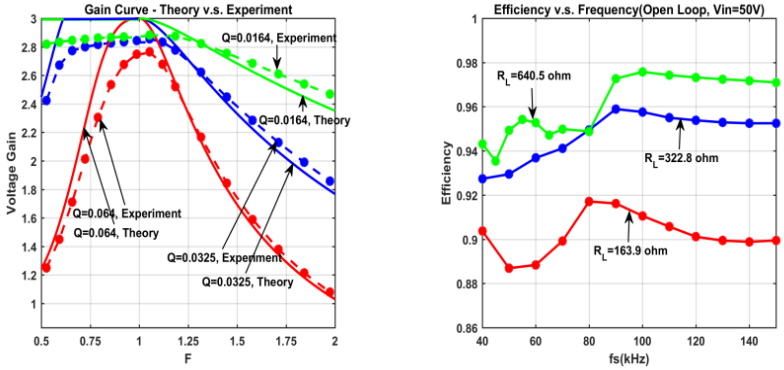


(a) V_{gs1}, V_{ds1}, i_{Lr} (b) $V_{ds1}, V_{ds2}\ V_{cr}, i_{Lr}$



(c) V_{gs1}, V_{gs2}, i_{in}

Fig. 2.11. Experimental waveforms at f_s=100kHz for 3X Ladder RSC



(a). Gain curve (b). Measured efficiency

Fig. 2.12. Experimental results of 3X Ladder RSC (Open-loop)

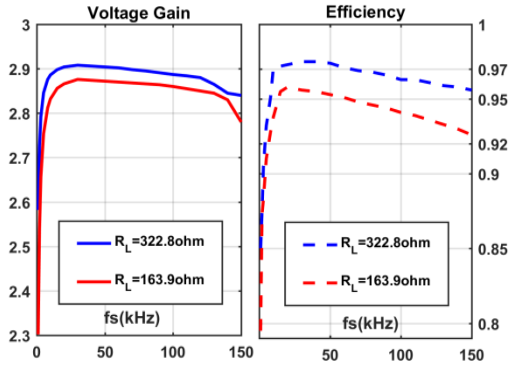


Fig. 2.13. Gain curve and efficiency of traditional 3X Ladder SCC

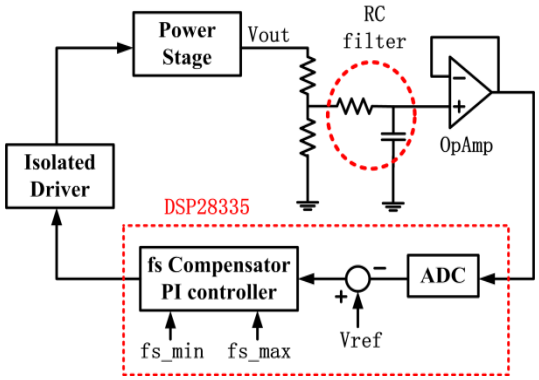
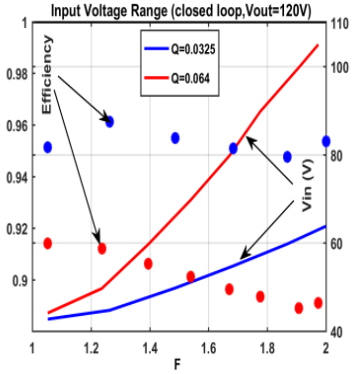
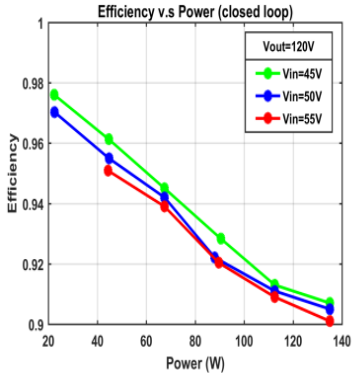


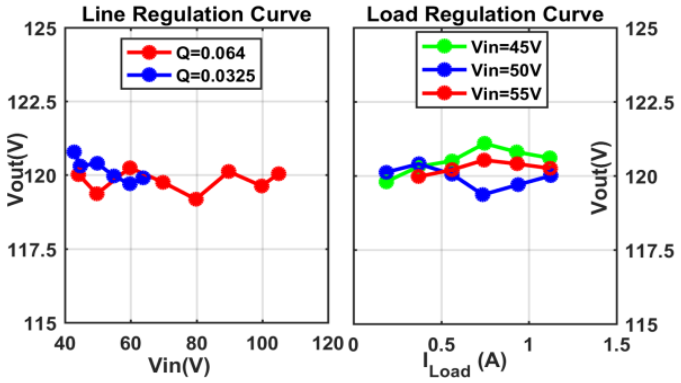
Fig. 2.14. Circuit diagram of the feedback controller



(a). Input voltage range

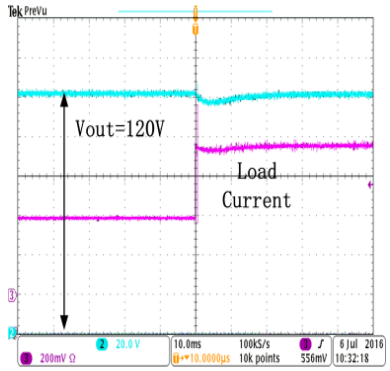


(b). Efficiency v.s. power

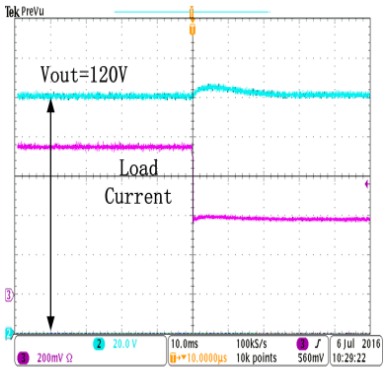


(c). Line and load regulation curves

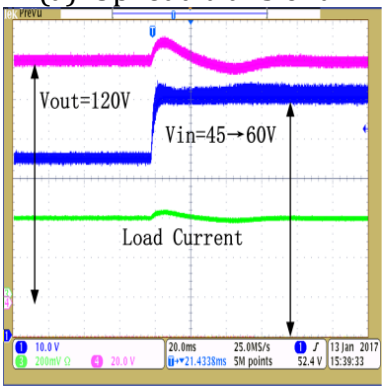
Fig. 2.15. Experimental results of 3X Ladder RSC (Closed-loop)



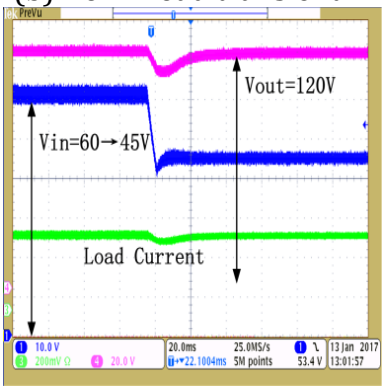
(a). Up load transient



(b) Down load transient



(c) Up line transient



(d) Down line transient

Fig. 2.16. Transient response of 3X Ladder RSC

2.9 Conclusion

In this chapter, the Ladder RSC has been analyzed to find the optimized operation region for regulated output voltage applications. By operating the Ladder RSC above the resonance, soft-switching operation could be ensured for transistors and diodes, while not sacrificing the voltage/current stress and converter stability. Most importantly, the voltage-gain range is improved significantly. Therefore it is more suitable for wide-line-regulation-range, low-power-level and high-frequency-operation applications in contrast to the traditional Ladder SCC. Some possible applications include fuel injectors for engineering equipment, solar cell energy harvesting with MPPT algorithm and so forth. In addition, a bidirectional configuration can be used for a 42V/14V dual voltage automotive system. Moreover, it has the potential to be integrated even including the resonant

inductor so as to be used in the power management system of a chip level system. This work is based on the contents published in [2].

2.10 References

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CHAPTER 3: A Family of Step-up Resonant Switched-Capacitor Converter with Continuously Adjustable Conversion Ratio

3.1 Introduction

The lack of bulky inductors or transformers makes the switched-capacitor converters (SCCs) attractive due to their small size, light weight, high efficiency, low electromagnetic interference (EMI) and high power density. However, the conversion ratio of the traditional SCC is predetermined by the circuit configuration with a small room for down adjustment with a compromised efficiency [2], which is a negative consequence compared to an inductor-based converter with continuous conversion ratio. In essence, the SCC regulates the output voltage by modulating the output impedance, whose value directly reflects the conduction loss and charge sharing loss of the SCC [3]. Typical modulation methods include frequency modulation, PWM modulation and so forth [3] [4]. As aforementioned, the above modulation methods can only regulate the output in a narrow range while maintaining an acceptable conversion efficiency.

To expand the voltage-gain range, some reconfigurable SCC topologies with fractional and variable conversion ratio were reported in [5] [6] [7]. However, they still require the inefficient linear regulation after selecting the operating mode that gives the output voltage that is closest to the desired voltage for a given input voltage [2]. Moreover, the high peak current during transition from one voltage level to another may cause high stress to the components especially for high-power applications, therefore proper control methods are needed to ensure soft transition [8]. Another approach by combining a low-frequency inductor-based converter with a SCC was applied in [9]-[14], so the voltage-gain-boosting of a SCC and the good voltage regulation of an inductor-based converter can be obtained at the same time. Obviously, the bulky magnetic components increase the converter size and cost significantly.

The zero current switching (ZCS) resonant switched-capacitor converter (RSC) - also named “indirect” RSC - was proposed in [15], where all switches realize ZCS, and the high current spike can be reduced significantly by operating below the resonance. However, the limitation of the ZCS RSCs due to their inability to provide regulation against line voltage changes still remains [16]. Several methods were reported to improve the voltage regulation capability, where one or two additional charge-balance states were introduced. In [17], the active switches of a 2X Dickson RSC were operated below the resonant frequency, while duty cycle control is applied to one of MOSFETs. Consequently, the line regulation is improved to handle an input voltage variation of 20%. In [18], one extra MOSFET is added to a basic 1:1 RSC to form a gyrator, i.e. a voltage-dependent current source, with a wide range of voltage conversion ratio. But zero cross detection is needed, and all three operation intervals need to be designed carefully to ensure normal operation. In [19] [20] [21], the resonant tank of the Dickson RSC or Ladder RSC is operating above the resonance, thus the voltage-gain range is significantly expanded, the zero voltage switching (ZVS) operation is ensured for two MOSFETs and the ZCS is ensured for all diodes. However, this method can only be applied to Ladder SCC, Dickson SCC and two-switch boosting switched-capacitor converter (TBSC) [22], where there exist intrinsic paths to conduct the reverse resonant current. Nevertheless, the regulation capability is poor at light load. Phase-shift control was applied to create the charge-balance states to improve the line regulation capability for an input voltage variation of 28%-38% [23] [24] [25]. However, all diodes must be replaced by active switches. In chip level design, this issue may be not severe. But for board level design with much higher power, the extra active switches and driving circuits increase the size and cost.

The soft-charging technique by cascading a high-efficient SCC with a high-frequency, low-voltage regulating stage was proposed to smooth the charging current and provide efficient regulation [2]. To minimize the component count, only a small inductor is inserted either to the output port (for step-down) or to the input port (for step-up) to achieve the similar soft-charging operation. This configuration is also named as “direct” RSC [26]. At very light load, the dynamic off-time modulation (DOTM) is applied to retain the high efficiency [27]. At moderate load or in high-frequency designs, it operates at resonance to ensure ZCS operation; and at heavy load, it operates above resonance to minimize the current ripple, even though the ZCS operation is lost [28]. However, the efficient regulation capability will be lost if only frequency modulation is applied. To recover the voltage regulation, the phase-shift control (also named quasi-resonant) was adopted in [29][30][31], where switching frequency is above the resonance and ZVS operation is ensured for all active switches. Similar to the phase-shift control for “indirect” RSC, all switches of “direct” RSC must be active/synchronous switches rather than diodes, which is not favorable for board-level design with high power. Also, the voltage gain can only be varied around the nominal one with a limited range due to the high resonant current, so the phase-shift angel should be carefully designed.

In patent [1], Cuk proposed a groundbreaking step-down PWM-Resonant Cuk topology, which realized overlapping dual resonance to regulate the output voltage using duty cycle control. Small size, light weight, high efficiency, fast transient response and good voltage regulation capability were all achieved.

Inspired by the Cuk dual resonance concept, a step-up Cuk Dual Resonance Core (DRC) is proposed, which can be extended to the Series-parallel (SP) SCC, Fibonacci SCC and voltage

doubler (VD), forming a family of step-up RSCs with continuous conversion ratio. With the Cuk dual resonance method, the regulation capability - upper bounded by the nominal gain determined by the circuit configuration - is well kept even at light load condition, so no special control or control mode transition is required to retain the high efficiency. Moreover, in order to decrease the switching loss, the on-time fixed frequency modulation is adopted to achieve ZCS turn-on for all MOSFETs and ZCS turn-off for all diodes. A comprehensive analysis about the Cuk DRC is given. A characteristic comparison between the Cuk DRC and the traditional "direct" and "indirect" resonant core is given. An open loop - 48V to 62~92V - converter prototype is built to verify the analysis. The contents in this chapter have been published in [32]

3.2 Nomenclature

$\mathbf{C_{1,2,...N}}$, $\mathbf{C_{out}}$:Intermediate capacitors and output capacitor;

$\mathbf{C_r}$:Resonant capacitor;

$\mathbf{D_{1,2,...N}}$:Power diodes;

$\boldsymbol{f_{r1,2}}$:Resonant frequencies with $f_{r1,2} = 1/2\pi\sqrt{L_{r1,2}C_r}$;

$\boldsymbol{f_s}$:Switching frequency;

F: Frequency ratio with $F = t_{on}/T_s = f_s/2f_{r1}$;

$\boldsymbol{h}$: An intermediate variable with $h = cos2\pi\left(\frac{f_{r1}}{kf_s} - \frac{1}{2k}\right)$;

$\boldsymbol{i_{Lr1,2}(t)}$, $\boldsymbol{I_{Lr1,2}}$: Transient and average resonant inductor currents;

$\boldsymbol{i_{s1,2...N}(t)}$, $\boldsymbol{i_{D1,2...N}(t)}$: Transient current flowing through $S_{1,2,...N}$, $D_{1,2,...N}$;

$\boldsymbol{I_{s1,2...N}}$, $\boldsymbol{I_{D1,2...N}}$: Average current flowing through $S_{1,2,...N}$, $D_{1,2,...N}$;

$\boldsymbol{i_{C1,2...N}(t)}$, $\boldsymbol{i_{Cout}(t)}$, $\boldsymbol{i_{Cr}(t)}$:Transient current flowing through $C_{1,2,...N}$, C_{out}, C_r;

$\boldsymbol{I_{C1,2\ldots N}}$, $\boldsymbol{I_{Cout}}$, $\boldsymbol{I_{Cr}}$: Average current flowing through $C_{1,2,\ldots N}$, C_{out}, C_r;

$\boldsymbol{I_b}$:Current base with $I_b = V_{in}/\sqrt{L_{r1}/C_r}$;

$\boldsymbol{J_{L_{r1,2}}}$: Normalized rms current of $L_{r1,2}$ with $J_{L_{r1,2}} = I_{Lr1,2\_rms}/I_b$;

$\boldsymbol{J_{S1,2}}$, $\boldsymbol{J_{D1,2}}$:Normalized rms current of $S_{1,2}$, $D_{1,2}$ to I_b;

$\boldsymbol{k}$: the relationship between L_{r1} and L_{r2} with $L_{r2} = k^2 L_{r1}$;

$\mathbf{L_{r1,2}}$:Resonant inductors;

m: An intermediate variable with m=$C_r R_L f_s$;

$\boldsymbol{M_{cr\_max}}$: Normalized maximum value of $V_{cr}(t)$ to V_{in};

$\boldsymbol{M_{cr\_min}}$:Normalized minimum value of $V_{cr}(t)$ to V_{in};

M: voltage gain of V_o to V_{in};

$\boldsymbol{M_{S1,2}}$, $\boldsymbol{M_{D1,2}}$:Normalized voltage stress of $S_{1,2}$, $D_{1,2}$ to V_{in};

$\boldsymbol{P_{sw.}}$, $\boldsymbol{P_{con.}}$:Switching loss and conduction loss;

$\boldsymbol{q_{t_0\sim t_1}}$, $\boldsymbol{q_{t_1\sim t_3}}$: The net charge flowing through C_r during different intervals;

Q: Quality factor with $Q = \sqrt{L_{r1}/C_r}/R_L$;

$\mathbf{R_L}$:Load resistance;

$\boldsymbol{r_{Lr1,2}}$, $\boldsymbol{r_{s1,2}}$:ESRs of the resonant inductors and active switches;

$\mathbf{S_{1,2,3\ldots N}}$:MOSFETs;

$\boldsymbol{t_{on}}$:Turn-on time of S_1 with $t_{on} = 1/2f_{r1}$;

$\boldsymbol{V_{in}}$, $\boldsymbol{V_o}$:Input and output voltage;

$\boldsymbol{V_{cr}(t)}$:Voltage across C_r;

$\boldsymbol{V_{cr\_max}}$, $\boldsymbol{V_{cr\_min}}$:Maximum and minimum values of $V_{cr}(t)$;

$\boldsymbol{V_f}$:Forward voltage of the diode.

3.3 Topology and Operation Principle of the Cuk DRC

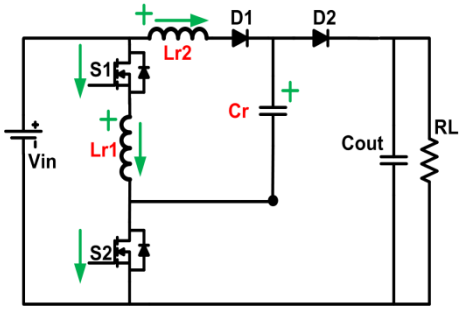
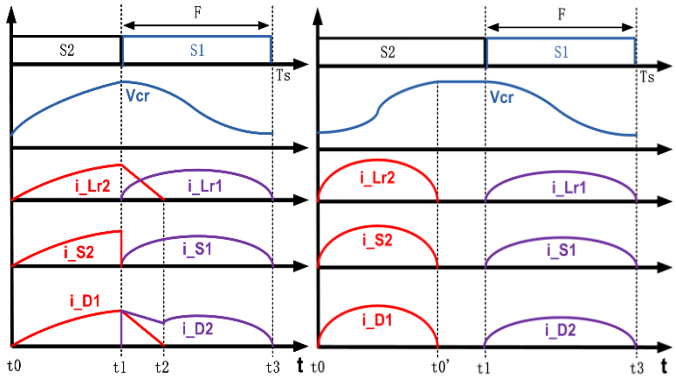


Fig. 3.1. Topology of the Cuk DRC



(a) Mode 1 (b) Mode 2

Fig. 3.2. Operating waveforms of the Cuk DRC

The topology of the step-up Cuk DRC is shown in Fig. 3.1. The resonant inductor L_{r1} is in series with S_1, while L_{r2} is in series with D_1. C_r is the resonant capacitor, while C_{out} is the output capacitor with large capacitance. The first resonant path consists of L_{r1} and C_r with resonant frequency $f_{r1} = \frac{1}{2\pi\sqrt{L_{r1}C_r}}$, while the second resonant path consists of L_{r2} and C_r with $f_{r2} = \frac{1}{2\pi\sqrt{L_{r2}C_r}}$.

The on-time fixed frequency modulation control is adopted – that is, the turn-on time of S_1 is fixed at $t_{on} = \frac{1}{2f_{r1}}$. By varying the switching frequency f_s, two operation modes can be obtained, as given in Fig. 3.2.

Fig. 3.2(a) shows the operating waveforms in mode 1, in which there exists an overlapping period between two resonant paths. By introducing the overlapping period, the charge balance of C_r can be satisfied during this period. As a result, the conversion ratio of the core can be different from the target value which is determined by the circuit configuration and can vary continuously. This mode is defined as regulated mode.

Fig. 3.2(b) shows the operating waveforms in mode 2, where the i_{Lr1} does not overlap with i_{Lr2}. This mode is similar to the operation of traditional ZCS SCCs [15], so the voltage gain is almost fixed, named as unregulated mode.

3.4 Conversion Ratio Curve of the Cuk DRC

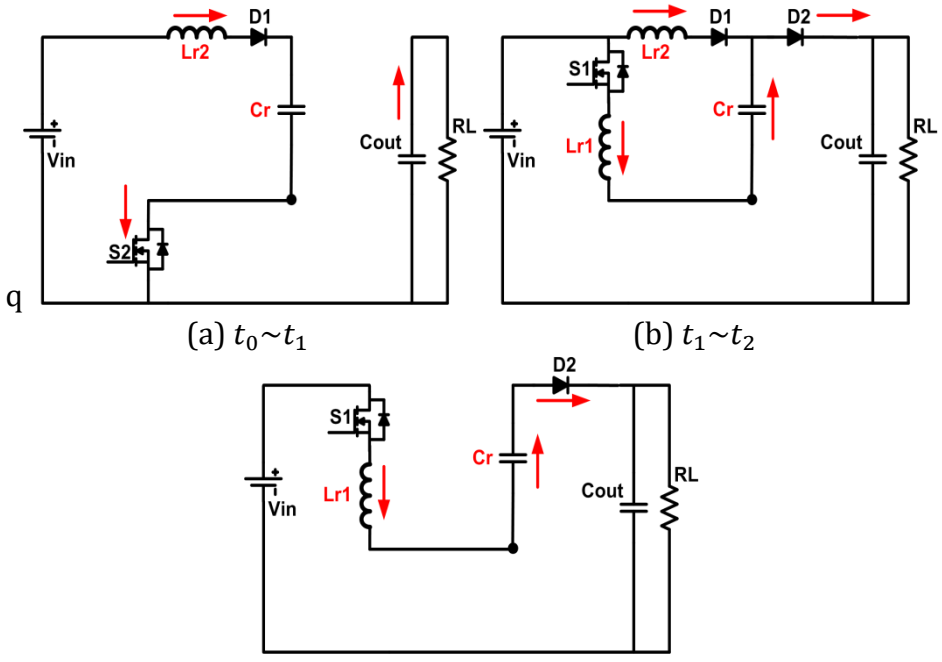


Fig. 3.3. Operating states of the Cuk DRC

The topology of the Cuk DRC is given in Fig. 3.1, in which the positive direction is defined by the green arrows. In this section, the conversion ratio of the DRC will be derived. Several assumptions are made as follows. The C_{out} is large enough, so the output voltage is regarded as a constant V_{out}. Equivalent Series Resistances (ESRs) of capacitors, parasitic

components of switches and forward voltage of diodes are neglected. The dead-time is ignored as well. Compared to the practical application, the approximation leads to higher maximum gain and voltage-gain curve. In board level design, this approximation is acceptable, such as the analysis for resonant converters [33] and for RSC [19]-[21]. For chip-level design, the parasitic elements should be considered.

3.4.1 Mode 1 (Regulated Mode)

The operating waveforms and operating states in mode 1 are shown in Fig. 3.2(a) and Fig. 3.3, respectively.

$[t_0 - t_1]$: At t_0, transistor S_2 and diode D_1 start conducting the resonant current with ZCS turn-on as shown in Fig. 3.3(a). In this state, the KVL and KCL equations are obtained as:

$$V_{in} - L_{r2}\frac{di_{Lr2}(t)}{dt} - V_{cr}(t) = 0 \quad (1)$$

$$C_r\frac{dV_{cr}(t)}{dt} = i_{Lr2}(t) \quad (2)$$

From Fig. 3.2(a), the boundary conditions are:

$$i_{Lr2}(t_0) = 0, V_{cr}(t_0) = V_{cr\_min} \quad (3)$$

Based on (1)-(3), the following expressions are obtained:

$$i_{Lr2}(t) = -(V_{in} - V_{cr\_min})\sqrt{\frac{C_r}{L_{r2}}}sin2\pi f_{r2}(t - t_0) \quad (4)$$

$$V_{cr}(t) = V_{in} - (V_{in} - V_{cr\_min})cos2\pi f_{r2}(t - t_0), \text{ where } f_{r2} = \frac{1}{2\pi\sqrt{L_{r2}C_r}} \quad (5)$$

$[t_1 - t_2]$: At t_1, transistor S_2 is turned off and S_1 is turned on with ZCS operation. Since $i_{Lr2}(t)$ hasn't resonated to zero, it continues flowing through D_1. Meantime, the new resonant path starts resonating through S_1 as shown in Fig. 3.3(b). During this interval, the two inductor current waveforms overlap. In this state, the KVL and KCL equations are obtained as following:

$$V_{in} - V_{out} = L_{r2}\frac{di_{Lr2}(t)}{dt} \tag{6}$$

$$V_{in} - L_{r1}\frac{di_{Lr1}(t)}{dt} + V_{cr}(t) - V_{out} = 0 \tag{7}$$

$$C_r\frac{dV_{cr}(t)}{dt} = -i_{Lr1}(t) \tag{8}$$

From Fig. 3.2(a), the boundary conditions are:

$$i_{Lr1}(t_1) = 0, V_{cr}(t_1) = V_{cr\_max} \tag{9}$$

Based on (7)-(9), the following expressions are obtained:

$$i_{Lr1}(t) = (V_{in} - V_{out} + V_{cr\_max})\sqrt{\frac{C_r}{L_{r1}}}sin2\pi f_{r1}(t - t_1) \tag{10}$$

$$V_{cr}(t) = -(V_{in} - V_{out}) + (V_{in} - V_{out} + V_{cr\_max})cos2\pi f_{r1}(t - t_1)$$

$$\text{where } f_{r1} = \frac{1}{2\pi\sqrt{L_{r1}C_r}} \tag{11}$$

$[t_2 - t_3]$: At t_2, $i_{Lr2}(t)$ decreases to zero and D_1 is turned off with ZCS operation. Transistor S_2 and diode D_2 continue conducting the resonant current as Fig. 3.3(c). The expressions of resonant current and voltage are the same as (10) and (11). At t_3, the $i_{Lr1}(t)$ resonates to zero and S_2, D_2 will be turned off with ZCS operation.

Assuming that $L_{r2} = k^2L_{r1}(k > 0)$, so

$$\frac{f_{r1}}{f_{r2}} = \sqrt{\frac{L_{r2}}{L_{r1}}} = k \tag{12}$$

During $t_0 - t_1$, the net charge flowing into C_r is:

$$q_{t_0 \sim t_1} = C_r\left(V_{cr\_max} - V_{cr\_min}\right) = \int_{t_0}^{t_1} i_{Lr2}(t)dt \tag{13}$$

Since the turn-on time of S_1 is fixed at $t_{on} = \frac{1}{2f_{r1}}$, so

$$t_3 - t_1 = \frac{1}{2f_{r1}} \text{ and } t_1 - t_0 = \frac{1}{f_s} - \frac{1}{2f_{r1}} \tag{14}$$

According to (4) (12)-(14), the following expression is obtained:

$$h = cos2\pi\left(\frac{f_{r1}}{kf_s} - \frac{1}{2k}\right) = \frac{(V_{cr\_max} - V_{in})}{(V_{cr\_min} - V_{in})} \quad (15)$$

Similarly, the net charge flowing out of C_r during $t_1 - t_3$ is:

$$q_{t_1 \sim t_3} = C_r\left(V_{cr\_max} - V_{cr\_min}\right) = \int_{t_1}^{t_3} i_{Lr1}(t)dt \quad (16)$$

By substituting (10) (14) into (16), the following expression is obtained:

$$(V_{out} - V_{in}) = \frac{1}{2}(V_{cr\_max} + V_{cr\_min}) \quad (17)$$

In each period, the following equation is held in every interval:

$$i_{Lr2}(t) = i_{cr}(t) + i_{D2}(t) = i_{cr}(t) + i_{cout}(t) + \frac{V_{out}}{R_L} \quad (18)$$

According to the charge balance on C_r and C_{out}, the average value of $i_{cr}(t)$ and $i_{out}(t)$ in one switching cycle is equal to zero, so

$$I_{Lr2} = f_s \int_{t_0}^{t_2} i_{Lr2}(t)\mathrm{dt} = I_{cr} + I_{cout} + \frac{V_{out}}{R_L} = \frac{V_{out}}{R_L} \quad (19)$$

According to (4) (6) (13)-(15) (19), the following expression is derived:

$$\frac{V_{out}}{V_{in}} = \frac{2m(V_{cr\_max} - V_{cr\_min})}{V_{cr\_max} + V_{cr\_min}}, \text{ where m=} C_r R_L f_s \quad (20)$$

According to (15) (17) (20), the following expressions are derived:

$$M_{cr\_max} = \frac{V_{cr\_max}}{V_{in}} = \frac{2h^2(m-1) + h(A-2m-1) + 1}{(h+1)^2},$$

$$\text{where A} = \sqrt{h^2(4m^2 - 12m + 1) + h(2 - 8m^2) + 4m^2 + 12m + 1} \quad (21)$$

$$M_{cr\_min} = \frac{V_{cr\_min}}{V_{in}} = -2m - M_{cr\_max} - 1 + \sqrt{4m^2 + 4m(1 + 2M_{cr\_max}) + 1} \quad (22)$$

$$M = \frac{V_{out}}{V_{in}} = \frac{2m(M_{cr\_max} - M_{cr\_min})}{M_{cr\_max} + M_{cr\_min}} \quad (23)$$

3.4.2 Mode 2 (Unregulated Mode)

The operating waveforms in mode 2 are shown in Fig. 3.2(b). Only operating states in Fig. 3.3 (a) (c) are included in mode 2.

Similarly, according to the net charge flowing into or out of C_{r1} during $t_0 - t_1$ and $t_1 - t_3$, the following expressions are obtained correspondingly:

$$V_{out} - V_{in} = \frac{V_{cr\_max} + V_{cr\_min}}{2} \tag{24}$$

$$V_{in} = \frac{V_{cr\_max} + V_{cr\_min}}{2} \tag{25}$$

Similarly, the average value of $i_{Lr2}(t)$ in one switching cycle is equal to the average output current, i.e.

$$V_{cr\_max} - V_{cr\_min} = \frac{V_{out}}{m} \tag{26}$$

Based on (24)-(26), the following expressions can be derived:

$$M_{cr\_max} = \frac{m+1}{m} \tag{27}$$

$$M_{cr\_min} = \frac{m-1}{m} \tag{28}$$

$$M = 2 \tag{29}$$

3.4.3 Conversion Ratio Curve

In order to plot the conversion ratio curve, two parameters are defined as follows:

$$\text{Frequency Ratio: F} = \frac{t_{on}}{T_s} = \frac{f_s}{2f_{r1}};$$

$$\text{Quality Factor: Q} = \frac{Z_{r1}}{R_L},\ Z_{r1} = \sqrt{L_{r1}/C_r} \tag{30}$$

The numerator of the quality factor is the impedance of the resonant tank, while the denominator is the equivalent load resistance. From the definition of Q, one can see the higher Q represents the higher load current once the resonant tank is determined. The definition of Q is widely used for analyzing the traditional resonant converters [33], and then is inherited to the RSC [19] [20] [21].

As a result, the relationships between h, m and F, Q are found as shown below:

$$h = cos2\pi\left(\frac{f_{r1}}{kf_s} - \frac{1}{2k}\right) = \cos\pi(\frac{1}{Fk} - \frac{1}{k}) \quad (31)$$

$$m = C_r R_L f_s = \frac{F}{Q}\frac{1}{\pi} \quad (32)$$

The converter will enter regulated mode if:

$$\frac{1}{2f_{r1}} + \frac{1}{2f_{r2}} > \frac{1}{f_s} \quad (33)$$

Consequently, the boundary between mode 1 and mode 2 is:

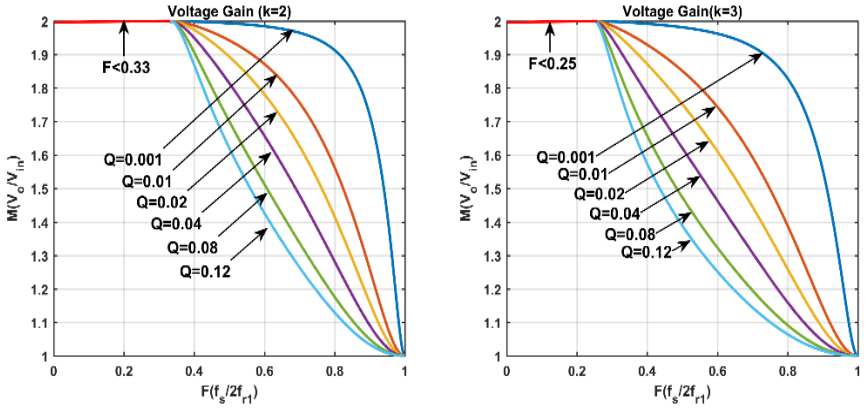
$$\text{Mode 1: } \frac{1}{k+1} < F < 1\text{; Mode 2: 0<F<}\frac{1}{k+1} \quad (34)$$

Considering the boundary condition (34) and substituting (31) (32) into (21) (22) (23), the complete expression of conversion ratio in terms of Q and F can be derived. For simplicity, the complete expression is not given, while the graphical conversion ratio curves with k=2,3 are plot in Fig. 3.4.

Several notes are concluded referred to the conversion ratio curves from Fig. 3.4:

1) When $0 < F < \frac{1}{k+1}$, the voltage gain is fixed at 2 and the resonant core will lose regulation capability, regardless of the load condition.
2) When $\frac{1}{k+1} < F < 1$, the conversion ratio of the resonant core can be well adjusted by changing *F*. At heavy load (high Q), the resonant core has wide regulation range when *F* below the upper limit 1. At light load (smaller Q), the regulation capability will be retained, which is an advantage compared to the poor light load regulation capability in [19] [20] [21]. However, the light load condition may cause stability issue if the switching frequency approaches the upper limit 1.
3) For smaller k, the f_s only needs to be varied in a narrower range if the regulation range is determined. However, the regulation accuracy is lower. At high *F*, a small deviation of

F causes a large variation of conversion ratio, which may cause stability issue if closed loop is applied.



(a) k=1 (b) k=2

Fig. 3.4. Conversion ratio curve of the Cuk DRC

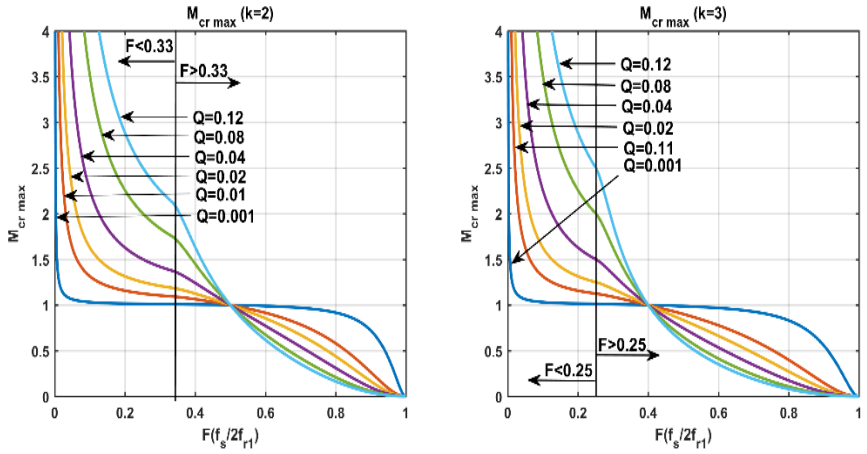
3.5 Components Stress and Conduction Loss Estimation

3.5.1 Voltage Stress

The selection of k and Q influences the voltage stress (VS) of the resonant capacitor, which directly affects the VS of other components. In this section, the normalized maximum voltage value (M_{cr_max}) of the resonant capacitor is discussed, and then the VS of other components is derived.

By substituting (31) (32) into the expressions (21) (27), M_{cr_max} in different operation modes can be obtained. Due to the boundary constraints, the M_{cr_max} of the resonant capacitor for the resonant core with k=2,3 is plotted in Fig. 3.5, where the black line represents the boundary between mode 1 and mode 2. Several notes are concluded according to the plot: (1) The M_{cr_max} of the resonant capacitor in the unregulated mode is higher than that in the regulated mode. (2) In the regulated mode, the higher Q leads to higher voltage stress of the resonant capacitor. (3) In the regulated mode, the higher k leads to higher voltage stress of the resonant capacitor if Q is determined.

Similarly, the VS (normalized to V_{in}) of the transistors and diodes is derived in Table 3.1.



(a) k=2 (b) k=3

Fig. 3.5. Normalized maximum voltage of the resonant capacitor in the Cuk DRC

3.5.2 Current Stress

The selection of k and Q influences the rms current stress (CS) of the resonant inductors, which directly affects the CS of other components. In this section, the rms current stress of the resonant inductors is discussed, and then the CS of other components is derived.

To begin with, the current base is defined as follows:

$$I_b = \frac{V_{in}}{\sqrt{L_{r1}/C_r}} \tag{35}$$

Since the turn-on time of S_1 is fixed at $t_{on} = \frac{1}{2f_{r1}}$, the current waveform of L_{r1} is always a half sinusoidal wave in both modes. According to (10) (35), the normalized rms current of L_{r1} is:

$$J_{L_{r1}} = \frac{I_{Lr1\_rms}}{I_b} = (1 - M + M_{cr\_max})\sqrt{\frac{F}{2}} \text{ (0<F<1)} \tag{36}$$

In mode 2, the current waveform of L_{r2} is also a half sinusoidal wave. According to (4) (35), the normalized rms current of L_{r2} in mode 2 is:

$$J_{L_{r2}} = \frac{I_{Lr2\_rms}}{I_b} = \frac{1}{k}(1 - M_{cr\_min})\sqrt{\frac{kF}{2}} \ (0<F<\frac{1}{k+1}) \tag{37}$$

In mode 1, $i_{Lr2}(t)$ consists of two parts ($t_0 \sim t_1$ *and* $t_1 \sim t_2$), as shown in Fig. 3.2(a). The first part is a partial sinusoidal wave, whose rms value is:

$$J_{L_{r2\_p1}} = \frac{I_{Lr2\_rms\_p1}}{I_b} = \frac{1}{k}(1 - M_{cr\_min})\sqrt{\frac{1-F}{2}\left(1 - \frac{sin2\pi(1-F)cos2\pi(1-F)}{2\pi(1-F)}\right)} \tag{38}$$

The second part is a triangle, whose rms value is:

$$J_{L_{r2\_p2}} = \frac{I_{Lr2\_rms\_p2}}{I_b} = \frac{1}{k}(1 - M_{cr\_min})\sqrt{\frac{1}{3}\frac{t_2 - t_1}{1/f_s}} \tag{39}$$

In mode 2, there exists an overlapping period, so

$$0 < \frac{t_2 - t_1}{1/f_s} < F \tag{40}$$

As a result, the following expression is obtained in mode 1:

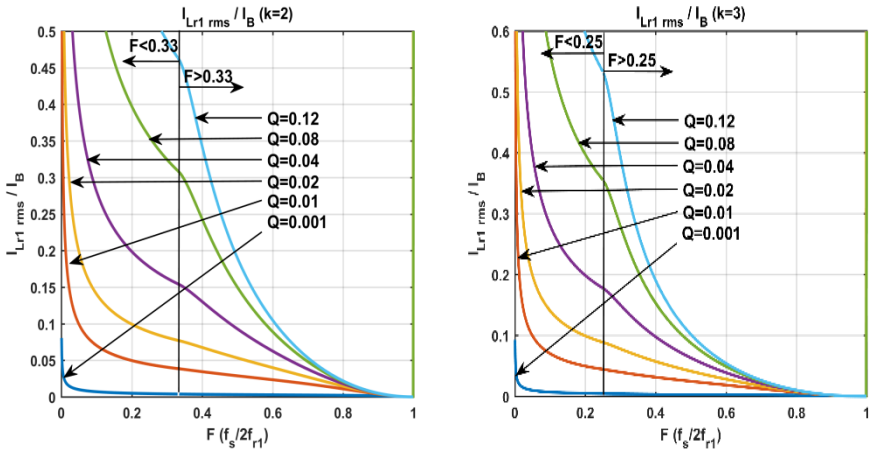
$$J_{L_{r2}} = \sqrt{{J_{L_{r2_{p1}}}}^2 + {J_{L_{r2_{p2}}}}^2}$$

$$< \frac{1}{k}\left(1 - M_{cr\_min}\right)\sqrt{\frac{1-F}{2}\left(1 - \frac{sin2\pi(1-F)cos2\pi(1-F)}{2\pi(1-F)}\right) + \frac{F}{3}} \ (\frac{1}{k+1}<F<1) \tag{41}$$

According to (21) (23) (27) (29) (36), the normalized rms CS of L_{r1} with k=2,3 is plot in Fig. 3.6. According to (22) (28) (37) (41), the normalized rms CS of L_{r2} with k=2,3 is plot in Fig. 3.7. Note that the curve in the regulated mode reflects the upper limit for simplicity, while the curve in the unregulated mode is the actual value.

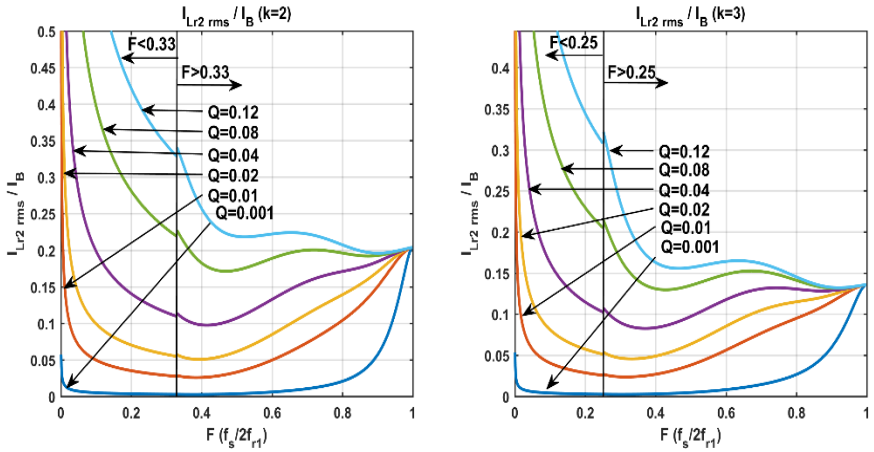
Several notes are concluded according to the plot: (1) The maximum $J_{L_{r1}}$ and $J_{L_{r2}}$ of the two resonant inductors in unregulated mode is higher than that in the regulated mode. (2) In the regulated mode, the higher Q leads to higher current stress. (3) In the regulated mode, the higher k leads to higher current stress of L_{r1} if Q is determined. (4) In the regulated mode, the higher k leads to lower current stress of L_{r2} if Q is determined.

Similarly, the CS (normalized to I_b) of the transistors and diodes is derived in Table 3.1.



(a) k=2 (b) k=3

Fig. 3.6. Normalized rms current of L_{r1} in the Cuk DRC



(a) k=2 (b) k=3

Fig. 3.7. Normalized rms current of L_{r2} in the Cuk DRC

Table 3.1. Component stress in the Cuk DRC

	VS (normalized to V_{in})	CS (normalized to I_B)
S_1	$M_{S1} = 1$	$J_{S1} = J_{Lr1}$
S_2	$M_{S2} = M - M_{cr\_min}$	$J_{S2} = J_{L_{r2\_p1}}$
D_1	$M_{D1} = M - 1$	$J_{D1} = J_{L_{r2}}$
D_2	$M_{D2} = M - M_{cr\_min}$	$J_{D2} = \sqrt{{J_{L_{r1}}}^2 + {J_{L_{r2\_p2}}}^2}$

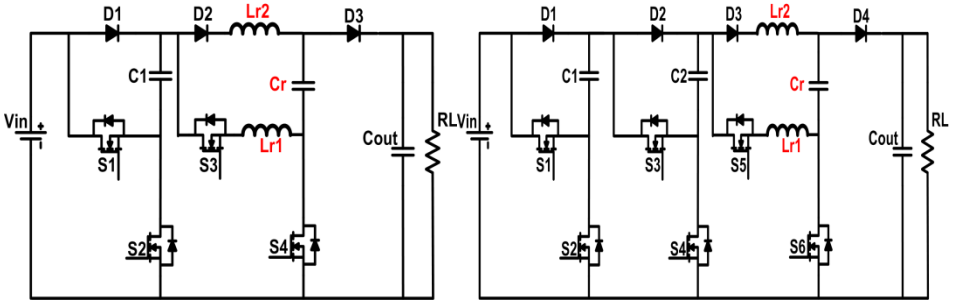
3.5.3 Conduction Loss Estimation

With the help of Table 3.1, the conduction loss can be approximated as:

$$P_{con.} = ({J_{Lr1}}^2 r_{Lr1} + {J_{Lr2}}^2 r_{Lr2} + {J_{S1}}^2 r_{s1} + {J_{S2}}^2 r_{s2}){I_B}^2 + (I_{D1} + I_{D2})V_f \qquad (42)$$

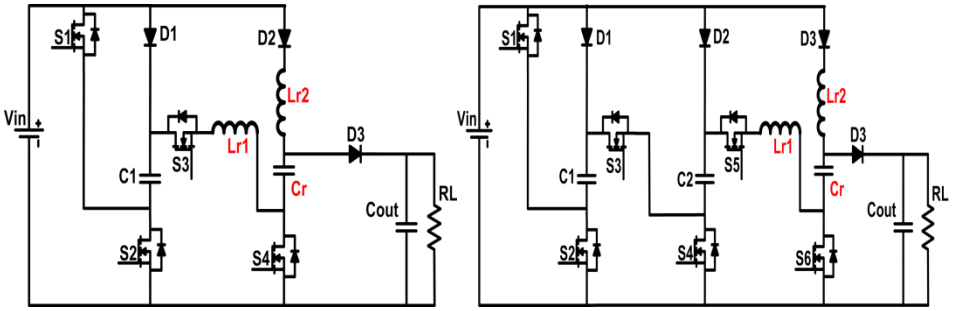
The $r_{Lr1,2}$ and $r_{s1,2}$ represent the ESRs of the resonant inductors and active switches, while V_f represents the forward voltage of the diodes. The expressions of $J_{Lr1,2}$ can be found from (36) (41), and $J_{S1,2}$ can be found from Table 3.1. As for the average current of the two diodes, the expression $I_{D1,2} = V_{out}/R_L$ is derived based on (18) (19). It's noteworthy that the ESRs of the capacitors are not considered here.

3.6 The Extension of Cuk DRC to a Family of Step-up RSC



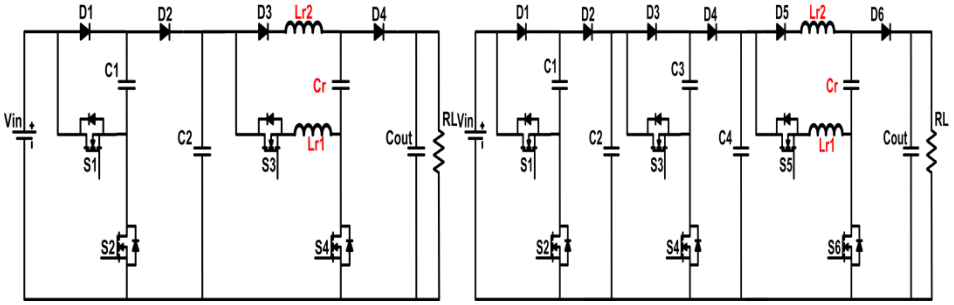
(a) 3X (b) 5X

Fig. 3.8. Topologies of step-up Fibonacci RSC with Cuk DRC



(a) 3X (b) 4X

Fig. 3.9. Topologies of step-up Series-parallel RSC with Cuk DRC



(a) 4X (b) 8X

Fig. 3.10. Topologies of resonant Voltage Doubler with Cuk DRC

In Fig. 3.8-3.10, the step-up Cuk DRC is extended to Fibonacci SCC, SP SCC and resonant VD, forming a family of step-up RSC. Since 2X configuration of all SCCs is exactly the same as the resonant core in Fig. 3.1, only the topologies with higher nominal conversion ratios are shown.

In all topologies, the intermediate capacitors are assumed to be much larger than the resonant one, so the voltage across the intermediate capacitors can be regarded as a constant in one switching cycle. With the Cuk DRC being inserted into the last stage of the SCCs, the output voltage can be regulated, while the intermediate voltage level is not changed. The switching schemes in the regulated mode are summarized in Table 3.2. The "↑" means the capacitor is charged or the inductor current is increasing, while the "↓" means the capacitor is discharged or the inductor current is decreasing.

Table 3.2. Switching schemes of different topologies

	State 1 (ON SW)	**State 2 (ON SW)**	**State 3 (ON SW)**
3X Fibonacci RSC	S_1, S_4, D_1, D_2	S_2, S_3, D_1, D_2	S_2, S_3, D_1
	$C_1 \downarrow, C_r \uparrow$ $i_{Lr1} = 0, L_{r2} \uparrow$	$C_1 \uparrow, C_r \downarrow$ $L_{r1} \uparrow, L_{r2} \downarrow$	$C_1 \uparrow, C_r \downarrow$ $L_{r1} \uparrow, i_{Lr2} = 0$
3X SP RSC	S_2, S_4, D_1, D_2	S_1, S_3, D_2, D_3	S_1, S_3, D_3
	$C_1 \uparrow, C_r \uparrow$ $i_{Lr1} = 0, L_{r2} \uparrow$	$C_1 \downarrow, C_r \downarrow$ $L_{r1} \uparrow, L_{r2} \downarrow$	$C_1 \downarrow, C_r \downarrow$ $L_{r1} \uparrow, i_{Lr2} = 0$
4X Resonant VD	S_2, S_4, D_1, D_3	S_1, S_3, D_2, D_3, D_4	S_1, S_3, D_2, D_4
	$C_1 \uparrow, C_2 \downarrow C_r \uparrow$ $i_{Lr1} = 0, L_{r2} \uparrow$	$C_1 \downarrow, C_2 \uparrow C_r \downarrow$ $L_{r1} \uparrow, L_{r2} \downarrow$	$C_1 \downarrow, C_2 \uparrow C_r \downarrow$ $L_{r1} \uparrow, i_{Lr2} = 0$

To take the 3X Fibonacci as an example. In state 1, S_1 and S_4 are turned on. The input V_{in} and C_1 are in series, and the resonant path with L_{r2}, C_r starts conducting the resonant current. In state 2, S_2 and S_3 are turned on. The V_{in} charges C_1, meantime both resonant inductors are conducting current. For L_{r1}, the initial current is zero and it starts resonating with C_r; while for L_{r2}, the initial current is positive and then i_{Lr2} starts decreasing linearly. In state 3, S_2 and S_3 are still turned on, while the i_{Lr2} decreases to zero. The V_{in} charges C_1,

meantime only the resonant path with L_{r1}, C_r is conducting current. As described, the basic operation principle is the same as the Cuk DRC.

With the similar method in section 3.4, the conversion ratio of different topologies can be derived. Some examples are listed as follows.

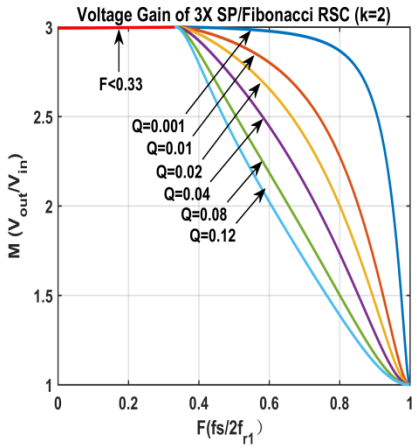
3X SP RSC:

$$\begin{cases} M_{cr\_max} = \frac{4h^2(m-1)+h(B-4m-3)+1}{(h+1)^2} \\ where\ \mathrm{B} = \sqrt{h^2(16m^2-40m+1)+h(2-32m^2)+16m^2+40m+1} \\ M_{cr\_min} = -4m - M_{cr\_max} - 3 + \sqrt{16m^2+24m+16mM_{cr\_max}+1} \\ M = \frac{4m(M_{cr\_max}-M_{cr\_min})}{2+M_{cr\_max}+M_{cr\_min}} \end{cases} \tag{43}$$

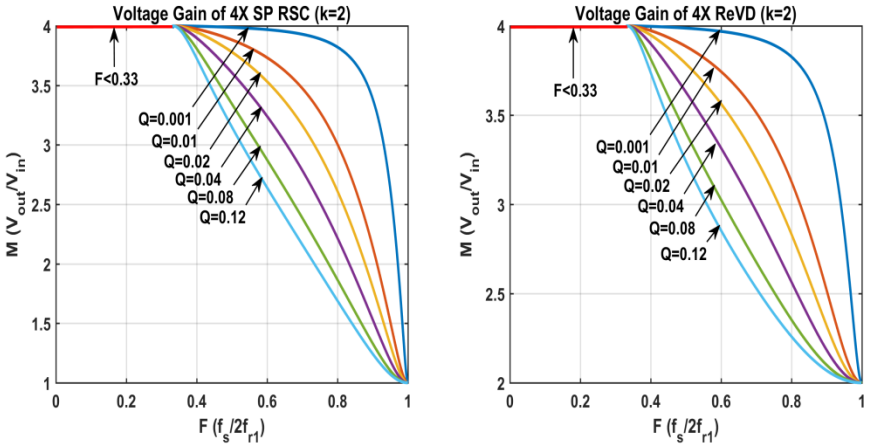
4X SP RSC:

$$\begin{cases} M_{cr\_max} = \frac{6h^2(m-1)+h(C-6m-5)+1}{(h+1)^2} \\ where\ \mathrm{C} = \sqrt{h^2(36m^2-84m+1)+h(2-72m^2)+16m^2+84m+1} \\ M_{cr\_min} = -6m - M_{cr\_max} - 5 + \sqrt{36m^2+60m+24mM_{cr\_max}+1} \\ M = \frac{6m(M_{cr\_max}-M_{cr\_min})}{4+M_{cr\_max}+M_{cr\_min}} \end{cases} \tag{44}$$

By substituting (31) (32) into the voltage-gain formulas, the conversion ratio curve of some topologies are given in Fig. 3.11. As stated, by inserting the Cuk DRC, the voltage gain of the family of step-up RSC can be continuously adjusted. It's noteworthy that a proper insertion of Cuk DRC to the Ladder SCC has not been found. With proper modification, it can be applied to the Dickson SCC, which will be analyzed in the future work.



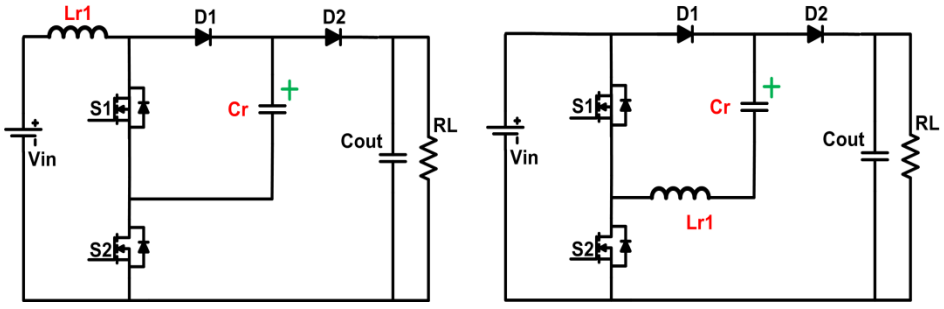
(a) 3X SP/Fibonacci RSC



(b) 4X SP RSC (c) 4X Resonant VD

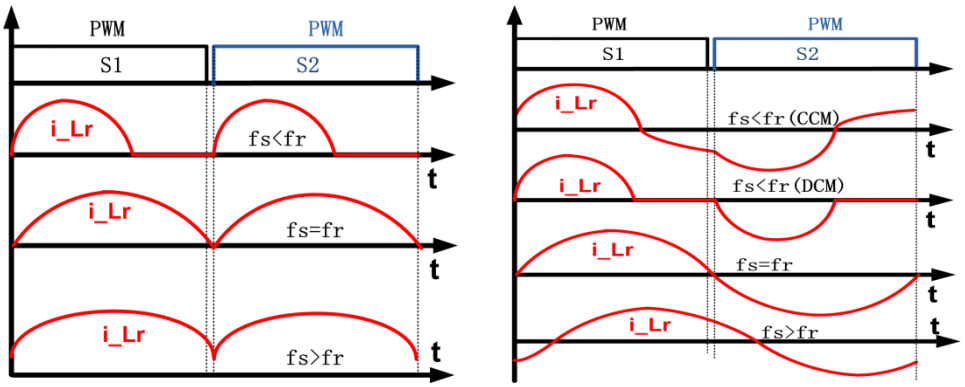
Fig. 3.11. Conversion ratio curves of different topologies (k=2)

3.7 Topologies Comparison



(a) "Direct" [28] (b) "Indirect" [21]

Fig. 3.12. Topologies of traditional resonant cores



(a) "Direct" Resonant Core (b) "Indirect" Resonant Core

Fig. 3.13. Inductor current waveforms in different modes

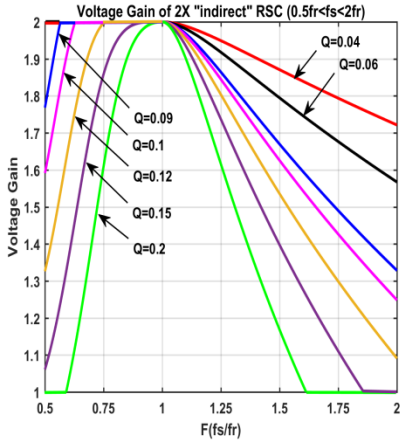


Fig. 3.14. Voltage gain curve of "indirect" resonant core

In this section, a brief characteristic comparison between the proposed Cuk DRC and the traditional "direct"/"indirect" resonant cores is given. The topologies of "direct" and "indirect" cores and their inductor current waveforms are given in Fig. 3.12, 3.13. For the "direct" core, two MOSFETs in [28] are replaced by two diodes to reduce the active switch count. For the "indirect" core, it's actually the 2X version of Ladder RSC reported in [21].

Some similarities exist among them. For example, all three cores are the combination of SCC with resonant tank(s), so the needed inductor volume can be 10 to 100x lower compared to the traditional boost converter due to the reduced volt-second product provided by the SC stage [29]. For the "direct"/"indirect" cores, the reported inductors can

be as small as several uH [28] or even in the order of nH by utilizing the stray inductance [24] for board-level design. Analogously, the proposed Cuk DRC can decrease the needed inductor value to be as low as 10nH according to the Resonance Scaling Method [1], even though one more inductor is required. This feature makes the above three cores possible to be integrated in chip level with proper design [25][26][29][31], where all diodes are placed by MOSFETs.

Some differences between the three cores are discussed as follows

3.7.1 "Direct" Resonant Core

The resonant current is unidirectional. From Fig. 3.13(a), the resonant current is in discontinuous current mode (DCM) below and at resonance. All switches are ZCS turned on/off. Above the resonance, all switches are hard switched.

The conversion ratio has limited down adjustment range while sacrificing the efficiency, no matter in which modes. Phase-shift control (also named quasi-resonant) can be applied to improve the regulation capability, with all diodes being replaced by MOSFETs.

The "direct" resonant core with soft-charging operation can be extended to SP SCC, Fibonacci SCC, VD and Dickson SCC, not including the Ladder SCC [27]. However, the resonant frequency in each phase may be different for topologies that have different equivalent capacitance in each phase (such as Fibonacci and SP SCC). As a result, The ZCS operation may be lost in some phases.

3.7.2 "Indirect" Resonant Core

The resonant current is bidirectional. Below the resonance in Fig. 3.13(b), the resonant current can be either in DCM or in continuous current mode (CCM), depending on the

circuit parameters [21]. Above the resonance, the current waveform is quasi-sinusoidal. All MOSFETs are ZVS turned on, and all diodes are ZCS turned on/off.

The conversion ratio curve is plotted in Fig. 3.14. By operating above the resonance, the voltage-gain can be adjusted within a wide range while not sacrificing the overall efficiency [21]. But at light load, the regulation capability is poor.

The "indirect" resonant core with wide line regulation range can be extended to Ladder SCC and Dickson SCC [20]. However, for the N-X Ladder configuration (N>3), some diodes will lost the ZCS operation.

3.7.3 Cuk DRC

The Cuk DRC includes two resonant paths. In the regulated mode, the MOSFETs are ZCS turned on and all diodes are ZCS turned off.

With turn-on time fixed frequency modulation, the voltage-gain can be adjusted in a wide range, even at light load condition.

The Cuk DRC can be extended to Fibonacci SCC, SP SCC and VD. With proper modification, it can be applied to the Dickson SCC. However, for N-X configurations (N>2), the switches are hard switched except for the last stage.

3.8 Experimental Results

3.8.1 Hardware Design

A 48V to 67~96V Cuk DRC with maximum power 120W was designed and built. As aforementioned, the selection of *k* is important. If *k* is small, the regulation accuracy is low and the rms current stress of L_{r2} is high; if *k* is large, it leads to large L_{r2}, high voltage stress of C_r and high rms current stress of L_{r1}. Considering the above tradeoffs, k=2 is selected and thus $L_{r2} = 4L_{r1}$. The turn-on time of S_1 is designed to be fixed at $5us$ (so $f_{r1} = 100kHz$).

If $C_r = 1uF$ is selected, the L_{r1} is $2.5uH$ according to $f_{r1} = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}}$. Then L_{r2} is $10uH$ and $f_{r2} = 50kHz$. Since the maximum V_{out} is $96V$ and maximum P is 120W, the quality factor $Q = \frac{\sqrt{L_{r1}/C_r}}{R_L} \leq 0.0206$. Three different load resistances – 80Ω, 160Ω, 800Ω are used to test the gain curves, so the corresponding quality factor is Q=0.02, 0.01, 0.002.

The Cuk DRC is ensured to be operating in the regulated mode ($F > 0.33$). In addition, if F is close to 1, the S_1 will be always ON and may be damaged. Therefore, the range of $0.33 < F < 0.9$ is used while selecting components. According to Table 3.1 in section 3.5.2, the VS of S_1 and D_1 is V_{in}. The normalized VS of S_2 and D_2 is plot in Fig. 3.15. As seen, the VS of S_2 and D_2 is $1.19V_{in}$. According to Fig. 3.6 and 3.7, the normalized rms CS of $L_{r1,2}$ when 0.33<F<0.9 (Q=0.02) is $0.175I_B$ and $0.125I_B$. According to Table 3.1, the normalized rms CS of all switches at heavier load (Q=0.02) is plot in Fig. 3.16. Within the range of $0.33 < F < 0.9$, the rms CS of S_1, S_2, D_1, D_2 is $0.077I_B$, $0.09I_B$, $0.17I_B$,$0.233I_B$ correspondingly ($I_B = \frac{V_{in}}{\sqrt{L_{r1}/C_r}} = 30.4A$). Based on the above analysis, components are selected and the specifications of the prototype are listed in Table 3.3.

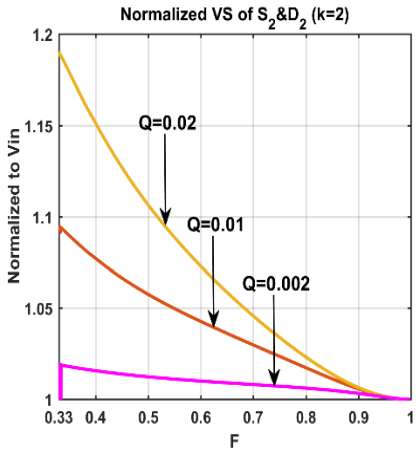


Fig. 3.15. Voltage stress of S_2, D_2 in the Cuk DRC

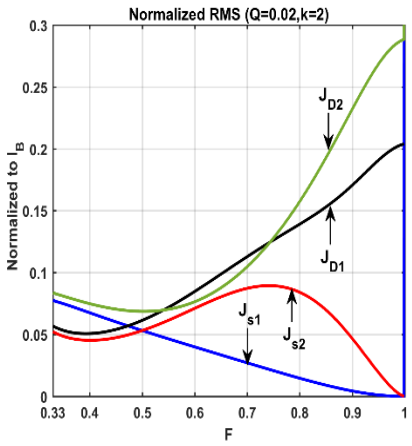


Fig. 3.16. Current stress of switches in the Cuk DRC

Table 3.3. Prototype specifications of the Cuk DRC

P	<120W	F	0.33~0.9
V_{in}	48V	C_r	1uF
V_{out}	62~94.6V	L_{r1}	2.5uH
f_s	67-180kHz	L_{r2}	10uH
f_{r1}	100kHz	$D_{1,2}$	8TQ080GPBF
f_{r2}	50kHz	$S_{1,2}$	FDPF770N15A

3.8.2 Experimental and Simulation Results

In this part, an open-loop prototype was built and tested. The three load resistances are measured to be 80.7Ω, 160.8Ω and 801.4Ω, i.e. Q=0.0196, 0.00983, 0.00197.

In the previous analysis, all devices are considered to be ideal. However, the parasitic capacitance of S_1 (C_{ds1}) affects the converter operation. From the experimental waveform in Fig. 3.17, the $i_{L_{r1}}$ doesn't start resonating from zero. In addition, the $i_{L_{r1}}$ continues resonating with much higher frequency after V_{gs1} becomes low. Consequently, the operating waveform is different from the theoretical one in Fig. 3.2(a). The above phenomenon is caused by the C_{ds1}. During t_0~t_1, the C_{ds1} and L_{r1} resonates through S_2. During t_1~t_2, the anti-parallel diode of S_1 should be blocked by C_{r1} in theory, so no reverse current is conducted. In practice, the reverse current can flow through C_{ds1} for a short

period until C_{ds1} is fully discharged. In order to ensure the normal operation, a Schottky diode (D_B) is cascaded in series with S_1 to block the reverse current.

After adding the blocking diode, the waveforms of $i_{L_{r1,2}}$ and V_{Cr} under different switching frequencies are shown in Fig. 3.18. The corresponding waveforms of V_{in} and V_{out} are shown in Fig. 3.19.

In Fig. 3.18(a), f_s is 67kHz (F=0.33) and the converter operates on the boundary between the regulated mode and the unregulated mode. As shown, both $i_{L_{r1}}$ and $i_{L_{r2}}$ are the positive half sinusoidal waves and they do not overlap. From Fig. 3.19(a), the V_{in} is 48V and the V_{out} is 91.2V. The maximum gain under Q=0.00196 is achieved at 1.9.

In Fig. 3.18(b), f_s is 100kHz (F=0.5) and the converter operates in the regulated mode. As shown, the $i_{L_{r1}}$ and $i_{L_{r2}}$ overlap for about 0.6us. The $i_{L_{r1}}$ is still a positive half sinusoidal wave because the on-time of S_1 is fixed at 5us. The $i_{L_{r2}}$ resonates and then decrease linearly, matching the waveforms in Fig. 3.2(a). From Fig. 3.19(b), the V_{in} is 48V and the V_{out} is 87.1V, so the conversion ratio is decreased to 1.81.

In Fig. 3.18(c), f_s is 140kHz (F=0.7) and the converter operates in the regulated mode. As shown, the $i_{L_{r1}}$ and $i_{L_{r2}}$ overlap for about 1.6us. The waveforms of $i_{L_{r1}}$ and $i_{L_{r2}}$ match Fig. 3.2(a) closely. From Fig. 3.19(c), the V_{in} is 48V and the V_{out} is 73.8V, so the conversion ratio is further decreased to 1.54.

The simulated and experimental gain curves are plotted in Fig. 3.20, where the solid lines represent the theoretical gain curves, while the dashed lines represent the simulated or experimental ones. The simulation parameters are the same as the Table 3.3 and all parasitic elements are ignored. From Fig. 3.20(a), the simulated gain curve matches the theoretical curve closely under different quality factors. From Fig. 3.20(b), the maximum

gain is about 1.97, peaking at 67kHz (F=0.33) when Q=0.00197. At very light load condition (Q=0.00197, 1/10 of the rated power), the voltage gain can be decreased to 1.47 at $f_s = 180kHz$, which is a significant advantage compared to [21]. For Q=0.00983, the voltage gain changes from 1.93 to 1.45 by regulating f_s from 67kHz to 160kHz. For Q=0.00196, the voltage gain changes from 1.9 to 1.3 within the same frequency range. The deviations of the experimental curves from the theoretical ones are mainly caused by ESRs, diode forward voltage and parasitic capacitances. However, the profile of the experimental gain curve is close to the analysis, verifying the continuous conversion ratio.

Two power meters (Chroma 66202) were used to record the input and output power, and the efficiency curves under open loop are given in Fig. 3.21(a), where the solid lines represent the experimental curves, while the dashed lines represent the estimated curves with considering the conduction loss only. In Fig. 3.21(a), the V_{in} is 48V and the output is unregulated while varying the f_s. When Q=0.00197, the experimental peak efficiency is 97.8% at 80kHz (F=0.4). When Q=0.00983, the experimental peak efficiency is 97% at 80kHz (F=0.4). As the f_s increases, the efficiency is decreasing to the minimum value 94.3% at 160kHz (F=0.8). At heavier load (Q=0.0196), the experimental peak efficiency is 96.75% at 80kHz (F=0.4) and the minimum value is 94% at 160kHz (F=0.8). According to the analyses in section 3.5.3, the estimated efficiency curves are plotted with dashed lines. The estimated curves do not include the turn-of loss of the transistors, dead-time loss or the conduction loss on the newly added blocking diode (D_B), so the estimated efficiency curves are well above the experimental ones. In Fig. 3.21(b), the V_{in} is 48V and the voltage gain is regulated to be at 1.8 or 1.5 when the load current is varying. When the voltage gain is fixed at 1.8, the overall efficiency is above 95.5% and the peak efficiency is 96.15% at 0.54A.

When the voltage gain is fixed 1.5, the overall efficiency is above 93.8% and the peak efficiency is 94.4% at 0.45A.

The estimated power loss distribution when $f_s = 100kHz$ and Q=0.0196 is shown in Table 3.4. At this operating point, the input power P_{in} is 97.3W and the output power P_{out} is 93.2W. As listed, the loss of the diodes is dominant. To further improve the efficiency, $D_{1,2}$ may be replaced by MOSFETs to achieve synchronous rectification. In addition, the blocking diode D_B may be removed by proper design, which will be the focus of our future work. The switching loss $P_{sw.}$ of the switches is the second highest. Even though $S_{1,2}$ are turned on with ZCS operation, ZVS operation is preferred to reduce the turn-on loss caused by the parasitic drain-source capacitance of the MOSFETs. Moreover, the deadtime incurs additional switching losses.

Table 3.4. Power loss distribution of the Cuk DRC

Device	ESR or V_f	RMS Current (A)	Average Current (A)	Power Loss (W)	Loss Ratio
S_1	80mΩ	1.62	-	0.21	5.1%
S_2	80mΩ	1.62	-	0.21	5.1%
D_1	0.72V	-	1.2	0.86	21%
D_2	0.72V	-	1.2	0.86	21%
D_B	0.72V	-	1	0.72	17.6%
L_{r1}	2.5mΩ	1.62	-	0.0066	0.16%
L_{r2}	10mΩ	1.87	-	0.035	0.85%
$P_{sw.}$	-	-	-	1.2	29.2%

To further demonstrate the continuously adjustable conversion ratio of the family of step-up RSC. The conversion ratios of 3X SP/Fibonacci SCC, 4X SP SCC and 4X resonant VD are simulated and given in Fig. 3.22. As shown, the simulated results (dashed line) match the theoretical curves (solid line) closely.

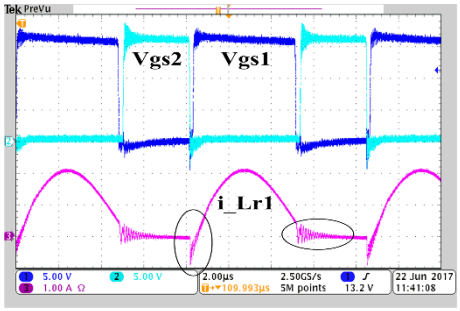
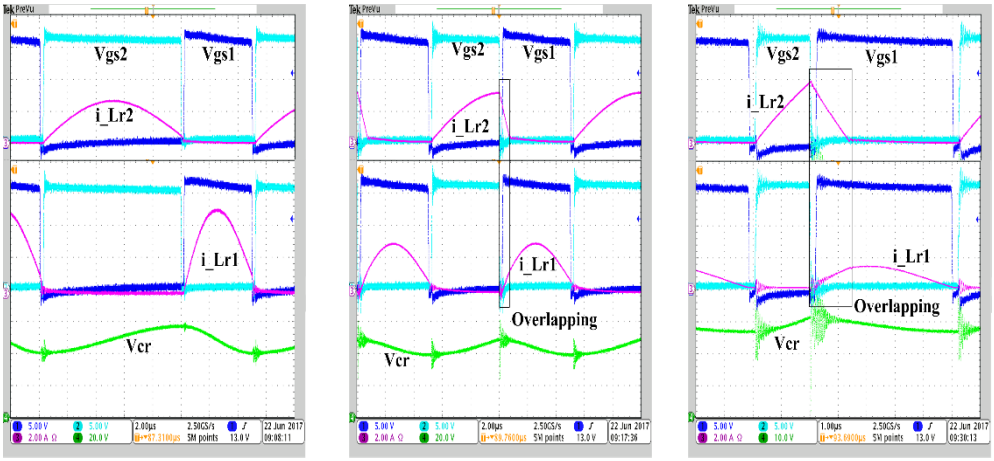
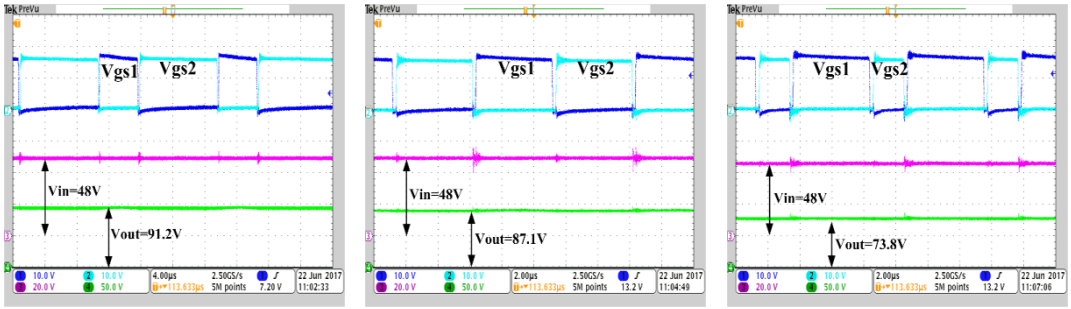


Fig. 3.17. Waveform of i_{Lr1} without blocking diode
$(f_s = 120kHz, Q = 0.0196)$



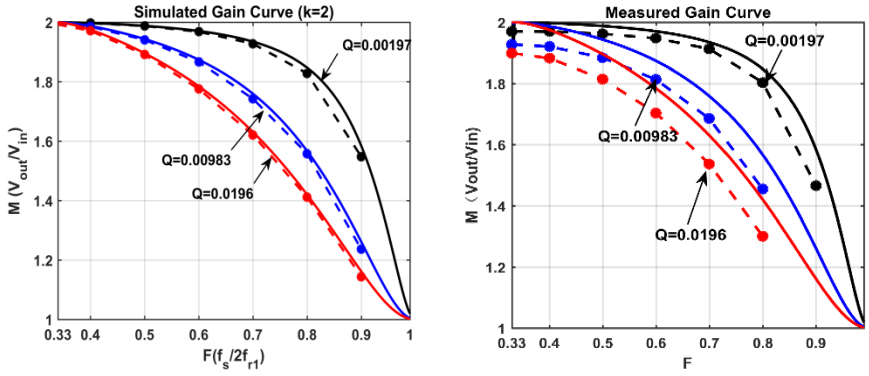
(a) $f_s = 67kHz$ (b) $f_s = 100kHz$ (c) $f_s = 140kHz$

Fig. 3.18. Waveforms of $i_{Lr1,2}, V_{cr}$ with blocking diode $(Q = 0.0196)$
$(V_{gs1,2}: 5v/div\,; i_{Lr1,2}: 2A/div\,;\ V_{cr}: (a) - (c)\ 20v/div\,, (d) 10v/div)$



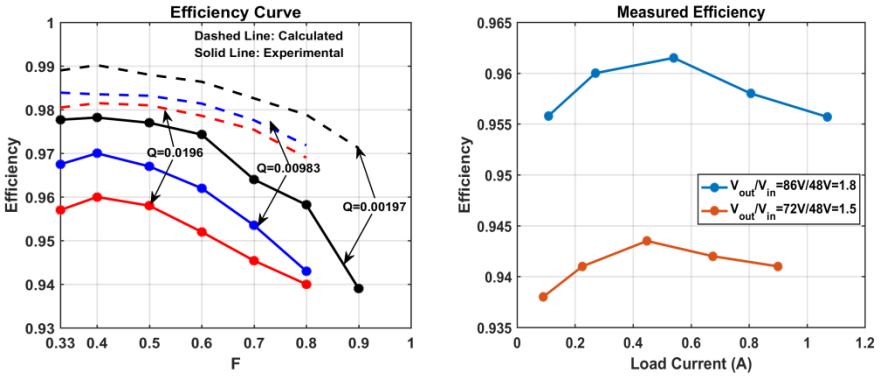
(a) $f_s = 67kHz$ (b) $f_s = 100kHz$ (c) $f_s = 140kHz$

Fig. 3.19. Waveforms of V_{in}, V_{out} of in the Cuk DRC $(Q = 0.0196)$
$(V_{gs1,2}: 5v/div\,; V_{in}: 20V/div\,;\ V_{out}: 50v/div)$



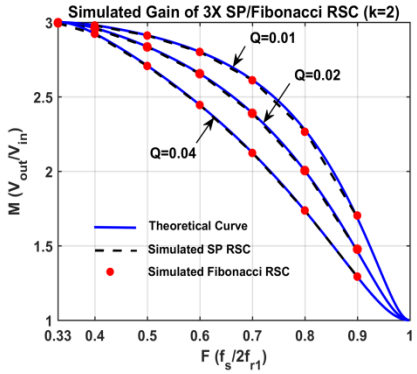
(a) Simulated curve (b) Experimental curve

Fig. 3.20. Gain curve comparison of the Cuk DRC

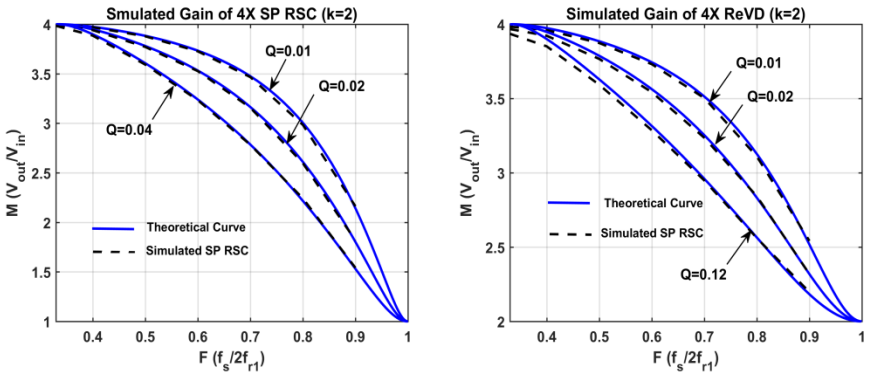


(a) Efficiency v.s F (b) Efficiency v.s load current

Fig. 3.21. Measured efficiency of in the Cuk DRC



(a) 3X SP/Fibonacci RSC



(b) 4X SP RSC (c) 4X Resonant VD

Fig. 3.22. Simulated gain curves of different topologies

3.9 Conclusion

In this chapter, the Cuk DRC is adapted for step-up resonant switching capacitor application forming a family of step-up RSCs with members including the Series-parallel SCC, Fibonacci SCC and the VD. This family breaks through the limitation of voltage regulation that was previously bounded to the nominal voltage ratio inherent to the traditional SCC topologies. The new family is suitable for applications requiring small size, high efficiency, and wide regulation range.

A comprehensive analysis about the operation principle, voltage-gain curve and voltage/current stresses of the resonant tank is given. A 48V to 62~94.6V prototype was built that provides the peak efficiency 97.8% and maximum power 120W. This efficiency is achieved with a diode rectifier instead of a synchronous one. The experimental waveforms of the inductor current verify the overlapping interval, and the measured and simulated gain curves prove the good regulation capability of the Cuk DRC.

3.10 References

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CHAPTER 4: A Cuk Dual Resonance Core-Based Dickson Resonant Switched-Capacitor with Continuous Conversion Ratio

4.1 Introduction

As mentioned in the previous chapter, the Cuk dual resonance core (DRC) can be extended to the Dickson Switched-Capacitor Converter (SCC) with proper modification. In this chapter, a Cuk DRC-based Dickson Resonant Switched-capacitor Converter (Cuk DDRSC) was proposed. With on-time fixed frequency modulation, all transistors are turned on with ZCS operation and all diodes are turned off with ZCS operation, eliminating the switching loss caused by the reverse recovery current. Most importantly, the conversion ratio of the Cuk DDRSC can be regulated continuously and efficiently, even at light load condition.

4.2 Nomenclature

$\mathbf{C_{1,2,\dots N}}$, $\mathbf{C_{out}}$:Intermediate capacitors and output capacitor;

$\mathbf{C_{r1,2}}$:Resonant capacitors, both with capacitance C_r;

$\mathbf{D_{1,2,\dots N}}$:Power diodes;

$\boldsymbol{f_{r1,2}}$:Resonant frequencies with $f_{r1} = \frac{1}{2\pi\sqrt{2L_{r1}C_r}}$ and $f_{r2} = \frac{1}{2\pi\sqrt{L_rC_r}}$;

$\boldsymbol{f_s}$:Switching frequency;

F: Frequency ratio with $F = t_{on}/T_s = f_s/2f_{r1}$;

$\boldsymbol{h}$: An intermediate variable with $h = cos2\pi\left(\frac{f_{r2}}{f_s} - \frac{\sqrt{2}}{2k}\right)$;

$\boldsymbol{i_{Lr1,2,3}(t)}$, $\boldsymbol{I_{Lr1,2,3}}$: Transient and average inductor currents;

$\boldsymbol{i_{s1,2\dots N}(t)}$, $\boldsymbol{i_{D1,2\dots N}(t)}$: Transient current flowing through $S_{1,2,\dots N}$, $D_{1,2,\dots N}$;

$\boldsymbol{i_{c1,2\dots N}(t)}$, $\boldsymbol{i_{Cout}(t)}$, $\boldsymbol{i_{cr1,2}(t)}$:Transient current flowing into $C_{1,2,\dots N}$, C_{out}, $C_{r1,2}$;

$\boldsymbol{k}$: the relationship between L_{r1} and $L_{r2,3}$ with $L_{r2,3} = L_r = k^2L_{r1}$;

$\mathbf{L_{r1}}$, $\mathbf{L_{r2,3}}$:Resonant inductors, with $L_{r2} = L_{r3} = L_r$;

m: An intermediate variable with m=$C_r R_L f_s$;

$\boldsymbol{M_{cr1,2\_max}}$: Normalized maximum value of $V_{cr1,2}(t)$ to V_{in};

$\boldsymbol{M_{cr1,2\_min}}$:Normalized minimum value of $V_{cr1,2}(t)$ to V_{in};

M: voltage gain of V_o to V_{in};

Q: Quality factor with Q = $\sqrt{L_{r1}/2C_r}/R_L$;

$\mathbf{R_L}$:Load resistance;

$\mathbf{S_{1,2,3\ldots N}}$:MOSFETs;

$\boldsymbol{t_{on}}$:Turn-on time of S_1 with $t_{on} = 1/2f_{r1}$;

$\boldsymbol{V_{in}}$, $\boldsymbol{V_o}$:Input and output voltage;

$\boldsymbol{V_{cr1,2}(t)}$:Voltage across $C_{r1,2}$;

$\boldsymbol{V_{c1}}$:Voltage across C_1;

$\boldsymbol{V_{cr1,2\_max}}$, $\boldsymbol{V_{cr1,2\_min}}$:Maximum and minimum values of $V_{cr1,2}(t)$;

4.3 Topology and Operation Principle

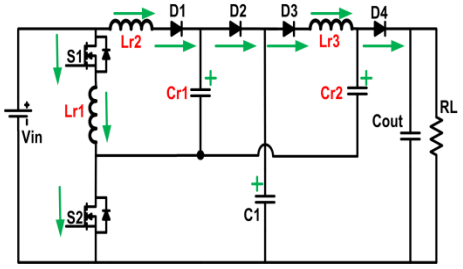
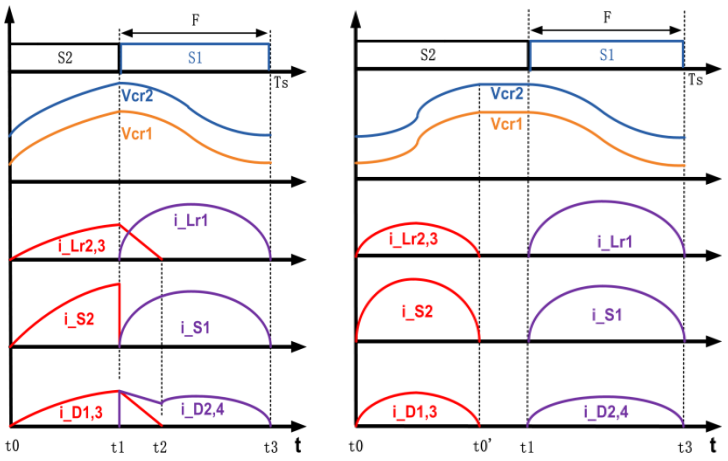


Fig 4.1. Topology of the 3X Cuk DDRSC



(a) Regulated mode (b) Unregulated mode

Fig 4.2. Operating waveforms

The topology of the 3X Cuk DDRSC is shown in Fig. 4.1. The resonant inductor L_{r1} is in series with S_1, while L_{r2} and L_{r3} are in series with D_1 and D_3 respectively. C_{r1} and C_{r2} are the resonant capacitors, while C_1 is the intermediate capacitor bank and the C_{out} is the output capacitor, both with much higher capacitance value than C_{r1} and C_{r2}. To simplify the operation states, the values of L_{r2} and L_{r3} both are equal to L_r, and the values of C_{r1} and C_{r2} both are equal to C_r.

The first resonant path consists of L_{r1} and $2C_r$ (C_{r1} and C_{r2} are in parallel) with resonant frequency $f_{r1} = \frac{1}{2\pi\sqrt{2L_{r1}C_r}}$. The second resonant path consists of L_{r2} and C_{r1} and the third one consists of L_{r3} and C_{r2}, both with resonant frequency $f_{r2} = \frac{1}{2\pi\sqrt{L_rC_r}}$.

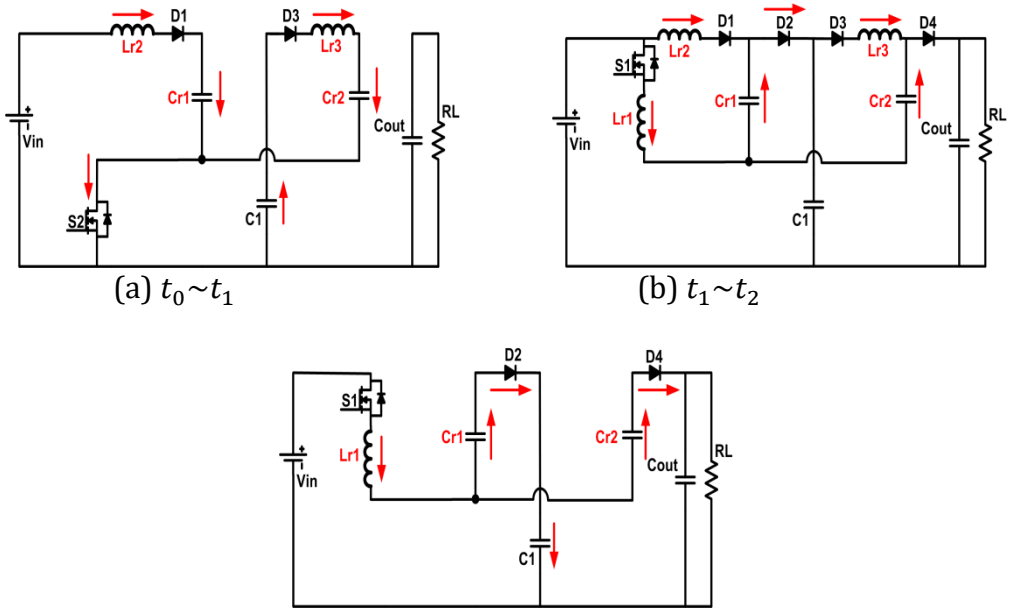
The on-time fixed frequency modulation control is adopted – that is, the turn-on time of S_1 is fixed at $t_{on} = \frac{1}{2f_{r1}}$. By varying the switching frequency f_s, two operation modes can be obtained, as given in Fig. 4.2.

Fig. 4.2(a) shows the operating waveforms in the regulated mode, in which there exists an overlapping period between i_{Lr1} and $i_{Lr2,3}$. By introducing the overlapping period, the

conversion ratio of Cuk DDRSC can be different from the target value which is determined by the circuit configuration and can be varied continuously.

Fig. 4.2(b) shows the operating waveforms in the unregulated mode, where the i_{Lr1} does not overlap with i_{Lr2} or i_{Lr3}. This mode is similar to the operation of traditional ZCS resonant SCCs, and the voltage gain is almost fixed.

4.4 Conversion Ratio Curve



(a) $t_0 \sim t_1$ (b) $t_1 \sim t_2$

(c) $t_2 \sim t_3$

Fig. 4.3. Operating states

In this section, the conversion ratio of the 3X Cuk DDRSC in regulated mode will be discussed, since the voltage gain in the unregulated mode is almost fixed at 3. Several assumptions are made as follows. The C_1 and C_{out} are large enough, so the voltage across them is approximated to be constants V_{C1} and V_{out}. Equivalent Series Resistances (ESRs) of capacitors, parasitic components of switches and forward voltage of diodes are neglected for simplicity.

The defined positive directions are denoted with green arrows in Fig. 4.1. The operating waveforms and operating states in the regulated mode are shown in Fig. 4.2(a) and Fig. 4.3, respectively.

$[t_0 - t_1]$: At t_0, transistor S_2 and diode $D_{1,3}$ start conducting the resonant current with ZCS turn-on, as shown in Fig. 4.3(a). During this interval, the V_{in} charges C_{r1}, while V_{C1} charges C_{r2}. In this state, the KVL and KCL equations are obtained as:

$$V_{in} - L_{r2}\frac{di_{Lr2}(t)}{dt} - V_{cr1}(t) = 0 \quad (1)$$

$$C_{r1}\frac{dV_{cr1}(t)}{dt} = i_{Lr2}(t) \quad (2)$$

Where the boundary condition is $i_{Lr2}(t_0) = 0, V_{cr1}(t_0) = V_{cr1\_min}$.

$$V_{c1} - L_{r3}\frac{di_{Lr3}(t)}{dt} - V_{cr2}(t) = 0 \quad (3)$$

$$C_{r2}\frac{dV_{cr2}(t)}{dt} = i_{Lr3}(t) \quad (4)$$

Where the boundary condition is $i_{Lr3}(t_0) = 0, V_{cr2}(t_0) = V_{cr2\_min}$.

Based on (1)-(4), the following expressions are obtained:

$$i_{Lr2}(t) = (V_{in} - V_{cr1\_min})\sqrt{\frac{C_r}{L_r}}sin2\pi f_{r2}(t - t_0) \quad (5)$$

$$V_{cr1}(t) = V_{in} - (V_{in} - V_{cr1\_min})cos2\pi f_{r2}(t - t_0) \quad (6)$$

$$i_{Lr3}(t) = (V_{c1} - V_{cr2\_min})\sqrt{\frac{C_r}{L_r}}sin2\pi f_{r2}(t - t_0) \quad (7)$$

$$V_{cr2}(t) = V_{c1} - (V_{c1} - V_{cr2\_min})cos2\pi f_{r2}(t - t_0) \quad (8)$$

Where $L_{r2} = L_{r3} = L_r$, $C_{r1} = C_{r2} = C_r$, and thus $f_{r2} = \frac{1}{2\pi\sqrt{L_r C_r}}$.

$[t_1 - t_2]$: According to the equivalent circuits in Fig. 4.3(b) (c), the following equation is held in $[t_1 - t_2]$ and $[t_2 - t_3]$:

$$V_{cr1}(t) - V_{cr2}(t) = V_o - V_{c1} \quad (9)$$

As a result,

$$C_r \frac{dV_{cr1}(t)}{dt} = C_r \frac{dV_{cr2}(t)}{dt} = i_{cr1}(t) = i_{cr2}(t) \quad (10)$$

At t_1, transistor S_2 is turned off and S_1 is turned on with ZCS operation. Since $i_{Lr2}(t)$ and $i_{Lr3}(t)$ have not resonated to zero, they continue flowing through $D_{1,3}$ and decreasing linearly with the slope of $(V_{in} - V_{c1})/L_r$ and $(V_{c1} - V_o)/L_r$ respectively. Meantime, the new resonant path consists of L_{r1} and $2C_r$ (C_{r1} and C_{r2} are in parallel) starts resonating through S_1 as shown in Fig. 4.3(b). During this interval, the waveform of i_{Lr1} and $i_{Lr2,3}$ will overlap. In this state, the KVL equations are obtained as:

$$V_{in} - V_{c1} = L_{r2} \frac{di_{Lr2}(t)}{dt} \quad (11)$$

$$V_{in} - L_{r1} \frac{di_{Lr1}(t)}{dt} + V_{cr1}(t) - V_{c1} = 0 \quad (12)$$

$$V_{c1} - V_o = L_{r3} \frac{di_{Lr3}(t)}{dt} \quad (13)$$

$$V_{in} - L_{r1} \frac{di_{Lr1}(t)}{dt} + V_{cr2}(t) - V_o = 0 \quad (14)$$

Based on (10), the current flowing through the resonant capacitor $C_{r1,2}$ is:

$$C_r \frac{dV_{cr1}(t)}{dt} = C_r \frac{dV_{cr2}(t)}{dt} = -\frac{1}{2} i_{Lr1}(t) \quad (15)$$

From Fig. 4.2(a), the boundary conditions are:

$$i_{Lr1}(t_1) = 0, V_{cr1}(t_1) = V_{cr1\_max}, V_{cr2}(t_1) = V_{cr2\_max} \quad (16)$$

Based on (12) (14)-(16), the following expressions are obtained:

$$i_{Lr1}(t) = (V_{in} - V_{c1} + V_{cr1\_max}) \sqrt{\frac{2C_r}{L_{r1}}} sin2\pi f_{r1}(t - t_1) \quad (17)$$

$$V_{cr1}(t) = -(V_{in} - V_{c1}) + (V_{in} - V_{c1} + V_{cr1\_max}) cos2\pi f_{r1}(t - t_1) \quad (18)$$

$$i_{Lr1}(t) = (V_{in} - V_o + V_{cr2\_max})\sqrt{\frac{2C_r}{L_{r1}}} sin2\pi f_{r1}(t - t_1) \quad (19)$$

$$V_{cr2}(t) = -(V_{in} - V_o) + (V_{in} - V_o + V_{cr2\_max})cos2\pi f_{r1}(t - t_1) \quad (20)$$

Where $C_{r1} = C_{r2} = C_r$, and thus $f_{r1} = \frac{1}{2\pi\sqrt{2L_{r1}C_r}}$.

The two expressions of $i_{Lr1}(t)$ should be equivalent, so the following expression is derived according to (17) (19):

$$V_o - V_{c1} = V_{cr2\_max} - V_{cr1\_max} \quad (22)$$

$[t_2 - t_3]$: At t_2, $i_{Lr2,3}(t)$ decrease to zero at the same time and $D_{1,3}$ are turned off with ZCS operation. Transistor S_1 and diode $D_{2,4}$ continue conducting the resonant current as Fig. 4.3(c). The expressions of resonant current and voltage are the same as (17)-(20). At t_3, the $i_{Lr1}(t)$ resonates to zero and S_1, $D_{2,4}$ will be turned off with ZCS operation.

During $t_0 - t_1$, the net charge flowing into C_{r1} and C_{r2} is:

$$q_{cr1\_t_0 \sim t_1} = C_r\left(V_{cr1\_max} - V_{cr1\_min}\right) = \int_{t_0}^{t_1} i_{Lr2}(t)dt \quad (23)$$

$$q_{cr2\_t_0 \sim t_1} = C_r\left(V_{cr2\_max} - V_{cr2\_min}\right) = \int_{t_0}^{t_1} i_{Lr3}(t)dt \quad (24)$$

According to (15) and the charge balance of the resonant capacitors, the net charge flowing out of C_{r1} and C_{r2} during $t_1 - t_3$ is:

$$q_{cr1_{t_1 \sim t_3}} = C_r\left(V_{cr1\_min} - V_{cr1\_max}\right) =$$

$$q_{cr2\_t_1 \sim t_3} = C_r\left(V_{cr2\_min} - V_{cr2\_max}\right) = -\frac{1}{2}\int_{t_1}^{t_3} i_{Lr1}(t)dt \quad (25)$$

According to the expressions and the boundary conditions of $i_{Lr2,3}(t)$ in (5)(7), and (22)-(25), the following expression is derived:

$$V_o - V_{c1} = V_{cr2\_max} - V_{cr1\_max} = V_{cr2\_min} - V_{cr1\_min} = V_{c1} - V_{in} \quad (26)$$

Assuming that $L_r = k^2 L_{r1}(k > 0)$, so

$$\frac{f_{r1}}{f_{r2}} = \sqrt{\frac{L_r}{L_{r1}}} = k \tag{27}$$

Since the turn-on time of S_1 is fixed at $t_{on} = \frac{1}{2f_{r1}}$, so

$$t_3 - t_1 = \frac{1}{2f_{r1}} \text{ and } t_1 - t_0 = \frac{1}{f_s} - \frac{1}{2f_{r1}} \tag{28}$$

According to (5) (23) (27)(28), the intermediate variable is obtained:

$$h = cos2\pi\left(\frac{f_{r1}}{kf_s} - \frac{\sqrt{2}}{2k}\right) = \frac{(V_{cr1\_max} - V_{in})}{(V_{cr1\_min} - V_{in})} \tag{29}$$

In each period, the following equation is held in every interval:

$$i_{Lr2}(t) = i_{cr1}(t) + i_{D2}(t) = i_{cr1}(t) + i_{c1}(t) + i_{Lr3}(t)$$

$$= i_{cr1}(t) + i_{c1}(t) + i_{cr2}(t) + i_{Cout}(t) + \frac{V_{out}}{R_L} \tag{30}$$

According to the charge balance on $C_{r1,2}$ and C_{out}, the average value of $i_{cr1,2}(t)$, $i_{c1}(t)$ and $i_{Cout}(t)$ in one switching cycle is equal to zero, so

$$I_{Lr2} = f_s \int_{t_0}^{t_2} i_{Lr2}(t)\mathrm{dt} = f_s\left(\int_{t_0}^{t_1} i_{Lr2}(t)\mathrm{dt} + \int_{t_1}^{t_2} i_{Lr2}(t)\mathrm{dt}\right) = \frac{V_{out}}{R_L} \tag{31}$$

The expressions of $i_{Lr2}(t)$ in $[t_1 - t_2]$ and $[t_2 - t_3]$ are given in (5) (11), and the expression of $\int_{t_0}^{t_1} i_{Lr2}(t)\mathrm{dt}$ is given in (23). So the following expression is found:

$$sin^2 2\pi\left(\frac{f_{r1}}{kf_s} - \frac{\sqrt{2}}{2k}\right) = 1 - h^2 = \frac{((V_{cr1\_min} + V_{cr1\_max})[\frac{V_o}{m} - (V_{cr1\_max} - V_{cr1\_min})]}{(V_{cr1\_min} - V_{in})^2}$$

$$\text{Where m=} C_r R_L f_s \tag{32}$$

In addition, with the expression of h in (29), the voltage gain is:

$$\frac{V_{out}}{V_{in}} = \frac{2m(V_{cr1\_max} - V_{cr1\_min})}{V_{cr1\_max} + V_{cr1\_min}} \tag{33}$$

According to (26) (29) (33), the following expressions are derived:

$$M_{cr1\_max} = \frac{V_{cr1\_max}}{V_{in}} = \frac{h^2(2m-3) + h(A-2m-1) + 2}{2(h+1)^2}$$

where $A = \sqrt{h^2(4m^2 - 20m + 1) + h(2 - 8m^2) + 4m^2 + 20m + 1}$ (34)

$$M_{cr1\_min} = \frac{V_{cr1\_min}}{V_{in}} = -m - M_{cr1\_max} - \frac{1}{2} + \frac{\sqrt{4m^2+4m(1+4M_{cr\_max})+1}}{2} \quad (35)$$

$$M = \frac{V_{out}}{V_{in}} = \frac{2m(M_{cr1\_max}-M_{cr1\_min})}{M_{cr1\_max}+M_{cr1\_min}} \quad (36)$$

In order to plot the conversion ratio curve, two parameters are defined as follows:

Frequency Ratio: $F = \frac{t_{on}}{T_s} = \frac{f_s}{2f_{r1}}$;

Quality Factor: $Q = \frac{Z_{r1}}{R_L}$, $Z_{r1} = \sqrt{L_{r1}/2C_r}$ (37)

The numerator of the quality factor is the impedance of the resonant tank, while the denominator is the equivalent load resistance. From the definition of Q, one can see the higher Q represents the higher load current once the resonant tank is determined. As a result, the relationships between h, m and F, Q are found as shown below:

$$h = cos2\pi\left(\frac{f_{r1}}{kf_s} - \frac{\sqrt{2}}{2k}\right) = \cos\pi\left(\frac{\sqrt{2}}{Fk} - \frac{\sqrt{2}}{k}\right) \quad (38)$$

$$m = C_r R_L f_s = \frac{F}{Q}\frac{1}{2\pi} \quad (39)$$

The converter will enter regulated mode if:

$$\frac{1}{2f_{r1}} + \frac{1}{2f_{r2}} > \frac{1}{f_s} \quad (40)$$

Consequently, the boundary between regulated mode and unregulated mode 2 is:

Regulated Mode: $\frac{\sqrt{2}}{k+\sqrt{2}} < F < 1$ (41)

Considering the boundary condition (41) and substituting (38) (39) into (34)- (36), the complete expression of conversion ratio in terms of Q and F can be derived. For simplicity, the complete expression is not given, while the graphical conversion ratio curves with k^2=8 is plot in Fig. 4.4.

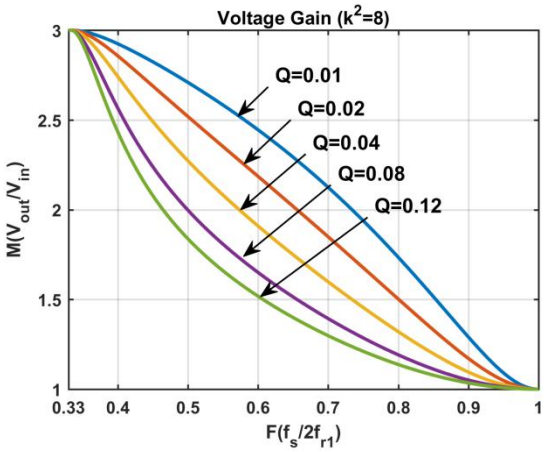


Fig. 4.4. Voltage gain curve ($k^2 = 8$)

As seen from the derived gain curve, when $\frac{\sqrt{2}}{k+\sqrt{2}} < F < 1$, the conversion ratio of the resonant core can be well adjusted by changing F. At heavy load (high Q), the Cuk DDRSC has wide voltage regulation range when F below the upper limit 1. At light load (smaller Q), the regulation capability will be retained, which is an advantage compared to the poor light load regulation capability in chapter 1 and 2. However, the light load condition may cause stability issue if the switching frequency is approaching the upper limit 1.

In order to verify the theoretical gain, a circuit with $V_{in} = 48V$, $L_{r1} = 1.25uH$, $L_{r2,3} = 10uH$, $C_{r1,2} = 1uH$, $R_L = 80\Omega, 160\Omega, 800\Omega$ (Q=0.01, 0.005,0.001) is simulated using Psim. The switching frequency is varied from 67k-180k (0..3<F<0.9) to regulate the output voltage. The simulated gain curves under different load conditions are given in Fig. 4.5. As shown, the simulated results (dashed line) match the calculated results (solid line) closely, demonstrating the validity of the derived formulas.

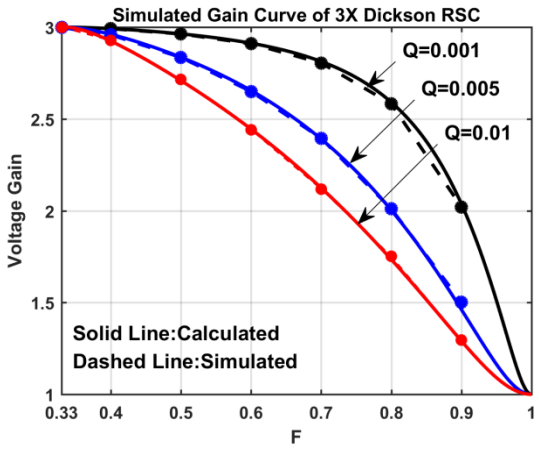


Fig. 4.5. Simulated gain curve ($k^2 = 8$)

4.5 Conclusions

In this chapter, the Cuk DRC is extended to a 3X Dickson SCC to form a 3X Cuk DDRSC, so the voltage gain can be regulated within a wide range, even at light load condition. The theoretical gain curve is derived, which is verified by simulation results, demonstrating the continuously adjustable conversion ratio, even at 1/10 of the heavy load condition.

CHAPTER 5: Comparison of Different Step-up Dickson Resonant Switched-capacitor Converters

5.1 Introduction

According to the analysis in chapter 1-4, Ladder SCC, Dickson SCC and TBSC can adopt the concept of above-resonance operation to achieve ZVS operation and wide line regulation capability. In addition, Fibonacci SCC, SP SCC, VD and Dickson SCC can adopt the Cuk DRC to improve the line regulation capability, even at the light load condition. It's noteworthy that only Dickson SCC can adopt both methods (the resonant configuration in chapter 1 or the Cuk DRC in chapter 3) to improve the regulation capability. In this chapter, different topologies of step-up Dickson RSC are introduced and a comparison about operation principle, operating waveforms and regulation capability is given.

5.2 Dickson RSC with "Indirect" Resonant Core

The topology of 3X Dickson RSC with "indirect" resonant core is shown in Fig. 5.1, which is exactly the same as that in [1]. However, the converter in [1] operates below the resonance with ZCS operation for both transistors and diodes, and its voltage gain variation range is very limited. For the converter in the part, it operates above the resonance, so the transistors are ZVS turn-on and diodes are ZCS turn-off. In addition, the output voltage can be regulated within a wide range by frequency modulation. In this part, the voltage gain of 3X Dickson RSC ($f_r < f_s < 2f_r$) is analyzed in details. The operating waveforms and states within $f_r < f_s < 2f_r$ are given in Fig. 5.2 and Fig. 5.3.

In Fig. 5.1, the S_1 and S_2 are the main switches with internal anti-parallel diodes. D_1~ D_4 are power diodes. A resonant inductor L_r and two small film capacitors $C_{r1,2}$ constitute the resonant tank. Capacitors C_1 works as the charge bank with relatively large capacitance.

As shown in Fig. 5.2, the duty cycle of the main switches S_1 and S_2 is fixed at 0.5 and their driving signals are complimentary with a short dead-time to avoid shoot-through. The

voltage across $C_{r1,2}$ is denoted as $V_{cr1,2}(t)$ and the maximum /minimum voltage values across them are represented by $V_{cr1,2\_max}/V_{cr1,2\_min}$ respectively. The currents flowing through the resonant inductor L_r, switches $S_{1,2}$ and diodes $D_1 \sim D_4$ are represented by $i_{Lr}(t)$, $i_{s1,2}(t)$ and $i_{D1\sim D4}(t)$ respectively. The defined positive directions of current and voltage are highlighted in green arrows and plus signs in Fig. 5.1.

In order to simplify the steady-state analysis, several assumptions are made as follows. The capacitances of C_{r1} and C_{r2} are both equal to C_r, while the capacitance of C_1 is much larger compared to C_r, so the voltage on C_1 is considered to maintain at a constant value V_c in one switching cycle. Similarly, the output voltage is regarded as a constant value V_o in one switching cycle. ESRs of all capacitors, on-resistance of switches and forward voltage of diodes are neglected. The parasitic capacitances of the transistors and diodes are considered to be very small, so the charging/discharging time of parasitic capacitances are neglected. Dead-time between the complimentary driving signals is neglected in steady-state calculation.

First, KVL and KCL equations in each switching modes are obtained.

$[t_0 \sim t_1]$: In this state, there are two charging loops denoted in blue arrows, as shown in Fig. 5.3(a). The KVL and KCL equations are obtained as:

$$L_r \frac{di_{Lr}(t)}{dt} + V_{cr1}(t) - V_C = 0 \quad (1)$$

$$L_r \frac{di_{Lr}(t)}{dt} + V_{cr2}(t) - V_o = 0 \quad (2)$$

$$C_r \frac{dV_{cr1}(t)}{dt} = \frac{1}{2} i_{Lr}(t) \ (C_{r1} = C_{r2} = C_r) \quad (3)$$

From Fig. 5.2, the boundary conditions are:

$$i_{Lr}(t_1) = 0, V_{cr1}(t_1) = V_{cr1\_min} \quad (4)$$

Based on (1) - (4):

$$i_{Lr}(t) = (V_C - V_{cr1\_min})\sqrt{\frac{2C_r}{L_r}}sin2\pi f_r(t - t_1) \quad (5)$$

$$V_{cr1}(t) = V_C - (V_C - V_{cr1\_min})cos2\pi f_r(t - t_1), \text{ where } f_r = \frac{1}{2\pi\sqrt{2L_rC_r}} \quad (6)$$

$$V_o = V_C + [V_{cr2}(t) - V_{cr1}(t)] \quad (7)$$

$[t_1 \sim t_2]$: In this state, two charging loops are denoted in blue arrows, as shown in Fig. 5.3. (b). With the same method, the KVL and KCL equations are:

$$V_{in} - L_r\frac{di_{Lr}(t)}{dt} - V_{cr1}(t) = 0 \quad (8)$$

$$V_c - L_r\frac{di_{Lr}(t)}{dt} - V_{cr2}(t) = 0 \quad (9)$$

$$C_r\frac{dV_{cr}(t)}{dt} = \frac{1}{2}i_{Lr}(t)\ (\mathrm{C_{r1}} = \mathrm{C_{r2}} = \mathrm{C_r}) \quad (10)$$

From Fig. 5.2, the boundary conditions are:

$$i_{Lr}(t_1) = 0, V_{cr1}(t_1) = V_{cr1\_min} \quad (11)$$

Based on (8) - (11):

$$i_{Lr}(t) = (V_{in} - V_{cr1\_min})\sqrt{\frac{2C_r}{L_r}}sin2\pi f_r(t - t_1) \quad (12)$$

$$V_{cr1}(t) = V_{in} - (V_{in} - V_{cr1\_min})cos2\pi f_r(t - t_1), \text{ where } f_r = \frac{1}{2\pi\sqrt{2L_rC_r}} \quad (13)$$

$$V_{cr2}(t) - V_{cr1}(t) = V_C - V_{in} \quad (14)$$

$[t_2 \sim t_4]$: This interval is composed of three parts: $t_2 \sim t_3'$, $t_3' \sim t_3$ and $t_3 \sim t_4$. At t_2, transistor S_2 is turned off and then the loop current will charge the parasitic capacitance $\mathrm{C_{ds1}}$ of S_2 and discharge $\mathrm{C_{ds2}}$ of S_1 till t_3', shown in Fig. 5.3(c). As mentioned in the assumptions, the parasitic capacitance is so small and this interval is very short, which is neglected in steady-state analysis. After t_3', the voltage across $\mathrm{C_{ds1}}$ is discharged to zero and then the anti-parallel diode of S_1 starts conducting current, shown in Fig. 5.3(d). At t_3,

transistor S_1 is turned on with ZVS operation, reducing switching loss and thus improving the efficiency. During $[t_2 \sim t_4]$, the KVL and KCL equations are:

$$L_r \frac{di_{Lr}(t)}{dt} + V_{cr1}(t) = 0 \tag{15}$$

$$V_{in} - V_C + L_r \frac{di_{Lr}(t)}{dt} + V_{cr2}(t) = 0 \tag{16}$$

$$C_r \frac{dV_{cr}(t)}{dt} = \frac{1}{2} i_{Lr}(t) \ (\mathrm{C_{r1}} = \mathrm{C_{r2}} = \mathrm{C_r}) \tag{17}$$

From Fig. 5.2, the boundary conditions are:

$$i_{Lr}(t_4) = 0, V_{cr1}(t_4) = V_{cr1\_max} \tag{18}$$

Based on (15) - (18):

$$i_{Lr}(t) = (-V_{cr1\_max}) \sqrt{\frac{2C_r}{L_r}} sin2\pi f_r (t - t_4) \tag{19}$$

$$V_{cr1}(t) = V_{cr1\_max}) cos2\pi f_r (t - t_4), \text{ where } f_r = \frac{1}{2\pi\sqrt{2L_r C_r}} \tag{20}$$

$$V_{cr2}(t) - V_{cr1}(t) = V_C - V_{in} \tag{21}$$

During $[t_1 \sim t_4]$, from Fig. 5.2 and the above analysis, both the resonant current and voltage are composed of two different parts of sinusoidal waveforms and the overall frequency is equal to the switching frequency f_s, i.e.:

$$t_2 - t_0 = t_4 - t_1 = \frac{1}{2}\frac{1}{f_s} \text{ (dead-time is neglected)} \tag{22}$$

According to the resonant current (12) and (19) at t_2:

$$i_{Lr}(t_2) = (V_{in} - V_{cr1\_min}) \sqrt{\frac{2C_r}{L_r}} sin2\pi f_r (t_2 - t_1)$$

$$= (-V_{cr1\_max}) \sqrt{\frac{2C_r}{L_r}} sin2\pi f_r (t_2 - t_4) \tag{23}$$

According to (22), equation (23) can be simplified as:

$$(V_{in} - V_{cr1\_min}) sin2\pi f_r \left(\frac{1}{2}\frac{1}{f_s} + t_0 - t_1\right) + V_{cr1\_max} sin2\pi f_r (t_0 - t_1) = 0 \tag{24}$$

With the same method, according to (13), (20), (22):

$$(V_{in} - V_{cr1\_min})cos2\pi f_r\left(\frac{1}{2}\frac{1}{f_s} + t_0 - t_1\right) + V_{cr1\_max}cos2\pi f_r(t_0 - t_1) = V_{in} \qquad (25)$$

By solving the set of equations (24),(25), the following expression can be derived:

$$cos\frac{f_r}{f_s}\pi = \frac{V_{cr1\_min}^2 - 2V_{in}V_{cr1\_min} + V_{cr1\_max}^2}{2V_{cr1\_min}V_{cr1\_max} - 2V_{cr1\_max}V_{in}} < 0 \ (f_r < f_s < 2f_r) \qquad (26)$$

Secondly, according to (7) and (14) at t_1:

$$V_o = V_C + [V_{cr2}(t) - V_{cr1}(t)] = V_C + [V_{cr2}(t_1) - V_{cr1}(t_1)] = 2V_c - V_{in} \qquad (27)$$

Based on (8), at t_1^+:

$$V_{in} - V_{cr1\_min} - L_r\frac{di_{Lr}(t)}{dt}|t = t_1^+ = 0 \qquad (28)$$

Similarly, according to Fig 5.3(f) at t_4^+:

$$V_{in} + V_{cr1\_max} - V_C + L_r\frac{di_{Lr}(t)}{dt}|t = t_4^+ = 0 \qquad (29)$$

In addition, according to the slope of resonant current at t_1^+ and t_4^+ in Fig. 5.2:

$$\frac{di_{Lr}(t)}{dt}|t = t_1^+ = -\frac{di_{Lr}(t)}{dt}|t = t_4^+ \qquad (30)$$

The following equation is obtained based on (28) – (30):

$$V_C = V_{cr1\_min} + V_{cr1\_max} \qquad (31)$$

As a result, the output voltage is calculated as:

$$V_o = 2V_c - V_{in} = 2\left(V_{cr1\_min} + V_{cr1\_max}\right) - V_{in} \qquad (32)$$

Thirdly, all the charges delivered to the load will be first stored in C_{r1} in each switching cycle according to the charge balance on C_{r1}, i.e.:

$$C_r(V_{cr1\_max} - V_{cr1\_min}) = \frac{V_o}{R_L} * \frac{1}{f_s}, \text{ where } R_L \text{ is the load resistance} \qquad (33)$$

By solving equations (32) and (33):

$$V_{cr\_max} = \frac{(2 + C_rR_Lf_s)V_{cr\_min} - V_{in}}{C_rR_Lf_s - 2} \qquad (34)$$

For simplicity, assume $d = cos\frac{f_r}{f_s}\pi$ and $k = C_r R_L f_s$. Substitute (34) into (26) and solve the equation:

$$M_{cr\_min} = \frac{V_{cr\_min}}{V_{in}} = \frac{(1-d)k^2+(A-d-3)k+6d+6-2A)}{2[(1-d)k^2+4d+4]} \quad (35)$$

$$M_{cr\_max} = \frac{V_{cr\_max}}{V_{in}} = \frac{(k+2)M_{cr\_min}-1}{k-2}$$

$$\text{where A}=\sqrt{(d^2-2d+1)k^2+(2d^2-2)k+d^2+8d+7} \quad (36)$$

Finally, substitute (35), (36) into (32) and the output voltage is calculated as:

$$M = \frac{V_o}{V_{in}} = \frac{k[(1-d)k+2A-4d-4]}{(1-d)k^2+4d+4} \quad (37)$$

In order to derive the voltage gain curve, two parameters are defined as follows:

$$\text{Frequency Ratio: F} = \frac{f_s}{f_r}, where\ f_r = \frac{1}{2\pi\sqrt{2L_rC_r}} \quad (38)$$

$$\text{Quality Factor: Q} = \frac{Z_r}{R_L}, \text{where resonant impedance } Z_r = \sqrt{L_r/2C_r} \quad (39)$$

As a result, the relationships between d, k and F, Q are:

$$d = cos\frac{f_r}{f_s}\pi = \cos(\frac{\pi}{F}) \quad (40)$$

$$k = C_r R_L f_s = \frac{F}{Q} * \frac{1}{4\pi} \quad (41)$$

Substituting (40) and (41) into (37) and then the voltage gain curve in terms of F and Q is plot in Fig. 5.4 when 1<F<2.

Seen from Fig. 5.4, the voltage gain can be regulated within a wide range, compared to the traditional Dickson SCC. At higher load (Q is large), the voltage gain can be varied from 1 to 3 when 1<F<2; while at lighter load (Q is small), the voltage-gain-variation range is narrower. In order to vary the output voltage, the switching frequency need be varied a lot.

At no load condition, the gain curve becomes a straight line, and the regulation capability will be lost totally.

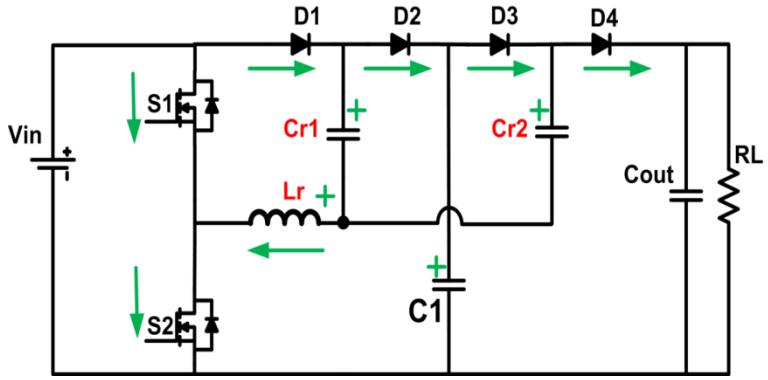


Fig. 5.1. Topology of Dickson RSC with "indirect" resonant core

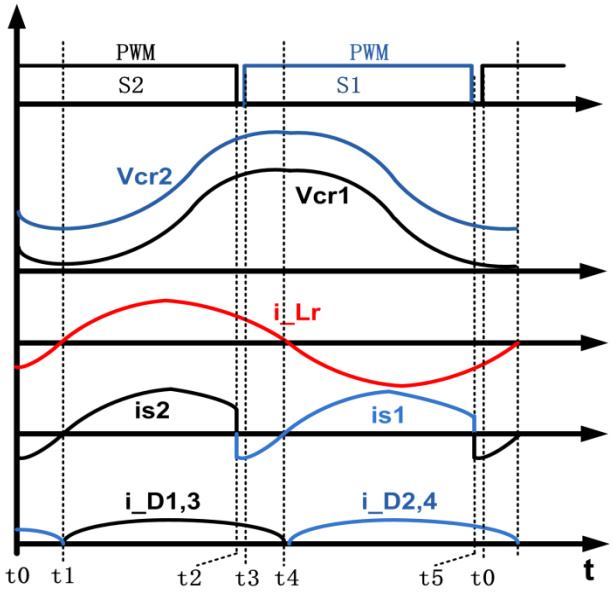
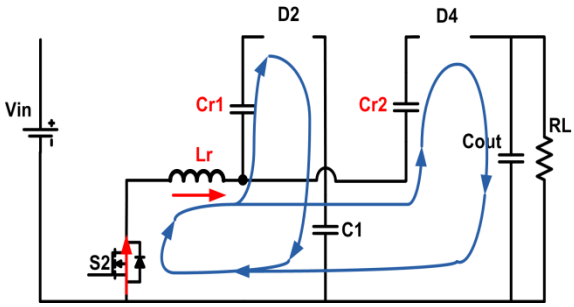
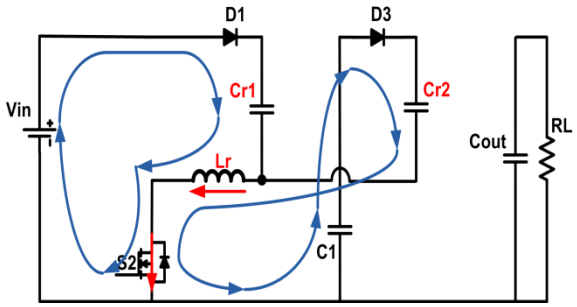


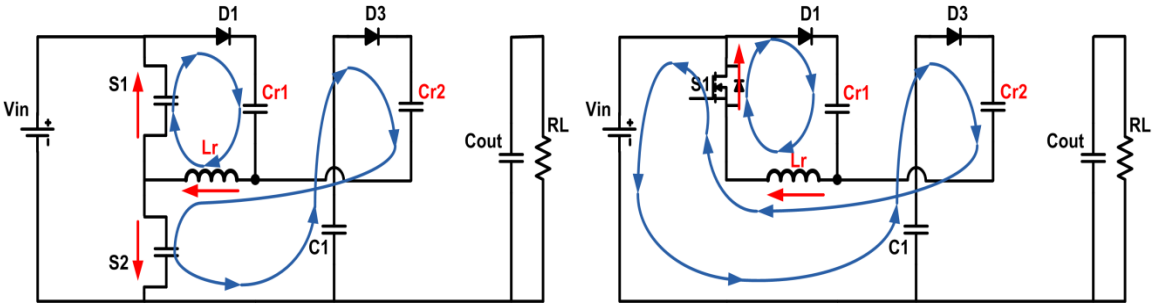
Fig. 5.2. Operating waveforms



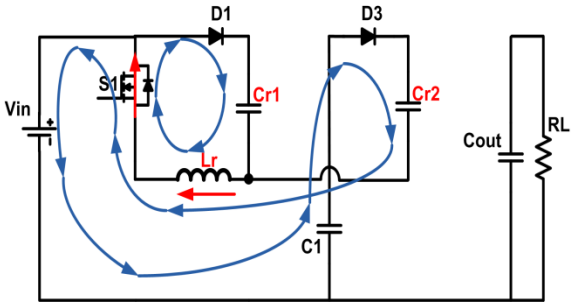
(a) $[t_0 \sim t_1]$



(b) $[t_1 \sim t_2]$



(c) $[t_2 \sim t_2']$ (d) $[t_2' \sim t_3]$



(e) $[t_3 \sim t_4]$

Fig. 5.3. Operating states above the resonance

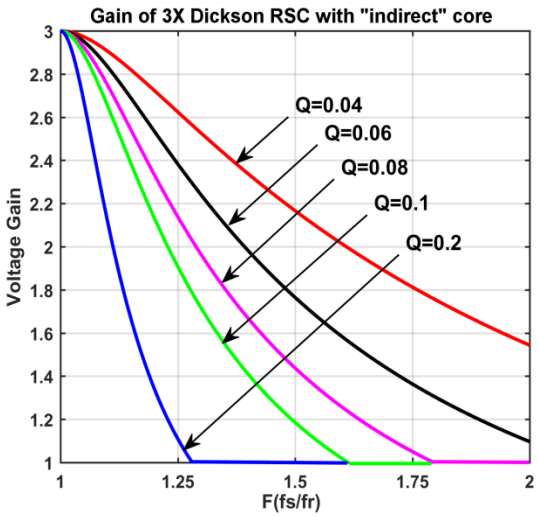


Fig. 5.4. Theoretical voltage gain curve

5.3 Dickson RSC with Cuk Dual Resonance Core

The operation principle of the Dickson RSC with Cuk DRC is discussed in chapter 4. The topology is shown in Fig. 5.5, and the derived voltage gain is given in Fig. 5.6. Seen from Fig. 5.6, no matter at high load (Q is large) or light load (Q is small), the voltage gain can be well

regulated from 1 to 3. Even at no load condition, the output voltage can be regulated by approaching the F to 1 in theory, which is an improvement compared to the Dickson RSC with "indirect" resonant core.

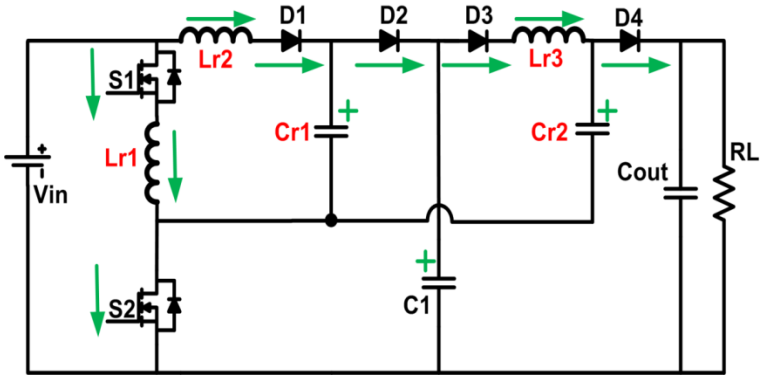


Fig. 5.5. Topology of Dickson RSC with Cuk DRC

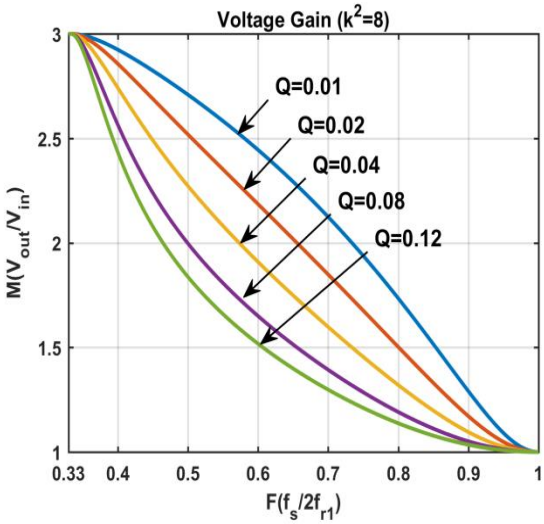


Fig. 5.6. Theoretical voltage gain curve

5.4 Phase-shift Regulated Dickson RSC with "Indirect" Resonant Core

The topology of the phase-shift regulated Dickson RSC with "indirect" resonant core is shown in Fig. 5.7. All diodes in Fig. 5.1 are replaced by MOSFETs, while the other components do not change. The defined positive directions of current and voltage are highlighted in green arrows and plus signs in Fig. 5.7.

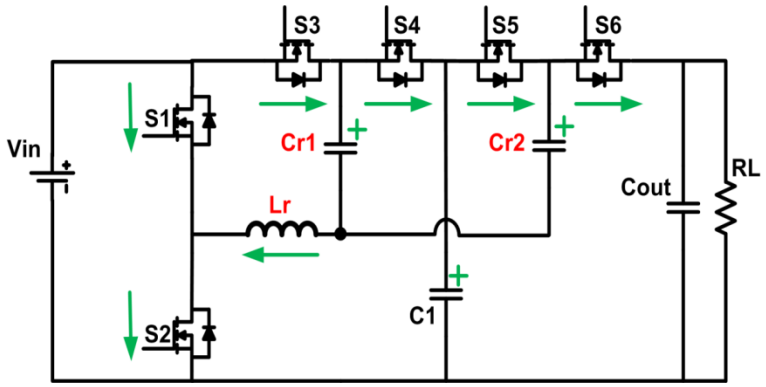


Fig. 5.7. Topology of phase-shift regulated Dickson RSC with “indirect” resonant core

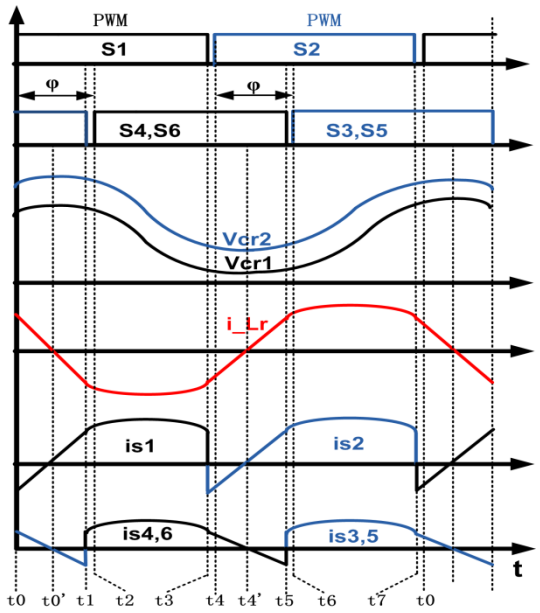
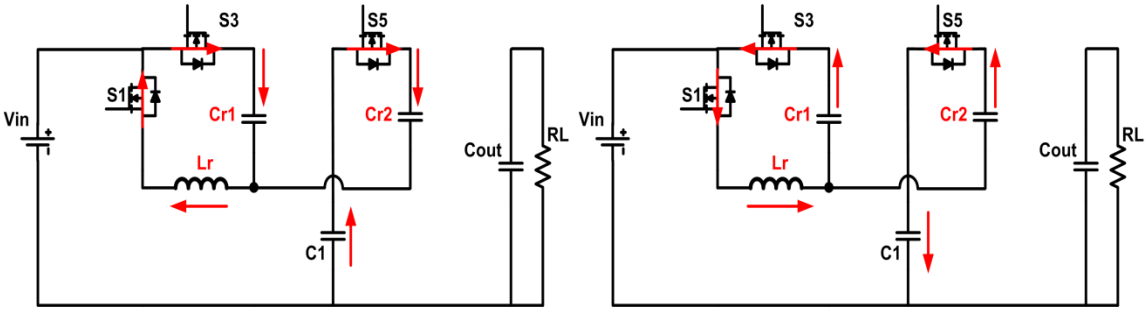
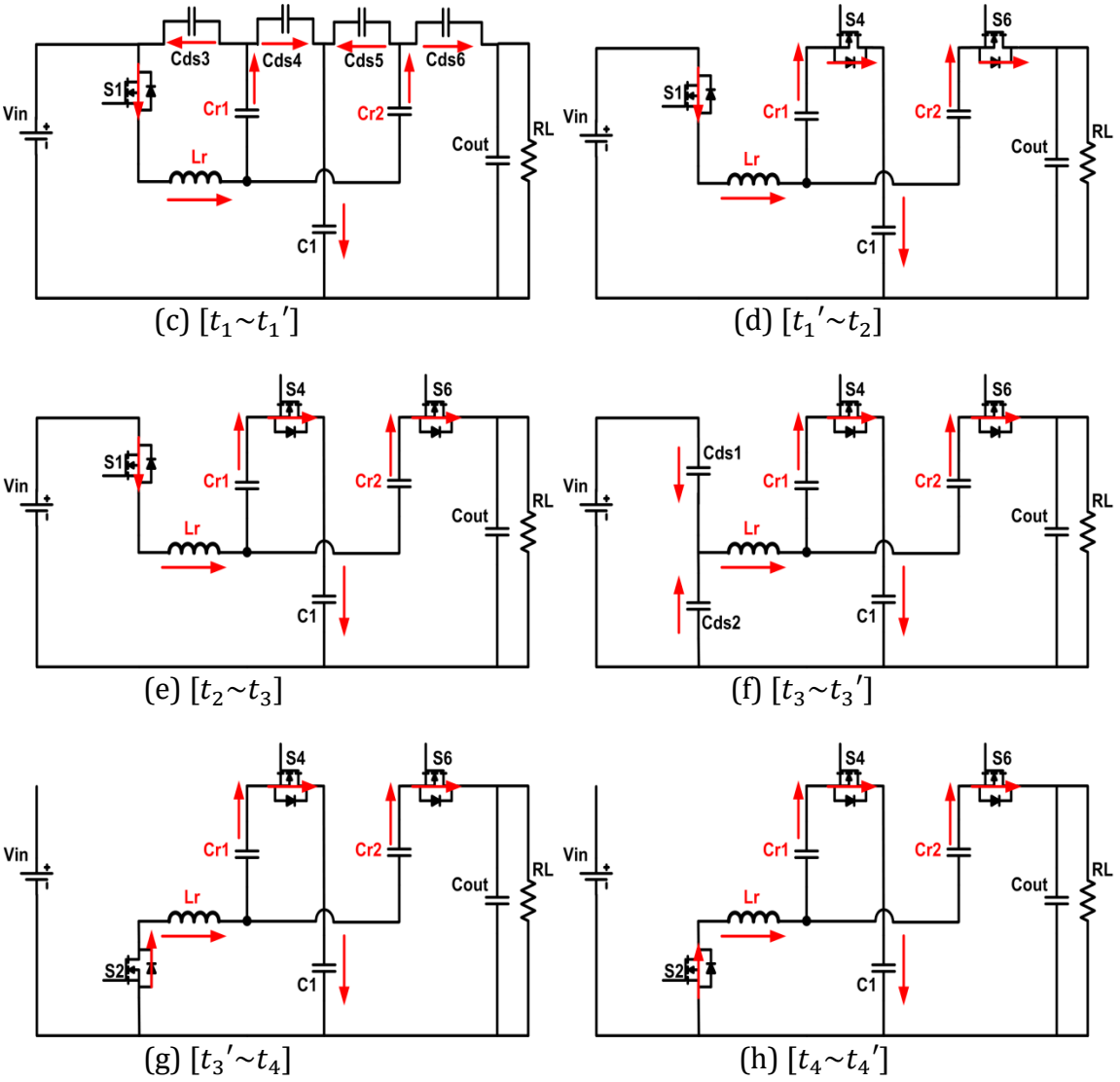


Fig. 5.8. Operating waveforms



(a) $[t_0 \sim t_0']$ (b) $[t_0' \sim t_1]$



(c) $[t_1 \sim t_1']$ (d) $[t_1' \sim t_2]$

(e) $[t_2 \sim t_3]$ (f) $[t_3 \sim t_3']$

(g) $[t_3' \sim t_4]$ (h) $[t_4 \sim t_4']$

Fig. 5.9. Operating states

Based on the operating waveforms in Fig. 5.8, the duty cycle of all MOSFETs are 0.5. S_1's driving signal is complementary with S_2's driving signal, while $S_{4,6}$'s driving signal is complementary with $S_{3,5}$'s driving signal. In addition, there is a phase-shift ratio Ø between the rising edge of S_1's driving signal and $S_{4,6}$' driving signal.

With phase-shift control, the operating principle is analyzed as follows.

$[t_0 \sim t_0']$: At t_0, the S_1 is turned on, while S_3 and S_5 are still on. The inductor current is positive, so L_r is resonating with $C_{r1} + C_{r2}$ (in parallel), as shown in Fig. 5.9(a).

[t_0'~t_1]: At t_0', the resonant inductor current resonates back to zero and starts flowing in the negative direction, while the resonant tank retains, as shown in Fig. 5.9(b)

[t_1~t_1']: At t_1, S_3 and S_5 are turned off, and then the loop current will charge the parasitic capacitance $C_{ds3,5}$ of $S_{3,5}$ and discharge $C_{ds4,6}$ of $S_{4,6}$ till t_1', as shown in Fig. 5.9(c). The parasitic capacitance is very small, so this interval is very short, which is neglected in steady-state analysis.

[t_1'~t_2]: After t_1', the voltage across $C_{ds4,6}$ are discharged to zero and then the anti-parallel diode of $S_{4,6}$ starts conducting current, shown in Fig. 5.9(d). L_r is still resonating with $C_{r1} + C_{r2}$ (in parallel).

[t_2~t_3]: At t_2, transistor $S_{4,6}$ are turned on with ZVS operation, reducing switching loss and thus improving the efficiency. The two charging loops retain, as shown in Fig. 5.9(e).

[t_3~t_3']: At t_2, the transistor S_1 is turned off. The loop current will charge the parasitic capacitance C_{ds1} of S_1 and discharge C_{ds26} of S_2 till t_3', as shown in Fig. 5.9(f). The parasitic capacitance is very small, so this interval is very short, which is neglected in steady-state analysis.

[t_3'~t_4]: After t_2', the voltage across C_{ds2} is discharged to zero and then the anti-parallel diode of S_2 starts conducting current, as shown in Fig. 5.9(g). At t_4, the first half switching cycle ends.

[t_4~t_4']: At t_4, transistor S_2 are turned on with ZVS operation. The inductor current is negative and the charging loops maintain the same, as shown in Fig. 5.9(h)

The detailed analysis was well discussed in [2][3]. As proved, the voltage gain can be regulated either below 3 or above 3 by phase-shift control. However, it can't be varied from

the target gain (3) too much, as the inductor current will increase abruptly, deteriorating the overall efficiency.

5.5 Conclusions

The comparison of the three Dickson RSCs in terms of devices, soft-switching operation, modulation method, voltage gain range and light-load regulation capability is summarized in Table 5.1 and 5.2 as follows.

Table 5.1. Component Comparison

3X Dickson RSC	MOSFET	Diode	Resonant Inductor	Resonant Capacitor	Capacitor Bank
"indirect"	2	4	1	2	1
Cuk DRC	2	4	2	2	1
Phase-shift	6	0	1	2	1

Table 5.2. Characteristics Comparison

3X Dickson RSC	MOSFET	Diode	Modulation	Gain Range	Light Load Regulation
"indirect"	ZVS	ZCS	Frequency modulation	High Q:1~3 Low Q: <3	Poor
Cuk DRC	ZCS	ZCS	On-time fixed frequency modulation	1~3	Good
Phase-shift	ZVS	N/A	Phase-shift modulation	around 3	Good

5.6 References

[1] K. K. Law, K. W. E. Cheng and Y. P. B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52, no. 5, pp. 943-948, May 2005.

[2] K. Sano and H. Fujita, "Performance of a High-Efficiency Switched-Capacitor-Based Resonant Converter With Phase-Shift Control," in IEEE Transactions on Power Electronics, vol. 26, no. 2, pp. 344-354, Feb. 2011.

[3] D. Cao, X. Lu, X. Yu and F. Z. Peng, "Zero voltage switching double-wing multilevel modular switched-capacitor DC-DC converter with voltage regulation," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2013, pp. 2029-2036.

PART II

CHAPTER 6: A Control Map for a Bidirectional PWM Plus Phase-Shift-Modulated Push-Pull DC-DC Converter

6.1 Introduction

Bidirectional dc-dc converters have been widely used in dc motor drives, hybrid electric vehicles, uninterruptible power supplies, distributed renewable energy systems and so forth [1]. Galvanic isolation is typically required for user-accessible and/or grid-connected applications. In the upcoming era of smart grids, energy storage systems of smart houses and HEVs will store surplus electrical energy rectified from the grid in the normal mode and inject power back to the grid during blackouts and peak cut time. Furthermore, industrial equipment such as elevators and automated guided vehicles (AGVs) has the potential to store regenerative energy generated during deceleration of the motors in rechargeable batteries and supply the stored energy for the motor during start-up operation [2]. As a result, an isolated bidirectional dc-dc converter (IBDC) is usually used to achieve the bidirectional power flow [3].

The full-bridge IBDC was proposed in [4] and different clamp circuits were proposed in [5] [6]. When power flows from the current-fed bridge to the voltage-fed bridge, the active clamp circuit helps absorb the current difference between the current-fed inductor and leakage inductance, and ZVS is achieved for the primary transistors. As for the reverse power flow, the converter works as a phase-shift ZVZCS full-bridge converter and the clamp circuit helps reset the transformer current on the voltage-fed bridge quickly. A control strategy for the bidirectional full-bridge converter was proposed in [7] to reduce or eliminate the clamp circuitry. By controlling the turn on/off signal of transistors on the voltage-fed bridge, the current in leakage inductance is preset to the current-fed inductor current before commutation event occurs. This concept has been extended to some other bidirectional topologies [8]-[12].

The dual active bridge (DAB) IBDC was proposed in [13][14], which is composed of two voltage-fed full bridges and a high-frequency transformer. Duty cycle of all switches is fixed at 0.5 and the phase-shift between the two bridges is controlled to regulate the power flow. Snubber or clamp circuit is not required. In order to expand the ZVS region and to decrease the circulating current, extended phase-shift control, dual phase-shift control and triple-phase-shift control were proposed and analyzed in [15]-[19]. However, the current flowing in the dc buses contains high ripples; therefore appropriate filtering circuits are necessary. Furthermore, proper control is required to prevent dc saturation of the transformer on both sides [20]. In addition, a large leakage inductance or even an auxiliary inductor is needed to limit the peak current, decreasing the voltage gain of the DAB. As a result, DAB is more suitable for low-voltage-gain, narrow-input-voltage-variation and high-power applications.

A dual half bridge with phase-shift control was proposed in [21]. It has small input current ripple and large voltage gain. But in many IBDC applications, both dc buses have voltage variations imposed by the system [20]. When the voltage amplitudes of the primary side and secondary side are not matched, the current stress and circulating current become much higher, deteriorating the efficiency badly. Aside from the phase-shift angle, another control variable – duty cycle of the primary and secondary switches – is introduced to optimize efficiency of DHB in [22]. In [23], two back-to-back current-fed half-bridges are combined into a new IBDC, with relatively small input and output current ripples.

For a specific group of IBDCs, the PWM plus phase-shift (PPS) control strategy can be adopted [24][25]. In those two-level PPS converters, the duty cycle is controlled to match the voltage amplitudes of the two-level square waves on both sides, while phase-shift angle

is regulated to control the power flow. Low current stress, wide ZVS range and wide input-voltage-variation range can be achieved [24].

In [26], the PPS control strategy was extended to a traditional dual-inductor half bridge converter proposed in [27]. With this control, the voltage on the transformer's primary side becomes a three-level square wave with an extra zero level, defined as a three-level PPS converter. Similarly, another three-level PPS converter was reported in [28] by applying PPS control strategy to the isolated winding-coupled bidirectional converter proposed in [29]. However, neither [26] or [28] provided complete analysis about different operation modes to find the optimized region. In addition, the relationship between duty cycle and phase-shift ratio in different operation modes was not revealed, bringing difficulties to operate the PPS converters.

In [30], the traditional current-fed push-pull with active clamp was proposed. This converter applies PWM control and it has small input current ripple with the help of the input inductor. But the secondary-side diodes are hard switched, causing high reverse recovery current. In [31], a unidirectional resonant push-pull converter was proposed, whose structure originated from [30]. The ZCS operation of the secondary diodes can be obtained. However, due to the resonance, the component stresses are much higher. And the resonant tank should be carefully designed to ensure the normal operation. In [32], a bidirectional resonant push-pull converter is modified based on [31], to regulate bidirectional power flow.

So far PPS control has only been applied to a specific group of converters [24][25][26][28]. In this chapter**,** the PPS control strategy is extended to a bidirectional push-pull converter whose structure originated from [30]. With the PPS control, the

transistor channel rather than the parasitic diode conducts the current in steady-state periods, avoiding the diode reverse recovery phenomenon. Meantime, the input-voltage-variation range and the soft-switching operation region of the primary transistors are expanded. A comprehensive analysis of 12 different operation modes is presented. Based on this understanding, a control map and a circuit parameter k are proposed to assist converter design and operation that can avoid high-circulating-current regions, low-power-transmission -capability regions, and hard-switched regions. The proposed control map can provide a guideline about how to choose the duty cycle and the corresponding phase-shift value to achieve PPS control. The limit of the circuit parameter k is found, beyond which the PPS converter no longer operates normally. The above analyzing method is suitable for all PPS converters. A 30~48V/380V prototype rated at 100~1000W was built to verify the analysis. The contents in this chapter have been published in paper [33].

6.2 Operation Modes

The PPS push-pull converter is shown in Fig. 6.1. On the low-voltage side, S_1 and S_2 are the main switches, while switches S_3 and S_4 are two active clamp switches, being connected to a clamp capacitor C_s. The clamp circuit is highlighted by the blue dashed line. The input inductor L is fed into the transformer center tap. On the high-voltage side, an active voltage doubler with transistors $S_{5,6}$ is used, where L_s is the leakage inductance referred to the secondary side. The turns-ratio of the transformer is 1:1:n. The defined current symbols and positive directions are denoted in red arrows.

The duty cycle of S_1 and S_2 is denoted as D, with a 180° phase-shift between each other. The driving signals of S_1 and S_3, S_2 and S_4 are complimentary. The duty cycle of S_5 and S_6 is fixed at 0.5 and φ is defined as the phase-shift ratio between the rising edge of S_1 and S_5's

driving signal, which is equal to phase-shift angle over 2π. D is from 0 to 1, while φ can be varied from -0.5 ($-180°$) to 0.5 (180°). When power flows from the low-voltage side to the high-voltage side, it's defined as boost mode (P>0); for the reverse power direction, it's defined as buck mode (P<0). According to the different profiles of leakage current, there are 12 different operating modes as listed in Table 6.1.

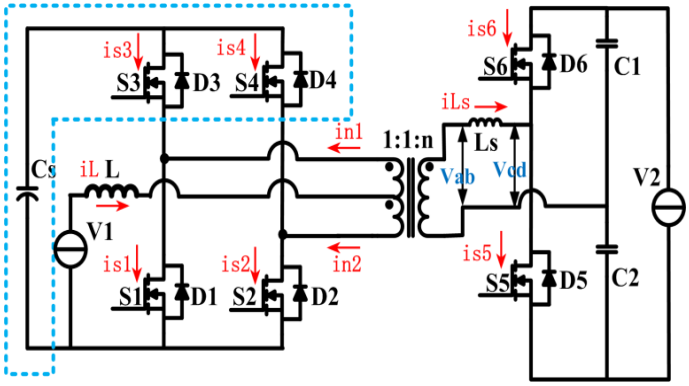


Fig. 6.1 Topology of the bidirectional PPS push-pull converter

Table 6.1 Operation modes of PPS push-pull converter

D	Power	Relationship between D & φ	Mode
$[0, \frac{1}{2}]$	P<0	$-0.5 < \varphi < (D-0.5) < 0$	a'(-)
	P<0	$D-0.5 < \varphi < 0.5(D-0.5) < 0$	b'(-)
	P>0	$0.5(D-0.5) < \varphi < 0$	b'(+)
	P>0	$0 < \varphi < D$	a(+)
	P>0	$D < \varphi < D + 0.5(0.5-D)$	b(+)
	P<0	$D + 0.5(0.5-D) < \varphi < 0.5$	b(-)
$[\frac{1}{2}, 1]$	P>0	$-0.5 < \varphi < -[(1-D) + 0.5(D-0.5)] < 0$	c'(+)
	P<0	$-[(1-D) + 0.5(D-0.5)] < \varphi < -(1-D) < 0$	c'(-)
	P<0	$-(1-D) < \varphi < 0$	d'(-)
	P<0	$0 < \varphi < 0.5(D-0.5)$	c(-)
	P>0	$0.5(D-0.5) < \varphi < D-0.5$	c(+)
	P>0	$D-0.5 < \varphi < 0.5$	d(+)
Note: '+', '-' means direction of the power flow; Punctuation 'prime' means the phase shift is negative.			

6.3 Operation Principle

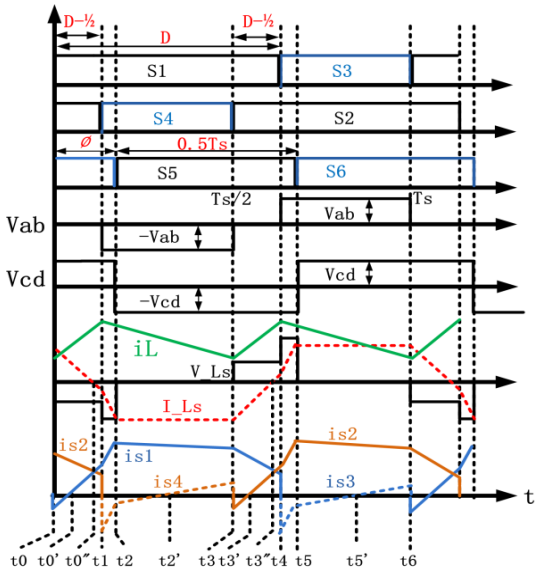
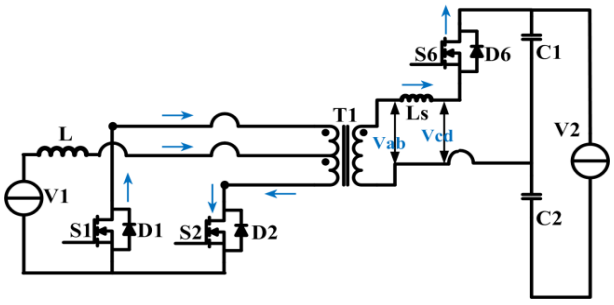
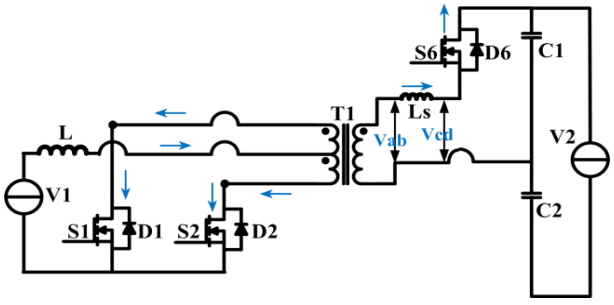


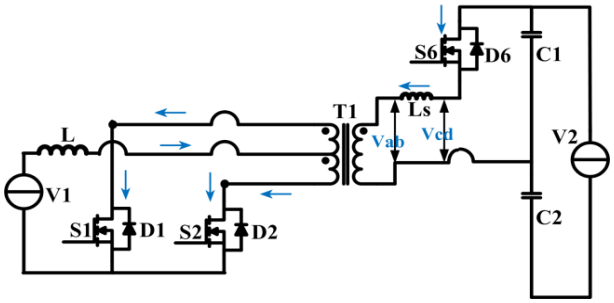
Fig. 6.2. Operation waveforms in mode d(+) for PPS push-pull converter



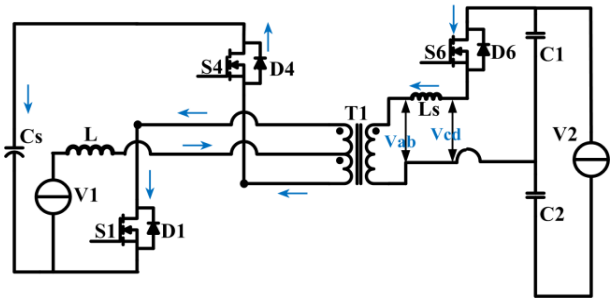
(a) Stage 1 $[t_0 - t_0']$



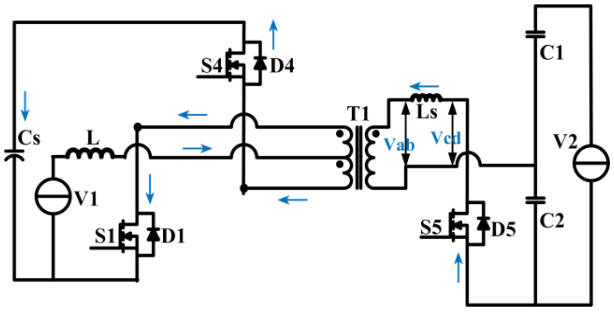
(b) Stage 2 $[t_0' - t_0'']$



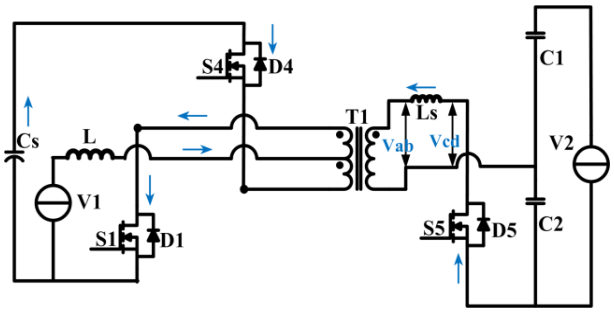
(c) Stage 3 $[t_0'' - t_1]$



(d) Stage 4 $[t_1 - t_2]$



(e) Stage 5 $[t_2 - t_2']$



(f) Stage 6 $[t_2' - t_3]$

Fig. 6.3. Switching states for PPS push-pull converter

In this section, the operation principle in mode d(+) -boost mode- is analyzed as an example. The operation waveforms are given in Fig. 6.2 and the switching stages are shown

in Fig. 6.3. Several assumptions are made for simplicity. The parasitic elements of the transistors and diodes are ignored. The leakage inductance referred to the primary side is much smaller than the magnetizing inductance and the input inductor. The voltages on C_s and $C_{1,2}$ are considered to maintain constant in one switching cycle. Dead-time between the complimentary driving signals is neglected.

To begin with, the voltage across the clamp capacitor can be derived according to the v-s balance on the input inductor.

$$V_{Cs} = \frac{1}{1-D} V_1 \tag{1}$$

In the steady state, the amplitudes of the primary and secondary square wave are:

$$V_{ab} = nV_{Cs}/2 = \frac{n}{2(1-D)} V_1 \text{ and } V_{cd} = \frac{V_2}{2} \tag{2}$$

With PWM control, the amplitudes of the two square waves are regulated to be equal. Thus, the voltage conversion ratio is:

$$\frac{V_2}{V_1} = \frac{n}{1-D} \tag{3}$$

According to the property of transformer, two equations are held in all states:

$$i_{n1} + i_{n2} = i_L, \tag{4}$$

$$i_{n1} * N_1 - i_{n2} * N_2 + i_{Ls} * N_3 = 0, \text{ where } N_1 : N_2 : N_3 = 1 : 1 : n \tag{5}$$

As a result, i_{n1} and i_{n2} can be derived:

$$i_{n1} = \frac{i_L - n i_{Ls}}{2} \tag{6}$$

$$i_{n2} = \frac{i_L + n i_{Ls}}{2} \tag{7}$$

Stage 1 $[t_0 - t_0']$: Before t_0, $S_{2,3,6}$ are conducting. $i_{S2,3}$ and i_{Ls} are positive. At t_0, S_3 is turned off and meantime S_1 is turned on. According to (6), i_{n1} cannot change abruptly, so it

will flow through S_1 reversely, achieving ZVS for transistor S_1. In this stage, the voltage across the input inductor L is V_1 and the voltage across reflected leakage inductance L_s is $-\frac{1}{2}V_2$. The following expressions can be obtained:

$$\frac{di_L}{dt} = \frac{V_1}{L} > 0 \tag{8}$$

$$\frac{di_{Ls}}{dt} = -\frac{V_2}{2L_s} < 0 \tag{9}$$

$$\frac{di_{n1}}{dt} = \frac{di_{S1}}{dt} = \frac{1}{2}\left(\frac{di_L}{dt} - \frac{ndi_{Ls}}{dt}\right) = \frac{V_1}{2L} + \frac{nV_2}{4L_s} > 0 \tag{10}$$

$$\frac{di_{n2}}{dt} = \frac{di_{S2}}{dt} = \frac{1}{2}\left(\frac{di_L}{dt} + \frac{ndi_{Ls}}{dt}\right) = \frac{V_1}{2}\left[\frac{1}{L} - \frac{1}{2(1-D)} * \frac{1}{L_s/n^2}\right] < 0$$

$$\text{with } L_s/n^2 \ll \text{L}, 0.5 < \text{D} < 1 \tag{11}$$

At t_0', i_{S1} is increasing linearly to zero, so this interval is:

$$t_0' - t_0 = \frac{-I_{S1}(0)}{\frac{V_1}{2L} + \frac{nV_2}{4L_s}} \tag{12}$$

Stage 2 $[t_0' - t_0'']$: After t_0', i_{S1} will become positive and continue increasing with the same slope as (10). At t_0'', i_{S1} is equal to i_{S2} and thus the leakage inductance current i_{Ls} decreases to zero according to (5), so this interval is:

$$t_0'' - t_0 = \frac{I_{Ls}(0)}{\frac{V_2}{2L_s}} \tag{13}$$

Stage 3 $[t_0'' - t_1]$: After t_0'', i_{Ls} will become negative and continue decreasing with the same slope as (9). The total time from t_0 to t_1 is:

$$t_1 - t_0 = (D - \frac{1}{2})T_s \tag{14}$$

Stage 4 $[t_1 - t_2]$: At t_1, S_2 is turned off and meantime S_4 is turned on. According to (7), i_{n2} cannot change abruptly, so it will flow through S_4 reversely, achieving ZVS for transistor S_4. In this stage, the voltage across the input inductor L is $V_1 - \frac{1}{2}V_{Cs}$ and the voltage across

reflected leakage inductance L_s is $-\frac{1}{2}nV_{Cs}-\frac{1}{2}V_2$. With (1) and (3), the following relationships can be obtained:

$$\frac{di_L}{dt}=\frac{1}{L}(V_1-\frac{1}{2}V_{Cs})=\frac{1-2D}{2(1-D)}\frac{V_1}{L}<0 \tag{15}$$

$$\frac{di_{Ls}}{dt}=\frac{1}{L_s}\left(-\frac{1}{2}nV_{Cs}-\frac{1}{2}V_2\right)=-\frac{n}{1-D}\frac{V_1}{L_s}<0 \tag{16}$$

$$\frac{di_{n1}}{dt}=\frac{di_{S1}}{dt}=\frac{V_1}{2(1-D)}\left(\frac{1}{L_s/n^2}-\frac{D-0.5}{L}\right)>0 \tag{17}$$

$$\frac{di_{n2}}{dt}=-\frac{di_{S4}}{dt}==\frac{V_1}{2(1-D)}\left[\left(\frac{1}{2}-D\right)\frac{1}{L}-\frac{1}{L_s/n^2}\right]<0$$

$$\text{with } L_s/n^2 \ll \text{L}, 0.5<\text{D}<1 \tag{18}$$

The total time from t_1 to t_2 is:

$$t_2-t_1=[\varphi-(D-\frac{1}{2})]T_s \tag{19}$$

Stage 5 $[t_2-t_2']$: At t_2, S_6 is turned off and meantime S_5 is turned on with ZVS operation because the leakage current cannot change direction abruptly at this moment. The voltage across reflected leakage inductance L_s becomes $-\frac{1}{2}nV_{Cs}+\frac{1}{2}V_2=0$ with PPS control scheme, which means i_{Ls} will not change during this interval. The following relationships can be obtained:

$$\frac{di_{n1}}{dt}=\frac{di_{S1}}{dt}=\frac{1}{2}\left(\frac{di_L}{dt}-\frac{ndi_{Ls}}{dt}\right)=\frac{1-2D}{2(1-D)}\frac{V_1}{L}<0 \tag{20}$$

$$\frac{di_{n2}}{dt}=-\frac{di_{S4}}{dt}=\frac{1}{2}\left(\frac{di_L}{dt}+\frac{ndi_{Ls}}{dt}\right)=\frac{1-2D}{2(1-D)}\frac{V_1}{L}<0 \tag{21}$$

As a result, the current slopes of i_{s1} and i_{s4} are opposite in this stage. Meantime, the leakage current is a constant and thus its peak value is limited.

Stage 6 $[t_2'-t_3]$: At t_2', i_{S4} becomes positive and continues increasing until t_3. At t_3, the half switching cycle is over. The total from t_2 to t_3 is:

$$t_3 - t_2 = (\frac{1}{2} - \varphi)T_s \quad (22)$$

From $t_3 \sim t_6$, the operation stages are similar to those in the first half cycle

6.4 Power Transmission Capability

In this section, the power transmission capability of the bidirectional PPS push-pull converter is analyzed, with the similar method in [34]. Mode d(+) in Fig. 6.2 is analyzed in details as an example to derive the power transmission capability. The amplitudes of the primary and secondary square waves are given in (2).

During $[t_0, t_1]$, the leakage current is decreasing linearly from $i_{Ls}(0)$ to $i_{Ls}(D - \frac{1}{2})$. The voltage on the reflected inductance L_s is:

$$-V_{cd} = -\frac{V_2}{2} \quad (23)$$

During $[t_1, t_2]$, the leakage current is decreasing from $i_{Ls}(D - \frac{1}{2})$ to $i_{Ls}(\varphi)$. The voltage on L_s is:

$$-V_{ab} - V_{cd} = -\frac{nV_1}{1-D} = -V_2 \quad (24)$$

During $[t_2, t_3]$, the voltage on L_s is zero, so the current value will remain at $i_{Ls}(\varphi)$ in this interval. Due to the completely symmetrical structure [34]:

$$i_{Ls}(0) = -i_{Ls}(\frac{T_s}{2}) \quad (25)$$

Based on (23) (24) (25):

$$i_{Ls}(0) = \frac{V_2}{4L_s f_s}(-D + 2\varphi + \frac{1}{2}) \quad (26)$$

$$i_{Ls}\left(D - \frac{1}{2}\right) = -\frac{V_2}{4L_s f_s}(-3D + 2\varphi + \frac{3}{2}) \quad (27)$$

Thus the input power in a half switching cycle is:

$$P * \frac{T_s}{2} = \frac{i_{Ls}(0)+i_{Ls}\left(D-\frac{1}{2}\right)}{2} * \left(D-\frac{1}{2}\right) T_s * -V_{cd}$$

$$+\frac{i_{Ls}\left(\mathrm{D}-\frac{1}{2}\right)+i_{Ls}(\varphi)}{2} * \left(\varphi - D + \frac{1}{2}\right) T_s * (-V_{ab} - V_{cd}) \quad (28)$$

As a result, the power transmission capability in mode d(+) is:

$$P = \frac{nV_1V_2}{4L_sf_s} * \frac{1}{1-D}\left(-2\varphi^2 + 2D\varphi - D^2 + \frac{1}{2}D\right)$$

$$\text{Where } D - 0.5 < \varphi < 0.5 \quad (29)$$

With the similar method, the power transmission capability of all operation modes is derived.

When 0<D<0.5, the power transmission capability is:

$$P\begin{cases} \frac{nV_1V_2}{4L_sf_s} * \frac{1}{1-D}\left(2\varphi^2 - 2D\varphi + 2\varphi + D^2 - \frac{3}{2}D + \frac{1}{2}\right) & a'(-) \\ \frac{nV_1V_2}{4L_sf_s} * \frac{D}{1-D}\left(2\varphi - D + \frac{1}{2}\right) & b'(-)\,, b'(+) \\ \frac{nV_1V_2}{4L_sf_s} * \frac{1}{1-D}\left(-2\varphi^2 + 2D\varphi - D^2 + \frac{1}{2}D\right) & a(+) \\ \frac{nV_1V_2}{4L_sf_s} * \frac{D}{1-D}\left(-2\varphi + D + \frac{1}{2}\right) & b(+), b(-) \end{cases} \quad (30)$$

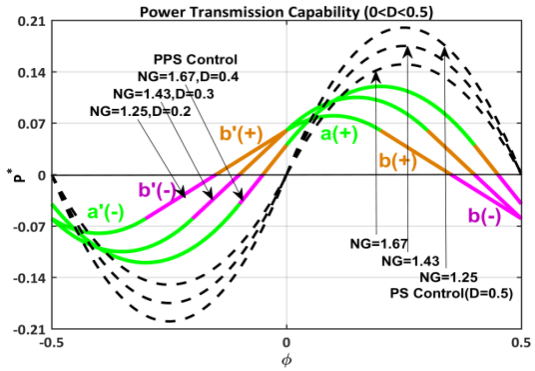
When 0.5<D<1, the power transmission capability is:

$$P\begin{cases} \frac{nV_1V_2}{4L_sf_s}\left(-2\varphi + D - \frac{3}{2}\right) & c'(+), c'(-) \\ \frac{nV_1V_2}{4L_sf_s} * \frac{1}{1-D}\left(2\varphi^2 - 2D\varphi + 2\varphi + D^2 - \frac{3}{2}D + \frac{1}{2}\right) & d'(-) \\ \frac{nV_1V_2}{4L_sf_s}\left(2\varphi - D + \frac{1}{2}\right) & c(-), c(+) \\ \frac{nV_1V_2}{4L_sf_s} * \frac{1}{1-D}\left(-2\varphi^2 + 2D\varphi - D^2 + \frac{1}{2}D\right) & d(+) \end{cases} \quad (31)$$

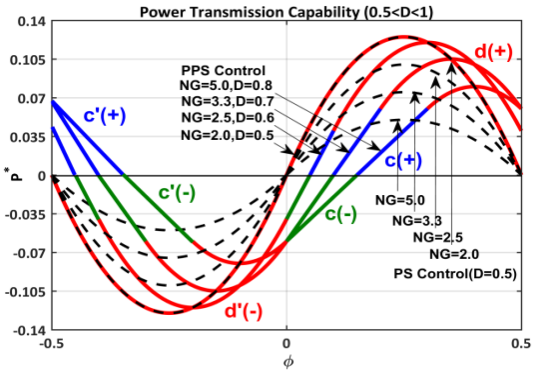
According to (30) (31), the normalized power transmission capability P^*(normalized to $\frac{V_2^2}{4L_sf_s}$) with PPS and PS control is plotted in Fig. 6.4 (a) (b). The curves in solid lines stand for P^* under PPS control. Different colors represent different operation modes and each

curve has different normalized gain (NG) which is normalized to the turns ratio n. The curves in dash lines stand for P^* under PS control with fixed D=0.5.

As shown, when 0<D<0.5, the maximum P^* of PS control is higher than that of the PPS control. When 0.5<D<1, the maximum P^* of PS control is lower than that of the PPS control. As a result, in order to fully utilize the capability of the converter, the main operation region should be 0.5<D<1, defined as the high power-transmission-capability region.



(a)0<D<0.5



(b)0.5<D<1

Fig. 6.4. Normalized power transmission capability curve for PPS push-pull converter

6.5 Soft Switching Operation Analysis

In this section, the soft-switching operation of the PPS push-pull converter in mode d(+) is analyzed, and then it is extended to all 12 operation modes. Based on the operation

principle analysis in section 6.3, equation sets (32) should be satisfied to ensure ZVS turn-on for transistors:

$$\begin{cases} S_{1,2}: i_{S1}(t_0^+) = \quad i_{n1}(t_0^+) = -i_{S3}(t_0^-) < 0 \\ S_{3,4}: i_{S3}(t_4^+) = -i_{n1}(t_4^+) = -i_{S1}(t_4^-) < 0 \\ \qquad\qquad S_{5,6}: i_{ls}(t_2) < 0 \end{cases} \tag{32}$$

First, the transmitted power in mode d(+) has been derived in (31). With the similar method in [34], the initial value of leakage current is:

$$i_{Ls}(t_0) = \frac{V_2}{4L_s f_s}\left(-D + 2\varphi + \frac{1}{2}\right) > 0, D - \frac{1}{2} < \varphi < \frac{1}{2} \tag{33}$$

$$\text{So, } i_{Ls}(\varphi) = i_{Ls}(t_2) = -i_{Ls}(t_0) < 0 \tag{34}$$

As a result, ZVS turn-on is guaranteed for $S_{5,6}$ in mode d(+) according to (32).

Secondly, the current value of transistor S_1 at t_3^+ is:

$$i_{S1}(t_3^+) = \frac{P_o}{2V_1} - \frac{V_1}{4f_s L}\left(D - \frac{1}{2}\right) + \frac{nV_2}{8f_s L_s}(-D + 2\varphi + \frac{1}{2}) \tag{35}$$

According to (3) (11) (31) (35),

$$i_{S1}(t_4^-) = \frac{V_2/n}{4Lf_s}(1 - D)\left(D - \frac{1}{2}\right) + \frac{nV_2}{8L_s f_s} *$$

$$\left[\frac{1}{1-D}\left(-2\varphi^2 + 2D\varphi - D^2 + \frac{1}{2}D\right) + \left(-3D + 2\varphi + \frac{3}{2}\right)\right] > 0$$

$$\text{where } 0 < D - \frac{1}{2} < \varphi < \frac{1}{2} \tag{36}$$

As a result, ZVS turn-on is guaranteed for $S_{3,4}$ in mode d(+) according to (32).

Thirdly, the initial current value of S_3 is:

$$i_{S3}(t_4^+) = -i_{S1}(t_4^-) < 0 \tag{37}$$

After t_4, it will increase steadily with the slope in (18). Due to the i-s balance of the clamp capacitor in each half switching cycle, the final current value of S_3 must be positive, i.e.:

$$i_{S3}(t_6^-) = i_{S3}(t_0^-) > 0 \tag{38}$$

As a result, ZVS turn-on is guaranteed for $S_{1,2}$ in mode d(+) according to (32).

With the same method, soft-switching operations are summarized in Table 6.2.

Table 6.2. Soft-switching condition of PPS push-pull converter

Boost Mode(P>0)		$S_{1,2}$	$S_{3,4}$	$S_{5,6}$
0<D<0.5	a(+) b'(+)	Hard-switched	ZVS	ZVS
	b(+)	ZVS	ZVS	ZVS
0.5<D<1	c(+),c'(+),d(+)	ZVS	ZVS	ZVS
Buck Mode(P<0)		$S_{1,2}$	$S_{3,4}$	$S_{5,6}$
0<D<0.5	a'(-), b'(-)	ZVS	Hard-switched	ZVS
	b(-)	ZVS	ZVS	ZVS
0.5<D<1	c(-),c'(-),d'(-)	ZVS	ZVS	ZVS

6.6 The Proposed Control Map

6.6.1 The Relationship Between D And φ

In this part, mode d(+) is analyzed as an example to derive the relationship between D and φ. Then the similar analysis is extended to 12 operation modes.

In both boost and buck mode, the equivalent load resistance R_L (P/V_2^2) on the secondary side could be utilized for calculating. From the last section, the power transmission capability in mode d(+) has been derived in (31). In mode d(+), P>0 and the power flows from V_1 to V_2. Assuming the efficiency is 100%:

$$P = \frac{nV_1V_2}{4L_sf_s} * \frac{1}{1-D}\left(-2\varphi^2 + 2D\varphi - D^2 + \frac{1}{2}D\right) = \frac{V_2^2}{R_L} \quad (39)$$

The output voltage is figured out:

$$V_2 = \frac{nV_1}{4L_sf_s} * R_L * \frac{1}{1-D}\left(-2\varphi^2 + 2D\varphi - D^2 + \frac{1}{2}D\right) \quad (40)$$

With PPS control, the amplitudes of the two square waves are regulated to be equal and the voltage gain has been derived in (3). Therefore, the relationship between D and φ is:

$$-2\varphi^2 + 2D\varphi + \frac{1}{2}D - D^2 - 2k = 0, \text{where } k = \frac{2f_sL_s}{R_L} \quad (41)$$

Similarly, the relationships between D and φ in all operation modes are derived.

For 0<D<0.5, the equation sets are:

$$\begin{cases} -2\varphi^2 + 2\varphi D - 2\varphi + \frac{3}{2}D - D^2 - \frac{1}{2} - 2k = 0 & Mode\ a'(-) \\ \varphi = \frac{D^2 - \frac{1}{2}D - 2k}{2D} & Mode\ b'(-) \\ \varphi = \frac{D^2 - \frac{1}{2}D + 2k}{2D} & Mode\ b'(+) \\ -2\varphi^2 + 2D\varphi + \frac{1}{2}D - D^2 - 2k = 0 & Mode\ a(+) \\ \varphi = \frac{D^2 + \frac{1}{2}D - 2k}{2D} & Mode\ b(+) \\ \varphi = \frac{D^2 + \frac{1}{2}D + 2k}{2D} & Mode\ b(-) \end{cases} \quad (42)$$

For 0.5<D<1, the equation sets are:

$$\begin{cases} \varphi = \frac{-D^2 + \frac{5}{2}D - \frac{3}{2} - 2k}{2(1-D)} & Mode\ c'(+) \\ \varphi = \frac{-D^2 + \frac{5}{2}D - \frac{3}{2} + 2k}{2(1-D)} & Mode\ c'(-) \\ -2\varphi^2 + 2\varphi D - 2\varphi + \frac{3}{2}D - D^2 - \frac{1}{2} - 2k = 0 & Mode\ d'(-) \\ \varphi = \frac{-D^2 + \frac{3}{2}D - \frac{1}{2} - 2k}{2(1-D)} & Mode\ c(-) \\ \varphi = \frac{-D^2 + \frac{3}{2}D - \frac{1}{2} + 2k}{2(1-D)} & Mode\ c(+) \\ -2\varphi^2 + 2D\varphi + \frac{1}{2}D - D^2 - 2k = 0 & Mode\ d(+) \end{cases} \quad (43)$$

6.6.2 The Control Map

In this part, according to (42) (43) and the boundary conditions in Table 6.1, a control map is proposed in Fig. 6.5 (a) (b). In different operation modes, the control curve is in different colors. The x and y axes represent the duty cycle and phase-shift ratio, respectively. The blue x axis on the top represents the normalized gain to the transformer turns ratio n.

One ellipse corresponds to a same circuit parameter k ($\frac{2f_sL_s}{R_L}$) and the limit of k will be discussed in part 6.6.3. In order to achieve PPS control strategy, D and the corresponding φ should be pinpointed on each ellipse. For example, a PPS push pull converter with fixed switching frequency f_s and fixed leakage inductance L_s is designed to be operating with voltage-gain of 10. If the turns-ratio is 1:1:4, the normalized gain (NG) is 2.5. From Fig. 6.4(a), the NG=2.5 corresponds to D=0.6. With different load conditions (R_L), the corresponding φ can be pinpointed from the control map to ensure PPS control strategy.

From the control map, several converter operation notes can be obtained:

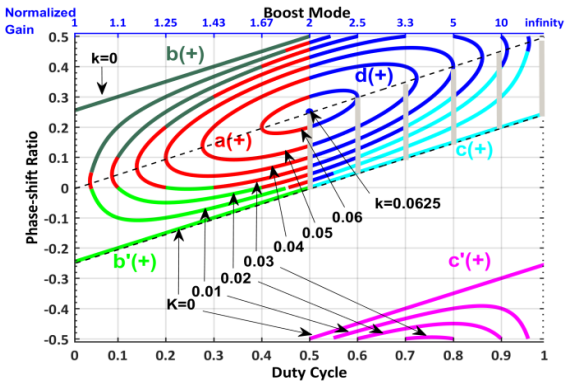
1) If the NG is fixed, the duty cycle is fixed as well. Then if the load is changed, only φ need to be regulated, jumping from one ellipse to another one with a different k;
2) If the load is fixed and only the NG is changed, both D and φ need to be changed following the same ellipse;
3) When the NG and the load are fixed, the corresponding D and k are determined. However, φ has two possible values to be selected. In this scenario, proper φ should be selected to avoid the high-circulating-current region. As known, the higher phase-shift leads to higher circulating current [9]. Therefore, the smaller φ should be adopted. The low-circulating-current region has been denoted between two dash lines in Fig. 6.5.
4) From the analysis in section 6.5, within the low-circulating current region, all transistors can be operated with ZVS when 0.5<D<1, while transistors $S_{1,2}$ or $S_{3,4}$ will be hard switched when 0<D<0.5.

5) From the analysis in section 6.4, in order to fully utilize the capability of the converter, the main operation region should be in the high power-transmission-capability region $0.5<D<1$.

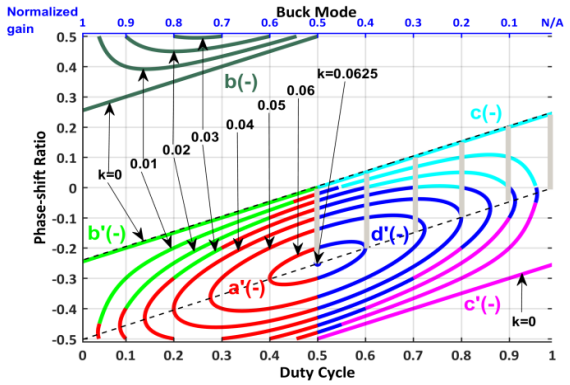
6) From the efficiency and converter utilization point of view, the nominal operation region should be designed to be 0.5<D<1 within the low-circulating current region, as highlighted with grey lines in Fig. 6.5.

7) As the value of k is increasing, the control curve will "shrink". As a result, the input-voltage-variation range becomes narrower. To sum up, with lighter load (smaller k), the voltage-gain range is wider; with heavier load (larger k), the voltage-gain range is narrower. While designing the converter, the tradeoff between voltage-gain range and power level should be considered.

8) In the closed-loop design, the control map can provide the duty cycle and phase-shift limit to ensure the converter operate in the soft-switching and low-circulating-current regions. For boost mode($k\neq0$), the limit of φ is $[\frac{1-\sqrt{(1-16k)}}{4}, \frac{1+\sqrt{1-16k}}{4}]$ and the limit of D is $[0.5, \frac{1+\sqrt{1-16k}}{2}]$. For buck mode($k\neq0$), the limit of φ is $[\frac{-1+\sqrt{1-16k}}{4}, \frac{-1+\sqrt{2(1-16k)}}{4}]$ and the limit of D is still $[0.5, \frac{1+\sqrt{1-16k}}{2}]$.



(a)Boost mode



(b)Buck mode

Fig. 6.5. The proposed control map for PPS push-pull converter

6.6.3 The Circuit Parameter k

In this part, the limit of *k* is derived to assist converter design.

The minimum *k* is 0, which means the load resistance is infinity and load current is zero. In theory, the PPS push-pull converter can operate based on the linear control curve as shown in Fig. 6.5 when *k*=0.

The upper limit for *k* can be derived from the following analysis. As the value of *k* is increasing, the operation modes will only have mode a(+), d(+) in boost mode and mode a'(-), d'(-) in buck mode as shown in Fig. 6.5(a) (b). In mode a(+) d(+), the relationship between D and φ is:

$$-2\varphi^2 + 2D\varphi + \frac{1}{2}D - D^2 - 2k = 0, \text{ where } 0<D<1 \quad (44)$$

The real roots of the equation are:

$$\varphi = \frac{1}{2}D \mp \frac{1}{2}\sqrt{D - D^2 - 4k}, \text{ where } 0<D<1 \quad (45)$$

In order to have real roots, $D - D^2 - 4k$ should be larger than 0, so the upper limit of *k* is:

$$k<0.0625 \quad (46)$$

With the similar approach, the same upper limit is obtained for *k* in mode a'(-) and d'(-).

If k>0.0625, the PPS control can't be applied, because there is no zero-level voltage across the reflected leakage inductance any more, which means there is no interval in which the leakage current remains constant.

The normalized voltage gain when k>0.0625 is:

$$\frac{V_2}{nV_1} = \frac{1}{2k} * \frac{1}{1-D}\left(-2\varphi^2 + 2D\varphi - D^2 + \frac{1}{2}D\right), k = \frac{2f_s L_s}{R_L} \quad (47)$$

The limit of k - 0<k<0.0625 - is general to all PPS converters and it provides an important guideline while designing the converter parameters - f_s , L_s, R_L. Based on the circuit specifications given in the references, k=0.022 in [14] and k=0.0265 in [16] – both are within the k limit. However, neither [14] or [16] mentioned how to choose the circuit parameter k in order to ensure PPS control strategy.

6.7 Hardware Design and Experimental Results

6.7.1 Hardware Design

In a household micro-grid, dc instead of conventional ac can be used as the main bus. The voltage level of dc bus is typically 380V and that of the storage elements is typically 30-48V. Therefore, a bidirectional PPS push-pull converter with voltage gain of 8-13 is a good candidate for this application.

According to the proposed control map in Fig. 6.5, the PPS push-pull converter should be operating in 0.5<D<1. Some extreme duty cycles can't be realizable from efficiency point of view. If the duty cycle is too high, the voltage-gain will drop significantly considering the parasitic elements. In order to make up the decreased voltage gain, a much higher phase-shift ratio is needed. Therefore, the higher circulating current will introduce higher power losses, deteriorating the overall efficiency badly. So the range of 0.5<D<0.75 （2<NG<4）is

chosen. In order to achieve the gain of 8-13, the transformer turns ratio is designed to be 1:1:4.

In addition, the leakage inductance L_s (referred to the secondary side) is measured to be 32uH. The maximum power level of this converter is designed to be 1kW. If V_2 is fixed at 380V, so the minimum equivalent load resistance R_L on the secondary side is 144 ohm. From the proposed control map, the parameter k should be lower than 0.0625, so the switching frequency f_s should be lower than 136kHz according to $k = \frac{2f_s L_s}{R_L}$. Referred to Fig. 6.5, f_s is designed to be 50kHz (k=0.023) so as to have a relatively wide conversion ratio range, while ensuring the normal operation of PPS control. Considering the tradeoff between wide-voltage-gain range (lower k) and high power level (higher k), a higher switching frequency (<136kHz) could be chosen if the PPS converter is designed to be at a higher power, sacrificing some voltage-gain range though. This is a design tradeoff for different applications.

According to the operation principle in section 6.3 and the above circuit parameters, the voltage and current stresses of converter components are summarized in Table 6.3.

Then, a 30~48V/380V prototype rated at 100~1000W was built and operated according to the proposed control map. The specifications are listed in Table 6.4.

Table 6.3. Component stress of PPS push-pull prototype

Components	Voltage Stress (V)	Max. RMS Current (A)
$S_{1,2}$	95	23.5
$S_{3,4}$	95	2.8
$S_{5,6}$	380	5.7
C_s	95	-
$C_{1,2}$	190	-
L	-	34
L_s	-	8.1

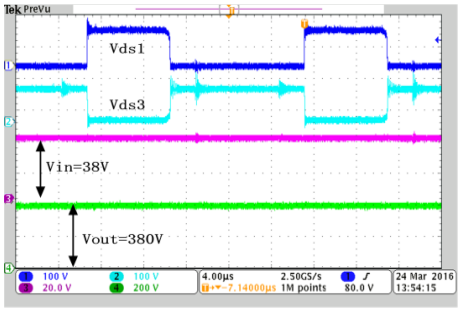
Table 6.4. Specifications of PPS push-pull prototype

Power Level	100W~1kW	$S_{1,2}$	IRFB4332PBF
LV Side (V_1)	30V~48V	$S_{3,4}$	IRFP450
HV Side (V_2)	380V	$S_{5,6}$	IPW60R 190C6
Frequency (f_s)	50kHz	C_s	10uF
Turns Ratio	10:10:40	L	45uH
Leakage (L_s)	32uH	$C_{1,2}$	15uF

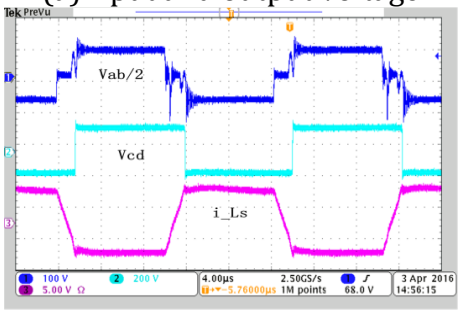
6.7.2 Experimental Results

The experimental waveforms in boost mode -mode d(+)- are given in Fig. 6.6. The voltage gain is designed to be 10 (NG=2.5) with D=0.6 according to the control map in Fig. 6.5(a). The load resistance R_L is 160Ω, so the circuit parameter $k = \frac{2f_s L_s}{R_L} = 0.002$. Referred to Fig. 6.5(a), the phase-shift ratio φ should be 0.1 (36°), while in practice $\varphi = 0.117$ (42°). The waveforms of input and output voltage are shown in Fig. 6.6(a), where the voltage gain of 10 can be achieved. In Fig. 6.6(b), the three-level ($V_{ab}/2$)and two-level (V_{cd}) square waves, as well as the leakage inductance current waveform are given. The waveforms match the analysis in Fig. 1.2, where there exists a period that the leakage current maintains constant. In Fig. 6.6(c), the ZVS operation waveforms of S_1 are shown. When the driving signal V_{gs1} becomes high, the transistor is turned on with ZVS operation because i_{n1} is negative, satisfying the ZVS constraints in (32). Similarly, the ZVS operation of $S_{3,5}$ can be demonstrated in Fig, 6.6(d) and 6.6(e).

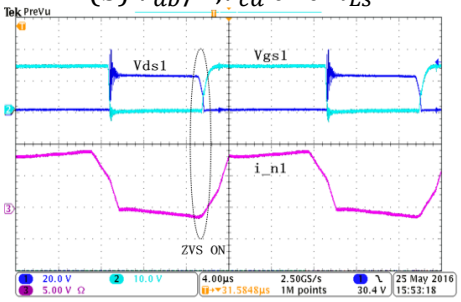
As analyzed in section 6.5, transistors $S_{1,2}$ will be hard switched in mode b'(+). The Fig. 6.7 demonstrates the analysis, where the converter operates in b'(+) and transistor $S_{1,2}$ are hard switched obviously. So this mode is typically avoided in normal operation.



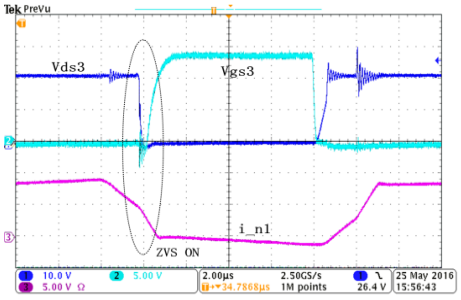
(a)Input and output voltage



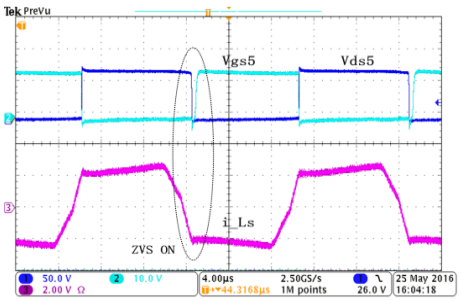
(b) $V_{ab}/2$,V_{cd} and i_{Ls}



(c) ZVS operation of *S1*



(d) ZVS operation of *S3*



(e) ZVS operation of *S5*

Fig. 6.6. Experimental waveforms in mode d(+) for PPS push-pull converter

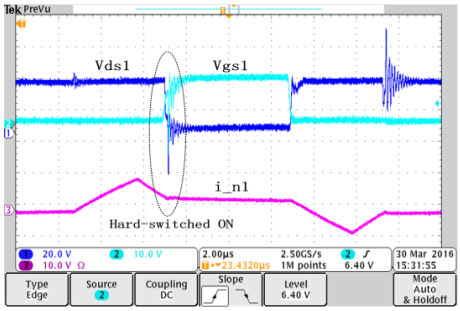
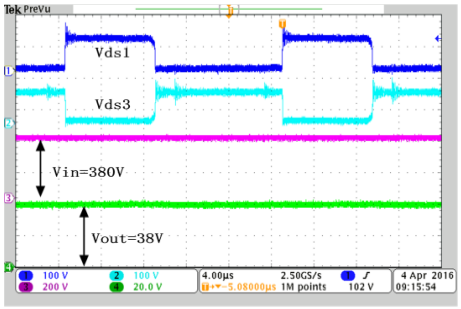


Fig. 6.7. Hard-switched operation of S1 in mode b'(+) for PPS push-pull converter

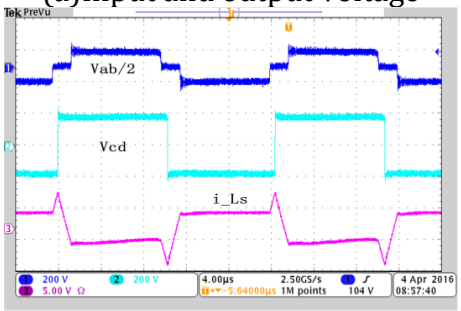
The experimental waveforms in buck mode -mode c(-) - are given in Fig. 6.8. The voltage gain is designed to be 0.1(NG=0.4) with D=0.6 according to the control map in Fig. 6.5(b). In addition, the circuit parameter $k = 0.01$. Referred to Fig. 6.5(b), the phase-shift ratio φ should be 0.03 (11°), while $\varphi = 0.02$ (7°) in practice. The waveforms of input and output voltage are shown in Fig. 6.8(a). The voltage gain of 0.1 can be achieved. In Fig. 6.8(b), the three-level ($V_{ab}/2$)and two-level (V_{cd}) square waves, as well as the leakage inductance current waveform are given, where there exists a period that the leakage current maintains constant. Similarly, ZVS operation can be achieved for transistors $S_{1,3,5}$. The soft switching waveforms are pretty similar to Fig. 6.6(c)-(e), which are not given.

In order to verify the validity of the control map, Fig. 6.9 is plotted to compare the theoretical results, simulation results and experimental results. In Fig. 6.9(a), the solid line represents theoretical control curve and the black dots are simulation results. All operation

modes are simulated to verify the proposed control map. The following circuit parameters are used: turns ratio 1:1:4; $f_s = 50\text{kHz}$; $L_s = 32\text{uH}$; $V_2 = 400\text{V}$; $V_1 = 10\sim90\text{V}$; $P = 1\text{kW}$, $k = 0.02$. For a specific conversion ratio, the duty cycle value is determined, while several phase-shift ratios could be chosen to ensure the PPS control. Each phase-shift ratio corresponds to one operation mode. As shown, the simulation results closely match the theoretical values in all operation modes, if the conduction loss or switching loss is not considered. In Fig. 6.9(b), the solid line stands for the theoretical control curve with k=0.005(R_L=640Ω) in the boost mode and the black dots are the experimental results. The prototype specifications have been given in Table 6.4. From this comparison, the experimental phase-shift ratios are higher than the theoretical ones, because the parasitic components of MOSFET and transformer will introduce power losses. Higher phase-shift ratio is needed to transmit more power. Generally, the experimental results are close to the calculated curve, verifying the control map.

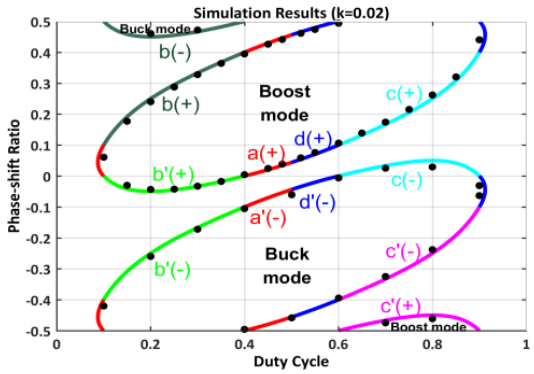


(a)Input and output voltage

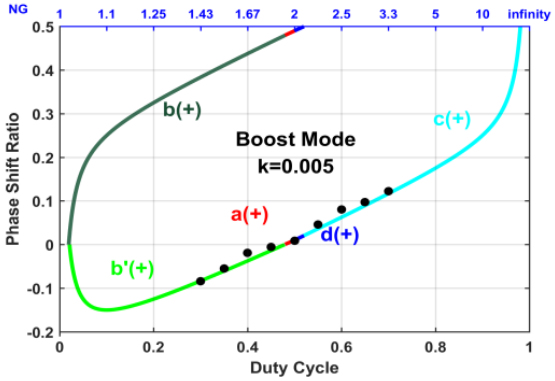


(b) $V_{ab}/2$,V_{cd} and i_{Ls}

Fig. 6.8. Experimental waveforms in mode c(-) for PPS push-pull converter



(a) Simulation results with k=0.02



(b) Experimental results with k=0.005

Fig. 6.9. Measured control map for PPS push-pull converter

The measured efficiency curves of the PPS push-pull converter are plotted in Fig. 6.10. The solid lines in different colors represent different conversion ratios as denoted. In boost mode, the peak efficiency is 94.1% at 752W when the voltage gain is 7.9. The lower the conversion ratio, the higher the efficiency is. In the buck mode, the peak efficiency is 94.5% at about -547W when the voltage gain is 0.127.

In Fig. 6.11, the efficiency comparison between PPS and PS control in boost mode is given. The secondary voltage V_2 is fixed at 380V and the load resistance is 160ohm. As shown, the efficiency of PPS control is well above 91% when V_1 is 30-48V. However, for PS control, the efficiency will drop badly if V_1 is deviated from the nominal value 48V (D=0.5). This result

indirectly proves the feature of wide conversion ratio for the PPS push-pull converter, as analyzed in Fig. 6.5.

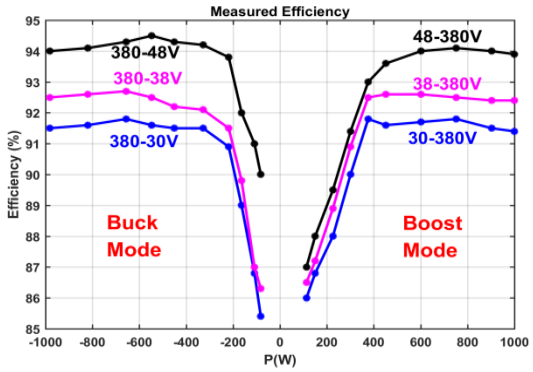


Fig. 6.10. Measured efficiency of PPS push-pull converter

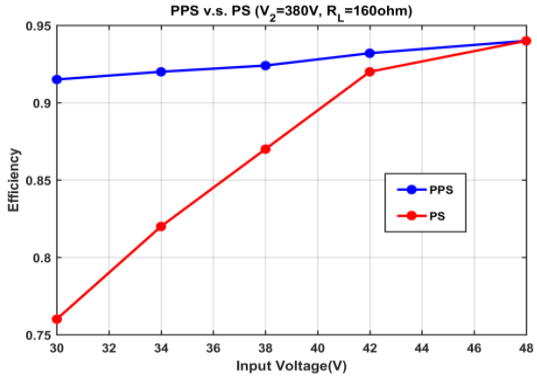


Fig. 6.11. Comparison of PPS and PS control for push-pull converter

6.8 Conclusion

In this chapter, a bidirectional three-level PPS converter is investigated with new add-on feature of PPS control scheme. Extensive analysis is presented to reveal the comprehensive characteristics for this converter. According to different profiles of leakage current waveform, 12 operation modes are traversed. A control map based on the complete analysis is proposed to assist converter design and operation that can effectively avoid high-circulating-current regions, low-power-transmission-capability regions and hard-switched regions. A 30~48V/380V prototype rated at 100~1000W was built to verify the analysis.

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CHAPTER 7: Analysis and Design of a Family of Two-level PWM Plus Phase-Shift Modulated DC-DC Converters

7.1 Introduction

An isolated bidirectional dc-dc converter (IBDC) with PWM plus Phase-shift (PPS) control was proposed in [1]. The duty cycle of transistors is used to match the voltage amplitudes of both sides and phase-shift is controlled to regulate the power flow. In [2]- [5], PPS control strategy was extended to the dual-inductor half-bridge converter, winding-coupled bidirectional converter, push-pull converter and dual-half-bridge (DHB) converter respectively, forming the three-level PPS converters.

In [6], a technique to synthesize a family of two-level PPS IBDCs was presented. The voltage on the primary side of the transformer is a two-level square wave, so they can be defined as two-level PPS converters. Literature [6] presented three groups of switch cells, from which any two cells belonging to different groups can be combined to form a new two-level PPS converter. Compared with the DAB, the two-level PPS converters have the advantages of guaranteed ZVS operation, high conversion ratio, low current ripples and wide voltage-gain variation range. Compared with the traditional PS control, the efficiency of the PPS-modulated converter will not drop badly even if the conversion ratio deviates from the nominal one significantly, because the duty cycle is adjusted to limit the leakage current. The two-level PPS converters are more suitable for high voltage gain, wide conversion-ratio-variation-range and low to medium power level applications.

In this chapter, operation modes, unified solution of the power transmission capability, component stresses, ZVS region and control maps of the two-level PPS converter are presented to assist converter operation and design. A 29-67V/380V prototype – the combination of group (C+A) - rated at 100~1000W was built to verify the analysis. The contents in this chapter have been published in my journal paper [7].

7.2 Nomenclature

$\boldsymbol{C1}, \boldsymbol{C2}$: Capacitors;

$\boldsymbol{D}$: Duty cycle of S_1 and S_1'; $\boldsymbol{1-D}$: Duty cycle of S_2 and S_2';

$\boldsymbol{i_{S1,2}}$: Current of $S_{1,2}$, positive when flows from drain to source;

$\boldsymbol{i_{Ls}}$: Leakage current;

$\boldsymbol{i_L}$: Transient inductor current;

$\boldsymbol{I_L}$: Average inductor current;

$\Delta \boldsymbol{i_L}$: Current ripple of the inductor

$\boldsymbol{L_s}$: Leakage inductance referred to the primary side;

$\boldsymbol{L}$: Inductance of the inductor;

$\boldsymbol{1:n}$: transformer turns ratio (n>1);

$\boldsymbol{N_A}$,$\boldsymbol{N_B}$,$\boldsymbol{N_C}$: The negative amplitude of the two-level square wave on the output port of a switch cell from group A, B, C;

$\boldsymbol{P}$: Transmitted power;

$\boldsymbol{P_A}$,$\boldsymbol{P_B}$,$\boldsymbol{P_C}$: The positive amplitude of the two-level square wave on the input port of a switch cell from group A, B, C;

$\boldsymbol{S_{1,2}}$: MOSFET 1,2 on the primary side;

$\boldsymbol{S_{1,2}}'$: MOSFET 1,2 on the secondary side;

$\boldsymbol{V_p}$: Voltage level before L_s;

$\boldsymbol{V_s}'$: Voltage level after L_s, referred to the primary side;

$\boldsymbol{V_s}$: Voltage level after L_s, referred to the secondary side;

$\boldsymbol{V_A}$,$\boldsymbol{V_B}$,$\boldsymbol{V_C}$: Voltage level on the input port of a switch cell from group A, B, C;

$\boldsymbol{V_{Ls}}$: Voltage across the leakage inductance;

$\boldsymbol{V_{C1,C2}}$: Voltage across the capacitor $C1, C2$;

∅: Phase-shift ratio between the rising edges of driving signal of S_1 and $S_1{}'$, which is equal to the phase-shift angel over 2π.

7.3 Review of Two-level PPS Converters

The block diagram of the two-level PPS converter is shown in Fig. 7.1, where the positive current direction is defined by the red arrow. Any two cells belonging to different groups given in Fig. 7.2 can be synthesized into a PPS converter. Some switch cells can be modified to their equivalent cells. For example, switch cell (b1') is the equivalent switch cell of (b1), by changing the position and direction of switch S_1. Furthermore, only two-switch cells are considered to reduce the degree of freedom. Otherwise, one more switch will contribute to tens of different switch cells. Finally, the switch cell (c) in [6] is dysfunctional by analysis and simulation, so it's not listed here.

The left side of the switch cell is defined as the input port, which is connected to a voltage source $V_A/V_B/V_C$. The right side is defined as the output port, which is connected to one of the transformer windings. These two-switch cells can be divided into three groups in terms of square-wave amplitudes of their output ports. Assuming all components are ideal and the voltage on the capacitor is constant in one switching cycle [6]:

1) Group A: switch cell (a1) ,(a2)

$$P_A = (1 - D)V_A, N_A = DV_A \quad (1)$$

2) Group B: switch cell (b1), (b1'), (b2), (b2'), (b3)-(b7)

$$P_B = V_B, N_B = \frac{DV_B}{1-D} \quad (2)$$

3) Group C: switch cell (c1), (c1'), (c2), (c3)

$$P_C = \frac{(1-D)V_C}{D}, N_C = V_C \quad (3)$$

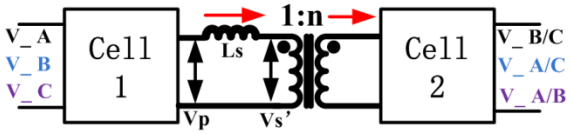


Fig. 7.1. Block diagram of a two-level PPS IBDC

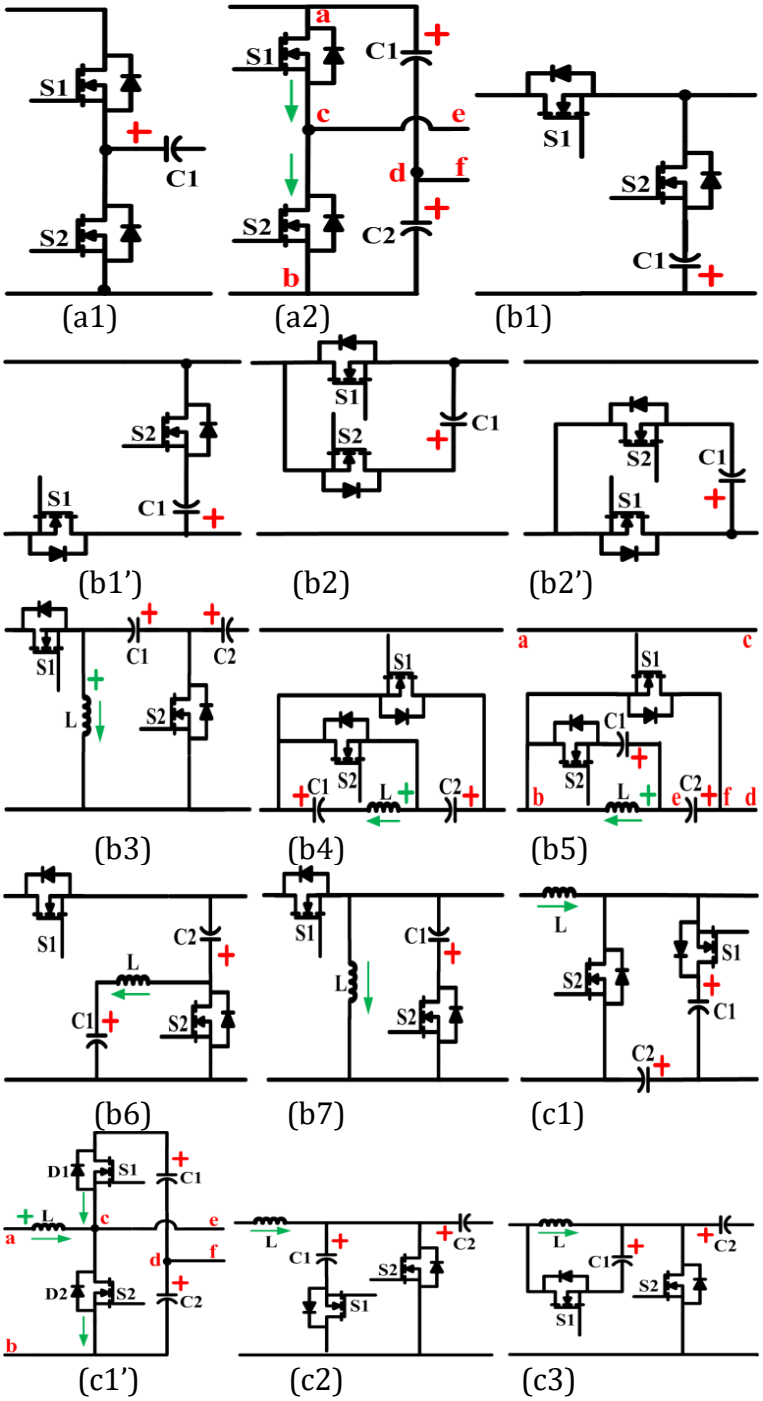


Fig. 7.2. Two-switch cells of two-level PPS IBDCs

7.4 Operation Modes

Fig. 7.3 shows the typical operating waveforms of any two-level PPS IBDCs. To give an example, switch cell (b2') and switch cell (a2) are synthesized into a PPS IBDC by inserting a transformer, shown in Fig. 7.4. The positive amplitude of V_p is $V_1 = P_B = V_B$ and the negative amplitude of V_p is $V_2 = N_B = \frac{DV_B}{1-D}$. Similarly, $V_3 = P_A{}' = (1-D)V_A/n$ and $V_4 = N_A{}' = DV_A/n$. On one hand, D is regulated to ensure amplitudes of the two square waves match each other, where $V_1 = V_3$ ($V_B = \frac{(1-D)V_A}{n}$) and thus $V_2 = V_4$ ($\frac{DV_B}{1-D} = \frac{DV_A}{n}$). As a result, the leakage current will be constant during the interval ($t_1 \sim t_2$ and $t_3 \sim t_4$). One the other hand, φ is modulated to control the power flow.

For any two-level PPS IBDC, D is from 0 to 1, while φ can be adjusted from -0.5 ($-180°$) to 0.5 (180°). According to different relationships between D and φ, 8 operation modes are given in Table 7.1. When power flows from primary side to secondary side, it's defined as forward mode and P>0. When power flows from secondary side to primary side, it's defined as flyback mode and P<0.

Table 7.1. Operation modes of two-level PPS IBDC

Power	Relationship between D & φ	Mode
Forward $P > 0$	$0 < D < \varphi < 0.5$	b
	$0 < \varphi < D < 0.5$	a(1)
	$0 < \varphi < 1 - D < 0.5$	a(2)
	$0 < 1 - D < \varphi < 0.5$	c
Flyback $P < 0$	$-0.5 < \varphi < -D < 0$	b'
	$-0.5 < -D < \varphi < 0$	a'(1)
	$-0.5 < D - 1 < \varphi < 0$	a'(2)
	$-0.5 < \varphi < D - 1 < 0$	c'

7.5 Unified Solution of the Power Transmission Capability

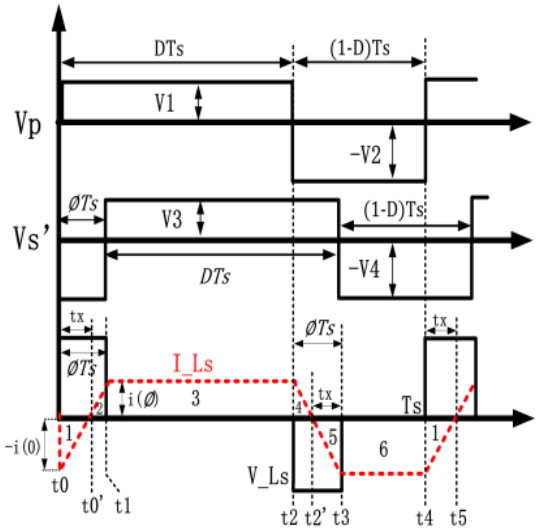


Fig. 7.3. Operating waveforms of the two-level PPS IBDC

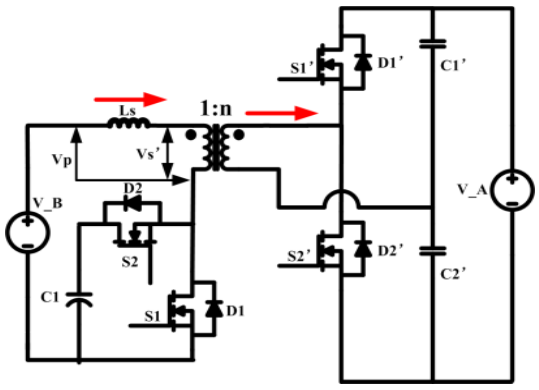


Fig. 7.4. Topology of cell (b2') + cell (a2)

In this section, the unified solution of the power transmission capability for each operation mode is derived, applicable for the family of two-level PPS converters. The unified solution provides an important tool to continue on the following analysis, such as the component stress analysis, ZVS operation analysis and the control map derivation. Mode a(2) in Fig. 7.3 is analyzed in details to exemplify the derivation.

For simplicity, a few assumptions are made as follows. The parasitic capacitance of the transistors and diodes is ignored. The leakage inductance is much smaller than the

magnetizing inductance. The voltage on the capacitor is considered to be a constant in one switching cycle. Dead-time between the complimentary driving signals is neglected.

During $t_0 \sim t_1$, i_{Ls} is increasing linearly from $-i(0)$ to $i(\phi)$, thus the current difference is:

$$\Delta i_{Ls} = i(0) + i(\phi) \tag{4}$$

Assuming i_{Ls} increases to 0 and changes its direction at t_x:

$$t_x = \frac{i(0)}{\Delta I_{Ls}} * \phi T_s \tag{5}$$

From Fig. 7.2, all the switch cells in group A and group C have one or two capacitors directly connected to their output ports. As known, the net change of the capacitor voltage must be zero over one switching period in steady state. Therefore, the integral of the capacitor current over one switching period should be zero. No matter what is the switch cell combinations (group A+B, group A+C or group B+C), the i-s area of leakage inductance current (either on primary or secondary side) above the horizontal axis should be equal to that under the horizontal axis in one switching cycle, i.e.:

$$< i_{Ls} >= 0 \tag{6}$$

$$[2(\mathrm{D} - \varphi)T_s + 2(\varphi T_s - t_x)] * \frac{i(\phi)}{2} = [2(1 - \mathrm{D} - \varphi)T_s + 2t_x] * \frac{i(0)}{2} \tag{7}$$

According to (4), (5), (7):

$$\mathrm{i}(\varphi) = (1 - \mathrm{D}) * \Delta i_{Ls} \tag{8}$$

$$\mathrm{i}(0) = \mathrm{D} * \Delta i_{Ls} \tag{9}$$

$$t_x = D * \varphi T_s \tag{10}$$

The transmitted power in one switching cycle is:

$$PT_s = Area\ (-1+2+3)V1 + Area\ (4-5-6)(-V2)$$

$$= [\frac{-D\Delta i_{Ls} t_x}{2} + \frac{(1-D)\Delta i_{Ls}(\varphi T_s - t_x)}{2} + (1-\mathrm{D})\Delta i_{Ls}(D-\varphi)T_s]V_1$$

$$+ [\frac{(1-D)\Delta i_{Ls}(\varphi T_s - t_x)}{2} - \frac{D\Delta i_{Ls} t_x}{2} - D\Delta i_{Ls}(1-D-\varphi)T_s](-V_2) \quad (11)$$

From (1)-(3), no matter what is the switch cell combinations, the ratio of positive amplitude of the two-level square wave to its negative amplitude is fixed at:

$$\frac{P_A}{N_A} = \frac{P_B}{N_B} = \frac{P_C}{N_C} = \frac{1-D}{D} \quad (12)$$

That is,

$$\frac{V_1}{V_2} = \frac{V_3}{V_4} = \frac{1-D}{D} \quad (13)$$

Finally, *D* is regulated to match the amplitudes of two square waves, i.e.:

$$V_1 = V_3\ and\ V_2 = V_4 \quad (14)$$

According to (8)- (11), (13), (14), a unified solution to the power transmission capability in mode a(2) is derived:

$$P = \frac{V_1 V_4}{L_s f_s} * \frac{\varphi}{D} * [D - \frac{\varphi}{2(1-D)}] \quad (15)$$

With the similar method, the unified solutions for different operating modes are given in Table 7.2, which are applicable for the whole family of two-level PPS IBDCs. With the unified solution, it's easy to figure out the power transmission capability of all two-level PPS converters to facilitate further analysis.

Table 7.2. Unified solution of the two-level PPS IBDC

Power Transmission Capability	**Mode**
$P_{a\&a'} = \frac{V_1 V_4}{L_s f_s} * \frac{\varphi}{D}[D - k * \frac{\varphi}{2(1-D)}]$	$\begin{cases} k = 1 \ \ Mode\ a(1), a(2) \\ k = -1\ Mode\ a'(1), a'(2) \end{cases}$
$P_{b\&b'} = k * \frac{V_1 V_4}{L_s f_s} * \frac{D}{(1-D)}(\frac{1}{2} - k * \varphi)$	$\begin{cases} k = 1 \ \ Mode\ b \\ k = -1 \ \ Mode\ b' \end{cases}$
$P_{c\&c'} = k * \frac{V_1 V_4}{L_s f_s} * \frac{1-D}{D} * (\frac{1}{2} - k * \varphi)$	$\begin{cases} k = 1 \ \ Mode\ c \\ k = -1 \ \ Mode\ c' \end{cases}$

7.6 Component Stress

In this section, the voltage/current stress of some important components - voltage on $C_{1,2}$, current ripple and average current of *L,* voltage stress (VS) and rms current stress of $S_{1,2}$ - of all switch cells will be given. For simplicity, while calculating the RMS current, the trapezoidal leakage current waveform is approximated to be a square wave. In addition, the inductor current ripple of cells (b3) (b7) (c1)-(c3) is neglected. The defined polarity is shown in Fig. 7.2 and the derived results are given in Table 7.3 and Table 7.4.

In addition, some switching cells – (b1)(b2)(b4)(b5)(b6) - have no dc blocking capacitor(s) at the output port, so the transformer has to sustain dc-bias current, causing some issues such as transformer noise, over-heat and so forth. For PPS converters including the above cells, they are not suitable for high-power-level applications, because the transformer may enter saturation region easily.

Table 7.3. Stresses of capacitor/inductor for two-level PPS IBDC

Cell	V_{C1}	V_{C2}	Δi_L	I_L
(a1)	$\mathrm{D}V_A$	--	--	--
(a2)	$(1-\mathrm{D})V_A$	$\mathrm{D}V_A$		
(b1)	$\frac{D}{1-D}V_B$	--		
(b2)	$\frac{1}{1-D}V_B$	--		
(b3)	$\frac{D}{1-D}V_B$	$\frac{D}{1-D}V_B$	$\frac{V_B}{2L}DT_S$	$\frac{P}{V_B}$
(b4)		$\frac{1}{1-D}V_B$		0
(b5)		V_B		
(b6)		$\frac{D}{1-D}V_B$		
(b7)		--		$\frac{P}{V_B}$
(c1)(c3)	$\frac{1-D}{D}V_C$	V_C	$\frac{V_C}{2L}(1-D)T_S$	$\frac{P}{V_C}$
(c2)	$\frac{V_C}{D}$			

Table 7.4. Stresses of switch for two-level PPS IBDC

Cell	VS: S_1	VS: S_2	RMS of S_1	RMS of S_2
(a1) (a2)	V_A	V_A	$\frac{V_A\lvert\varphi\rvert T_s}{L_s}\sqrt{D}$	$\frac{V_A\lvert\varphi\rvert T_s}{L_s}\frac{D}{\sqrt{1-D}}$
(b1) (b2)	$\frac{V_B}{1-D}$	$\frac{V_B}{1-D}$	$\frac{V_B\lvert\varphi\rvert T_s}{L_s}\sqrt{D}$	$\frac{V_B\lvert\varphi\rvert T_s}{L_s}\frac{D}{\sqrt{1-D}}$
(b3) (b7)			$(\frac{P}{V_B}+\frac{V_B\lvert\varphi\rvert T_s}{L_s})\sqrt{D}$	$\left(\frac{D}{1-D}\frac{V_B\lvert\varphi\rvert T_s}{L_s}-\frac{P}{V_B}\right)\times\sqrt{1-D}$
(b4) (b5) (b6)			$\frac{V_B\lvert\varphi\rvert T_s}{L_s}\sqrt{D}\times\sqrt{1+\frac{1}{3}(\frac{DL_s}{2\varphi L})^2}$	$\frac{V_B\lvert\varphi\rvert T_s}{L_s}\frac{D}{\sqrt{1-D}}\times\sqrt{1+\frac{1}{3}(\frac{(1-D)L_s}{2\varphi L})^2}$
(c1) (c2) (c3)	$\frac{V_C}{D}$	$\frac{V_C}{D}$	$(\frac{V_C\lvert\varphi\rvert T_s}{L_s}-\frac{P}{V_C})\sqrt{D}$	$\left(\frac{D}{1-D}\frac{V_C\lvert\varphi\rvert T_s}{L_s}+\frac{P}{V_C}\right)\times\sqrt{1-D}$

7.7 Analysis of ZVS Operation

In this section, the ZVS operation of all switch cells is analyzed. Assuming all switch cells are located at the primary side and mode a(2) in Fig. 7.3 is analyzed. Then, the similar conclusion could be extended to different operation modes and different positions of the switch cells.

In order to ensure ZVS operation of $S_{1,2}$, the following constraints should be satisfied:

$$\begin{cases} i_{s1}(t_0) < 0 \\ i_{s2}(t_2) < 0 \end{cases} \tag{16}$$

1) Switch Cell (a1), (a2), (b1), (b1'), (b2), (b2')

The above cells contain no inductor. Cell (a2) in Fig. 7.2 is analyzed as an example. Before t_0, S_2 is turned off. The i_{Ls} is negative (flow from node e to c), so the leakage current is fed through the anti-parallel diode of S_1. At t_0 when S_1 is turned on, the ZVS operation can be achieved. Similarly, when S_2 is turned on at t_2, eq. (16) is satisfied.

2) Switch Cell (b4), (b5), (b6)

The above cells contain an inductor, which is only connected to one or two capacitors at a certain node. Cell (b5) is analyzed as an example. First, according to charge balance of $C_{1,2}$ and KCL at node e, the average value of I_L is 0, as shown in Table 7.3. Secondly, from t_0 to t_2, the voltage on L is $V_L = -V_{C2} < 0$, so i_L is decreasing; from t_2 to t_4, $V_L = V_{C1} > 0$, so i_L is increasing. Therefore, at t_0, the inductor current $i_L(t_0)$ is positive and then it decreases to $i_L(t_2) < 0$ at t_2. At t_0, S_2 is turned off and its antiparallel diode is blocked by V_{C1}. The i_{Ls} is negative (flow from node f to d), so $i_{s1}(t_0) = i_{Ls}(t_0) - i_L(t_0) < 0$. At t_0 when S_1 is on, the ZVS operation can be achieved. Similarly, when S_2 is turned on at t_2, (16) is satisfied.

3) Switch Cell (b3), (b7), (c1), (c1'), (c2), (c3)

The above cells contain an inductor, whose average current value is not zero. Cell (c1') is analyzed as an example. From Fig. 7.3 and eq. (8), the leakage current at t_2 is $i_{Ls}(t_2) = i_{Ls}(t_1) = i_{Ls}(\emptyset) = \frac{(V_1+V_4)}{L_s}(1-D)\emptyset T_s$. According to the current ripple and average current of inductor in Table 7.3, the inductor current at t_2 is $i_L(t_2) = I_L - \Delta i_L = \frac{P}{V_C} - \frac{V_C}{2L}(1-D)T_S$. Referred to the unified solution in Table 7.2, when the switch S_2 is turned on at t_2,

$i_{s2}(t_2) = i_L(t_2) - i_{Ls}(t_2) = -\left(\frac{D}{2L} + \frac{\emptyset^2}{2L_s D(1-D)}\right) < 0$. As a result, the ZVS operation can be achieved. Similarly, when S_1 is turned on at t_1, eq. (16) is satisfied.

The similar method has been used to analyze different operation modes and different positions of the switch cells. Under PPS control strategy, ZVS operation can be guaranteed for all active switches regardless of the load condition under the assumptions made in section 7.5.

7.8 Proposed Control Maps

In this section, the control maps for the two-level PPS converters are proposed, to assist converter operation and design in the low circulating current region. A circuit parameter *k* is proposed and its upper limit is found, providing a design limit to select switching frequency, leakage inductance, turns ratio and power level. Beyond the limit, the PPS control can't be operating normally, which has not been revealed before.

7.8.1 Combination of Group A +Group B

For the combination of group A and group B, switch cell from group B is better to be placed on the low voltage side. Because the voltage conversion ratio is maximized with this configuration:

$$\frac{V_A}{V_B} = \frac{n}{1-D} \tag{17}$$

Mode a(2) in Fig. 7.3 is analyzed as an example to derive the relationship between *D* and ∅, under different circuit parameters. According to (1), (2) and the unified solution in Table 7.2, the power transmission capability in mode a(2) is:

$$P = \frac{V_A V_B/n}{L_s f_s} * \varphi * [D - \frac{\varphi}{2(1-D)}] \tag{18}$$

In mode a(2), P>0 and the power flows from V_B to V_A. Assume that R_L is the equivalent load resistance on the high-voltage side and the power transmission efficiency is 100%:

$$P = \frac{V_A V_B/n}{L_s f_s} * \varphi * [D - \frac{\varphi}{2(1-D)}] = \frac{V_A^2}{R_L} \tag{19}$$

The output voltage can be figured out:

$$V_A = \frac{V_B/n}{L_s f_s} * R_L * \varphi * [D - \frac{\varphi}{2(1-D)}] \tag{20}$$

Under PPS control, the amplitudes of the two square waves are regulated to be equal. The voltage conversion ratio has been given in (17), i.e.:

$$\frac{V_A}{V_B} = \frac{1}{nL_s f_s} * R_L * \varphi * [D - \frac{\varphi}{2(1-D)}] = \frac{n}{1-D} \tag{21}$$

The following relationship between D and $\emptyset$ in mode a(2) is derived:

$$\varphi^2 - 2D(1-D)\varphi + k = 0, \text{where } k = \frac{2f_s L_s}{R_L/n^2} \text{ and } 0 < \varphi < 1 - D < \frac{1}{2} \tag{22}$$

Similarly, the relationships between D and $\emptyset$ in all operation modes are derived.

For P>0:

$$\begin{cases} \varphi = \frac{1}{2} - \frac{k}{2D^2} & Mode\ b \\ \varphi^2 - 2D(1-D)\varphi + k = 0 & Mode\ a(1), a(2) \\ \varphi = \frac{1}{2} - \frac{k}{2(1-D)^2} & Mode\ c \end{cases} \tag{23}$$

For P<0:

$$\begin{cases} \varphi = -\frac{1}{2} + \frac{k}{2D^2} & Mode\ b' \\ -\varphi^2 - 2D(1-D)\varphi - k = 0 & Mode\ a'(1), a'(2) \\ \varphi = -\frac{1}{2} + \frac{k}{2(1-D)^2} & Mode\ c' \end{cases} \tag{24}$$

Note that R_L is the equivalent load on high-voltage side if P<0.

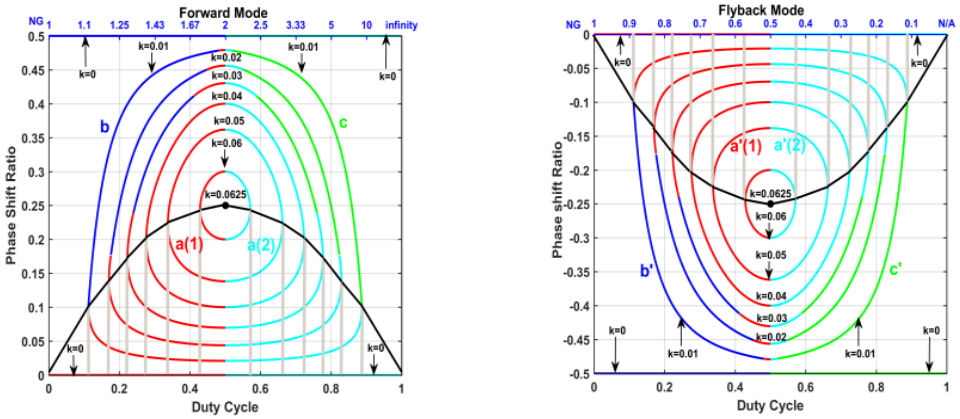
According to (23) (24) and the boundary conditions in Table 7.1, the control map is plot in Fig. 7.5. In different operation modes, the control curve is in different color. The blue axis represents the normalized gain (NG) to the transformer turns ratio n.

From the control map, several converter operation notes can be obtained:

1) If the NG is fixed, the *D* is fixed according to (17). Then if the load changes, only φ has to be regulated, jumping from one quasi-circle to another one with a different *k*;
2) If the load is fixed and only the NG changes, both *D* and φ have to be changed following the same quasi-circle;
3) If the NG and the load are fixed, the corresponding D and k are determined. However, φ has two possible values to be selected. As known, the higher phase-shift leads to higher circulating current. Therefore, the converter has to be operating in the low-circulating-current region, which is shaded by the grey lines in Fig. 7.5.
4) In the closed-loop design, the control map can provide the duty cycle and phase-shift limit to ensure the converter operate in the low-circulating-current regions. For boost mode($k\neq 0$), the limit of φ is $[0, \sqrt{k}]$ and the limit of D is $[\frac{1-\sqrt{1/4-\sqrt{k}}}{2}, \frac{1+\sqrt{1/4-\sqrt{k}}}{2}]$. For buck mode($k \neq 0$), the limit of φ is $[-\sqrt{k}, 0]$ and the limit of D is still $[\frac{1-\sqrt{1/4-\sqrt{k}}}{2}, \frac{1+\sqrt{1/4-\sqrt{k}}}{2}]$.
5) From the analysis in section 7.7, within the low-circulating current region, all transistors can be operated with ZVS.
6) As the value of $k = \frac{2f_s L_s}{R_L/n^2}$ is increasing (heavier load), the control curve will "shrink". As a result, the input-voltage-variation range becomes narrower. While designing the

converter, the tradeoff between input-voltage-variation range and power level should be considered.

7) The minimum k is 0, which means no load condition. The upper limit k is 0.0625. If k>0.0625, PPS control can't be applied, because there is no interval in which the leakage current remains at a constant value. The converter will work with a lower voltage gain – that is, $\frac{V_A}{V_B} = \frac{1}{nL_s f_s} * R_L * \varphi * [D - \frac{\varphi}{2(1-D)}]$. The limit of k provides a design constraint about selection of circuit parameters – switching frequency, leakage inductance, turns ratio, power level.



(a) Forward mode (b) Flyback mode

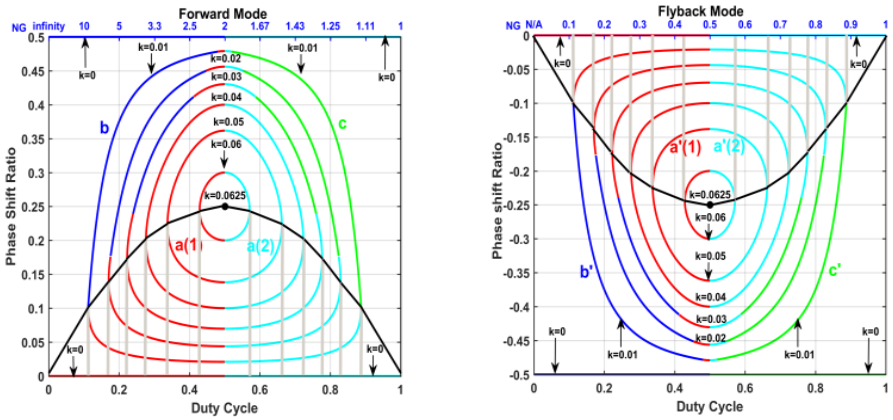
Fig. 7.5. Control map of group (B+A)

7.8.2 Combination of Group A +Group C

For the combination of group A and group C, switch cell from group C is better to be placed on the low voltage side. Because the voltage conversion ratio is maximized with this configuration:

$$\frac{V_A}{V_C} = \frac{n}{D} \qquad (25)$$

Similarly, the relationships between D and $\emptyset$ in all operation modes can be derived, which are exactly the same as (23) (24). The only difference is the normalized gain, as shown in the control map in Fig. 7.6 (a), (b).



(a) Forward mode (b) Flyback mode

Fig. 7.6. Control map of group (C+A)

7.8.3 Combination of Group B +Group C

For the combination of group B and group C, switch cell from group C is better to be placed on the low voltage side. With this configuration, the input inductor of the switch cell in group C will help reduce the input current ripple significantly.

The voltage conversion ratio of this combination is:

$$\frac{V_B}{V_C} = \frac{n(1-D)}{D} \tag{26}$$

The relationships between D and $\emptyset$ are derived:

For P>0:

$$\begin{cases} \varphi = \frac{1}{2} - \frac{k(1-D)^2}{2D^2} & Mode\ b \\ \varphi^2 - 2D(1-D)\varphi + k(1-D)^2 = 0 & a(1)\ a(2) \\ \varphi = \frac{1}{2} - \frac{k}{2} & Mode\ c \end{cases} \tag{27}$$

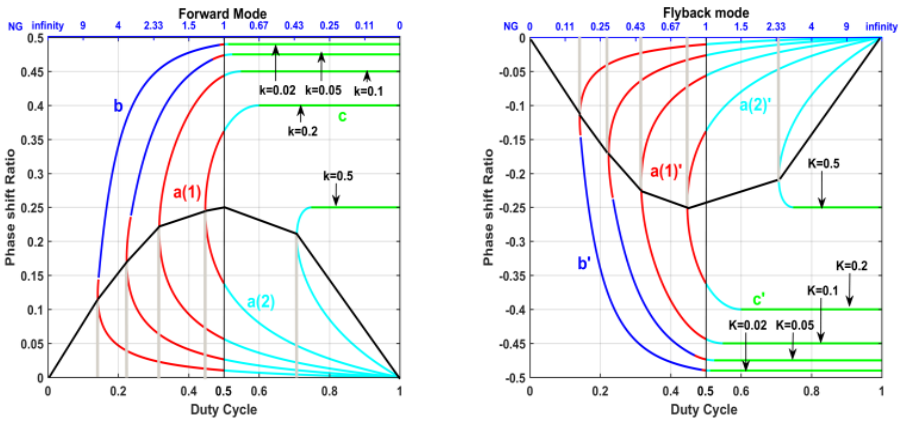
For P<0:

$$\begin{cases} \varphi = -\frac{1}{2} + \frac{k(1-D)^2}{2D^2} & Mode\ b \\ -\varphi^2 - 2D(1-D)\varphi - k(1-D)^2 = 0 & a(1), a(2) \\ \varphi = -\frac{1}{2} + \frac{k}{2} & Mode\ c \end{cases} \quad (28)$$

Where $k = \frac{2f_S L_S}{R_L/n^2}$, and R_L is the virtual load on the high-voltage side.

From the control map in Fig. 7.7, several converter operation notes can be obtained:

1) Unlike the aforementioned two combinations, this combination can either step up or step down the input voltage. Therefore, the input-voltage-variation range is much wider.
2) The converter should be operating in the low-circulating-current region, which is shaded by the grey lines in Fig. 7.7.
3) In the closed-loop design, the control map can provide the duty cycle and phase-shift limit. For boost mode($k \neq 0$), the limit of φ is $[0, \sqrt{k}(1-\sqrt{k})]$ and the limit of D is $[\sqrt{k}, 1]$. For buck mode($k \neq 0$), the limit of φ is $[-\sqrt{k}(1-\sqrt{k}), 0]$ and the limit of D is still $[\sqrt{k}, 1]$.
4) The minimum k is 0, which means no load condition. As the value of k increases, the control curve will "shrink". As a result, the input-voltage-variation range becomes narrower, but the "control sensitivity" – that is, slop of the control curve – is higher. If $k > 0.25$, the NG will be always smaller than 1. The upper limit of k is 1.



(a) Forward mode (b) Flyback mode

Fig. 7.7. Control map of group (C+B)

7.9 Simulation and Experimental Results

7.9.1 Simulation Results

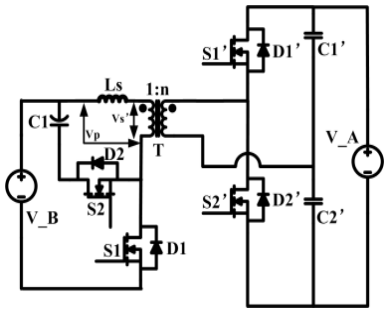
To verify the control maps proposed in section 7.8, three different combinations of the PPS converter are simulated with the parameters in Table 7.5.

The topologies and the simulated control curves are shown in Fig. 7.8 and Fig. 7.9. The black dots/stars represent the simulation results, while the solid lines stand for the theoretical control maps. For combinations of (C+A) and (C+B), the simulation results match the theoretical curves closely all over the operation range, as shown in Fig. 7.9(b), (c). While for the combination of (B+A), the simulation results have deviations with the theoretical curve in the high-circulating-current regions when 0<D<0.5, as shown in Fig. 7.9(a). The reason is that this combination has high input current ripples without an input inductor. When 0<D<0.5, switch S_2 will be turned on for more than half a cycle. The high input current will charge and discharge the capacitor C_1 and thus the voltage on C_1 will not be a constant, especially in the high-circulating-current regions. However, those unfavorable regions can be avoided by operating in the shaded area based on the control map in Fig. 7.5.

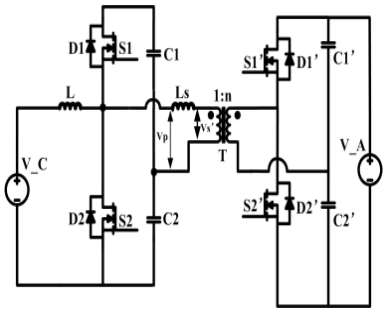
In Fig. 7.10, the RMS current of S_{1-4} for the topology in Fig. 7.8 (b) is plot. The solid lines represent the RMS current under PS control (D=0.5 is fixed), while the dashed lines represent that under PPS control. As shown, the current stresses under PPS control are much lower than those under PS control, especially when the input voltage varies within a wide range.

Table 7.5. Simulation parameters of the two-level PPS IBDCs

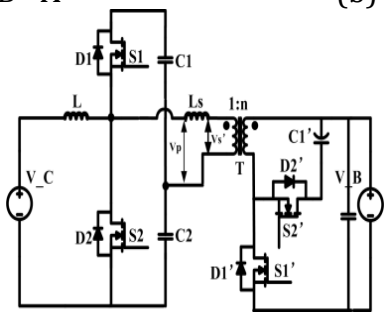
Group	**Pri. Side**	**Sec. Side**	**1:n**	L_s	f_s	**Inp./Out. Voltage**
B+A	(b1')	(a2)	1:4	10uH	50K	20~80-400V
C+A	(c1')	(a2)				20~80-400V
C+B	(c1')	(b1')				25~400-400V



(a) B+ A

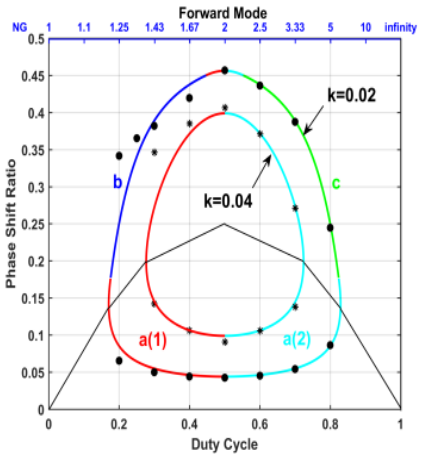


(b) C+A

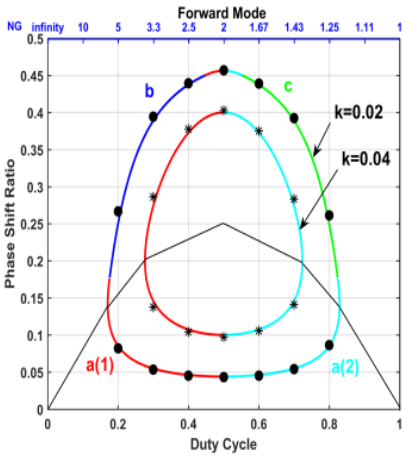


(c) C+B

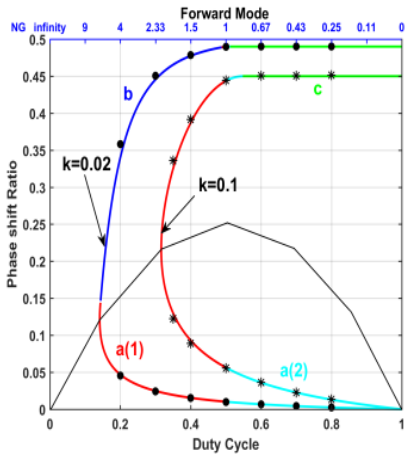
Fig. 7.8. Topologies of the simulated two-level PPS IBDC



(a) B+ A

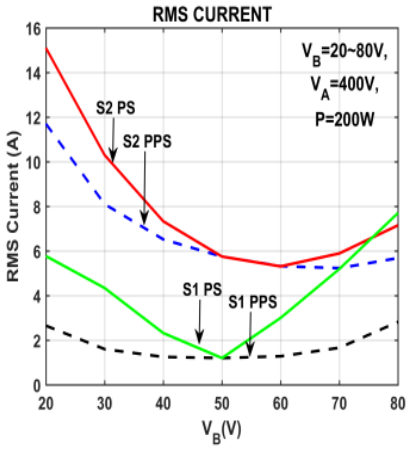


(b) C+A

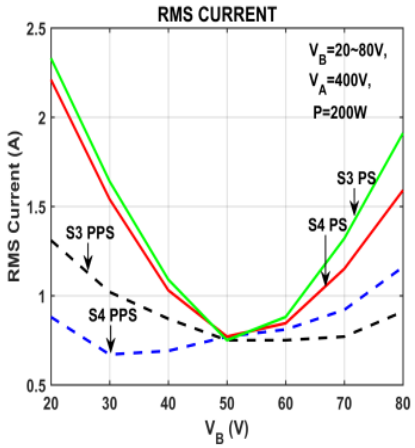


(c) C+B

Fig. 7.9. Simulated control maps for two-level PPS IBDC



(a) RMS of $S_{1,2}$



(b) RMS of $S_{3,4}$

Fig. 7.10. Simulated RMS current of combination C+A

7.9.2 Experimental Results

To further verify the analysis, a 29~67V/380V prototype – combination of (C+A) in Fig. 7.8(b) - rated at 100~1000W was designed and built.

According to the proposed control map in Fig. 7.6, the range of 0.3<D<0.7 (1.43<NG<3.3）is chosen to avoid extreme duty cycle values. In order to achieve the gain of 5.7-13, the transformer turns ratio is designed to be 1:4, and then the leakage inductance L_s is measured to be 2.31uH. The maximum delivered power is 1kW. If V_A is fixed at 380V, so the minimum equivalent load resistance R_L is 144 ohm. From the proposed control map, the upper limit of k is 0.0625, so the switching frequency f_s should be lower than 122kHz ($k = \frac{2f_sL_s}{R_L/n^2} < 0.0625$). Referred to Fig. 7.6, f_s is designed to be 50kHz (k=0.026) so as to have a wide voltage gain range. In addition, the voltage and current stresses of important components have been figured out in section 7.6. The parameters of the prototype are listed in Table 7.6.

Table 7.6. Prototype specifications of combination C+A

P	100W~1kW	S_1	STP52N25M5
V_C	29~67V	S_2	IRFB4332PBF
V_A	380V	$S_{3,4}$	IPW60R 190C6
f_s	50kHz	$C_{1,2}$	10uF
1:1:n	10:40	$C_{3,4}$	15uF
L_s	2.31uH	L	100uH

The experimental results in mode a(1) are shown in Fig. 7.11. The driving signals are given in Fig. 7.11(a). At this operating point, the voltage gain is 10 with D=0.4 according to (25), and k $= \frac{2f_sL_s}{R_L/n^2} = 0.006$, $\varphi = 9°$. The primary side V_c is 38V and the secondary side V_A is regulated to be 380V, as shown in Fig. 7.11(b). In Fig. 7.11(c), the two-level square waves of V_p and V_s, and the leakage current waveform match the analysis in Fig. 7.3, where there is

an interval in which the leakage current remains at a constant value. Therefore, the circulating current and thus the conduction loss is reduced.

The experimental results in mode a(2) are shown in Fig. 7.12. The driving signals are given in Fig. 7.12(a). At this operating point, the voltage gain is 6.67 with D=0.6 according to (25), and k $= \frac{2f_S L_S}{R_L/n^2} = 0.012$, $\varphi = 18°$. The primary side V_c is 57V and the secondary side V_A is regulated to be 380V, as shown in Fig. 7.12(b). In Fig. 7.12(c) and 7.12(d), the waveforms of ZVS operation for S_{1-4} are given.

When the converter operates in the flyback mode (from V_A to V_c), the experimental results in mode a'(1) are shown in Fig. 7.13. The driving signals are given in Fig. 7.13(a). At this operating point, the voltage gain is 0.1 with D=0.6, and k $= \frac{2f_S L_S}{R_L} = 0.0045$, $\varphi = -9.6°$. The V_c is 38V and the V_A is regulated to be 380V, as shown in Fig. 7.13(b). Fig. 7.13 (c) shows the waveforms of V_p, V_s and i_{Ls}.

To verify the control map in Fig. 7.6, Fig. 7.14 is plotted to compare the experimental results and theoretical results. In Fig. 7.14, the solid line represents theoretical control map with k=0.012 and k=0.03, while the black dots are the experimental results. From the comparison, the experimental results have some deviations from the calculated curve, but the general profile is close. On one hand, the error is partially caused by the parasitic ESRs, so a higher phase-shift ratio is needed to transfer more power. Moreover, the negative amplitude of the primary square wave is not a strictly constant value, because the current flowing through C_2 is much higher than that through C_1, which is the unbalanced issue discussed in [8].

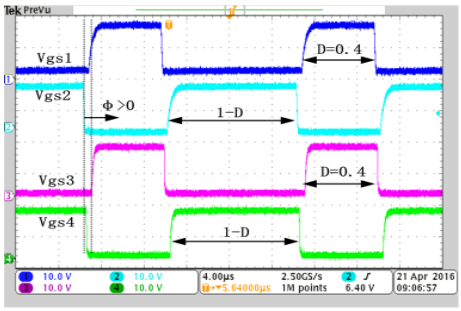
The measured efficiency versus power level is plotted in Fig. 7.15. Different colors represent different conversion ratios as denoted. In forward mode, the peak efficiency is 96.2% at about 600W when the voltage gain is 6.7. In flyback mode, the peak efficiency is 96.3% at 450W when the voltage gain is 0.15. The power loss distribution analysis when 48V-380V (D=0.5) and output power 450W is given in Table 7.7. At this operating point, the efficiency is 94.3% and the power loss is 27.2W. With soft-switching operation of transistors, the switching loss is estimated to be zero and only conduction loss is considered. As listed, the loss of the transformer is dominant and the inductor loss is the second highest. To further increase the efficiency, transformer and inductor with low ESRs should be redesigned.

Table 7.7. Estimated power loss of combination C+A

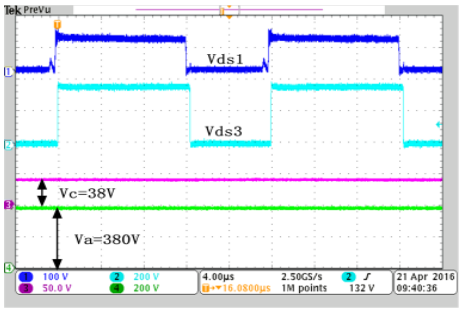
Device	**ESR**	**RMS Current**	**Power Loss**	**Loss Ratio**
s_1	60mΩ	3A	0.54W	2%
s_2	30mΩ	14 A	5.9 W	21.7%
s_3	200mΩ	2 A	0.8 W	2.95%
s_4	200mΩ	2 A	0.8 W	2.95%
L	80mΩ	9.8 A	7.7 W	28.3%
Tx	100mΩ	10 .1A	10.3 W	37.9%
C_1	10mΩ	3 A	0.09W	4.2%
C_2	10mΩ	10A	1W	
C_3	10mΩ	1.3A	0.035W	
C_4	10mΩ	1.3A	0.035W	

To make a comparison between PPS control and PS control, the converter in Fig. 7.8(b) was tested with PS control (D=0.5 fixed) and the experimental results are given in Fig. 7.16. Since the rms current stress under PS control is pretty high, the converter operates with lower voltage and power level. In Fig. 7.16(a), the leakage current i_{Ls} has high peak value instead of a “flat part” as the PPS control does. In Fig. 7.16(b), the efficiency of the converter is well above 90% under PPS control within the gain range of 6.5-10, while the efficiency

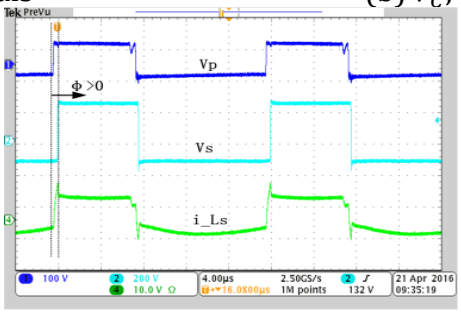
with PS control drops significantly when the conversion ratio deviates from the nominal value 8 due to the high leakage current.



(a) Driving signals

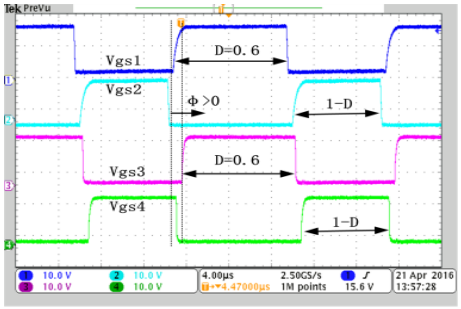


(b) V_C, V_A

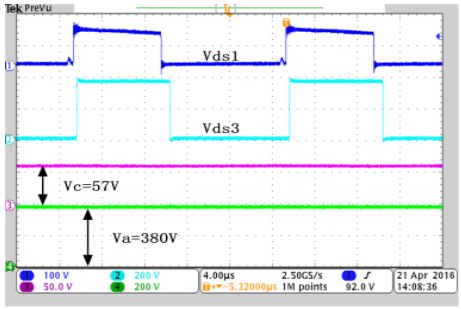


(c) V_p, V_s, i_{Ls}

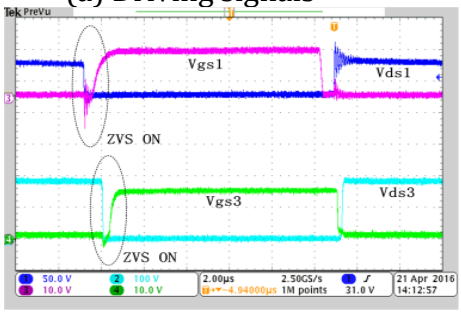
Fig. 7.11. Experimental results in mode a(1)



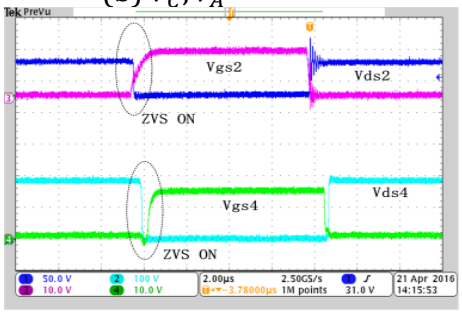
(a) Driving signals



(b) V_C, V_A

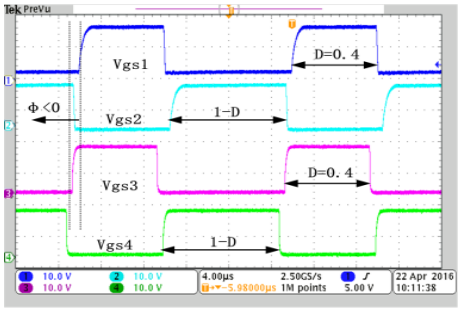


(c) ZVS operation of S_1, S_3

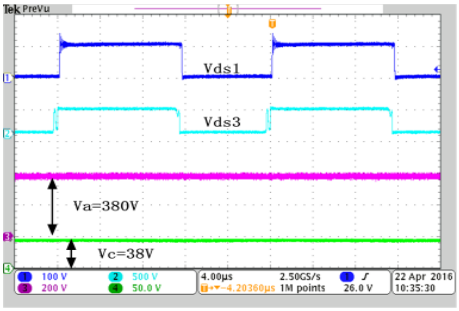


(d) ZVS operation of S_2, S_4

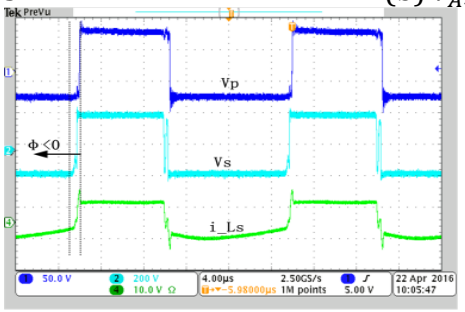
Fig. 7.12. Experimental results in mode a(2)



(a) Driving signals



(b) V_A, V_C



(c) V_p, V_s, i_{Ls}

Fig. 7.13. Experimental results in mode a'(1)

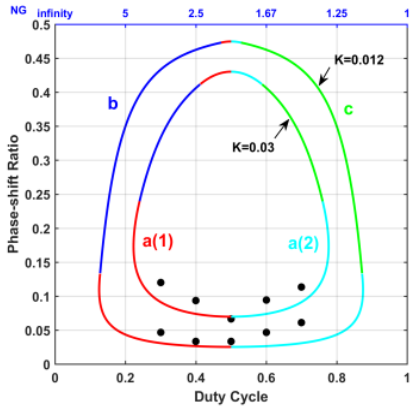


Fig. 7.14. Experimental control map for combination C+A

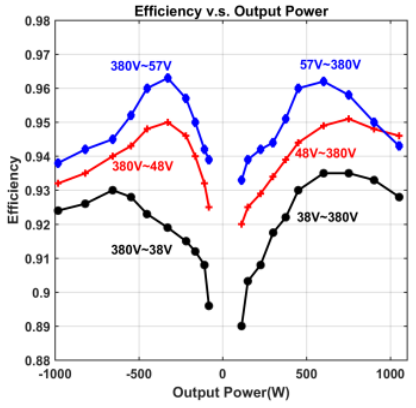
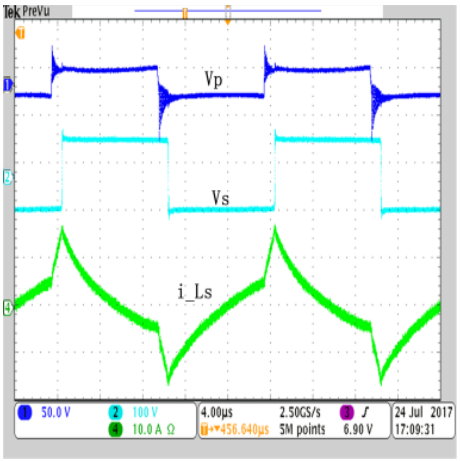
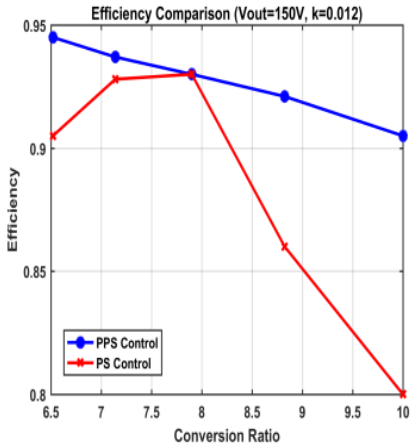


Fig. 7.15. Measured Efficiency for combination C+A



(a) V_p, V_s, i_{Ls} $(15-150V, k=0.012)$



(b) Efficiency comparison

Fig. 7.16. Experimental results with PS control strategy

7.10 Conclusion

In this chapter, the operation modes, power transmission capability and component stresses of a family of two-level PPS converters are analyzed. On the basis, the analysis of ZVS operation for all switch cells are given. In addition, control maps for three different combinations are proposed, assisting converter design and operation that can effectively avoid high-circulating-current regions. The simulation and experimental results verify the operating waveforms in different modes, ZVS operation and the control maps.

7.11 References

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