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The Reduction and Cancellation of Phase Noise in Digital Frequency
Synthesizers and Quadrature Receivers

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Electrical Engineering

by

Zuow-Zun Chen

2016

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ABSTRACT OF THE DISSERTATION

The Reduction and Cancellation of Phase Noise in Digital Frequency Synthesizers and Quadrature Receivers

by

Zuow-Zun Chen

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2016

Professor Mau-Chung Frank Chang, Chair

Circuit and system techniques for reducing phase noise in frequency synthesizers, and cancelling phase noise effect in quadrature receivers are presented.

Phase noise performance of digital phase-locked loops (PLLs) is limited by the time resolution of time-to-digital converters (TDC). In contrast to TDCs in the past that concentrate on the arrival time difference between the divider feedback edge and the reference signal edge. Our approach extracts the timing information that is embedded in voltage domain. This approach not only achieves a higher time resolution, lower phase noise, but also consumes less power. A digital background calibration circuit is also presented to reduce the output spurious tones when the digital PLL operates under fractional- N divisions.

Ring Oscillators (ROs) have the advantage of small area, wide tuning range, and multiphase output. However, their higher phase noise and higher sensitivity to supply noise may seriously deteriorate the wanted signal in wireless receivers. To circumvent this non-ideality, a low overhead phase noise cancellation technique for ring oscillator-based quadrature receivers is presented. The proposed technique operates in background and extracts ring oscillator phase noise as well as supply-induced phase noise from the digital PLL. The obtained phase noise information is then used to restore the randomly rotated baseband signal in digital domain.

In recent years, the unsilenced band at 57~64 GHz frequency range has motivated the building of high-data rate radio systems targeting wireless personal area network (WPAN) applications. To address this demand, a low-noise wide-band integer- N PLL is presented which serves as the carrier generator of a 60 GHz heterogeneous transceiver. The PLL employs sub-sampling phase detection technique to achieve low-noise performance, and provides 48 GHz LO and 12 GHz IF carrier signals for the heterogeneous transceiver.

The dissertation of Zuow-Zun Chen is approved.

William J. Kaiser

Danijela Cabric

Songwu Lu

Mau-Chung Frank Chang, Committee Chair

University of California, Los Angeles

2016

Dedicated to my parents

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1. **Z.-Z. Chen**, Y. Li, Y.-C. Kuan, B. Hu, C.-H. Wong, and M.-C. F. Chang, “Digital PLL for Phase Noise Cancellation in Ring Oscillator-Based I/Q Receivers,” in *Symp. VLSI Circuits Dig.*, 2016, pp. 114–115.
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6. B. Hu, F. Ren, **Z.-Z. Chen**, X. Jiang , and M.-C. F. Chang, “A 9-Bit TDC-Assisted Compressive-Sensing ADC With 4GS/s Equivalent Speed”, *IET Electronics Letters*, vol. 52, no. 6, pp. 430-432, 2016.
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Chapter 1

Thesis Overview

This dissertation covers topics on circuit and system techniques for reducing and cancelling phase noise in frequency synthesizers and quadrature receivers. It consists of 3 distinct parts. Chapter 2 introduces the design and analysis of a low-noise sub-sampling fractional- N digital PLL. Chapter 3 presents a phase noise cancellation technique for ring oscillator base quadrature receiver utilizing digital PLL, while an mm-Wave low-noise integer- N PLL for 802.15.3c heterodyne transceivers is shown in Chapter 4. A more detailed overview of each chapter is given below. Because each chapter presents a self-contained work, the conclusions are drawn at the end of each chapter, rather than at the end of the thesis.

Chapter 2: A Low-Noise Sub-Sampling Fractional- N Digital Frequency Synthesizer

Digital PLL are increasingly being used in modern communication systems. They are especially valuable because of their better scalability to advanced technologies and excellent re-configurability. Nonetheless, the phase noise performance of digital PLL is limited by the time resolution of time-to-digital converters (TDC). In contrast to TDCs in the past that concentrate on the arrival time difference between the divider feedback edge and the reference signal edge.

Our approach extracts the timing information that is embedded in voltage domain. This approach not only achieves a higher time resolution, lower phase noise, but also consumes less power.

Chapter 3: Digital PLL for Phase Noise Cancellation in Ring-Oscillator Based Quadrature Receivers

Ring Oscillators (ROs) have gained increasing interest for applications in radio receivers due to their small area, wide tuning range, and multiphase output. However, their higher phase noise and higher sensitivity to supply noise may seriously deteriorate the received signal. Although increasing PLL BW can reduce RO phase noise, the BW is limited to $F_{REF} / 10$ in conventional type-II PLL due to stability concerns. Larger BW also trades off higher spurious tones at PLL output. Our phase noise cancellation technique solves this constraint through a system level approach. It first extracts RO phase noise information from LO generator then applies it to the digital circuit to restore the randomly rotated baseband signal.

Chapter 4: A Low-Noise 48GHz CMOS PLL for 802.15.3c Heterodyne Transceivers

An integer- N PLL in 65 nm CMOS process is designed to generate low noise carrier signal for high-data rate 802.15.3c heterodyne transceivers. Sub-sampling phase detection technique is employed to achieve low phase noise performance. Moreover, unlike tradition sub-sampling

technique which directly samples the VCO output signal, in this work the VCO output is first divided-by-16 then sent to the phase detector. This increases the lock range and improves reliability.

Chapter 2

A Low-Noise Sub-Sampling Fractional- N Digital Frequency Synthesizer

2.1. Introduction

Digital phase locked-loop (PLL) has recently gain interest in communication and clocking systems due to its compact digital-loop filters and high re-configurability [1][2]. In advanced technology more and more functionality can be integrated within a smaller area. Digital PLLs take advantage of this by replacing the bulky passive loop filter in conventional analog PLLs with digital-loop filter. This not only reduces the size of the PLL, makes the BW to be easily configured, but also allows various calibration scheme to be implemented for resolving circuit non-idealities. The key circuit that enables these is the time-to-digital converter (TDC). Figure 2.1 shows the operation of a TDC. It senses the time difference between the reference signal and the divider feedback signal and quantizes the difference into digital codes. The digital codes are then processed in the digital-loop filter. There are two main noise sources in digital PLLs, namely the TDC quantization noise and the digital controlled oscillator (DCO) phase noise. The DCO phase noise dominates the PLL output high frequency offset phase noise. On the other hand, the TDC noise dominates the in-band portion of phase noise. The time resolution of the TDC

limits digital PLL in-band phase noise performance. The relation between TDC resolution and PLL in-band phase noise is shown by the equation below [3],

$$\mathcal{L}(f) = \frac{t_{res}^2}{12} \times \frac{1}{f_{ref}} \times \left(\frac{2\pi}{T_{osc}} \right)^2. \quad (2.1)$$

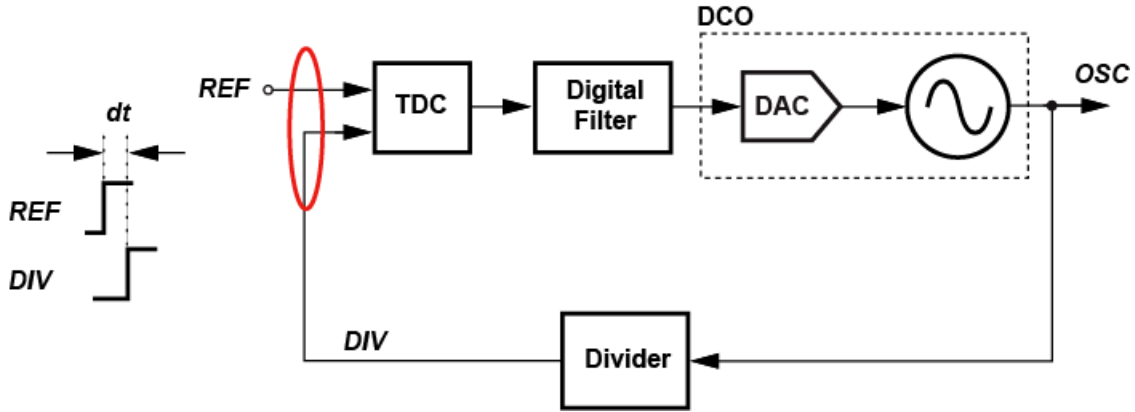


Figure 2.1: Digital PLL block diagram and TDC operation.

Where t_{res} is the TDC resolution, f_{ref} is the reference frequency, and T_{osc} is the oscillator period.

The equation indicates that if the TDC time resolution can continue to be improved, the in-band phase noise of the PLL can be reduced and ultimately approach the phase noise limit of the XTAL reference. There has been several research works in the past that proposed different TDC architecture, as shown in Fig. 2.2 [2]-[5]. The Vernier delay line senses the time information using delay cells and DFFs, this topology is relatively simple but has coarse time resolution. The resolution can be improved by adding a time amplifier stage to amplify the input time difference.

However, time amplifiers have worse linearity that cause spurious tones and noise folding at the PLL output. An alternative approach is the gated-ring oscillator, which inherits a 1st-order noise shaping function on the TDC quantization noise. Nonetheless, the method is more complicated and consumes more power. Although these approaches have very different architectures they all concentrate on the time difference between the reference signal edge and the divider feedback edge. In this work, we present a fractional- N digital PLL that employs a new time-to-digital conversion technique based on sub-sampling phase detection. Instead of focusing on the edge difference, it extracts timing information embedded in voltage-domain and converts it into digital codes. This achieves a higher time resolution while consuming less power.

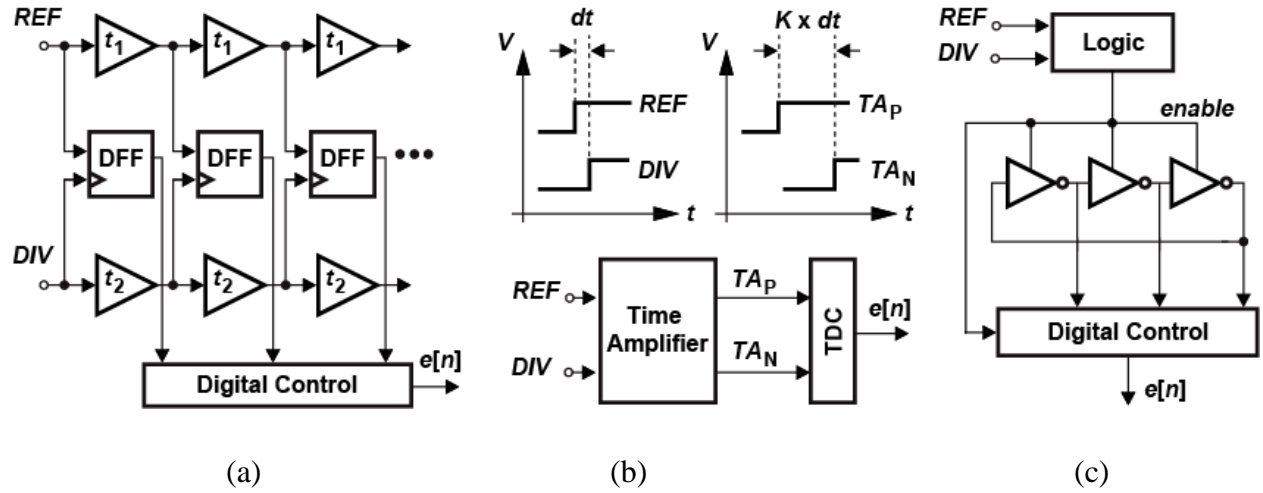


Figure 2.2: (a) Vernier delay line. (b) Time amplifier. (c) Gated-ring oscillator.

2.2. Sub-Sampling Digital PLL Architecture

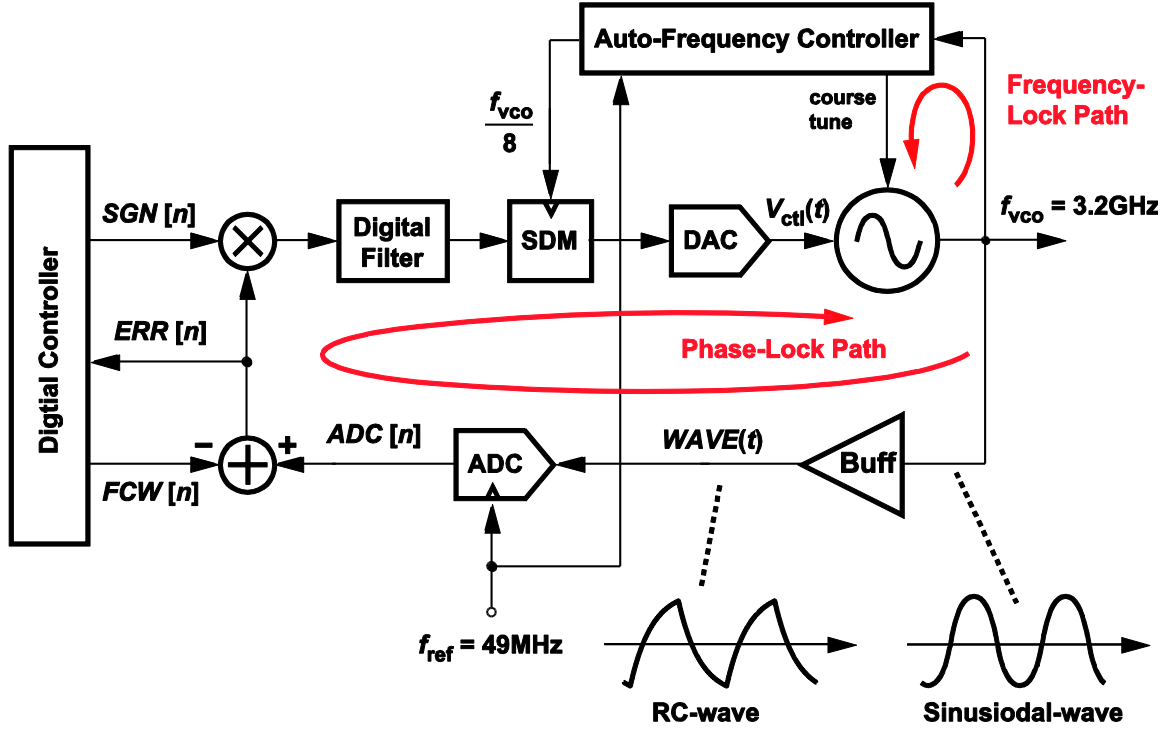


Figure 2.3: The proposed sub-sampling fractional- N digital PLL block diagram.

Fig. 2.3 shows the block diagram of the proposed digital PLL. It contains two paths: the first is the core phase lock path and the second is a frequency lock path that assists locking. During the locking process, the frequency lock path first brings the DCO near the targeted frequency. Then the phase lock path is enabled and continues to lock the DCO phase to the reference phase. Timing information is extracted by a SAR-ADC that directly samples the DCO buffer output voltage. In contrast to prior arts [6][7], where sampled voltage signals were sent to

Gm-Cell and analog LPF, here the voltage values are converted to digital codes and processed in the digital domain. Timing information is retained through the analog-to-digital conversion process. Neither multi-modulus dividers nor additional TDCs are required [8].

Fig. 2.4 shows the principle of the digital PLL integer- N operation. During phase locking, the phase lock path will adjust the DCO phase so that the sample instant of ADC happens at the negative slope side of $WAVE(t)$, and aligns with the zero crossing part. Thus when loop is locked, ADC output digital code equals 0, no update to the digital filter, and the DCO remains in its steady-state.

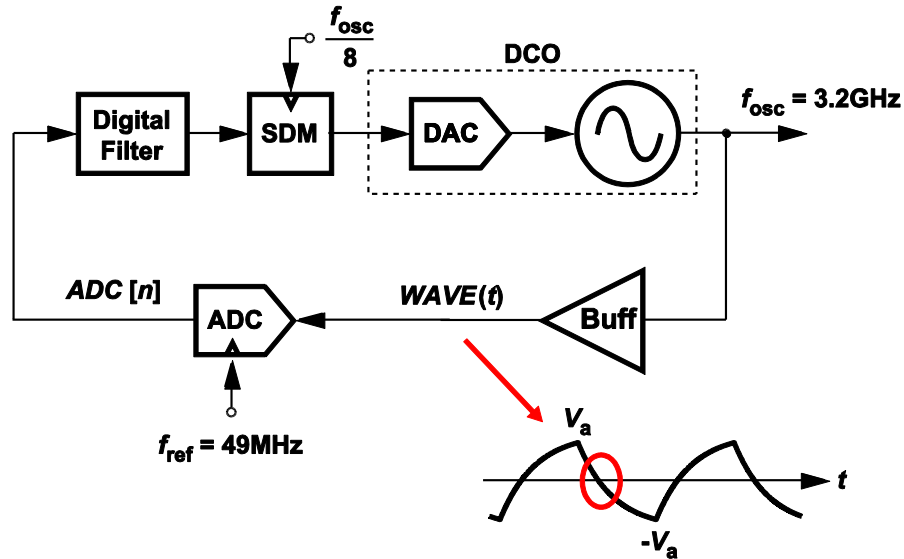


Figure 2.4: In integer- N operation the digital PLL samples at the zero crossing part of $WAVE(t)$.

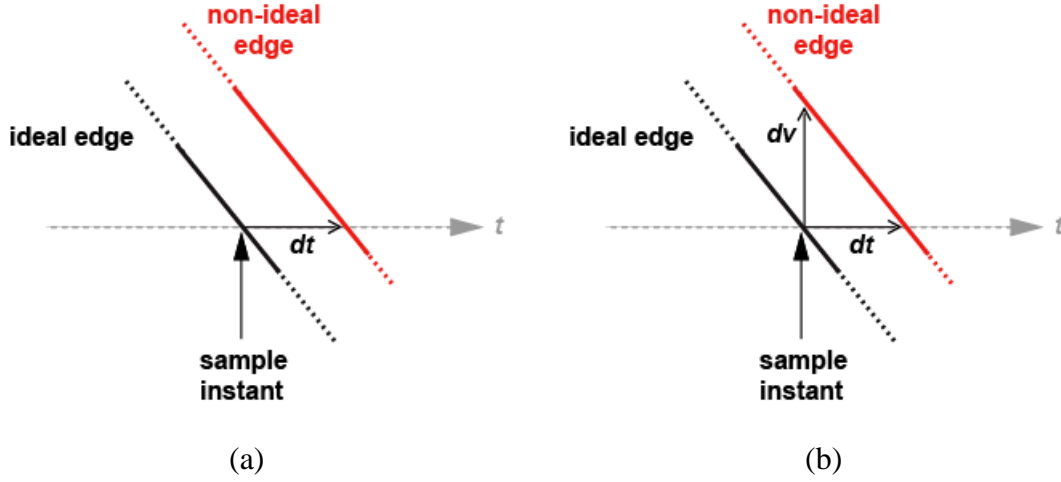


Figure 2.5: (a) Ideal crossing edge shifted by dt due to phase noise. (b) The ADC sample value changes by dv due to phase noise.

The proposed sub-sampling TDC uses SAR-ADC to convert the sampled input voltage into digital code. The equivalent time resolution of the TDC can be explain using Fig. 2.5. Assume $WAVE(t)$ contains phase noise and it causes the idea zero-crossing point to shift by dt . Then the ADC sampled voltage value would not be 0 but deviates by dv . If the voltage deviation is greater than an LSB of the ADC, the time shift due to phase noise can be detected. Therefore, the resolution of the sub-sampling time-to-digital conversion technique can be calculated as,

$$t_{res} = \frac{LSB_{adc}}{K_{slope}}, \quad (2.2)$$

where LSB_{adc} is the ADC LSB voltage value, K_{slope} represents the $WAVE(t)$ signal slope. For an example, if the ADC has an LSB of 4 mV and the input waveform has a slope of 2×10^9 (V/Sec), then the time resolution can be calculated as 2 psec. This transfers to an in-band phase noise of

-114 dBc/Hz, which is very good. From (2.2), we can also see that if the signal slope increases or the ADC LSB is reduced this enables smaller time shift to be detected, and thus improves the TDC time resolution.

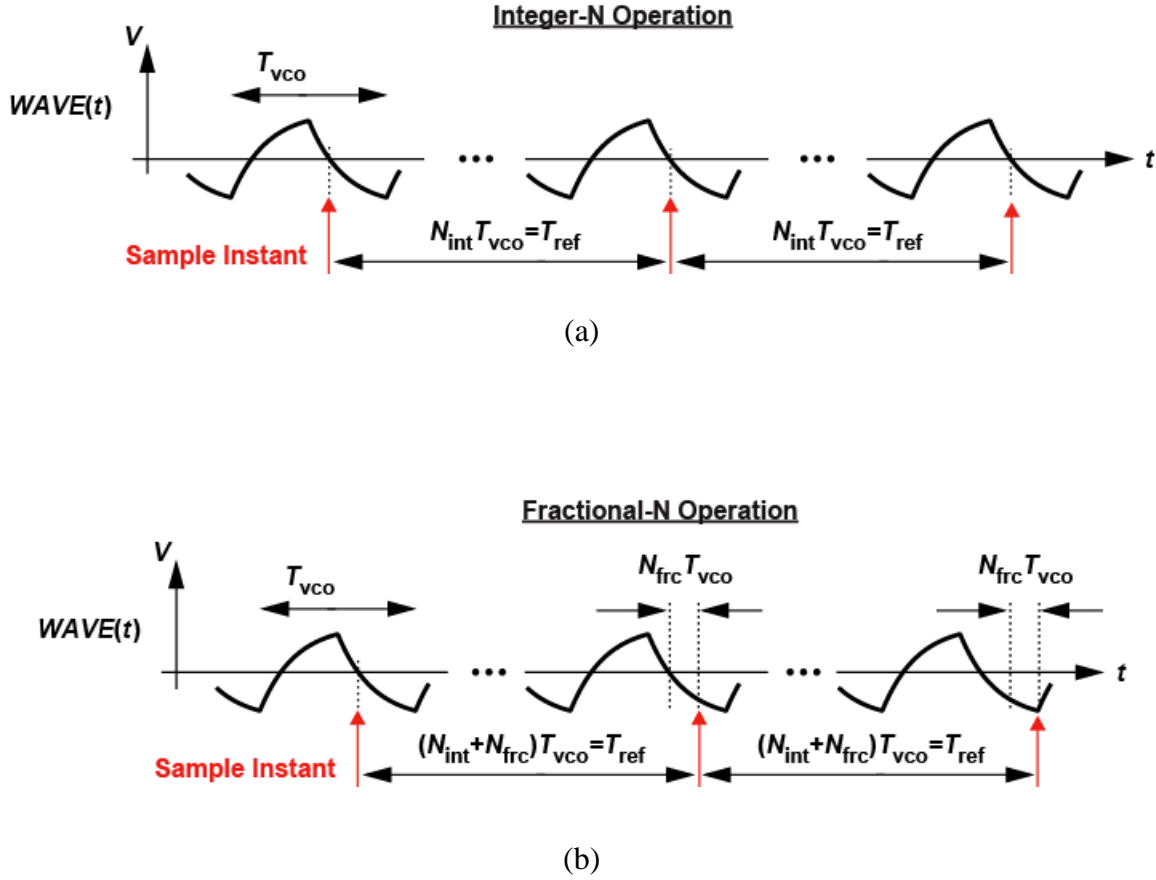


Figure 2.6: The difference between (a) integer- N operation, and (b) fractional- N operation.

2.3. Fractional- N Operation

The proposed digital PLL can also operate under fractional divisions. Fig. 2.6 (a) and (b) illustrates the difference between integer- N and fractional- N operations. As shown in Fig. 2.6(a),

when the digital PLL locks under integer- N mode the ADC sample instant happens at an integer number of the DCO period. N_{int} is the integer division and T_{osc} is the DCO period. Because $N_{int} \times T_{osc}$ equals to the reference clock period, therefore, when PLL settles the sampled value is a constant zero. In contrast, under fractional- N operation the ADC sample instant happens at a fractional number of the DCO period. As depicted in Fig. 2.6(b), the sample instant does not appear at the same location, but shifts by $N_{frac} \times T_{osc}$ from its last sample location. N_{frac} is the fractional division. This means even under locked condition. The ADC sample voltage would not be a constant value but varies.

In order to resolve the above issue, in analog sub-sampling fractional- N PLL a digital pulse-width modulator (DPWM) was employed to modulate REF clock edge position [7]. The DPWM acts like a DAC that converts digital information to analog edge position signal. As depicted in Fig. 2.7, the DPWM circuit adjusts the REF signal edge so that the sample instant happens at the zero-crossing edge. However, like all DAC circuits, it contains non-idealities such as gain and phase mismatch that causes INL and DNL degradation. In PLL these non-idealities result in spurious tone and noise folding at the output. It requires additional calibration scheme such as dynamic element matching and gain calibration to mitigate these non-idealities [7].

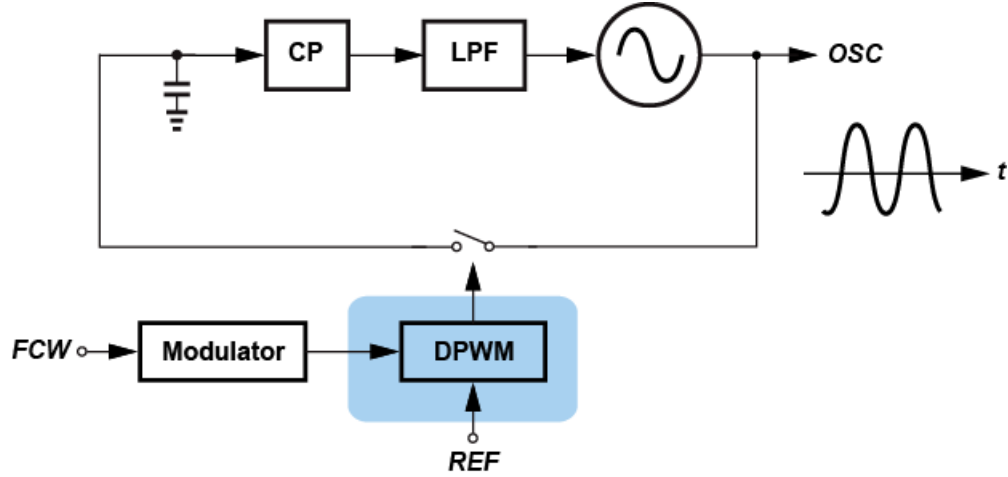


Figure 2.7: Adjusting the sampling edge using DPWM circuit [7].

In our work, instead of employing DPWM the sampling position variation issue is solved by digital circuit. Here explains our observation. The sub-sampling operation causes aliasing and signal folding effect. Since the input signal is high frequency signal around 3 GHz and the sample clock frequency is low frequency 50 MHz signal, the sampled output signal is folded back to the first Nyquist Zone. As shown in Fig. 2.8, the ADC sampled signal actually resembles the ADC input signal $WAVE(t)$. Further, since the high frequency signal waveform of a PLL is usually a known waveform, that is depending on the buffer circuit implementation it can be either sinusoidal, rectangular, or RC waveform. By taking advantage of this pre-knowledge of the high-frequency signal waveform it is possible to build a sub-sampling fractional- N digital PLL.

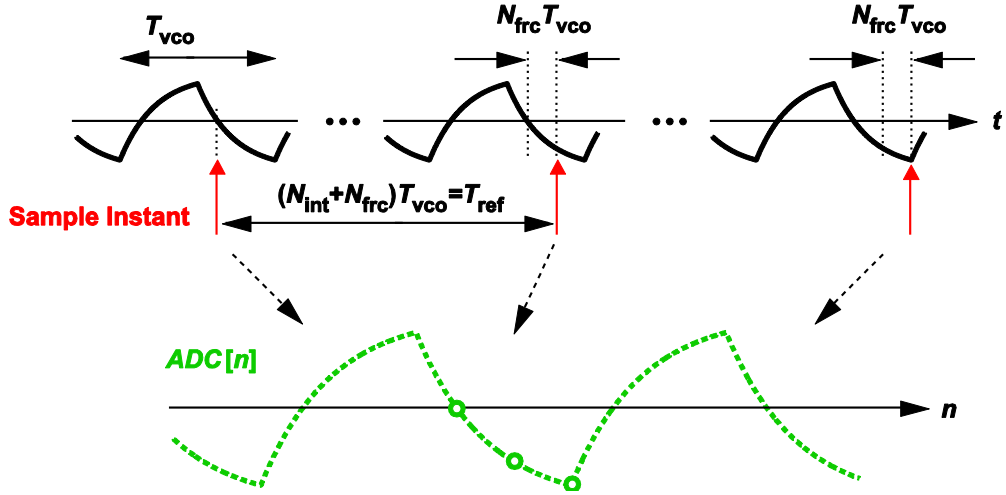


Figure 2.8: Aliasing and signal folding effect caused by sub-sampling operation.

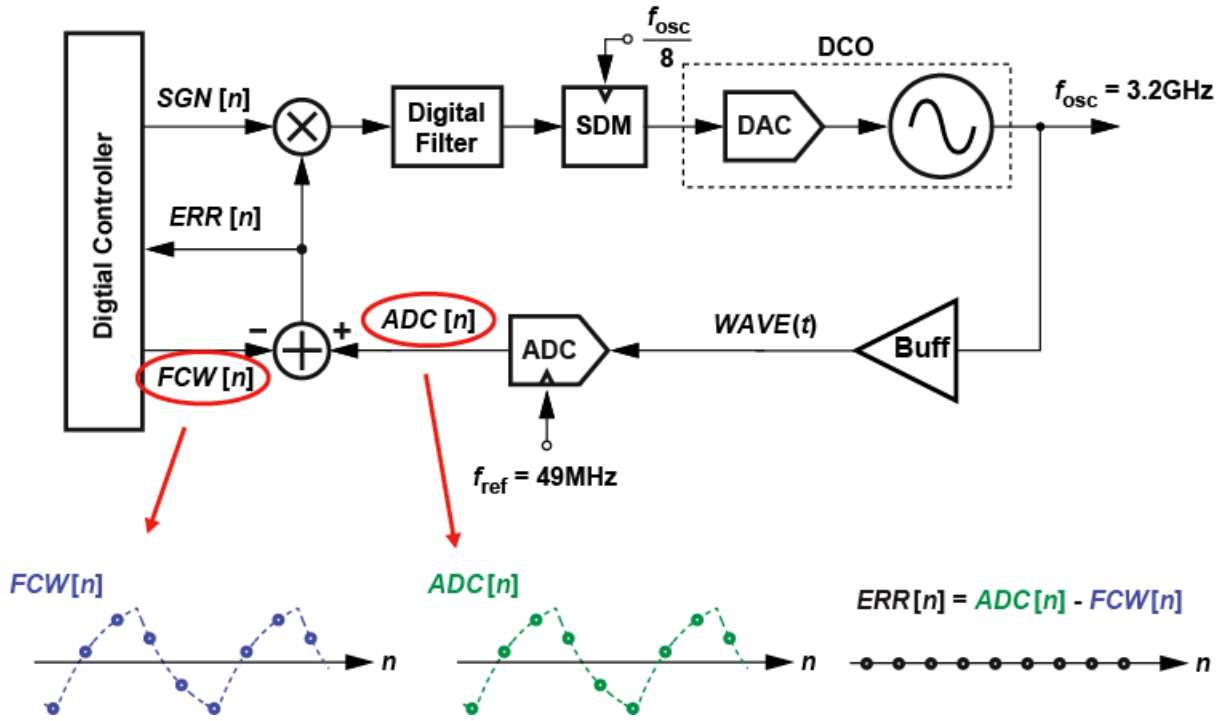


Figure 2.9: Fractional- N operation by calculating $FCW[n]$ in digital circuit.

As illustrated in Fig. 2.9, a digital controller circuit is implemented to calculate the folded

$WAVE(t)$ signal in digital domain. The calculated digital waveform is then fed into the loop through the frequency control word $FCW[n]$. As depicted, when the loop settles $FCW[n]$ will align itself with the folded $WAVE(t)$ signal and cancels out. If they perfectly match the error term $ERR[n]$ would be zero. Then there would be no update to the digital filter and DCO, and the digital PLL is locked.

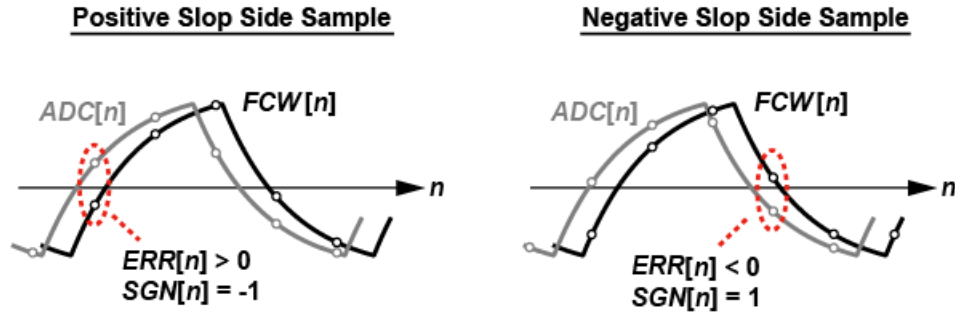


Figure 2.10: Principle of sign signal $SGN[n]$.

Moreover, to maintain a negative-feedback loop, a sign signal $SGN[n]$ is introduced to change the sign of $ERR[n]$. As indicated in Fig. 2.10, ADC's sample instant may happen on either the positive slope side or negative slope side of the folded and digitized $WAVE(t)$ signal. The sign signal $SGN[n]$ should be -1 when sampling on the positive slope side, or 1 on the other side. Since $ADC[n]$ aligns with $FCW[n]$ under the phase locked condition, $SGN[n]$ can be simply calculated from $FCW[n]$. In reality due to PVT variation it is not a trivial task to predict a $FCW[n]$

sequence that matches perfectly with the ADC sequence. This causes spurious tones at the PLL output. To deal with this non-ideality a calibration scheme is employed as explained in the next section.

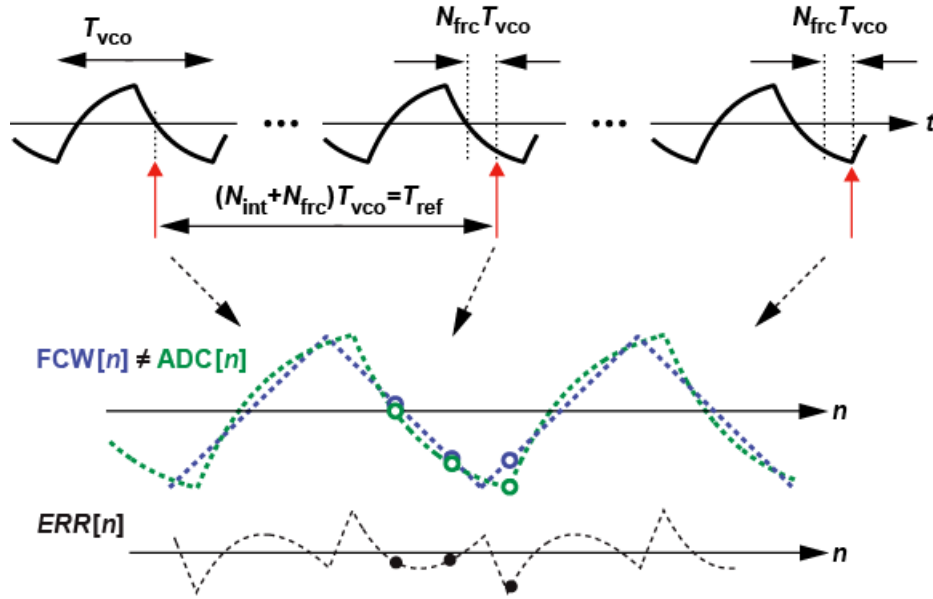


Figure 2.11: Mismatch between $FCW[n]$ and $ADC[n]$ causes non-zero $ERR[n]$ feedback.

2.4. Digital Background Calibration

Due to PVT variation it is not a trivial task to predict a FCW sequence that matches with the folded $WAVE(t)$ signal. If they don't match, the error term $ERR[n]$ would not be zero, as shown in Fig. 2.11. This creates spurious tones and noise at the PLL output. To deal with this non-ideality a background calibration scheme is employed to calibrate the $FCW[n]$ sequence to match with

the folded $WAVE(t)$ signal.

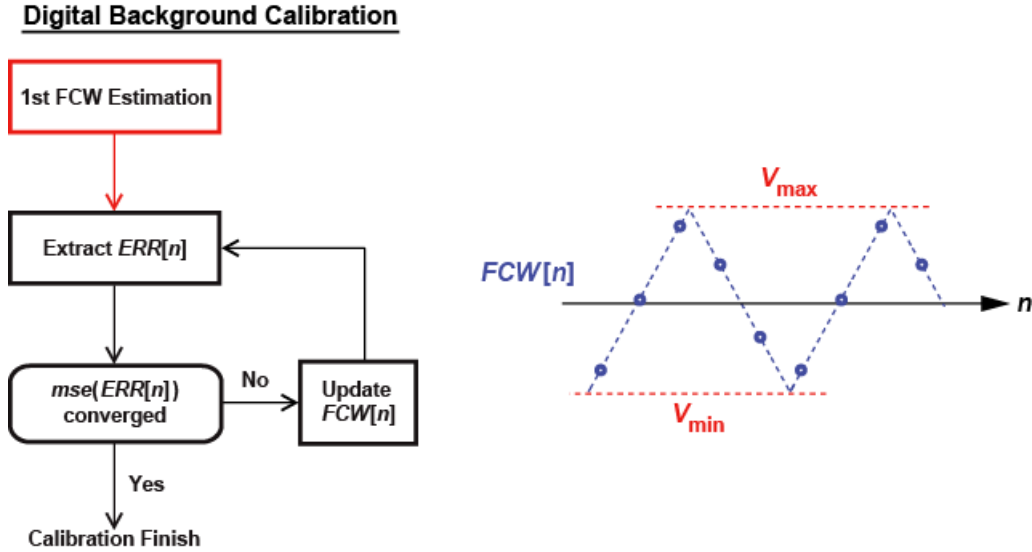


Figure 2.12: Use triangular wave as first estimated $FCW[n]$ sequence.

Fig. 2.12 shows the proposed digital background calibration scheme. At the first step, a triangular wave is generated as the first estimation of $FCW[n]$ sequence to lock the PLL at the targeted frequency. There are three parameters needed to generate the triangular waveform: the fractional division number N_{frac} (which is a known value), the maximum amplitude value V_{max} , and the minimum amplitude value V_{min} . While the N_{frac} is a known value, V_{max} and V_{min} are unknown values but can be easily extracted from the ADC output after the frequency lock path brings the DCO near the targeted frequency.

Digital Background Calibration

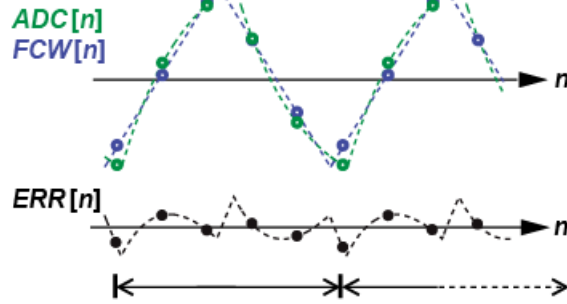
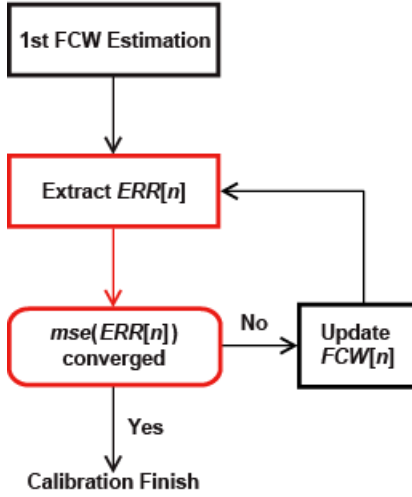


Figure 2.13: Extract the error term $ERR[n]$ and calculate its MSE.

Because the triangular wave sequence is just a coarse first estimation, in reality it would not match with the folded $WAVE(t)$ signal. This causes non-zero error term $ERR[n]$. Thus, after the PLL is locked by the triangular FCW sequence we start to extract the error term, calculate the mean-square error (MSE), and compare it with a predefined threshold value. As illustrated in Fig. 2.13, if the MSE is greater than the threshold, the calibration will correct and update the $FCW[n]$ sequence. On the other hand, if the MSE is less than the threshold, the calibration is stopped. To be noted here, because the folded and digitized $WAVE(t)$ sequence and $FCW[n]$ are periodic signals, the error term pattern also repeats, this causes spurious tones and noise at the PLL output.

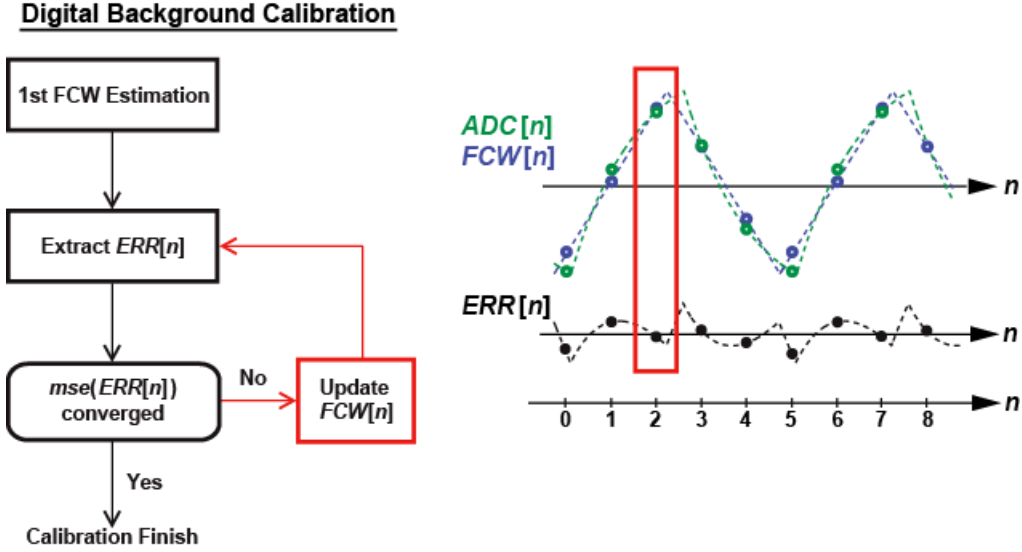


Figure 2.14.: Digital background calibration scheme.

Fig. 2.14 depicts how the $FCW[n]$ sequence is updated. Take the signals at the second index for an example, where $ERR[2]$ equals to $ADC[2]$ minus $FCW_{OLD}[2]$. $ADC[2]$ is the unknown, and $FCW_{OLD}[2]$ is known. Your goal is to calculate a $FCW_{NEW}[2]$ that matches with $ADC[2]$. The subscripts OLD and NEW are added here to emphasize the $FCW[2]$ before and after update. Having to know the value of $ERR[2]$; $FCW_{NEW}[2]$ can be calculated by adding up the old $FCW_{OLD}[2]$ with $ERR[2]$. In practice, we average the error term before adding it to $FCW_{OLD}[2]$. After the $FCW[n]$ sequence is updated, the extraction of $ERR[n]$ term and the calculation of MSE continues until it converges. All of these calibration steps happen at background without disturbing the normal operation of the digital PLL.

2.5. Mathematical Model and Behavioral Simulation Results

In order to help understand the system behavior of the proposed digital PLL a time-domain mathematical model is derived. This gives us more design insights on how each individual circuit parameter affect the loop dynamics such as BW, phase margin, and noise performance. Furthermore, a behavioral model including the digital PLL and digital calibration circuit are implemented in Cppsim simulation tool. This enables us to run transient simulations to observe the PLL operation in real time.

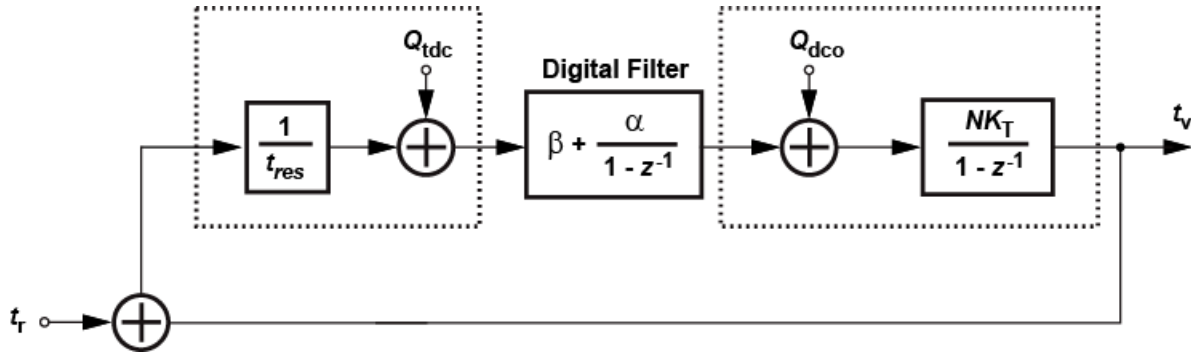


Figure 2.15: Discrete-time time-domain mathematical model.

2.5.1. Sub-sampling digital PLL time-domain mathematical model

Fig. 2.15 shows the digital PLL discrete-time time-domain model [9]. T_{ref} is the reference clock period and K_T is the DCO gain. In order to simplify the analysis we apply the following linearizing approximation

$$1 - z^{-1} = 1 - (\cos(2\pi T_{ref} f) - j \sin(2\pi T_{ref} f)) \approx j 2\pi f T_{ref} = s T_{ref} . \quad (2.3)$$

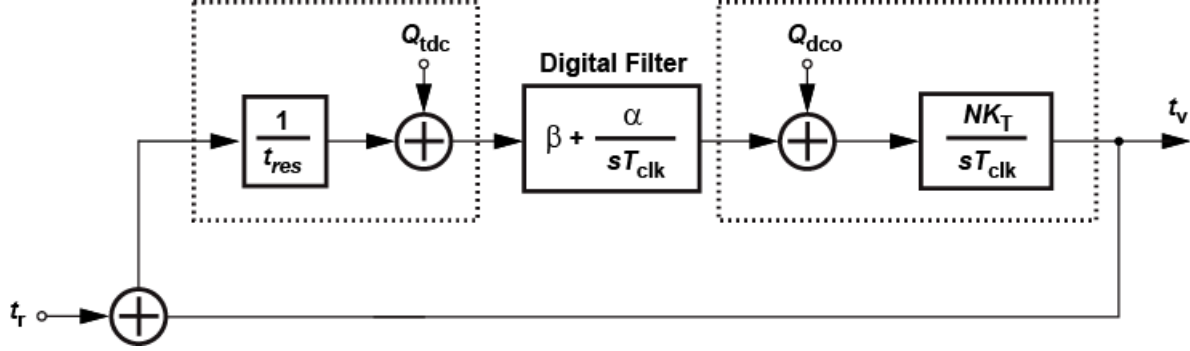


Figure 2.16: Linearized time-domain mathematical model.

Therefore, the mathematical model in Fig. 2.15 can be redrawn as Fig. 2.16. By using the linearized model the open-loop transfer function can be derived as

$$A(s) = \frac{1}{t_{res}} \left(\frac{\alpha + \beta s T_{ref}}{s T_{ref}} \right) \frac{N K_T}{s T_{ref}} = \frac{1}{t_{res}} \frac{N K_T}{s T_{ref}} \beta \left(1 + \frac{\alpha}{\beta s T_{ref}} \right) , \quad (2.4)$$

and the closed-loop transfer function can be calculated as

$$H(s) = \frac{1 + A(s)}{A(s)} . \quad (2.5)$$

Thus given the reference frequency, target BW, and target phase margin the parameters α , β , and

f_z can be derived as,

$$\begin{aligned} \beta &= \frac{1}{t_{res}} \frac{N K_T}{2\pi T_{ref}} \frac{1}{f_{BW}} \\ \alpha &= 2\pi T_{ref} \beta f_z \\ f_z &= \frac{f_{BW}}{\tan(PM)} \end{aligned} \quad (2.6)$$

2.5.2. CPPsim behavioral model and simulation results

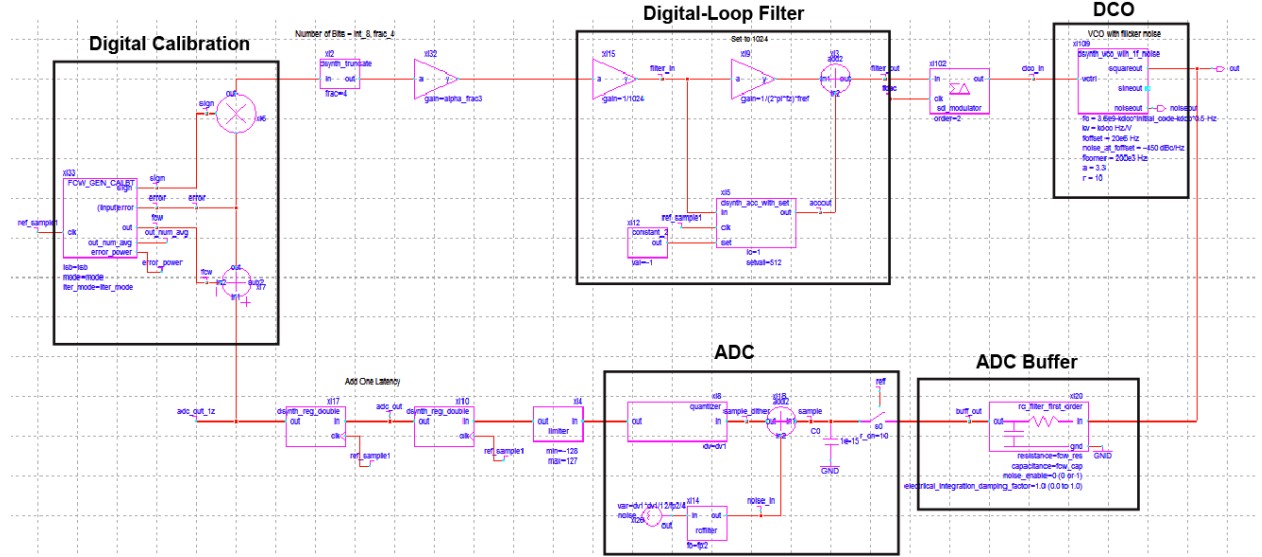


Figure 2.17: CPPsim behavioral model.

Fig. 2.17 shows the sub-sampling fractional- N digital PLL behavioral model built in CPPsim.

The most important building blocks are marked in the figure, which includes the ADC, ADC

buffer, digital calibration circuit, digital-loop filter, and DCO. Fig. 2.18 plots the calculation and

simulation results of the behavioral model with the PLL operating under integer- N mode. The

simulation results match with the calculation results verifying the proposed sub-sampling TDC

technique. Furthermore, the case with fractional- N operation and digital calibration technique

enabled is shown in Fig. 2.19. The calibration reduces fractional spurious more than 15 dB,

which verifies the proposed calibration scheme functionality.

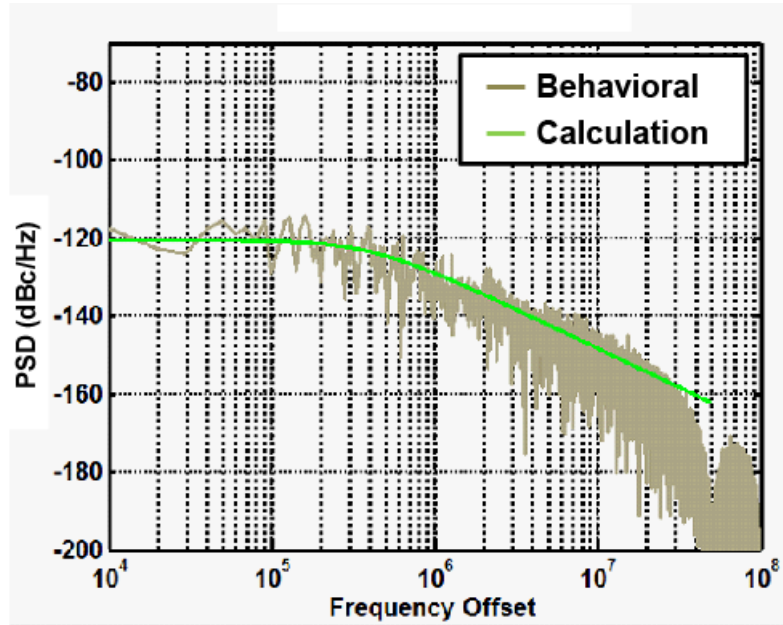


Figure 2.18: Integer- N mode calculation and simulation results.

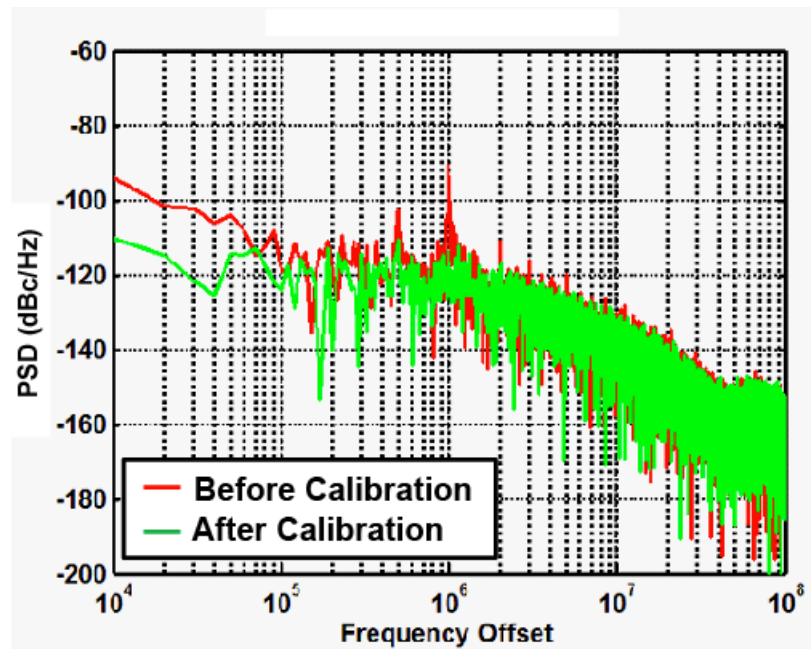


Figure 2.19: Fractional- N mode simulation results.

2.6. Circuit Design and Implementation

This section describes the circuit design details of the most critical building blocks including the SAR-ADC, ADC buffer, and class-C DCO.

2.6.1. SAR-ADC

The core of the sub-sampling digital PLL is the SAR-ADC, Fig. 2.20 shows the block diagram.

Although it is used to convert voltage signal to digital codes its rule is to serve as the sub-sampling TDC. In our work, an asynchronous SAR-ADC architecture is employed due to its high energy efficiency and short conversion latency. The SAR-ADC has 10 physical bits with a sampling clock frequency equal to the reference clock frequency, which is 49 MHz.

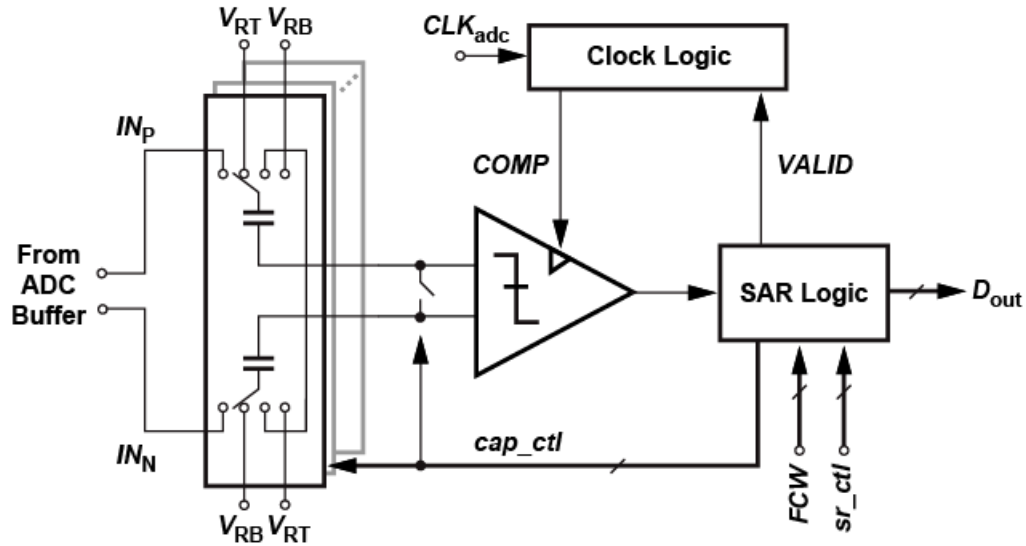


Figure 2.20: Asynchronous SAR-ADC block diagram.

This SAR-ADC can operate under normal mode and sub-ranging mode operation. For normal mode the SAR comparator compares 10 times to resolve all 10bits. On the other hand the SAR-ADC can also operate in sub-ranging mode. Conventional sub-ranging ADC requires a coarse ADC to first resolve the MSBs. Here we can take advantage of the MSBs in $FCW[n]$ codes. This is because when the digital PLL is locked and the calibration is finished, $FCW[n]$ will match with $ADC[n]$, meaning the MSBs of the $ADC[n]$ is known and equals to the MSBs of $FCW[n]$. By running ADC in the sub-ranging mode, the number of comparisons between each of clock samples is reduced which saves ADC power consumption.

However, sub-ranging ADCs can have residue voltage over-range problem that saturates the consecutive comparison stages. Fig. 2.21 shows a residue plot of a 2-bit sub-ranging example. The 2-bit MSBs are directly taken from $FCW[n]$ code. In this example, the input voltage is 0.125 V but the 2-bit MSB codes are “01”. If the SAR-ADC switch capacitors DAC follow those MSB codes, this would generate a residue voltage of 0.1875V which saturate the remaining comparison stages. The nominal input voltage range of the remaining stage is +/- 0.125V. In conventional ADCs the over-range problem originates from the offset and gain mismatch between the coarse and fine ADCs. But in the proposed sub-sampling fractional- N digital PLL the case is different as explain in the following.

Note that the 2-bit MSB codes were extracted directly from $FCW[n]$, which matches with the folded $WAVE(t)$ signal. Therefore, it is the circuit noise that added onto the $WAVE(t)$ that causes mismatch between the MSB bits and the ADC output value. In other words, because we are using old MSB bits to predict the new MSB bits which contain additional noise, this causes the residue voltage over-range problem.

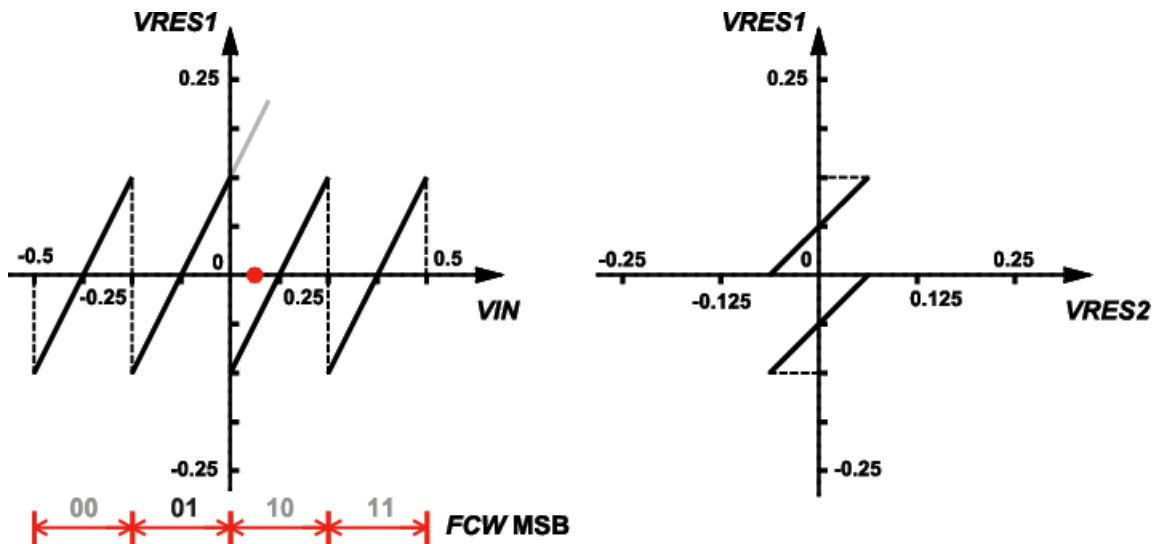


Figure 2.21: Residue voltage plot of 2-bit sub-ranging example.

This over-range problem can be solved by utilizing more MSB bits or so called redundant bits also taken from $FCW[n]$. As shown in Fig. 2.22, previously we use 2-bit MSB to do sub-ranging which saves 2 comparisons. Now by utilizing 2 more redundant bits, a total of 4 MSBs are used. Note the number of comparisons that are saved is still 2. From the example in

Fig. 2.22, the input value is slightly greater than 0.125 V. Ideally the MSBs should be 100, due to input noise it becomes 011. But because of the redundant bit the residue voltage would not over-range and would not saturate the remaining comparison stages.

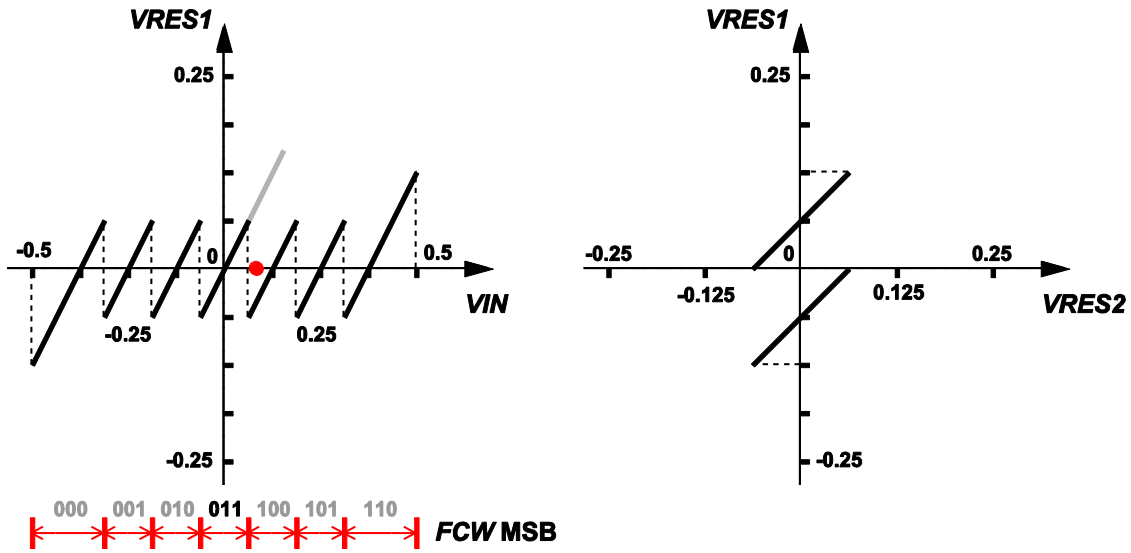


Figure 2.22: 2-bit sub-ranging example with redundant bits used to avoid over-range problem.

2.6.2. ADC Buffer

As mentioned in previous sections, $FCW[n]$ can be calculated based on the prior content of $WAVE(t)$. This requires $WAVE(t)$ to be well-defined. To cope with this challenge, a buffer is inserted after DCO to shape the waveform that enters ADC. The buffer schematic is shown in Fig. 2.23. It is designed to simply turn the DCO sinusoidal signal into RC charging and discharging waveforms. The advantage of such waveforms is the slope remaining steep at every instant as

compared to sinusoidal signals. This is important because the slope affects the time resolution. Note that the operating frequency is around 3 GHz; it is sufficiently high to prevent RC-waveform from entering the flat region. A 5 bit resistor array is used to control the waveform amplitude. To save power, the buffer is 20% duty-cycled. Although, due to process variations, the buffer output may not be an ideal RC-waveform and the calculated $FCW[n]$ may not fully cancel out with $ADC[n]$. This can be taken care of by our proposed digital background calibration scheme.

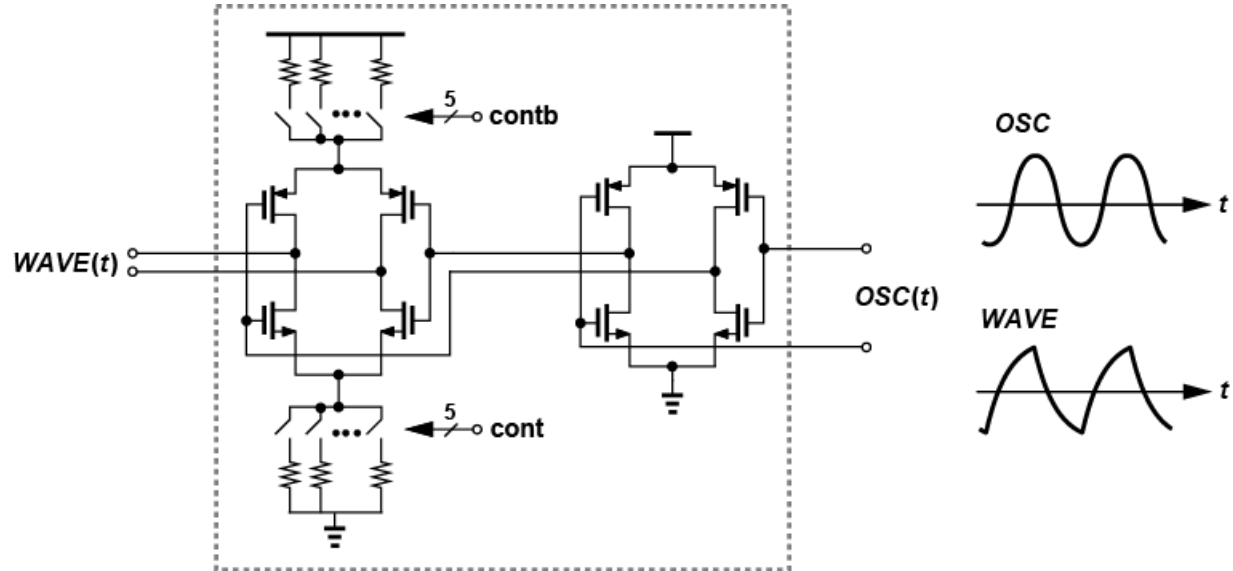


Figure 2.23: Schematic of ADC input buffer.

2.6.3. Class-C DCO and DAC circuit

Fig. 2.24 shows the diagram of the class-C DCO including DAC. The DCO is a LC-based oscillator. To reduce phase noise and power consumption, the cross-coupled pair transistors are biased in class-C [10]. A 10-bit coarse tuning switch capacitor bank controls DCO center frequency from 2.6 GHz to 3.9 GHz. For finer tuning, there is an 8-bit resistor ladder DAC that controls varactor voltage. From simulation, it is observed that the phase lock path can lock the digital PLL only if DCO frequency is near the targeted frequency within 2500 ppm. This task is accomplished by the frequency lock path. An auto-frequency controller (AFC) calculates the DCO frequency based on the 49 MHz reference signal. Further, the AFC controls the DCO center frequency by adjusting the coarse tuning switch capacitors in the DCO.

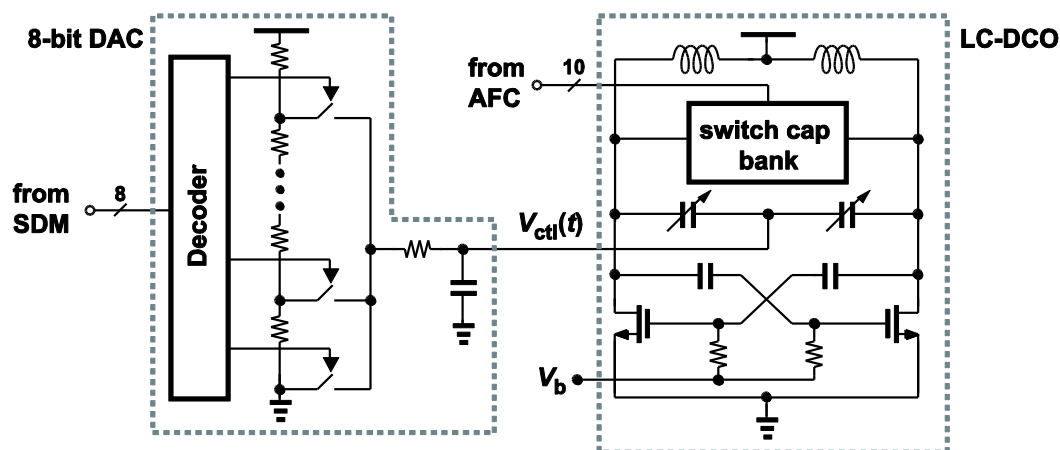


Figure 2.24: Schematic of the class-C DCO including DAC.

2.7. Measurement Results

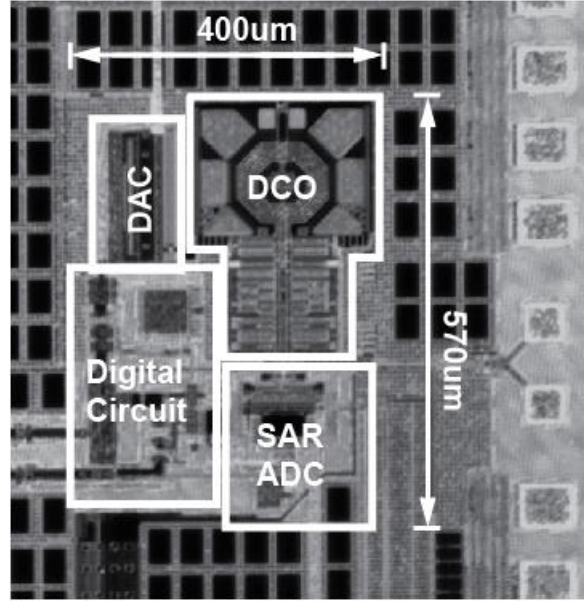


Figure 2.25: Chip micrograph.

The sub-sampling fractional- N digital PLL has been fabricated in TSMC 65nm CMOS technology. Fig. 2.25 shows the chip micrograph. The core area is $400 \times 570 \text{ um}^2$. To characterize the phase noise performance of the proposed sub-sampling digital PLL the output phase noise is measured using Keysight N9020A MXA signal analyzer. Fig. 2.26 and Fig. 2.27 show the measurement results. When the PLL operates under integer- N mode at 3.83 GHz, the measured in-band phase noise is -111.05 dBc/Hz at 100 kHz offset frequency. The rms jitter integrated from 1 kHz to 100 MHz is 229.6 fs. When the digital PLL operates under fractional- N

mode at 2.68 GHz the in-band phase noise is -110.57 dBc/Hz at 100 kHz offset frequency. The rms jitter integrated from 1 kHz to 100 MHz is 226 fs.

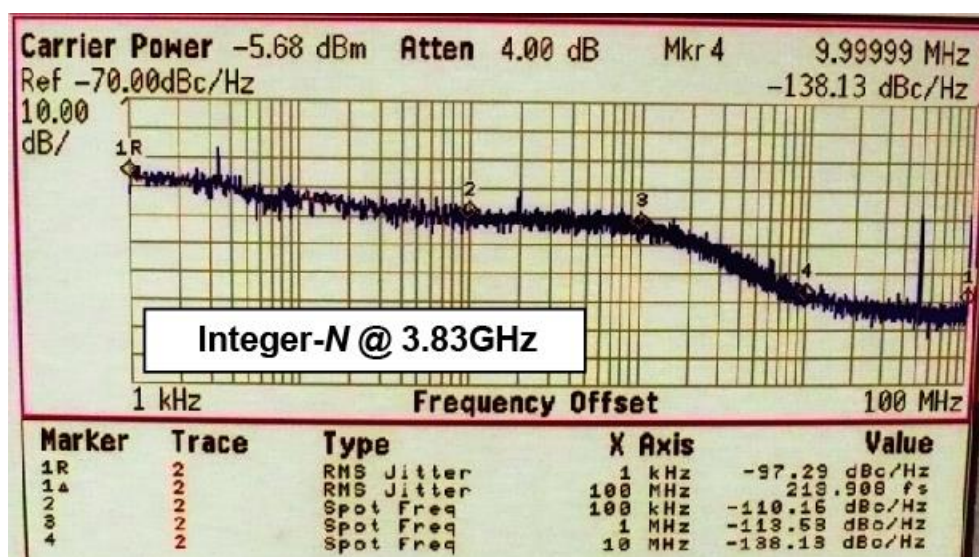


Figure 2.26: Measured PLL phase noise performance under integer- N operation.

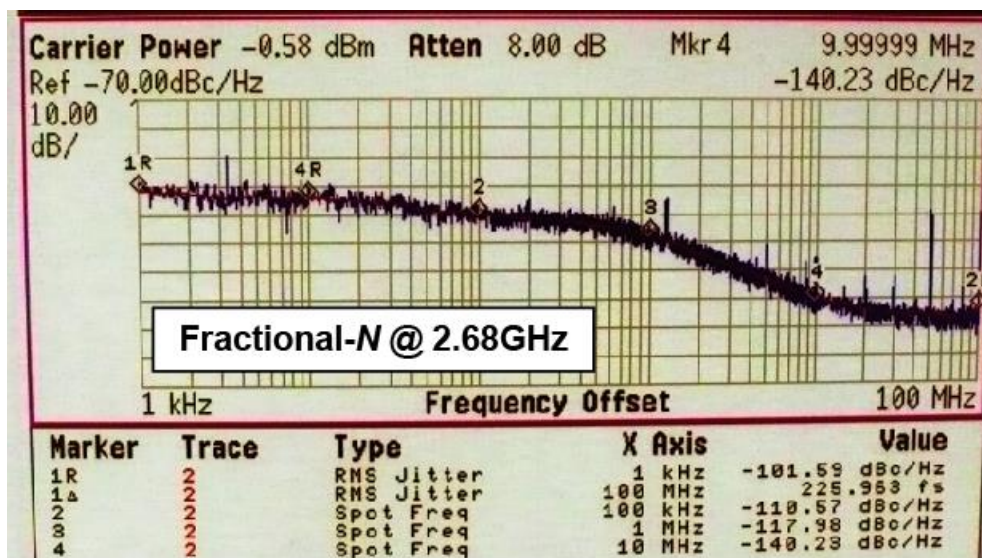


Figure 2.27: Measured PLL phase noise performance under fractional- N operation.

To verify the digital background calibration scheme the PLL output spectrum before and after calibration are measured. As shown in Fig. 2.28 is the spectrum when triangular wave $FCW[n]$ sequence is applied and the DCO is locked at the targeted frequency. Before calibration the fractional- N spur level is at -46.9 dBc. The result after running digital background calibration is shown in Fig. 2.29. The fractional spurs level is improved by 16.2 dB to -63.1 dBc. This validates the proposed calibration scheme successfully matches $FCW[n]$ sequence to the ADC output codes. Moreover, Fig. 2.30 plots the $ERR[n]$ MSE convergence curve.

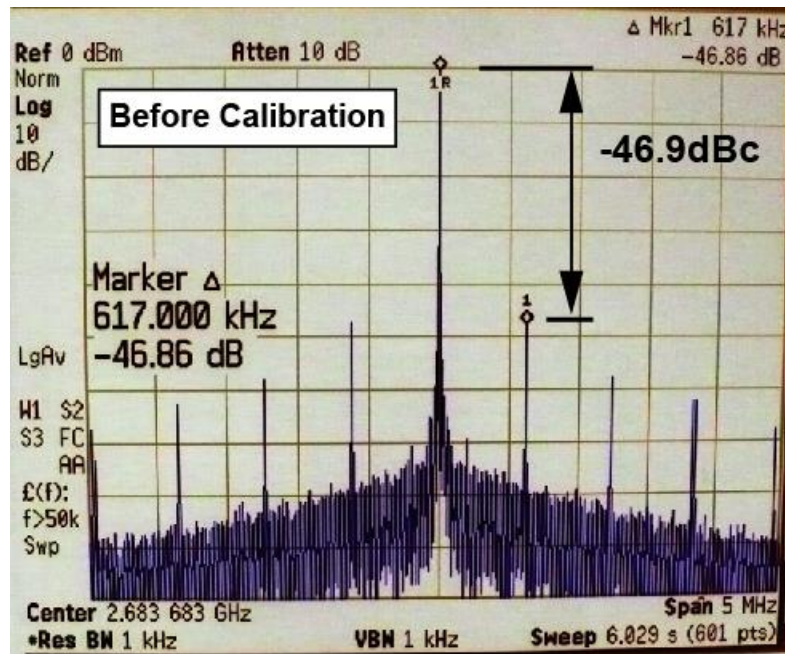


Figure 2.28: Measured PLL output spectrum before calibration.

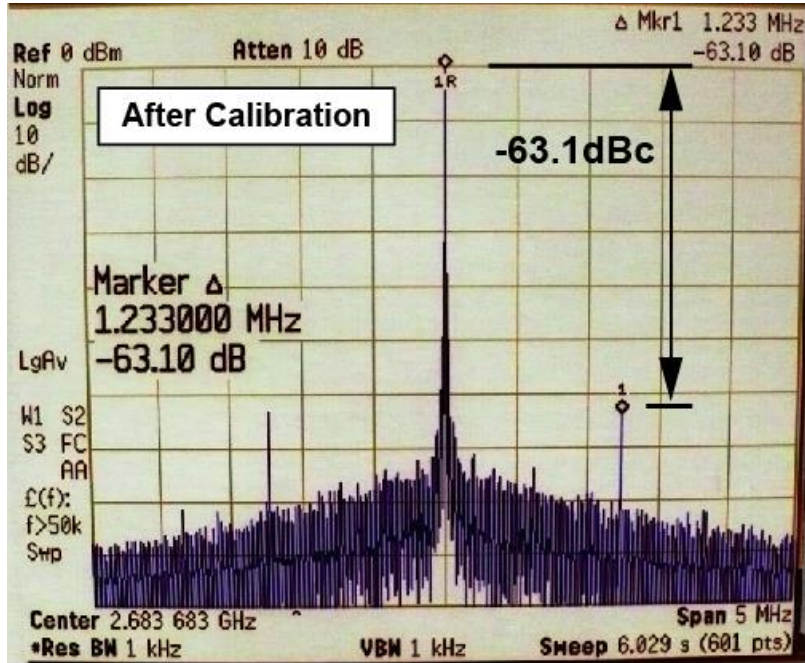


Figure 2.29: Measured PLL output spectrum after calibration.

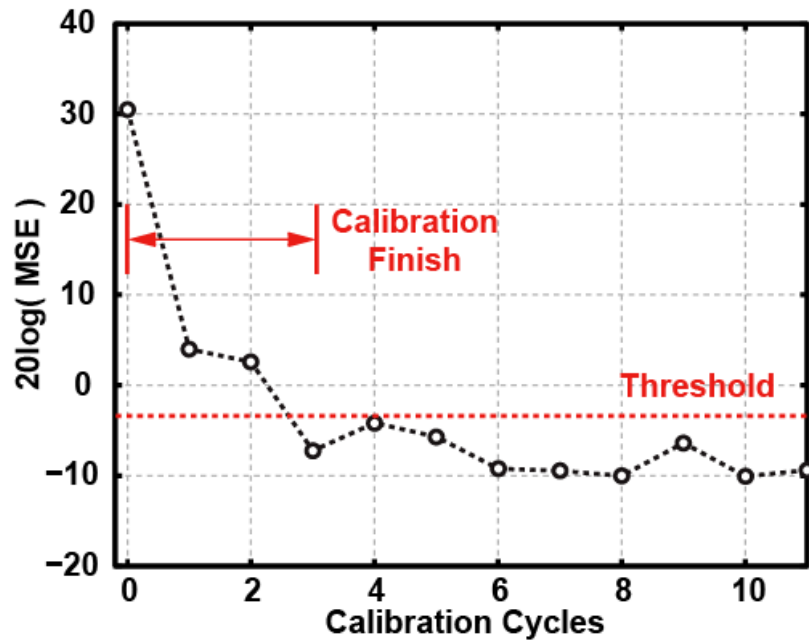


Figure 2.30: $ERR[n]$ MSE convergence curve.

In order to verify that using triangular wave as the first estimation sequence for $FCW[n]$ can lock the digital PLL to the targeted frequency, we have manually applied amplitude error and offset error on the triangular waveform and observed the PLL locking condition. Measurement results show that given amplitude and offset error the PLL still settles to the targeted frequency. Further, as shown in Fig. 2.31 and Fig. 2.32 after applying the digital background calibration the mismatch between $FCW[n]$ and ADC output can be greatly reduced, resulting in a fractional spur level less than -60 dBc for all cases.

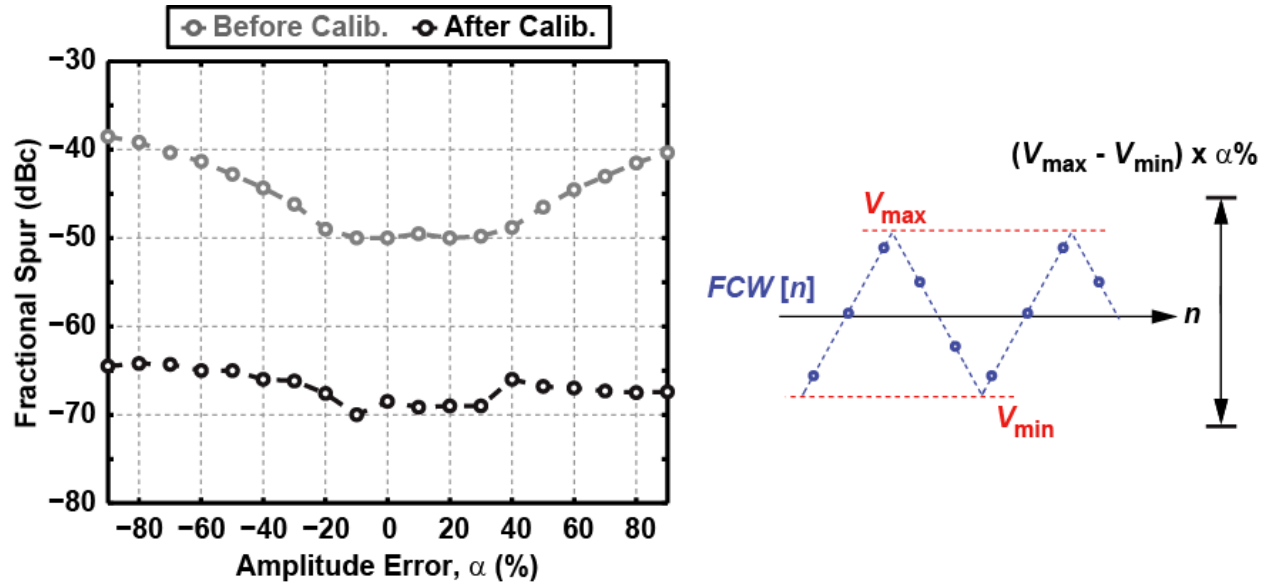


Figure 2.31: Measured PLL output spurs level before and after calibration with gain error applied on the first estimate triangular waveform.

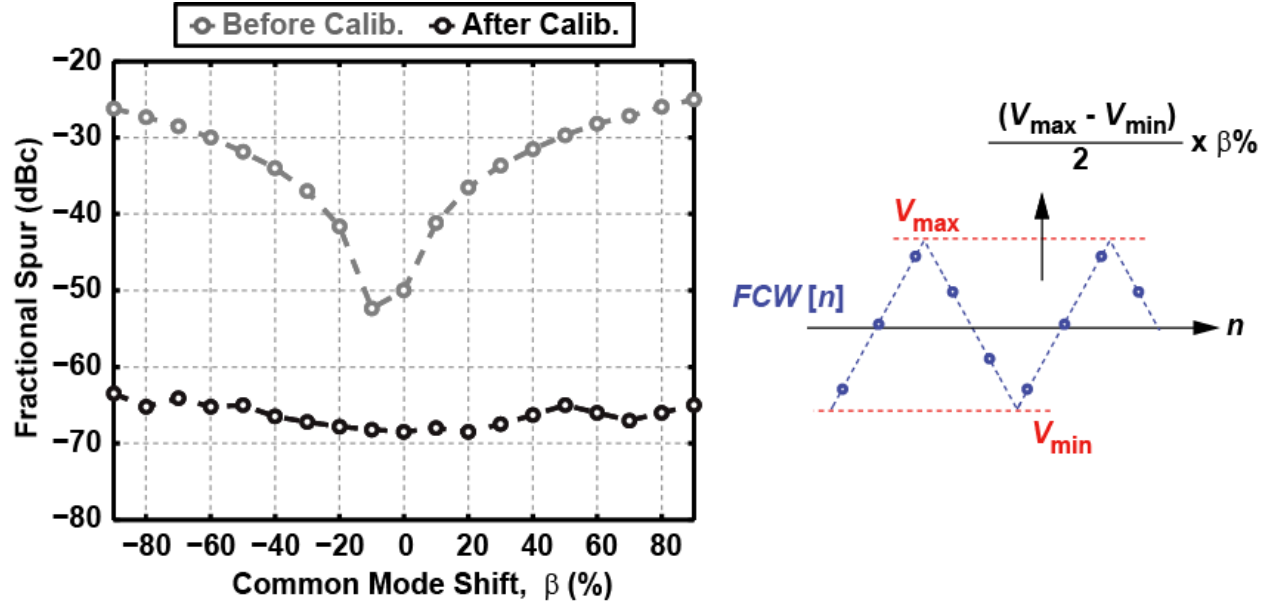


Figure 2.32: Measured PLL output spurs level before and after calibration with amplitude error on the first estimate triangular waveform.

Table 2.1 summarizes the performance of the proposed digital PLL and compared with state-of-the art fractional- N digital PLLs. The output frequency achieve 40 % tuning range from 2.6 to 3.9 GHz. The supply voltage is 1 V. Total power consumption is 11.5 mW, including 5 mW for the DCO, 6 mW for the DCO buffer and SAR-ADC, and 0.5 mW for digital circuits. Figure 2.33 shows the FoM results compared to other state-of-the art digital PLLs. The FoM of the proposed sub-sampling based fractional- N digital PLL achieves -241.8 dB.

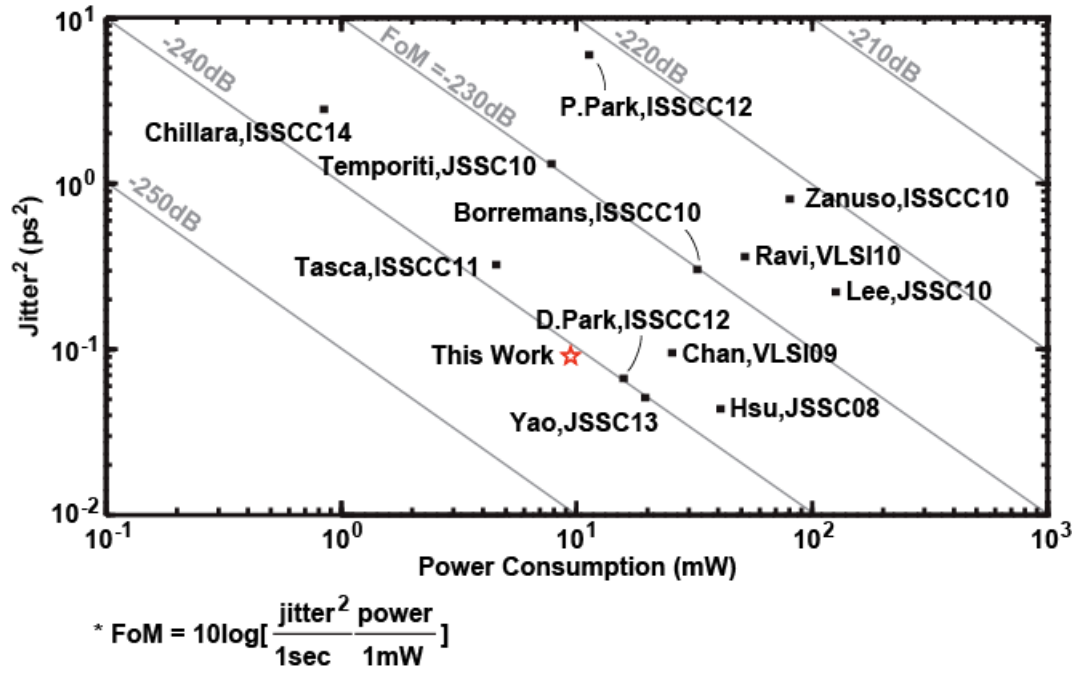


Figure 2.33: Figure of merit.

2.8. Conclusions

In summary, sub-sampling SAR-ADC is used in the proposed architecture to convert the timing information embedded in analog voltage signals into digital codes. Under fractional- N operation, the background digital calibration scheme is adopted to reduce the mismatch between $FCW[n]$ and the folded and digitized $WAVE(t)$ signal. Fractional spurs can be suppressed more than 15 dB after calibration. Consequently, the fractional- N digital PLL can yield low noise with low power consumption.

Table 2.1: Performance summary and comparison to other fractional- N digital PLLs.

	C.M.Hsu [ISSCC '08]	M.Lee [JSSC '09]	D.Tasca [ISSCC '11]	C.W.Yao [JSSC '13]	V.K.Chillara [ISSCC '14]	This work
Reference (MHz)	50	25	40	52	32	49.15
Output (GHz)	3.67	1.68	2.9 - 4.0	2.8 - 3.2	2.1 - 2.7	2.6 - 3.9
Tunning Range (%)	N/A	N/A	31.9	13.3	25	40
RMS Jitter (fsec)	204 - 300 (1K~40MHz)	495 (1K~40MHz)	400 - 560 (3K~30MHz)	230 (1K~40MHz)	1710 (1K~100MHz)	226-240 (1K~100MHz)
Bandwidth (KHz)	500	400	312	950	200	700
PN at 1MHz (dBc/Hz)	-120	-120	-110	-114.4	-109	-118
In-band PN (dBc/Hz)	-101.8	-117	-102	-111.6	-90	-110.6
Ref supr (dBc)	-65	-54	-72	-75	-70	-60
Fractional Spur (dBc)	-42	-48	-42	-55	-38	-62.3
Power (mW)	46.7	110	4.5	17	0.86	11.5
FoM (dB)	-233.8	-225.7	-238.3	-240.4	-236	-241.8
Area (mm ²)	0.95	2.25	0.22	0.62	0.2	0.23
Process (nm)	130	90	65	180	40	65

Chapter 3

Digital PLL for Phase Noise Cancellation in Ring-Oscillator Based Quadrature Receivers

3.1. Introduction

Ring Oscillators (ROs) have gained increasing interest for applications in radio receivers due to their small area, wide tuning range, and multiphase output. However, compared to LC oscillators, ROs have higher phase noise and higher sensitivity to supply noise that may seriously deteriorate the received signal during the mixer down-conversion process. As shown in Fig. 3.1, there are two effects. The first one occurs where the noisy LO signal mixes with the wanted signal. As illustrated in Fig. 3.1(a), this leads to LO close-in phase noise falling inside the signal bandwidth (BW) and degrading the signal-to-noise ratio (SNR). The second mechanism is the reciprocal mixing of interference signal. In addition to the wanted signal, in a wireless environment various interference signals can also enter the receiver front-end. As depicted in Fig. 3.1(b), the LO signal mixes with the interference signal and causes phase noise to fold back on top of the wanted signal and thus degrades the SNR. While the reciprocal mixing noise can be cancelled using the symmetrical property of phase noise [12][13], cancelling the close-in phase noise

remains a challenge. The main focus of this work is to alleviate the close-in phase noise effect in RO-based quadrature receivers.

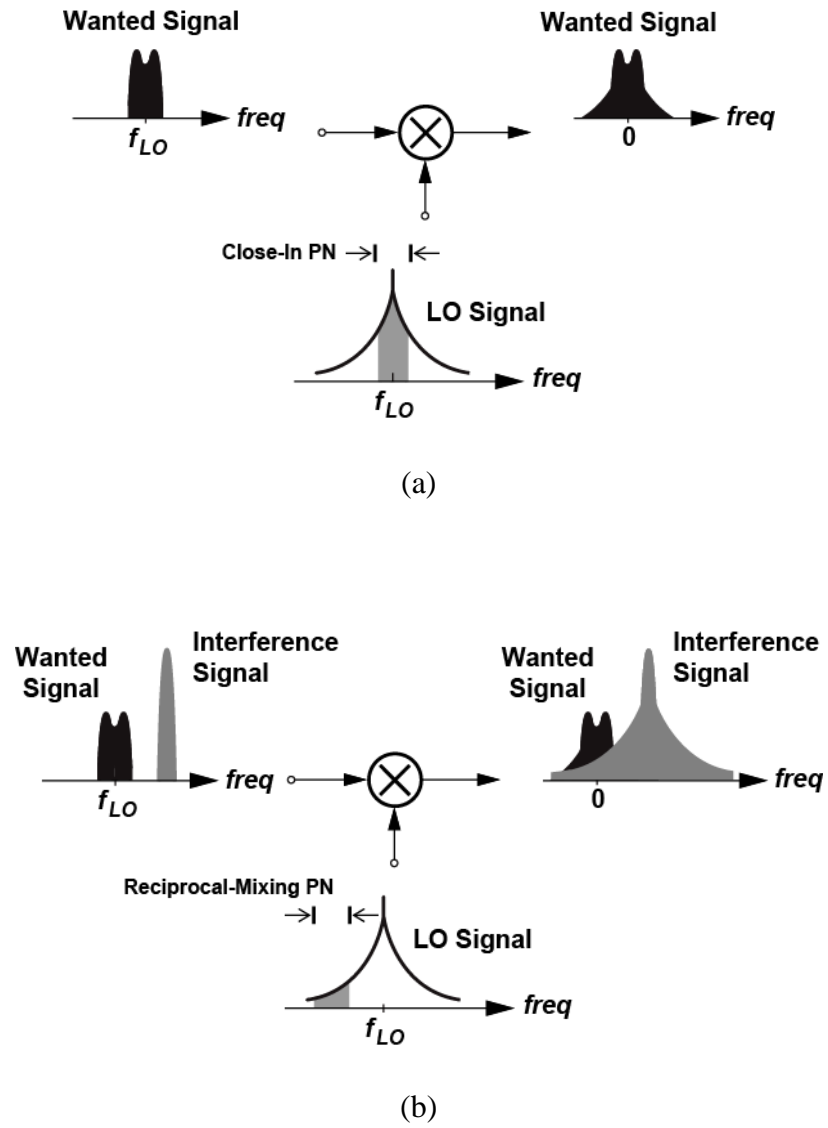


Figure 3.1: The effect of LO phase noise in radio receivers. (a) Close-in phase noise effect. (b)

Reciprocal-mixing phase noise effect.

Increasing PLL BW can reduce the close-in phase noise of ROs [14]. Since voltage-controlled oscillator (VCO) phase noise is high-pass filtered when appearing at the PLL output, larger BW results in more suppression on RO close-in phase noise. This relationship holds true for digitally-controlled oscillators (DCO) in digital PLLs as well. However, the BW is limited to $1/10$ of the reference frequency (F_{REF}) in conventional type-II PLLs due to stability concerns. Moreover, increasing PLL BW causes larger spurs at PLL output. The reason is because spurious tones mostly originate from the non-linear behavior of either the time-to-digital converter (TDC) in digital PLLs, or phase-frequency detector (PFD) and charge pump (CP) circuits in analog PLLs. These spurs encounter a low-passed transfer function at the PLL output. Therefore, increasing the BW inevitably reduces the suppression on these spurious tones. A delay-discriminator-based technique was proposed to cancel RO phase noise [15]. However, the technique showed limited jitter (or IPN) improvement, and is conducted in the analog domain. To circumvent the aforementioned constraints, here we present a digital phase noise cancellation technique capable of reducing both RO close-in and supply-induced phase noise for RO-based quadrature receivers.

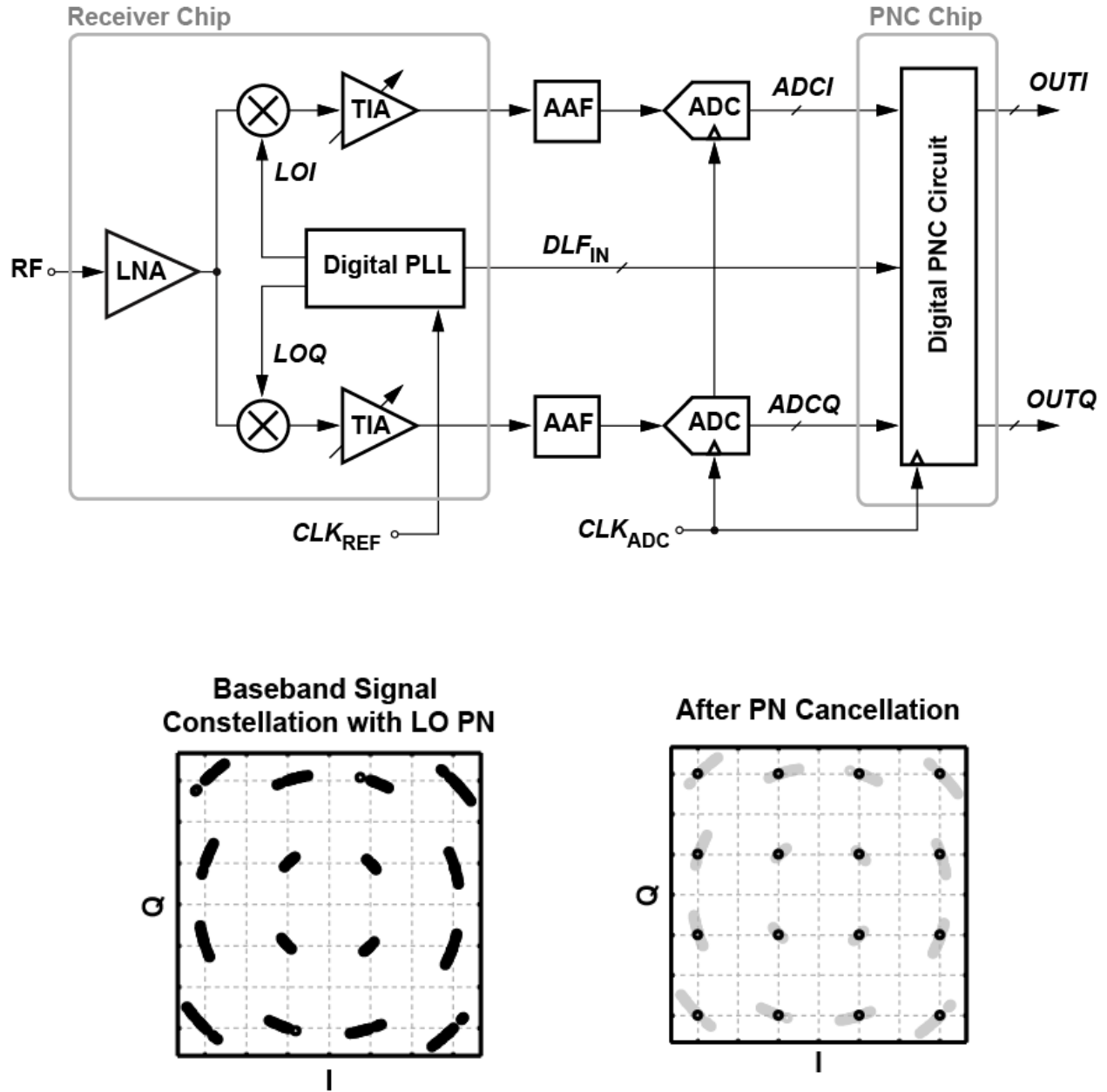


Figure 3.2: The proposed PNC quadrature receiver system diagram and the baseband signal constellation affected by LO phase noise.

3.2. Phase-Noise Cancelling Receiver Architecture

Fig. 3.2 shows the block diagram of the proposed phase-noise-cancelling (PNC) receiver [16].

The receiver system employs a common-gate low-noise amplifier (LNA) followed by quadrature passive mixers. The mixers outputs are buffered by transimpedance amplifiers (TIAs), which convert current to voltage. The following anti-aliasing filters (AAFs) reject the out-of-channel noise, and after that a pair of ADCs quantizes the analog quadrature baseband signals into digital.

Furthermore, the digitized signals are applied to the digital PNC circuit for phase noise cancellation. The quadrature LO signals are generated from the digital PLL which employs a RO as the DCO. The idea behind the proposed PNC technique can be explained by observing the effect of LO close-in phase noise in time domain. Assume the input RF signal has the form of $RF(t) = I(t)\cos \phi_{LO}t + Q(t)\sin(\phi_{LO}t)$, where $I(t)$ and $Q(t)$ are the analog quadrature baseband signals. The RF frequency is ϕ_{LO} . The quadrature LO signals can be written as $LOI(t) = \cos(\phi_{LO}t + \phi_{LO}(t))$ and $LOQ(t) = \sin(\phi_{LO}t + \phi_{LO}(t))$, where $\phi_{LO}(t)$ is the LO phase noise term. After down conversion and digitization through the I/Q mixers and ADCs, the baseband signal in complex form can be expressed as

$$BB[n] = V_a (I[n] + jQ[n])\exp(j\phi_{LO}[n]), \quad (3.1)$$

where V_a denotes the signal amplitude. $I[n]$ and $Q[n]$ are the digitized quadrature baseband signals, and $\phi_{LO}[n]$ is the digitized LO phase noise. As shown in (3.1), the wanted signal is

multiplied by a phase noise term which causes random rotation on the constellation (Fig. 3.2). In order to restore the deteriorated baseband signal, we can first find a replica version of the phase noise information (e.g. $\phi_{LO}[n]$) and further apply a complex multiplication of $\exp(-j\phi_{LO}[n])$ with $BB[n]$. In the proposed PNC technique this replica phase noise information is extracted from the digital PLL, and then used to counteract the random rotation in the digital PNC circuit.

In contrary to research in the past which concentrates more on reducing phase noise from a PLL circuitry perspective, this work tackles the problem from a system level point of view. Moreover, the proposed PNC technique is not limited to RO-based digital PLL but can be applied to LC-based digital PLL as well. The advantage of the technique is that now the loop BW is no longer under the restriction to be increased to suppress DCO phase noise but has more freedom to be designed for other purposes, such as for allowing more suppression on spurious tones at PLL output. In wireless applications, it is important to reduce the level of spurious tones in the LO signal because the interference signal can mix with these spurs and get down-converted right on top of the wanted signal. Since interference signal usually has larger power compared to the wanted signal, the spurs level need to be much lower than the main LO tone. This requirement has motivated several research works to reduce PLL output spurs, such as linearization method, dithering method, and spurs cancellation technique [17]-[19]. A simple yet

efficient way is by decreasing the digital PLL BW. Although lower BW increases DCO close-in phase noise, this part of noise can be removed by our proposed PNC technique. Lower BW also slows down digital PLL settling behavior. Nonetheless, this can be resolved by switching to a larger BW when changing channel frequency. For digital PLLs another efficient method is to switch gear to type-I PLL for fast settling, and then switch back to type-II configuration after the loop settles [20].

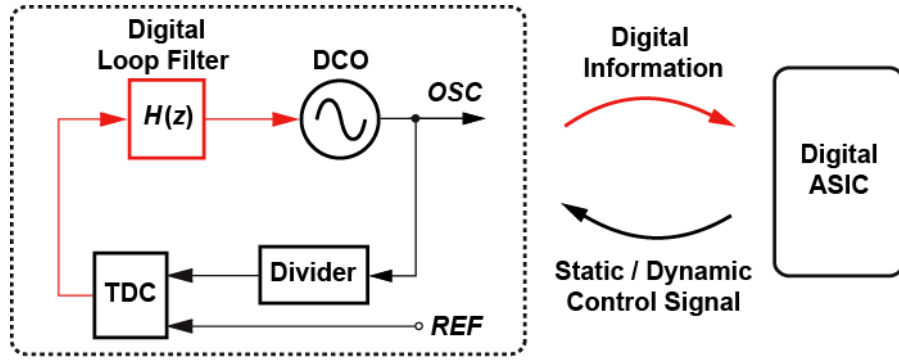


Figure 3.3: Digital PLL re-configurability.

3.3. Phase Noise Extraction

Digital PLLs are known for their compact digital loop filter (DLF) and re-configurability of loop parameters. The latter feature, as illustrated in Fig. 3.3, comes from the fact that the digital signal in the feedback loop can be readily accessed and analyzed by a digital ASIC to obtain information regarding the loop dynamics, including circuit impairments. The digital ASIC can

then send either static control signal back into the loop to change the parameters, or dynamic calibration signals to mitigate the impairments. This property has been utilized to alleviate several digital PLL non-idealities [3][21][22]. In this work, we take advantage of the re-configurability feature to extract RO phase noise. But instead of sending correction signal back to the digital PLL, our approach applies the extracted RO phase noise information to digital baseband and cancels the phase noise effect in digital domain. In order to understand how RO phase noise is obtained, we examine the noise transfer functions of the digital PLL. Fig. 3.4 shows a digital PLL discrete-time phase-domain model [23]. $H(z)$ is the DLF transfer function. The operation of the RO-based DCO is modeled as an integrator. K_{DCO} [Hz/s] and K_{TDC} [1/rad] are the gain of the DCO and TDC, respectively. $T_{REF} = (1 / F_{REF})$ [sec] is the period of the reference clock. The transfer functions for RO phase noise to PLL output and DLF input ($DLF_{IN}[n]$) can be derived as

$$\frac{\phi_{LO}(z)}{\phi_{RO}(z)} = \frac{1}{1 + A(z)}, \text{ and} \quad (3.2)$$

$$\frac{DLF_{IN}(z)}{\phi_{RO}(z)} = \frac{-K_{TDC}}{1 + A(z)}, \quad (3.3)$$

where $A(z) = 2\pi K_{TDC} K_{RO} H(z) / (1 - z^{-1})$ is the open-loop transfer function. As shown in Fig. 3.5(a), the RO phase noise encounters a high-passed transfer function at the PLL output and more interestingly it equals to the transfer function of RO phase noise to DLF input multiplied by $(-1 / K_{TDC})$. This means RO phase noise in $\phi_{LO}[n]$ can be eliminated in principle by subtracting it with

$(-DLF_{IN}[n] / K_{TDC})$. In addition, the phase noise extraction concept also applies to RO supply noise. Fluctuations on RO supply alters the oscillation frequency and further transfers into phase noise at the RO output. Since supply-induced phase noise and RO intrinsic phase noise are indistinguishable, both of them are captured in $DLF_{IN}[n]$ and cancelled through the noise subtraction process conducted in the digital PNC circuit.

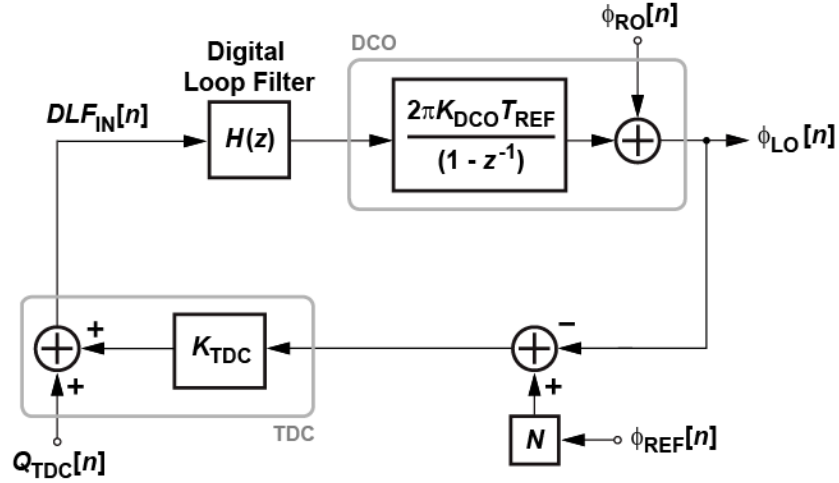


Figure 3.4: Digital PLL discrete-time phase-domain model.

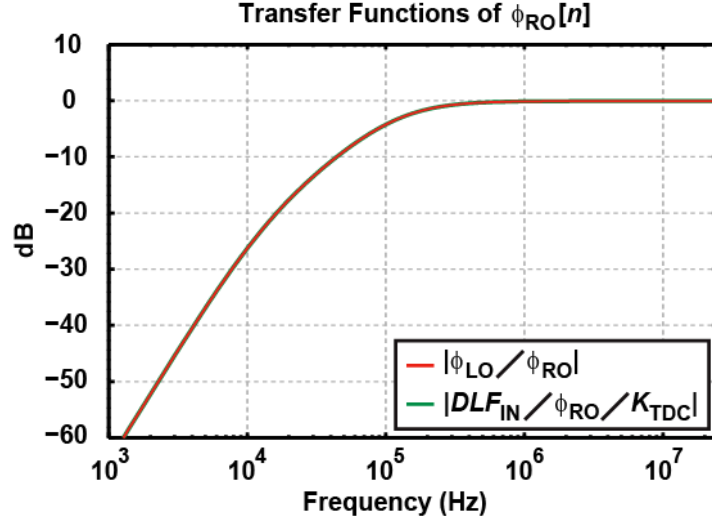
Other than RO phase noise, the TDC quantization noise ($Q_{TDC}[n]$) should also be carefully considered in digital PLL. The transfer functions of $Q_{TDC}[n]$ to PLL output and DLF input are derived below:

$$\frac{\phi_{LO}(z)}{Q_{TDC}(z)} = \frac{A(z)}{K_{TDC}(1 + A(z))}, \text{ and} \quad (3.4)$$

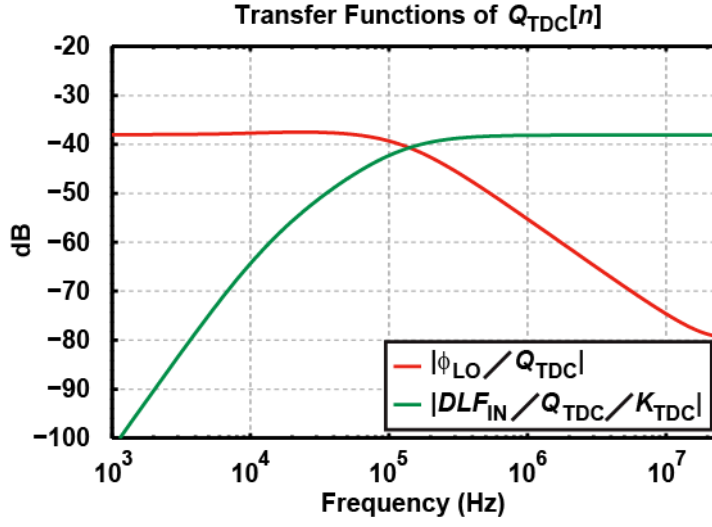
$$\frac{DLF_{IN}(z)}{Q_{TDC}(z)} = \frac{1}{1 + A(z)}. \quad (3.5)$$

As plotted in Fig. 3.5(b), the TDC quantization noise encounters a low-passed transfer function at the PLL output, but a high-passed transfer function at the DLF input.

Fig. 3.6 depicts the calculated digital PLL noise spectrum. It can be seen that the RO phase noise at PLL output and DLF input are the same. However, the TDC quantization noise shows a low-passed shape at PLL output but a high-passed shape at DLF input. This indicates that while utilizing $DLF_{IN}[n]$ for phase noise cancellation, RO phase noise can be removed but TDC quantization noise still remains. For this reason, the sub-sampling TDC technique proposed in [24] is employed here in our digital PLL. The sub-sampling TDC directly samples the high-frequency signal of the digital PLL via a SAR-ADC and extracts the timing information that is embedded in voltage domain. The technique achieves a high resolution time-to-digital conversion and thus low TDC noise. This helps to improve the overall noise performance after phase noise cancellation.

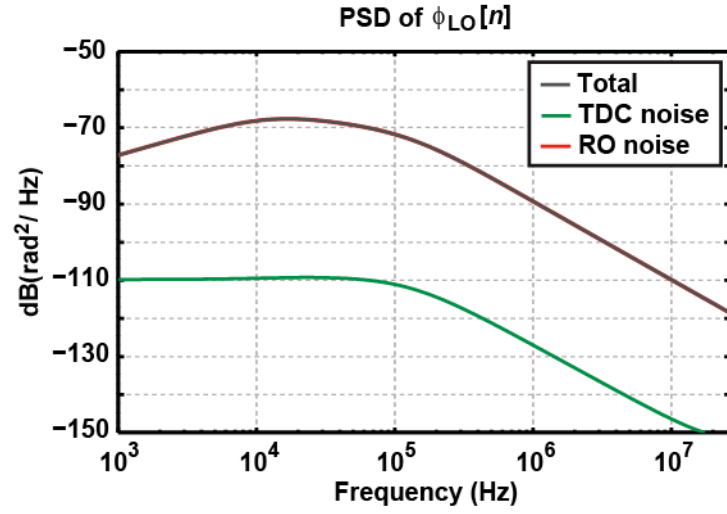


(a)

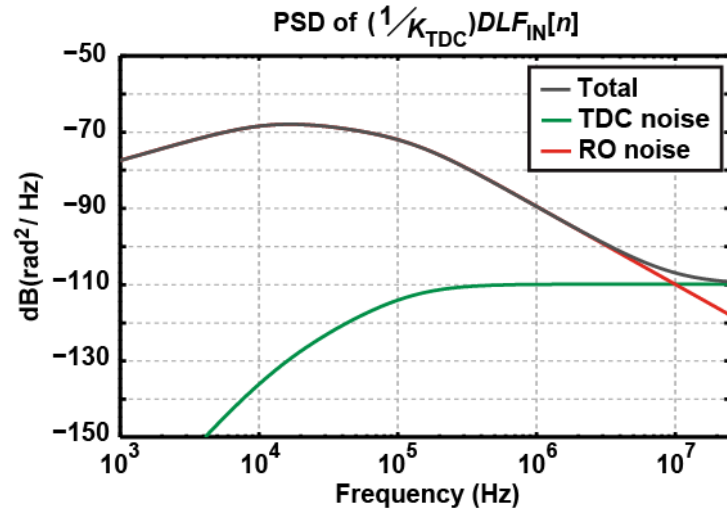


(b)

Figure 3.5: (a) Transfer functions of $\phi_{RO}[n]$ to PLL output and DLF input. (b) Transfer functions of $Q_{TDC}[n]$ to PLL output and DLF input.



(a)



(b)

Figure 3.6: (a) Calculated PSD of $\phi_{LO}[n]$. (b) Calculated PSD of $(DLF_{IN}[n] / K_{TDC})$.

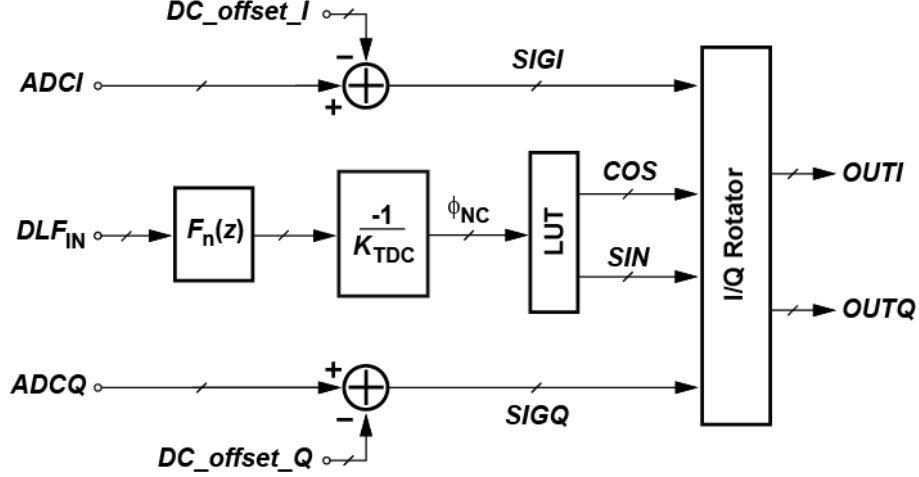


Figure 3.7: Digital PNC circuit block diagram.

3.4. Phase Noise Cancellation

Fig. 3.7 shows the block diagram of the digital PNC circuit. The input signal $DLF_{IN}[n]$ from digital PLL is first applied to a digital LPF $F_n(z)$ to filter out the high frequency part of TDC noise (see Fig. 3.6(b)). Afterwards, the digital LPF output is scaled by $(-1 / K_{TDC})$ and sent to the LUT to generate the digital sine and cosine signals. The I/Q rotator then calculates the complex multiplication of $(SIGI[n] + jSIGQ[n])$ and $(\cos(\phi_{NC}[n]) - j\sin(\phi_{NC}[n]))$, where $SIGI[n]$ and $SIGQ[n]$ are the digital baseband signal after DC offset removal. As illustrated in Fig. 3.8, the DC offsets on the baseband signal paths need to be removed for correct rotation. Further on, the time-domain expression for the output of the digital PNC circuit can be written as

$$out[n] = V_a' (I[n] + jQ[n]) \exp(j\phi_{LO_NC}[n]), \quad (3.6)$$

where $\phi_{LO_NC}[n] = (\phi_{LO}[n] - \phi_{NC}[n])$ is the remaining noise that affects the baseband signal. From

(3.2) and (3.3), the transfer function of $\phi_{RO}[n]$ to $\phi_{LO_NC}[n]$ can be derived as

$$\frac{\phi_{LO_NC}(z)}{\phi_{RO}(z)} = \frac{1}{1 + A(z)} - \frac{F_n(z)}{1 + A(z)}. \quad (3.7)$$

Similarly, the transfer function of $Q_{TDC}[n]$ to $\phi_{LO_NC}[n]$ can be obtained with the aid of (3.4) and

(3.5) as

$$\frac{\phi_{LO_NC}(z)}{Q_{TDC}(z)} = \frac{A(z)}{K_{TDC}(1 + A(z))} + \frac{F_n(z)}{K_{TDC}(1 + A(z))}. \quad (3.8)$$

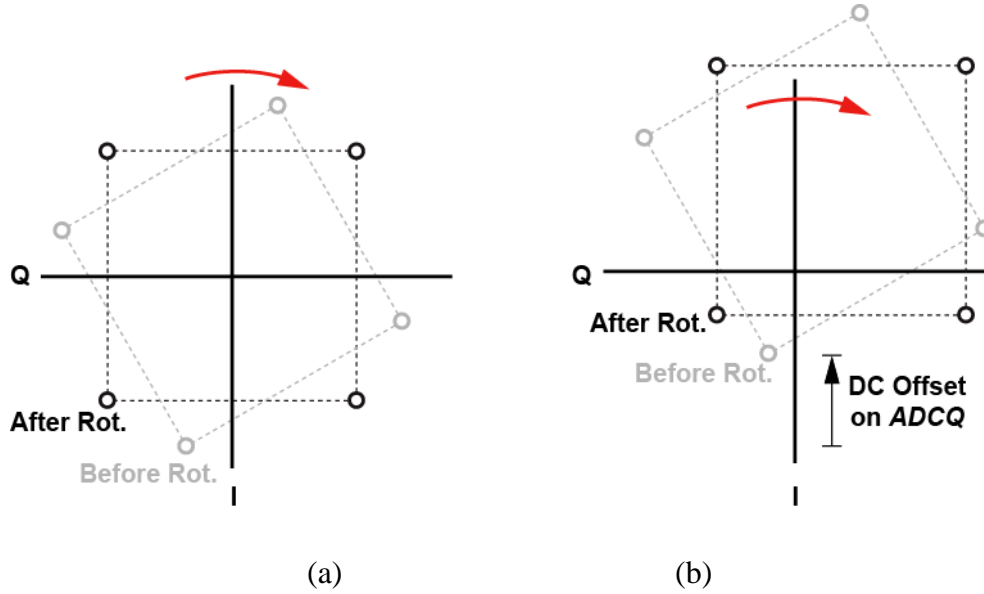


Figure 3.8: (a) Correct I/Q rotation without DC offset. (b) Incorrect I/Q rotation with DC offset

in $ADCQ[n]$.

Fig. 3.9 depicts the transfer functions of $\phi_{RO}[n]$ and $Q_{TDC}[n]$ to $\phi_{LO_NC}[n]$. Fig. 3.10 shows the calculated noise spectrum of $\phi_{LO_NC}[n]$. Compared to Fig. 3.6(a), it can be seen that the RO close-in phase noise is greatly reduced. The remaining noise is the TDC quantization noise and the residue of RO phase noise. Fig. 3.11 shows the impact of the $F_n(z)$ BW to the overall IPN. A small $F_n(z)$ low-pass corner reduces the TDC noise but increases the residue of RO phase noise after cancellation. This can be observed from (3.7), where the reduction of the second part results in less suppression on RO phase noise at high-frequency offsets and thus causes IPN to increase. On the other hand, a large $F_n(z)$ low-pass corner reduces the residue of RO phase noise but increases the TDC noise. From (3.8), it is the second part that increases, allowing more high-frequency TDC noise to appear in $\phi_{LO_NC}[n]$ and raising IPN again. In order to optimize the IPN after cancellation, $F_n(z)$ BW is set at the frequency where RO and TDC noise spectra intersect [25]. This renders both noise sources to have approximately equal contributions to IPN. In our case, the $F_n(z)$ BW is set at around 12 MHz.

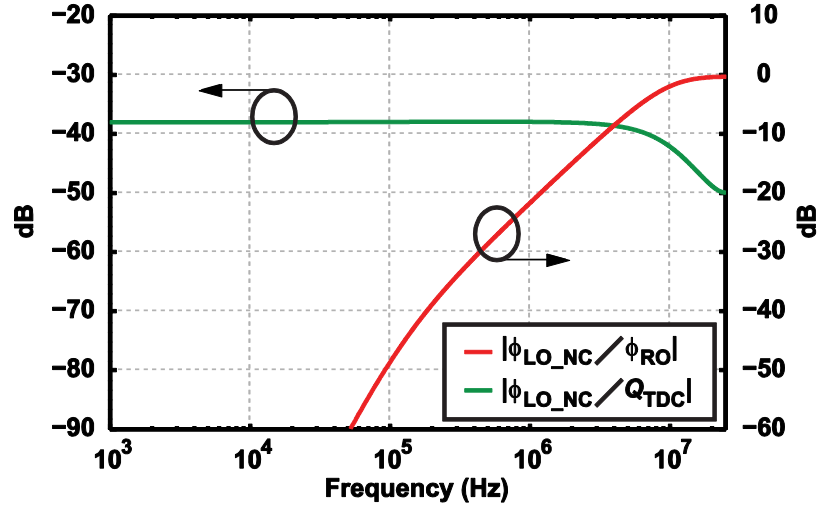


Figure 3.9: Transfer functions of $\phi_{RO}[n]$ to $\phi_{LO_NC}[n]$ and $Q_{TDC}[n]$ to $\phi_{LO_NC}[n]$.

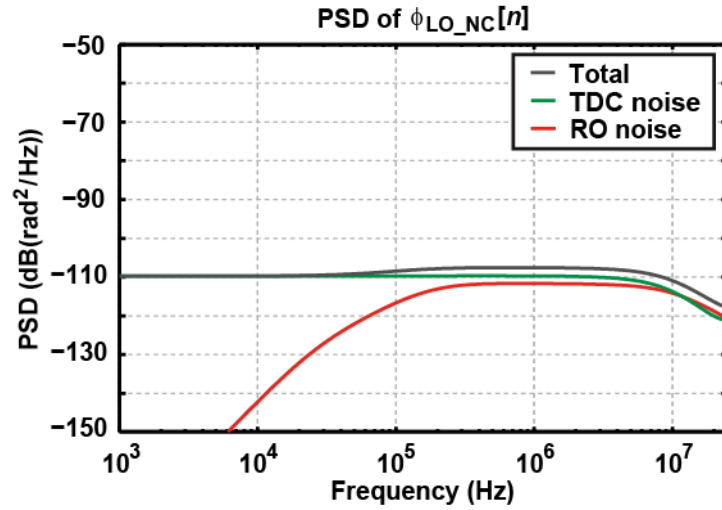


Figure 3.10: Calculated PSD of $\phi_{NC_LO}[n]$.

To be noted, the signal $\phi_{NC}[n]$ used for noise cancellation also contains spurious tones originated from the nonlinear behavior of the sub-sampling TDC. These spurs affect the wanted signal during the complex multiplication implemented in the I/Q rotator of the digital PNC

circuit. However, they are not as critical as the spurs that appear in the LO signal. This can be observed from the receiver chain in Fig. 3.2. The interference signal at the receiver input can be very large compared to the wanted signal. But after down conversion, the interference signal will be greatly attenuated by the baseband AAFs thus significantly relaxes the spurs requirement for $\phi_{\text{NC}}[n]$.

There are two important delay paths in the PNC technique; their delay difference affects the effectiveness of noise cancellation. These two delay paths are illustrated in a simplified PNC receiver block diagram shown in Fig. 3.12. The first one is the I/Q signal path, which starts from the digital PLL RO output, continues through the mixer, baseband ADC, and ends at the I/Q rotator in the digital PNC circuit. This is the path where phase noise deteriorates the wanted signal. The other path is the phase noise extraction path, which begins at the digital PLL RO output, continues through the TDC, and also ends at the I/Q rotator. This is the path where LO phase noise is extracted and sent to digital PNC baseband for noise cancellation. The delay difference issue can be explained by taking a signal $x(t)$ and subtract it with a delayed version of itself $x(t - \tau)$, where τ is the delay difference. Due to this non-zero time delay, the subtraction would not be zero and in frequency domain becomes $2\sin(\pi f \tau)|X(f)|$. Plotted in Fig. 3.13 is the effect of delay difference on the IPN after phase noise cancellation. As shown, the larger the

delay differences the worse the cancellation will be. Moreover, in the PNC receiver prototype the reference clock (CLK_{REF}) frequency, 49 MHz, and the ADC clock (CLK_{ADC}) frequency, 62 MHz, are not the same. Due to the different operation frequency the delay differences would not be a constant but varies over time. To minimize the delay difference and achieve an optimum performance, the delay of each path is carefully controlled by using register arrays as explained in the following.

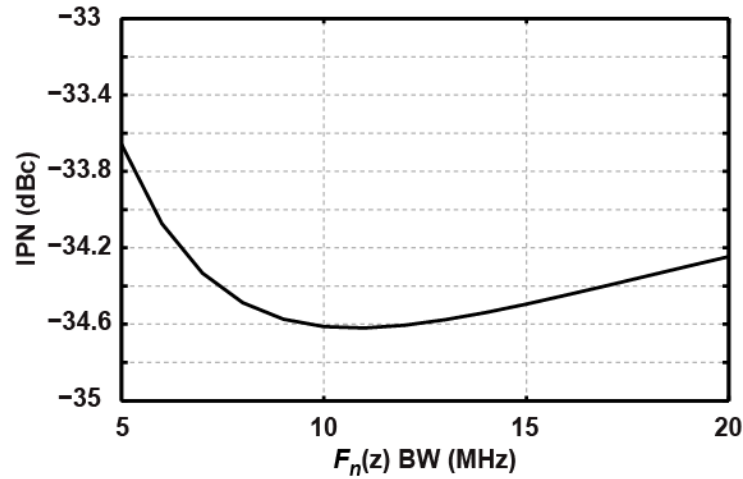


Figure 3.11: The effect of $F_n(z)$ BW on the overall IPN.

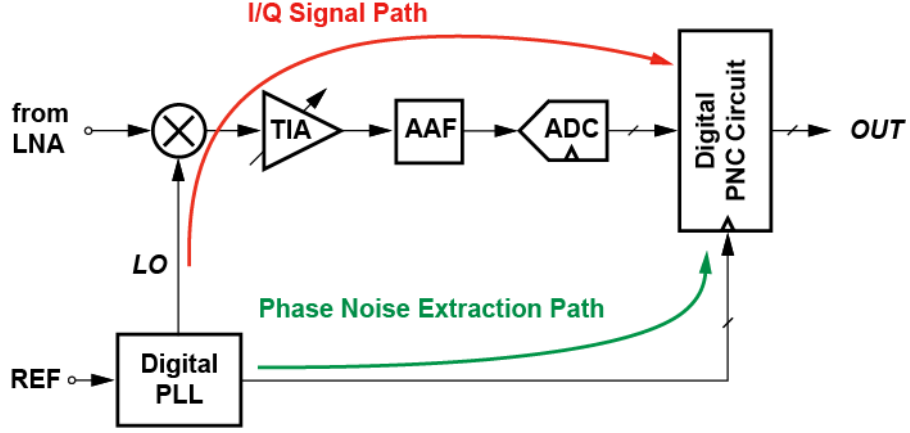


Figure 3.12: Two delay paths: I/Q signal path and phase noise extraction path.

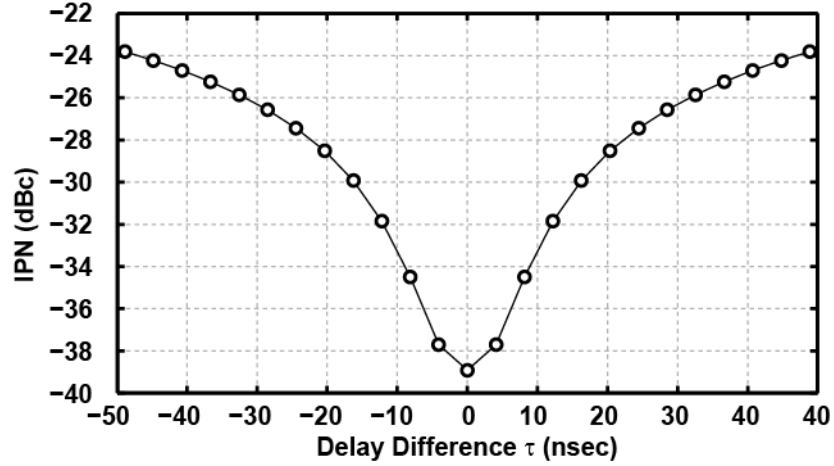


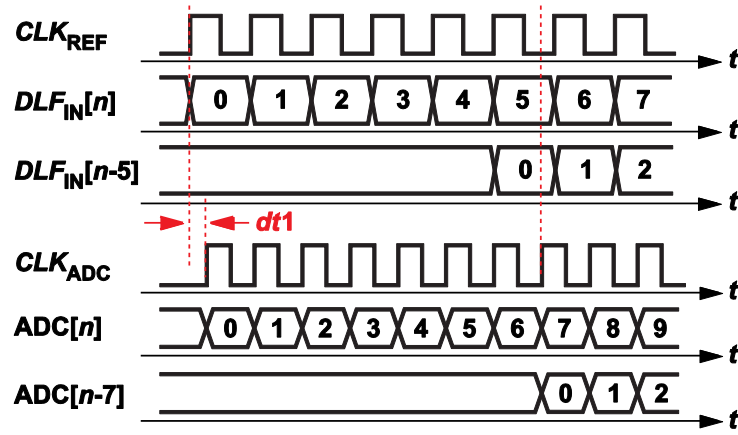
Figure 3.13: The effect of delay difference τ on the overall IPN.

Fig. 3.14(a) shows a timing diagram of $DLF_{IN}[n]$ and $ADC[n]$, and their sampling clocks CLK_{REF} and CLK_{ADC} , respectively. In order to simplify the discussion and without loss of generality, here we assume the delay of LO phase noise to TDC and that to baseband ADC both zero. In practice, they are not zero and have a constant delay difference due to narrow band

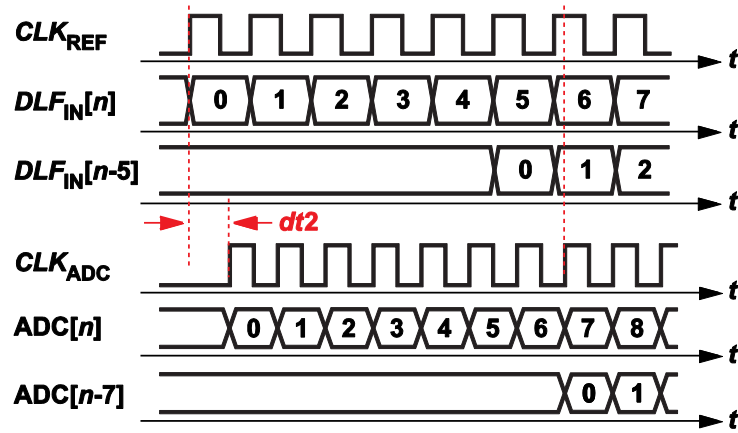
operation. As discussed latter in this section this constant delay difference can be compensated.

In Fig. 3.14(a), the first sample edge of CLK_{REF} leads the first sample edge of CLK_{ADC} by $dt = dt1$. This indicates that the phase noise which affects the baseband signal $ADC[0]$ is a delayed version of the phase noise captured in $DLF_{IN}[0]$. Furthermore, the $DLF_{IN}[0]$ sample is delayed by K reference clock cycles before reaching the digital PNC circuit. Afterwards, $DLF_{IN}[0]$ is re-sampled by the digital PNC circuit at the 8th sample edge of CLK_{ADC} . On the other hand, the $ADC[0]$ sample is delayed by M ADC clock cycles before arriving at digital PNC circuit ($K = 5$ and $M = 7$ in this example). Then $DLF_{IN}[0]$ will be used to cancel the phase noise in $ADC[0]$. For this case, the delay difference τ equals to $dt1$, as marked in Fig. 3.14(c). In order to characterize the statistic of τ , instead of tracing all sample data to find out each delay difference, an alternative way is to consider the possible cases of dt (the delay difference of the first sample edges) and observe its relationship with respect to τ . Fig. 3.14(b) depicts another example where the first sample edge of CLK_{REF} leads that of CLK_{ADC} by $dt = dt2$. Here $dt2$ is greater than $T_X = ((K+1) \times T_{REF} - M \times T_{ADC})$ but less than T_{REF} . Under this condition, the 8th sample edge of CLK_{ADC} would capture $DLF_{IN}[1]$ instead of $DLF_{IN}[0]$. This means $DLF_{IN}[1]$ will be used in digital PNC circuit to cancel phase noise in $ADC[0]$. As marked in Fig. 3.14(c), the delay difference τ of this case equals to $(dt2 - T_{REF})$. The relationship between dt and τ can be analyzed in a similar manner for larger dt . As shown in Fig. 3.14(c), τ is actually periodic with respect to dt . This indicates τ is

confined and uniformly distributed between $-\alpha T_{\text{REF}}$ sec and $+(1 - \alpha)T_{\text{REF}}$ sec, where $\alpha = (MT_{\text{ADC}} - KT_{\text{REF}}) / T_{\text{REF}}$ is a constant value. Moreover, if we take into account the constant delay difference originated from the delay of LO phase noise to TDC and that to baseband ADC, by setting the proper values of K and M , the overall delay difference can be controlled to be uniformly distributed within -10 nsec and +10 nsec. This corresponds to an rms delay difference of 5.8 nsec, and from simulation this can achieve an IPN around -36 dBc.



(a)



(b)

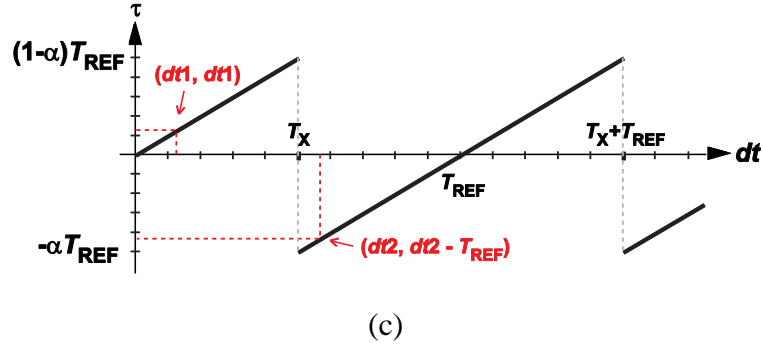


Figure 3.14: Delay difference timing diagram. (a) Case 1: $0 < dt < T_X$. (b) Case 2: $T_X < dt < T_{REF}$.

(c) Delay difference τ with respect to dt .

3.5. Measurement Results

The PNC quadrature receiver prototype consists of two chips: a receiver chip and a PNC chip.

Fig. 3.15 shows their micrograph. The receiver chip contains the RO-based digital PLL, LO buffers, and receiver chain (LNA, mixers, and TIAs). Its core area is measured to be 0.91 mm x 0.52 mm. The second chip contains the digital PNC circuit with a core area of 0.11 mm x 0.34 mm. Both chips are fabricated in a 65-nm CMOS technology and tested together with off-chip AFFs and ADCs.

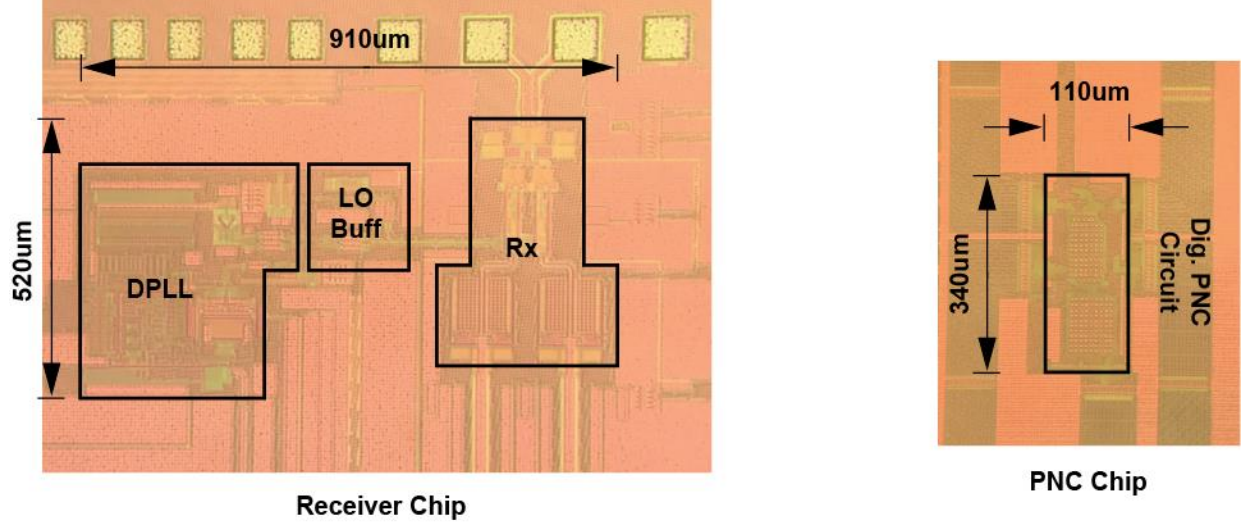
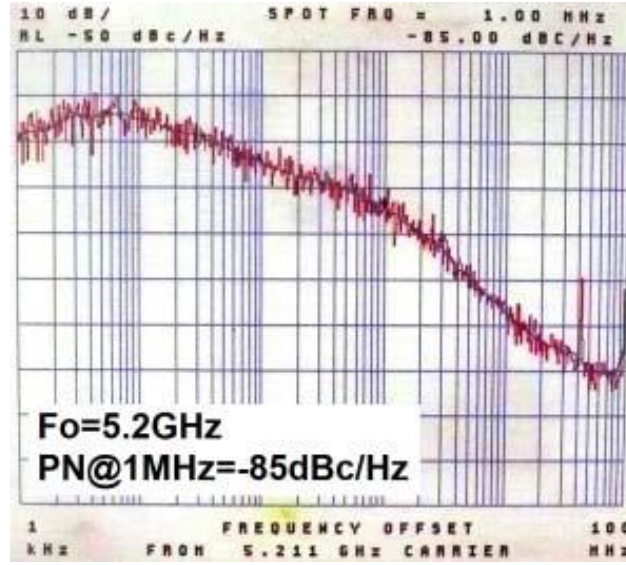
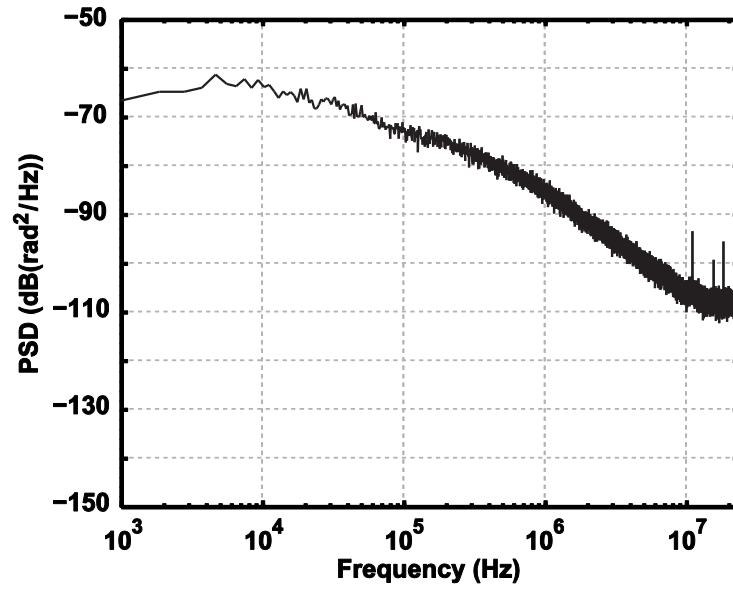


Figure 3.15: Micrograph of receiver chip and PNC chip.

The digital PLL performance is characterized from a standalone chip. The measured digital PLL output frequency is from 4.5 to 6.5 GHz, and 2.25 to 3.25 GHz through a divide-by-2 and multiplexing circuit at the digital PLL output. The measured phase noise results along with the extracted $(DLF_{IN}[n] / K_{TDC})$ spectra are reported in Fig. 3.16. As shown, the two noise spectra match up to around 12 MHz ($\approx F_{REF}/4$), and after that, TDC high-passed noise dominates the high frequency spectrum of $(DLF_{IN}[n] / K_{TDC})$.



(a)

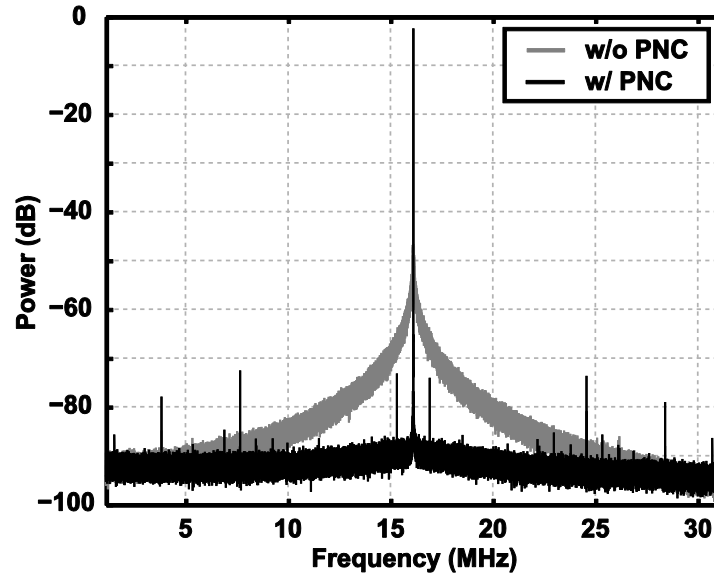


(b)

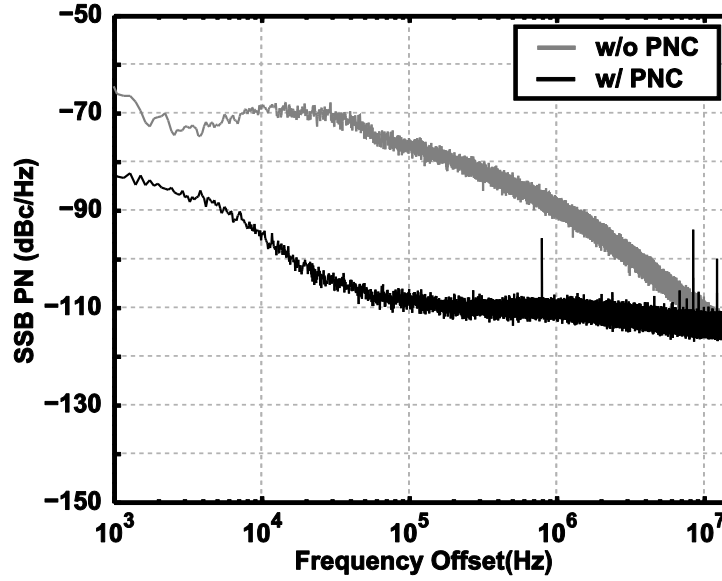
Figure 3.16: Measurement results. (a) PLL output phase noise at 5.2 GHz. (b) PSD of ($DLF_{IN}[n]$

$/ K_{TDC}$).

To verify the phase noise cancellation concept, the PNC quadrature receiver is first tested by receiving a 2.4 GHz single-tone signal. Fig. 3.17 (a) and (b) shows the power spectrum and single-side band (SSB) phase noise of the digitized baseband signal, respectively. With PNC the spot phase noise at 1 MHz offset is reduced by 21 dB, from -88 to -109 dBc/Hz. The IPN integrated from 1 KHz to 15 MHz frequency offset is improved by 17.8dB from -16.8 to -34.6 dBc. It is also noted the SSB phase noise result with PNC is dominated by noise from the RF signal source at low frequency offset.



(a)



(b)

Figure 3.17: 2.4GHz single-tone input signal test. (a) Power spectrum of the digitized baseband signal. (b) SSB phase noise of the digitized baseband signal.

Furthermore, to verify the PNC technique on supply noise reduction a 240 KHz sinusoidal tone is injected onto RO supply. Fig. 3.18(a) shows the test setup. The test result is shown in Fig. 3.18(b). With PNC the supply-induced phase noise is suppressed by 38 dB, from -33 to -71 dBc. Fig. 3.19 shows the measured constellation results of receiving BPSK and 64QAM signals with 10 Msymb/sec of data rate and carrier frequency around 2.4 GHz. The EVM improvement demonstrates that the proposed PNC technique greatly reduces RO phase noise, achieving an EVM of -37.5 dB for 64QAM signal.

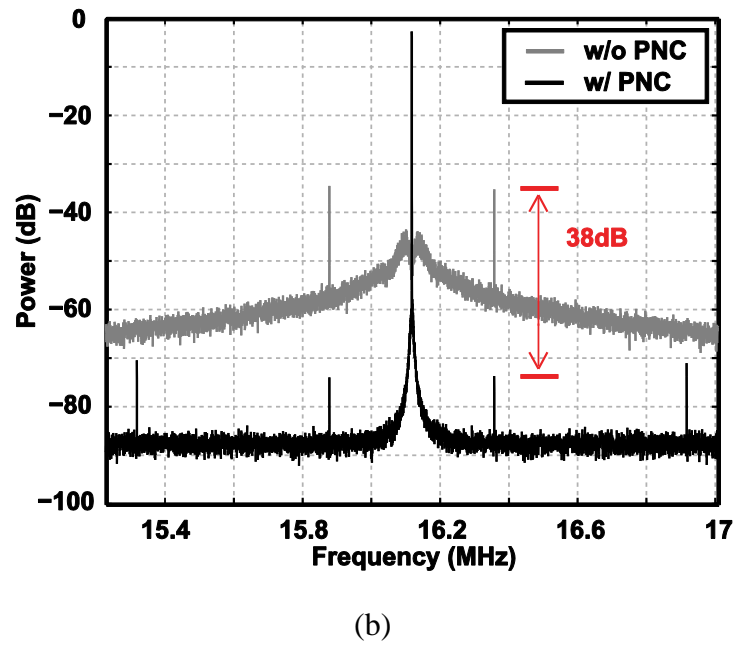
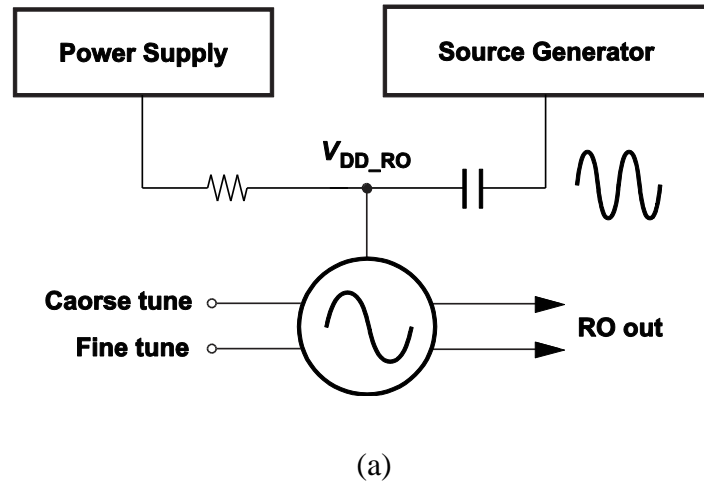


Figure 3.18: 2.4GHz single-tone input signal test with supply noise injection. (a) Test setup. (b)

Power spectrum of the digitized baseband signal.

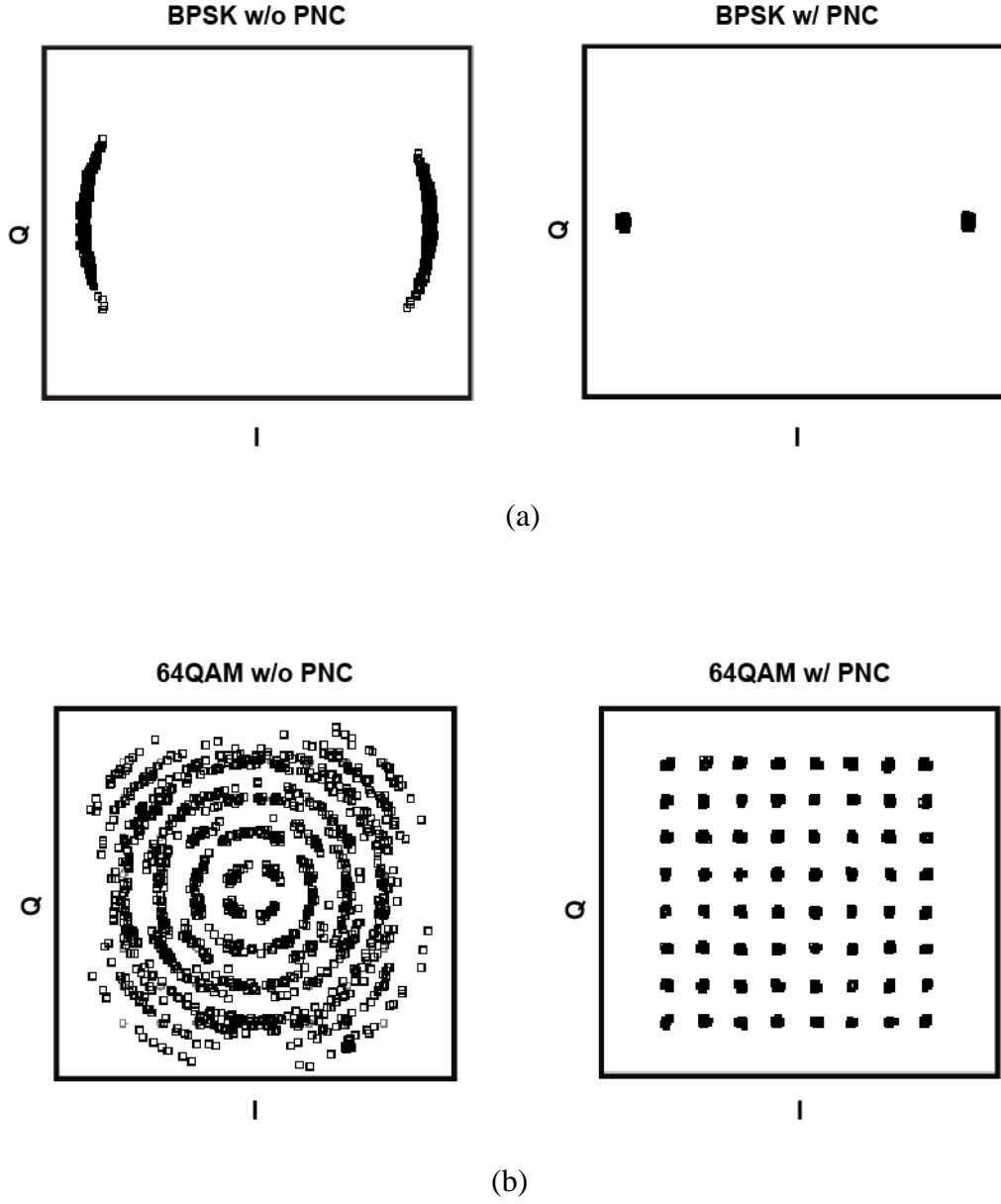


Figure 3.19: Measured constellation with and without PNC. (a) BPSK signal. (b) 64QAM signal.

The supply voltages of each building blocks are 1 V for the digital PLL, LO buffer, and digital PNC circuit, and 1.2 V for the receiver chain. The total power consumption, excluding off-chip AFFs and ADCs, is 46.5 mW, where 32.5 mW is consumed by the receiver chain, and 14

mW from the digital PLL including the digital PNC circuit. The digital PNC circuit itself consumes 2 mW of power and 0.04 mm² of area. Table 3.1 summarizes the system performance.

3.6. Conclusions

In summary, a digital PNC technique for RO-based quadrature receivers is presented. The RO phase noise information is extracted from the digital PLL, and used to restore the randomly rotated baseband signal in digital domain. The proposed technique enables RO-based LO to be used in complex modulation systems which are more sensitive to phase noise. In practice, the overall noise performance is limited by the TDC noise and the delay difference between the I/Q signal path and the phase noise extraction path. However, it is believed that the TDC resolution can continue to be improved as CMOS process advance. The delay difference limitation can also be mitigated through digital interpolation filters. The digital-intensive and background processing natures of the proposed PNC technique allows it to be easily implemented in parallel with reciprocal mixing noise cancellation techniques [12][13], to reduce both close-in and out-of-band phase noise.

Table 3.1: Performance summary and comparison to other noise cancelling PLLs.

		This Work	[15]	[21]
Topology	Noise Extraction	Digital PLL	Delay Discriminator	Test-Signal Based
	Noise Cancellation	Digital PNC Circuit	NC Delay Cell	NC Transistors ⁽⁵⁾
Operation Freq. (GHz)		2.25~3.25, 4.5~6.5	3.5~7.1	0.4~3
Spot PN w/o PNC (dBc/Hz)		-88@1MHz	-92.5@1MHz	N/A
Spot PN w/ PNC (dBc/Hz)		-109@1MHz	-105@1MHz	N/A
RMS Jitter w/o PNC (psec)		9.6 (1K~15M) ⁽¹⁾	5.2 (10K~10M)	8 (50K hits)
RMS Jitter w/ PNC (psec)		1.2 (1K~15M) ⁽¹⁾	3.8 (10K~10M)	4.8 (50K hits)
Core Area (mm ²)		0.47 ⁽²⁾ / 0.17 ⁽³⁾ / 0.04 ⁽⁴⁾	0.12 ⁽³⁾	0.08 ⁽³⁾
Power (mW)		46.5 ⁽²⁾ / 14 ⁽³⁾ / 2 ⁽⁴⁾	29.6 ⁽³⁾	3.1 ⁽³⁾
Supply (V)		1 / 1.2	1.2	1
Technology (nm)		65	90	130

⁽¹⁾Calculated from IPN ⁽²⁾Off-chip AAFs and ADCs excluded

⁽⁴⁾Digital PNC circuit

⁽³⁾PLL circuit including noise extraction & cancellation

⁽⁵⁾Supply noise cancellation

Chapter 4

A Low-Noise 48GHz CMOS PLL for 802.15.3c

Heterodyne Transceivers

4.1. Introduction

In wireless communications, to achieve high-data rate the system would either utilize larger BW or employ complex modulation schemes such as QAM. While under some situations one cannot arbitrary enlarge their BW, e.g. technical regulations, employing QAM with large constellation size becomes the better choice to enhance the data rate. However, larger constellation size requires lower error vector magnitude (EVM). Integrated phase noise (IPN) of a frequency synthesizer directly affects the EVM. Therefore, in systems with complex constellations the required EVM determines the synthesizer phase noise specification. Building a low noise carrier signal may not be a problem in cellular band but becomes very challenging in the mm-Wave regime. The challenges show up as following. First, the VCO phase noise, which dominates PLL high-offset frequency phase noise, is worse as the loss in the resonators becomes larger. Second, because of the greater division ratio of f_{vco} over f_{ref} , the detector noise contribution to the PLL output in-band noise also becomes larger. In this paper we focus on the second problem and employ mm-Wave sub-sampling phase detection technique to reduce the detector noise. This

work extends previous published work [26] by improving the in-band phase noise and IPN over 10 dB while reducing the power consumption by 6 mW. Dummy metal filling is also added in all mm-Wave building blocks.

4.2. PLL Architecture

In conventional PLL design the in-band phase noise is dominated by detector noise, which is the sum of the reference source, PFD, and CP noise. As the frequency becomes higher the division ratio also increases which greatly magnifies the noise contribution from these sources to PLL output. In our case the division ratio is 448 which is 53 dB of magnification. To address this problem, an mm-Wave sub-sampling PLL is presented as shown in Fig. 4.1. The high frequency VCO, buffer, and divide-by-2 employ the unique DiCAD structure based LC-tanks for ultra-wideband operation [26]. The PLL contains two feedback paths, one frequency lock path and one phase lock path, as indicated in Fig. 4.1. When the PLL turns on, the frequency lock path is first activated and phase lock path is disabled. The frequency locked path helps to bring the VCO to its targeted frequency. After the frequency is locked, the circuit automatically disables frequency lock path and turns on the phase lock path. The phase lock path then locks the VCO phase to the phase of the reference clock.

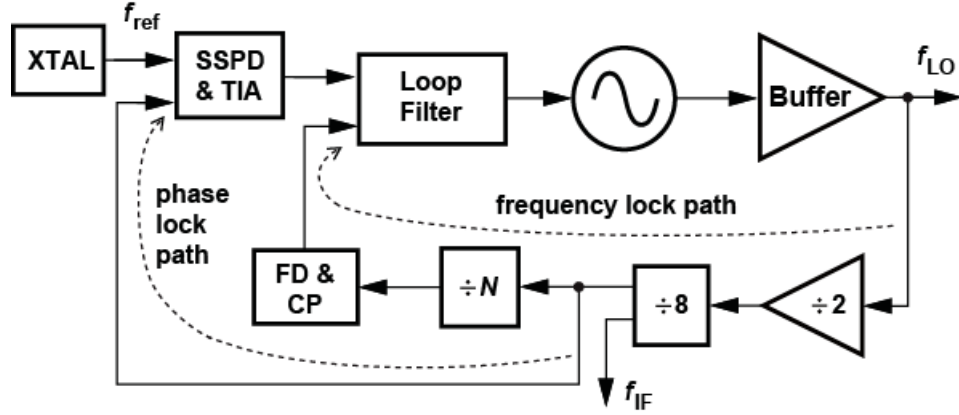


Figure 4.1: PLL block diagram.

Compared to low frequency sub-sampling PLL [6], the frequency of the VCO here is too high for reference signal to directly sample it. The main problem is that the sub-sampling phase detector (SSPD) has limited lock range. Note that for conventional phase frequency detectors (PFD), the locking range, calculated as T_{fb} / T_{ref} , can be as high as 100% of the reference period. T_{fb} is the period of the divider feedback signal. On the other hand, SSPD's locking range would be as small as 0.2%, because $T_{fb} = T_{vco}$ in traditional SSPD PLL [6]. To solve this limited locking range problem, instead of directly connecting the VCO to the SSPD, the 48 GHz signal is first divided down to 3 GHz and then sent to the SSPD. This extends the lock range to 6.25%. An additional benefit of this approach is that there is no need for dummy circuitry to prevent reference spurs problem [6]. The dividers naturally prevent the sampling circuit from disturbing the VCO. The SSPD and transimpedance amplifier (TIA) circuits are shown in Fig. 4.2 and Fig.

4.3, respectively.

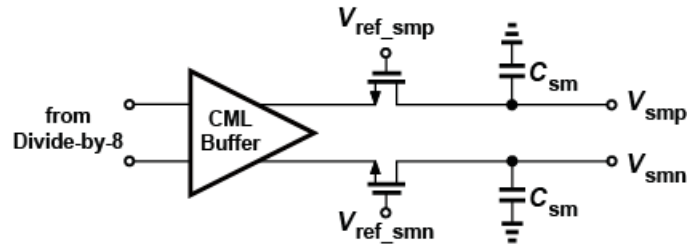


Figure 4.2: SSPD circuit.

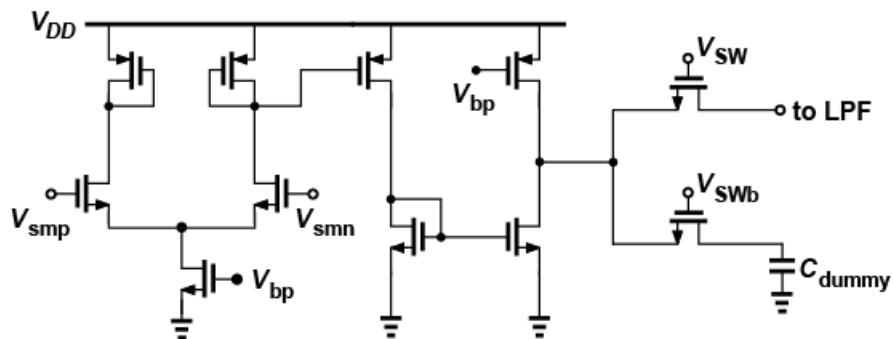


Figure 4.3: Transimpedance amplifier circuit.

All the RF passive components were designed to be compliant with process design rules. Failure to do so will result in serious manufacturability issues or unacceptable RF performance. In 65 nm CMOS process or high nodes, one of the challenges is to design passive elements, such as inductors, with good immunity to the presents of dummy structures required by layer density rules. For example the artificial dummy fillers over entire BEOL metal stack were properly

arranged in the layouts of our VCO inductor and DiCADs, and the overall performances were carefully verified in EM simulation. Compared to the non-dummy filled inductor, the dummy-filled one shows very minor performance changes, a 1.8% inductance drop from 87.1 to 85.5 pH and a 3.6% degrade of Q factor from 27.3 to 26.4. The impact of artificial dummy fillers on the DiCAD capacitance and Q-factor is designed to be negligible in simulation.

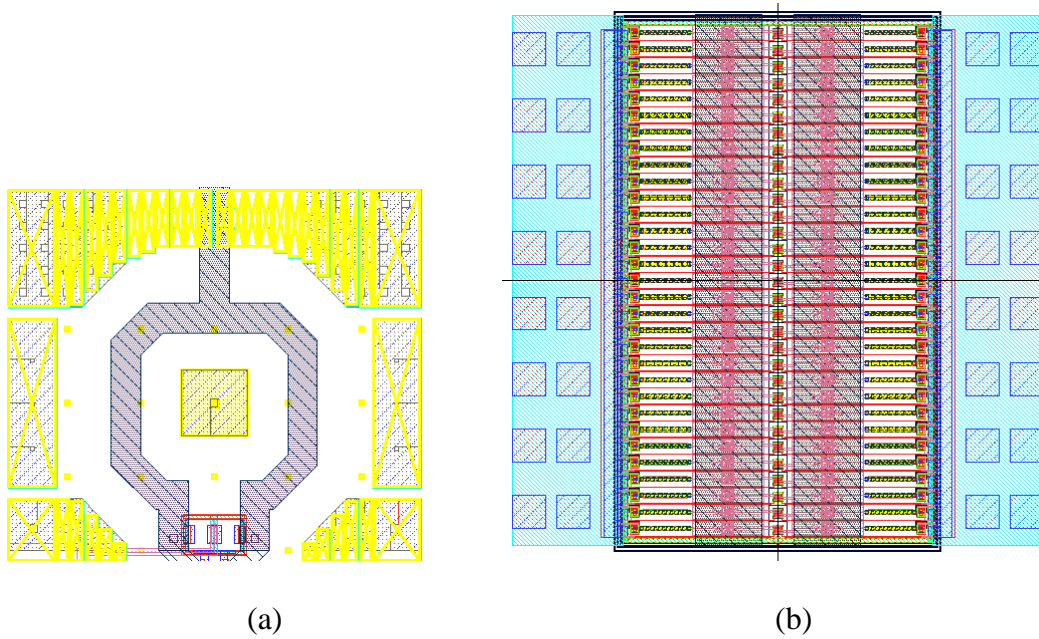


Figure 4.4: Passive components layout design with artificial dummy fillers.

(a) VCO inductor, and (b) DiCAD.

4.3. Measurement Results

The PLL is fabricated in TSMC 65nm CMOS process. Fig. 4.5 is the chip micrograph with the partition of major blocks. The reference frequency is 108 MHz and the PLL occupies a die area of 0.25 mm^2 . The loop BW is set to 2 MHz. The loop filter passive devices are partially design off-chip on the PCB board. Fig. 4.6 shows the measured phase noise result at 48.38 GHz. The in-band phase noise is -96 dBc/Hz. The integrated phase noise calculated from 10 KHz to 10 MHz is -30 dBc. The power consumption is 66mW from 1 V supply, which is measured after phase locked and the divide-by-N and FD/CP bias circuitry is powered down.

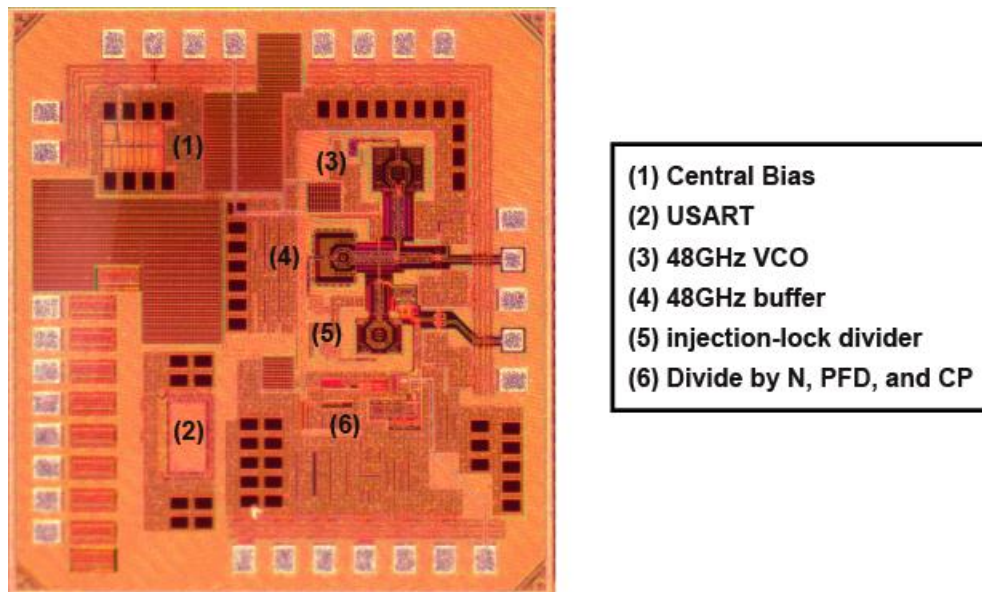
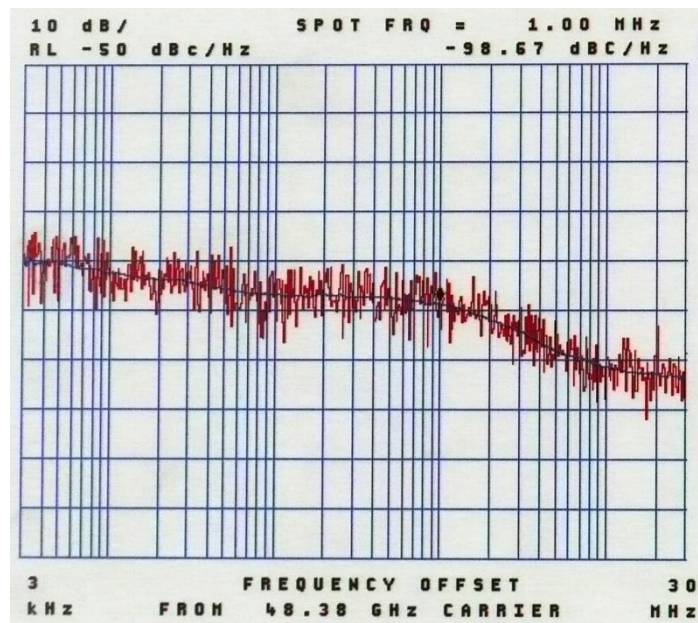
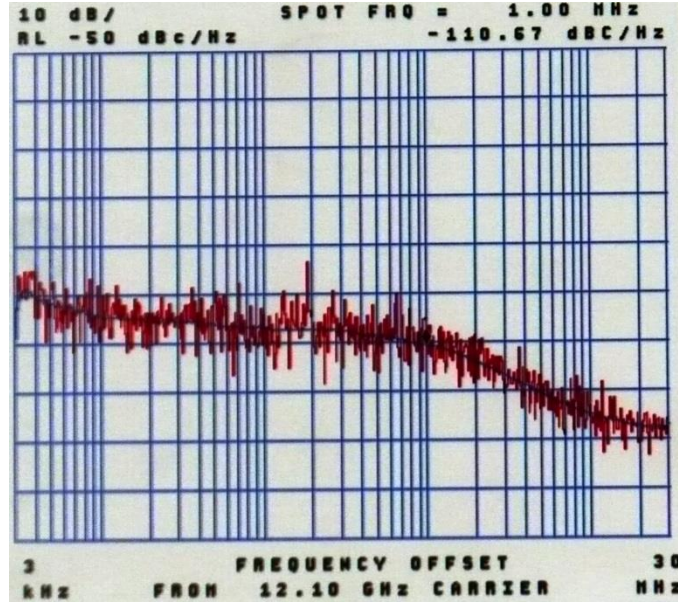


Figure 4.5: Micrograph of the mm-Wave integer- N PLL.

Table 4.1 compares this work with other recently published PLLs targeting at mm-Wave frequencies. This work achieves 10 dB better in-band phase noise than others thanks to the proposed technique.



(a)



(b)

Figure 4.6: Measured PLL output phase noise.

4.4. Conclusions

A low-noise wide-band integer- N PLL is presented to generate low noise carrier signal for high-data rate 802.15.3c heterodyne transceivers. Sub-sampling technique is employed to improve the phase noise performance. Unlike tradition sub-sampling technique which directly samples the VCO output, in this work the VCO signal is first divided-by-16 then sent to the phase detector to increases the lock range and improve reliability. Measurement shows a -98.7 dBc/Hz in-band phase noise and -30 dBc integrated phase noise at 48 GHz, which is suitable for 64 QAM data communication at 60 GHz.

Table 4.1: Performance summary and comparison to other mmWave PLLs

	[27]	[28]	[29]	[30]	This Work
Center Freq. (GHz)	58~63	55~66	57.9~68.3	53.8~63.3	43.2~51.8
Technology (nm)	65	40	65	40	65
Reference Freq. (MHz)	36	20000	135	40	108
PN (dBc/Hz) @10KHz	-57.7	-71	-81	-81	-92
PN (dBc/Hz) @100KHz	-63.6	-85	-85	-88	-96
PN (dBc/Hz) @1MHz	-95	-102	-91	-88.3	-98.7
PN (dBc/Hz) @10MHz	-113	-108	-109	-107.5	-111
IPN (dBc)	N/A	N/A	N/A	N/A	-30
Jitter (fsec)	N/A	N/A	N/A	203-230	102
Supply (V)	1.2V	1.1V	1.2V	0.9/1	1V
Power (mW)	80	112	24.6	42	66
Area (mm ²)	2.48	N/A	0.192	0.16	0.25

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