UNIVERSITY OF CALIFORNIA, SAN DIEGO

Energy-Efficient Integrated Biomedical Circuits and Systems for Unobtrusive Neural Recording and Wireless Body-Area Networks

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Bioengineering

by

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Professor Patrick P. Mercier

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The dissertation of Chul Kim is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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DEDICATION

Dedicated to my family Aehyang Park, Ahrin Kim and Elmin Kim,
my parents and my Lord.

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Chapter Four is largely a combination of material that will be submitted to the IEEE Journal of Solid-State Circuits and appeared in 2016 Symposium on VLSI Circuits: C. Kim, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs, "A Miniaturized Fully Integrated Wireless-power-receiver-on-chip with an Adaptive Buck-boost Regulating Rectifier and Low-loss H-tree Signal Distribution," in IEEE Journal of Solid-State Circuits (JSSC), in

preparation. C. Kim, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier and G. Cauwenberghs, "A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and Low-Loss H-Tree Signal Distribution," 2016 Symposium on VLSI Circuits, Kyoto, June 2016. The author is the primary author and investigator of these works.

Chapter Five is largely a reprint of material that will appear in the 2018 IEEE International Solid-State Circuits Conference (ISSCC): C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92dB dynamic range subμVrms noise 0.8μW/ch neural recording ADC array with predictive digital autoranging," 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, Feb. 2018, to appear. The author is the primary author and investigator of this work.

Chapter Six is largely a reprint of material in the Proceedings of the ESSCIRC 2014: C. Kim, S. Ha, C. M. Thomas, S. Joshi, J. Park, L. E. Larson, and G. Cauwenberghs, "A 7.86 mW +12.5 dBm In-Band IIP3 8-to-320 MHz Capacitive Harmonic Rejection Mixer in 65nm CMOS," Proceedings of the ESSCIRC, Sep. 2014. The author is the primary author and investigator of this work.

Chapter Seven is largely a selection of material in the following two venues: C. Kim, S. Joshi, C. M. Thomas, S. Ha, L. E. Larson and G. Cauwenberghs, "A 1.3 mW 48 MHz 4 Channel MIMO Baseband Receiver With 65 dB Harmonic Rejection and 48.5 dB Spatial Signal Separation," in IEEE Journal of Solid-State Circuits (JSSC), vol. 51, no. 4, pp. 832-844, April 2016 (VLSI Circuits 2015 Special Issue). C. Kim, S. Joshi, C. M. Thomas, S. Ha, A. Akinin, L. E. Larson, and G. Cauwenberghs, "A CMOS 4-channel MIMO baseband receiver with 65dB harmonic rejection over 48MHz and 50dB spatial signal separation over 3MHz at 1.3mW," 2015 Symposium on VLSI Circuits, Kyoto, pp. C304-C305, Jun. 2015. The author is the primary author and investigator of this work.

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PUBLICATIONS

C. Kim, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs, "A Miniaturized Fully Integrated Wireless-power-receiver-on-chip with an Adaptive Buck-boost Regulating Rectifier and Low-loss H-tree Signal Distribution," in *IEEE Journal of Solid-State Circuits (JSSC)*, in preparation.

C. Kim, C.-S. Chae, Y.-S. Yuk, C. M. Thomas, Y.-G. Kim, J.-K. Kwon, S. Ha, G. Cauwenberghs, and G.- H. Cho, "A 500 MHz-bandwidth 7.5 mV_{PP}-ripple Power-Amplifier Supply Modulator for RF Polar Transmitters," in *IEEE Journal of Solid-State Circuits (JSSC)*, in revision.

C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92dB dynamic range sub? μVrms noise 0.8μW/ch neural recording ADC array with predictive digital autoranging," *2018 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 2018, to appear.

J. Park, C. Kim, A. Akinin, S. Ha, G. Cauwenberghs, and P. P. Mercier, "Wireless Powering of mm-scale Fully-on-chip Neural Interfaces," *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings*, Oct. 2017.

C. Kim, S. Ha, J. Park , A. Akinin , P. P. Mercier and G. Cauwenberghs, "A 144 MHz Fully Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation for mm-sized Implants," in *IEEE Journal of Solid-State Circuits (JSSC)*, 2017, to appear.

C. Kim, S. Ha, A. Akinin, J. Park, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs, "Design of Miniaturized Wireless Power Receivers for mm-sized Implants," *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, pp. 1-8, Apr. 2017 (Invited Paper).

S. Joshi, C. Kim, S. Ha, and G. Cauwenberghs, "From Algorithms to Devices: Enabling Machine Learning through Ultra-Low-Power VLSI Mixed-Signal Array Processing," *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, pp. 1-9, Apr. 2017 (Invited Paper).

S. Joshi, C. Kim, S. Ha, Y. M. Chi and G. Cauwenberghs, "2pJ/MAC 14b 8×8 linear transform mixed- signal spatial filter in 65nm CMOS with 84dB interference suppression," *2017 IEEE International Solid- State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 364-365, Feb. 2017.

S. Ha, A. Akinin, J. Park, C. Kim, H. Wang, C. Maier, P. P. Mercier, and G. Cauwenberghs, "Silicon- Integrated High-Density Electrocortical Interfaces," in *Proceedings of the IEEE*, vol. 105, no. 1, pp. 11-33, Jan. 2017.

S. Joshi, C. Kim and G. Cauwenberghs, "A 6.5?W/MHz Charge Buffer With 7-fF Input Capacitance in 65- nm CMOS for Noncontact Electropotential Sensing," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 12, pp. 1161-1165, Dec. 2016.

S. Ha, C. Kim, J. Park, S. Joshi, and G. Cauwenberghs, "Energy-Recycling Telemetry IC with Simultaneous 11.5-mW Power and 6.78-Mbps Backward Data Delivery over a Single 13.56-MHz Inductive Link," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 11, pp. 2664-2678, Nov. 2016.

C. Kim, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier and G. Cauwenberghs, "A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and Low-Loss H-Tree Signal Distribution," *2016 Symposium on VLSI Circuits*, Kyoto, June 2016.

S. Joshi, C. Kim, and G. Cauwenberghs, "A 6μW/MHz charge buffer with 7fF input capacitance in 65nm CMOS for non-contact electropotential sensing," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2907-2907, May 2016.

C. Kim, S. Joshi, C. M. Thomas, S. Ha, L. E. Larson and G. Cauwenberghs, "A 1.3 mW 48 MHz 4 Channel MIMO Baseband Receiver With 65 dB Harmonic Rejection and 48.5 dB Spatial Signal Separation," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 4, pp. 832-844, April 2016 (VLSI Circuits 2015 Special Issue).

C. Kim, S. Ha, J. Park, A. Akinin, P. P. Mercier and G. Cauwenberghs, "A 144MHz integrated resonant regulating rectifier with hybrid pulse modulation," *2015 Symposium on VLSI Circuits*, Kyoto, pp. C284- C285, Jun. 2015.

C. Kim, S. Joshi, C. M. Thomas, S. Ha, A. Akinin, L. E. Larson, and G. Cauwenberghs, "A CMOS 4- channel MIMO baseband receiver with 65dB harmonic rejection over 48MHz and 50dB spatial signal separation over 3MHz at 1.3mW," *2015 Symposium on VLSI Circuits*, Kyoto, pp. C304-C305, Jun. 2015.

S. Ha, A. Akinin, J. Park, C. Kim, H. Wang, C. Maier, G. Cauwenberghs, and P.P. Mercier, "A 16-channel wireless neural interfacing SoC with RF-powered energy-replenishing adiabatic stimulation," *2015 Symposium on VLSI Circuits*, Kyoto, pp. C106-C107, Jun. 2015.

J. Park, S. Ha, C. Kim, S. Joshi, T. Yu, W. Ma and G. Cauwenberghs, "A 12.6 mW 8.3 Mevents/s contrast detection 128128 imager with 75 dB intra-scene DR asynchronous random-access digital readout," *2014 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings*, Lausanne, pp. 564-567, Oct. 2014.

C. Kim, S. Ha, C. M. Thomas, S. Joshi, J. Park, L. E. Larson, and G. Cauwenberghs, "A 7.86 mW +12.5 dBm In-Band IIP3 8-to-320 MHz Capacitive Harmonic Rejection Mixer in 65nm CMOS," *Proceedings of the ESSCIRC*, Sep. 2014.

S. Ha, C. Kim, J. Park, S. Joshi and G. Cauwenberghs, "Energy-Recycling Integrated 6.78-Mbps Data 6.3- mW Power Telemetry over a Single 13.56-MHz Inductive Link," *2014 Symposium on VLSI Circuits*, pp. 53-54, Jun. 2014.

S. Ha, C. Kim, Y.M. Chi, A. Akinin, C. Maier, A. Ueno, G. Cauwenberghs, "Integrated Circuits and Electrode Interfaces for Noninvasive Physiological Monitoring," in *IEEE Transactions on Biomedical Engineering (TBME)*, vol. 61, no. 5, pp.1522-1537, May 2014.

Y.S. Yuk, S.-C Jung, C. Kim, H.-D Gwon, S. Choi, G.-H. Cho, "PSR Enhancement Through Super Gain Boosting and Differential Feed-Forward Noise Cancellation in a 65-nm CMOS LDO Regulator," in *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, pp.1-11, Nov. 2013.

Y.S. Yuk, S.-C Jung, B. Lee, S.-W. Wang, C. Kim, G.-H. Cho, "A CMOS LDO regulator with high PSR using Gain Boost-Up and Differential Feed Forward Noise Cancellation in 65nm process," *Proceedings of the ESSCIRC*, pp.462-465, Sep. 2012.

J.-C. Lee, S.-H. Jin, D.-S. Kim, Y.-J. Ku, C. Kim, B.-K. Park, H.-G. Kim, S.-J. Ahn, J.-J. Lee, S.-J. Hong, "A Low-Power Small-Area Open Loop Digital DLL for 2.2Gb/s/pin 2Gb DDR3 SDRAM," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 14-16, Nov. 2011.

C. Kim, C.-S. Chae, Y.-S. Yuk, Y.-G. Kim, J.-K. Kwon, G.-H. Cho, "A 105dB-Gain 500MHz-Bandwidth 0.1Ω-Output-Impedance Amplifier for an Amplitude Modulator in 65nm CMOS," 2010 *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 88-89, Feb. 2010.

T.-W. Kwak, M.-C. Lee, Y.-S. Yuk, K.-H. Lee, H.-H. Park, C. Kim, G.-H. Cho,"Hybrid Switching Amplifier Using a Novel Two Quadrant Wideband Buffer for Dynamic Power Supply Applications," *IEEE Power Electronics Specialists Conference (PESC)*, pp. 546-551, Jun. 2008.

ABSTRACT OF THE DISSERTATION

Energy-Efficient Integrated Biomedical Circuits and Systems for Unobtrusive Neural Recording and Wireless Body-Area Networks

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Despite tremendous progress over the years, current brain-machine interface (BMI) systems are relatively bulky, highly invasive, and limited in their effectiveness except for highly constrained tasks such as moving a cursor on a computer screen. To improve performance of current BMI systems, it is necessary to dramatically increase spatial resolution and coverage across the brain without constraining the mobility of the subject. This calls for innovative approaches to high-density integrated neural recording and stimulation using non-invasive or minimally invasive microelectrode and custom silicon integrated circuits at extreme energy and area efficiency.

In this thesis, I present energy-efficient fully integrated miniaturized implants for electrocortical recording and stimulation, and unobtrusive body-area networks systems for subcutaneous power delivery and data communication, as fundamental building blocks to next generation BMI. First I describe a fully wireless, encapsulated neural interface and acquisition chip (ENIAC) in 180nm silicon-on-insulator (SOI) complementary metal-oxide-semiconductor (CMOS) technology for 16-channel neural recording and stimulation including integrated 4×4 electrode array, coil antenna, and wireless power transfer and data telemetry without any external components, completely contained in less than $3mm^3$ volume suitable for minimally invasive surgical insertion on the cortical surface. A novel fully integrated wireless power receiver design with an RF-decoupled H-tree signal distribution network delivers 1mW power over 1 cm distance while mitigating RF interference in the sensitive analog front-end and acquisition circuits for recording of electrocorticography (ECoG) signals transmitted through the skull. Second I highlight a $1mm^2$ 16-channel neural recording and acquisition system-on-chip in 65nm CMOS offering 92 dB input dynamic range and <1μVrms input-referred noise covering DC-500Hz signal bandwidth at 0.8μW power consumption per channel, offering a record 2.6 power efficiency factor (PEF). Validation with in vivo recordings in frontal cortex of marmoset primates reveals infra-slow (<0.1 Hz) local-field potentials (LFP) indicative of subject arousal during a visual attention task alternating with periods of rest and feeding. I will further present advances in cognitive radio baseband transceivers for ultra-low power RF wireless non-line-of-sight body-area network communication with spectral tuning and spatial selectivity across 48MHz signal bandwidth at 1.2mW power. These technology advances combine to support further developments towards modular wireless, minimally invasive, whole-brain electrocortical recording at near-cellular resolution.

Chapter 1

Introduction

My research aims at improving the quality of human life through advancing the engineering and applications of silicon integrated technology interfacing with biology in a variety of forms ranging from high-density brain-machine interfaces (BMI) for whole-brain chronic neural recording and stimulation to unobtrusive wearable sensors and body-area networks for continuous health monitoring and electroceutical treatment.

1.1 Objectives

BMI research has been traditionally directed towards clinical and consumer applications of brain decoding for improved mobility of the motor impaired. Despite tremendous progress over the years, current BMI systems are relatively bulky, highly invasive, and limited in their effectiveness except for highly constrained tasks such as moving a cursor on a computer screen. To improve performance in registering complex cognitive brain function in highly dynamical settings over extended time periods, it is necessary to dramatically increase spatial resolution and coverage across the brain without constraining the mobility of the subject. This calls for innovative approaches to high-density integrated neural recording and stimulation using microelectrode arrays and custom silicon integrated circuits at extremely high energy and area efficiency.

In addition, the endurance of BMIs should be dramatically improved from

their current acute (short-term) use in neuroscience applications to chronic (long-term) use for clinical applications. Non-invasive or minimally invasive implants are preferred over invasive techniques due to their superior foreign body response and substantially reduced risk of infection. Power autonomous and fully encapsulated miniaturized implants overcome major obstacles to the longevity of BMI technologies, as reduced micro-motions result in less astroglial scarring and cell death, especially for high-resolution intracortical microelectrode arrays. There is great interest in the medical community for the development of such long-term, information-rich and unobtrusive BMIs to enable quality of life improvements for patients suffering from debilitating conditions.

Thus the objective of my BMI research is to pursue the design, implementation, and *in vivo* validation of energy-efficient fully integrated miniaturized implants for electrocortical recording and stimulation, and unobtrusive body-area networks systems for subcutaneous power delivery and data communication, as fundamental building blocks to next generation BMI.

1.2 Organization

Chapter 2 presents a design methodology of miniaturized implants focusing on wireless power transmission (WPT). Advances in free-floating miniature medical implants promise to offer greater effectiveness, safety, endurance, and robustness than today's prevailing medical implants. WPT is key to miniaturized implants by eliminating the need for bulky batteries. This chapter reviews design strategies for WPT with mm-sized implants focusing on resonant electromagnetic and ultrasonic transmission. While ultrasonic WPT offers shorter wavelengths for sub-mm implants, electromagnetic WPT above 100 MHz offers superior power transfer and conversion efficiency owing to better impedance matching through inhomogeneous tissue. Electromagnetic WPT also allows for fully integrating the entire wireless power receiver system with an on-chip coil. Attaining high power transfer efficiency requires careful design of the integrated coil geometry for high quality factor as well as loop-free power and signal distribution routing to avoid

eddy currents. Regulating rectifiers have improved power and voltage conversion efficiency by combining the two RF to DC conversion steps into a single process. Example designs of regulating rectifiers for fully integrated wireless power receivers are presented.

Chapter 3 presents a fully-integrated resonant regulating rectifier (IR^3) with an on-chip coil used to wirelessly power mm-sized implants. By combining rectification and regulation in a single stage, and controlling this stage via a hybrid pulse-width modulation (PWM) and pulse-frequency modulation (PFM) feedback scheme, the IR^3 avoids efficiency-limiting cascaded losses while enabling tight voltage regulation with low drop out and ripple. The IR^3 is implemented in 0.078 mm^2 of active area in 180 nm SOI CMOS, and achieves a 1.87% $\Delta V_{DD}/V_{DD}$ power supply regulation ratio with a 1 nF decoupling capacitor despite a ten-fold load current variation from 8 μA to 80 μA. A 0.8 V V_{DD} is maintained at a 8 kΩ load for 144 MHz RF inputs ranging from 0.98 to 1.5 V. At 1 V regulation, the voltage conversion efficiency is greater than 92% with less than 5.2 mVpp ripple, while the power conversion efficiency is 54%. The measured overall wireless power transfer system efficiency (WSE), from the primary coil to V_{DD} output of the IR^3, is 2% at 160 μW load, and reaches 5% at 700 μW.

In chapter 4, an adaptive buck-boost resonant regulating rectifier (B^2R^3) with an integrated on-chip coil and low-loss H-Tree power/signal distribution is presented for efficient and robust wireless power transfer (WPT) over a wide range of input and load conditions. The B^2R^3 integrated on a 9 mm^2 chip powers integrated neural interfacing circuits as a load, with a TX-load power conversion efficiency of 2.64% at 10 mm distance, resulting in a WPT system efficiency FoM of 102.

Chapter 5 presents a 16-channel neural recording ADC array with predictive digital autoranging (PDA) in 65nm CMOS. PDA offers a 22dB increase in SNDR and 30× improvement in bandwidth, resulting in 92dB dynamic range at 0.8V supply and faster than 1ms recovery to 100mV input differential transient artifacts. Noise is <1μVrms over DC-500Hz bandwidth at 32kHz chopping and 1μA supply current. Noise efficiency factor of the combined front-end amplifier and ADC is

1.81, offering a record 2.6 power efficiency factor. Area per channel is 0.024mm^2.

A 4-channel multi-input multi-output (MIMO) complex baseband receiver for spectrum and space aware cognitive radio applications is presented in Chapter 6. The MIMO baseband receiver comprises a capacitive harmonic rejection down-converting mixer (HRM) receiver and a signal separation multi-input multi-output analog core (MAC) on a single integrated circuit. The HRM receiver performs frequency selection of the incoming RF signals by programmable spectral down-conversion and filtering with minimal harmonic folding. The subsequent MAC separates the spectrally overlapping but spatially diverse signals by weighted complex matrix multiplication. The entire signal path is implemented using energy-efficient g_{m}-C analog circuits with digitally controlled capacitive weighting for configurable baseband down/up-conversion ranging from -24 MHz to +24 MHz in the HRM, and programmable spatial filtering with 4×4 complex (8×8 real) 14-bit coefficients in the MAC. Measurements demonstrate greater than 65 dB harmonic folding rejection by the HRM, and greater than 48.5 dB spatial signal separation by the MAC. The 65 nm CMOS IC occupies 3.27 mm^2 active area, and consumes 480 μW digital power at 45 MHz LO and 840 μW analog power at 3 MHz baseband from a 1.2 V supply.

Chapter 7 presents a low-power high-linearity capacitive harmonic rejection mixer for cognitive radio applications. A passive mixer first receiver with capacitive 16-phase sinusoidal weighting implements harmonic rejection down-conversion, and an AC-coupled fully differential capacitor feedback transimpedance amplifier provides baseband linear voltage gain and band-pass filtering achieving an in-band IIP3 of +12.5 dBm at 320 MHz LO over 3 MHz baseband. The 1.62mm^2 mixer in 65nm CMOS consumes 40 μW per I/Q complex output channel, and 7.82 mW for 16-phase PLL clock generation and distribution.

Finally, Chapter 8 offers concluding remarks on the advances contributed in this thesis, their significance, and directions for future research.

Chapter 2

Design of Miniaturized Wireless Power Receivers for mm-sized Implants

2.1 Introduction

Miniaturization of implants to millimeter dimensions as illustrated in Fig. 2.1 opens up new possibilities to long-lasting, robust, and information-rich brain-machine interface (BMI) technologies. BMI technologies with current implantable devices offering limited operation time (months to a year) have proven their potential. For instance, recent BMI research successfully demonstrates recovery from spinal cord injuries [7]. Thus, there is a great interest in the medical community for the development of long-term and unobtrusive BMIs to enable quality of life improvements for patients suffering from debilitating conditions. Miniature implants overcome a major obstacle to the longevity of BMI technologies, as reduced micro-motions result in less astroglial scarring, and cell death [32, 48, 58, 69]. In addition, miniature implants can be modularly deployed to extend their coverage to the entire cortical surface while maintaining high spatial resolution [23, 62].

The biggest component by volume in conventional implants is typically the battery. Ideally, the total size of an implant for BMI should be mainly limited by

the physical requirements of the sensor and functional electronics rather than that of the energy source. Therefore, bulky batteries are not an acceptable solution to power implants for BMI. Wireless power transfer (WPT) offers a viable alternative to battery power, by enabling drastic miniaturization and extended life time of the implant [50].

However, miniaturization to mm dimensions is still challenging because a plurality of up-to-date current WPT techniques still rely on bulky external power receiving (RX) coils and energy-storage decoupling capacitors. Thus, implementation of WPT with a small form factor for mm-sized implants persists as an unresolved issue. Ultimate miniaturization can be truly enabled by integrating those external bulky components into an free-floating on-chip wireless power receiver.

This paper reviews two major WPT modalities for mm-sized implants in Sec. 2.2, and discusses main design considerations for fully integrated wireless power receivers in Sec. 2.3. In Sec. 2.4, two state-of-the-art regulating rectifiers applicable to miniaturized wireless power receiver with an on-chip coil are presented with measurement results, followed by a performance comparison and conclusions in Sec. 2.5.

2.2 Wireless Power Transfer Modalities for Miniaturized Implants

Two different WPT modalities have been widely investigated for mm-sized implants: WPT using either electromagnetic or ultrasound waves. Baseline mechanisms, advantages and disadvantages are discussed for each of these two modalities in the following section.

2.2.1 Ultrasonic Wireless Power Transfer

For ultrasonic WPT, power transmitting (TX) and receiving (RX) parts are implemented with piezoelectric transducers for conversion between electrical and acoustic energy. On the TX side, electrical energy is converted to a pres-

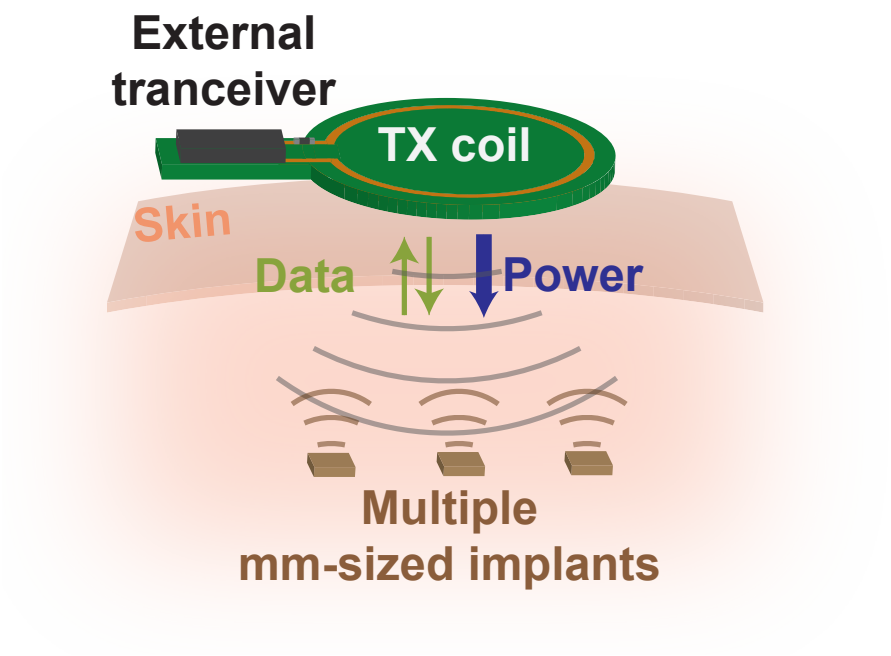

Figure 2.1: Wireless power transfer and bi-directional data communication with multiple mm-sized implants served by a single external transceiver.

sure wave, which is then transcutaneously transmitted to the RX side (implants) through the media. The RX transducer converts part of the received acoustic energy back to electrical form [67]. Owing to relatively slow speed of propagation ($\approx$ 1540 m/s in human soft-tissue), ultrasound offers a wavelength comparable ($\approx$ 1.5 mm at 1 MHz of operating frequency) to the mm-sized implant dimensions. The matched wavelength and implant dimensions allow for focal power delivery resulting in efficient coupling efficiency [59]. Correspondingly, recent studies successfully demonstrated ultrasonic WPT delivery of up to 100 μW to mm-sized implants at cm-range separation between TX and RX as shown in Fig. 2.2 (a) [79] and (b) [11].

Despite great advantages, applications of ultrasonic WPT to implants are limited. As the ultrasonic pressure wave travels toward the implant, it traverses several layers of tissue with substantial differences in acoustic impedances. Crossing tissue boundaries causes reflections of the pressure wave proportional in amplitude to the degree of acoustic impedance mismatch. While such reflections are highly beneficial as the key principle in ultrasonographic imaging, they deteriorate

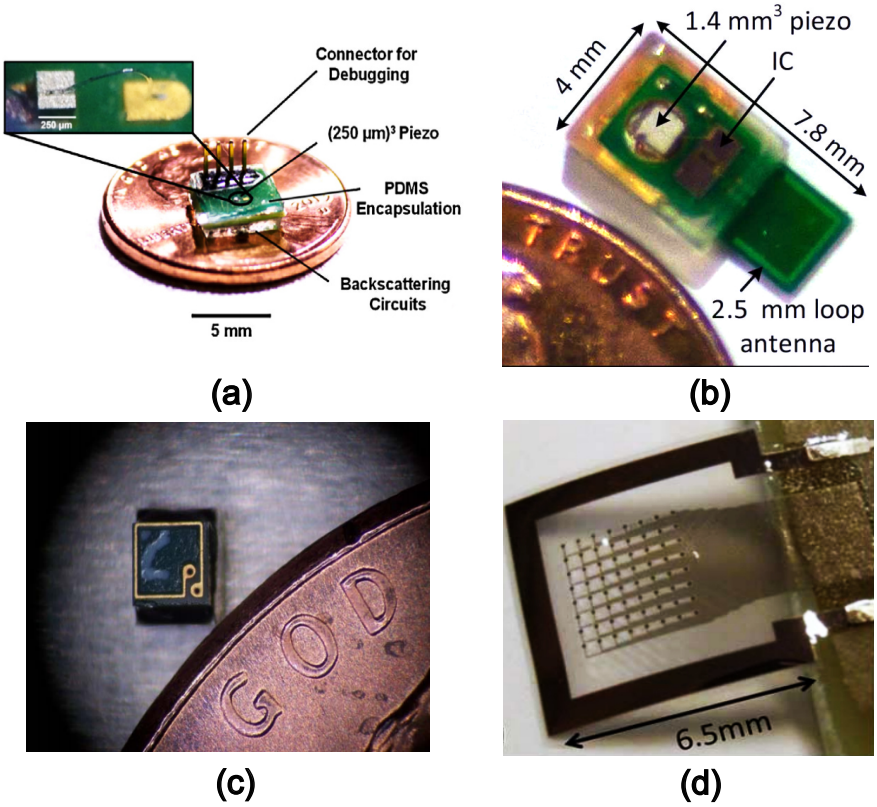

Figure 2.2: Example mm-sized implants with ultrasonic and electromagnetic WPT modalities. Ultrasonic WPTs with: (a) 250 μm^3 piezo transducer and backscattering circuits composing of several discrete components [79]; and (b) a 1.4 mm^3 piezo transducer, a 1 mm $\times$ 2 mm chip, and a 2.5 mm $\times$ 2.5 mm off-chip RF antenna for data communication [11]. Electromagnetic WPTs with: (c) 1 mm $\times$ 1 mm 535 MHz RX coil connected to the same size CMOS IC beneath [56]; and (d) 6.5 mm $\times$ 6.5 mm 300 MHz RX coil and 64 channel electrode array [62].

the energy coupling efficiency in WTP applications. For example, the acoustic impedance of skull is more than 4.6 times greater than that of adjacent soft tissue layers, causing a pressure reflection ratio of 0.64, and resulting in less than 2% of the incident power making it across towards a transcranial implant [18, 90]. As such, ultrasonic WPT is only effective for powering implants where there is little to negligible acoustic impedance mismatch in the path from TX to the implant. The reach of ultrasonic WPT could however be extended, in principle, by inserting repeaters at impedance mismatch boundaries. For instance, to avoid the huge power

losses due to skull reflection, a WPT hub sub-cranial interrogator can be inserted under the skull combining electromagnetic WPT to an external transceiver above, with ultrasonic WPT to mm-sized implants underneath [79]. Typical currently achievable transfer efficiencies from WPT interrogators to mm-sized implants at cm-range distances are less than 0.1 % due in part to severe size limits in both piezo transducers. In addition to power delivery, data communication via ultrasound has a limited data rate due to its relatively low operating frequency ($\leq$ 10 MHz). To improve up-link (from implants to external transceiver) data rates to several Mbps, 4 GHz ultra-wideband (UWB) RF communication has been employed with an additional PCB loop antenna [11].

It is worth mentioning also that most of current state-of-the-art ultrasonic WPTs employ lead zirconate titanate (PZT) which offers high transfer efficiency owing to its superior electromechanical coupling coefficient compared to other piezo-materials. Unfortunately, PZT components included in implants pose significant health risks of long-term lead exposure inside the human body. These and other current challenges of ultrasonic WPT will likely be overcome with future research advances in materials and integrated circuit design.

2.2.2 Electromagnetic Wireless Power Transfer

Electromagnetic (EM) WPT is currently most commonly adopted with mm-sized implants. EM WPT requires TX and RX coils to be inductively coupled through matching resonant tanks for wireless power delivery. Due to the miniature size of the implant, the tank resonance condition requires the addition of lumped capacitance to the coil inductance, requiring careful sizing considerations. The TX coil produces a time varying magnetic flux, which is shared with the RX coil where an electromotive force (EMF) is generated. Since the EMF is directly proportional to the area of RX coil by Faraday's law of induction, the size of the RX coil often dominates the size of implants for better WPT performance. The challenge with miniaturized implants is then to minimize the size of the RX coil without greatly compromising WPT performance. A common strategy is to increase the operating frequency of the implant resonant tank, which increases induction via higher time-

varying rate of magnetic flux, and increases quality (Q) factors of both TX and RX coils. A higher operating frequency, however, also increases tissue absorption of the incident electromagnetic radiation, and thus reduces the maximum transmittable power to the implant under the regulations of Specific Absorption Rate (SAR). As such, by balancing both effects, operating frequencies from 100 MHz to 1 GHz have proven optimal for EM WPT to mm-sized implants. [1, 56, 57, 62, 66, 70]. Examples of mm-sized implants utilizing EM WPT operating in this range of resonant frequencies are shown in Fig. 2.2 (c) and (d).

Operating frequencies above 100 MHz open up the possibility of full integration of the RX coil directly on chip with a standard CMOS process. This integration offers significant advantages to mm-sized implants: *i)* ultimate miniaturization of implants by eliminating the space previously occupied by the RX coil, *ii)* no special fabrication process is needed to implement a RX coil, *iii)* greatly simplified encapsulation via removing any lines and connectors between the RX coil to the electronics, and *iv)* reduced parasitic capacitance and resistance between the RX coil and its fully integrated matching network (thereby eliminate additional power loss) [36, 42, 94, 95]. Therefore, integration of RX coil on-chip is a significant step toward free-floating miniaturized implants.

2.3 Design Considerations for Fully Integrated Inductive Wireless Power Receivers

While implementing an on-chip coil offers various advantages, it requires careful design of the wireless power receiver to optimize the WPT system efficiency (WSE), defined as the ratio of RX power delivered to the load to the TX transmitted power. WSE is an overall measure accounting for several factors in the WPT system, including two important factors on the implant side: the efficiency of the TX-RX inductive link, and the efficiency of RX RF-to-DC conversion. These two factors are described in turn in the following sections, with a figure-of-merit account of overall WSE for comparison with the state-of-the-art in Sec. 2.4.3.

2.3.1 RX Coil Design

The maximum achievable TX-RX link efficiency, and hence WSE, depends strongly on the coupling coefficient k. To first order, the coupling coefficient k depends on coil geometry and separation distance between TX and RX coil, which are mostly given by the application [78]. Controllable design parameters in maximizing WSE are mainly the Q factors of TX and RX coils, both of which should be maximized. Optimal design of the on-chip RX coil is of paramount importance since the Q of the RX coil is limited more stringently compared to that of TX coil [1].

As a guiding principle, the on-chip RX coil is implemented with thick top-layer metal at the chip boundaries to maximize its area (for better coupling coefficient, k) and to minimize its parasitic resistance (for higher Q factor) and parasitic capacitance to substrate (for minimum losses and higher self-resonance frequency).

The number of turns of the RX coil critically affects its Q factor. At a given resonant frequency, a higher number of turns leads to a larger coil inductance and smaller matching capacitance of the LC tank. To first order, the inductance of the coil is proportional to the square of the number of turns while parasitic series resistance increases with the number of turns. As such, Q tends to increase with number of turns at certain frequency range. If large number of metal stacks are supported in the process, then series connections of two or three top-layer metal lines can be used to increase the effective number of turns within the space constraints [95]. Likewise, multiple metal layers in parallel can reduce sheet resistance of the RX coil to improve Q factor.

At large number of turns or at higher frequencies, however, Q tends to decrease rather than increase with the number of turns because the increased parasitic capacitance results in a lower self-resonance frequency. Furthermore, a many-turn coil offers larger voltage swing but limited current driving capability at the LC tank. This induces circuit design difficulties where the load implied by the implant circuits draws sparse but instantly large current out of the LC tank, such as for electrical stimulation. Supply voltage generation at the rectifier and regulator may then fail due to significant voltage drop at the LC tank. Resonance with a

smaller matching capacitor is also more vulnerable to any parasitic capacitance and fabrication mismatch.

In summary, designs with larger numbers of turns for the RX coil offer greater Q for greater WSE, but at the expense of vulnerabilities to parasitics. In practice, for typical mm-sized implants operating between 100 MHz and 300 MHz, between 2 and 4 turns are appropriate.

2.3.2 Power and Signal Distribution

One additional challenge in fully integrated WPT receivers arises due to the proximity of active electronics to the receiving coil. Eddy currents induced by the alternating magnetic field affect significant energy losses limiting the Q of the RF coil, and further affect the functioning of sensitive analog circuits in the implant. Eddy currents in the silicon substrate can be minimized by adopting a silicon-on-insulator (SOI) process; however eddy currents in metal layers potentially pose a more significant problem, requiring to pay extreme attention on metal routing near the coil.

In particular it is critically important to avoid any metal loops in the design and layout of all circuits in the implant chip. The main culprits in generating Q-reducing loops and large metal planes are often power and signal lines distributed across the entire chip such as ESD power supply lines connected to all pads or chip guard-ring metal, and congregated decoupling capacitors (decaps). These loops and metal planes induce eddy currents reducing Q factor of the RX coil by over 60% (thereby reducing WPT efficiency), while also introducing noise to sensitive circuits and a signal distribution network. To avoid large metal planes on-chip, [94] reduced decaps to only 20 pF through inclusion of a high-performance but high-power linear regulator on the wireless power receiver. A fractal H-tree power and signal distribution network with distributed decaps shown in Fig. 2.3 (a) is a practical solution to systematically remove all loops and large planes from the wireless power receiver [42]. This H-tree topology furthermore serves as a network backbone for eliminating differential mode interference in sensitive analog differential signals by ensuring equidistant signal paths. HFSS simulation and

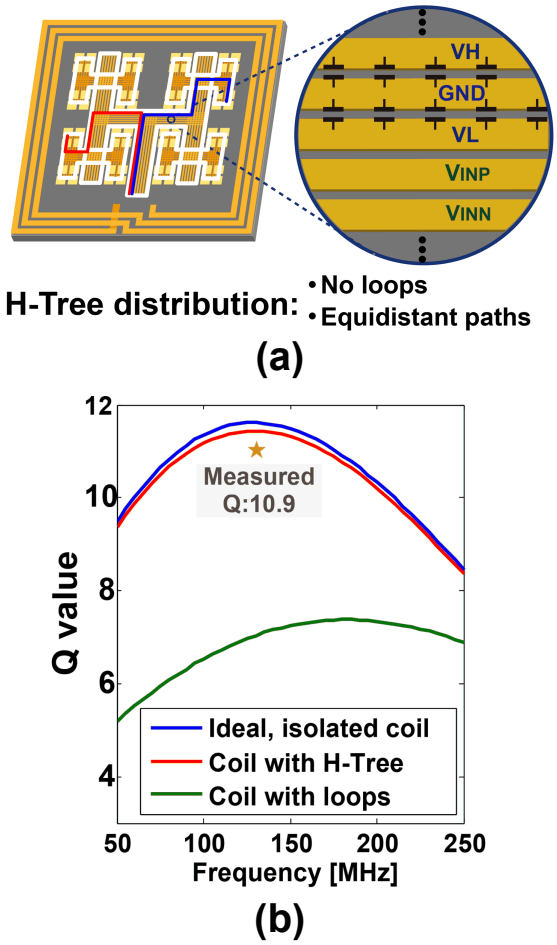

Figure 2.3: Power and signal distribution for minimal RF interference in fully integrated mm-sized WPT. (a) Fractal low-loss H-Tree power and signal distribution network with energy-storage decoupling capacitors without loops and with equidistant signal paths (red and blue lines), and (b) simulated and measured Q factor of the RX coil [42].

measurement in Fig. 2.3 (b) show negligible loss in Q compared to an ideal, isolated coil, such that most of the incident RF energy directly couples to the RX coil rather than the metal traces cohabiting the chip. Hence, with H-tree power and signal distribution on a wireless power receiver, WSE is maximized while also decoupling RF interference.

2.4 RF-DC conversion: Regulating Rectifiers

An integrated regulating rectifier accomplishes simultaneous rectification of the RF input and regulation of the DC, in a single step. As such, it improves power conversion efficiency (PCE) and voltage conversion efficiency (VCE) by eliminating losses in a separate regulation step. For regulation, a standalone low-drop-out (LDO) is commonly employed, which often is the most power consuming block [11] and [56]. The following section presents two example designs of regulating rectifiers operating with on-chip RX coil for mm-sized implants, along with a comparison with the state-of-the-art.

2.4.1 Integrated Resonant Regulating Rectifier

A CMOS fully-integrated resonant regulating rectifier (IR^3) for inductive power telemetry in mm-sized implantable devices was presented in [36]. To counter disadvantages of cascaded two-stage conversion, a fully integrated solution to combined rectification and regulation directly coupling the on-chip resonant tank to the on-chip load, by hybrid pulse-width modulation (PWM) and pulse-frequency modulation (PFM) of the conductive path between the tank and the load as illustrated in Fig. 3.3 (a) was proposed for IR^3. Each pulse activates a conductive path between the resonant tank and the load, accomplishing both rectification and regulation in one step. For rectification, the pulse generator in Fig. 3.3 (a) activates the up-rectifying power PMOS transistor M_{PU} by lowering V_{GU} when its RF input, V_{UP}, exceeds V_{DD}. Conversely, the down-rectifying power PMOS transistor M_{PD} is activated by lowering V_{GD} when its RF input, V_{DN}, exceeds V_{DD} in the opposite RF phase for full-wave rectification. For regulation, the width of the activation pulse is controlled by PWM through analog feedback, and its pulse frequency is controlled by PFM through digital feedback.

The PWM module regulates V_{DD} simultaneously with rectification, by adjusting the pulse-width based on error accumulation between V_{SEN} (divided from V_{DD}) and a predefined reference voltage, V_{REF} shown in Fig. 3.3 (b). The PWM offers accurate regulation of V_{DD} since large loop gain analog feedback rejects static

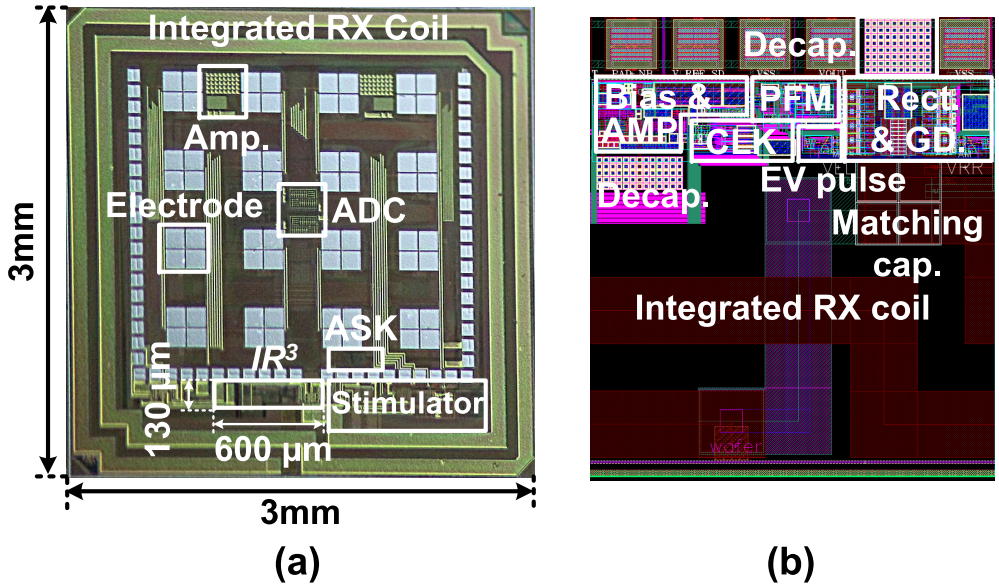

Figure 2.4: (a) Microphotograph of a fully-integrated resonant regulating rectifier (IR^3) for inductive wireless power telemetry in mm-sized implantable devices, and (b) detailed layout of IR^3 [36].

error in inputs of an error integrator, A_{ERR}, by error integration. However, due to compensation with C_D,R_Z, and C_{ND} for stability of the analog feedback loop, response time of PWM analog feedback is relatively slow, in the range of several hundred microseconds. In addition, narrow pulse widths prohibit the IR^3 from achieving high PCE at light load conditions. As such, PWM alone is insufficient for accurate and efficient regulation.

To address these challenges and provide rapid digital feedback, another PFM regulation loop is included in addition to and in tandem with PWM. The PFM module increases the pulse frequency of V_{GU} and V_{GD} when either pulse width being regulated by PWM reaches an upper threshold; conversely, the pulse frequency is decreased when either pulse width reaches a lower threshold. As such, PFM together with PWM provides broad-range and rapid regulation and improved power conversion efficiency at light load conditions. A power-on-reset generates an INIT signal forcing the IR^3 into passive mode with diode-connected PMOS transistors and initializing digital state variables in the PFM module during start-up [50].

A microphotograph of the mm-sized implantable system powered by the IR^3 and detailed layout of the IR^3 are shown in Fig. 2.4 (a) and (b), respectively. The active area of the IR^3 design is 0.078 mm^2 in 180 nm 1P4M SOI CMOS. An on-chip RX coil is implemented at the chip edge so as to maximize its area with two turn top metal for 23.7 nH inductance. Metal width of the coil is 100 μM for a small series resistance, R_{coil}, rendering around 12 of Q_{coil} with *HFSS* electromagnetic simulation. The IR^3 is located right after matching capacitor to reduce any possible parasitics.

2.4.2 Adaptive Buck-Boost Resonant Regulating Rectifier

The IR^3 has demonstrated complete on-chip integration of a regulating rectifier. For further improvement in robustness to wide RF input voltage range coming from link variations, a buck-boost resonant regulating rectifier (B^2R^3) was presented in [42] and is described in detail in 2.4. The presented B^2R^3 accomplishes regulated rectification over wide input range through a mode arbiter that adapts to the sensed RF envelope, as illustrated in Fig. 4.6 (a). BOOST mode converts low RF voltage to larger regulated DC voltage, while BUCK1,2,3 modes efficiently convert larger RF voltage down. For smooth transition between modes, a combined BUCK-BOOST mode operates at an intermediate region. The B^2R^3 produces dual supply voltage, VH and VL, and is composed of boost and buck regulating rectifiers, a feedback part, and a distributed decoupling capacitors for each power supply and a shared block of mode arbiter for both supply voltages.

A microphotograph of the 3 mm $\times$ 3 mm sized implantable wireless power receiver and detailed layout of the power-management blocks, B^2R^3, are shown in Fig. 2.5 (a) and (b), respectively. A three-turn on-chip RX coil is integrated with the top metal routing in 180 CMOS SOI process offering 60.3 nH of inductance with 10.9 of Q factor. Active area of B^2R^3 is 0.194 mm^2, which is slightly larger than that of the IR^3 in Sec. 2.4.1 due largely to the area of mode arbiter and boost regulating rectifier. Owing to these extra blocks for mode adaptation, the B^2R^3 produces regulated output voltages even under highly dynamic input conditions such as 50 % amplitude variation in PA input, as shown in Fig. 4.12 (a) and (b). This

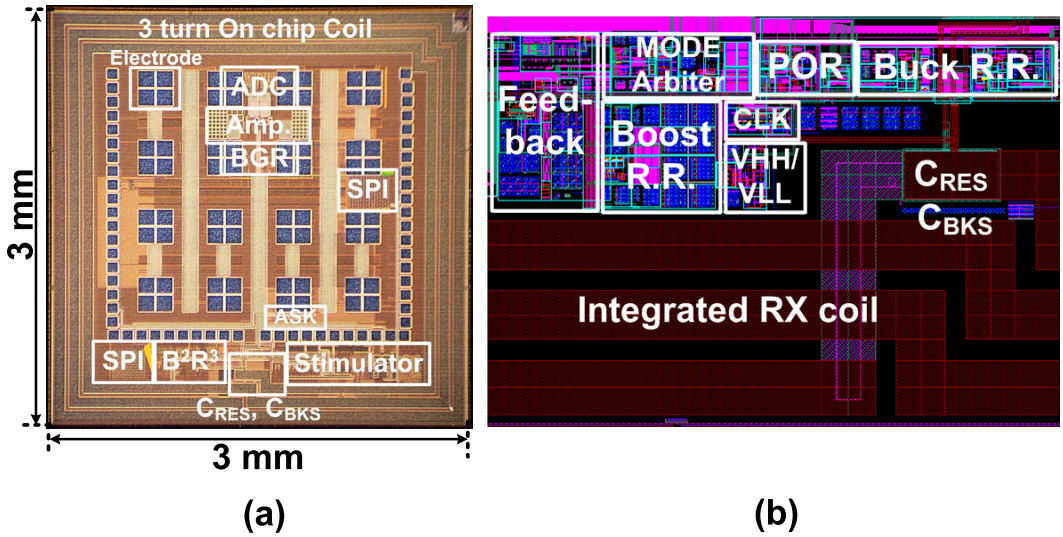

Figure 2.5: (a) Microphotograph of a 3 mm × 3 mm implantable WPT system with adaptive buck-boost resonant regulating rectifier (B^2R^3) and low-loss H-Tree power and signal distribution, and (b) detailed layout of B^2R^3. Active silicon area for B^2R^3 is 0.194 mm^2 [42].

mode adaptation is important since the RF input power can vary substantially for a number of reasons such as variations in link distance, alignment, and impedance.

2.4.3 Comparison with state-of-the-art designs

Table 2.1 summarizes key performance measures in comparison with the state of the art. The table shows IR^3 and B^2R^3 are the only fully integrated mm-sized WPT receivers with regulating rectifier for one-step power conversion at higher than 100 MHz resonant frequency. It is important to note that link efficiency from TX coil to RX coil is inversely proportional to the cube of the distance between TX and RX coils [70] and the cube of the square root of the area of RX coil [95] for the case of mm-sized RX coil. For a fair comparison to the state-of-the-art designs, normalizing for TX-RX distances (typically ranging 5-15 mm), and for RX diameters (typically ranging 1-8 mm), a figure-of-merit (FoM) was proposed by [95]. However, this FoM takes only link efficiency from TX to RX coil into account. Hence, an adjusted FoM that accounts for full WPT system efficiency (WSE) from TX coil to regulated DC rather than WPT link efficiency

Table 2.1: Performance Comparison

	Seo JNM15	Charthad JSSC15	Muller JSSC15	Zargham TBCAS15	Mark VLSI11	O'Driscoll ISSCC09	Kim VLSI15	Kim VLSI16
WPT method	ultrasonic	ultrasonic	EM	EM	EM	EM	EM	EM
Dimension (mm^2)	5.06	31.2	43.97	4.84[a]	1[a]	4.37[a]	9	9
Operating Freq. (MHz)	6.1	1	300	160	535	915	144	144
Power RX/ dimension /location (Value (nH))	PZT/ 0.015 mm^3 /off-chip	PZT/ 1.4 mm^3 /off-chip	Coil/ 42.25 mm^2 /off-chip (32)	Coil/ 4.36 mm^2 /on-chip (130)	Coil/ 1 mm^2 /off-chip (5.73)	Coil/ 4 mm^2 /off-chip (N.R.)	Coil/ 8.64 mm^2 /on-chip (23.7)	Coil/ 8.74 mm^2 /on-chip (60.3)
Regulator	Not needed	separate LDO	separate LDO	separate LDO	separate LDO	separate LDO	regulating rectifier	regulating rectifier
Dec. Cap (nF)	Not needed	3.3	4	0.02	1.39	N/R	1	0.25
Process	Discrete	65 nm CMOS	65 nm CMOS	0.13 µm CMOS	65 nm CMOS	0.13 µm CMOS	0.18 µm CMOS SOI	0.18 µm CMOS SOI
WSE* (%)	< 0.1[b]	N/R	1.19[b]	0.62[c]	0.02 (-37 dB)	0.048 (-33.2 dB)	2.04	2.64
Distance (mm)	30	30	12.5	10	13	15	10	10
WSE FoM**	Not applicable	Not applicable	8.46	68.1	43.94	20.25	80.3	102.1

[a]not include data communication

[b]TX PZT transducer to RX PZT transducer

[c]estimated from provided data, TX PW: 13mW, P_{DC_LOAD}: 0.160mW

[d]estimated from provided data, estimated η_{LDO}: 68 % (V_{DD}: 3.1 V, V_{REC2}: 4.5 V), η from TX to the rectifier: 0.9 %

*WSE = WPT system efficiency (from TX to regulated DC)

**WPT System Efficiency FoM = $\frac{\eta_{overall} \times D^3}{A^{1.5}}$, where $\eta_{overall}$ is TX-regulated DC efficiency;

D is distance between TX-RX coils; and A is area of the RX coil.

was proposed in [42]:

$$\text{WPT system efficiency FoM} = \frac{\text{WPT system efficiency} \times D^3}{A^{1.5}} \tag{2.1}$$

where D is the distance between two TX and RX coils, and A is the area of the RX coil (outer dimension) [42]. The two presented regulating rectifiers in Secs. 2.4.1 and 2.4.2 offer WSE FoM of 80.3 and 102.1, respectively.

2.5 Conclusion

Miniaturization of implants enables long-term and robust BMI technologies by improving their longevity, safety, and high spatial resolution. This review highlighted two major WPT methods for mm-sized implants: ultrasonic WPT and

electromagnetic WPT. While ultrasonic WPT offers advantages particularly for sub-mm implants, electromagnetic WPT is superior for BMI applications, as it is better suited for transcranial transmission and can support higher data rates. Critical design considerations for optimal integration of RX coils on-chip include sizing and number of turns of the coil, and H-tree power and signal distribution. Two example designs for regulating rectifiers operating as fully integrated wireless power receivers were presented with high WPT system efficiency figure-of-merit. As a significant advancement in miniaturization, fully integrated wireless power receivers enable next-generation modular mm-sized wireless implants. On-going and future research directions include closed-loop communication between external beamforming transceiver and distributed modular implants [41, 80].

Acknowledgments

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C. Kim, S. Ha, A. Akinin, J. Park, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs conceived and contributed these works. C. Kim wrote the first draft of the paper. S. Ha, A. Akinin, J. Park, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs extensively contributed to edit the paper.

Chapter 3

A 144 MHz Fully Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation for mm-sized Implants

3.1 Introduction

Miniaturized, highly energy-efficient wireless power transfer (WPT) integrated circuits are critical components in the development of fully-encapsulated implanted brain-computer interface systems that will, through additional advances in improved spatial resolution and coverage of neural recording and stimulation electrodes, enable next-generation neuroscience and neurology experimentation. As an example, modular mm-sized wireless implants which lie directly on the cortical surface, as illustrated in Fig. 3.1, can support more accurate recording of local brainwaves and a higher spatial resolution ($\leq$ 1 mm) than conventional electrocorticography (ECoG) approaches [23, 62]. In addition to spatial coverage and density benefits, recent studies have suggested that small devices can reduce incidence of tissue inflammation, astroglial scarring, and cell death [1, 32, 48, 58], thereby underscoring the need to miniaturize implants.

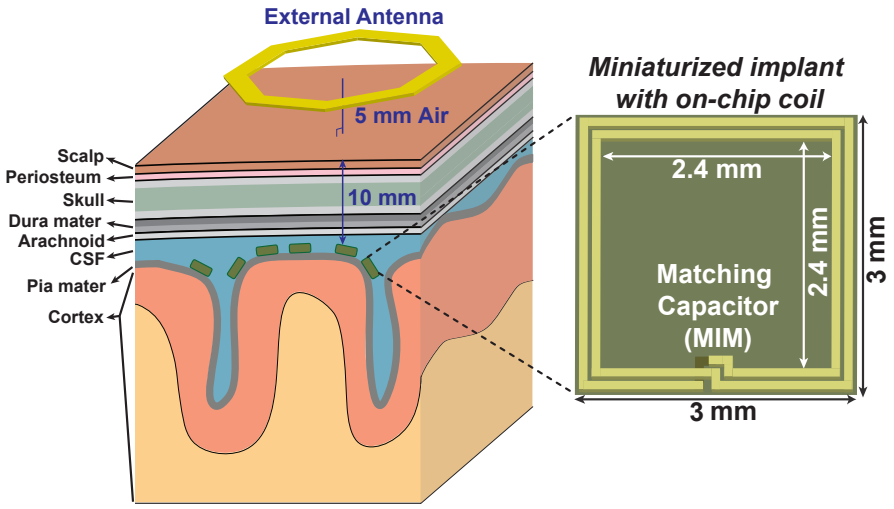


Figure 3.1: Transcutaneous wireless power delivery to mm-sized distributed implants on the cortical surface, each with an integrated power receiving coil.

Since the size of miniaturized implanted devices are often limited by the size of the embedded WPT coil and corresponding power management and energy-storage circuitry, significant research efforts have been directed at reducing the size of such components. For example, it has been shown that increasing the RF carrier frequency used for WPT can yield a reduction in receiver size [53, 55–57, 66], since a higher resonant frequency: *i)* increases induction via a higher rate of incident magnetic flux over a small receiving coil [70, 95], *ii)* increases the quality factor (Q) of both power transmitting (TX) and receiving (RX) coils [1, 95], and *iii)* reduces the area required of the resonant matching capacitor.

On the other hand, tissue absorption of electromagnetic waves increases with frequency, resulting in additional tissue losses that ultimately limit the efficiency of WPT. Making matters worse, increased tissue absorption also limits the amount of allowable transmit power due to regulations on the Specific Absorption Rate (SAR) of RF power in human tissue. Balancing of these considerations leads to optimal resonant frequencies in the 100 MHz–1 GHz range under various conditions, enabling the design of mm-sized implants that can efficiently receive sufficient power to operate load circuits under SAR constraints [1, 70, 71, 93, 95].

The pursuit of implant miniaturization also requires research on miniatur-

izing the rest of the power management and energy storage circuitry. For example, most conventional wirelessly-powered implants utilize a segmented architecture, where the WPT coil is physically separated from the rectifying and regulating circuits. Such an approach requires complex interconnect, packaging, and discrete components that occupy unwanted volume and increase cost [95].

To address these issues and enable further miniaturization of wirelessly-powered implants, this work presents the design of a fully-integrated resonant regulating rectifier (IR^3) that performs voltage and power conversion from an integrated 3 mm $\times$ 3 mm on-chip coil to loads; no external components are required for operation. By combining rectification and regulation into a single stage, as illustrated in Fig. 3.2 (b), the proposed IR^3 eliminates the conventionally-required inter-stage decoupling capacitance, saving significant volume and eliminating cascaded losses for high efficiency. A hybrid pulse modulation control scheme is also proposed to enable power efficient rectification and regulation over a large range of RF input amplitude and load current.

Simplified circuit schematics and initial measurement results of the IR^3 were presented in [36]. This paper presents analysis and optimization of system-level parameters, significantly more detailed circuit schematics, and measurements and characterization of IR^3 performance under varying input and load conditions. This paper is organized as follows: limitations of conventional segmented architectures motivating the integration of resonant rectification and regulation are discussed in Section 3.2. The proposed operation of IR^3 with hybrid pulse frequency and width modulation is outlined in Section 3.3, with circuit details elaborated in Section 3.4, and simulated and measured results presented in Section 3.6. Finally, conclusions are given in Section 3.7.

3.2 Architectural Considerations

The purpose of this section is to show that performing combined rectification and regulation with an integrated coil is not only advantageous from a size perspective, but that merging these two functions into a single stage has tangible

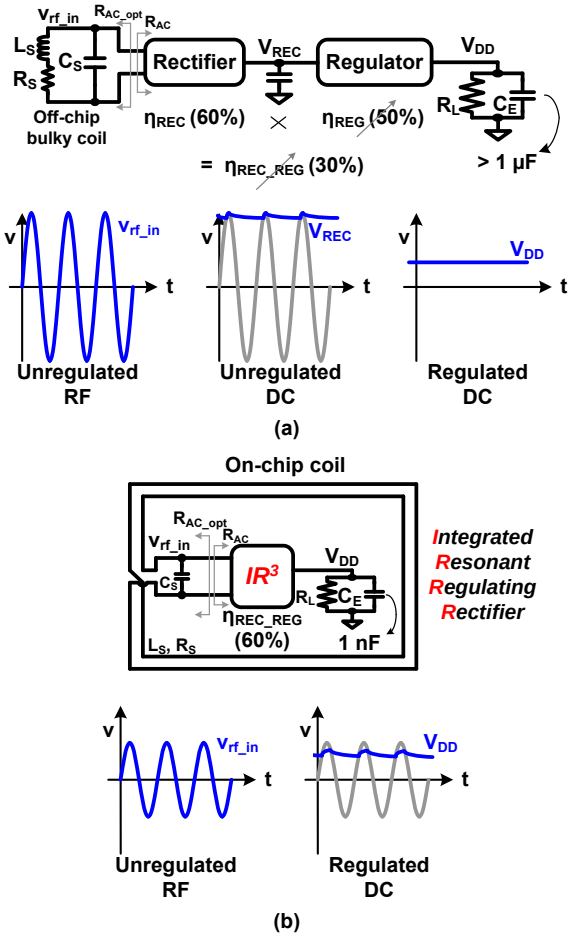


Figure 3.2: Integration of rectification and regulation for one-step conversion without cascaded loss in PCE and VCE.

system-level efficiency benefits. To demonstrate this, we first show that to maximize overall system efficiency in mm-sized systems, it is necessary to maximize not only PCE, but also VCE. Then, we show how maximizing both VCE and PCE in conventional cascaded systems is difficult, while attaining high efficiency can be more easily achieved by merging rectification and regulation.

3.2.1 Importance of Voltage and Power Conversion Efficiency

The wireless power transfer system efficiency (WSE, the net power gain from the transmitted power at the TX coil to the RX load after the regulation)

and the magnitude of power delivery to the load are limited by the size of the RX coil [70,95]. Furthermore, in the case shown in Fig. 3.1 where multiple implants receive power from a single external power transmitter, it is infeasible to control the received power level at each implant individually by adjusting the shared transmitted power. As such, the spread in distances between the external transmitter and the implants (and thereby, the range of coupling coefficients) becomes an efficiency limiting factor. Therefore, particularly for multiple mm-sized WPT implants with on-chip coils, it is important to maximize both the WPT system efficiency and magnitude of delivered power.

It can be shown that, to a first order, maximum efficiency and maximum power in a WPT system, when operating at low coupling coefficients, k, are achieved at the same optimal load of the secondary LC tank, $R_{\text{AC\_opt}}$ [60]. Specifically:

$$R_{\text{AC\_opt}} \approx \frac{L_S}{C_S R_S} \approx Q_{\text{coil}}^2 R_S, \tag{3.1}$$

where L_S, C_S, and R_S are inductance and capacitance of the secondary LC tank, and the parasitic series resistance of the RX coil as shown in Fig. 3.2. Q_{coil} is $\omega_o L_S/R_S$ where $\omega_o \approx 1/\sqrt{L_S C_S}$ at the parallel tuned LC tank.

By a series-to-parallel impedance transformation [61,78], the output impedance of the parallel tuned LC tank is the same $R_{\text{AC\_opt}}$. Hence, both the efficiency and the amount of power are maximized through *impedance matching* between the receiver LC tank and the subsequent IR^3 circuitry. Several recent designs control matching capacitance or inductance in the secondary LC tank to adjust $R_{\text{AC\_opt}}$ according to Eqn. (3.1), either to improve power transfer efficiency [47,66] or to increase amount of power delivery [60]. These improvements come at the expense of some additional implant area and power loss due to the addition of series switches connecting to several separate capacitors in parallel or the inductor in series.

The IR^3 equivalent input resistance, R_{AC} shown in Fig. 3.2, can be found by relating the AC power consumption at its input $P_{in} = v_{\text{rf\_in\_peak}}^2 \,/\, 2R_{\text{AC}}$, where $v_{\text{rf\_in\_peak}}$ is the peak voltage in the secondary LC tank, to the output DC power $P_L = V_{\text{DD}}^2 \,/\, R_L$ delivered to a load with resistance R_L. In terms of the power conversion efficiency, PCE $= P_L/P_{in}$, and voltage conversion efficiency, VCE $=$

V_{DD} / $v_{\mathrm{rf\_in\_peak}}$ of the combined rectifier and regulator, this becomes:

$$R_{\mathrm{AC}} = \frac{\mathrm{PCE}}{2\mathrm{VCE}^2} R_L \,. \tag{3.2}$$

Eqn. (3.2), together with (3.1), underscore the importance of maintaining high VCE in maximizing overall WSE through impedance matching. Indeed, typical on-chip inductors with quality factor $Q_{\mathrm{coil}} = 12$ and series resistance $R_S = 3.5\ \Omega$ yield an optimal LC tank load $R_{\mathrm{AC\_opt}}$ roughly 500 Ω. In turn, a typical ECoG application [23,62] incurs a load $R_L = 2\ k\Omega$ at PCE = 0.5. Under these conditions, the equivalent input resistance R_{AC} (3.2) is perfectly matched to this optimal load when VCE = 1. Conversely, when VCE = 0.2, R_{AC} becomes 12.5 $k\Omega$, substantially off from the optimal load $R_{\mathrm{AC\_opt}}$. Hence, in general, mm-sized WPT receivers with less than 1 mW DC load require not only high PCE, but also high VCE.

3.2.2 Limitations of Conventional Cascaded Rectification and Regulation

Achieving both high PCE and high VCE is challenging with conventional WPT receivers which employ a cascaded two-step conversion approach: RF-DC rectification followed by DC regulation. For rectification, the simplest design is a passive rectifier built with diode-connected MOS transistors, although at low PCE and VCE due to an inherent V_{TH} voltage drop across the diodes. Alternatively, active rectifiers with high-speed comparators for active low-voltage diodes yield improved VCE, as well as PCE [50]. Both the passive and active rectifier operate, essentially, by tracking the envelope of the RF input and pulling up the output voltage whenever it is lower. As such, the rectified output tends to the peak voltage of the RF input *regardless of the required output voltage*. Hence, variations in the received RF input amplitude due to changes in coupling conditions (and thereby, coupling coefficient) between the TX and RX coils during movement require regulation of the rectified voltage for stable operation of the implant circuits. A conventional WPT receiver accomplishes this through a separate additional regulation stage. For this purpose, low-drop-out (LDO) regulators have been widely

adopted [56, 57, 62, 66, 94].

The separation between rectification and regulation functions incurs several inefficiencies as illustrated in Fig. 3.2 (a). To support this two-step conversion, two large supply-decoupling capacitors are required before and after regulation to reduce voltage ripple and improve regulation feedback stability. Full on-chip integration of two large capacitors in a mm-sized implant is prohibitive not only because of the large silicon area required, but also because of eddy currents induced by the RF magnetic field in large solid metal planes which substantially reduce WSE. High-speed LDO regulators permit lowering the size of the two decoupling capacitors [94], though this is achieved by increasing bandwidth of the LDO and therefore quiescent power consumption.

In addition, the cascaded rectification-regulation two-step conversion leads to multiplicative losses in conversion efficiencies: $\eta_{\mathrm{REC\_REG}} = \eta_{\mathrm{REC}} \times \eta_{\mathrm{REG}}$, both for VCE and PCE. This is particularly problematic with LDO linear regulators for which both the $\mathrm{VCE_{REG}}$ and $\mathrm{PCE_{REG}}$ are limited by the ratio of regulated to rectified voltage:

$$\mathrm{PCE_{REG}} \leq \mathrm{VCE_{REG}} = \frac{V_{\mathrm{DD}}}{V_{\mathrm{REC}}}, \tag{3.3}$$

which can be arbitrarily low depending on RF input conditions. In the case of a single implant, regulator efficiencies can be improved by dynamically adjusting the transmitted RF power at the external antenna to control V_{REC} slightly greater than V_{DD} [53, 55]. However, in the case of multiple implants as depicted in Fig. 3.1, the minimum level of transmitted RF power is is set by the weakest link (generally, the farthest implant from the external transmitting antenna). As a result, a uniformly high VCE and PCE cannot be guaranteed across all implants when using cascaded conversion with LDO linear regulators. Furthermore, it is important to note that the drop-out voltage ($V_{\mathrm{REC}} - V_{\mathrm{DD}}$) is generally greater than a few hundred mV and increases its portion as the supply voltage is scaled down [12]. As such, a LDO regulator is the most static power consuming block in several mm-sized implantable designs [11, 56].

3.3 Integrated Resonant Rectification and Regulation

To address the disadvantages of cascaded two-stage conversion, this paper proposes a fully integrated solution to combine rectification and regulation by directly coupling the on-chip resonant tank to the on-chip load via hybrid pulse width and frequency modulation of the conductive path between the tank and the load.

3.3.1 Benefits of Integration

Combination of rectification and regulation functions within a single stage offers greater integration density as well as high efficiencies [15, 17, 36, 51, 54]. For further improvement in size and efficiencies, the RX coil is also integrated on-chip such that the integrated resonant regulating rectifier (IR^3) presented here directly converts the induced RF power at the integrated coil to the regulated DC supply driving on-chip loads without cascaded losses in overall VCE and PCE, as illustrated in Fig. 3.2 (b). Hence, the IR^3 is capable of attaining high PCE and VCE not limited by the two-stage inefficiencies in (3.3). In particular, owing to improved overall VCE (greater than 90 %, Fig. 3.13) by combining two functions into a single stage, the equivalent input resistance of the IR^3, R_{AC}, is close to the optimal LC tank load, R_{AC_opt}, leading to improved overall WSE. While not implemented here, real-time R_{AC_opt} tracking functionality can be included with IR^3 for further improvement in overall WSE.

In addition to removing cascaded losses in efficiencies, full monolithic integration also reduces parasitic capacitance and inductance in the LC tank interfacing to the IR^3. To support full integration in an mm-sized implant, decoupling capacitance is reduced to 1 nF, which is adequate for regulation within 5 mV ripple (Fig. 3.11).

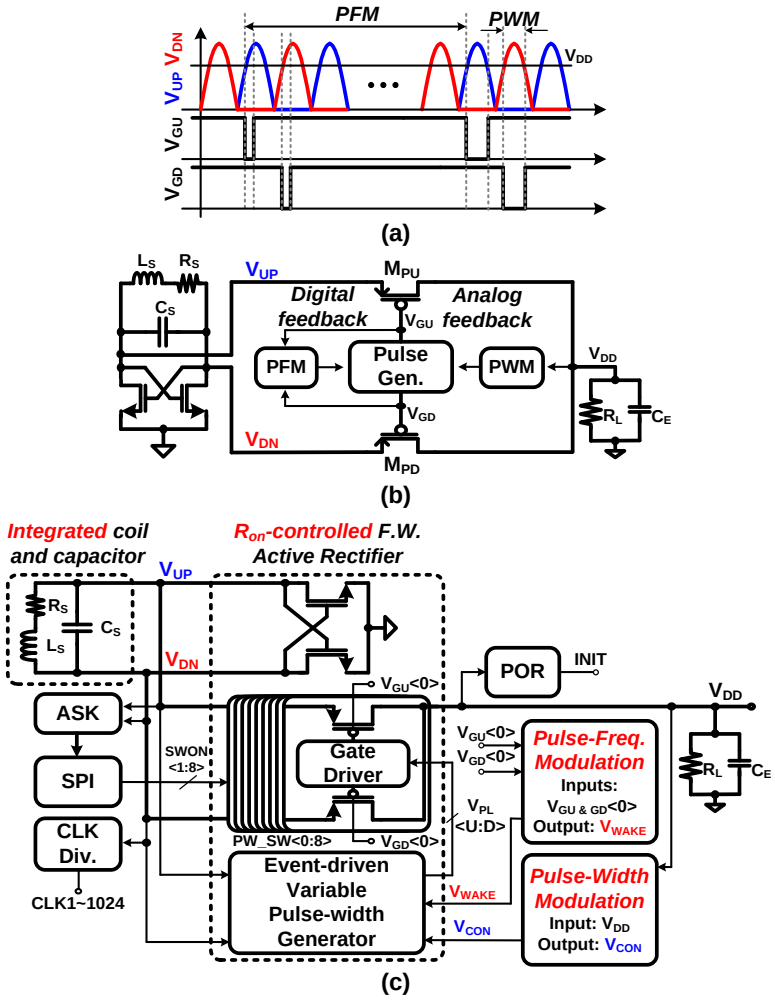


Figure 3.3: Hybrid pulse modulation (HPM) with combined pulse-width modulation (PWM) and pulse-frequency modulation (PFM) for integrated resonant rectification and regulation (IR^3). (a) Conceptual operation and timing diagram. (b) Analog PWM and digital PFM feedback loops. (c) Block-level IR^3 circuit diagram.

3.3.2 Hybrid Pulse Modulation

The IR^3 performs simultaneous rectification and regulation by controlling the amount of power transferred from the RF input to the regulated DC output, V_{DD}, through a hybrid pulse modulation (HPM) scheme that combines pulse-width modulation (PWM) and pulse-frequency modulation (PFM), illustrated in Fig. 3.3 (a). Each pulse activates a conductive path between the resonant tank and the load, accomplishing both rectification and regulation in one step. For rectification,

the pulse generator in Fig. 3.3 (b) activates the up-rectifying power PMOS transistor, M_{PU}, by lowering V_{GU} when its RF input, V_{UP}, exceeds V_{DD}. Conversely, the down-rectifying power PMOS transistor, M_{PD}, is activated by lowering V_{GD} when its RF input, V_{DN}, exceeds V_{DD} in the opposite RF phase for full-wave rectification. For regulation, the width of the activation pulse is controlled by PWM through analog feedback [52], and its pulse frequency is controlled by PFM through digital feedback.

The PWM module regulates V_{DD} simultaneously with rectification, by adjusting the pulse-width based on comparison of V_{DD} with a predefined reference voltage. Owing to large loop gain at DC in purely analog feedback (Fig. 3.7 and Eqn. (3.5)), the PWM mode offers accurate regulation of V_{DD}. However, due to a dominant pole compensation for stability of the analog feedback, the response time of PWM analog feedback is relatively slow: in the range of several hundred microseconds. In addition, due to timing constraints in rectification of the RF input, pulse widths themselves are very short: in the range of a few nanoseconds at tank resonant frequencies above 100 MHz.

Hence, considering typical rise and fall times in V_{GU} and V_{GD} in the upper hundreds of picoseconds range, the dynamic range of pulse-width control is very limited, and PWM alone is insufficient for accurate regulation across varying input and output power conditions. Furthermore, narrow pulse widths prohibit the IR^3 from achieving high PCE at light load conditions.

To address these challenges and provide rapid digital feedback covering wide dynamic range, another PFM regulation loop is included in addition to and in tandem with PWM. The PFM module increases the pulse frequency of V_{GU} and V_{GD} when either pulse width being regulated by PWM reaches an upper threshold; conversely, the pulse frequency is decreased when either pulse width reaches a lower threshold. As such, PFM together with PWM provides broad-range and rapid regulation and improved power conversion efficiency at light load conditions [20, 77].

Fig. 3.3 (c) shows the block-level circuit diagram of the IR^3. The analog output V_{CON} of the PWM module and the digital output V_{WAKE} of the PFM

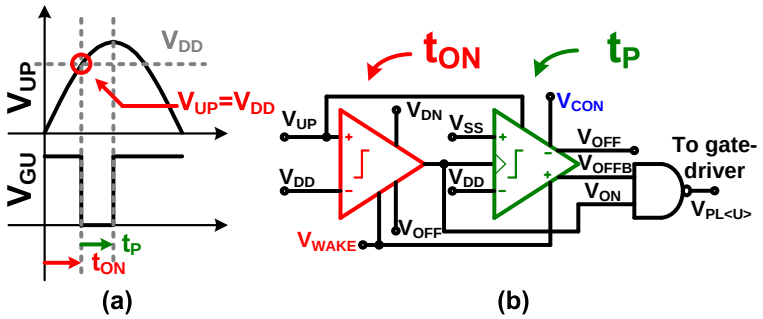


Figure 3.4: The event-driven variable pulse-width generator driven by V_{CON} PWM and V_{WAKE} PFM controls. (a) Timing diagram. (b) Simplified circuit diagram. Only the upper half (V_{UP} controlling V_{GU}) of the circuit is shown; the other half (V_{DN} controlling V_{GD}) is identical.

modules control the width and frequency of the pulsed waveforms $V_{\mathrm{PL<U>}}$ and $V_{\mathrm{PL<D>}}$ driving the gates of up to nine parallel-connected power PMOS transistors. The LC tank recovered clock signal is binary divided to provide various clocks (CLK1−1024) for the entire system including the PFM module and other on-chip loads. A power-on-reset generates an INIT signal forcing the IR^3 into passive mode with diode-connected PMOS transistors and initializing digital state variables in the PFM module during start-up [50]. Circuit implementation and operation of various blocks are detailed in the following section.

3.4 Circuit Implementation

3.4.1 Event-driven variable pulse-width generator

The schematic of the event-driven variable pulse width generator is shown in Fig. 3.4 for half of a cycle (i.e., the positive phase of full-wave rectification). This block produces the pulse waveform $V_{\mathrm{PL<U>}}$ from the analog PWM control V_{CON} and event-driven digital PFM control V_{WAKE} shown in Fig. 3.3 (c). It comprises a fast comparator defining the turn-on time, t_{ON}, when V_{UP} exceeds V_{DD}, followed by a triggered (i.e., zero idle power) variable delay element defining the pulse width, t_P, and synthesizes the overall pulse through a NAND gate. Voltage control V_{CON} over the delay variable t_P establishes PWM control over a 0.4 ns−2.5 ns range. For

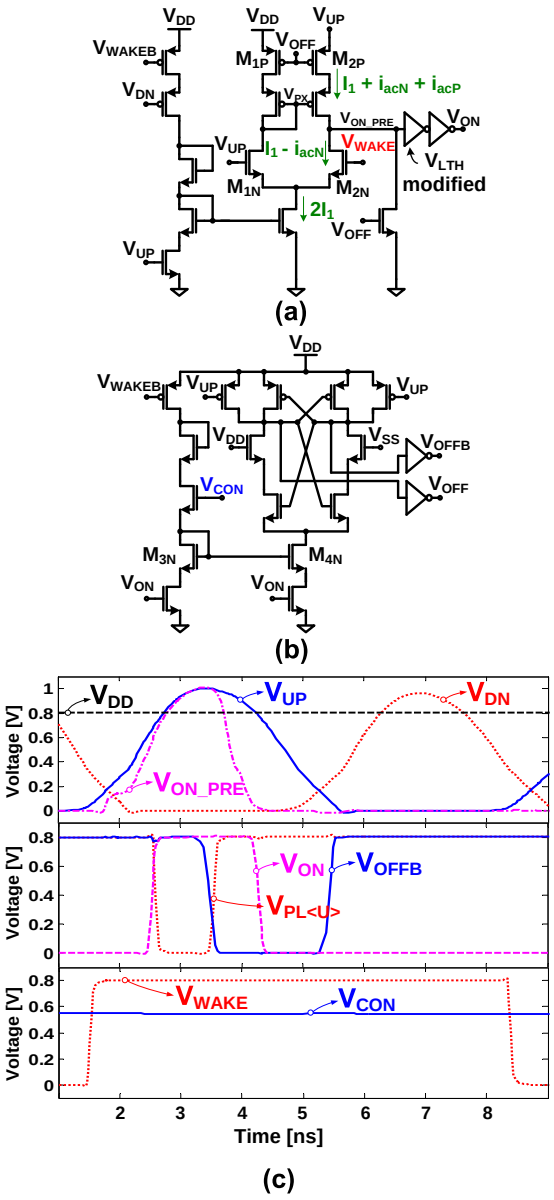


Figure 3.5: Circuit implementation of the pulse width generator in Fig. 3.4. (a) Event-driven dynamically biased t_{ON} comparator, (b) triggered variable delay t_P element, and (c) simulated time domain waveforms.

PFM control and to reduce power consumption, the entire pulse generator circuit is gated by the V_{WAKE} digital signal, which powers up the comparator and delay element only when actively pulsed. The PFM power gating is especially effective at light loads to alleviate active power by lowering the operating frequency of the pulse generator and gate driver.

Low-power design of the t_{ON} comparator is critical in the overall energy efficiency of the WPT receiver, as it operates at up to 144 MHz. Prior-art high-performance comparators consume on the order of $100-800$ μW at 13.56 MHz [50]; a similar approach at 144 MHz would lead to prohibitively high comparator power in the $1-10$ mW range, drastically limiting the power conversion efficiency PCE [49]

$$\mathrm{PCE} = \frac{P_L}{P_L + P_{\mathrm{comp}} + P_{\mathrm{other}}}, \tag{3.4}$$

where P_L, P_{comp}, and P_{other} are the portions of power consumed by the DC load, the comparator, and other blocks, respectively. For example, a typical DC load of $P_L = 10$ μW with conventional comparator power $P_{\mathrm{comp}} = 1$ mW would limit PCE below 1 % even if the power consumed by all other blocks were negligible.

For a workable alternative offering fast decision at low-power consumption, a bias-point-assisted dynamic comparator is proposed in Fig. 3.5 (a). The proposed dynamic t_{ON} comparator is active only when V_{WAKE} goes high to eliminate static power consumption. Since V_{WAKE} rises all the way to V_{DD}, dynamic t_{ON} comparison is accomplished by detecting the time at which V_{UP} exceeds V_{WAKE}. As V_{UP} reaches its peak, $V_{\mathrm{ON\_PRE}}$ also approaches its optimal bias point for fast and accurate comparison, with V_{PX} near the logic-threshold of the following inverter chain (as illustrated in Fig. 3.5 (c)). To compensate for gate driver delay (around 200 ps in simulation), the logic threshold V_{LTH} of the first inverter is adjusted for a faster decision. Further dynamic enhancement in comparator speed is accomplished with a current-reuse active g_m cell composed of M_{1N} and M_{2N}, in addition to the PMOS pair M_{1P} and M_{2P}, to dynamically increase the output current to $2i_{\mathrm{acN}}+i_{\mathrm{acP}}$ for fast voltage slew in $V_{\mathrm{ON\_PRE}}$, while retaining low DC current consumption. In contrast, current state-of-the-art comparators limit the available current for voltage slew to i_{acP}. As such, the simulated average power consumption of the comparator reduces to $0.15 - 1.5$ μW from a 0.8 V supply across all operating frequencies up to 144 MHz.

The variable delay circuit generates a pulse of width t_P as controlled by V_{CON}, when triggered by V_{ON}. Its schematic is shown in Fig. 3.5 (b). Here, V_{CON} controls the transconductance of a dynamic latch triggered by V_{ON} to provide

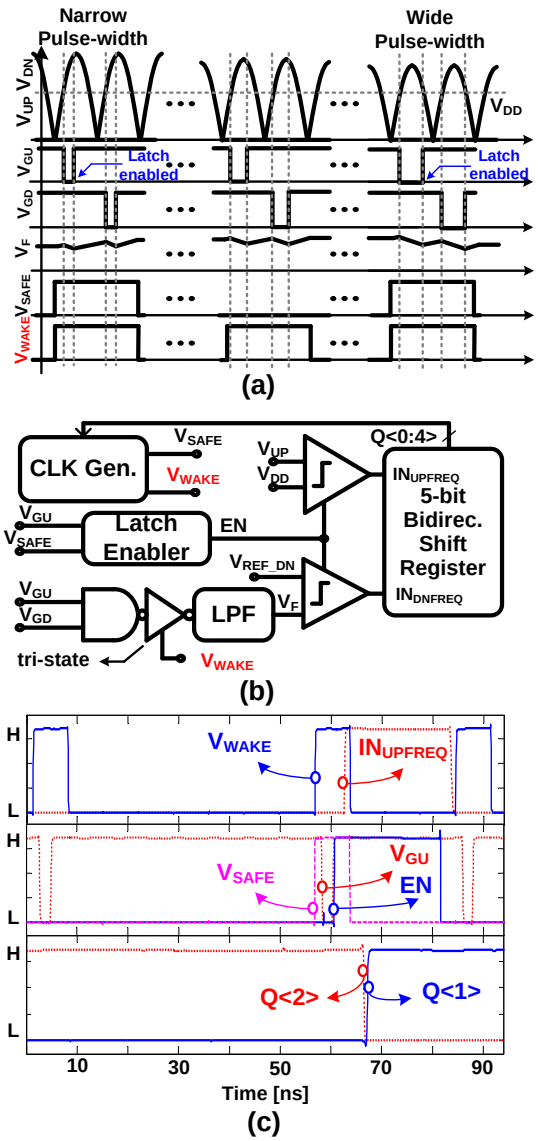


Figure 3.6: Pulse frequency modulator (PFM) module supplying the periodic V_{WAKE} signal gating the pulse generator for rapid digital feedback. (a) Pulse frequency is decreased at a critically narrow pulse width reaching a minimum threshold while Pulse frequency is increased at a critically wide pulse width where V_{UP} (or V_{DN}) reaches below V_{DD}. (b) PFM module block diagram. (c) Simulated time domain waveforms of the PFM module when pulse frequency is increased.

precise short delays (0.4 ns−2.5 ns). Simulated averaged power consumption of the delay element for 1.5 ns t_P is 0.056 − 1.32 μW from a 0.8 V supply, across all operating pulse frequencies from 4.5 MHz to 144 MHz.

3.4.2 Pulse-frequency modulation (PFM) control module

The block diagram of the PFM module is illustrated in Fig. 3.6 along with operational timing diagrams. Under light load conditions, pulse frequency is decreased to counteract critically narrow pulse widths that would otherwise limit the resolution in PWM mode, thereby reducing the overall switching power losses (left side of Fig. 3.6 (a)) Conversely, under heavy load conditions, pulse frequency is increased to avoid reverse currents from load to the tank at critically wide pulse widths (right side of Fig. 3.6 (a)). The PFM module considers either critical action by monitoring pulse-width on a periodic 140 kHz V_{SAFE} schedule. Correspondingly, at the first rising edge of the active-low pulse V_{GU} when V_{SAFE} is active as shown in Fig. 3.6 (a), the latch enabler in Fig. 3.6 (b) triggers two latched comparators to detect two types of threshold events on the pulse-width. Critically wide pulse widths are detected by comparing V_{UP} against V_{DD}, thereby avoiding reverse current by maintaining $V_{\mathrm{UP}} \geq V_{\mathrm{DD}}$ throughout pulse activation. The two comparators are latched on the EN signal to reduce power and to control the updates in pulse frequency by shifting a one-hot representation, Q<0:4>, in a 5-bit bidirectional shift register. The pulse frequency of V_{WAKE} in the clock generator is decided based on 5-bit outputs Q<0:4> of the shift register. The PFM control module shown in Fig. 3.6 (b) in turn controls the operating frequency of the IR^3. The simulated time domain waveforms for a critically narrow pulse width case are shown in Fig. 3.6 (c).

3.4.3 Pulse-width modulation (PWM) control module

The PWM module shown in Fig. 3.7 provides a feedback signal, V_{CON}, to the rectifier core, which contains an event-driven variable pulse generator and power transistors. A voltage divider, comprising a double chain of $4 + 4$ nMOS transistors, used to construct a centered sensing voltage as half of the supply voltage $V_{\mathrm{SEN}} = V_{\mathrm{DD}}/2$, at the expense of 6 dB loop gain loss. The quiescent current of the divider is around 40 nA, resulting in $R_R \approx 20\ M\Omega$ at $V_{\mathrm{DD}} = 0.8$ V. Negative feedback around the error amplifier, A_{ERR}, comparing V_{SEN} with a locally generated reference, V_{REF}, regulates the rectified supply V_{DD} near $2\,V_{\mathrm{REF}}$.

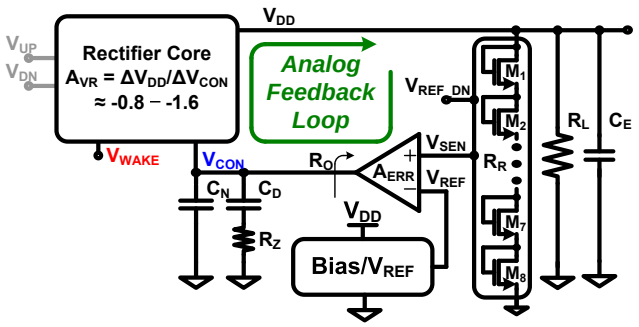


Figure 3.7: Pulse-width modulation (PWM) module for precise analog feedback.

The current consumption of the reference generator block for V_{REF} is 600 nA when V_{DD} is 0.8 V.

Large loop gain plays a significant role in reducing the regulation error. As such, a two-stacked folded-cascode amplifier offering 68 dB open-loop gain at DC consuming 240 nA at V_{DD} of 0.8 V is chosen for the error amplifier. Stability of the analog feedback in supply regulation requires both dominant-pole and zero compensation in the loop. The dominant pole is set by an inserted capacitance, C_D, loading the error amplifier along with its output impedance, R_O. Asserting the dominant pole independent of load conditions requires that $R_0 C_D \gg R_{L,\mathrm{MAX}} C_E$, where $R_{L,\mathrm{MAX}}$ is the minimum load from the supply and C_E is the supply decoupling capacitance. For sufficient phase margin, a zero is inserted at $f_Z = 1/2\pi R_Z C_D$ by adding a resistor R_Z in series with C_D. To mitigate the resulting increase in high-frequency noise, an additional small capacitor, C_N, is inserted in parallel with C_D and R_Z, contributing a non-dominant pole at $f_N = 1/2\pi R_Z C_N$. The small-signal voltage gain of the rectifier core, A_{VR}, ranges between -0.8 and -1.6 depending on input and load conditions through PFM in the V_{WAKE} waveform. First-order analysis gives the loop gain of:

$$A_L = \frac{1/2 \cdot A_{\mathrm{ERR}} \cdot A_{\mathrm{VR}} \cdot (1 + SR_Z C_D)}{(1 + SR_O C_D)(1 + SR_Z C_N)(1 + SR_L C_E)}. \tag{3.5}$$

Accommodating a broad range of load resistances, R_L, the load pole $f_L = 1/2\pi R_L C_E$ varies from 4 kHz to 160 kHz as illustrated in Fig. 3.8. Owing to the dominant pole and zero compensation, the phase margin is guaranteed greater than 48^o for loads heavier than 40 kΩ, ensuring stability of the analog feedback over the operating

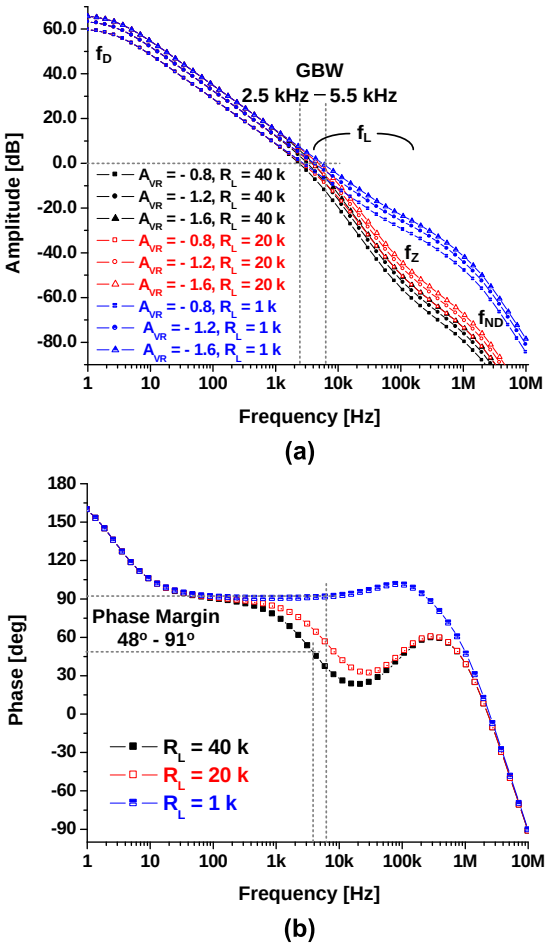


Figure 3.8: Loop gain of regulator feedback with the PWM of Fig. 3.7. Simulated amplitude (a) and phase (b) are obtained with $A_{\text{ERR}} = G_m R_O = 68.2$ dB, $C_D = 22$ pF, $R_Z = 88.6$ $k\Omega$, $C_N = 0.6$ pF, $C_E = 1$ nF, and R_L = 1-40 $k\Omega$.

range.

3.5 Hybrid Pulse Modulation under RF Input Variation

To prove efficacy of the proposed HPM, the IR^3 is simulated with a time-varying RF input voltage as shown in Fig. 3.9. Here, a 144 MHz RF input is amplitude modulated with a 0.1 AM modulation index at 0.4 kHz, resulting in an amplitude variation from 0.98 V to 1.1 V at the half-waved rectified voltage,

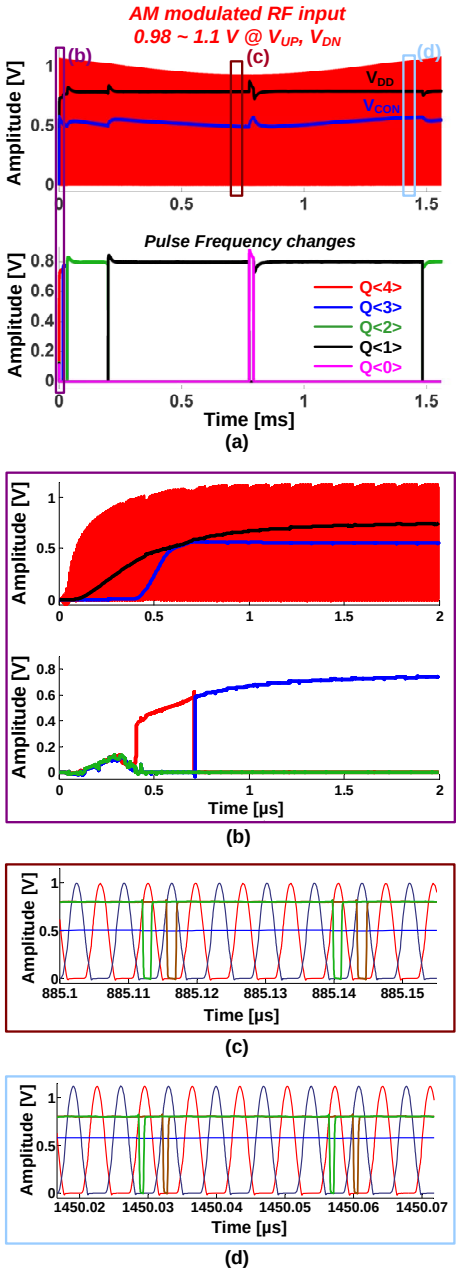


Figure 3.9: Integrated rectification and regulation with HPM under amplitude modulated (AM) RF input. (a) Pulse-frequency is dynamically adjusted based on the pulse-width by changing Q<0:4>. Colored outlined insets show (purple, b) initial power build-up waveforms, and (brown, c) pulse-frequency and pulse-width waveform detail at low RF input voltage, and (cyan, d) at high RF input voltage.

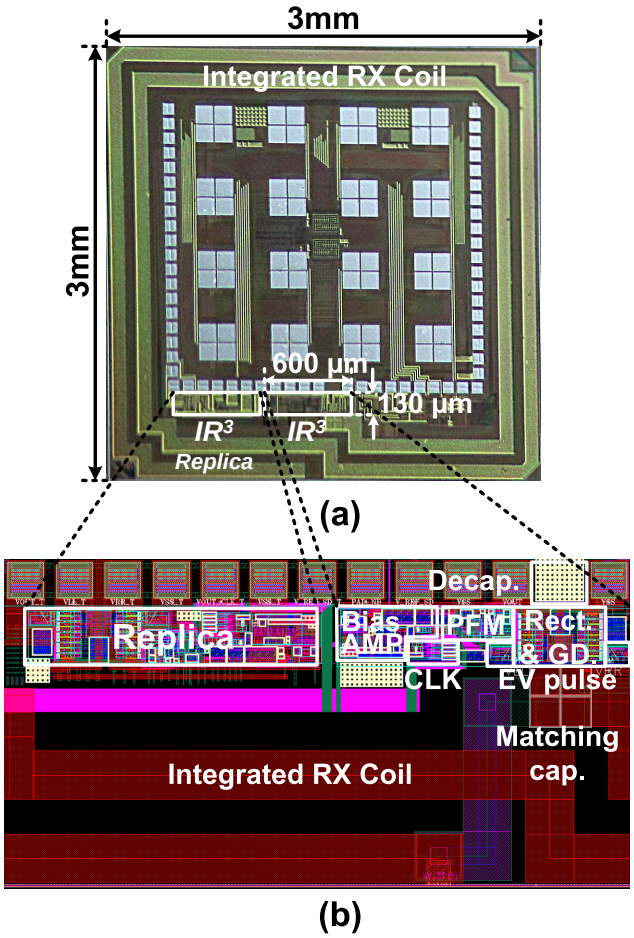


Figure 3.10: (a) Microphotograph of the presented IR^3 integrated as part of a mm-sized electrocortical neural interface chip [23] with recording, stimulation and communication circuits comprising the IR^3 load, and (b) layout detail of the IR^3 part.

V_{UP} and V_{DN}. After V_{DD} initially develops owing to a passive diode-connected rectification mode, the HPM starts rectification and regulation simultaneously on V_{DD} by changing, first, V_{CON} for the pulse-width and, later, Q<1:4> for the pulse-frequency as depicted in Fig. 3.9 (a). This can be more clearly seen in Fig. 3.9 (b) and (c). At decreasing RF input voltages, the PWM control circuit accordingly widens the pulse width via analog feedback at the fixed Q<1> mode. At its maximum pulse-width shown in Fig. 3.9 (b), the PFM increases the pulse-frequency to the Q<0> mode. After reaching its minimum, the RF input voltage begins to increase again. As such, the pulse-width is getting narrowed and the

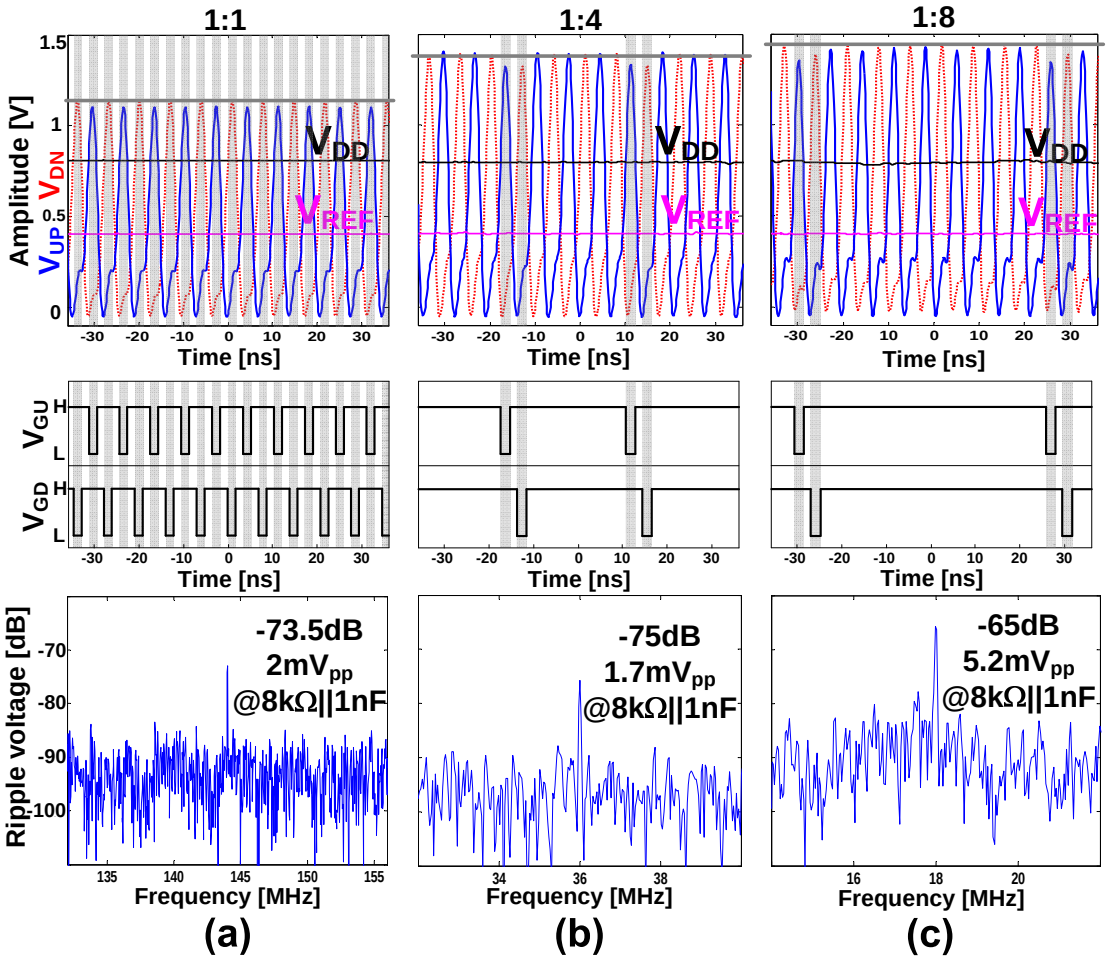


Figure 3.11: Measured RF inputs, V_{UP} and V_{DN}, and DC-regulated output V_{DD} under 8 $k\Omega$ || 1 nF load operating in (a) Q<0>(144 MHz) mode, (b) Q<1>(144 MHz/4) mode, and (c) Q<2>(144 MHz/8) mode. Arrows indicate active cycles and show RF input loading at the regulation pulse frequency. Spectra for voltage ripple in the regulated output V_{DD}, peaking at the pulse frequency, are shown below for each.

pulse-frequency is back to Q<1> mode for regulation under increasing RF input. When critically narrowed pulse-width is detected by the PFM module, the pulse-frequency is increased to the Q<2> mode to avoid degradation in PCE and failure of regulation.

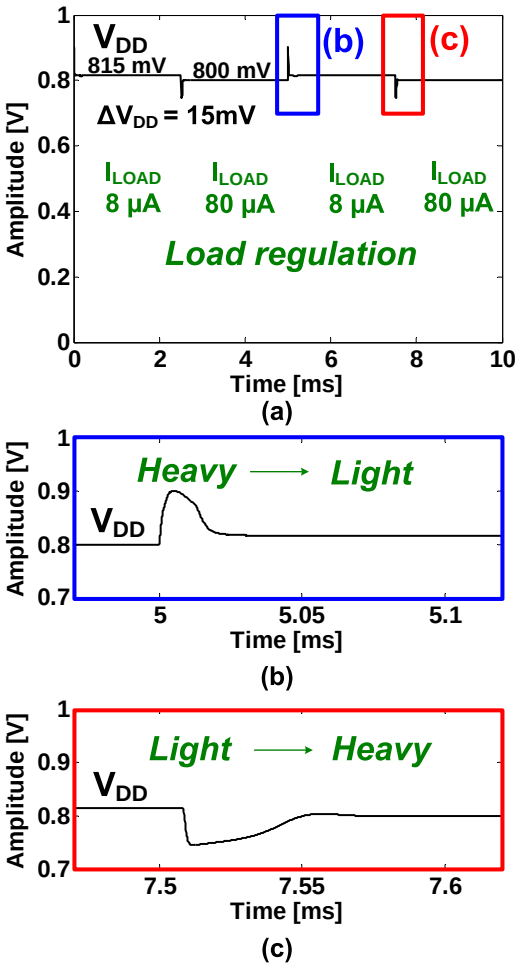


Figure 3.12: (a) Measured dynamic load regulation of V_{DD} with I_{LOAD} alternating between 8 μA and 80 μA with a 1 nF decoupling capacitor at V_{DD} node. PFM improves the regulation speed by changing the pulse-frequency at heavy-to-light load transition (b) and light-to-heavy load transition (c).

3.6 Measurement Results

A microphotograph of an electrocortical neural interface chip [23] internally powered by the presented IR^3 is shown in Fig. 3.10 (a). The active area of the IR^3 part of the chip, presented here, is 0.078 mm^2 in 180 nm 1P4M SOI. An on-chip RX coil is implemented at the chip edge so as to maximize its area with two turns of top metal for 23.7 nH of inductance. The top metal width of the coil is 100 μm to ensure a small series resistance, R_S. As such, HFSS electromagnetic simulation

shows Q_{coil} of the RX coil is 12 at 144 MHz. As shown in Fig. 3.10 (b), the rectifier core in the IR^3 is placed physically adjacent to a matching resonant capacitor to reduce parasitics. To mitigate high-frequency switching noise, sensitive analog blocks in the PWM module are placed far from the rectifier core.

For isolated characterization of RF input regulation, load regulation, and conversion efficiencies of the IR^3 circuit independent of the integrated RX coil, a PCB RF transformer (TC1-1G2+, Mini-Circuits) is initially used to bypass the on-chip LC tank and directly supply V_{UP} and V_{DN} as differential RF sinusoidal signals from a vector signal generator (Keysight N5181A).

Fig. 3.11 shows measurements of the IR^3 regulating V_{DD} at 0.8 V within 5.2 mVpp ripple at various RF input levels representative of typical link distance variations, with correspondingly varying frequency modulations. As expected, the rate of rectification (i.e., PFM frequency) is maximum (i.e., 144 MHz) at lowest RF input voltage amplitude, as the rectifier goes active every RF cycle (maximum PFM) to extract as much power from the input as possible (Fig. 3.11, a). Conversely, the rectifier skips several cycles (lower PFM) at high RF input levels (Fig. 3.11, b and c), as a sufficient amount of energy can be extracted from the input over fewer RF cycles. To characterize ripple, FFT spectra of the regulated voltage V_{DD}, shown at the bottom of Fig. 3.11 in each case (a) through (c), reveal a peaking tone at the pulse-frequency. Note that 144 MHz RF energy coupling through parasitics on the PCB also partially couples to V_{DD} such that Fig. 3.11 (a) shows slightly higher ripple voltage than (b) despite higher pulse frequency. Altogether, the measurements demonstrate the effectiveness of the proposed hybrid pulse modulation technique under various RF input voltages.

The presented IR^3 powers a neural interface system having very different static power consuming levels according to two main operational modes, stimulation vs. recording [23]. To evaluate the capability of the IR^3 accommodating a large dynamic range in static power levels, V_{DD} is measured while changing I_{LOAD} from 8 μA to 80 μA. Owing to the proposed HPM in the IR^3 regulation functionality, a tenfold change in I_{LOAD} incurs less than 15 mV static variation in V_{DD} as shown in Fig. 3.12 (a). This static variation could be further improved by increas-

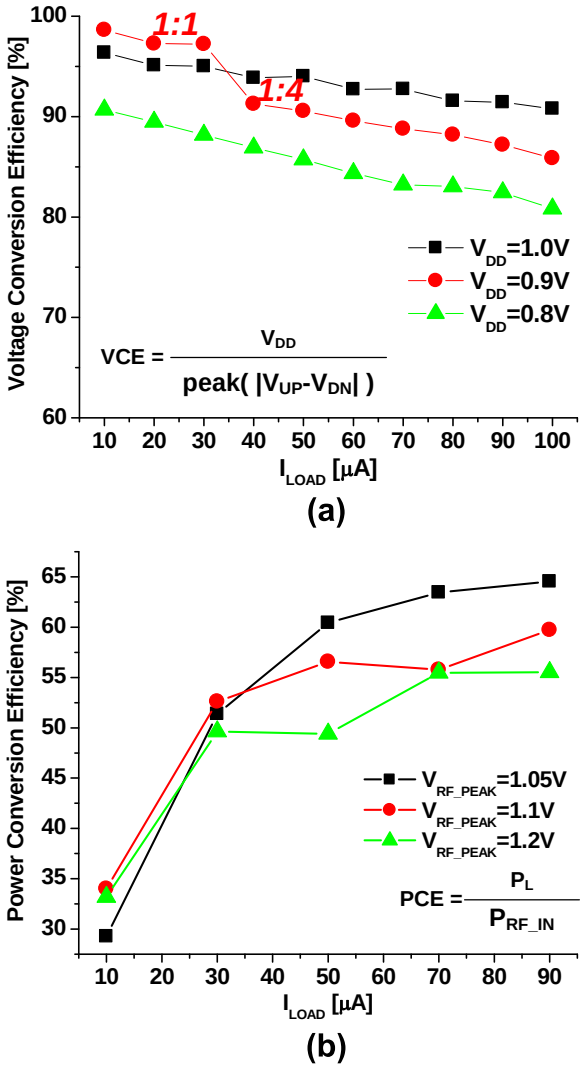


Figure 3.13: Measured voltage conversion efficiency (a) and simulated power conversion efficiency (b) of the IR^3 under varying external load current, target regulation voltage, and RF input conditions.

ing loop gain with a higher gain error amplifier. PFM effectiveness in transient regulation response under rapid load transitions is shown in Fig. 3.12 (b) and (c).

Since the IR^3 performs rectification and regulation simultaneously, voltage and power conversion efficiencies from *both rectification and regulation* are reported as shown in Fig. 3.13 (a) and (b). Compared to advanced active rectifier designs [3, 49] achieving around 80% of VCE from only rectification, greater than 80% of VCE is observed across the range of load conditions at various target

supply voltage V_{DD} levels, controlled by an externally supplied, bypassed reference V_{REF}. At $V_{\mathrm{DD}} = 1\ V$, the lowest measured VCE is 92%. As shown in Fig. 3.13 (b), PCE is higher than 30% even under 8 μW load. As such, the total power consumption of the IR^3, including power losses from the power transistors, is less than 20 μW at 144 MHz. The low power consumption is achieved mainly because of the proposed bias point assisted dynamic t_{ON} comparator. PCE improves at increasing load currents since the portion of the power consumed by control blocks of the IR^3 are independent of load changes. At maximum load, the integral PCE of the IR^3, combining rectification and regulation, reaches 60%. In contrast, power converters in state-of-the-art mm-sized implants [56, 66] achieve around 60% of PCE for rectification, in cascade with 50% to 80% of PCE for regulation, for a net 30% to 50% combined PCE.

The wireless inductive link efficiency and overall WSE with the RX integrated on-chip coil connected to the IR^3 are characterized using a 2.5 cm $\times$ 2.5 cm, single-turn TX coil integrated with a passive matching network on a printed circuit board (PCB) as depicted in Fig. 3.14 (a). Quality factor of the TX coil is greater than 70 at the resonance frequency. The TX coil inductively couples to the on-chip two-turn (2.4 mm $\times$ 2.4 mm inner-loop, 2.9 mm $\times$ 2.9 mm outer-loop) RX coil over 1 cm distance as shown in Fig. 3.14 (b). In this setup, S-parameters between the TX coil and the RX integrated on-chip coil are measured with a network analyzer (Keysight, E5080A), and converted to Z-parameters. Parasitics from the matching network, PCB traces, SMA connectors, and cables are measured and de-embedded [1, 28] to obtain the accurate link efficiency showing the net power gain from the transmitted power at the TX coil (P_{TX}) to the received power at a 4.3 kΩ AC load R_{AC} to the RX coil. According to Eqn. (3.2), 4.3 kΩ of AC load R_{AC} is equivalent to 8.9 kΩ of R_L with 0.82 of VCE and 0.65 of PCE (Fig. 3.13), rendering a 90 μW load to V_{DD}. With this load, the peak link efficiency across various RF frequencies is 2.7% at the RX coil resonance frequency as shown in Fig. 3.15 (a). Measured overall WSE (P_L/P_{TX}) under various load conditions is shown in Fig. 3.15 (b). The IR^3 maintains a constant 800 mV V_{DD} for loads up to 700 μW. Greater than 2% overall WSE from TX coil to the regulated DC is

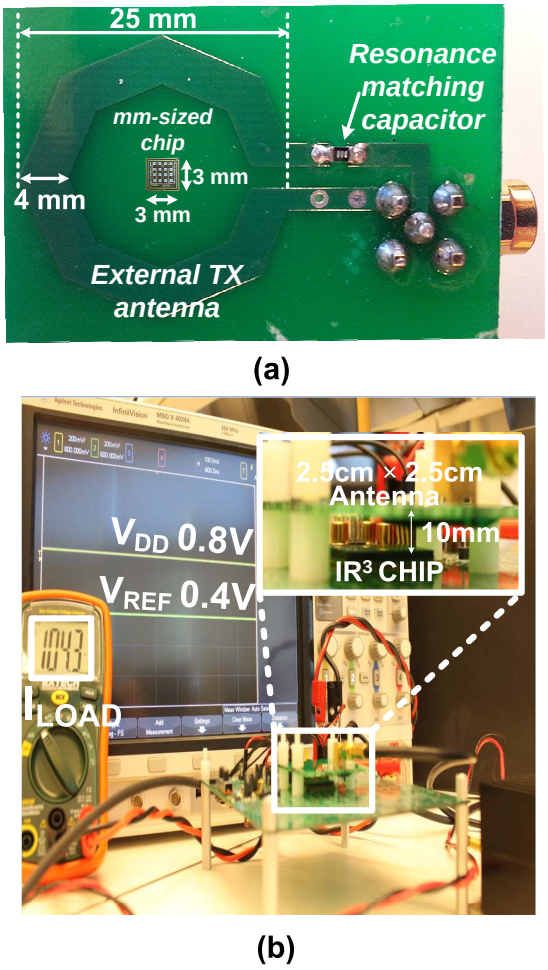


Figure 3.14: Test setup for WSE system validation. (a) External 2.5 cm × 2.5 cm TX coil with matching network. The mm-sized implant chip with the presented IR^3 shown in Fig. 3.10 (a) is superimposed in the center for size comparison. (b) Wireless power transfer at 1 cm distance between TX and on-chip RX coils.

demonstrated with a 160 μW load over air while, at the same input power to the TX coil, 8 dB additional power loss is measured in a more realistic biomedical setting implemented by inserting 1 cm of porcine fatty abdominal tissue.

Table 3.1 summarizes key performance measures of the IR^3 in comparison to state-of-the-art designs for mm-sized implants. Among these, only IR^3 utilizes a regulating rectifier to improve PCE and, thus, WSE. The tabulated figure-of-merit (FoM) is based on one proposed by [95], considering that for mm-sized RX coils (in the mid-field regime) the TX-RX link efficiency is inversely proportional to the

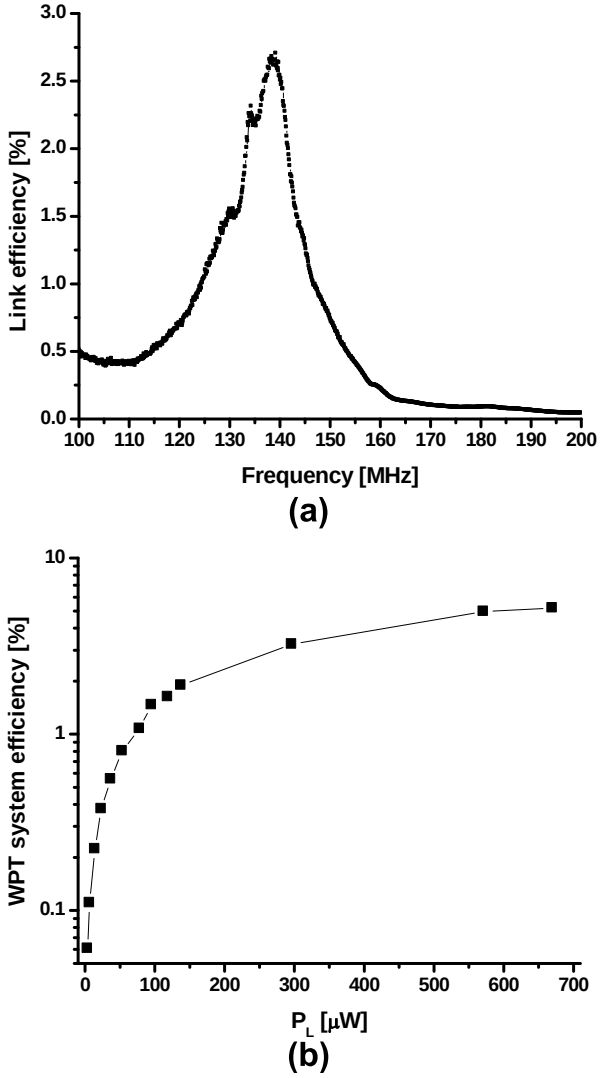


Figure 3.15: Measured WPT power efficiencies with external 2.5 cm × 2.5 cm TX coil. (a) Link efficiency between the external TX coil and the RX 2-turn on-chip coil with AC resistance $R_{\mathrm{AC}} = 4.3$ kΩ. (b) WPT system efficiency, WSE = $P_{\mathrm{L}}/P_{\mathrm{TX}}$ at 1 cm distance between TX and on-chip RX coils. The IR^3 maintains a constant 800 mV V_{DD} for loads up to 700 μW.

cube of the inter-coil distance [70] and the cube of square root of RX coil area [95]. In the comparison of Table 3.1 we extend this FoM from TX-RX link efficiency to overall WSE also accounting for the implant PCE, of the form:

$$\text{WSE FoM} = \frac{\text{WSE} \times D^3}{A^{1.5}} \tag{3.6}$$

where D is the distance between TX and RX coils, and A is the outer-loop area of

Table 3.1: Performance Comparison

	Muller JSSC15	O'Driscoll ISSCC09	Mark VLSI11	Zargham TBCAS15	Kim JSSC17
RX Coil	Off-chip/ 32 nH	Off-chip/ N/R	Off-chip/ 5.73 nH	On-chip/ 130 nH	On-chip/ 23.7 nH
Area of RX coil [mm^2]	42.25	4	1	4.36	8.64
Res. Freq. [MHz]	300	915	535	160	144
Regulator	Separated LDO	Separated LDO	Separated LDO	Separated LDO	Regulating rectifier
Regulation* [%]	N/R	N/R	N/R	N/R	1.87
Decoupling Cap. [nF]	4	N/R	1.39	0.02	1
Process	65 nm 1P7M CMOS	0.13 µm CMOS	65 nm CMOS	0.13 µm 1P8M CMOS	0.18 µm 1P4M CMOS SOI
Overall WSE (TX to V_{DD}) [%]	1.19[a]	0.048 (-33.2 dB)	0.02 (-37 dB)	0.62[b]	2.04[c]
Distance [mm]	12.5	15	13	10	10
WSE FOM**	8.46	20.25	43.94	68.1	80.3

[a]estimated from provided data
transmit PW: 13mW, reveived PW: 0.225mW (simulated link gain, -16.5 dB) and P_L: 0.160mW
[b]estimated from provided data
provided efficiency from TX to the output of rectifier: 0.9 %, calculated efficiency of LDO: 68 % (V_{DD}: 3.1 V, V_{REC2}: 4.5 V)
[c]measured TX power: 7.87mW and P_L: 0.160mW

*defined by [25], Regulation = Static ΔV_{DD} / nominal V_{DD}

**modified from [12], WSE FOM = $\frac{\text{Overall WSE} \times \text{Distance}^3}{\text{Area of RX coil}^{1.5}}$

the RX coil.

3.7 Conclusions

This work has shown the first fully integrated mm-sized WPT receiver for micropower mm-sized biomedical implants operating without off-chip components. Higher resonant frequencies, such as 144 MHz demonstrated here, support full integration of the RX coil with reduced size matching capacitor, and offer higher link efficiency. Crucially, the integration of rectification and regulation yields substantially higher PCE and VCE along with savings in silicon area by avoiding the

need for decoupling capacitors in mm-sized implants. The unique combination of RF inductive resonant power transfer, rectification, and hybrid PWM-PFM regulation of the IR^3 offers superior voltage and power conversion efficiency alleviating severe powering conditions of deep mm-size biomedical implants. As suggested in Fig. 3.1, we envision tiled arrays of mm-sized implants distributed across the surface of cortex with fully integrated IR^3s for power reception and with data transceivers for data communication, performing simultaneous parallel power delivery and data telemetry using a single external loop antenna driven by a beamforming transceiver IC [41, 80].

Acknowledgments

Chapter Three is largely a combination of material in the following two venues: C. Kim, S. Ha, J. Park , A. Akinin, P. P. Mercier and G. Cauwenberghs, "A 144 MHz Fully Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation for mm-sized Implants," in IEEE Journal of Solid-State Circuits (JSSC), to appear, 2017. C. Kim, S. Ha, J. Park, A. Akinin, P. P. Mercier and G. Cauwenberghs, "A 144MHz integrated resonant regulating rectifier with hybrid pulse modulation," 2015 Symposium on VLSI Circuits, Kyoto, pp. C284-C285, Jun. 2015. C. Kim is the primary author and investigator of this work.

C. Kim, P. P. Mercier and G. Cauwenberghs conceived and contributed to the work. C. Kim wrote the first draft of the paper, with S. Ha, J. Park, A. Akinin contributing several sections. P. P. Mercier and G. Cauwenberghs contributed to edit the paper.

Chapter 4

A Miniaturized Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and a Low-Loss Perpendicular Signal Distribution Network

4.1 Introduction

Miniaturization of implants is of paramount importance in enabling emerging applications such as high-density multi-site neural interfaces [62] or mm-sized modular neural interfaces [23] for next-generation brain-computer interface systems and neurology experimentation. Preceding studies have reemphasized the need of miniaturization of implants by showing a decrease in incidence of tissue inflammation, astroglial scarring, and cell death [32, 58].

For miniaturization of implants, wireless power transmission (WPT) via inductive coupling has been typically utilized to replace bulky heath-risky batter-

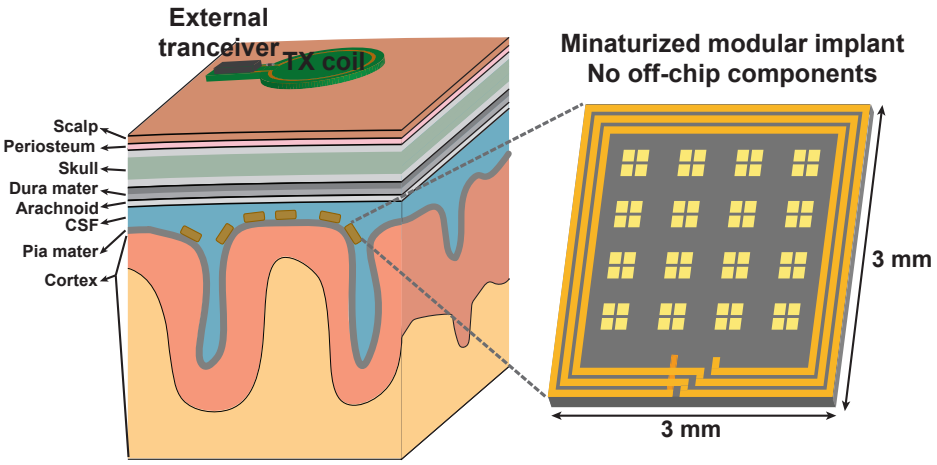


Figure 4.1: Fully modular implants distributed on the cortical surface for next-generation brain-computer-interface applications are enabled with an ultimately miniaturized wireless-power-receiver-on-chip on each implants.

ies [49]. An increase of power carrier frequency allows further miniaturization by reducing size of transmitting (TX) and receiving (RX) coils while compensating diminution of incident magnetic flux over small TX and RX coils [70]. In addition to coil size, huge energy storage components, *i.e.*, decoupling capacitors, for several DC voltages such as a rectifier output and a regulator output, have been also an area limiting factor. Combining rectification and regulation step into one conversion step by implementing a regulating rectifier is a remedy for huge area used for decoupling capacitors since the regulating rectifier has only one DC voltage node [14, 17, 51, 54]. *Ultimate miniaturization* is truly enabled by integrating all external bulky components such as coils and capacitors into a modular implant as shown in Fig. 4.1 [37, 94].

Although a recent fully integrated regulating rectifier eliminated all external components for miniaturization while improving power and voltage conversion efficiencies (PCE and VCE, respectively) from RF voltage at the RX coil to DC voltage at its output node [36, 37], robustness to RF interference, load transition, and wireless link variations is significantly improved on a presented fully integrated wireless-power-receiver-on-chip (WiPow-RX) with an adaptive buck-boost

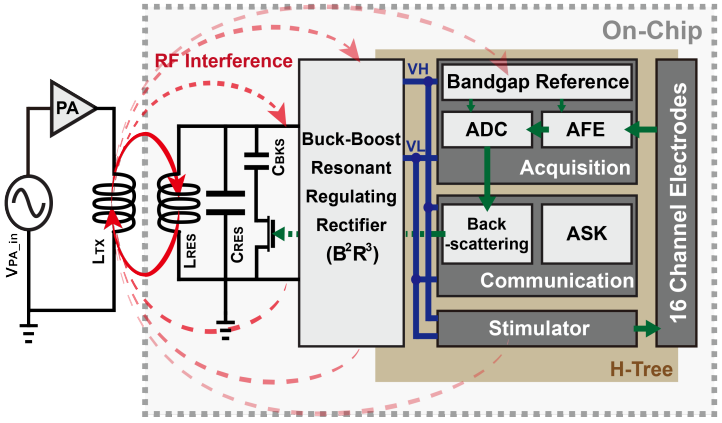


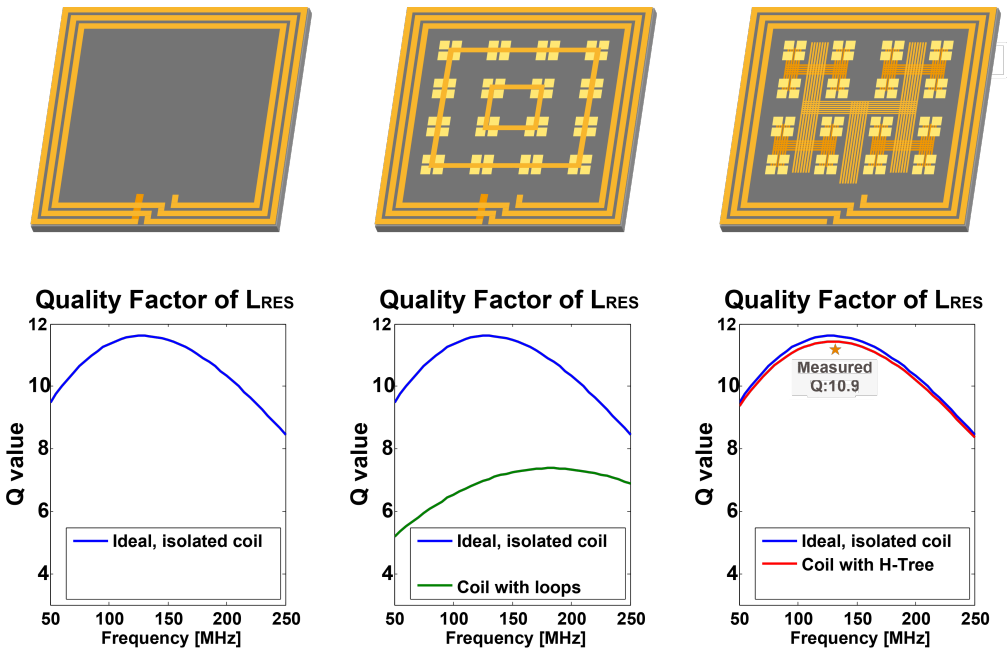
Figure 4.2: Magnetic flux generated from TX coil couples to RX coil while also couples to any other loops on-chip, inducing RF interference

resonant regulating rectifier and low-loss H-tree power/signal distribution. This is because the presented WiPow-RX features: *i*) loop-free H-tree geometry power line/signal distribution networks optimized for maximum RF power collection and minimum RF interference; *ii*) a control feedback loop offering fast load regulation performance; and *iii*) autonomous mode-adaptation to received RF power widening RF input range [42].

Simplified circuit schematics and initial measurement results of the WiPow-RX were presented in [42]. This paper newly presents significantly more detailed circuit schematics, and Q factors of both TX and RX coil, analog front-end (AFE) functionality for system-level validations of the WiPow-RX under WPT conditions. This paper is organized as follows:

4.2 Low-loss H-tree power and signal distribution

RF magnetic flux generated at the TX coil by time-varying current couples to the RX coil for induction of electromotive force (EMF) according Faraday's law of induction. The induced EMF is the main energy source of implants, and produces voltage and current at the secondary LC tank, L_{RES} and C_{RES} in Fig. 4.2. A power management block, the buck-boost resonant regulating rectifier ($\mathrm{B^2R^3}$),



(a) (b) (c)

Figure 4.3: Simulated Q-factor of the RX on-chip coil with: (a) no internal lines; (b) signal and power distribution loops connected to electrodes; and (c) the proposed H-tree signal and power distribution network.

develops dual supplies VH and VL from the secondary LC tank. The dual supplies power on-chip loads such as electronics for signal acquisition, communication, and stimulation. Since 16-channel on-chip electrodes are multiplexed to a differential AFE and an ADC, sensitive analog bio-potential signals from electrodes are also distributed across the entire chip WiPow-RX. These signal and power distribution ought to take extreme care under WPT, especially with the on-chip RX coil. Otherwise, the RF magnetic flux also couples to rather than the RX coil, any other loops on-chip induced by a signal and power distribution network, leading to critical problems such as degradation in efficiency by decreasing Q-factor of the RX coil and saturation of the AFE by inducing differential out-of-band noise at signal lines.

RF interference is simulated in Fig. 4.3 with a full-wave electromagnetic field simulator, HFSS (Ansoft, Pittsburgh, PA) by comparing Q-factor of the RX coil in three different cases for: (a) the isolated coil; (b) the coil with unintentional

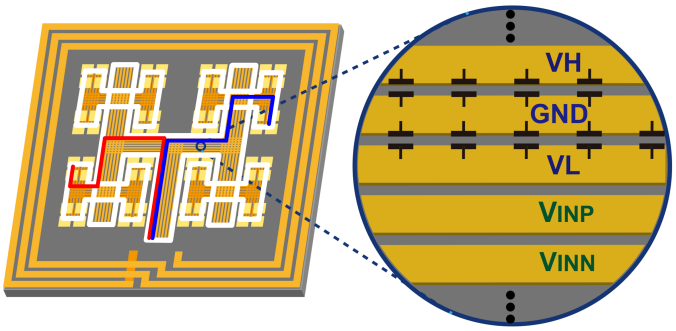


Figure 4.4: Equidistant signal paths and decoupling capacitors in the H-tree network.

loops; and (c) the coil with the H-tree signal and power distribution network. With unintentional loops, Q-factor of the RX coil is severely degraded since unintentional loops intercept RF magnetic flux, generate eddy current, and finally produce additional magnetic flux against incidence of the magnetic flux from the TX coil to RX coil. Since overall WPT system efficiency (WSE; the net power gain from the transmitted power at the TX coil to the RX load after the regulation) is typically limited by Q-factor of the RX coil for the case of miniaturized implants [1, 28, 95], any degradation in the Q-factor of the RX coil ought to be avoided. The H-tree signal and power distribution network systematically eliminates unintentional loops such that the Q-factor of the RX coil with the H-tree network is similar to that of the isolated RX coil, implying the H-tree network absorbs negligible RF magnetic flux from the TX side.

Fig. 4.4 depicts an additional virtue of the H-tree network: the equidistant signal paths. Although the proposed H-tree decouples most RF interference though perpendicular geometry, any residual RF interference is possibly large enough to saturate the AFE since the AFE has a high gain, greater than 70 dB to deal with a few μV input signals [23]. The equidistant signal paths in the H-tree network convert residual RF interference to common-mode noise, which is easily rejected by common-mode rejection functionality of the AFE. In addition, underneath power and signal lines, distributed 1 nF (VH-GND: 0.5 nF and GND-VL: 0.5 nF) MOS-cap decoupling capacitors are placed. As such, large metal plane, which is also able to generate eddy currents under WPT, for decoupling capacitors is avoided.

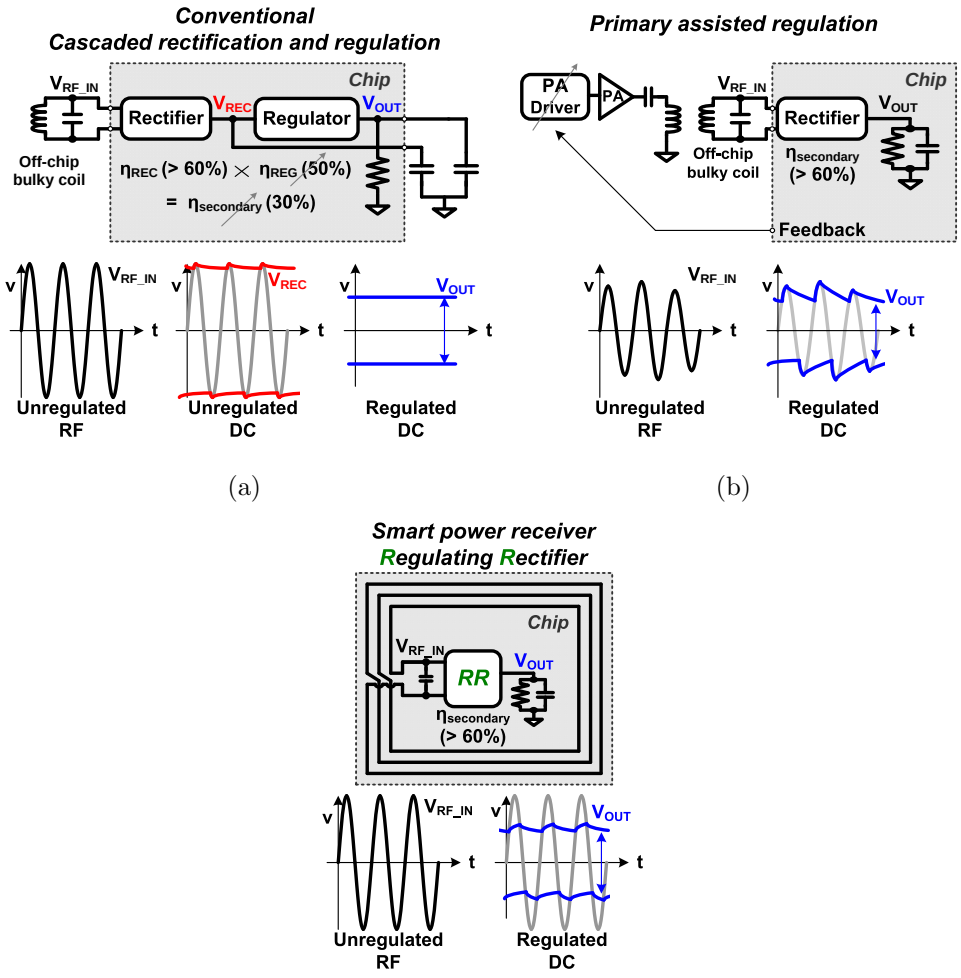


Figure 4.5: Approaches for rectification and regulation; (a) Conventional separated rectification and regulation; (b) Primary assisted regulation; (c) Regulating rectifier with no primary assistance.

Another method avoiding large metal plane from decoupling capacitors is utilizing a high-performance and high-power consuming linear regulator with limited decoupling capacitance, 20 pF [94].

4.3 Rectification and regulation

As suggested in Fig. 4.1, wireless link distances and alignments between the external TX coil and each implant are diverse. Therefore, coupling coeffi-

cient, k, for each link is also individual leading to different received RF energy at the secondary LC tank of each implant. Regardless of wireless link environments, however, power supplies developed by a power management circuit should be regulated for stable operation of on-chip loads such as AFE and ADC. Hence, a power management circuit has to include functionalities of both rectification and regulation.

Cascaded rectification and regulation shown in Fig. 4.5 (a) has been widely adopted since it is simple to implement and robust to wireless link variation [56, 57, 62, 66]. However, it should undergo cascaded loss in PCE and VCE from both rectification and regulation while requiring two huge decoupling capacitors. To remove regulators at the secondary side, primary assisted regulation method in Fig. 4.5 (b) was proposed. The basis of the method is that the transmitted power at the TX coil is controlled by feedback signal from the secondary implant according to rectified output voltage V_{OUT} [46,54]. By this approach, the primary side may be optimized to a specific wireless link environment and thereby to a specific implant. However, this implies that for multiple modular implants, multiple TX coils are required. In addition, regulation speed is possibly be limited since this feedback is composed of a gigantic loop including many delay components, and should have a dominant delay in the loop for stability. For the case that multiple implants receive magnetic flux from the shared TX coil as illustrated in Fig. 4.1, each implant ought to be smart enough to do rectification and regulation simultaneously and locally. Hence, regulating rectifiers shown in Fig. 4.5 (c) have been gradually adopted for modular multiple implants [14, 36, 42] and even for RFID authentication tags [51].

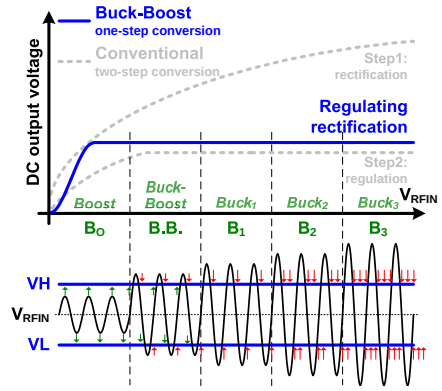
4.4 Adaptive buck-boost mode regulating rectifier

The regulating rectifier shown in Fig. 4.5 (c) should have wide RF input-range to cover the diverse wireless link distances between TX coil and implants, and offer fast regulation speed to support RF input and load transitions from, for example, amplitude-shift-keying (ASK) RF envelop data communication and stim-

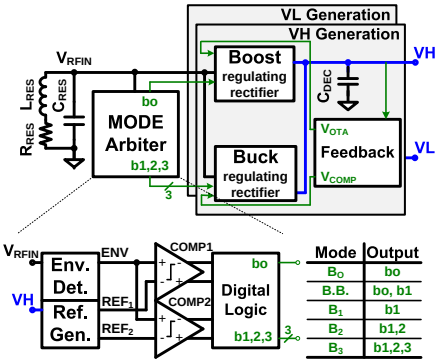
ulation on/off, with on-chip decoupling capacitor rather than off-chip capacitor. The presented adaptive buck-boost resonant regulating rectifier (B^2R^3) conducts rectification and regulation simultaneously to produce dual outputs, VH and VL. For each output, 3 building blocks, feedback module, buck-mode regulating rectifier (buck RR), and boost-mode regulating rectifier (boost RR) are implemented while mode-arbiter is shared to both outputs. Mode-arbiter with two different regulating rectifiers support multi-mode adaptation for greater than 11 dB RF input-range and a dual path feedback loop in the feedback module features less than 0.5 μs load regulation speed. In this section, four individual building blocks are detailed.

4.4.1 Mode arbiter

Multi-mode adaptation is proposed to widen RF input range, and thereby, to increase robustness to wireless link variation. At low RF input ($\ll$ 0.45 V in amplitude), the B^2R^3 is configured to the boost mode such that lower RF input than target output voltage is converted to dual DC target voltages, *i.e.*, VH and VL, while at high RF input ($\gg$ 0.45 V in amplitude), buck modes configuration enables the B^2R^3 to offer voltage-down rectification and regulation. In buck modes, three segmented power MOSFETS in the buck-mode regulating rectifier are turned on/off according to RF input voltage to alleviate power loss in the power MOSFETS, as illustrated in Fig. 4.6 (a). Mode arbiter shown in Fig. 4.6 (b) features automatic multi-mode adaptation to various RF inputs by sensing RF input voltage and configuring the B^2R^3 accordingly. A conventional Dickson charge pump composed of diode-connected MOSFETs and a flying capacitor works as an envelope detector which provides information on RF input voltage to following comparators. With two references voltages, REF_1 and REF_2, from a simple voltage division reference generator, the two comparator and digital logic make decision for appropriate configuration. Since the B^2R^3 has 5 different modes, with a conventional two output states (HIGH and LOW) comparator, 4 comparators with 4 references are required. To save power and area, three output states comparator (HIGH, SIMILAR, and LOW) in Fig. 4.6 (c) is utilized. The comparator



(a)



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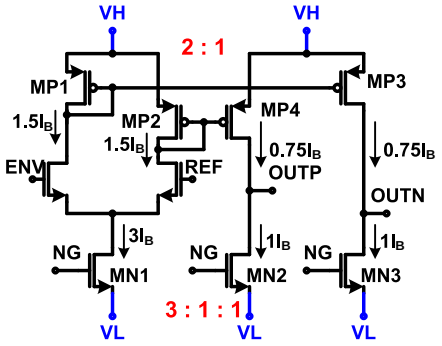


(c)

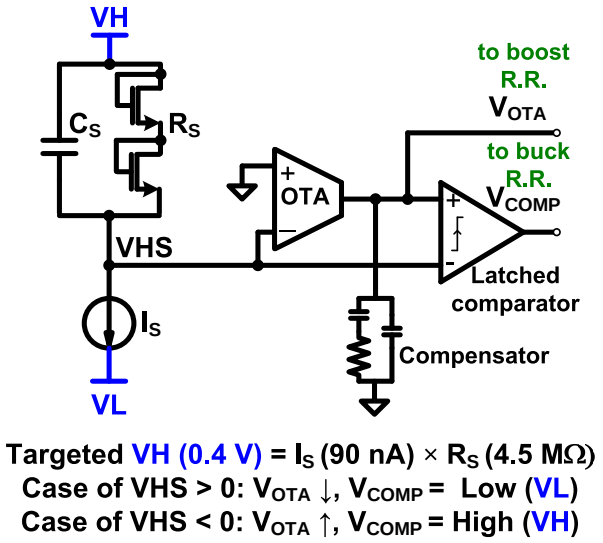
Figure 4.6: Multi-mode adaptation to various RF inputs is detailed. (a) 5 different buck and boost regulating rectification mode switching covers wide RF input range. (b) Mode arbiter sense RF input voltage and changes configuration of the B^2R^3 automatically with 4 digital output bits, bo, b1−b3. (c) The simplified schematic of the proposed comparator in the mode-arbiter is shown. The comparator has three output states.

is fully differential; differential input (difference of ENV and REF) and differential output (difference OUTP and OUTN). DC bias current of the comparator output stage is intentionally off: DC bias current from PMOS (MP3 and MP4) is set to 0.75 I_B while NMOS (MN2 and MN3) is supposed to flow current of 1 I_B. As such, when input voltage is either ENV $\gg$ REF or ENV $\ll$ REF, output is in either HIGH state (OUTP:H, OUTN:L) or LOW state (OUTP:L, OUTN:H). When input voltage is small enough (ENV $\simeq$ REF), output is in SIMILAR state (OUTP:L, OUTN:L). I_B is set to 40 nA and total static current for the comparator is 200 nA for COMP1 and 180 nA for COMP2 from 0.8 V supply (VH: +0.4 V, VL: -0.4 V). The comparator remains at the SIMILAR state when input is in the range of $\pm$5 mV with 150 mV reference (REF1) and $\pm$10 mV with 200 mV reference (REF2).

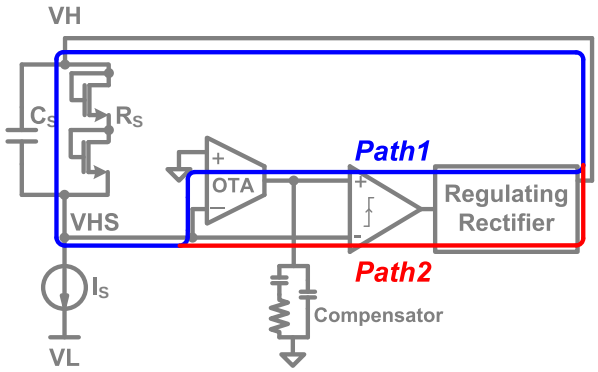
4.4.2 Feedback

The main mechanism of regulation is feedback. That is, a sensor in the feedback module shown in Fig. 4.7 (a) provides information on output voltage and based on this information, the feedback module delivers feedback signal to either a boost RR or a buck RR to adjust effective R_{ON} resistance between V_{RFIN} and VH or VL for regulation. The sensor in the module for VH generation is composed of a parallel of a capacitor (C_S) and two diode connected MOSFETs (R_S) and a current source (I_S). Since VH is sensed to VHS with level shift generated from I_S and R_S and the sensed voltage, VHS, is compared to ground at the input of a OTA and a latched comparator, VH guarantees two threshold voltages (V_{TH}) headroom from ground. I_S is set to 90 nA while R_S is 4.5 MΩ for 0.4 V of targeted VH. Because of somewhat large resistance of two diode connected MOSFETs, parasitic capacitance at a VHS node induces non-negligible RC delay and affect the sensing speed. To avoid significant delay, 150 fF capacitance, C_S, is added parallel with the two diode connected MOSFETs.

The simplest modality for R_{ON} resistance adjustment is an on/off control of regulating rectifier(RR)s, so called bang-bang control. Bang-bang control turns off RRs if output voltage is greater than a target voltage, and vice versa. Bang-bang control features simple implementation and fast load regulation since it requires



(a)



(b)

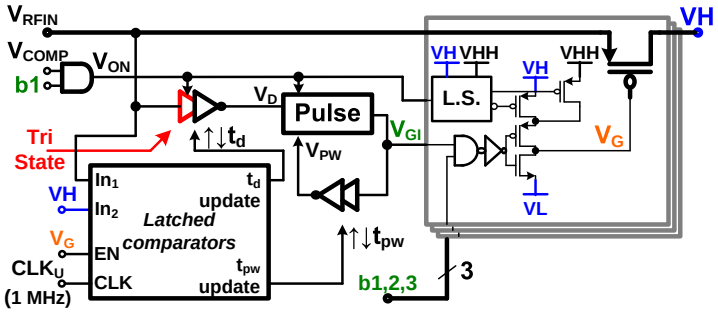
Figure 4.7: (a) Block diagram of the dual path feedback module, and (b) dual path feedback loop for fast and accurate regulation.

only one comparator and no compensation. However, it has non-avoidable disadvantage: output voltage is never able to reach a target voltage. In other words, bang-bang control always permits a certain amount of error between output voltage and target voltage. On the other hand, an error integration control that continuously adjusts R_{ON} resistance of RRs directly based on information of integrated error. Although this error integration control eliminates error at the output voltage nodes, since it relies on error integration, it allows for lagging on feedback signal. As such, the speed of load regulation is limited.

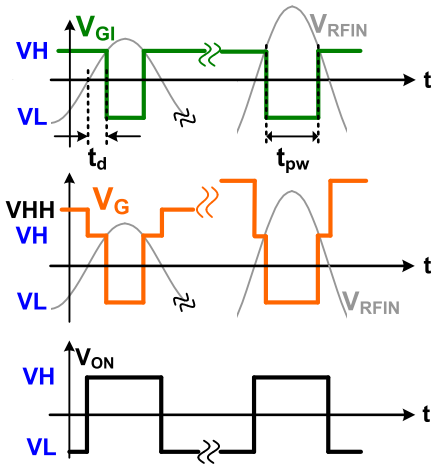
The feedback module utilized in the B^2R^3 features fast load regulation and accurate control on output voltage with a dual path feedback loop as shown in Fig. 4.7 (b). The sensed voltage, VHS, goes directly to the negative input of the latched comparator for the bang-bang control enabling fast load regulation. In conventional bang-bang control, positive input of the comparator is typically connected to a reference such that VHS is close to the reference with some amount of error. Here, an adjustable reference generated from an error integrator composed of an OTA and a compensator is adopted to eliminate error between VHS and the reference. The error integrator receives VHS voltage as well as the reference, here ground, as input signals and integrates error between VHS and ground. Therefore, if VHS is less than ground, output of the integrator, V_{OTA} increases such that the latched comparator produces more frequently an enabling signal to the regulating rectifier. Owing to error integration, it is feasible that error between VHS and ground, and thereby, VH and target voltage, is eliminated. Hence, the B^2R^3 has both advantages from the bang-bang control and the error integration control, simultaneously. A conventional folded cascode amplifier is employed for the OTA and consumes 400 nA of static current from 0.8 V supply. The latched comparator consists of a pre-amplifying stage and a latch stage. Pre-amplifying stage has three cascaded self-biased inverter type amplifiers [4] followed by a conventional inverter type clocked-latch. The latched comparator consumes 600 nA of static current and 800 nA dynamic current at 32 MHz clock speed for the latch from 0.8 V supply. Pre-amplifying stage amplifies difference between V_{OTA} and VHS to CMOS level (rail-to-rail) while it induces less than 10 ns delay.

4.4.3 Buck-mode RR

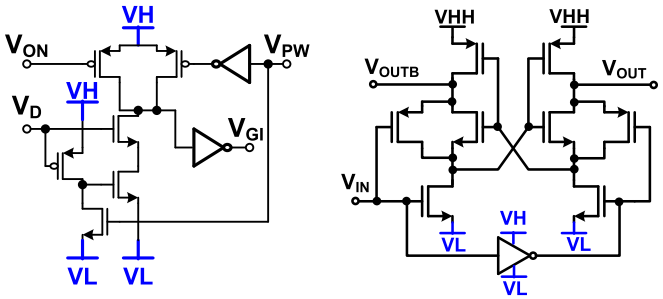
When RF input amplitude is greater than 0.45 V, the mode arbiter configures the B^2R^3 to buck modes by asserting b1 to permit buck-mode regulating rectifiers (buck RR) shown in Fig. 4.8 (a) to be enabled according to V_{COMP}. The enabled buck RR (V_{COMP}: HIGH) basically implements a conductive path from RF input, V_{RFIN}, to VH through a power PMOS when V_{RFIN} is greater than VH. This path is power efficient owing to low R_{ON} resistance of the PMOS since the



(a)



(b)



(c) (d)

Figure 4.8: (a) Block diagram of the buck-mode regulating rectifier, and (b) time waveforms. Detailed circuit schematics for (c) pulse generator and (d) level-shifter in the buck-mode regulating rectifier.

PMOS is fully turned on by lowering V_G to VL. However, because of the low R_{ON} resistance, turning on/off the PMOS at the optimal time is critical. Otherwise, power conversion efficiency (PCE) of the RR is severely degraded due to huge reverse current for the case of wider on-time and/or switching loss coming from gate capacitance of the large sized power PMOS for the case of narrow on-time. Typically, at the expense of significant power consumption, high speed comparators have been employed hitherto to turn on the PMOS when V_{RFIN} starts to greater than VH and turn off when V_{RFIN} becomes less than VH, which is the optimal time for PCE [49]. Although a recent work presents a power-efficient high speed comparator [36], it requires additional adjustable delay element to turn off the PMOS. It turns out that if local negative feedback loops figure out only two time variables, t_d and t_{pw} in Fig. 4.8 (b), the high-speed comparators are no longer required [42,62]. These time variables are updated every 1 μs by comparing V_{RFIN} and VH with two conventional latched comparators at falling and rising edge of the gate voltage, V_G, for each variable to maximize t_{pw} for the optimal on-time. Since a current starved inverter chain is utilized for each time variable, V_D and V_{PW} have slow rising and falling time, possibly inducing non-negligible short-circuit current with a conventional logic for pulse generation. As such, a pulse generator that has three inputs, V_D, V_{PW} and V_{ON}, one output, V_{GI}, and offers no short-circuit current is proposed as shown in Fig. 4.8 (c).

On the other hand, when the buck RR is disabled, it is important to turn off the PMOS completely. If the PMOS is gated with the voltage level of VH, whenever V_{RFIN} is greater than V_{TH} on top of VH, a weak conductive path from V_{RFIN} to VH is induced through the PMOS. As such, it fails to regulation at high RF input case. Furthermore, this path has large R_{ON} resistance, leading to degradation on PCE. Hence, the PMOS should be gated with higher voltage level than V_{RFIN}. For this purpose, VHH is internally generated based on V_{RFIN} amplitude and utilized to gate the PMOS completely with a level-shifter. Since the switching frequency can be as high as 144MHz/2, switching power consumption of a conventional level-shifter with a NMOS input pair and a cross-coupled PMOS pair is not acceptable. A main culprit of the power loss in a conventional level-shifter is fighting nodes

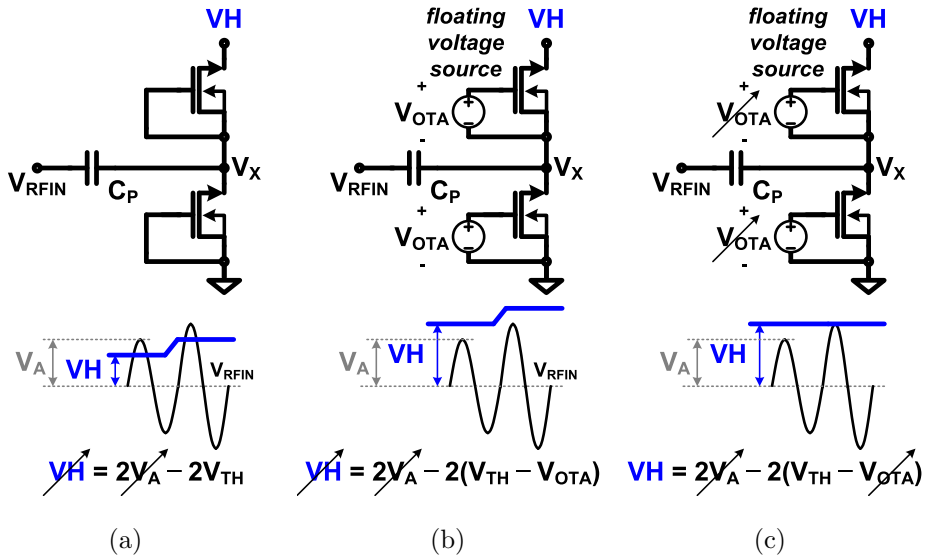
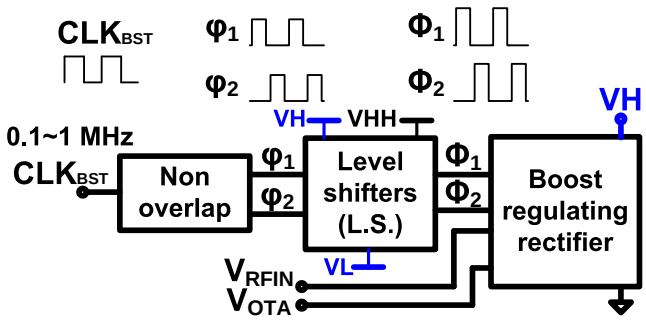


Figure 4.9: Boost RF-DC rectifiers; (a) a conventional Dickson charge-pump rectifier, (b) a V_{TH} cancellation rectifier, and (c) a V_{TH} cancellation regulating rectifier.

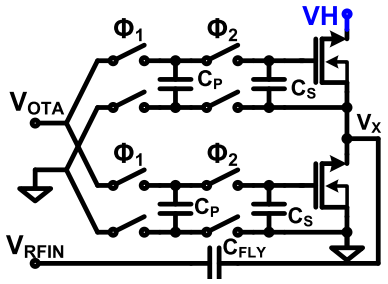
between the NMOS input pair and the PMOS cross-coupled pair. The presented level-shifter shown in Fig. 4.8 (d) has another stage between two NMOS and PMOS pair to remove fighting nodes. Therefore, it consumes 1.5 μW at 10 MHz switching frequency with 100 fF capacitive load for less than 1.5 ns rising time, which is a 3$\times$ improvement over a conventional design.

4.4.4 Boost-mode RR

Even if RF input amplitude is less than target DC voltage, RF to DC rectification is feasible with boost-mode rectifiers. A conventional Dickson charge-pump in Fig. 4.9 (a) has been widely adopted for boost-mode RF to DC rectification [56] because of its simplicity for implementation at the expense of losses in PCE and VCE from V_{TH} of two diode-connected NMOSs. The conventional Dickson charge-pump has only rectification functionality such that when RF input varies, output voltage directly follows the variation of RF input. Hence, a regulator inducing additional PCE and VCE losses is required. It is viable to alleviate V_{TH} losses by inserting a floating voltage source between gate and drain of NMOS as depicted in



(a)



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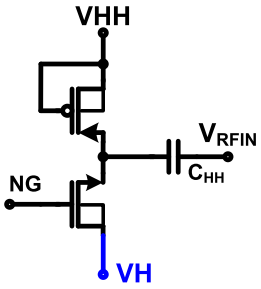


(c)

Figure 4.10: Implementation of the boost-mode regulating rectifier; (a) block diagram with clock time waveforms, and (b) a V_{TH} cancellation regulating rectifier with switched capacitor circuits serving as floating voltage sources. (c) High voltage generator for switched-capacitor circuits in the boost-mode regulating rectifier and high-voltage gating of the buck-mode regulating rectifier.

Fig. 4.9 (b) since positive voltage, V_{OTA} from the inserted voltage source cancels V_{TH} voltage of the NMOS. Here, regulation functionality is simply added along with rectification by adjusting V_{OTA} to control the amount of the V_{TH} cancellation as shown in Fig. 4.9 (c). There are two approaches in controlling the amount of V_{TH} cancellation; open-loop and closed-loop control methods. An open-loop method is that the amount is set based on on RF input variation. That is, when RF input is low, the amount of V_{TH} cancellation increases by increasing V_{OTA}. Although it enables RF input regulation, when load condition varies, VH fails to be regulated. In order to have input and load regulation simultaneously, the amount of the V_{TH} cancellation should be adjusted by a feedback signal from a feedback module monitoring a output voltage for a closed-loop control method. Luckily, the $\mathrm{B^2R^3}$ has the feedback module for the buck RR. Hence, no additional feedback module is required for the boost-mode regulating rectifier (boost RR).

Figure 4.10 is a block diagram of the boost RR utilizing switched capacitor circuits as floating voltage sources with high-voltage non-overlapping clocks. A conventional non-overlapping clock generator [29] provides non-overlapping clock out of a single-ended clock ranging from 0.1 to 1 MHz, and following level shifters change voltage domain from VH to VHH. Non-overlapping clock generator and level-shifters consume 200 nW at 1 MHz clock speed from 0.8 V VH supply and 1.2 V VHH supply. C_{P}, C_{S}, and C_{FLY} in Fig. 4.10 (b) are 1.2, 3, and 22 pF, respectively. VHH is generated by a charge-pump rectifier shown in Fig. 4.10 (c). NG is set to VH level at boost mode in order for target voltage of VHH to be VH + $2V_A$ - $2V_{\mathrm{TH}}$. When the $\mathrm{B^2R^3}$ is configured to buck1,2,3 modes, NG is biased to GND, -0.1 V, and -0.2 V, respectively. C_{HH} is 700 fF.

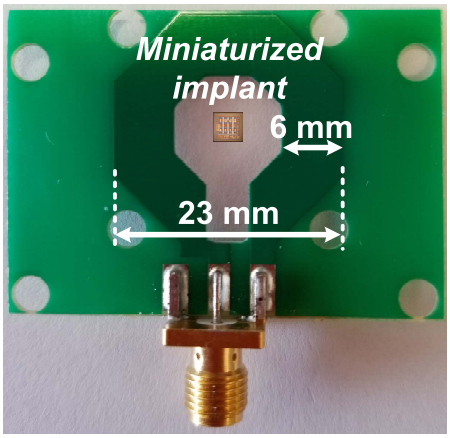
The fully integrated wireless-power-receiver-on-chip (WiPow-RX) including the $\mathrm{B^2R^3}$ were measured with an external 23 mm $\times$ 23 mm coil shown in Fig. 4.11 (a). Quality factor (Q) of the TX coil is greater than 200 at 144 MHz. This TX coil is driven by a power amplifier (Mini-Circuits, ZHL-42W+). The 3 mm $\times$ 3 mm WiPow-RX in Fig. 4.11 (b) receives magnetic flux from by the TX coil and develops RF voltage at the secondary LC tank. TheA‘’ $\mathrm{B^2R^3}$ provides dual regulated power supplies, VH and VL, to power on-chip loads including amplifiers

and an amplitude-shift-keying (ASK) module. The RX coil is 3 turn for 62.2 nH inductance, L_{RES}. The Q factor of the RX coil is measured as 10.9 at 144 MHz, rendering series parasitic resistance R_{RES} to be 5.1 Ω. This series resistance is equivalent to 610 Ω of parallel resistance (R_P) after series-to-parallel conversion. Simulated (ANSYS HFSS) L_{RES}, Q factor, and R_P of the RX coil are 60 nH, 11.2, and 610 Ω, respectively. Measurement characterization was done with 10 mm of link distance between TX and RX coils. Otherwise, link distance is specified.

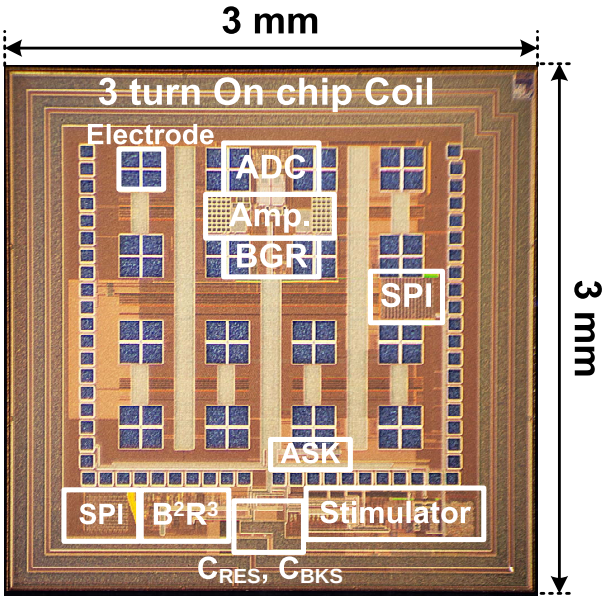
4.4.5 Measurement of B^2R^3

Under RF input envelope variation induced by any changes of link environment, the presented B^2R^3 performs input regulation through mode-adaptation for coarse regulation and dual path feedback for fine regulation as shown in Fig. 4.12. The primary coil was driven by the power amplifier receiving 100 mV for Fig. 4.12 (a) and 60 mV for Fig. 4.12 (b) amplitude modulated signals to generate RF input envelope transient variation, as depicted in blue-gray colored background waveform. The mode arbiter in the B^2R^3 sensed RF input envelope and changed configuration of the B^2R^3 adaptively from buck1 mode to buck3 mode for (a) and from buck-boost mode to buck2 mode for (b). Independently, the feedback module also sensed output voltages, VH and VL, and provided feedback signal V_{OTA} to each regulating rectifier. Owing to these combined regulation methodologies, the B^2R^3 offers rectification and regulation under RF input variation.

Load regulation is an important function for the B^2R^3 since on-chip loads such as ADC and stimulator draw switching current out of supply voltages. To mimic radical load variation, external time-varying current load from 0 to 200 μA was connected between VH and VL, and output voltages VH and VL were measured as shown in Fig. 4.13 (a). Other than on-chip 250 pF decoupling capacitance implemented with H-tree (two 500 pF capacitors in series for VH-GND and GND-VL), no additional decoupling capacitor was connected to output nodes. The buck-mode regulating rectifier in the B^2R^3 performed rectification and regulation with the dual path feedback. When load is heavy, ripple voltage at output nodes is decreased to 3 mV because output nodes had smaller resistance than resistance

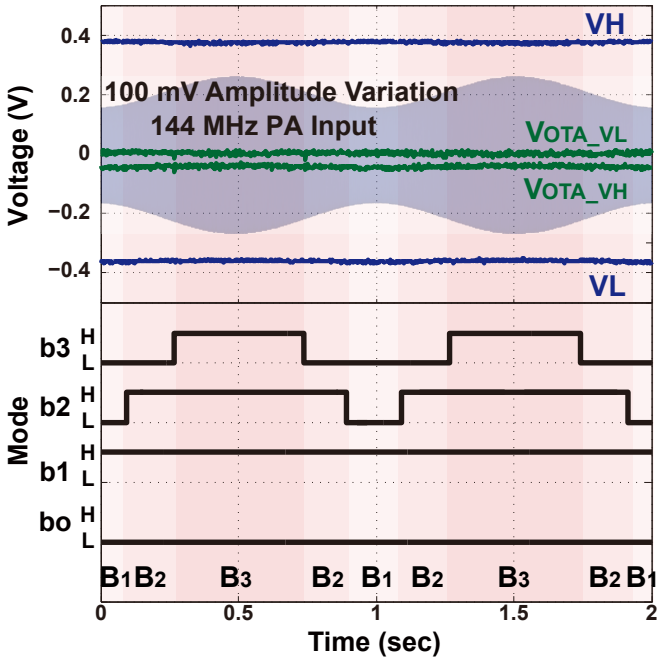


(a)

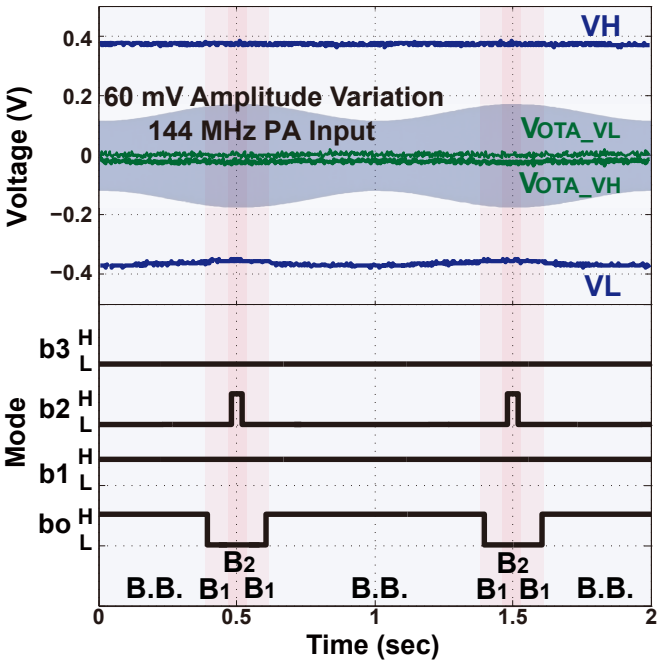


(b)

Figure 4.11: (a) External 23 mm × 23 mm octagonal power TX antenna, and (b) microphotograph for fully integrated wireless-power-receiver-on-chip (WiPow-RX) with low loss H-tree distribution network.



(a)



(b)

Figure 4.12: RF input regulations through mode adaptation; (a) from buck1 to buck3 mode, and (b) from buck-boost to buck2 mode based on RF input envelope.

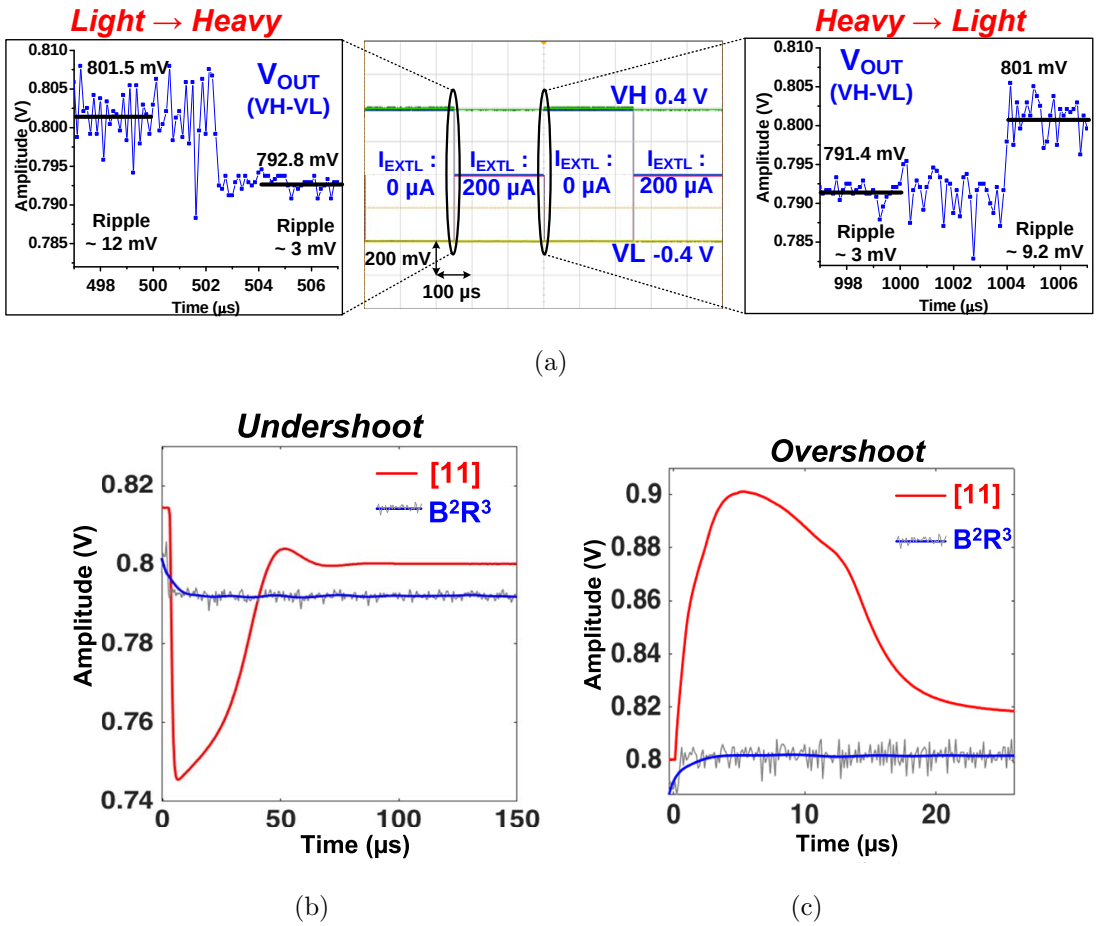


Figure 4.13: (a) Load regulation measurement with external load current changing from 0 to 200 μA to 0.8 V V_{OUT}. (b) Undershoot and (c) overshoot performance comparison with a prior art [37].

with light load. Since the dual path feedback features fast regulation owing to a bang-bang control path (path 2, Fig. 4.7), the B^2R^3 offered negligible undershoot and overshoot as compared a prior art utilizing only an error integration feedback path similar to path 1 of Fig. 4.7 (b) [37].

Transfer function from the input of the power amplifier (PA) to output voltages (V_{OUT}) of the B^2R^3 in Fig. 4.14 was measured by changing input with three different load conditions at 10 mm of link distance between TX coil to RX on-chip coil. At small RF input, the B^2R^3 operated in the boost-mode to generate target output voltage while at large RF input, high voltage gating technique in the buck-mode regulating rectifier blocked an unintended and inefficient conductive

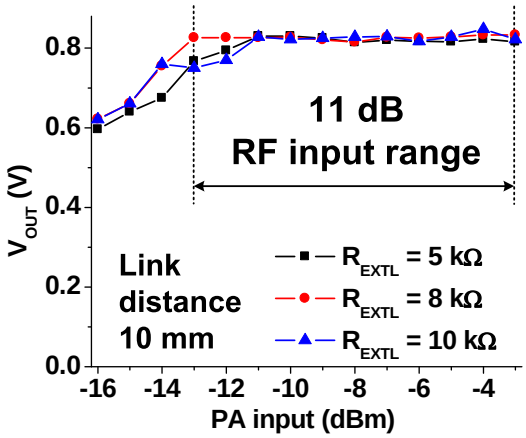
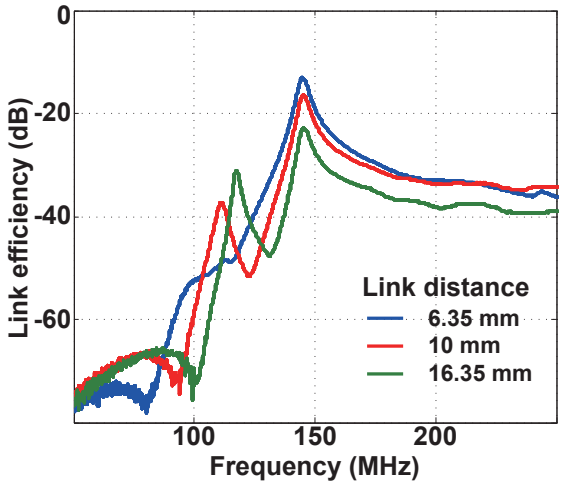


Figure 4.14: Transfer function curve showing RF input range of the B^2R^3.

path generated by a power PMOS diode-connection from RF input to output voltages to maintain target voltage as explained in 4.4.3 and 4.4.4. Hence, the B^2R^3 has 11 dB of the wide RF input range compared to a prior art that has 4 dB RF input range [37]. Greater than -3 dB RF input may reach breakdown voltage of MOSFET transistors in gate drivers of the buck RRs.

Power efficiencies shown in Fig. 4.15 were measured at three different link distances. Parasitics from the TX matching network, PCB traces, SMA connectors, and cables were de-embedded to obtain the accurate power gain [1,28,37]. For link efficiency, S-parameters between the TX coil and the RX integrated on-chip coil were measured by changing RF frequencies from 100 to 250 MHz with a network analyzer (Keysight, E5080A), and converted to Z-parameters to obtain the power gain from TX coil to RX coil as shown in Fig. 4.15 (a) [28]. Owing to low-loss H-tree power and signal distribution network, link efficiency and overall WPT system efficiency are as high as 5.6 % and 3.5%, respectively at 6.35 mm link distance.

For system level validation, measurements for an analog-front end (AFE) module and an amplitude-shift keying (ASK) module along with the B^2R^3 was conducted. AFE is the most sensitive analog building block in the miniaturized implant since it amplifies small electrocortical signal ($\ll$ 1 mV) to a few hundred mV for better digitization as shown in Fig. 4.16 (a). Due to this small amplitude of input signal, the presented H-tree should de-couple RF interference and convert



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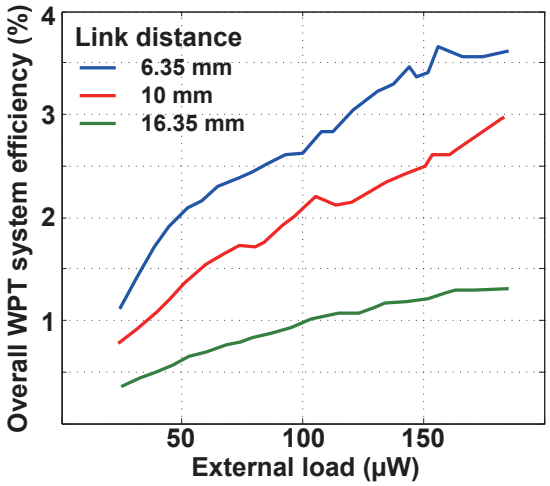
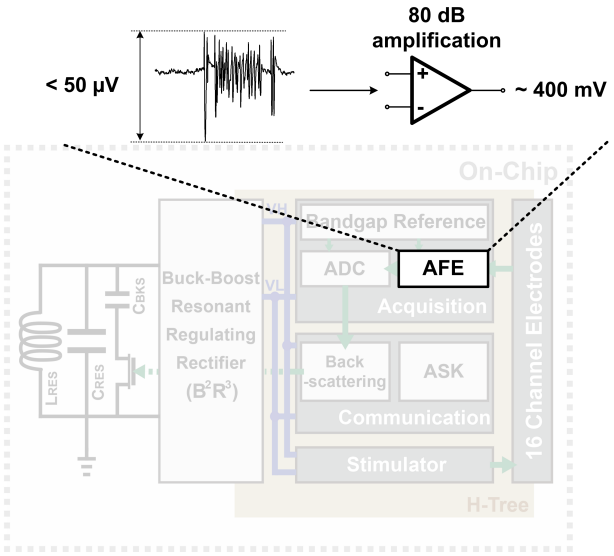


(b)

Figure 4.15: Measured wireless power transmission (WPT) efficiencies; (a) Link efficiency between TX and RX coils, and (b) overall WPT system efficiency (WSE) from TX to regulated V_{OUT}.

residual RF interference to common-mode noise. Given the same input, Fig. 4.16 (b) shows AFE output voltages with three different conditions; external power, external power with RF interference, and only RF power. Owing to the efficacy of the H-tree, the amplified waveforms are hardly distinguishable.

Although ASK is the energy-efficient data communication methodology, it produce severe disturbance to the B^2R^3 since the ASK module inherently utilize



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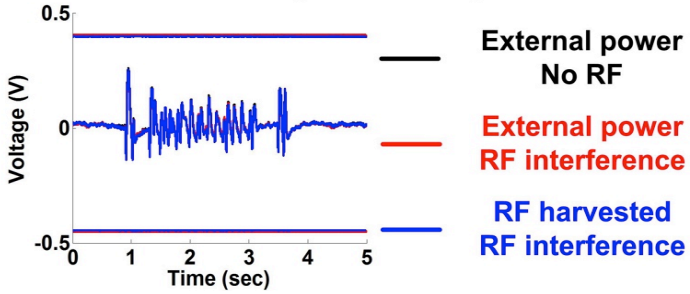
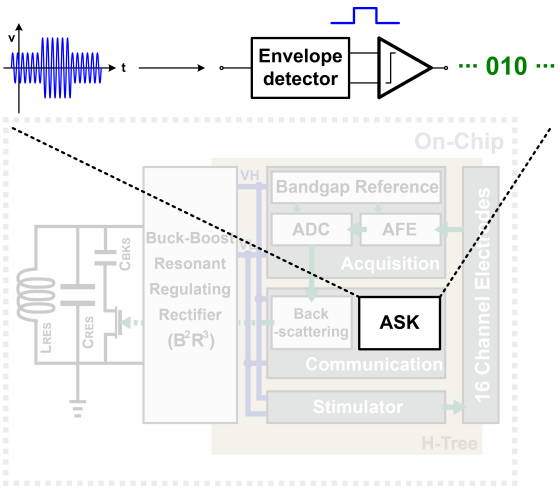


(b)

Figure 4.16: Analog front-end (AFE) system level validation; (a) test set-up and (b) amplified time-domain waveforms with three different conditions; external power, external power with RF interference, and fully RF powered.

amplitude variation at received RF input voltage as shown in Fig. 4.17 (a). The measured input voltage to the primary LC tank and output voltage of the ASK module along with regulated DC voltages VH and VL under RF power case are shown in Fig. 4.17 (b).

Table 4.1 summarizes key performance measures of the B^2R^3 in comparison to state-of-the-art designs for mm-sized implants.



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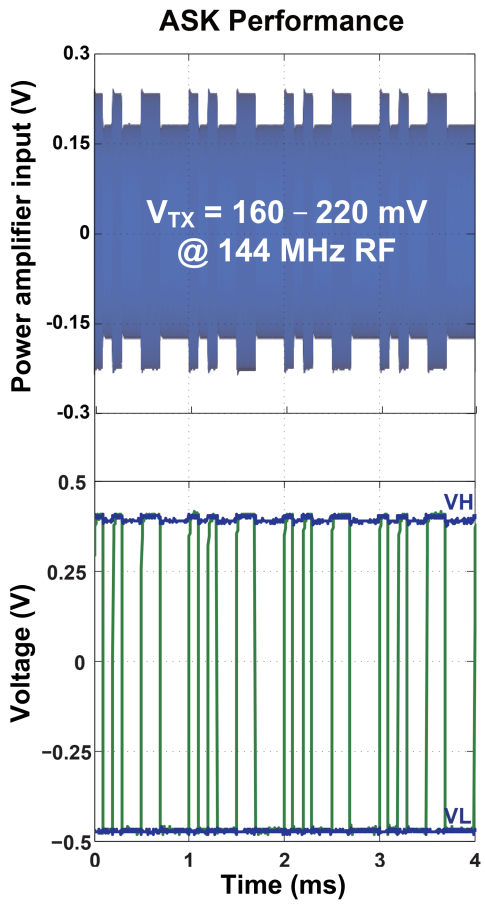


(b)

Figure 4.17: ASK module system level validation; (a) test set-up and (b) ASK output voltage with regulated DC voltages VH and VL.

Table 4.1: Performance Comparison

	Muller JSSC15	Zargham TBioCAS 2015	Mark VLSI 2011	O'Driscoll ISSCC09	Kim JSSC17	Kim JSSC18
Res. Frequency (MHz)	300	160	535	915	144	144
RX Coil/Value(nH) /Area(mm^2)	Off-chip/32 /42.25	On-chip/130 /4.36	Off-chip/5.73 /1	Off-chip/N/R /4	On-chip/23.7 /8.64	On-chip/60.3 /8.74
Number of modes	1	1	1	1	1	5
Regulation approach	Separate LDO	Separate LDO	Separate LDO	Separate LDO	Regulating rectifier	Regulating rectifier
Regulation*(%)	N/R	N/R	N/R	N/R	1.87	1.12
Overshoot (mV)	N/R	N/R	N/R	N/R	100	< 1
Decoupling Capacitor (nF)	4	0.02	1.39	N/R	1	0.25
Process	65 nm CMOS	0.13 µm CMOS	65 nm CMOS	0.13 µm CMOS	0.18 µm CMOS SOI	0.18 µm CMOS SOI
Overall PCE(%)	1.19	0.62	0.02 (-37 dB)	0.048 (-33.2 dB)	2.04	2.64
Distance (mm)	12.5	10	13	15	10	10
WPT System Efficiency FoM**	8.46	68.1	43.94	20.25	80.3	102.1

4.5 Conclusions

Miniaturized electrocortical neural interfaces are essential for next-generation brain-computer-interface systems. The wireless-power-receiver-on-Chip presented in this chapter enables ultimate miniaturization of implants by integrating WPT components on-chip such as a coil. The presented H-Tree power and signal distribution for eliminating any possible loops systematically and implementing equidistant signal path is crucial for ultimate miniaturized on-chip WiPow-RX. To widen RF input-range, multi-mode B^2R^3 is also presented and experimentally characterized. System-level validation for the B^2R^3 is provided with measurement results of an AFE and ASK module.

Acknowledgments

Chapter Four is largely a combination of material that will be submitted to the IEEE Journal of Solid-State Circuits and appeared in 2016 Symposium on VLSI Circuits: C. Kim, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs, "A Miniaturized Fully Integrated Wireless-power-receiver-on-chip with an Adaptive Buck-boost Regulating Rectifier and Low-loss H-tree Signal Distribution," in IEEE Journal of Solid-State Circuits (JSSC), in

preparation. C. Kim, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier and G. Cauwenberghs, "A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and Low-Loss H-Tree Signal Distribution," 2016 Symposium on VLSI Circuits, Kyoto, June 2016. C. Kim is the primary author and investigator of the work.

C. Kim, P. P. Mercier and G. Cauwenberghs organized the work. C. Kim wrote the first draft of the paper, with J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang contributing several sections. P. P. Mercier and G. Cauwenberghs contributed to edit the paper.

Chapter 5

A 92dB dynamic range sub-μVrms noise 0.8μW/ch neural recording ADC array with predictive digital autoranging

5.1 Introduction

High-density multi-channel neural recording is critical to driving advances in neuroscience and neuroengineering through increasing the spatial resolution and dynamic range of brain-machine interfaces. Neural signal acquisition ICs have conventionally been designed composed of two distinct functional blocks per recording channel: a low-noise amplifier front-end (AFE), and an analog-digital converter (ADC) [10, 13]. Hybrid architectures utilizing oversampling ADCs with digital feedback [30, 33, 62] have seen recent adoption due to their increased power and area efficiency. Still, input dynamic range (DR) is relatively limited due to aggressive supply voltage scaling and/or kT/C sampling noise. This paper presents the first neural recording ADC chip with 92dB dynamic range and 0.99μVrms of noise at 0.8μW power consumption per channel over 500Hz signal bandwidth, owing to *i*) a predictive digital autoranging (PDA) scheme in a hybrid analog-digital second-

order oversampling ADC architecture, *ii*) no specific sampling process through capacitors avoiding kT/C noise altogether. Digitally predicting the analog input at 12-bit resolution from a single-bit quantization of the continuously integrated residue at effective 32 oversampling ratio (OSR), the PDA handles a ±130mV electrode differential offset (EDO) and recovers from >200mVpp transient artifacts within <1ms. Furthermore, using digital circuits for integration ensures the architecture benefits from process scaling and the resulting compactness makes it suitable for incorporation in high-density recording arrays.

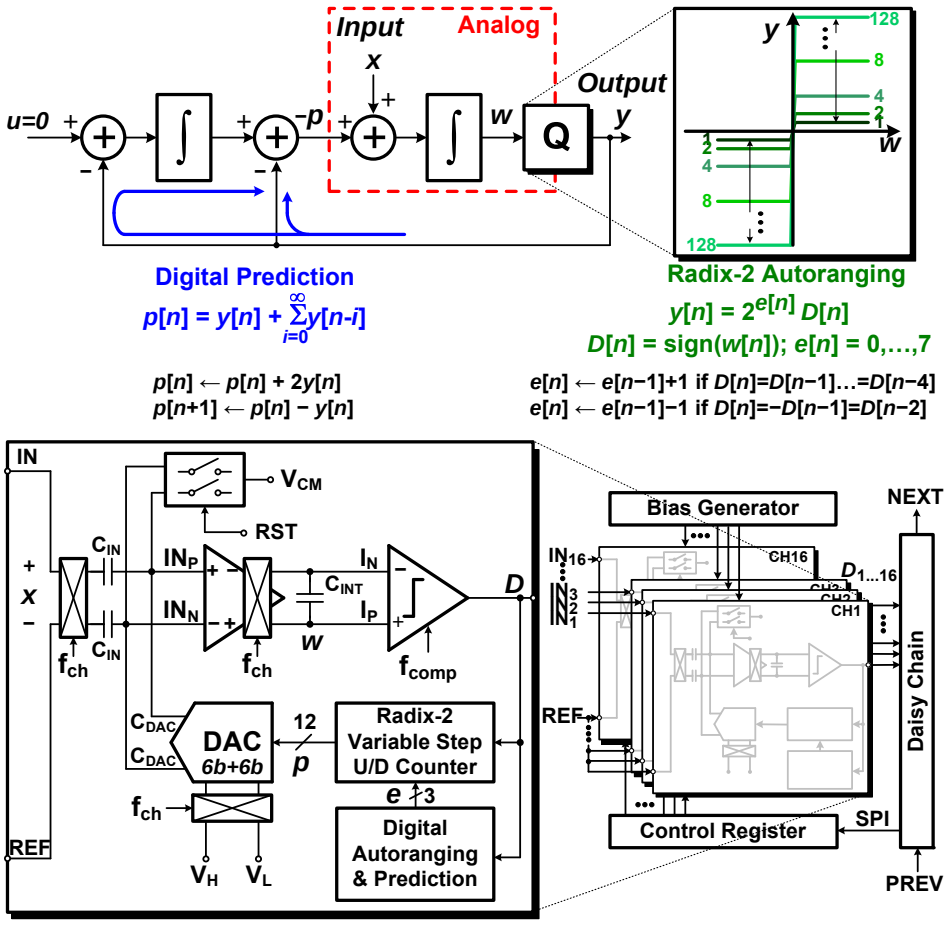


Figure 5.1: System diagram and circuit architecture of predictive digital autoranging (PDA) neural ADC.

5.2 ADC Architecture

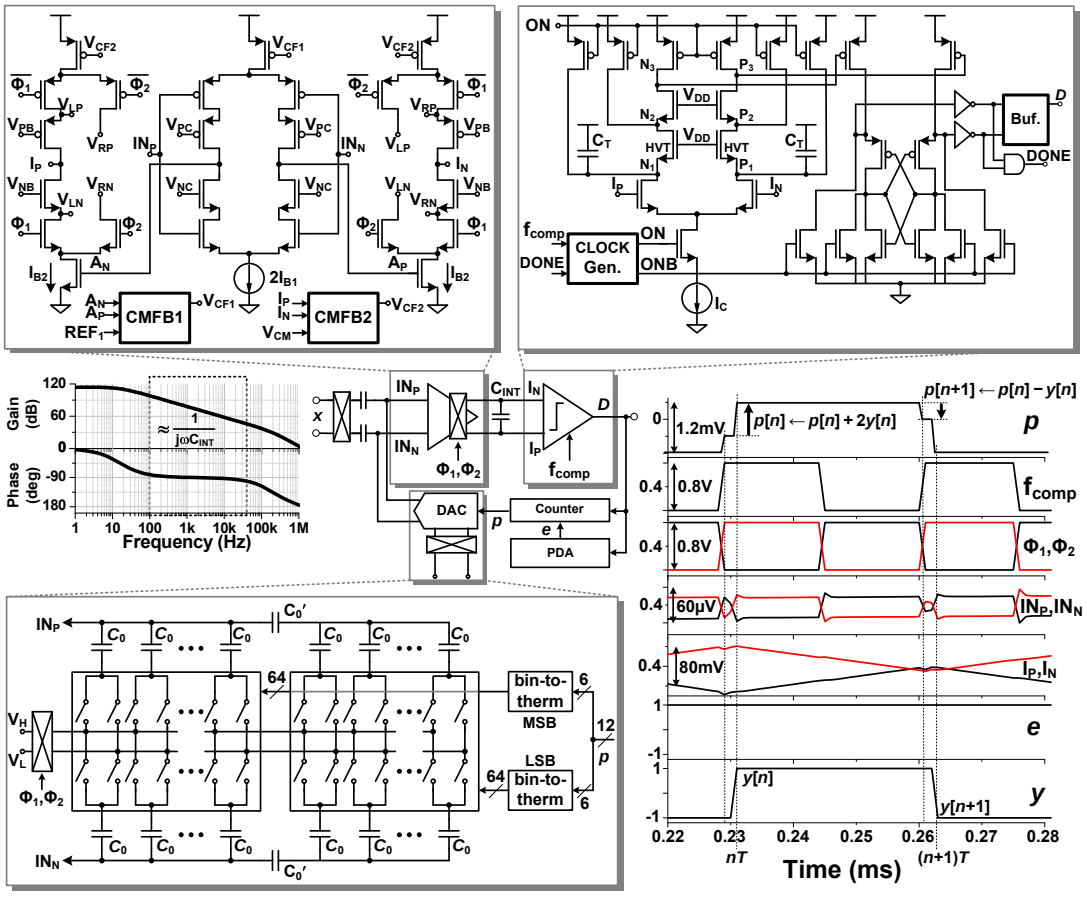


Figure 5.2: PDA neural ADC circuit implementation and timing waveforms.

Fig. 5.1 presents the system diagram circuit architecture for one of 16 ADC channels in the neural signal acquisition IC, with the analog integrator and comparator highlighted. The digital feedback along with the continuous analog integration implements a second-order predictive loop accommodating for potentially large offset and slope at the input, such as EDO in the DC-coupled input and higher-frequency content in the signal at relatively low OSR. Unlike conventional second-order delta-sigma modulation, the input enters the second integrator, where zero input to the first integrator ($u = 0$) ensures stable saturation-free loop dynamics with only single-bit quantization (Fig. 5.1 top). The resulting first-order differentiation in the signal transfer function produces first-order noise-shaping of

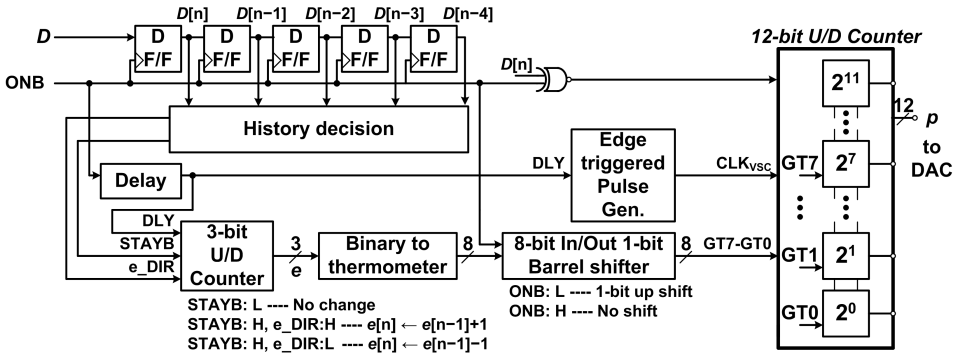


Figure 5.3: Detail of integrated digital circuits to update the state variables for digital prediction and autoranging.

the quantizer in the input; however, the extra loop gain contributed by the first digital integrator leads to improved resolution owing to digital prediction improving with OSR. The dynamic range and transient response of the ADC loop are substantially improved by radix-2 autoranging of the quantizer, in which the history of the quantizer bits $D[n]$ triggers either a factor two expansion or contraction in the digital feedback from the quantizer $y[n]$. A 3-bit exponent $e[n]$ covers 7 octaves (1, 2, ... 128) in digital gain, where a run of five successive decisions with identical polarity increments the exponent expanding the range, whereas a run of three alternating polarity decisions decrements the exponent contracting the range. The combination of digital prediction and radix-2 autoranging constitutes PDA. A reference-chopped 12-bit 6b-6b segmented DAC reconstructs $p[n]$, the predicted analog value of the chopped input, with the resulting residue $x[n]$ - $p[n]$ unchopped to baseband for continuous-time integration onto C_{INT} and quantization (Fig. 5.1 bottom). The digital prediction $p[n]$ in turn is obtained as the instantaneous sum of the digital feedback $y[n]$ and its running accumulation, completing the second-order loop. A radix-2 variable-step up/down counter implements the update in $p[n]$ in two phases: a double increment/decrement step at the counters binary input position $e[n] + 1$, followed by a retracing step with opposite polarity at input position $e[n]$ just before the next cycle. The 16 channels on-chip share common reference, bias and control signals, and their outputs $D_{1..16}[n]$ are daisy-chained at the output to enable higher channel counts through cascaded multi-chip configuration.

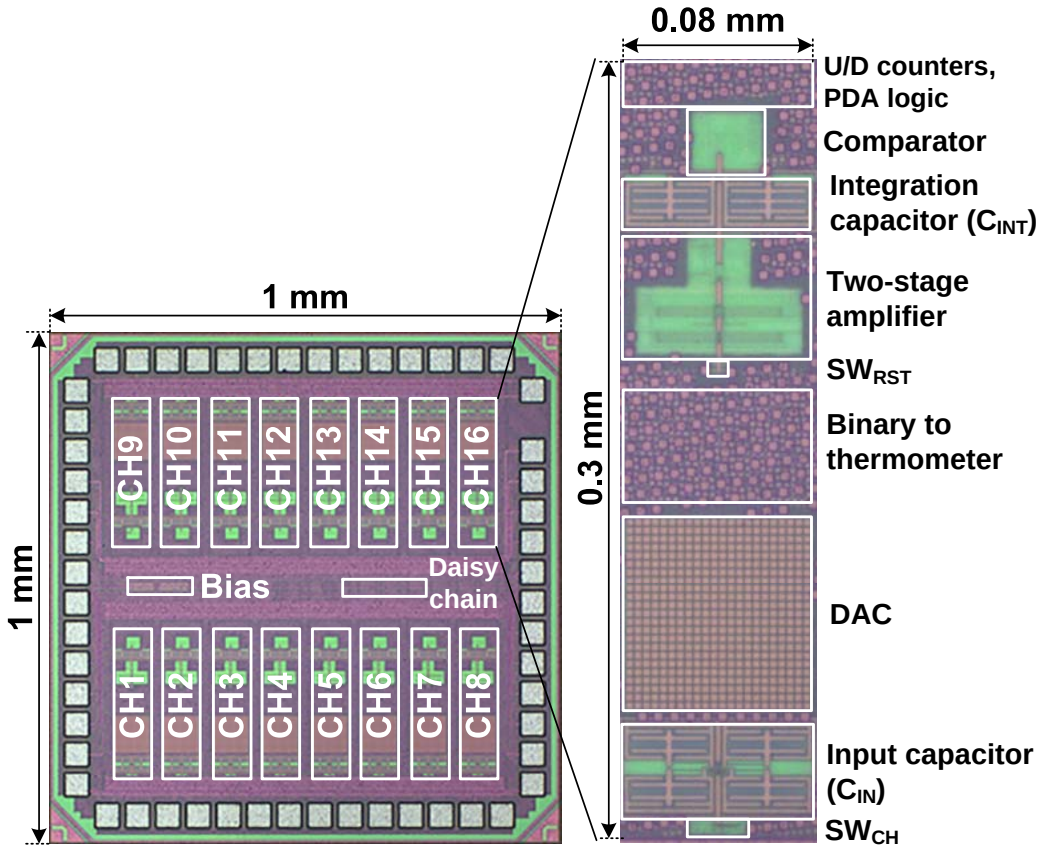


Figure 5.4: 16-channel PDA neural ADC IC micrograph and single channel detail.

A 2-stage fully-differential amplifier (Fig. 5.2 top left) with two independent stages of common- mode feedback feeds into a 1.35pF integration capacitor C_{INT}. Current biases for I_{B1} and I_{B2} are set to 375nA and 25nA, respectively. Current-reusing nMOS and pMOS input pairs in the first stage boost transconductance to 22µS for improved NEF, while 600mVpp output swing at 0.8V supply in the second stage increases spurious-free dynamic range. Simulated signal gain of the integrator is greater than 46dB near the 32kHz chopping frequency (Fig. 5.2 center left). A two-stage comparator (Fig. 5.2 top right) performs single-bit quantization. Decision time ranges from 1.5µs to 2µs depending on input amplitude, dominated by capacitive loading (C_T = 20fF) of the first-stage current-starved (I_C = 20nA) pre-amplifier. Each of two differential segmented 6b+6b DACs is implemented with two 64-element custom arrays of 2fF unit capacitors C_0, bridged by 4% larger

capacitor C_0 (Fig. 5.2 bottom left). Timing of the two-phase updates in the digital prediction state variable p is triggered by initiation and settling of the comparator output (Fig. 5.2 bottom right). Digital circuits are shown in Fig. 5.3. The digital circuits are clocked from a direct or delayed signal of a comparator output, ONB. A chain of 5 D-flip flops holds the history of the 5 recent ADC outputs. Based on this history, the exponent $e[n]$ for autoranging is updated. In order to implement $2\times y[n]$, updated exponent $e[n]$ is converted to 8-bit thermometer code and 1-bit shifted up through a 8-bit in/out barrel shifter. A 8-bit output is utilized for clock gating of 8 units of a 12-bit up/down counter to update its LSB. For example, if $e[n] = 0$, then, the 1-bit shifted up thermometer code becomes '00000001' and as a result, the unit receiving $GT0$ clock is gated. The outputs of the 12-bit up/down counter are directly connected to binary to thermometer code converter shown in the bottom-left figure of Fig. 5.1. At the rising edge of next clock cycle (f_{COMP}), ONB is asserted to implement $p[n+1] \leftarrow p[n] - y[n]$. In order words, the 12-bit up/down counter is updated twice within 1-clock cycle with the edge triggered pulse generator that provides short-pulse signal at rising/falling edge of the its input, delayed ONB signal.

5.3 Measurements

5.3.1 Measurement results for benchtop experimental characterization

The 16-channel neural ADC array measures 1mm×1mm in 65nm CMOS, with 0.024mm^2 per channel as shown in Fig. 5.4. Measurement set-up for electrical tests such as input-referred noise, bandwidth, artifact recovery, and input dynamic range is shown in Fig. 5.5.

Fig. 5.6 shows the measured input-referred noise of the combined front-end and ADC. Chopping above 8kHz reduces the noise density below 50nV/$\sqrt{Hz}$, resulting in 0.99μVrms integrated input-referred noise and 1.81 noise efficiency factor (NEF) at 32kHz chopping frequency and 1μA supply. The measured effect of

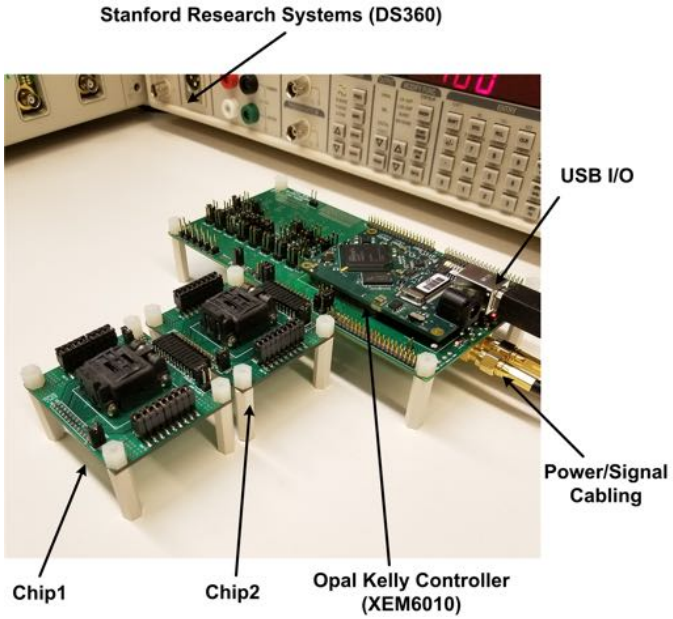


Figure 5.5: Experimental setup for benchtop characterization with I/O control console PCB and daisy-chain cascade of satellite PCBs each with 16-channel neural ADC IC.

PDA on transient response is highlighted in Fig. 5.7. Without PDA, the response to a large step transient is slew rate limited due to unity increments/decrements in the digital feedback. With PDA, measurements show a 30× bandwidth improvement for 4mV amplitude signals, and <1ms recovery to ±100mV input transients. The measured effect of PDA on increasing dynamic range is shown in Fig. 5.8. PDA extends the signal range at greater than 50dB SNDR by 22dB, approaching the full range of the DAC, covering 92dB input dynamic range (Fig. 5.8 bottom). The SNDR improvements at large signal amplitude results from both reduced spurs and reduced noise floor (Fig. 5.8 top).

5.3.2 *in vivo* test

The test set-up for *in vivo* recording of frontal cortex local field potentials in a marmoset primate subject (*Callithrix jacchus*) under visual stimulation is shown in Fig. 5.9. In vivo local-field potential (LFP) recordings using the 16-channel neural acquisition IC connecting to a NeuraLynx microwire electrode array inserted

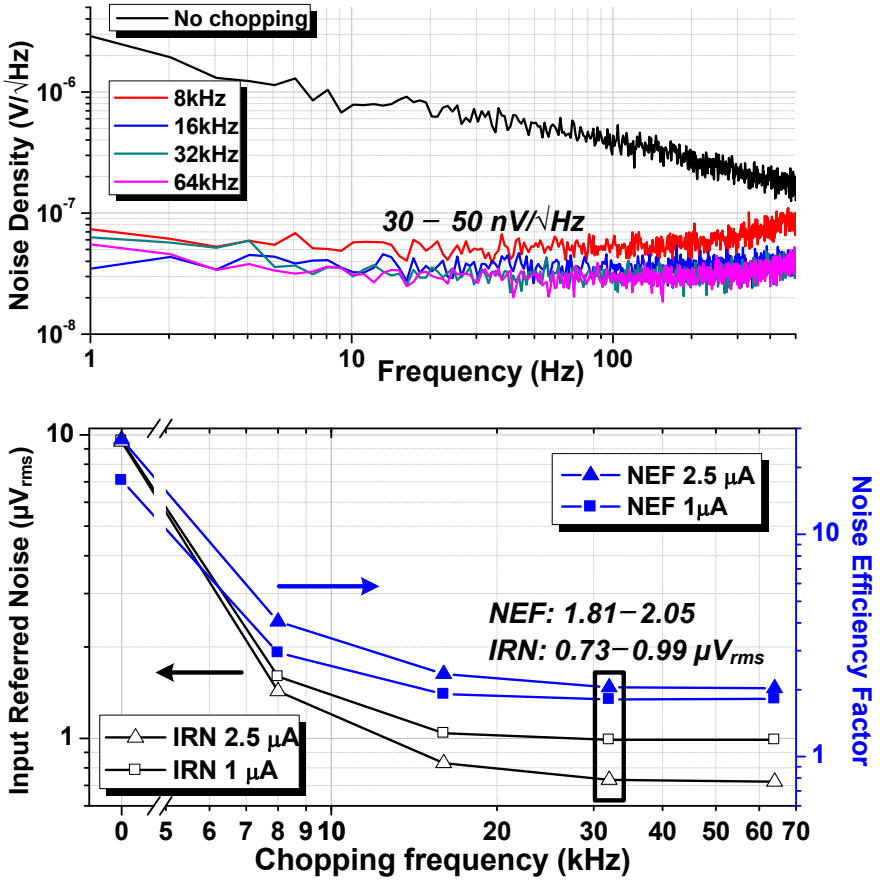


Figure 5.6: Measured noise spectral density and integrated noise for varying chopping frequency and supply current.

in frontal cortex of a marmoset primate (Callithrix jacchus) are shown in Fig. 5.10 (top), resolving slow potentials (<0.1Hz) indicative of subject arousal state that are often missed by AC-coupled commercial neural instrumentation without severe degradation in SNR [26].

5.3.3 Performance comparison

Comparison of key metrics with the state-of-the-art in neural recording ICs is given in the Table (Fig. 5.10 bottom). In addition to NEF, the neural ADC achieves a power efficiency factor (PEF) of 2.6, almost a fourfold improvement among integrated front-end ADCs reported in the literature.

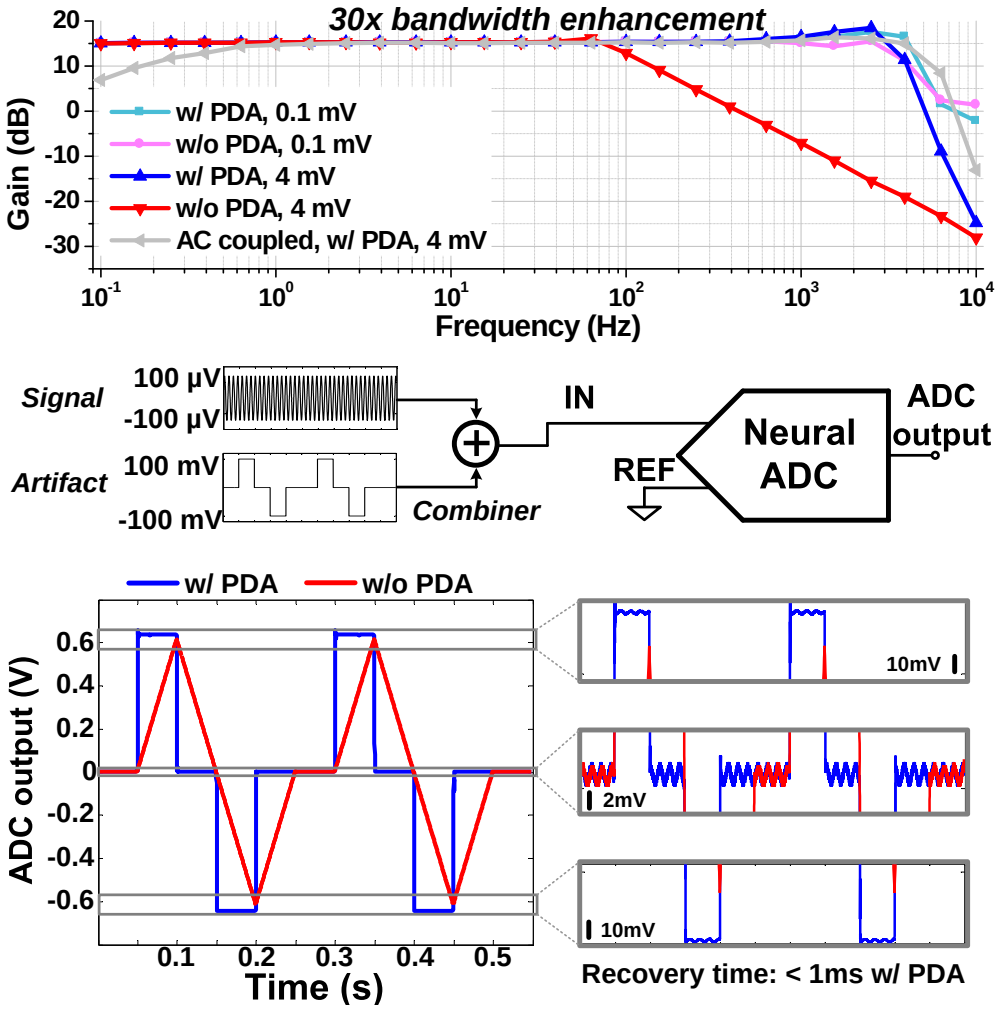


Figure 5.7: Measured large-signal bandwidth and transient response, with and without PDA.

5.4 Conclusion

This chapter presents the first neural recording ADC chip with greater than 90dB dynamic range, less than 1µVrms of noise at less than 1µW power consumption on per channel at 500Hz bandwidth, owing to a novel predictive digital autoranging scheme in a hybrid analogdigital second-order oversampling ADC architecture. It offers the best published figureofmerit for neural ADCs with a noise efficiency factor (NEF) of the combined frontend amplifier and ADC of 1.81, and a corresponding power efficiency factor (PEF) of 2.6. It is further capable of recording <0.01Hz slow potentials as well as recovering from >200mVpp

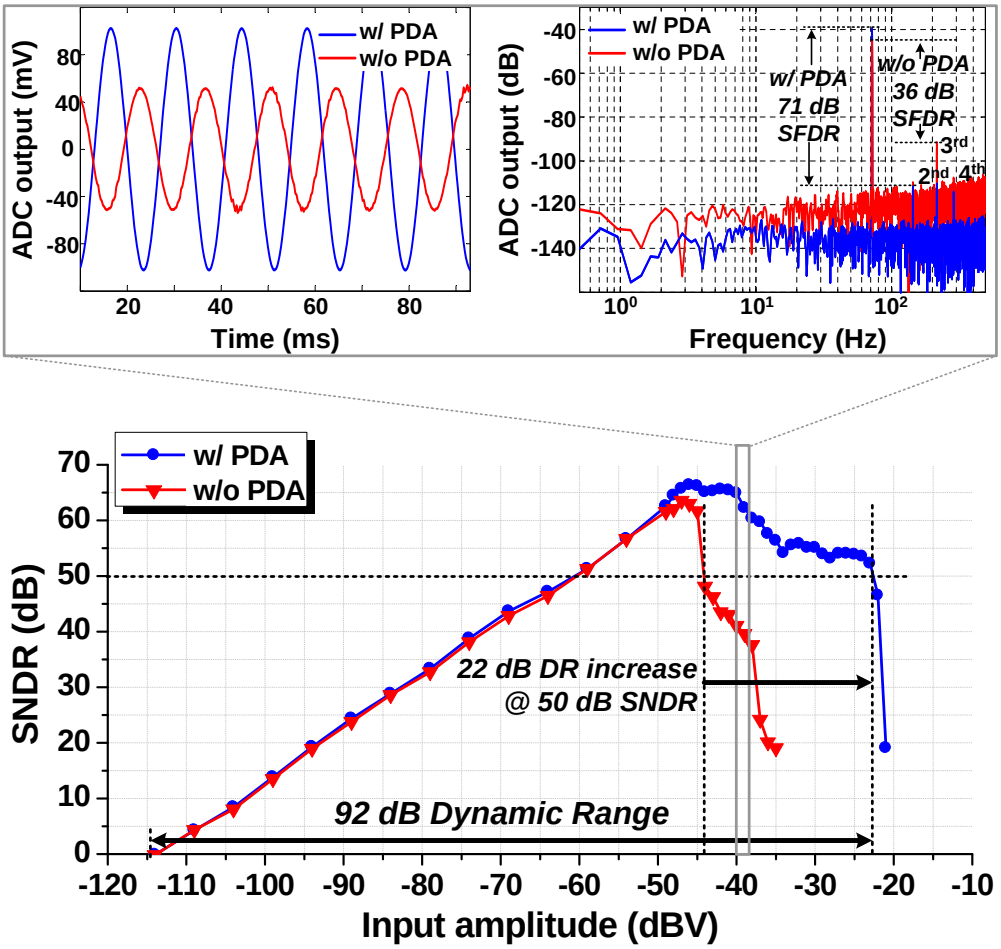


Figure 5.8: Measured output, signal-to-noise-and-distortion ratio, and dynamic range, with and without PDA.

transients in <1ms that are important in electrocortical recording. In vivo results from marmoset frontal cortex demonstrate the unique capabilities.

Acknowledgments

Chapter Five is largely a reprint of material that will appear in the 2018 IEEE International Solid-State Circuits Conference (ISSCC): C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92dB dynamic range subμVrms noise 0.8μW/ch neural recording ADC array with predictive digital

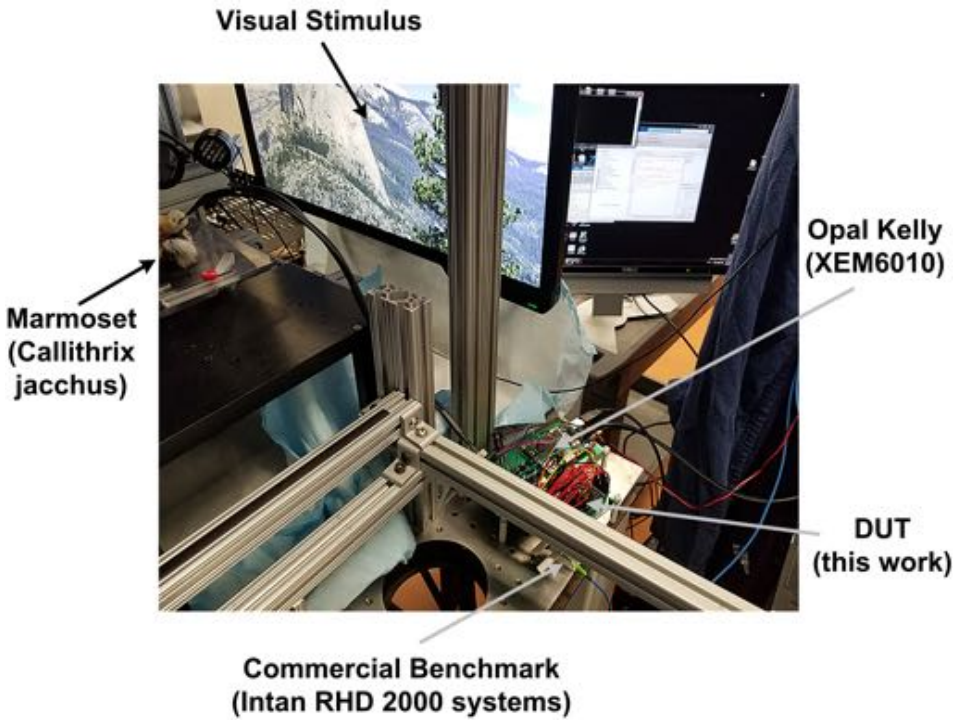
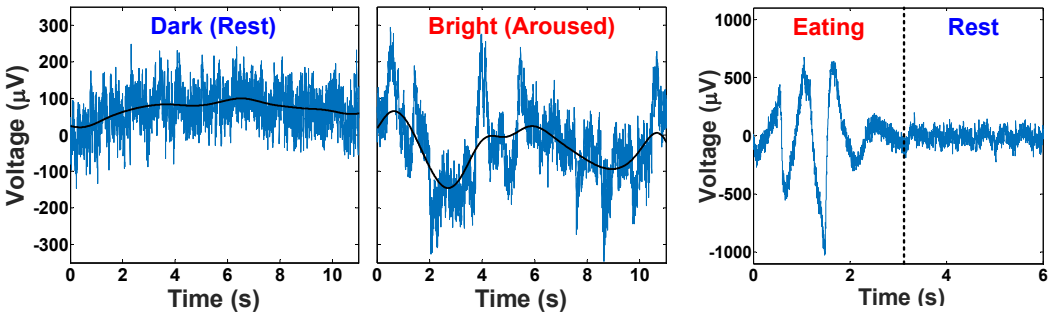


Figure 5.9: Experimental setup for *in vivo* recording of frontal cortex local field potentials in a marmoset primate subject (*Callithrix jacchus*) under visual stimulation.

autoranging," 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, Feb. 2018, to appear. C. Kim is the primary author and investigator of this work.

C. Kim, H. Courellis, C. Miller and G. Cauwenberghs conceived and organized the project. S. Joshi, H. Courellis and J. Wang, contributed on several sections and layout. C. Kim wrote the first draft of the paper, and S. Joshi and G. Cauwenberghs contributed in editing the paper.



	Chen JSSC14	Chandra-kumar ISSCC17	Muller JSSC15	Kassiri ISSCC17	Johnson VLSI17	Kim ISSCC18
Power/Ch (μW)	0.97	2.8	2.3	0.63	8	0.8
Supply voltage (V)	1.8	1.2	0.5	1.2	1	0.8
Noise density (nV/√Hz)[a]	63	127	58	101	71	44
NEF	1.77[b]	7.4[b]	4.76	2.86	7.8	1.81
PEF ($NEF^2 V_{DD}$)	5.6[b]	66[b]	11.3	9.8	60.8	2.6
ENOB (bits)	9.57	--	--	11.7	10.2	10.7
Dynamic range (dB)	--	81[c]	50[c]	--	90	92
EDO range (mV_{pp})	N/A[d]	N/A[d]	100	rail-to-rail	100	260 / N/A[d]
Rapid recovery	no	no	no	no	yes	yes
Area/Ch (mm^2)	0.09	0.069	0.025	0.013	0.06	0.024
Technology (nm)	180	40	65	130	180	65

[a]√(Input-referred noise²/BW), differential configuration
[b]front-end amplifier only, excluding ADC
[c]SNDR=0dB estimated from input-referred noise
[d]AC-coupled

Figure 5.10: *In vivo* LFP recordings from marmoset frontal cortex, and metric comparison with state of the art.

Chapter 6

A 7.86 mW +12.5 dBm In-Band IIP3 8-to-320 MHz Capacitive Harmonic Rejection Mixer in 65nm CMOS

6.1 Introduction

Spectral over-crowding has become a major concern considering the vast number of communication bands below 3 GHz (cellular, industrial, commercial TV, etc.) [21]. Such spectral over-crowding places strict constraints on the transceiver design in terms of susceptibility to out-of-band jammers desensitizing the receiver. Traditionally, to overcome the potential out-of-band jammers from near-by communications, many off-chip band-selecting filters, which are frequency fixed, are employed accompanied by power hungry receivers, which is undesirable. To meet the future needs of growing receiver complexity and desired agility, a fully integrated, highly tunable, low power, and robust receiver is desired.

Recently, passive mixer first receivers have gained popularity due to their highly linear nature making them appealing for cognitive radios operating in unoccupied TV bands. However, these approaches generally suffer from harmonic

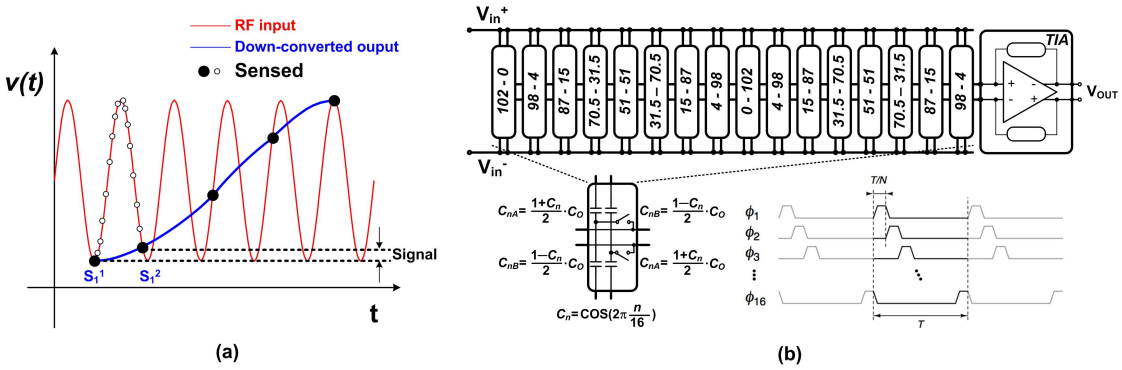


Figure 6.1: (a) Conceptual diagram for 16-phase discrete down conversion. (b) Sinusoidal weighted capacitive array for capacitive harmonic rejection mixer. The numbers of unit capacitors for each path shown are weighted double differentially. The 16-phase LO switch clocks ϕ_{1-16} are time interleaved.

folding and poor noise performance. [9, 45, 65, 73]

This paper presents a low power, linear passive mixer first receiver that implements a sinusoidal weighted switched capacitor array for harmonic folding rejection. A 16 phase sinusoidally weighted capacitor array is implemented for linear, low noise, harmonic rejection mixing and a low power PLL is implemented to create the multi-phase clock reference. Measurement results demonstrate an analog core power consumption of 40 μW per complex I/Q channel, with the PLL clock generation and distribution circuity consuming 7.82 mW, achieving an in-band IIP3 of 12.5 dBm for the implemented capacitive harmonic rejection mixer (HRM).

6.2 Capacitive Harmonic Rejection Mixing Principle

As an alternative to the conventionally used transconductance weighting in harmonic rejection mixing [5, 65, 73] we present a sinusoidally weighted capacitor array implementing a HRM. Owing to lower capacitor ratio mismatches and intrinsically zero power dissipation, capacitively weighted HRM offers the potential to outperform transconductance weighted HRMs in harmonic suppression and en-

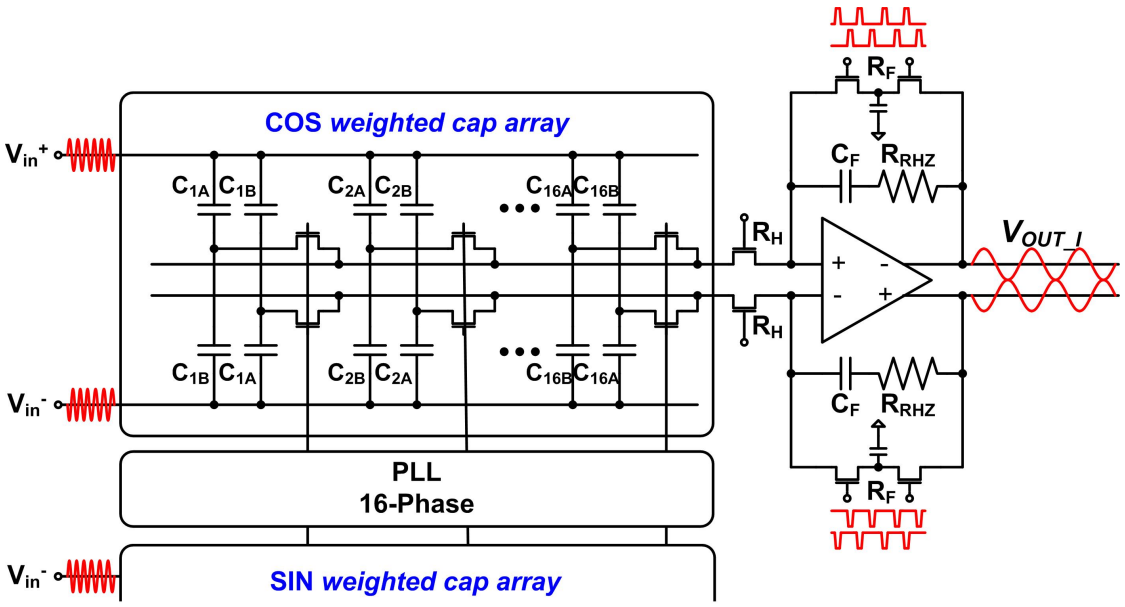


Figure 6.2: CMOS circuit implementation of the capacitive HRM with TIA and PLL.

ergy efficiency. Furthermore, capacitive weighting is inherently noise-free, whereas transconductance weighting is subject to thermal noise. The proposed capacitive harmonic rejection mixing, shown in Fig. 6.1 (a), reconstructs the down-converted baseband signal by accumulating the differentials of the sensed RF input at each cosine-weighted capacitor. A switched capacitor array implements 16-phase discrete harmonic modulation of the RF input as shown in Fig. 6.1 (b). By double-differential encoding of the 16-phase modulation sinusoid, each phase using 4 double-complementary capacitors, the RF input as well as the baseband transimpedance amplifier (TIA) see a constant capacitive load. Unit-capacitor-based sizes that discretely approximate the weighting factors for a given target of 60 dB rejection are given in Fig. 6.1. (b), where the half units are implemented using series combinations of the unit capacitors. A 10 fF unit capacitance is chosen as a tradeoff between area, mismatch, and energy efficiency. The charge injected by the harmonic rejection mixing capacitive array is summed and band-pass filtered by the combined effects of the baseband TIA and capacitors. With this simple structure, we implement harmonic rejection mixing, amplification, and filtering

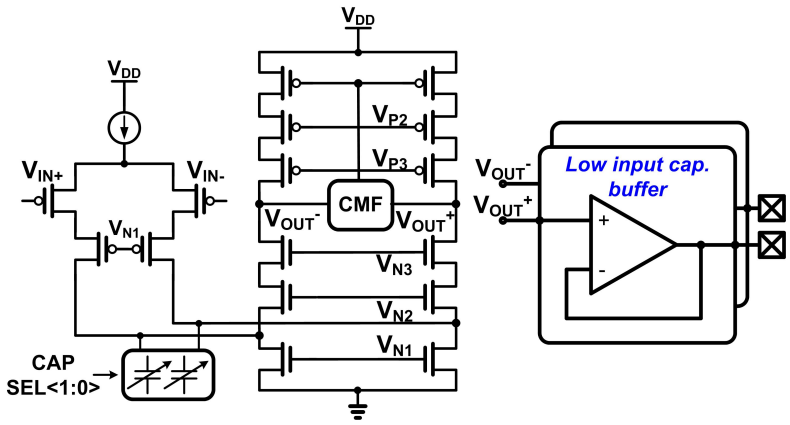


Figure 6.3: Fully differential OTA with low input capacitance buffer.

with only one OTA, resulting in low-power consumption.

6.3 Circuit Implementation

6.3.1 Low-Power Sinusoidal-Weighted Capacitive Array

Fig. 6.2 illustrates the implemented quadrature HRM, with only the I path shown. The I/Q paths are mirror-symmetric with cosine and sine weighted capacitive arrays, respectively. Furthermore, all bias, control and clock signals are shared in both paths for lower power consumption and better matching.

Unlike conventional transconductance-based harmonic rejection passive mixing, the size and on-resistance of the switches are not critical for matching, dynamic range, and linearity in this architecture. Furthermore, to first order, the switch mismatch does not contribute to harmonic rejection. Therefore, minimum length sized nMOS switches are used to lower power dissipation and to reduce the impact of charge injection and clock feed-through. The width was decided based on the charge transfer capabilities within the on phase of the clock, i.e. T/N shown in Fig.6.1 (b). Fig. 6.2 also shows an additional resistance, R_H, common for all clock phases, inserted to uniformly filter switching noise, and implemented with a pair of long nMOS transistors to ensure robustness to process variation.

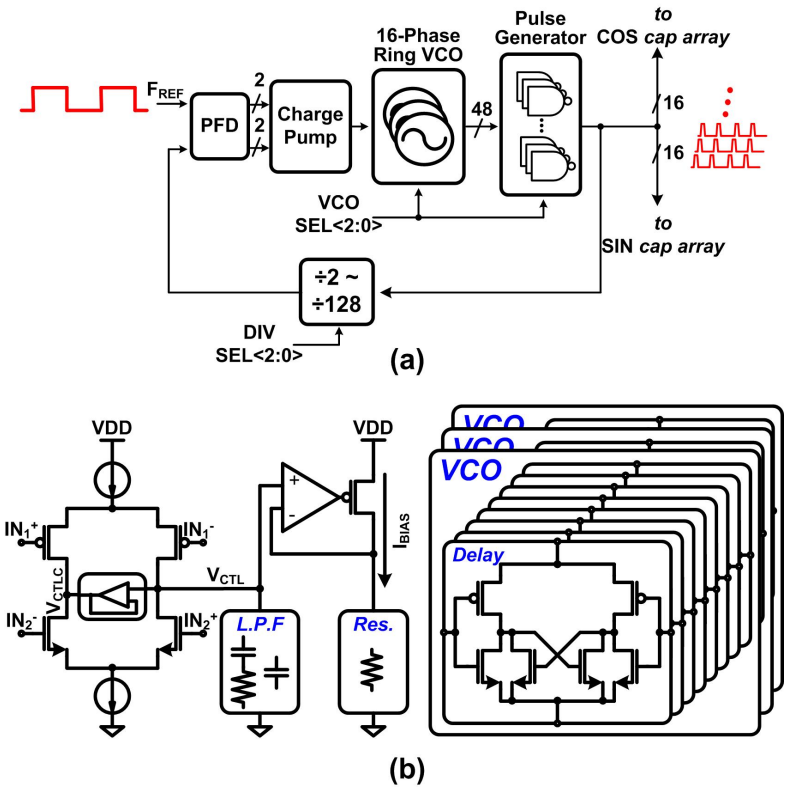


Figure 6.4: (a) Block diagram of the 16-phase PLL with 3 VCOs. (b) Charge pump and VCO.

6.3.2 TIA and Clock Generation

As presented in Fig. 6.2, the HRM TIA output stage implements a band-pass characteristic. The low-pass cut-off frequency depends on the transconductance of the OTA G_m, the nMOS resistance R_H, and total input capacitance $N\,C_O$ with $N = 16$. The high-pass cut-off is determined by a switched-capacitor resister R_F and the feedback capacitor C_F. The mid-band gain is set by the capacitance ratio $N\,C_O\,/\,C_F$. The programmable gain is obtained by varying the feedback capacitor C_F from 8 to 512 fF in powers of 2. The right-half-plane (RHP) zero in the TIA due to the C_F feed-through path is eliminated by inserting a series resistance R_{RHZ} with value $1\,/\,G_m$. Switching frequency control over the switched-capacitor resistance R_F allows for tuning of the high-pass cut-off to reduce the effects of $1/f$ noise.

In Fig. 6.3, the implemented fully differential three-stacked folded cascode

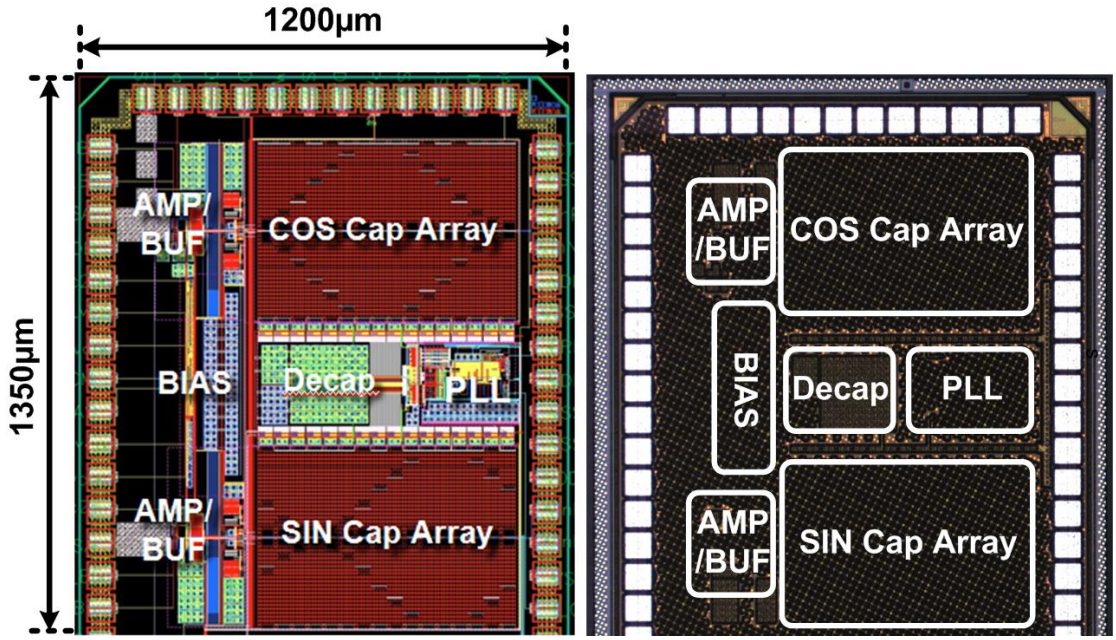


Figure 6.5: Chip layout (left) and micrograph (right). Sinusoidally-weighted ratios in the capacitor arrays are clearly shown in the layout.

OTA is shown. Subthreshold MOS operation offers high gain and linear current transconductance tuning owing to maximized g_m/I_D efficiency. The input cascode stack can help reduce the Miller effect across the C_{gd} capacitors of the input pair. For improved low-pass filtering at higher frequency, we intentionally lower the second pole of the OTA by inserting capacitors shown in Fig. 6.3 (a). For further improving power consumption, an ultra-low input capacitance buffer [16] is used to limit the total load capacitance seen by the TIA thus maintaining bandwidth efficiency.

The 16-phase clocks required for harmonic rejection are generated using a PLL described in Fig. 6.4 (a). The PLL has three 16-phase VCOs with frequencies ranging from 8–30 MHz, 200 MHz–1 GHz and 1–3 GHz, respectively. Digital gates generate pulse waveforms from these VCO outputs to drive the mixer. Fig. 6.4 (b) shows the core parts of the PLL. A unity gain buffer is used to decrease the effect of V_{DS} mismatch at the charge pump. The V_{CTL} voltage generated by the charge pump and loop filter is converted to a current through a rail-to-rail V-I converter for wide-frequency dynamic range. This PLL draws up to 1.5mA at 1.2V.

Table 6.1: Comparison of Measured Performance

		[65]	[45]	[73]	[9]	[2]	[81]	[38]
Power	Mixer & Analog[mW]	27	5.4	91.8	189 [1]	16	67	.04
	Clock [mW] @ LO [MHz]		-	10.4 @ 100		12.5 @ 3,800		7.82 @ 320
IIP3 [dBm]		5.01	8-9	12	-15	-3.5 [3]	11	12.5
P_{1db} [dBm]		-	-	-	-	-	-	-5.5
DSB NF [dB]		19	12	11	8	5	6.5	11
3^{rd} HRR [dB]		-	-	>52	>70 [2]	38 [3]	-	40
Technology		250nm BiCMOS	130nm CMOS	110nm CMOS	180nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS

[1] Including LNA

[2] After calibration

[3] Full receiver

6.4 Measurement Results

The chip was fabricated in a 65-nm CMOS process. Fig. 6.5 shows the layout and chip micrograph. The active area is 1.62 mm^2. The majority of the area is occupied by the weighted capacitor arrays (0.6 mm^2). Owing to the double-differential capacitance encoding, each differently weighted capacitor block has the same area, with the sinusoidal weights clearly visible in the layout. A fingered metal capacitor is adopted as the 10 fF unit capacitor. The use of high layer metals ensures reduced parasitics to the substrate.

For the measurement setup, two-tone differential input signals are generated through two single-ended MXG N5181A signal generators with a combiner and a balun. A PSA E4448A spectrum analyzer with high-current driving buffers and a DPO7254 oscilloscope are used to probe output signals.

Fig. 6.6 (a) shows the input (V_{IN}) and output (V_{OUT}) signals of the capacitive HRM for a two-tone test. The input signal combined with two equal-power tones at 320.35 MHz and 320.42 MHz is down-converted with an LO of 320 MHz

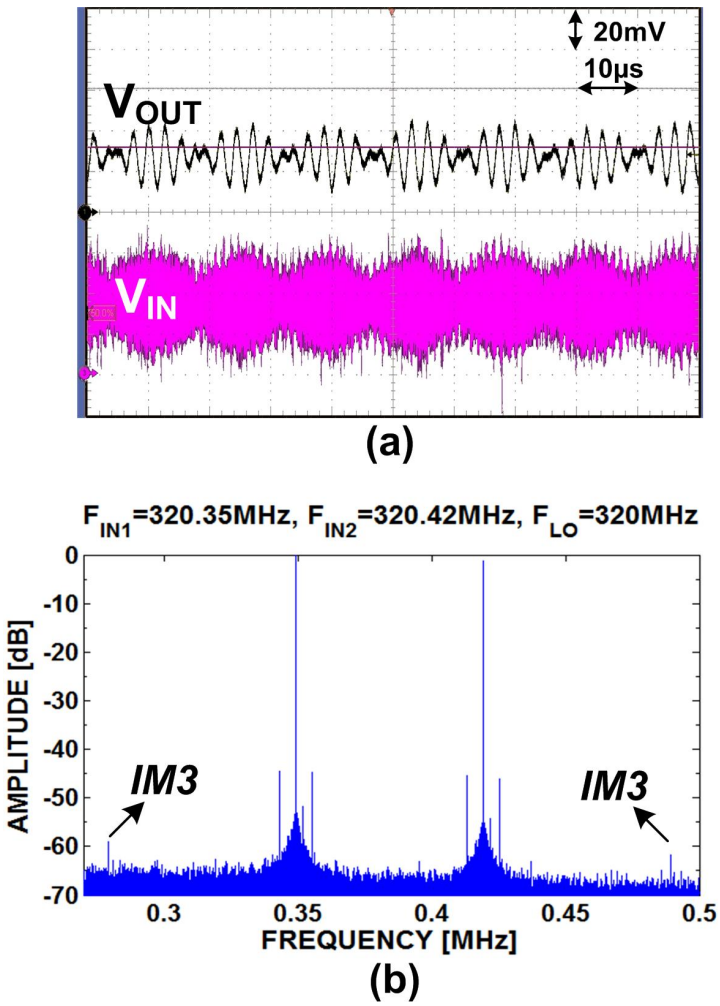


Figure 6.6: (a) Two-tone test. (b) Frequency spectrum showing intermodulation of the third-order harmonics.

to two tones at 0.35 MHz and 0.42 MHz. The spectrum of the output shown in Fig. 6.6 (b) shows a 3rd-order inter-modulation product around 60 dBc.

The input power compression point, third order intermodulation distortion and third-order intercept point are shown in Fig. 6.7. The P_{1dB} and in-band IIP3 are measured to be -5.5 dBm and $+12.5$ dBm, respectively. The measurable lowest IM3 is -74 dBc at -23.5 dBm input. The measured harmonic rejection ratio is 40 dB, limited in the current implementation by clock skew and phase mismatch in the 16-phase PLL LO. Table I summarizes the performance along with state-of-the-art references.

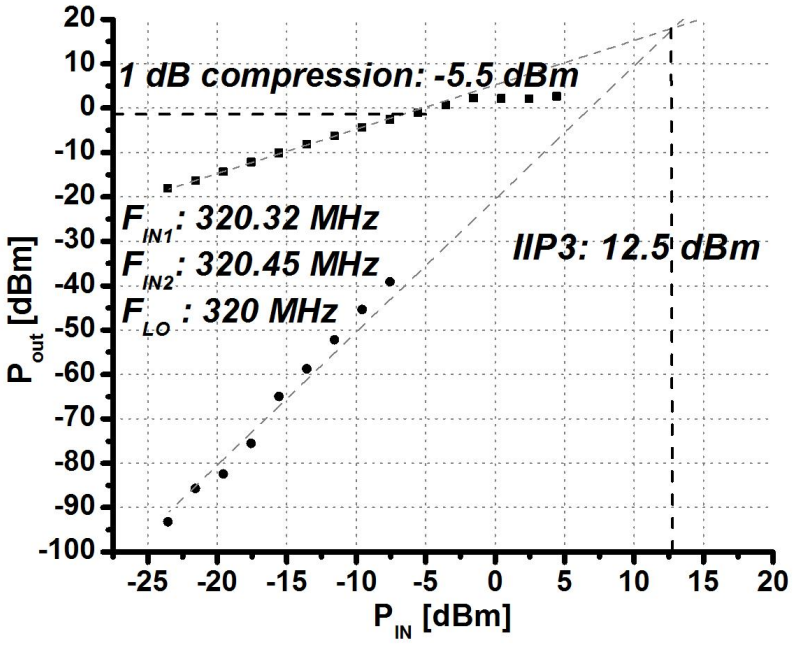


Figure 6.7: Two-tone linearity test showing in-band IIP3 and P_{1dB}.

6.5 Conclusion

A 16-phase sinusoidally weighted capacitive harmonic rejection downconversion mixer is presented as a low-power, high-linearity alternative to conductance-based mixing. In 65nm CMOS the implemented mixer shows +12.5 dBm of IIP3 in-band linearity at 40 μW power consumption per I/Q complex output channel. Decreased MOS switch size in charged-based harmonic rejection mixing, and sub-threshold region operation of fully differential transconductance amplifiers in gm-C baseband filtering contribute to enable micropower RF mixing. Overall power consumption of the mixer is 7.86 mW dominated by 16-phase PLL LO clock generation and distribution up to 320 MHz fundamental frequency (5.12 GHz per phase). Further power savings and higher harmonic rejection may result from direct digital synthesis of the LO.

Acknowledgments

Chapter Six is largely a reprint of material in the Proceedings of the ESSCIRC 2014: C. Kim, S. Ha, C. M. Thomas, S. Joshi, J. Park, L. E. Larson, and G. Cauwenberghs, "A 7.86 mW +12.5 dBm In-Band IIP3 8-to-320 MHz Capacitive Harmonic Rejection Mixer in 65nm CMOS," Proceedings of the ESSCIRC, Sep. 2014. C. Kim is the primary author and investigator of this work.

C. Kim, L. E. Larson and G. Cauwenberghs conceived and organized the project. J. Park contributed in building FPGA-based test structures. S. Ha, C. M. Thomas, S. Joshi, J. Park contributed in writing several sections and in conducting measurements.

C. Kim wrote the first draft of the paper, and C. M. Thomas and G. Cauwenberghs contributed in editing the paper.

Chapter 7

A 1.3 mW 48 MHz 4-Channel MIMO Baseband Receiver with 65 dB Harmonic Rejection and 48.5 dB Spatial Signal Separation

7.1 Introduction

Cognitive radio (CR) is emerging as an important area of research for efficient use of communication bandwidth over congested spectra [27, 75]. Due to the increase in applications in the mobile, military, wearable and biomedical space along with increasingly stringent energy constraints, a low-power receiver that enables dynamic allocation of available spectral bands, possibly against adversarial jammers, through spectrum sensing, signal separation, and classification is highly desirable.

Three key aspects of a CR receiver are spectral tuning, signal separation, and signal classification. This allows the receiver to tune to a desired band of operation, determine the presence and types of signals contained within that band, and then determine whether and how to communicate within that band to minimally interfere with the other signals. One objective of the CR approach presented

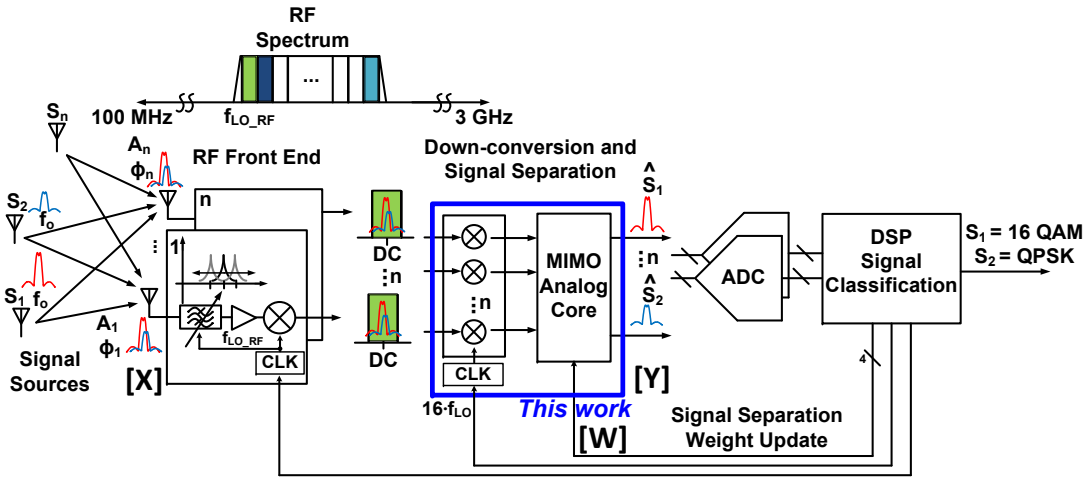


Figure 7.1: Combined spectrum and space aware cognitive radio with proposed MIMO baseband receiver.

here is to leverage spatial diversity in addition to spectral diversity, by integrating multi-input multi-output (MIMO) signal processing alongside spectral tuning and filtering in the CR receiver. Typically signal separation and classification rely on prior knowledge on key characteristics of the signal sources such as carrier frequency and modulation parameters. However, spatial diversity of signal reception across an array of distributed antennas allows separation of signal sources without such prior knowledge even when the signal spectra overlap completely [27].

Another objective of this work is to leverage advances in mixed-signal processing to alleviate dynamic range requirements in signal acquisition from the analog to digital domains, hence lowering overall power consumption of the CR receiver. Conventional signal separation and classification employs digital signal processors (DSP) following baseband analog-digital-converters (ADC) [76]- [91]. To enable sufficient signal resolving capabilities via DSP in the presence of a strong in-band jammer, an ADC with a high dynamic range (resolution) is required. Increasing the oversampling ratio (OSR) of the ADC can alleviate this at the cost of increased power consumption of both the ADC and the subsequent DSP. Thus, from a systems perspective, analog/RF preprocessing can significantly increase the energy efficiency by alleviating the requirement of high-resolution ADCs to

maintain high dynamic range under strong interference [75, 85].

System level considerations of these two objectives are outlined in Section 7.2. The proposed CR baseband receiver architecture [40], including harmonic rejection mixer (HRM) for spectral tuning and filtering, and MIMO analog core (MAC) for spatial source separation, is described in Section 7.3. Its low-power analog CMOS circuit implementation is detailed in Section 7.4. Measurements characterizing the HRM and MAC and the combined baseband receiver, and experimental validation of the overall system including antenna array and external RF front-end in separating RF modulated sources, are presented in Section 7.5. Lastly, conclusions are given in Section 7.6.

7.2 System Considerations

7.2.1 Spectrum and Space Aware Cognitive Radio

Fig. 7.1 shows the proposed spectrum and space aware receiver for CR composed of four parts: an antenna array providing spatial diversity, a RF front-end acquiring broad-band RF signals, a down-converting mixer and lowpass filter, and MIMO signal separator, followed by ADCs and DSP for identifying signals, deciding usable RF bands, and updating digital weights for signal separation.

A distributed geometry of multiple antennas receives a linear combination of signal sources $S_1, \ldots S_n$ present in the environment, each source and each antenna with a unique complex coefficient identifying mid-band amplitude gain and phase lag [27]. The amplitude and phase depend on the channel characteristics of each source as determined by attenuation and delay of its wavefront in relation to the antenna array. In turn, the amplitude and phase of the wavefront depend on frequency, and are approximately constant in a narrow frequency band. Hence, spectral and spatial diversity in the signal sources can be effectively leveraged by performing two-tiered spatiospectral signal separation: first tuning to a subset of signal sources within a given spectral band, followed by MIMO signal separation specific to that band. The maximum number of narrowband sources that can thus be separated equals the product of the number of spectral bands (spectral

multiplicity) and the number of antennas (spatial multiplicity). For broadband sources extending across multiple bands, the spectral components are separated separately in each band but can be identified and recombined for reconstruction, based on correspondence in angular or other spatial information derived from the MIMO weights.

The implemented system interfaces with a planar square array of four antennas, and covers sixteen 3-MHz spectral bands spanning 48 MHz with a center frequency tunable from 100 MHz to 3 GHz (Fig. 7.2). Hence, in principle a maximum of $4 \times 16 = 64$ sources can be jointly separated and spatially identified. The spectral selection of the 3-MHz band is done in two tiers: RF down-conversion by mixing with $f_{\text{LO\_RF}}$ from 100 MHz to 3 GHz and filtering at $\pm$24 MHz lowpass cut-off; followed by baseband up/down-conversion by complex mixing with f_{LO} from -22.5 MHz to 22.5 MHz in 3 MHz steps and filtering at $\pm$1.5 MHz cut-off. Hence coarse RF frequency selection is provided by $f_{\text{LO\_RF}}$, and fine baseband tuning is provided by f_{LO}, with the selected 3-MHz band centered at the sum frequency $f_{\text{LO\_RF}} + f_{\text{LO}}$. For modular implementation, the baseband up/down conversion by f_{LO} is combined with subsequent MIMO separation in the selected f_{LO} band on a single integrated circuit, as presented here. An RF front-end circuit at $f_{\text{LO\_RF}}$ is provided separately for each antenna, implemented on other integrated circuits using N-path tunable band-select filter [83], low-noise amplifier and RF quadrature mixer [38]. This arrangement with separate RF front-end and MIMO baseband receivers offers greater flexibility in tailoring specific CR applications than a single integrated solution: for instance, RF activity over 16 LO spectral bands can be monitored simultaneously using 16 parallel MIMO baseband receiver chips each operating at one fixed f_{LO}; or a single MIMO baseband receiver chip may suffice to scan the spectrum by hopping across f_{LO} bands.

7.2.2 Reduced Dynamic Range Requirement

The large dynamic range requirements imposed on the ADCs in CR have proven to be a major challenge for their widespread adoption in mobile applications [85], [74]- [84]. In-band jammers, typically 40 dB above the desired signal

in power, require an additional 6.6 effective number of bits (ENOB) in dynamic range in order to be able to resolve the signal at the same resolution using digital processing, leading to a 100-fold increase in ADC power consumption [85]. This severely constrains their use and prevents newly emerging devices in the mobile space from adopting CR technologies. However, dynamic range requirements and resulting ADC power consumption can be alleviated by analog pre-processing, prior to ADC [85, 87].

The proposed MIMO analog core (MAC) performs spatial filtering to recondition the signal and suppress the jammer through linear transformation, implementing high fidelity analog beamforming. Measurements (Section 7.5) demonstrate 68.5 dB jammer suppression in the MAC at less than 1 pJ of energy per multiple-accumulate. In what follows, we establish that the MAC pre-processing results in significant overall energy savings compared to the conventional approach directly quantizing the baseband signal.

We denote the ADC power in the absence of in-band jammers by P_{ADC}, at an ENOB of B. In order to accommodate a jammer d_{jam} dB above the signal at the input of the ADC, an increased ADC resolution is needed with ENOB of $B + B^*$ where:

$$B^* = \frac{d_{\text{jam}} - 10\log_{10}(\frac{3}{2})}{20\log_{10}(2)}. \tag{7.1}$$

Assuming ADC power is proportional to the number of quantization levels [44, 88], the cost in ADC power due to the presence of the in-band jammer in the conventional setting (without analog pre-processing) is thus $P^*_{\text{ADC}} = 2^{B^*}P_{\text{ADC}}$, exponential in the additional B^* ENOB and thus exponential in d_{jam}. A suitable MAC capable of suppressing the jammer and restoring the signal at full strength thus substantially reduces the ADC power consumption which amounts to a sizable fraction of the overall power of the CR receiver. The estimated reduction $P_{\text{reduction}}$ in overall power, at a MAC power of P_{MAC}, is:

$$\begin{aligned} P_{\text{reduction}} &= P^*_{\text{ADC}} - (P_{\text{MAC}} + P_{\text{ADC}}) \\ &= (2^{B^*} - 1)P_{\text{ADC}} - P_{\text{MAC}} \\ &\approx 2^{B^*}P_{\text{ADC}} \end{aligned} \tag{7.2}$$

for large jammers, $2^{B^*} \gg 1$. These savings can be significant. For instance, a typical state-of-the-art ADC with a figure-of-merit (FOM) in the lower fJ/step range incurs 46 μW of ADC power per channel at 6.4 Msps and 10.3-bit ENOB [19]. The critical requirement for substantial savings is for the MAC to offer large analog dynamic range d_{jam} in jammer suppression below the signal level, at very low power. At the demonstrated $d_{\text{jam}} = 68.5$ dB of MAC jammer suppression (Section 7.5), the additional 11 bits required according to (7.1) and (7.2) would amount to 92 mW in power savings per channel. In contrast, the measured MAC power is less than 50 μW per channel, insignificant compared to the contributed savings in ADC power. Similar approaches also suggest substantial (greater than 90%) ADC power savings owing to low-power high-dynamic range analog preprocessing ($d_{\text{jam}} = 40$ dB) [85].

7.3 MIMO Baseband Receiver Architecture

7.3.1 HRM and MAC analog signal path

The implemented MIMO baseband receiver architecture is illustrated in Fig. 7.2. A 4-channel capacitive harmonic rejection mixer (HRM) receiver directly up/down-converts a selected 3 MHz band in the RF complex inputs I_{1-4} and Q_{1-4} (48 MHz bandwidth) to baseband complex signals $I_{\text{HRM}\,1-4}$ and $Q_{\text{HRM}\,1-4}$. The HRM receiver produces minimal harmonic folding, such that a harmonic blocker f_{IJ} jamming into baseband f_{J} is maximally suppressed, ≥ 55 dB. Following 4-channel HRM, the MAC implements 4×4 complex spatial filtering for signal separation. The MAC 4×4 complex linear transform is implemented as 8×8 real matrix-vector multiplication in the I and Q components, where redundancy in the real weighting W_{ij} can be harnessed to mitigate analog coefficient mismatch as needed. Relying just on spatial diversity, the MAC is capable of separating signals with completely overlapping spectra. For example, jammers appearing in-band due to the RF front-end's down-conversion of harmonic blockers f_{RFJ} at multiples of $f_{\text{LO\_RF}}$ (*e.g.* $f_{\text{IJ}} + N' f_{\text{LO\_RF}}$ folding onto f_{I1} in-band) can still be separated by the MAC.

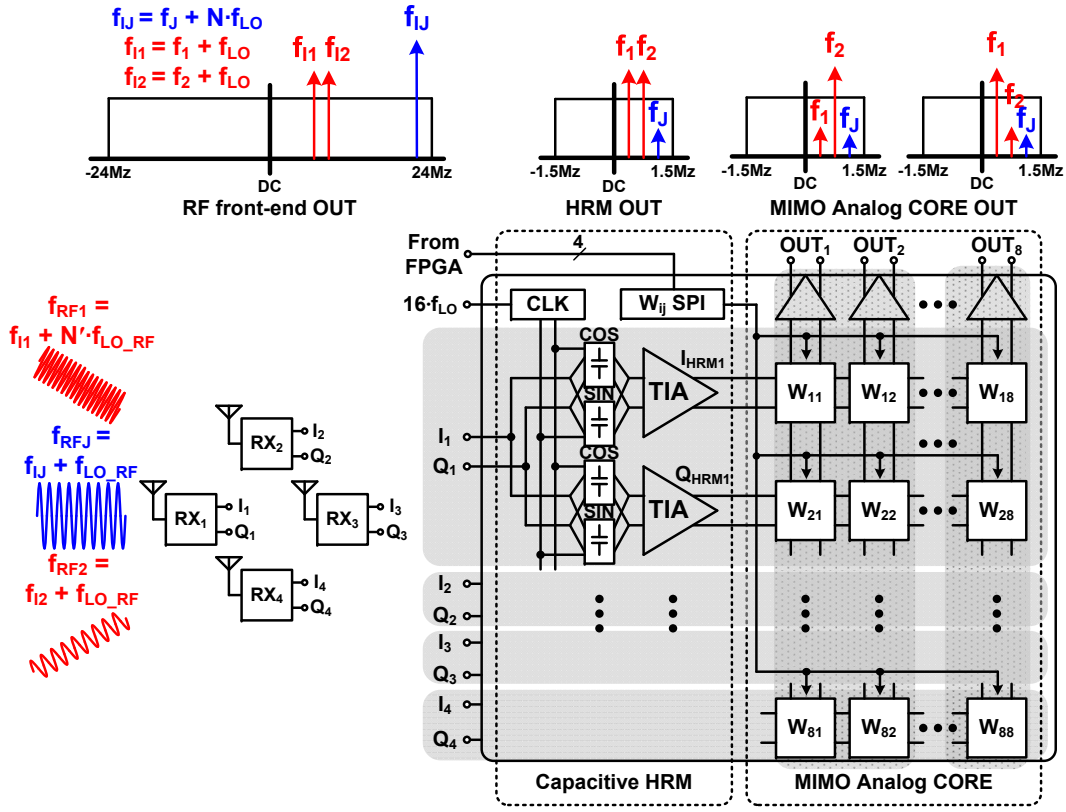


Figure 7.2: Presented 4-channel MIMO baseband receiver with example spectra of input/output signals, illustrating suppression of harmonic blockers through harmonic rejection mixer (HRM) baseband reception and separation of in-band jammers through MIMO analog core (MAC) spatial filtering.

7.3.2 HRM Order

The wide bandwidth of the RF front-end output, up to 16 times larger than the mixer carrier frequency f_{LO}, causes harmonic blockers of high orders, up to 16^{th} order in the case of $f_{\mathrm{LO}} = \pm 1.5$ MHz, to pass the front-end unattenuated. For enhanced resilience to strong harmonic blockers, the HRM needs to provide substantial harmonic rejection, up to 16^{th} harmonic order. This places stringent linearity and matching requirements on the design of the HRM receiver. Furthermore, the HRM layout is subject to severe area constraints to reduce mismatch variations and minimize clock skew across channels, and reduce the cost associated with silicon area.

7.3.3 MAC resolution

In addition to supporting harmonic rejection and broadband operation of the MIMO baseband receiver, highly linear mixing by the HRM is also necessary to support high dynamic range in MAC signal separation. To resolve residual mismatch in the HRM outputs and implement MAC signal separation over a wide range of angles, 14-bit accuracy is needed in the multiplying digital-to-analog converters (MDACs) for the digital weights W_{ij} in the MAC analog signal path.

These requirements must be met under power constraints while providing full programmability of the analog signal path by the DSP, adding further to the design challenge. The use of capacitive charge division to implement harmonic rejection in the HRM, as well as MDAC spatial filtering in the MAC, is crucial to the large reduction in power possible due to this architecture. To allow agile operation in dynamic CR environments, high-bandwidth ($>10^4$ updates/sec) programming of the MIMO receiver parameters (HRM frequency and gain parameters, and DAC digital weights W_{ij}) from external DSP is supported via a serial-peripheral-interface (SPI) bus having only 4 control lines.

7.4 Circuit Design and Implementation

7.4.1 Capacitive thermo-coded 16-phase sinusoidal modulation

High-precision 16-phase sinusoidal weighting is needed for harmonic modulation of the complex signal to accomplish 16^{th}-order harmonic rejection mixing. To this end, we pursue capacitive weighting in HRM in order to mitigate limited precision due to thermal noise and process threshold voltage variations in conventional resistive or transconductive HRM weighting. However, capacitive linear sinusoidal weighting over each of 16 phases over 4 complex channels incurs large area overhead. Each complex phase modulation coefficient carries 4 real (2 sine and 2 cosine) weights, for a total of $16 \times 4 \times 4 = 256$ weighted capacitors, and 512 for fully differential encoding. Precise digital encoding of each of the sinusoidal

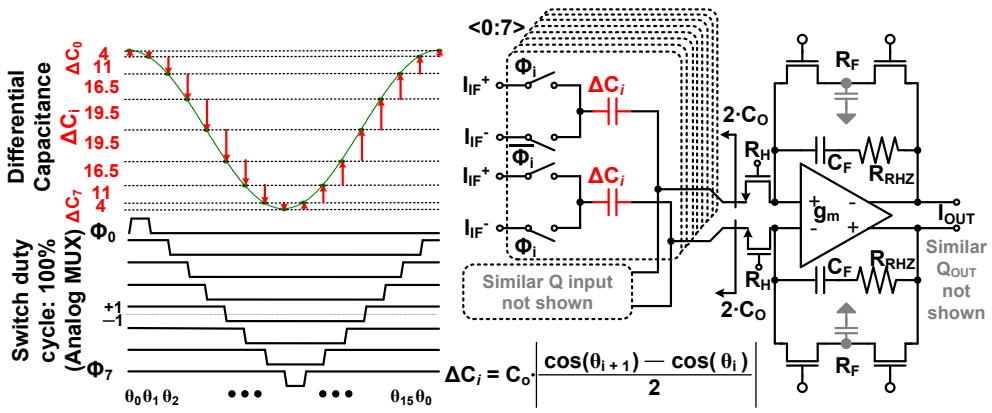


Figure 7.3: Capacitive 16th harmonic rejection mixer (HRM) baseband receiver with differential encoding of 16-phase sinusoidal weighting by thermo-coded clocking of incremental capacitance. The differential encoding reduces capacitance 16-fold for substantial area and power savings.

weights, with low quantization error, requires a large number of unit capacitors, around 100 [38]. Realized using high-linearity interdigitated capacitors with unit size $C_{\text{unit}} \approx 10\,\text{fF}$, this would lead to large nominal capacitance $C_O \approx 1$ pF, for each real weight, and thus a prohibitively large 256 pF total capacitance[1]. Here we propose an alternative sinusoidal weight encoding scheme which allows to reduce overall capacitance 16-fold, leaving only 4 nominal capacitances $4\,C_O$ per complex channel, or one nominal capacitance C_O per real sine/cosine modulation channel [40]. As shown in Fig. 7.3, the reduced capacitance encoding scheme implements the same sinusoidal modulation in incremental steps for each of the 16 phases, controlled by a thermo-coded clock, in which the *difference* in sinusoidal capacitance is added or subtracted between consecutive phases. At same resolution of quantization in the sinusoidal weights (same number of unit capacitors for nominal capacitance C_O), a single array of unit capacitors totaling C_O is partitioned into 8 segments of incremental capacitance, each added in during one of 16 phases and subtracted out during another of the 16 phases according to the sequence of

[1]The magnitude of the sine/cosine wave over all phases varies between 0 and C_O with an average of $0.5\,C_O$, summing to $128\,C_O$ for single-ended realization of the 4 complex channels, or summing to $256\,C_O$ accounting for both complementary branches of the signal path for fully differential realization.

the thermo-coded clock.

To further reduce the total number of unit capacitors two-fold, the sine/cosine wave coefficients are encoded in half fractional rather than integer unit steps, where any additional half unit is implemented as a series connection of two unit capacitors. For a target of -70 dBc harmonic distortion from ideal sinusoidal weights of the capacitor array, 9 phases (0 to π in $\pi/8$ steps) of a half sine/cosine wave were encoded with half-fractional coefficients: {0, 4, 15, 31.5, 51, 70.5, 87, 98, 102} as in [38], leading to the resulting 8 phases of differential capacitance encoded in corresponding half-fractional form: {4, 11, 16.5, 19.5, 19.5, 16.5, 11, 4}. Each coefficient represents the number of unit capacitors being switched in or out, including the series connections of two unit capacitors for the half step residues.

As highlighted in [89], gain and phase errors significantly degrade the harmonic rejection capacity of HRMs. Since this work encompasses a base-band receiver operating at LO frequencies up to ±22.5 MHz, gain errors are dominant due to component mismatch. Monte Carlo analysis over 1,000 runs with ±2.5% component mismatch reveals worst-case harmonic distortion of -58 dB at the second harmonic. The superior matching properties of capacitors instead of MOS transconductors along with careful layout techniques using dummy surround capacitors (Fig. 7.4 (c)) mitigate effects of mismatch in the proposed HRM circuit. Furthermore, the capacitive mixing mitigates thermal noise contributions common to transconductance-based mixing, while the analog multiplexing LO switching network avoids kT/C sampling noise typical of conventional switched-capacitor circuits.

Only the in-phase (I) input component for the I output component is shown in Fig. 7.3 for simplicity; the quadrature (Q) input component is symmetric for cosine rather than sine modulation as described next.

7.4.2 Capacitive Harmonic Rejection Receiver

Fig. 7.4 (a) shows the schematic of the I output component of the HRM receiver, with cosine modulated I input component and sine modulated Q input component. The Q output component of the HRM receiver is identical, with

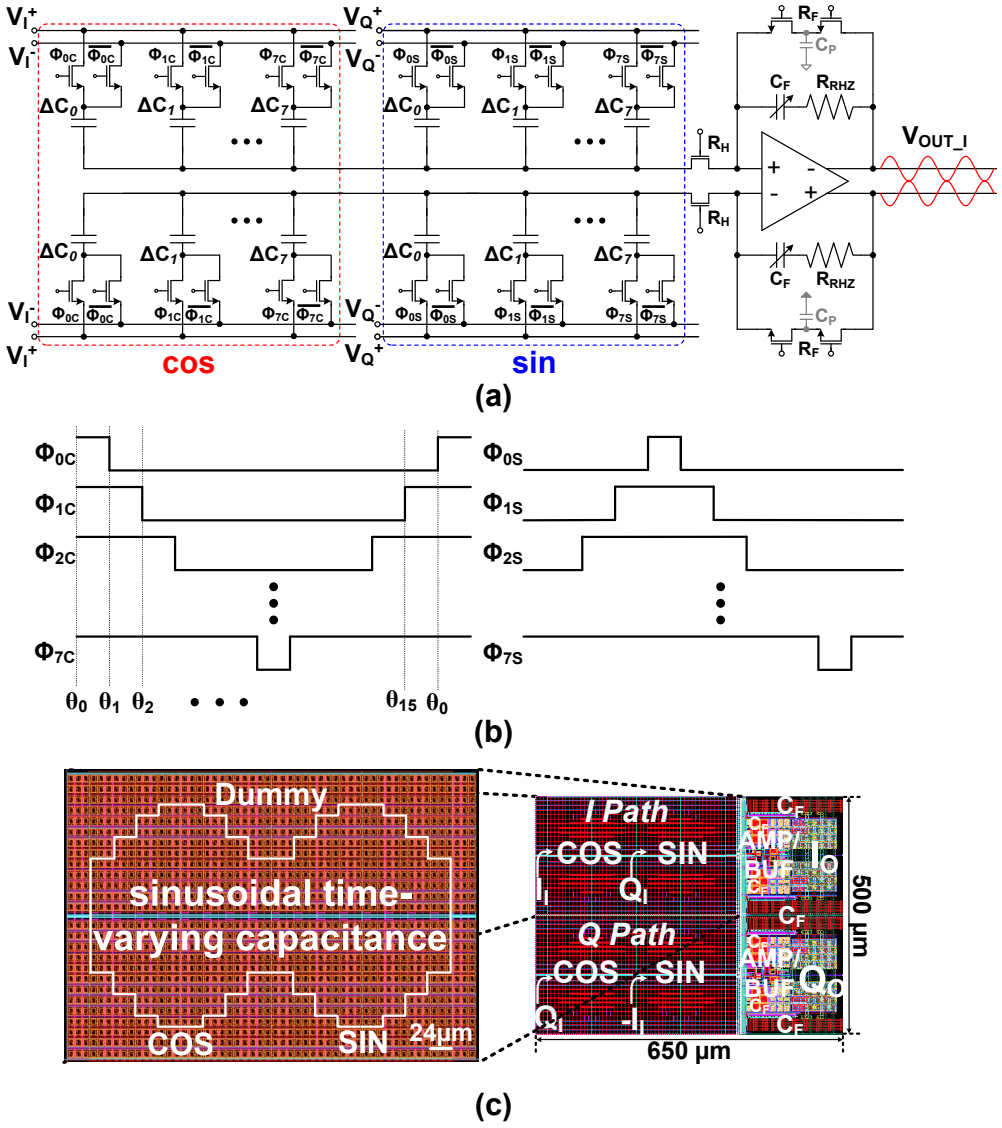


Figure 7.4: Harmonic rejection mixer (HRM) baseband receiver. (a) I/Q complex capacitive HRM implemented with nMOS switches and transimpedance amplifier (TIA) baseband filter. (b) Thermo-coded clock waveforms for generating sine/cosine harmonic weighting. (c) Layout of one complete I/Q complex HRM channel, with inset showing partitioning of the C_O unit array capacitor among 8 sine/cosine phases.

inverted polarity sine modulation of the I input component, and cosine modulation of the Q input component. As such, the HRM performs a frequency shift in the $I + jQ$ complex signal from input to output through complex multiplication with

the phasor $e^{j2\pi f_{LO}t}$, where f_{LO} ranges from -24 MHz to $+24$ MHz.

For each of the I and Q outputs, a trans-impedance amplifier (TIA) structure implemented using a fully-differential operational transconductance amplifier (OTA), integrates the charge injected by the sinusoidal weighted capacitive input contributions of the passive mixer. As the single active element in the HRM receiver, its compact structure and low power consumption lead to highly efficient multi-channel implementation. In addition to the simple structure, we note that passive mixing with capacitive sinusoidal weighting offers superior handling of high-power harmonic blockers. Conventional HRMs implement harmonic weighting in additional stages following an unweighted mixer and gain stage [73]- [86]. Hence, large harmonic blockers may saturate the down-conversion stage where they are amplified along with the signal, despite the harmonic rejection performance of subsequent stages. In contrast, precise linear harmonic weighting prior to amplification allows for the removal of large harmonic blockers up-front [63, 64]. In addition, large non-harmonic blockers can be accommodated with sufficient linearity through the gain control functionality of the HRM and the subsequent spatial filtering.

The digitally synthesized thermo-coded clock generator is composed of 16 registers generating 16-phase sine and cosine waveforms shown in Fig. 7.4 (b). For up-conversion rather than down-conversion (i.e., for inversion of the polarity of f_{LO}), the clock sequence is simply reverted in time, where a sign bit selects down- or up-conversion. In addition to reducing silicon area, the thermo-coded capacitor array also lowers power consumption due to parallel switching. Switches at each capacitor in Fig. 7.4 (a) are in parallel reducing the size of the switch such that the driving power consumption can be minimized. As a result, small switches (600 nm/60 nm) are employed for a 400 MHz maximum clock speed at 1.2 V supply.

With the simple structure, the HRM receiver for a I/Q complex channel occupies 650 μm × 500 μm in Fig. 7.4 (c). The sinusoidal time-varying capacitor is implemented by interdigitated metal-finger capacitors in higher metal layers (metal 4 and 5) for high linearity and immunity from substrate noise. The same layout is used for both sine and cosine weighting by modifying only the input connections

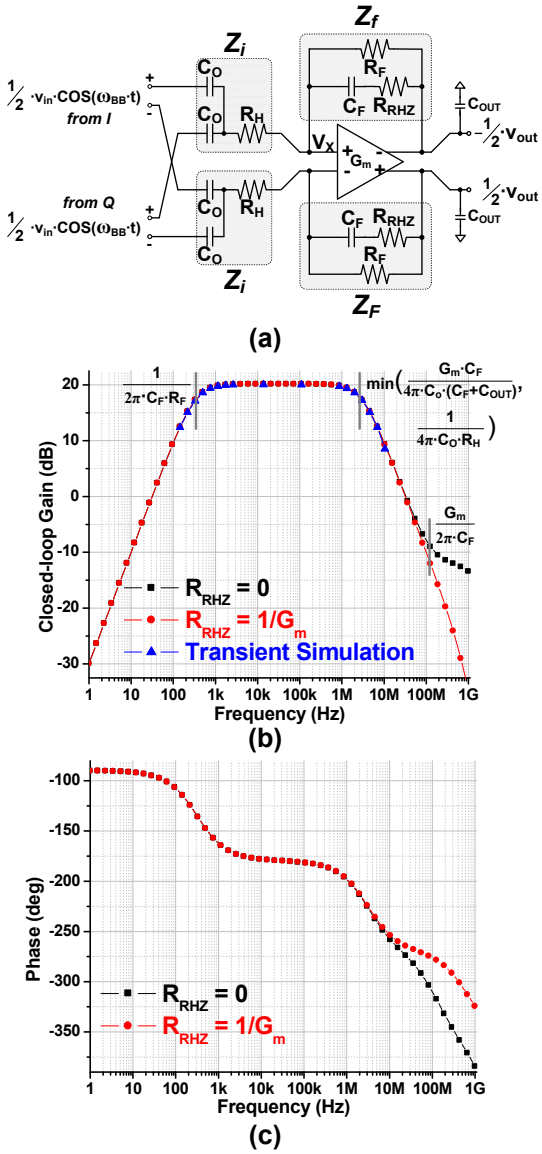


Figure 7.5: HRM baseband frequency response for: $C_F = 10$ fF, $C_O = 1.01$ pF, $G_m = 80\mu$S, $R_F = 5$ GΩ, $R_H = 10$ kΩ, $R_{\text{RHZ}} = 12.5$ kΩ, $C_{\text{OUT}} = 40$ fF, and OTA output impedance $R_{\text{out}} = 50$ MΩ. (a) AC small-signal model equivalent circuit for closed-loop gain and phase of the TIA baseband filter following passive HRM. (b) AC simulated closed-loop gain showing the effect of R_{RHZ}. Transient simulation results from the full HRM receiver circuit at select frequencies are superimposed for comparison. (c) AC simulated closed-loop phase corresponding to (b).

and clock sequence, greatly improving I and Q matching.

The AC small-signal closed-loop gain $A_{\mathrm{CL}}(j\omega) = v_{\mathrm{out}}(j\omega)/v_{\mathrm{in}}(j\omega)$ of the TIA baseband frequency response, following down-conversion by the passive mixer, is modeled using the linear equivalent circuit illustrated in Fig. 7.5 (a). The TIA input v_{in} represents the passive mixer down-/up-converted output, modeled as harmonically modulated I/Q input signals from the RF front-end. C_{OUT} at the v_{out} output node includes about 40 fF in parasitic capacitances, in addition to 100 fF to 200 fF in programmable capacitance. The resulting closed-loop gain and phase of the HRM baseband response are plotted in Fig. 7.5 (b) and (c). To validate linearity and stability, transient simulations with the full HRM receiver circuits were performed for closed-loop gain at select frequencies, the results of which were overlayed on the AC small-signal response. The closed-loop gain of the TIA is given by

$$A_{\mathrm{CL}}(j\omega) = -\frac{A_{\mathrm{OP}}(j\omega)\ (1 - F(j\omega))}{1 + A_{\mathrm{OP}}(j\omega)\, F(j\omega)} \approx -\frac{1 - F(j\omega)}{F(j\omega)} = -\frac{Z_f(j\omega)}{Z_i(j\omega)} \tag{7.3}$$

where $A_{\mathrm{OP}}(j\omega)$ is the TIA open-loop gain, and $F(j\omega)$ is the loop feedback factor [82]. The limiting approximation in (7.3) holds for very large loop-gain, $A_{\mathrm{OP}}\, F \gg 1$. The mid-band gain in the high loop-gain limit is thus set by C_i/C_f and the bandpass corners set by Z_f and Z_i: high-pass cut-off $1/(2\pi C_F R_F)$, and low-pass cut-off $1/(4\pi C_O R_H)$. However, in order to save power, the OTA transconductance G_m is set for a loop-gain unity-gain-bandwidth $G_m C_F/(4\pi C_O(C_F + C_{\mathrm{OUT}}))$ close to $1/(4\pi C_O R_H)$, and as a result, the low-pass cut-off also depends on the loop-gain unity-gain-bandwidth. To first order, the low-pass cut-off is the minimum of $G_m C_F/(4\pi C_O(C_F + C_{\mathrm{OUT}}))$ and $1/(4\pi C_O R_H)$. The resistor R_{RHZ} is inserted to remove a right-half plane (RHP) zero positioned to the $G_m/(2\pi C_F)$. The effect is clarified by verifying the frequency response for the setting $R_{\mathrm{RHZ}} = 0$, for which the RHP zero is clearly shown in the gain and phase plot in Fig. 7.5 (b) and (c). At very high frequencies (above 100MHz), the effect of an additional pole related to the transconductance of OTA, G_m, and C_{OUT} becomes visible.

The OTA in the HRM receiver is a three-stacked folded-cascode amplifier as shown in Fig. 7.6. With all MOS transistors operating in sub-threshold, the OTA transconductance is linear in bias current I_B. Furthermore, with a $V_{ds\ sat}$ of only

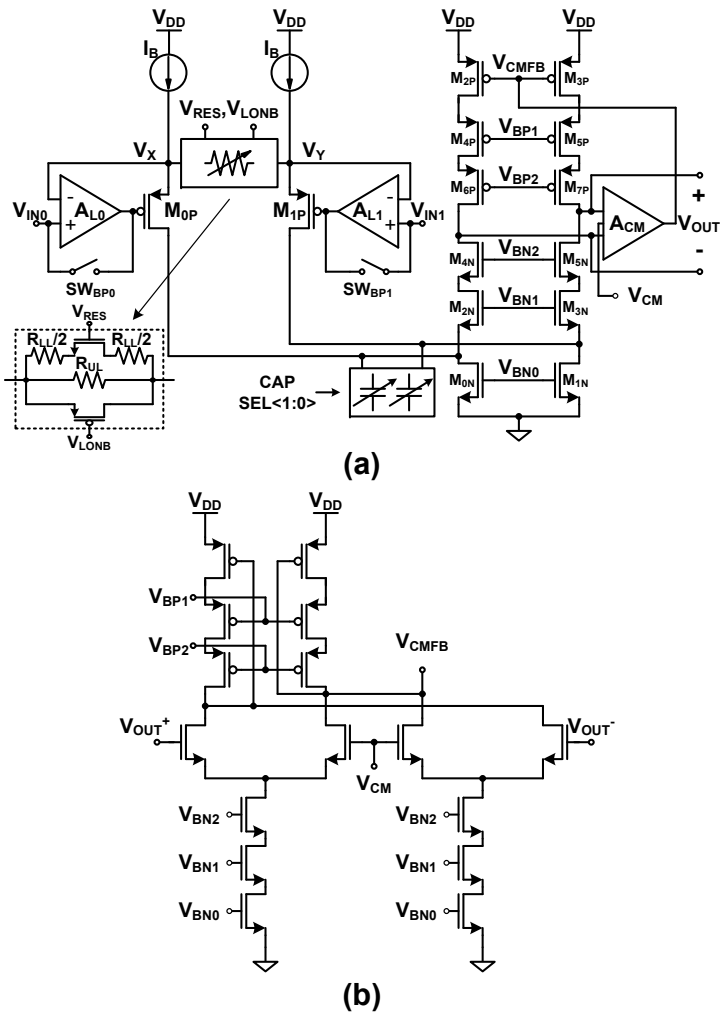


Figure 7.6: (a) Folded-cascode operational transconductance amplifier (OTA) in the TIA. All MOS transistors operate in sub-threshold for high-efficiency in g_m/I and large output swing range. For improved amplifier linearity, local feedback is applied to input pairs M_{0P} and M_{1P} using two conventional 5-transistor OTAs A_{L0} and A_{L1}. (b) Common-mode feedback (CMFB) circuit.

100 mV in sub-threshold, a 1.2 $V_{\rm pp}$ maximum differential output-swing range (600 m$V_{\rm pp}$ swing for each polarity) can be guaranteed without compromising linearity. Higher gain can be obtained in the deep sub-micron process through additional gain boosting as employed in [43]. Further improvement in linearity results from local feedback near input pairs, M_{0P} and M_{1P}, with two conventional 5-transistor amplifiers, $A_{\rm LO}$ and A_{L1}, consuming around 50 nA per local feedback amplifier. For

improved high-frequency cut-off, the second pole of the OTA can be adjusted by 2-b digital signals, CAPSEL<1:0>. The OTA is the only static power consuming circuit in the HRM receiver and its measured current draw from a 1.2 V supply is 8.84 μA.

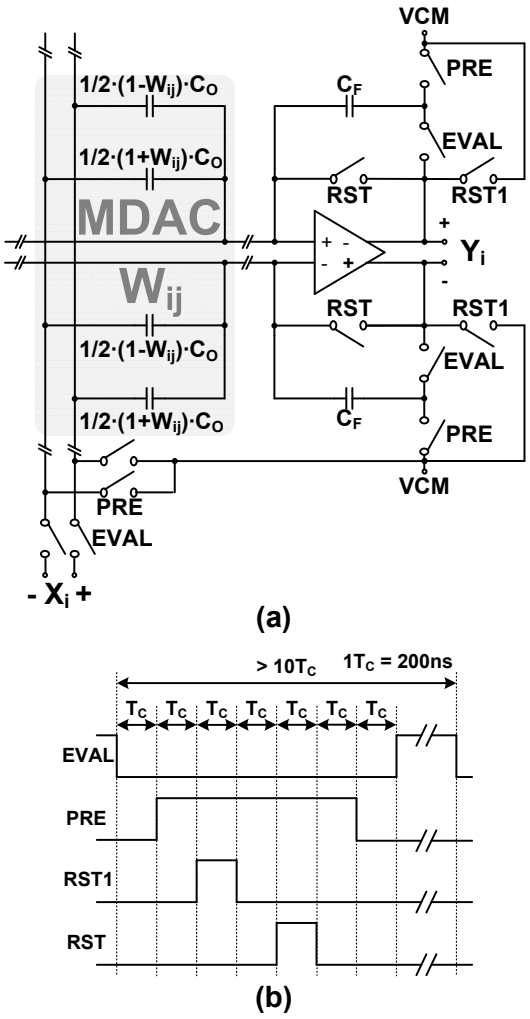


Figure 7.7: MIMO analog core (MAC) for signal separation by spatial filtering. (a) MAC circuit with 14-bit multiplying digital-to-analog converter (MDAC) implementing digitally programmable analog linear weighting in the MAC signal path. To reduce the effect of offsets in the MDAC and the OTA, a correlated double sampling (CDS) scheme is employed. (b) Timing diagram for CDS.

7.4.3 MIMO Analog Core

The MAC implements analog preprocessing on the outputs of the HRM receiver for further preprocessing, prior to digitization. The 8×8 matrix composing MAC consists of complementary 14-bit split capacitor multiplying digital-analog converters (MDAC) shown in Fig. 7.7 (a). In all experiments reported here, unless mentioned otherwise, the matrix coefficients are calculated from the angle of incidence of the RF signal and used to beamform the undesired incident signal at baseband before digitization. Compared to the conventional approaches that rely on LO-phase shifting [22] with N-path filtering techniques, we generate phase shifts by implementing a rotation matrix using complex matrix-vector multiplication with the 8×8 weight matrix. The minimum resolvable angle and the dynamic range in the resolution are, thus, determined by the accuracy of the MDAC. In order to ensure sufficient MDAC precision, offset cancellation at the MDAC and the OTA is implemented using Correlated Double Sampling (CDS) with the clock waveform in Fig. 7.7 (b), setting the input DC bias point of the capacitively coupled differential amplifier. The CDS frequency can be set to 500 Hz that is low enough to not disturb measurements. We create a custom shielded capacitive array structure for both the MDAC and the C_F in the OTA, resulting in a programmable gain range of -12 dB to 24 dB in steps of 6 dB at the output in addition to 14-b weighting of individual W_{ij} coefficients. The programmable gain is realized by digitally selecting different numbers of unit capacitors to constitute C_F in the feedback loop. A standard fully-differential folded-cascode OTA with the same common-mode feedback as in Fig. 7.6 is employed for the MAC.

7.5 Experimental Validation

The fully integrated MIMO baseband receiver with the 4-channel HRM receiver and the MAC was fabricated in 65 nm bulk CMOS with active area of 3.27 mm^2 in Fig. 7.8.

The HRM and MAC functional blocks are tested independently, and in their intended cascaded succession. For separate tests of the individual HRM and

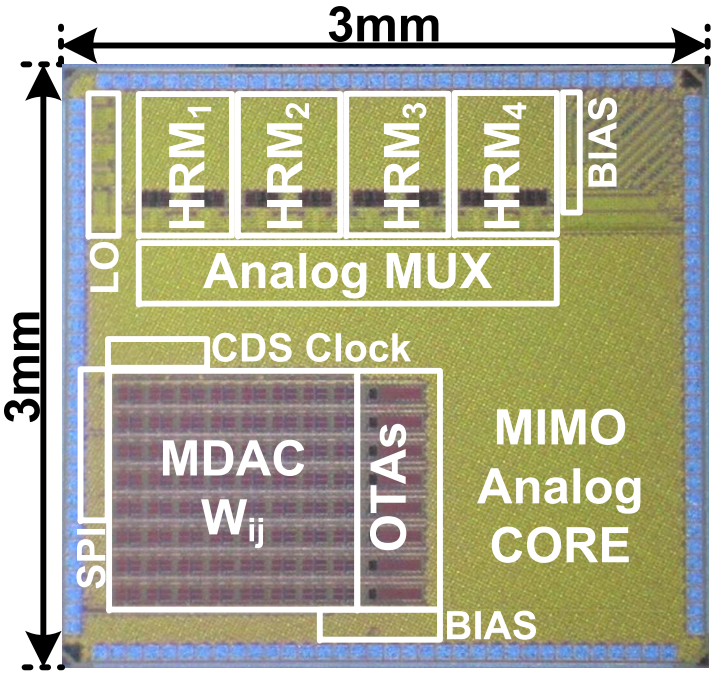


Figure 7.8: Micrograph of the MIMO baseband receiver with HRM and MAC modules indicated.

MAC blocks, an analog MUX stage implemented with CMOS switches was inserted between HRM and MAC stages on the integrated circuit, with separate external I/O connections. Finally, the complete system was validated for separation of RF sources with an antenna array and external front-end.

7.5.1 HRM receiver characterization

Two-tone linearity tests in Fig. 7.9 (a) show the measured in-band input and output intercept points (IIP3 and OIP3) for the isolated HRM receiver. DC biasing of the HRM inputs was set to 0 V, independent of that of the HRM outputs set to the supply midrange (0.6 V). Measured -3.8 dBm in-band 1 dB compression point is further revealed in the gain curve in Fig. 7.9 (b). In Fig. 7.10, the power at 0.2 MHz is measured with a fixed f_{LO} at 16.5 MHz for input frequency ranging from the fundamental at 16.7 MHz to the 16^{th} harmonic at 264.2 MHz. Worst-case harmonic suppression is -66.16 dB observed at the 16^{th} harmonic folding,

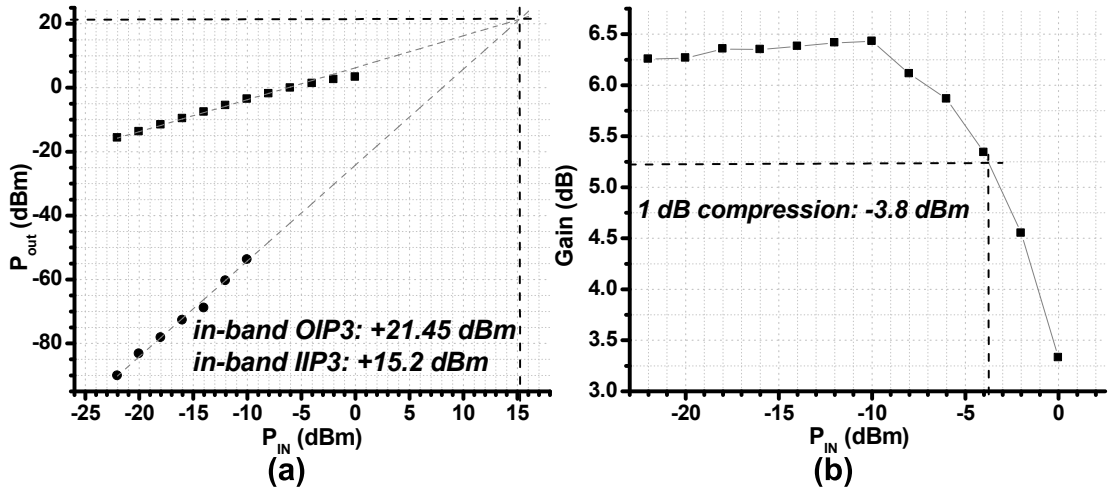


Figure 7.9: Two-tone linearity measurement for the HRM. (a) Measured in-band third-order input and output intercept points are IIP3= +15.2 dBm and OIP3= +21.45 dBm, respectively. (b) Gain versus input power shows 1 dB compression (P1dB) at -3.8 dBm.

limited by mismatch and to a lesser extent feedthrough of the external clock at $16\times f_{\mathrm{LO}}$. As expected, the 15^{th} harmonic folding is not harmonically rejected, but still attenuated by the sinc spectral profile resulting from the sampling by the LO switch network. Measurements shown in Fig. 7.11 demonstrate the HRM performance in the presence of large harmonic blockers under the condition that the power of the desired input signal is kept constant at -30 dBm (0.35 MHz $+f_{\mathrm{LO}}$) while the power of the 3$^{\mathrm{rd}}$ order harmonic blocker (0.38 MHz $+3\,f_{\mathrm{LO}}$) is increased. The measured power at 0.35 MHz frequency shows 1 dB compression points by the 3$^{\mathrm{rd}}$ harmonic blocker consistently greater than 0 dBm over various gain settings, demonstrating high resilience to blockers. At 6 dB gain setting, the 1 dB compression point could not be measured beyond +2 dBm since stronger harmonic blocker signals may damage switches in the HRM receiver.

7.5.2 MAC characterization

The measured two-tone separation capability of the MAC in isolation, shown in Fig. 7.12, demonstrates suppression of an in-band jammer signal $S2$

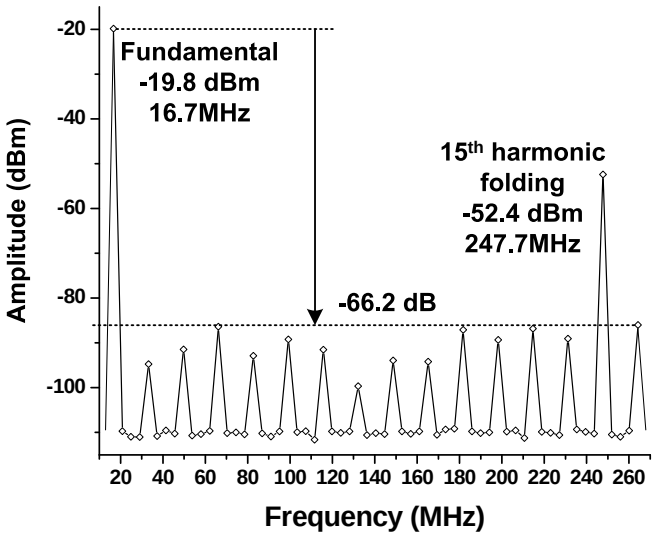


Figure 7.10: Measured harmonic folding up to the 16^{th} harmonic of the LO. The f_{LO} is set to 16.5 MHz, with input frequency from 16.7 MHz to 264.2 MHz.

20 dB above the signal tone $S1$ at the input, to 48.5 dB below the signal tone at the output, for a total of 68.5 dB jammer suppression. Synthetic mixtures with the algebraic sum and difference of the jammer $S2$ and 20 db attenuated signal $S1$ were presented through multichannel arbitrary waveform generators to two of the MAC inputs, with the other inputs grounded. The DAC digital weights W_{ij} were set to invert the synthesized linear mixing of the signals at the input, with fine adjustments for maximum nulling of the jammer.

7.5.3 Combined MIMO baseband receiver characterization

As a proof-of-concept of combined spectral and spatial jammer suppression in the setting illustrated in Fig. 7.2, a three-tone test with harmonic blocker and two closely spaced in-band signals, one signal of interest and one jammer, was performed on the combined MIMO baseband receiver (HRM + MAC). As shown in Fig. 7.13, the HRM down-converts f_{I1} and f_{I2} in-band while rejecting 3^{rd} harmonic blocker f_{IJ}. The down-converted signals from the HRM are further spatially filtered by the MAC to amplify the desired signal f_2 while rejecting in-band jammer f_1.

Fig. 7.14 shows better than 65 dB down-converting rejection of 2^{nd} through

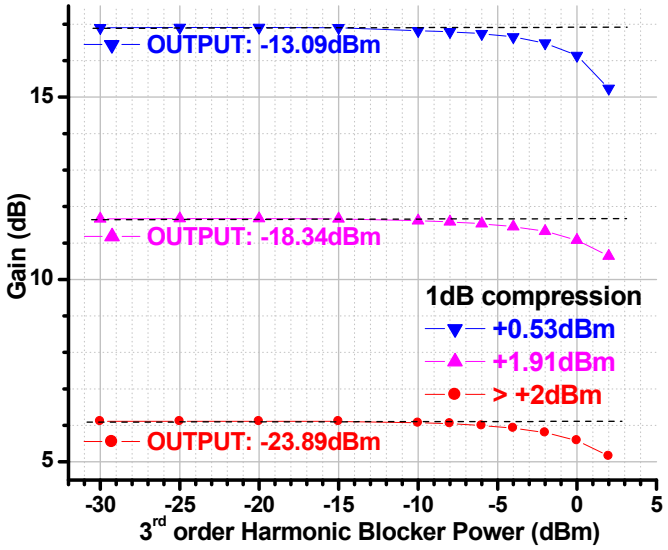


Figure 7.11: Measured output power of the HRM at various gain settings while providing a constant -30 dBm of input at 4.85 MHz and varying the power of blocker at the 3rd order harmonic at 13.95 MHz. f_{LO} is 4.5 MHz.

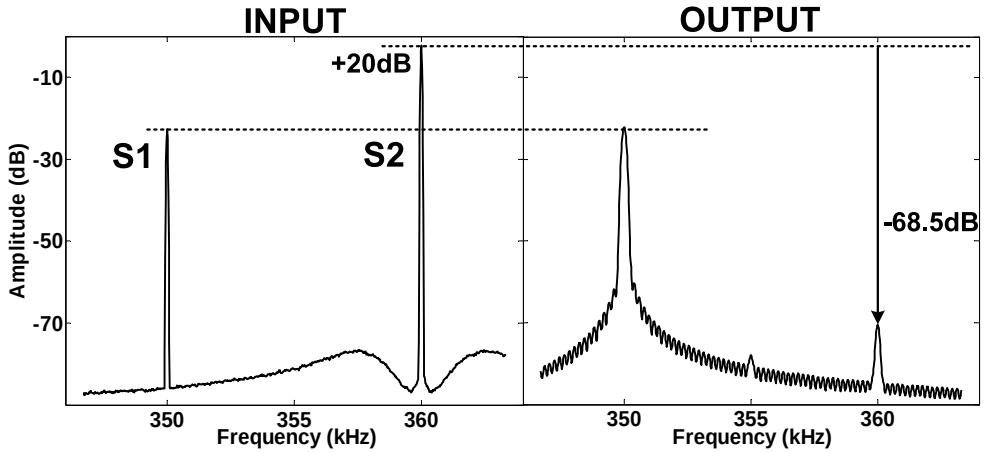


Figure 7.12: Measured in-band jammer rejection by the MAC for two synthesized inputs with linear mixtures of a signal $S1$ and an in-band jammer $S2$ +20 dB above $S1$, showing 68.5 dB jammer suppression at the MAC output.

5th harmonic blockers while resolving the signals spatially with greater than 48.5 dB separation, for LO frequencies spanning the -24 MHz to +24 MHz band.

For demonstrating both spectral and spatial filtering capabilities, synthe-

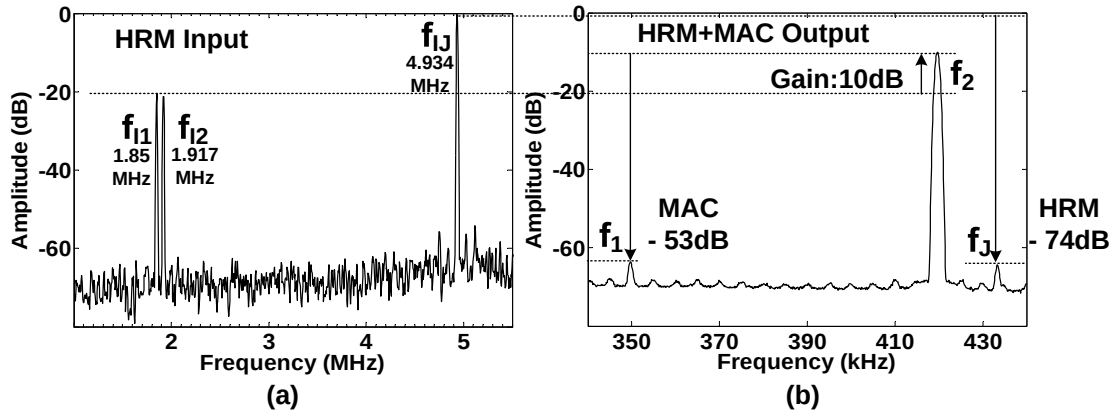


Figure 7.13: Three-tone test to quantify harmonic rejection ratio and in-band jammer rejection with f_{LO} of 1.5 MHz. Input signals feed directly into the HRM, and observed through the MAC, measured at its outputs. (a) Measured input signals, with in-band jammer f_{I1}, in-band desired signal f_{I2}, and 3$^{\text{rd}}$ order harmonic blocker f_{IJ} +20 dB above the f_{I1} and f_{I2} signals. (b) Measured rejected and amplified signals at the MAC output, showing HRM rejection of the harmonic blocker f_{IJ} and MAC suppression of in-band jammer f_{I1} to retain the desired signal f_{I2}.

sized waveforms composed of spectrally fully overlapping mixtures of QAM and QPSK along with a 3$^{\text{rd}}$ harmonic blocker 24 dB above the signals are presented to the MIMO baseband receiver. Four single-to-differential amplifiers each with 6 dB gain are employed as shown Fig. 7.15 (a). Fig. 7.15 (b) and (c) show spectra and time domain waveforms at each stage of the signal chain, through the HRM and the MAC. The +24 dB harmonic blocker clearly shown at the input is shown rejected by HRM, and the remaining mixture of QAM-QPSK is shown separated by the MAC in two complex channels. Eye diagrams and I/Q constellations for the recovered 16-QAM and QPSK signals were acquired by synchronizing the oscilloscope readout of the MAC outputs with the generation of the HRM inputs and LO. The EVMs of the recovered signals, 2.69% for QPSK and 3.64% for 16-QAM, are obtained from the constellations shown in Fig. 7.16. The capability of the MAC to separate signals with completely overlapping spectra owes to its reliance on spatial rather than spectral diversity. Indeed, techniques of independent component analysis for blind source separation (e.g., [8]) distinguish signals purely by

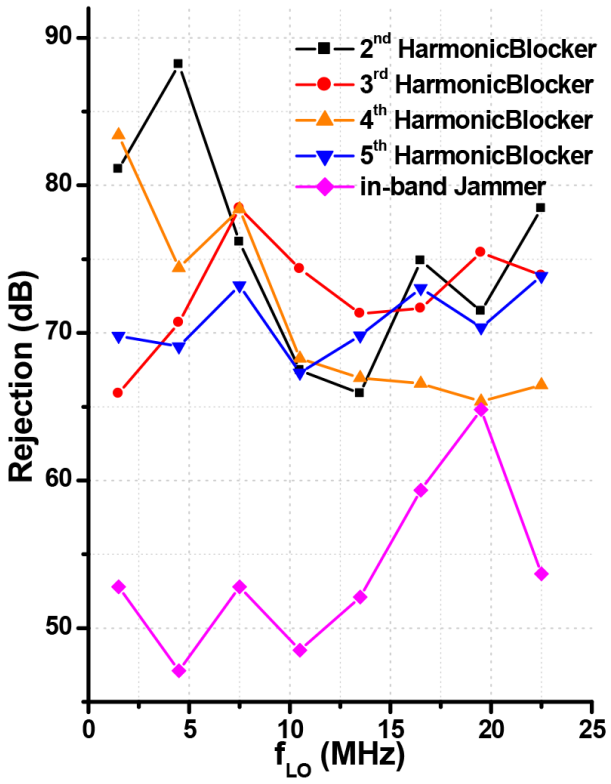


Figure 7.14: Higher-order harmonic rejection characteristics, obtained by sweeping f_{LO} across all 16 bands of the MIMO baseband receiver. All 2^{nd} to 5^{th} order harmonic rejections and in-band jammer rejections are measured using the same setup of Fig. 7.13.

statistical criteria and ignore their temporal spectral content.

Power measurements in Fig. 7.17 show approximately linear scaling of power consumption with bandwidth, indicating 13μW/MHz scaling of net LO and digital power with total IF input bandwidth (a), and 360μW/MHz scaling of net analog power with base bandwidth (b). More than 50% analog power is consumed by buffers between the HRM receiver and the MAC.

A summary of the combined HRM-MAC measured characteristics, and a comparison with the state of the art in HRM and spectral spatial filtering, are summarized in Table 7.1. A key advantage of the system is its low power consumption, which can be leveraged with relatively constant high energy-efficiency in different bandwidth settings for cognitive radio sensing.

Table 7.1: Performance Comparison of Harmonic Rejection and MIMO Receivers

		Yuan VLSI14	Kim ESSCIRC14	Rafi JSSC13	Murphy JSSC15	Ghaffari ISSCC13	Kim JSSC16
CMOS Technology		40nm	65nm	110nm	28nm	65nm	65nm
Topology Description		Blind Classifier	HRM Receiver	HRM Receiver	HRM Receiver	Passive Spatial & Spectral Filter	HRM & Spatial & Spectral Filter Receiver
Approach		Digital Processor	RF Analog	RF Analog	RF Analog	RF Analog	Baseband Analog
2,3,4,5 HRR (dBc)		-	- , > 40, - , -	- , > 52, - , >54	60, 52, 60, 54	-	> 66, > 66, > 65, > 69
Spatial Attn. (dB)		-	-	-	-	< 38	48.5 – 65
P_{1dB} (dBm)		-	-5.5 (In-Band)	-	-6 (Out-of-Band)	-5.5 (In-Band)	-3.8[a] (In-Band)
IIP3 (dBm)		-	+12.5 (In-Band)	+12[b] (-)	+10 (Out-of-Band)	+2 – +9 (In-Band)	+15.2[c] (In-Band)
3rd Harmonic Blocker P1dB (dBm)		-	-	-	-8[d]	-	> +0.53[a,e]
Power (mW)	RF+LO / RF Freq.	0.039/Ms	0.024/MHz	0.374/MHz[f]	0.015/MHz[g]	0.044/MHz[h]	0.011/MHz
	BB (BW)	-	0.04 (3 MHz)	64.8 (-)	12 – 24 (0.2 – 3 MHz)	36[i] (40 MHz)	0.21/Channel (3 MHz)
	Total		7.86	102[f]	36.8 – 62.4	68 – 195	1 – 1.3
Active Area (mm^2)		1.58	1.62	-	5	0.97	3.27

[a]HRM receiver part only for comparison to other HRM receivers
[b]IIP3 of mixer part only, extrapolated from receiver measurement
[c]HRM receiver part only at gain of +6dB for comparison to other HRM receivers. HRM+MAC has +14dBm of in-band IIP3 at 0dB gain and +6dBm of in-band IIP3 at +12dB gain
[d]at normilized gain
[e]at +17 dB gain
[f]16 phase case, LO=100MHz
[g]RF power = 22 mW, LO power = 24 mW at 3 GHz RF frequency
[h]LO power = 159 mW at 3.6 GHz RF frequency
[i]analog G_m blocks only

7.5.4 System validation with antenna array and RF front-end

To evaluate spectral and spatial separation performance in realistic RF conditions, measurements were conducted using an RF front-end with four antennas receiving spectrally overlapping and modulated 2.4 GHz signals from two transmitters in an un-controlled, non-line-of-sight, multi-path environment with the setup shown in Fig. 7.18 (a) and (b). The two TX antennas were positioned more than 1 m away from the four RX antennas, with a metallic plate inserted in between to obstruct the line-of-sight path. Hence all received contributions are multi-path to emulate challenging real-world use cases. The MIMO baseband receiver (DUT) can be seen along with the RX antennas. An ASK signal at 2.417 GHz and a

FM signal at 2.41715 GHz were chosen for the two RF sources, each with modulation depth of 25%. To quantify separation capability, first the down-converted signal was measured with the MAC weights set for no separation (identity weights, Fig. 7.18 (c)) and then the same test was repeated with MAC weights updated in a closed-loop fashion to separate out either of the two signals (Fig. 7.18 (d) for the ASK signal, Fig. 7.18 (e) for the FM signal). The digital weights were derived with an online greedy algorithm that maximizes the ratio of the peak power in the spectra of the down-converted, modulated signals. A net 38 dB of separation between the two signals was observed at the MAC outputs.

7.6 Conclusion

We proposed and demonstrated a 4 $\times$ 4 MIMO baseband receiver as an enabling technology for spectrally *and* spatially aware cognitive radio in next generation power constrained applications. This analog-assisted digital approach can tolerate large jammers at the front end and enable signal separation and amplification to significantly compress dynamic range before digitization. The proposed capacitive HRM shows $\geq$ 65 dB harmonic folding rejection and $\geq$ +0.53 dBm 1 dB compression to 3$^{\text{rd}}$ order harmonic blockers owing to capacitively weighted mixing followed by TIA filtering. The MAC offers programmable spatial filtering with $\geq$68 dB standalone ($\geq$ 48.5 dB combined HRM-MAC) jammer suppression, owing to high linearity in programmable digital weighting using 14-b MDACs. The IC implemented in 65 nm bulk CMOS occupies 3.27 mm^2 active area and consumes 0.67 mW to 1.28 mW at 1.2 V supply inclusive of inter-stage buffers. At an average energy consumption below 1 pJ per multiply accumulate and greater than 48 dB suppression in the analog signal path, this represents significant power savings compared to more conventional implementation directly digitizing the input where the up-front ADC would require an additional 8-bit of resolution to achieve the same dynamic range in harmonic rejection, jammer suppression, and signal separation.

Acknowledgments

Chapter Seven is largely a selection of material in the following two venues: C. Kim, S. Joshi, C. M. Thomas, S. Ha, L. E. Larson and G. Cauwenberghs, "A 1.3 mW 48 MHz 4 Channel MIMO Baseband Receiver With 65 dB Harmonic Rejection and 48.5 dB Spatial Signal Separation," in IEEE Journal of Solid-State Circuits (JSSC), vol. 51, no. 4, pp. 832-844, April 2016 (VLSI Circuits 2015 Special Issue). C. Kim, S. Joshi, C. M. Thomas, S. Ha, A. Akinin, L. E. Larson, and G. Cauwenberghs, "A CMOS 4-channel MIMO baseband receiver with 65dB harmonic rejection over 48MHz and 50dB spatial signal separation over 3MHz at 1.3mW," 2015 Symposium on VLSI Circuits, Kyoto, pp. C304-C305, Jun. 2015. C. Kim is the primary author and investigator of this work.

C. Kim, L. E. Larson and G. Cauwenberghs organized the work. C. Kim wrote the first draft of the paper, with S. Joshi, C. M. Thomas, S. Ha contributing several sections. C. Kim, L. E. Larson and G. Cauwenberghs contributed to edit the paper.

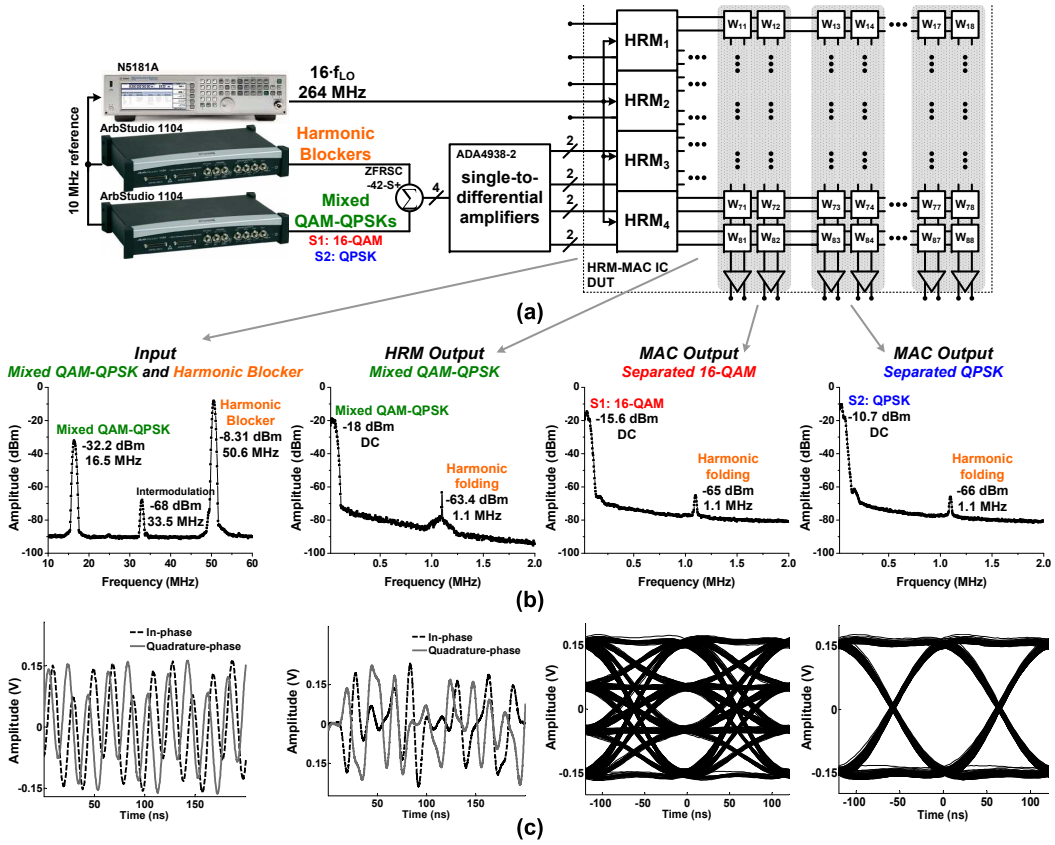


Figure 7.15: MIMO baseband receiver measurements demonstrating separation of signals with completely overlapping spectra in the presence of a strong harmonic blocker. (a) The measurement setup (b) Spectra obtained at each stage of the signal chain. The HRM output (the MAC input) contains the downconverted mixture while suppressing the blocker by 69 dB. The MAC simultaneously separates the 16-QAM and QPSK mixtures in two complex channels. (c) Time domain waveforms at each node. Eye diagrams are obtained by synchronization of oscilloscope readout with the signal inputs.

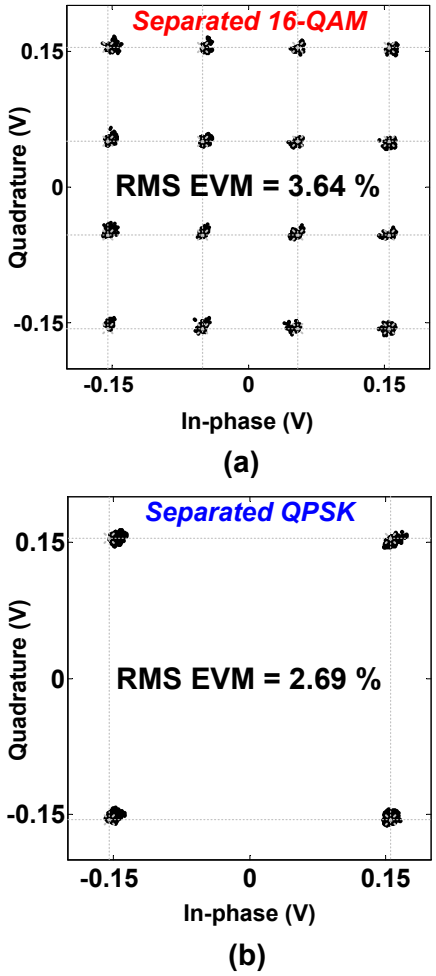


Figure 7.16: (a) Recovered 16-QAM with EVM of 3.64%. (b) Recovered QPSK with EVM of 2.69%. The constellation recovered after downconversion and signal separation by the baseband receiver clearly shows the capability of resolving complex modulated signals.

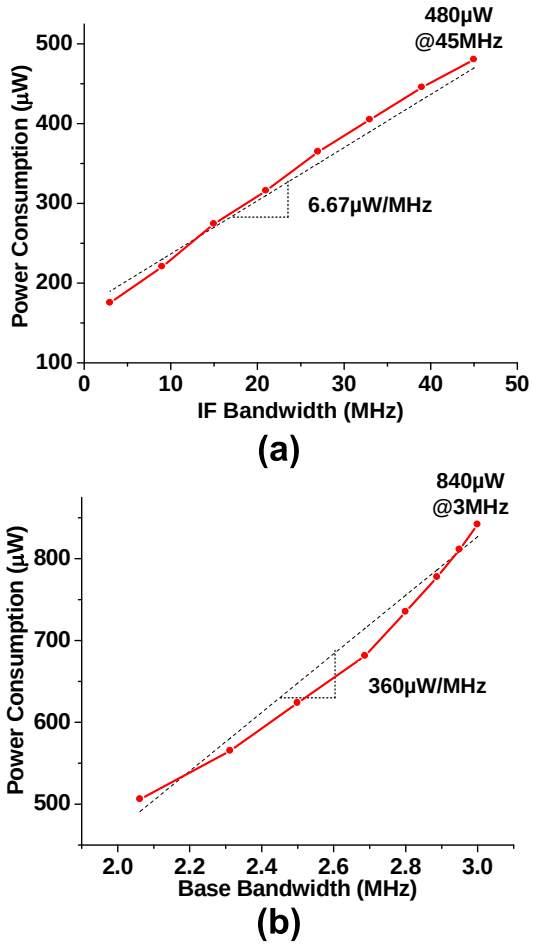


Figure 7.17: Measured power consumption of the 4×4 complex MIMO baseband receiver. (a) Digital power consumption for the HRM clock generator as a function of IF bandwidth (f_{LO}). (b) Analog power consumption of HRM TIA and MAC as a function of base bandwidth. Over 50% of the analog power is consumed by buffers between HRM and MAC.

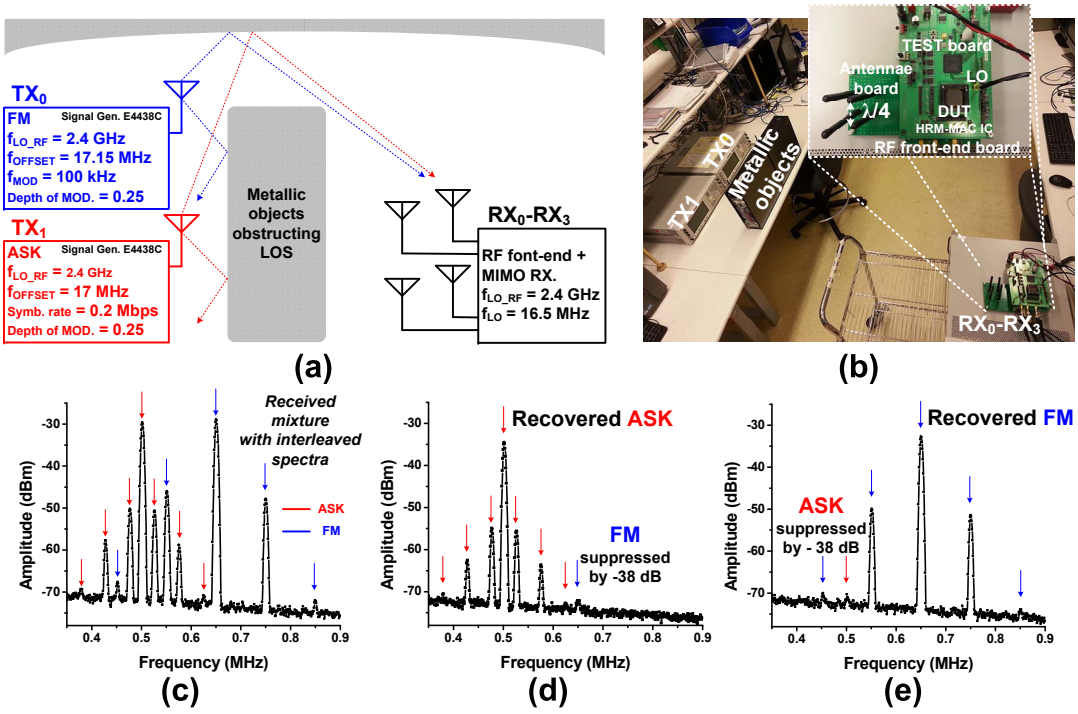


Figure 7.18: Proof-of-concept RF source separation in an uncontrolled open environment. The HRM-MAC IC outputs show recovery of non-line-of-sight RF sources with overlapping ASK and FM modulation spectra, with suppression of residual spectral components -38 dB below the signal of interest.

Chapter 8

Conclusion and Future Work

8.1 Miniaturized electrocortical neural recording/stimulation implants

8.1.1 Contributions and Impact

Brain monitoring, diagnostic, therapeutic, and prosthetic applications, such as deep-brain stimulation, epileptic seizure detection and intervention are enabled by significant advances in neural-interfacing microsystems. However, even state-of-the-art implantable neural interfacing devices still rely on bulky external components such as electrodes, antennae, and capacitors for system functionalities and/or efficiency improvements, limiting their utility when ultra-miniaturized integration is required. I took this challenge and led a team of graduate researchers to develop a prototype wireless neural-interface-on-chip that incorporates all functionality on a single chip: antenna, electrodes, stimulator, analog front-end, analog-to-digital converter (ADC), and wireless power receiver and data telemetry, requiring no external wires, substrates, batteries, or any other external components (Chapters 3 & 4). This miniaturized neural-interfacing microsystems is contained within a volume of $3\times3\times0.25$ mm^3, small enough to be placed amongst the folds and curves of the cortical surface, and to be implanted through minimally invasive surgical procedures inserted through small skull fissures [37, 42].

Other similar integrated circuit neurotechnology I have developed [39] (Chapter 5) has been applied *in vivo* to record local-field potentials (LFPs) connecting to a NeuraLynx microwire electrode array inserted into the frontal cortex of a common marmoset primate (*Callithrix jacchus*). The ADC array allowed for the accurate capturing of infra-slow LFP frequency (< 0.5 Hz) changes as the marmoset transitioned from sensory deprivation at rest to a state of heightened arousal induced by a barrage of sensory stimuli. The infra-slow LFP is an electrophysiological characteristic that is often uncaptured by AC-coupled commercial amplifiers, and the ability of the ADC to properly detect infra-slow LFPs is a testament to the neuroscientific and clinical applicability of this technology. Recent findings suggest that infra-slow LFP is correlated with resting state hemodynamics in the cerebral cortex [26], allowing for further scientific investigation of the relationship between BOLD fMRI and electrophysiology in the brain, as well as greater characterization of Default-Mode Network related disorders such as those on the Autism Spectrum.

8.1.2 Future Research Plan

I plan to extend the reach and impact of these miniaturized neurotechnologies and conduct research on understanding and intervening neurological disorders such as dystonia, epilepsy, and Parkinsons disease by developing wireless high-density chronic neural interfaces covering a very wide brain area. In addition to neurological disorders, understanding of ischemic stroke and trauma is also of great importance. Recent studies show that human ischemic stroke and trauma incur spreading depolarizations generating negative slow potential changes. I desire to make affirmative contributions to addressing the question how ischemic stroke can be sensed and intervened using new neural recording instrumentation specifically tailored to acquiring ultraslow (<0.1 Hz) electrocortical potentials and retain neural function through targeted stimulation. To achieve this goal, I plan to pursue three main research directions in this area:

First, I will pursue the development of a wireless ultra-high-density (1,024-channel) electrocortical recording and stimulation microsystem capable of resolving electrocorticography (ECoG) as well as ultra-slow potential signals (DC to

500 Hz), and rapidly (<1ms) recovering from large (>200mVpp) stimulation artifact transients. For its realization I envision a daisy-chain cascade of neural recording ADC array microchips interspersed between microelectrodes on a flexible substrate spanning the curved cortical surface, interfacing through minimal wiring with a transceiver hub with flexible coil antenna implanted beneath the scalp interfacing wirelessly to external electronics for wireless power reception and data communication. I already demonstrated key components of this proposed architecture in previous work. A daisy-chain cascadable 16-channel neural ADC array I recently developed offers 92 dB dynamic range and sub-microvolt input referred noise while consuming sub-microwatt power per channel, achieving a record 2.6 power efficiency factor (PEF) [39]. The neural recording chain will connect to an implantable transceiver hub performing wireless power reception and data communication over a single inductive link. Wireless power transmission and data telemetry technology for the implantable transceiver hub developed in other previous work [25] breaks through the conventional performance barrier of single-link inductive telemetry, achieving the highest data rate normalized to RF carrier frequency. We previously demonstrated data rates up to 10 Mbps, greater than half the 13.56 MHz carrier frequency, with simultaneous delivery of more than 10 mW power over the same inductive link. In addition, the hub will perform on-chip data processing for lossless data compressionenabling energy-efficient data-rich mobile BMI developments.

Second, I plan to further refine the development of neural-interface-on-chip platforms targeting neurological applications in close collaboration with clinical and neuroscience partners. By placing a recent developed neural ADC underneath an on-chip electrode, entire analog signal distribution is removed while increasing the number of recording channels effectively. Digitized signals will be serialized and transmitted to an external transceiver through the novel back-scattering technique [25]. Power and signal distribution is also important task for neural-interface-on-chip implementation since transmitted RF signals from external coils for power delivery and data communication induces severe disturbance of analog signal amplification while degrading wireless power transmission (WPT) efficiency.

Owing to a novel RF decoupled H-tree signal distribution network, my recent work successfully demonstrated signal amplification ($\geq$ 72 dB gain) under RF WPT achieving greater than 5% WPT system efficiency [35].

The third research will focus on high spatial resolution and high signal quality for information-rich BMIs. Due to volume conduction, surface electrode size and pitch are directly related to spatial resolution; small size and pitch of electrodes offers better spatial resolution [23]. However, it degrades signal quality simultaneously due to the reduced sensible area and increased impedance of electrodes. In order to mitigate this trade-off between spatial resolution and signal quality, I plan to develop multiple-input multiple-output (MIMO) beamforming recording and stimulation for spatial diversity through multiple miniaturized electrodes. The ultimate goal using such MIMO surface electrode technique is to achieve far better resolution and signal quality than penetrating electrodes.

8.2 Energy-efficient wireless bidirectional communication and power transmission to subcutaneous brain area networks

8.2.1 Contributions and Impact

Cognitive radio (CR) is an emerging electronic system for efficient use of communication bandwidth over congested spectra. While CR has found myriad applications in the mobile and military space, wearable and biomedical applications are rapidly emerging where the constraints of low-power and miniaturized operation are critical. The need for very high data transmission bandwidth in electrocortical recording has motivated the use of CR techniques that exploit spatial diversity for greater selectivity in the presence of large numbers of neural implants distributed across the brain. Hence a low-power radio-frequency (RF) receiver that enables dynamic allocation of available spectral bands, amidst significant interference and crosstalk, through spectrum sensing, signal separation, and classification is highly desirable. I led a team of graduate researchers to develop

a low-power RF baseband receiver including a 4-channel harmonic rejection mixer (HRM) for spectral tuning and a multiple-input multiple-output (MIMO) analog multiply-accumulate signal processing core (MAC) for spatial tuning (Chapters 6 & 7). While achieving greater than 65 dB harmonic rejection and 48.5 dB signal separation in test bench, with 4 antennas and 4-channel commercial low-noise amplifiers (LNAs) and mixers, I successfully demonstrate the spectral and spatial separation performance of the receiver in realistic RF conditions such as spectrally overlapping and modulated 2.4 GHz signals from two transmitters in an uncontrolled, non-line-of-sight, and multi-path environment [41], the receiver is also applicable to BMI applications for uplink communication (from implanted sensors to an external transceiver).

8.2.2 Future Research Plan

In this research area, I will take a two-track approach; developing a full RF receiver for CR and a full-duplex radio, and designing an external low-power transceiver for BMI applications.

First, I plan to develop an integrated low-power mixer-first RF receiver including a HRM, a MAC+ADC, a digital signal processor (DSP) and a phase-locked loop (PLL) clock generation unit. A 16-phase clock recovered by the PLL will provide spatial diversity in multi-channel HRM operation, enabling dynamic band allocation. Signal separation by the MAC will relax dynamic range requirements for a lower-resolution ADC, offering a significant decrease in power consumption [31]. The DSP will perform signal classification and weight updates for the spatial tuning of MAC. For weight updates, the development of an energy-efficient fast-tracking algorithm will be tackled. The blind signal separation capability offered by the MAC allows self interference cancellation in full-duplex radios, whereby the signal separation is conducted based on phase information rather than spectrum such that even signals with completely overlapping spectra can be fully separated.

Wireless-power-transmission (WPT) is another important objective. Based on my recent work on H-tree network for WPT with miniaturized implants [35], I will elaborate further improvements on WPT system efficiency by system-level

optimizations such as adaptive impedance matching. The development of ultra-low-noise power supply for on-chip loads including the neural ADCs will be tackled as well. Along with pursuing fundamental limit of performance in core sub-components, I will continue to address challenges in aspects of electromagnetic interference (EMI), biocompatible encapsulation, multi-user communication, etc. This work will truly enable a chronic implanted BMI system that makes enormous impact on neuroscience research and clinical treatments for numerous patients with neurological disorders and paralyzed limbs.

Third, I plan to implement a low-power battery-operated external transceiver for BMI applications. In order to receive signals from many implants simultaneously for higher data rate, since all implants work at the same carrier frequency, the transceiver should communicate with a single implant by a beamforming technique, the unique feature of the MAC. Furthermore, the transceiver is required to transmit data wirelessly to other devices such as computers or cell phones. Due to a severe power constraint coming from battery operation, a energy-efficient supply modulated RF power amplifier [34, 43] interfacing to a flexible skin-patch type antenna is a good candidate for unobtrusiveness.

8.3 Wearable sensors

8.3.1 Contributions and Impact

Unobtrusive wearable health monitoring devices promise to make more widespread and more prompt impact on medical diagnosis and quality of life than implantable devices owing to their ease, comfort, and accessibility of use. For autonomous operation, these sensors are required to harvest energy directly from the environment, the interrogator, or the signal of interest. The technologies and design techniques I developed and acquired throughout my Ph.D. studies (Chapters 3 through 7) can be directly applied in the wearable setting as well. For example, the wireless power and data telemetry systems that I developed for implantable use [42] can be immediately adopted into RF-powering wearable sensors. In addition, a non-contact sensing technology with a high front-end gain that I recently

developed will be an essential element for various sensor applications [24].

8.3.2 Future Research Plan

I plan to attack three main research directions in this research theme. First, I plan to investigate flexible-substrate-based distributed sensors for ambulatory health monitoring, entertainment and sport applications. For example, a flexible energy harvester near heart is a good cardiac arrest monitoring power autonomous sensor. When heart attack happens, outcomes from the flexible harvester will be below a certain threshold, triggering one-time event using scavenged energy from the sensor to a central hub such as cell-phone to make an emergency alarm.

The second research plan is to develop human-blackbox with low-power event-driven vision sensors. These vision sensors will be idle in normal operation, but whenever they detect some events, these sensors will start to capture images. The sensors will be required to have small form-factor for body-area distribution and eventually power autonomous. I will further refine my recent work for an asynchronous neuromorphic vision sensor [68] toward low-cost in power consumption, and high-bandwidth response to visual events. Since the neuromorphic vision sensor generates "spikes" (action potentials) as output signals, the sensor is directly compatible with neuromophic processors.

The third research direction will include development of body-area network for the sensors and a central hub. The distributed sensors will be as small as possible. Thus, for communications, a central hub will share most burden. For this work, I will extend my works on MIMO beamforming transceiver for an ultra-low-power central hub. This hub can be included in smartphones to utilize myriad resources related to smartphones, and provide user-friendly interface.

8.4 Conclusion

Investigations detailed above will advance myself towards a common goal, improvement in the quality of human life through technological innovation. The everything-on-chip integrated framework will provide a unique flagship tool for my

future research, and will offer an integration platform to host various sensors and actuators in our future life with ubiquitous healthcare and fitness monitoring. In addition, the technology innovations will foster the convergence of these technologies to real-life applications and vibrancy to industry. I believe that the pursuit of these research subjects will enable myself to contribute to the diversified and dynamic research environment enabled by superb colleagues in neuroengineering, neurology, and neuroscience.

Bibliography

[1] D. Ahn and M. Ghovanloo. Optimal design of wireless power transmission links for millimeter-sized biomedical implants. *IEEE Transactions on Biomedical Circuits and Systems*, 10(1):125–137, Feb. 2016.

[2] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. Abidi. An 800MHz to 5GHz software-defined radio receiver in 90nm CMOS. In *IEEE ISSCC Dig. Tech. Papers*, 2006.

[3] G. Bawa and M. Ghovanloo. Active high power conversion efficiency rectifier with built-in dual-mode back telemetry in standard cmos technology. *IEEE Transactions on Biomedical Circuits and Systems*, 2(3):184–192, Sept. 2008.

[4] M. Bazes. Two novel fully complementary self-biased CMOS differential amplifiers. *IEEE Journal of Solid-State Circuits*, 26(2):165–168, Feb. 1991.

[5] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi. CMOS mixers and polyphase filters for large image rejection. *IEEE J. of Solid-State Circuits*, 36(6):873–887, June 2001.

[6] J. Borremans, B. van Liempd, E. Martens, S. Cha, and J. Craninckx. A 0.9 V low-power 0.4 - 6 GHz linear SDR receiver in 28 nm CMOS. In *Symposium on VLSI Circuits (VLSIC)*, pages C146–C147, June 2013.

[7] M. Capogrosso, T. Milekovic, D. Borton, F. Wagner, E. M. Moraud, J.-B. Mignardot, N. Buse, J. Gandar, Q. Barraud, D. Xing, E. Rey, S. Duis, Y. Jianzhong, W. K. D. Ko, Q. Li, P. Detemple, T. Denison, S. Micera, E. Bezard, J. Bloch, and G. Courtine. A brainspine interface alleviating gait deficits after spinal cord injury in primates. *Nature*, 539(7628):284–288, 11 2016.

[8] A. Celik, M. Stanacevic, and G. Cauwenberghs. Gradient Flow Independent Component Analysis in Micropower VLSI. In *Adv. Neural Information Processing Systems (NIPS 2006)*, volume 8, pages 187–194. Cambridge: MIT Press, 2006.

[9] H. K. Cha, S. S. Song, H. T. Kim, and K. Lee. A CMOS harmonic rejection mixer with mismatch calibration circuitry for digital TV tuner applications. *IEEE Microw. Compon. Lett.*, 18(9):617–619, Sept. 2008.

[10] H. Chandrakumar and D. Markovic. A 2.8μW 80mVpp-linear-input-range 1.6GΩ-input impedance bio-signal chopper amplifier tolerant to common-mode interference up to 650mVpp. In *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.

[11] J. Charthad, M. J. Weber, T. C. Chang, and A. Arbabian. A mm-sized implantable medical device (imd) with ultrasonic power transfer and a hybrid bi-directional data link. *IEEE Journal of Solid-State Circuits*, 50(8):1741–1753, Aug 2015.

[12] W.-C. Chen, S.-Y. Ping, T.-C. Huang, Y.-H. Lee, K.-H. Chen, and C.-L. Wey. A switchable digital–analog low-dropout regulator for analog dynamic voltage scaling technique. *IEEE Journal of Solid-State Circuits*, 49(3):740–750, March 2014.

[13] W.-M. Chen, H. Chiueh, T.-J. Chen, C.-L. Ho, C. Jeng, M.-D. Ker, C.-Y. Lin, Y.-C. Huang, C.-W. Chou, T.-Y. Fan, M.-S. Cheng, Y.-L. Hsin, S.-F. Liang, Y.-L. Wang, F.-Z. Shaw, Y.-H. Huang, C.-H. Yang, and C.-Y. Wu. A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic CMOS SoC for Real-Time Epileptic Seizure Control. *IEEE Journal of Solid-State Circuits*, 49(1):232–247, Jan. 2014.

[14] L. Cheng, W. H. Ki, and C. Y. Tsui. A 6.78-MHz Single-Stage Wireless Power Receiver Using a 3-Mode Reconfigurable Resonant Regulating Rectifier. *IEEE Journal of Solid-State Circuits*, 52(5):1412–1423, May 2017.

[15] L. Cheng, W. H. Ki, T. T. Wong, T. S. Yim, and C. Y. Tsui. A 6.78MHz 6W wireless power receiver with a 3-level $1\times$ / $1/2\times$ / $0\times$ reconfigurable resonant regulating rectifier. In *IEEE International Solid-State Circuits Conference (ISSCC)*, pages 376–377, Jan. 2016.

[16] Y. M. Chi, C. Maier, and G. Cauwenberghs. Ultra-high input impedance, low noise integrated amplifier for noncontact biopotential sensing. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 1(4):526–535, Dec. 2011.

[17] J.-H. Choi, S.-K. Yeo, S. Park, J.-S. Lee, and G.-H. Cho. Resonant regulating rectifiers (3r) operating for 6.78 MHz resonant wireless power transfer (RWPT). *IEEE Journal of Solid-State Circuits*, 48(12):2989–3001, Dec. 2013.

[18] E. E. Christensen, T. S. Curry III, and J. E. Dowdey. *An Introduction to the Physics of Diagnostic Radiology, Second Edition.* Lea & Febiger, 1978.

[19] M. Ding, P. Harpe, Y.-H. Liu, B. Busze, K. Philips, and H. de Groot. A 5.5 fJ/conv-step 6.4 MS/S 13b SAR ADC utilizing a redundancy-facilitated background error-detection-and-correction scheme. In *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2015.

[20] R. W. Erickson and D. Maksimovic. *Fundamentals of Power Electronics, 2nd Ed.* Springer US, 2001.

[21] FCC. In the matter of the unlicensed operation in the TV broadcast bands additional spectrum for unlicensed devices below 900 MHz in the 3 GHz band. Technical report, FCC, 2010.

[22] A. Ghaffari, E. Klumperink, F. van Vliet, and B. Nauta. Simultaneous spatial and frequency-domain filtering at the antenna inputs achieving up to +10 dBm out-of-band/beam P1dB. In *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 84–85, Feb 2013.

[23] S. Ha, A. Akinin, J. Park, C. Kim, H. Wang, C. Maier, P. P. Mercier, and G. Cauwenberghs. Silicon-Integrated High-Density Electrocortical Interfaces. *Proceedings of the IEEE*, 105(1):11–33, Jan. 2017.

[24] S. Ha, C. Kim, Y. M. Chi, A. Akinin, C. Maier, A. Ueno, and G. Cauwenberghs. Integrated Circuits and Electrode Interfaces for Noninvasive Physiological Monitoring. *IEEE Transactions on Biomedical Engineering*, 61(5):1522–1537, May 2014.

[25] S. Ha, C. Kim, J. Park, S. Joshi, and G. Cauwengerghs. Energy Recycling Telemetry IC With Simultaneous 11.5 mW Power and 6.78 Mb/s Backward Data Delivery Over a Single 13.56 MHz Inductive Link. *IEEE Journal of Solid-State Circuits*, 51(11):2664–2678, Nov. 2016.

[26] J. Hartings, T. Watanable, J. Dreier, S. Major, L. Vendelbo, and M. Fabricius. Recovery of Slow Potentials in AC-Coupled Electrocorticography: Application to Spreading Depolarizations in Rat and Human Cerebral Cortex. *Journal of Neurophysiology*, 102(2):2563–2575, Oct. 2009.

[27] S. Haykin. Cognitive radio: brain-empowered wireless communications. *IEEE Journal on elected Areas in Communications*, 23(2):201–220, Feb 2005.

[28] A. Ibrahim and M. Kiani. A Figure-of-Merit for Design and Optimization of Inductive Power Transmission Links for Millimeter-Sized Biomedical Implants. *IEEE Transactions on Biomedical Circuits and Systems*, 10(6):1100–1111, Dec. 2016.

[29] D. A. Johns and K. Martin. *Analog Integrated Circuit Design.* Wiley, 1996.

[30] B. C. Johnson, S. Gambini, I. Izyumin, A. Moin, A. Zhou, G. Alexandrov, S. R. Santacruz, J. M. Rabaey, J. M. Carmena, and R. Muller. An implantable 700μW 64-channel neuromodulation IC for simultaneous recording and stimulation with rapid artifact recovery. In *Symposium on VLSI Circuits (VLSI Circuits)*, Jun. 2017.

[31] S. Joshi, S. Ha, Y. M. Chi, and G. Cauwenberghs. 2pJ/MAC 14b 8×8 linear transform mixed- signal spatial filter in 65nm CMOS with 84dB interference suppression. In *IEEE International Solid-State Circuits Conference (ISSCC)*, pages 364–365, Feb. 2017.

[32] L. Karumbaiah, T. Saxena, D. Carlson, K. Patil, R. Patkar, E. A. Gaupp, M. Betancur, G. B. Stanley, L. Carin, and R. V. Bellamkonda. Relationship between intracortical electrode design and chronic recording function. *Biomaterials*, 34(33):8061–8074, November 2013.

[33] H. Kassiri, R. Pazhouhandeh, N. Soltani, M. T. Salam, P. Carlen, J. L. P. Velazquez, and R. Genov. All-Wireless 64-Channel 0.013mm^2/ch Closed-Loop Neurostimulator with Rail-to-Rail DC Offset Removal. In *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2017.

[34] C. Kim, C.-E. Chae, Y.-S. Yuk, C. M. Thomas, Y.-G. Kim, J.-K. Kwon, S. Ha, G. Cauwenberghs, and G.-H. Cho. A 500 MHz-bandwidth 7.5 mV_{PP}-ripple Power-Amplifier Supply Modulator for RF Polar Transmitters. *IEEE Journal of Solid-State Circuits*, 2018.

[35] C. Kim, S. Ha, A. Akinin, J. Park, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs. Design of Miniaturized Wireless Power Receivers for mm-sized Implants. In *IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–8, Apr. 2017.

[36] C. Kim, S. Ha, J. Park, A. Akinin, P. Mercier, and G. Cauwenberghs. A 144 MHz integrated resonant regulating rectifier with hybrid pulse modulation. In *Symposium on VLSI Circuits (VLSI Circuits)*, pages 284–285, 2015.

[37] C. Kim, S. Ha, J. Park, A. Akinin, P. Mercier, and G. Cauwenberghs. A 144 MHz Fully Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation for mm-sized Implants. *IEEE Journal of Solid-State Circuits*, 2017.

[38] C. Kim, S. Ha, C. Thomas, S. Joshi, J. Park, L. Larson, and G. Cauwenberghs. A 7.86 mW +12.5 dBm in-band IIP3 8-to-320 MHz capacitive harmonic rejection mixer in 65nm CMOS. In *European Solid State Circuits Conference (ESSCIRC)*, pages 227–230, Sept 2014.

[39] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs. A 92dB dynamic range subμV_{rms} noise 0.8μW/ch neural recording ADC array with predictive digital autoranging. In *IEEE International Solid-State Circuits Conference (ISSCC)*, 2018.

[40] C. Kim, S. Joshi, C. Thomas, S. Ha, A. Akinin, L. Larson, and G. Cauwenberghs. A CMOS 4-Channel MIMO Baseband Receiver with 65dB Harmonic Rejection over 48MHz and 50dB Spatial Signal Separation over 3MHz at 1.3mW. In *Symposium on VLSI Circuits (VLSIC)*, 2015.

[41] C. Kim, S. Joshi, C. Thomas, S. Ha, L. Larson, and G. Cauwenberghs. A 1.3 mW 48 MHz 4-channel MIMO baseband receiver with 65 dB harmonic rejection and 48.5 dB spatial signal separation. *IEEE Journal of Solid State Circuits*, April 2016.

[42] C. Kim, J. Park, A. Akinin, S. Ha, P. P. Mercier, and G. Cauwenberghs. A fully integrated 144 MHz wireless-power-receiver-on-chip with an adaptive buck-boost regulating rectifier and low-loss h-tree signal distribution. In *Symposium on VLSI Circuits (VLSI Circuits)*, pages 284–285, 2016.

[43] C. Kim, C. seok Chae, Y.-S. Yuk, Y.-G. Kim, J. kee Kwon, and G.-H. Cho. A 105dB-gain 500MHz-bandwidth 0.1Ω-output-impedance amplifier for an amplitude modulator in 65nm CMOS. In *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 88–89, Feb 2010.

[44] B. Le, T. Rondeau, J. Reed, and C. Bostian. Analog-to-digital converters. *IEEE Signal Processing Magazine*, 22(6):69–77, Nov 2005.

[45] V. H. Le, H. N. Nguyen, I. Y. Lee, S. K. Han, and S. G. Lee. A passive mixer for a wideband TV tuner. *IEEE Trans. Circuits Syst. II: Exp. Briefs*, 58(7):398–401, July 2011.

[46] B. Lee, M. Kiani, and M. Ghovanloo. A Triple-Loop Inductive Power Transmission System for Biomedical Applications. *IEEE Transactions on Biomedical Circuits and Systems*, 10(1):138–148, Feb. 2016.

[47] B. Lee, P. Yeon, and M. Ghovanloo. A Multicycle Q-Modulation for Dynamic Optimization of Inductive Links. *IEEE Transactions on Industrial Electronics*, 63(8):5091–5100, Aug. 2016.

[48] H. Lee, R. V. Bellamkonda, W. Sun, and M. E. Levenston. Biomechanical analysis of silicon microelectrode-induced strain in the brain. *Journal of Neural Engineering*, 2(4):81–89, Dec. 2005.

[49] H.-M. Lee and M. Ghovanloo. An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(8):1749–1760, Aug. 2011.

[50] H.-M. Lee and M. Ghovanloo. A high frequency active voltage doubler in standard cmos using offset-controlled comparators for inductive power transmission. *IEEE Transactions on Biomedical Circuits and Systems*, 7(3):213–224, June 2013.

[51] H. M. Lee, C. S. Juvekar, J. Kwong, and A. P. Chandrakasan. A nonvolatile flip-flop-enabled cryptographic wireless authentication tag with per-query key update and power-glitch attack countermeasures. *IEEE Journal of Solid-State Circuits*, 52(1):272–283, Jan. 2017.

[52] H. M. Lee, H. Park, and M. Ghovanloo. A Power-Efficient Wireless System With Adaptive Supply Control for Deep Brain Stimulation. *IEEE Journal of Solid-State Circuits*, 48(9):2203–2216, Sept. 2013.

[53] X. Li, X. Meng, C. Y. Tsui, and W. H. Ki. Reconfigurable resonant regulating rectifier with primary equalization for extended coupling- and loading-range in bio-implant wireless power transfer. *IEEE Transactions on Biomedical Circuits and Systems*, 9(6):875–884, Dec. 2015.

[54] X. Li, C. Y. Tsui, and W. H. Ki. A 13.56 MHz Wireless Power Transfer System With Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices. *IEEE Journal of Solid-State Circuits*, 50(4):978–989, Apr. 2015.

[55] X. Li, C.-Y. Tsui, and W.-H. Ki. Wireless power transfer system using primary equalizer for coupling- and load-range extension in bio-implant applications,. In *IEEE International Solid-State Circuits Conference (ISSCC)*, pages 228–229, 2015.

[56] M. Mark. *Powering mm-Size Wireless Implants for Brain-Machine Interfaces*. PhD thesis, Electrical Engineering and Computer Sciences, University of California at Berkeley, December 2011.

[57] M. Mark, Y. Chen, C. Sutardja, C. Tang, S. Gowda, M. Wagner, D. Werthimer, and J. Rabaey. A $1mm^3$ 2 Mbps 330fJ/b Transponder for Implanted Neural Sensors. In *Symposium on VLSI Circuits (VLSI Circuits)*, pages 168–169, 2011.

[58] G. C. McConnell, H. D. Rees, A. I. Levey, C.-A. Gutekunst, R. E. Gross, and R. V. Bellamkonda. Implanted neural electrodes cause chronic, local inflammation that is correlated with local neurodegeneration. *Journal of Neural Engineering*, 6, October 2009.

[59] M. D. Menz, . Oralkan, P. T. Khuri-Yakub, and S. A. Baccus. Precise neural stimulation in the retina using focused ultrasound. *Journal of Neuroscience*, 33(10):4550–4560, 2013.

[60] P. P. Mercier and A. P. Chandrakasan. Rapid Wireless Capacitor Charging Using a Multi-Tapped Inductively-Coupled Secondary Coil. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 60(9):2263–2272, Sept. 2013.

[61] P. P. Mercier and A. P. Chandrakasan. *Ultra-Low-Power Short-Range Radios*. Springer, 2015.

[62] R. Muller, H.-P. Le, W. Li, P. Ledochowitsch, S. Gambini, T. Bjorninen, A. Koralek, J. Carmena, M. Maharbiz, E. Alon, and J. Rabaey. A Minimally Invasive 64-Channel Wireless μECoG Implant. *IEEE Journal of Solid-State Circuits*, 50(1):344–359, Jan. 2015.

[63] D. Murphy, H. Darabi, and H. Xu. A noise-cancelling receiver with enhanced resilience to harmonic blockers. In *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 68–69, Feb 2014.

[64] D. Murphy, H. Darabi, and H. Xu. A Noise-Cancelling Receiver Resilient to Large Harmonic Blockers. *IEEE Journal of Solid-State Circuits*, 50(6):1336–1350, June 2015.

[65] M. Notten, M. Bernard, V. Rambeau, and J. van Sinderen. A cmos quadrature down-conversion mixer with analog I/Q correction obtaining 55 dB of image rejection for TV on mobile applications. In *IEEE RFIC Symposium*, 2006.

[66] S. O'Driscoll, A. Poon, and T. Meng. A mm-sized implantable power receiver with adaptive link compensation. In *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 294–295, 2009.

[67] S. Ozeri and D. Shmilovitz. Ultrasonic transcutaneous energy transfer for powering implanted devices. *Ultrasonics*, 50(6):556–566, 2010.

[68] J. Park, S. Ha, C. Kim, S. Joshi, T. Yu, W. Ma, and G. Cauwenberghs. A 12.6 mW 8.3 Mevents/s contrast detection 128×128 imager with 75 dB intra-scene DR asynchronous random-access digital readout. In *IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings*, pages 564–567, Oct. 2014.

[69] S. S. Polikov, P. A. Tresco, and W. M. Reichert. Response of brain tissue to chronically implanted neural electrodes. *Journal of Neuroscience Methods*, 148(1):1–18, 2005.

[70] A. Poon, S. O'Driscoll, and T. Meng. Optimal frequency for wireless power transmission into dispersive tissue. *IEEE Transactions on Antennas and Propagation*, 58(5):1739–1750, May 2010.

[71] J. M. Rabaey, M. Mark, D. Chen, C. Sutardja, C. Tang, S. Gowda, M. Wagner, and D. Werthimer. Powering and communicating with mm-size implants. In *Design, Automation Test in Europe*, pages 1–6, Mar. 2011.

[72] A. Rafi, A. Piovaccari, P. Vancorenland, and T. Tuttle. A harmonic rejection mixer robust to RF device mismatches. In *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 66–68, Feb 2011.

[73] A. Rafi and T. Viswanathan. Harmonic Rejection Mixing Techniques Using Clock-Gating. *IEEE Journal of Solid-State Circuits*, 48(8):1862–1874, Aug 2013.

[74] B. Razavi. Challenges in the design of cognitive radios. In *Custom Integrated Circuits Conference*, pages 391–398, Sept 2009.

[75] B. Razavi. Cognitive Radio Design Challenges and Techniques. *IEEE Journal of Solid-State Circuits*, 45(8):1542–1553, Aug 2010.

[76] E. Rebeiz, F.-L. Yuan, P. Urriza, D. Markovic, and D. Cabric. Energy-Efficient Processor for Blind Signal Classification in Cognitive Radio Networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(2):587–599, Feb 2014.

[77] B. Sahu and G. A. Rincon-Mora. An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptive On-Time Pulse-Frequency Modulation (PFM) Control. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(2):312–321, Feb. 2007.

[78] R. Sarpeshkar. *Ultra Low Power Bioelectronics*. Cambridge: University Press, 2010.

[79] D. Seo, J. M. Carmena, J. M. Rabaey, M. M. Maharbiz, and E. Alon. Model validation of untethered, ultrasonic neural dust motes for cortical recording. *Journal of Neuroscience Methods*, 244:114–122, 2015.

[80] D. Seo, H. Y. Tang, J. M. Carmena, J. M. Rabaey, E. Alon, B. E. Boser, and M. M. Maharbiz. Ultrasonic beamforming system for interrogating multiple implantable sensors. In *2015 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 2673–2676, 2015.

[81] M. C. M. Soer, E. A. M. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta. A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving $\gg$ 11dbm IIP3 and $\ll$ 6.5 dB NF. In *IEEE ISSCC Dig. Tech. Papers*, 2009.

[82] B.-S. SONG. *Micro CMOS DESIGN*. CRC Press, 2012.

[83] C. M. Thomas and L. E. Larson. Broadband synthetic transmission line N-path filter design. *IEEE Transactions on Microwave Theory and Techniques* (*accepted*), 2015.

[84] J. van den Heuvel and D. Cabric. Spatial filtering approach for dynamic range reduction in cognitive radios. In *IEEE International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC)*, pages 2657–2662, Sept 2010.

[85] J. van den Heuvel, J.-P. Linnartz, P. Baltus, and D. Cabric. Full MIMO Spatial Filtering Approach for Dynamic Range Reduction in Wideband Cognitive Radios. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 59(11):2761–2773, Nov 2012.

[86] B. van Liempd, J. Borremans, S. Cha, E. Martens, H. Suys, and J. Craninckx. IIP2 and HR calibration for an 8-phase harmonic recombination receiver in 28nm. In *IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–4, Sept 2013.

[87] V. Venkateswaran and A.-J. van der Veen. Analog Beamforming in MIMO Communications With Phase Shift Networks and Online Channel Estimation. *Signal Processing, IEEE Transactions on*, 58(8):4131–4143, Aug 2010.

[88] R. Walden. Analog-to-digital converter survey and analysis. *IEEE Journal on Selected Areas in Communications*, 17(4):539–550, Apr 1999.

[89] J. Weldon, R. Narayanaswami, R. J.C., L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. Gray. A 1.75-ghz highly integrated narrow-band cmos transmitter with harmonic-rejection mixers. *IEEE Journal of Solid-State Circuits*, 36(12):2003–2015, Dec 2001.

[90] P. N. T. Wells. *Biomedical ultrasonics*. Academic Press, 1977.

[91] F.-L. Yuan, R. K. Palani, S. Basir-Kazeruni, H. Shih, A. Saha, R. Harjani, and D. Markovic. A Throughput-Agnostic 11.9-13.6GOPS/mW Multi-Signal Classification SoC for Cognitive Radios in 40nm CMOS. In *Symposium on VLSI Circuits Digest of Technical Papers*, 2015.

[92] F.-L. Yuan, T.-H. Yu, and D. Markovic. A 500MHz blind classification processor for cognitive radios in 40nm CMOS. In *Symposium on VLSI Circuits Digest of Technical Papers*, June 2014.

[93] M. Zargham and P. Gulak. Maximum achievable efficiency in near-field coupled power-transfer systems. *IEEE Transactions on Biomedical Circuits and Systems*, 6(3):228–245, June 2012.

[94] M. Zargham and P. Gulak. A 0.13 μm CMOS integrated wireless power receiver for biomedical applications. In *European Solid State Circuits Conference (ESSCIRC)*, pages 137–140, 2013.

[95] M. Zargham and P. Gulak. Fully integrated on-chip coil in 0.13 μm cmos for wireless power transfer through biological media. *IEEE Transactions on Biomedical Circuits and Systems*, 9(2):259–271, April 2015.