UNIVERSITY OF CALIFORNIA,
IRVINE

Millimeter-Wave Wireless Power Transfer Systems for the Internet of Things

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering and Computer Science

by

Med Nariman

Dissertation Committee:
Professor Franco De Flaviis, Chair
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2016

DEDICATION

To

my wife, my mom, and my family

in recognition of their worth

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I dedicate this work to the true angels of my life: my wife, my mom, and my family.

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ACHIEVEMENTS OF THIS WORK

- Wireless Power Transfer System
    - Most Compact WPT Solution Ever Built
    - First Full-System mm-Wave WPT Solution
- mm-Wave Energy Harvester in Digital CMOS; Design and Analysis
    - Highest Output Power
    - Highest Efficiency
    - Formulated All Key Specifications for the First Time
- 60 GHz Transmitter in Digital CMOS; Design and Implementation
    - Highest Power Delivery
    - Highest Power Density
    - Highest Level of Integration
- Grid Array Antennas; Design and Implementation
    - Highest EIRP Production
    - 70º Beam Steering without RF Frontend Complexity

ABSTRACT OF THE DISSERTATION

Millimeter-Wave Wireless Power Transfer for the Internet of Things

By

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Doctor of Philosophy in Electrical Engineering and Computer Science

University of California, Irvine, 2016

Professor Franco De Flaviis, Chair

The Internet of Things (IoT) would add computational power to a plethora of ordinary objects. Potential applications are vast and vary in terms of maturity from sensors tracking energy usage to smart wearables and many more futuristic applications. A challenge shared by many of such small devices, in the order of a few centimeters in length and width, is battery and power. Cost, size, weight, and lifetime of the battery motivate alternative methods for providing energy to such devices. A practical Wireless Power Transfer (WPT) system which can power battery-less and charge coil-free smart everyday-objects has a tremendous potential to address this demand. In this work we offer a reliable solution. The 60-GHz WPT system that is built in this project can be employed by any smart device which can be placed at a reasonably close distance to its power transmitter, without the alignment

and proximity challenges which are associated with the magnetic charging solutions. The leading applications to benefit enormously from this new 60-GHz WPT technology are miniature IoT devices, smart charge cards, business cards and IDs, smart posters, sensor fusion, and wireless flash memories.

In this work, the first reported full-system 60-GHz WPT solution which can power battery-less and charge coil-free compact smart devices is presented. The system is fabricated in a 40-nm digital CMOS process and an inexpensive 500-μm CCL-HL832MG antenna packaging material. The rectenna (RX) of this 60-GHz WPT system consists of a grid antenna with a measured gain of 10.7 dBi, integrated with a tuned complementary cross-coupled oscillator-like rectifier. It harvests DC power at a rate of 1 mW with a 28.2% RF-to-DC Power Conversion Efficiency (PCE). This PCE rate is significantly higher than the prior art and reaches 32.8% for 1.4 mA output current. A novel theoretical analysis of the unique rectifier circuitry is presented which helps formulating all key specifications and identifying the design trade-offs. We present a cascode version of the energy harvester that produces higher DC output voltage and higher PCE in low current regime. The theoretical analysis and the results of the measurement for that harvester is also presented. The transmitter (TX) is equipped with a quad-core power amplifier which produces a total saturated output power (P_{sat}) of 24.6 dBm, which is the highest reported power delivery in digital CMOS technology at mm-wave bands. The TX peak PAE is 9.4%. The quad-core PA performs a 4 × 8-way differential power combining and implements a binary-tree architecture by using power-splitting transformers which perform intra-stage matching too. The designed 2 × 2 grid array antenna helps the TX produce a peak EIRP level of 35.3 dBm. The coupling between the TX and RX antennas within 4 cm spacing is between -18.9 and -17.4dB. The results of full-system

characterizations of the WPT solution and the measurements data of the individually-fabricated grid antennas, harvester, transmitter, and all building blocks are reported. Programmability in the input polarities of the quad-core PA offers output power control and beam-steering capabilities to this 60-GHz WPT system. A four-input grid antenna is designed for the TX which in simulation shows an effective 70° beam-steering range in the broadside direction.

In order to demonstrate how the design and implementation of all the 60-GHz circuitry has been as successful as they are, the design of the VCOs, quadrature VCOs, PAs, unit-cell devices, pads and calibration circuitry, passive components like inductors, transformers, capacitors, the patch antennas, and the grid array antennas that have been done before the final implementation of the full wireless power transfer system are presented as well and the key design points are specified and explained. The architecture study for the transmitter and the energy harvester are also included in this dissertation since they have been most vital parts of accomplishing the design of the highest transmit power delivery and highest rectenna power conversion efficiency in digital CMOS technology. The 60-GHz WPT system designed for this work can serve miniature sized smart everyday-objects which require milliwatt-level power delivery and work in contact-less and close-proximity distances.

Introduction

Maxwell's equations, formulated in 1862, provide the fundamental theoretical bases for wireless power transfer. The Poynting vector of Electrodynamics conceptually introduces radio waves as energy flows [4]. Nicola Tesla used resonators for inductive power transmission. There are three mechanisms to perform Wireless Power Transfer (WPT): inductive coupling, resonant coupling, and radio waves. WPT systems have been traditionally implemented either in 125 kHz (LF band) or 13.56 MHz (HF band) using inductive or resonant couplers [40]. More recently, 900 MHz (UHF band), has hosted WPT systems to support RFID applications which utilize antennas in lieu of couplers and benefit from higher levels of integration, access to larger bandwidths, and longer ranges of operation by utilizing antennas in lieu of couplers [5-7] and [28-39]. Millimeter-wave WPT systems have area and cost advantages compared to UHF and all other current solutions, since they benefit from lower wavelength and the possibility of antenna integration. We showed that in our peer-reviewed publications [1-3]. In fact, the 60-GHz ISM band can be the new home to the WPT systems for Internet of Things (IoT) applications by offering the most inexpensive integrated solutions without having coexistence issues. Using 60 GHz WPT solutions

for wireless applications grants them access to the 7GHz ISM band which can be used to produce high throughputs. The 60 GHz WPT systems could enable new products and services in the near future and could revolutionize high-performance close-proximity wireless applications. An individual could carry their life-long electronic health records, together with detailed medical insurance information, on a wallet-sized high-speed smartcard with a rewritable nonvolatile memory. High-speed wireless flash memories, either individually or embedded in different gadgets, could store collections of digital books, movies, music, and other data. The 60 GHz frequency band in particular offers a 7dB higher FCC limit for peak EIRP level, higher antenna array gain per unit size, and much less coexistence issues compared with any alternative lower frequency band [41]. Successful implementations of fully-integrated highly-directive antennas have been shown in the mid-mm-wave band [42].

The use of mm-wave frequency bands for power harvesting has been suggested in recent years [8-11], but based on our study, this work is the first reported implementation of a full-system WPT system in mm-wave bands, which comprises the implementation of high-power TX and high efficiency rectenna, as well as the design and integration of RX and TX grid antennas, to produce milliwatt-scale DC output power and peak Power Conversion Efficiency (PCE) rates in excess of 30%, figures that are significantly higher than those of the prior art. The peak PCE reported by [8-11] are respectively 2% (version with the antenna), 8%, 7%, and 1.2%. In [8] and [11] multi-stage Dickson multiplier is used as a rectifier and in [9] and [10] multi-stage inductor-peaked is presented. But none of these works achieves a DC output power level larger than 0.25 mW. To achieve significantly higher DC output power and PCE rates a complementary cross-coupled rectifier, which was proposed in [12] for low frequency applications, is adopted for mm-wave frequency operation by turning it to a tuned oscillator-like circuitry. A novel theoretical analysis

of this unique architecture to formulate all key specifications and identify all design tradeoffs is presented.

The aforementioned references for mm-wave energy harvesting do not cover the design of the high power mm-wave transmitter. As a result, we compare the performance of the quad-core power amplifier of this 60-GHz WPT solution with what has been achieved by the leading mm-wave PA design teams in digital CMOS technology, with this notion that the goal for this design is purely power transfer and not data transfer. Achieving a high P_{sat} is the main objective of this design and high peak Power-Added Efficiency (PAE) is the second important specification. The P_{sat} reported in [13] through [18] are 20.9, 15.8, 22.6, 19.3, 18.6, 16.6 dBm, among which the highest number, 22.6 dBm, has been also achieved by our group. In order to produce power delivery level as high as 24.6 dBm at 60 GHz, which is achieved by this work, without violating voltage reliability limits, a 4 × 8-way differential power combining is implemented by the use of a quad-core PA. This is 4 times as high as the highest level of integration achieved by the references which is 8-way differential by [15] and [18]. For each PA core a binary-tree architecture is realized with the use of power-splitting transformers at the output of each stage. As such, the number of virtually parallel stages doubles from each stage to the next. The last stage of each PA core has 8 pseudo-differential PA units. The peak PAE of the transmitter is 9.4% which is competitive, considering the high power delivery. None of the referenced mm-wave PAs include the design of the antenna. But by using an inexpensive 500-µm CCL-HL832MG antenna packaging material we prove miniature antennas with decent gain and directivity can be integrated with mm-wave WPT systems. The project required the design and integration of the grid antennas and redesign of the circuitry in flip-chip technology in order to integrate with the antennas and realize the integrated rectenna.

In addition, we review prior technologies for wireless power transfer that have served the purpose of wireless power transfer in Chapter 1. The traditional technologies that are built to perform WPT were in Low Frequency (LF) band, High Frequency (HF) band, and more recently Ultra High Frequency (UHF) band. We review some examples for each of these designs. Chapter 2 reviews the mm-wave integrated circuit design in digital CMOS technology that we had done prior building the final product. These circuitry are different mm-wave VCOs, quadrature VCOs, power amplifiers, mm-wave rectifiers, passive components like inductors, transformers, capacitors, and unit-cells of the devices for mm-wave purposes, and finally calibration circuitry, power grids, and pads. Chapter 3 talks about the design of the antennas that have assisted this 60-GHz WPT system and also other samples that we made before we designed the final grid array antennas. Chapter 4 is dedicated to the theoretical analysis of the mm-wave power harvesters. The focus is on two versions. Both use the supply-less complementary tuned oscillator-like rectifiers. The first version is single stage and the second one has a cascode configuration. The design of the final product which is the first reported integrated mm-wave wireless power transfer system in digital CMOS is discussed in Chapter 5. The results of performance characterization in the forms of full-system measurements or mm-wave probing at 60-GHz probe-station are detailed in Chapter 6, where we compare the results of this work with other reported designs too.

Chapter 1

TRADITIONAL SOLUTIONS

The term close-proximity refers to wireless communication ranges similar to those of the Proximity Integrated Circuit Cards (PICCs), which follow ISO/IEC 14443-4 transmission protocols and support contactless communication with a few centimeter ranges [19]. A TX antenna with a dimension larger than half-wavelength (λ/2) creates four different regions of electromagnetic field around it as illustrated in Fig. 1.1, which was modified from a figure in [20]. The distance within λ/2π of the antenna is called the reactive region, in which the field has both tangential and orthogonal components. The outer bound of this reactive region for 900 MHz

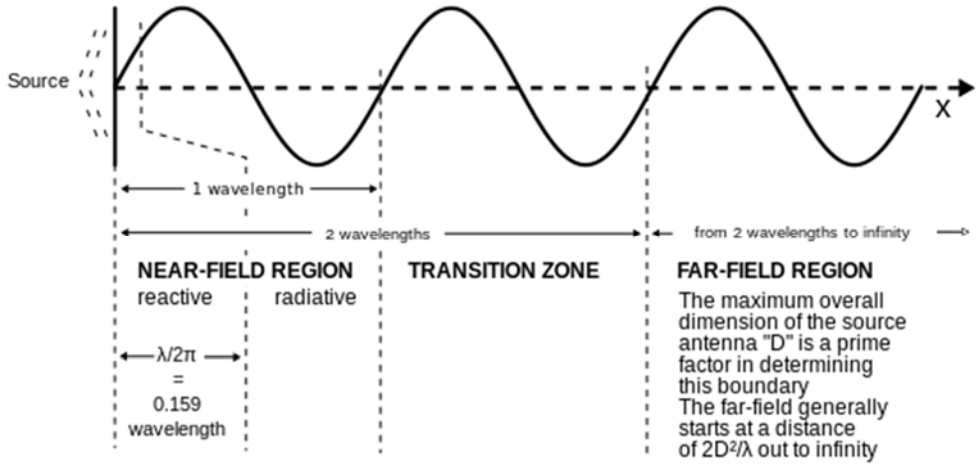


Fig. 1.1 Different electromagnetic field regions for an antenna with largest radiating dimension of D and radiating wavelength of λ in free space.

frequency is 5cm, whereas it is 0.8 mm for 60 GHz frequency. This means for all practical close-proximity purposes 60 GHz antennas, unlike UHF antennas, behave in radiative manners.

In the rest of the near-field region, the antenna behavior is radiative. It generates a beam which is not fully formed and changes with distance. The near-field region can extend as far as the greater of λ and D^2 / λ, where D is the largest radiating dimension of the antenna. In the transition region between the near-field and the far-field, the Fresnel diffraction equation, which is an approximation of the Kirchhoff-Fresnel equation for the near-field region, describes the field; therefore it is called the Fresnel region. The far-field behavior starts emerging from a distance larger than the greater of 2λ and the Fraunhofer distance (d_f) which is equal to $2 D^2 / \lambda$. For an n×n patch antenna array $D = n \lambda / 2$, therefore $d_f = n^2 \lambda / 2$. Beyond this distance, the far-field behavior is overwhelmingly dominant and the beam is fully formed. In the far-field region, unlike the near-field region, the power density has a fully deterministic relation with the distance from the TX antenna. It is inversely proportional to the distance squared.

The concept of the wireless power transfer has been formulated by the Maxwell's equations, but using it as a solution to power gadgets does not go back that long. The solutions have been in traditionally in Low Frequency (LF) band at 125 kHz and High Frequency (HF) band at 13 MHz which was chosen by the Near-Field Communication (NFC) systems. NFC dominated the field for a long while, [21]. The NFC systems cannot use antennas since the wavelength is too large. They have to rely on couplers. The coupler-assisted WPT systems suffer from very limited ranges of operation. Any coupling factor greater than ~0.2 creates adverse detuning effects on the couplers, and any coupling factor less than ~0.01 is practically insufficient for the WPT systems to perform power harvesting. Fig. 1.2, taken from [22], depicts the rapid decline of the mutual coupling factor between a sample pair of NFC couplers versus horizontal and vertical

displacements. The negative coupling factor in Fig. 1.2 corresponds to cases where the receiver captures the magnetic flux from behind.

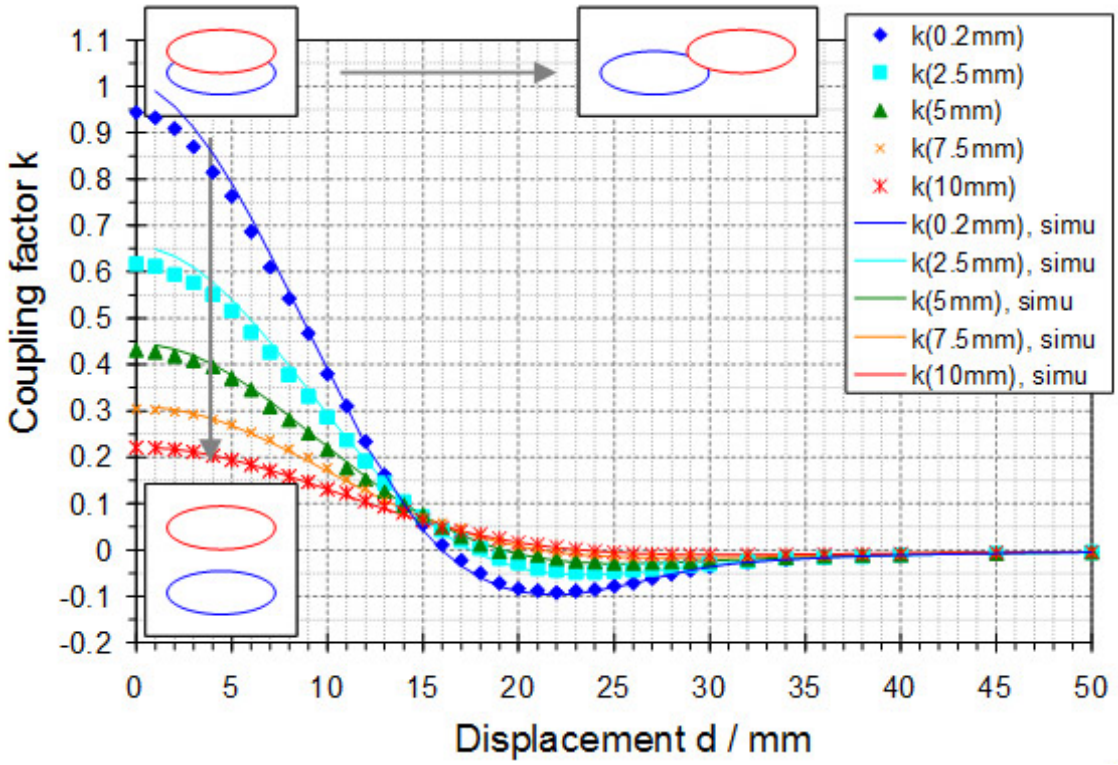


Fig. 1.2 Measured (points) and simulated (lines) coupling factor of two planar coils with 30mm diameters as a function of horizontal displacement while each curve corresponds to one particular vertical distance between the coils.

The UWB band is not a viable candidate to host WPT systems due to very low FCC-imposed limits on the Effective Isotropic Radiated Power (EIRP) and the transmission power levels. The 60 GHz band best suits the wireless power transfer needs of high data-rate contactless applications, which can enjoy the 7GHz available bandwidth that is exclusive to this band. Per the Shannon–Hartley theorem, equation (1), the capacity of the communication channel is proportional to the available bandwidth for the communication. It says

$$C(bps) = BW * \log_2(1 + \frac{S}{N}) \quad (1)$$

in which C is the communication channel capacity (bps), BW is the available bandwidth for the communication (Hz), and S/N is the required signal to noise power ratio of the communication (W/W). This means the 60 GHz band has a remarkable advantage compared to any other band to support high data-rate applications. Whereas the NFC, which is a popular solution for the WPT operation, only supports data rates up to 424 kbps. The tiny size of patch antenna elements at the 60 GHz band makes it possible to have compact antenna arrays with significant array gains. Fig. 1.3 compares the sizes of a typical NFC tag and a 60-GHz 2 × 2 patch antenna array. Another practical disadvantage of the magnetic coils is that they are shorted in the presence of metals, like the ones behind the battery or by the screen of cellular phones; whereas the RF antennas that already have ground planes on their back sides are not affected at such conditions.

Fig. 1.3 The back and front sides of an NFC tag which is 6 cm × 4 cm versus a 60 GHz 2 × 2 microstrip patch antenna array with an area of 6.6 mm × 6 mm.

Comparing a pair of typical NFC coupler with a pair of simple 60-GHz 2 × 2 microstrip patch antenna array indicates two findings. For the same amount of gain the NFC coupler needs 24 times larger area and for the same area the NFC tag would have 1/8 of the range. The acceptable range for the coupling factor for a coupler, e.g. NFC coupler, is very limited. Any coupling factor

less than 0.02 is too little to create a reliable link and any coupling factor more than 0.1 creates detuning effect on the tag. The alignment and orientation also can be very important for a coupler to establish a proper link. The fact that the coupler gain drastically decreases adjacent to metal plates which are found in abundance in the handheld devices is another limitation of the coupler-assisted wireless power transfer technologies. But so far, NFC is the most popular way that the wireless power transfer is done, even for the technologies in SHF band like Bluetooth and WiFi NFC is borrowed as the means for wireless power transfer, while the data transfer is done independently.

As shown by the summary in Table 1.1, the millimeter-wave band is superior to all other alternative bands in its capacity to host WPT systems, due to advantages in size, FCC transmission power limit, and the offered available bandwidth to the prospective employing applications. In upper UHF and lower SHF bands half-wavelength patch antenna elements are impractically large. For frequencies lower than UHF, including HF that hosts NFC, the reactive distance of $\lambda / 2\pi$ or $0.159\ \lambda$ covers the entire close-proximity range; therefore, the couplers are the only possible solutions [23].

TABLE 1.1
COMPARISON OF DIFFERENT BAND OF FREQUENCY

System	Band Name	Frequency (GHz)	λ (cm)	FCC P_{out} Limit (dBm)	FCC Peak EIRP Limit (dBm)	BW (MHz)	Data Rate (Mbps)	Remarks
NFC	HF	0.013	2200	N/A	N/A (Reactive)	1.8	0.106-0.424	Using Couplers (within $\lambda/2\pi$ range)
RFID	UHF	0.9	33	30	36 (Radiative)	26	0.04-0.424	Electro-magnetically Short Antennas
Bluetooth BDR, EDR, HS	RF (UHF)	2.4	12	30	36	1	1, 3, 24	Using NFC for Energy Transfer
WiFi Direct	RF (UHF/ SHF)	2.4 5.8	5 12	30	36	40	108 … 300	Using NFC for Energy Transfer
UWB	RF (SHF)	3.1 ... 10.6	2.8 … 10	-14.3	-14.3	500	675	In EU was limited to 6-8.5GHz in 2010
This work 60 GHz	mm-Wave (EHF)	57-64	0.5	27	43	7000	-	Average EIRP (40 dBm)

Chapter 2

MILLIMETER-WAVE INTEGRATED CIRCUITS

The design of integrated circuits in mm-wave frequencies requires special considerations. Not only the architectures and topologies of the blocks and systems, but also all passive and active devices should be carefully designed, floor-planned, laid out, and implemented [24]. The capacitive, inductive, and resistive parasitics of all components which cause detuning, excessive loss, higher noise and nonlinearity, and chance of unstability and quasi-stability. Narrow-band and wide-band modeling of the devices is a challenging job in mm-wave frequencies too. In order to have more predictable designs, it is best to use test-chips to use the device models based on the measured data. In order to best implement that the active devices use unit-cells. The passive components also can be treated the same way. Although if the simulation setup and the technology files are carefully done the simulations with HFSS creates decent models. For the sake of convergence of the transient simulations lumped models can be used. But in order to effectively create the lumped models the components of the model have to be chosen properly and as close as possible to physical components. In this chapter we review all the designs prior to the final design of the wireless power transfer system. These designs led to the way to the final design of the WPT system. There were five major test-chip tapeouts: 1) for different types of the VCOs in 65 nm digital CMOS technology, 2) for different unit-cells and passive and active components in 40-nm

digital CMOS technology, 3) for different quadrature VCOs in 40-nm digital CMOS technology, 4) for different power amplifiers in 40-nm digital CMOS technology, and 5) for different rectifiers in 40-nm digital CMOS technology.

2.1 A Switched-Capacitor mm-Wave VCO in 65-nm Digital CMOS

The first tape-out was related to the VCOs in 65 nm digital CMOS technology f_{max} of 200 GHz and f_T of 140 GHz. Fig. 2.1.1 shows the schematic diagram and the micrograph of the VCO and VCO buffer for a frequency range of 34.29 to 39.88 GHz frequency. The results were published in RFIC conference in 2010, [24]. Fig. 2.1.1 shows the micrograph of the 0.15 mm2 VCO, including the differential inductor and the transformer along with their guard rings. The DC pads on the top are to supply ground, power, and the control signals. The produced power of the output of the VCO buffer at 34 GHz is 0 dBm delivered to 100-Ω differential loading of the VCO buffer. The phase noise of the VCO is measured -98.1 dBc/Hz at 1 MHz offset frequency at maximum frequency. The tuning range is 15.1%. The current consumption is 12 mA from a 1.2 V supply voltage. The power consumption is 14.4 mW, FOM of -178.5 dB, and FOM_T accordingly is -182.1 dB. The analog tuning can be used to do FM modulation in the transmitter. The analog tuning is done by using accumulation varactors and the maximum K_{VCO} is 240 MHz/V. There are 5 bits of switched capacitor digital frequency tuning. The output power and the efficiency in generating power are the most important features of the VCOs for wireless power transfer, but for the sake of comparison the phase noise and Figure of Merit (FOM) of this VCO are reported. The

phase noise had the following relation with the circuit parameters and the FOM and FOM_T are defined as shown in (2), (3), and (4).

$$L\{\Delta f\} = 10\log\left[\frac{F.k.T}{2P_s} \cdot \left(\frac{f_0}{2Q_T.\Delta f}\right)^2 \cdot \left(1+\frac{f_c}{\Delta f}\right)\right] \quad (2)$$

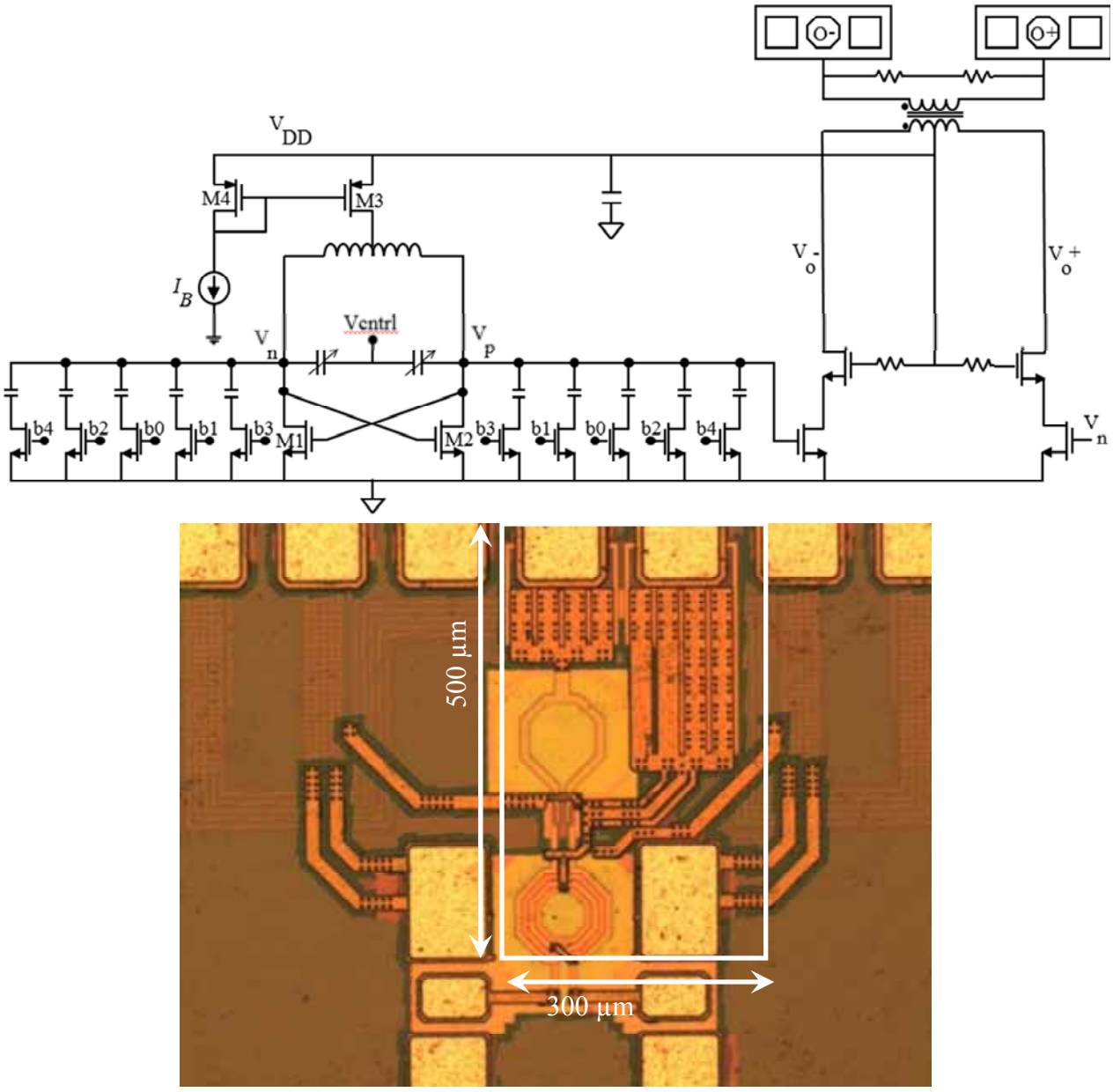


Fig. 2.1.1 The schematic diagram and the micrograph of the 34-40 GHz VCO in 65 nm digital CMOS.

$$FOM(\Delta f) = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \tag{3}$$

$$FOM_T(\Delta f) = FOM(\Delta f) - 20\log\left(\frac{TR}{10}\right) \tag{4}$$

Fig. 2.1.2 displays the results of the phase noise measurement of the free-running VCO at the highest oscillation frequency and the output signal at the lowest oscillation frequency on a

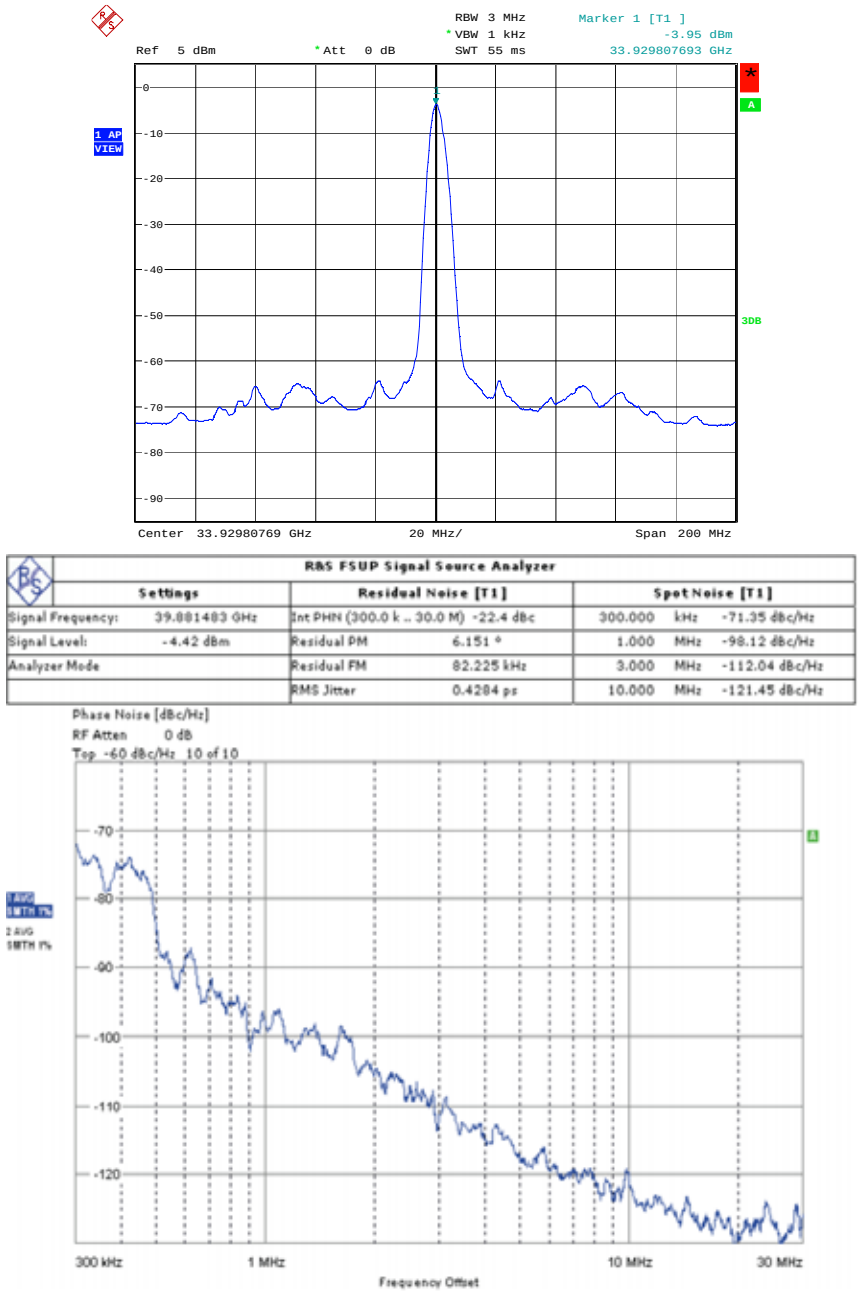


Fig. 2.1.2 The measured output power and phase noise results of the 34-40 GHz VCO in 65 nm digital CMOS.

Rohde & Schwarz 67-GHz Spectrum Analyzer (FSU).

The high level of integration creates the possibility of realizing "*DC-Boards"* on which interconnections are limited to pure DC routings and their high speed data buses are replaced by chip to chip wireless links, resulting in significant cost and power savings. This work is part of a project with an aim of evaluating the feasibility of small, low power, and high performance mm-wave transceivers in pure digital CMOS technology. As indicated in (2), phase noise of the VCO degrades 6 dB/octave as the oscillation frequency increases [45-46]. At frequencies > 20 GHz non-quasi-static effects for the capacitors and the skin and the proximity effects for the inductors severely degrade their quality factors and pose significant challenges to the design of the VCO [47]. Using only varactors to achieve a large tuning range for the VCO results in a high K_{VCO} which as (5) indicates increases the *AM* to *PM* conversion gain which in turn causes high phase noise and spurious signal levels. In this work using the switched-capacitors has helped in reducing the K_{VCO} and increasing the tuning range significantly. In (5) Φ_{PM} is the level of the *PM* signal at the output of the VCO oscillating at the frequency of f_0, in response to an *AM* disturbance voltage with amplitude of V_{AM} and frequency of f_{AM}.

$$\Phi_{PM}(f_0 + f_{AM}) = \left[\frac{K_{VCO}}{2f_{AM}}\right] \cdot V_{AM}(f_{AM}) \tag{5}$$

Doughnut transistors comprised of square-shaped polysilicon gates are used for the VCO cross-coupled pair. This reduces the contribution of the drain junction capacitors to less than 5% of the overall tank capacitance. Size selection for the core devices has been done based on four different factors: gain, Noise Figure (NF), current switching capability, and efficient power delivery by providing a proper bias to the VCO buffer. The optimum current density for the lowest NF depends on the lateral electric field in the channel [48]. For the process of this VCO, a current

density of 0.35 mA/μm results in a suitable performance from all of the mentioned aspects. Fig. 2.1.3 shows the unit cell of the VCO core with an optimal layout. The layout of the transistors should be optimized in order to achieve an optimal performance in terms of fmax, maximum stable gain, and the noise figure. Wider routings cause larger parasitic capacitances and couplings, while narrower interconnections create larger series resistances and inductances.

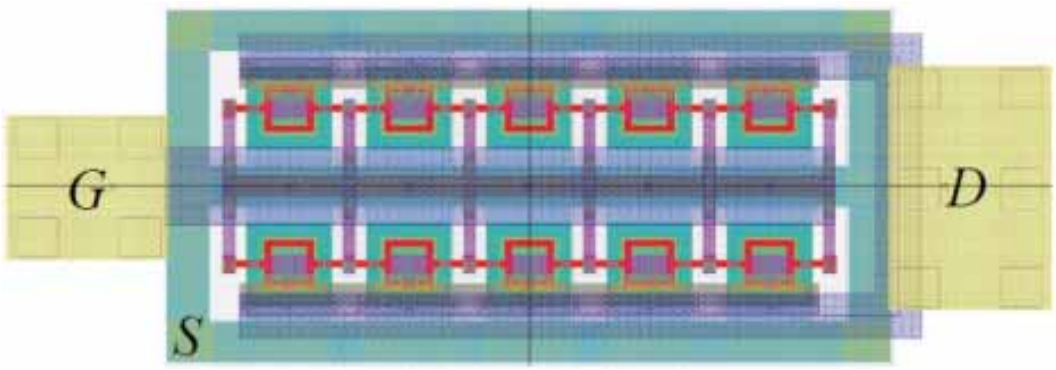


Fig. 2.1.3 Layout of the unit-cell for doughnut-shaped transistors for the devices of the VCO core.

The resonant tank is composed of a 135 pH differential octagonal-shaped inductor, accumulation-mode varactors and 5-bit binary-weighted switched finger-capacitors. The inductor uses a wall of well-grounded metals to provide a good current return-path and help confinement of the field, at the price of more parasitic capacitance and a little lower overall inductance. To reduce the losses due to the eddy currents, any substrate doping under the inductor and any metal loops in the guard rings and the routings have been avoided. The differential inductor has a quality factor of 24 at 34 GHz and a self-resonance frequency of 200 GHz. The switched capacitor uses doughnut-shaped NMOS switches to achieve a high ON to OFF capacitance ratio. As Fig. 2.1.4 demonstrates the capacitor array benefits from an innovative design in which a large finger capacitor splits to five binary-weighted capacitors to be used for the digital frequency tuning. The LSB units are positioned in between the MSB units in order to achieve a better accuracy. Conventional unit-cell based arrays suffer from significant relative accuracy when used for small

capacitor sizes. The proposed compact layout results in a better accuracy, a lower parasitic capacitance, and shorter connections to the switches. Effective parallel resistance of the tank is dominated by the capacitive branches, resulting in an overall tank quality factor of 10 at 40 GHz.

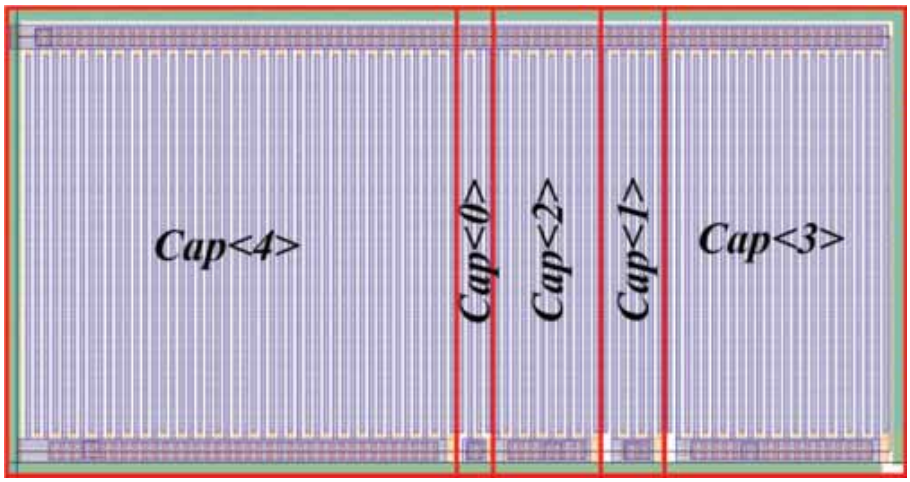


Fig. 2.1.4 Layout of the proposed capacitor array consisting of five binary-weighted capacitors in the optimum order.

The current source is programmable to work in either the linear mode or the saturation mode in order to be able to optimize the overall phase noise. When the current source is in the saturation mode its noise contribution increases, but the contribution of the supply and the cross-coupled pair decrease. In this design, should the current source be set to supply the same amount of current in both modes the linear mode shows a slightly better phase noise.

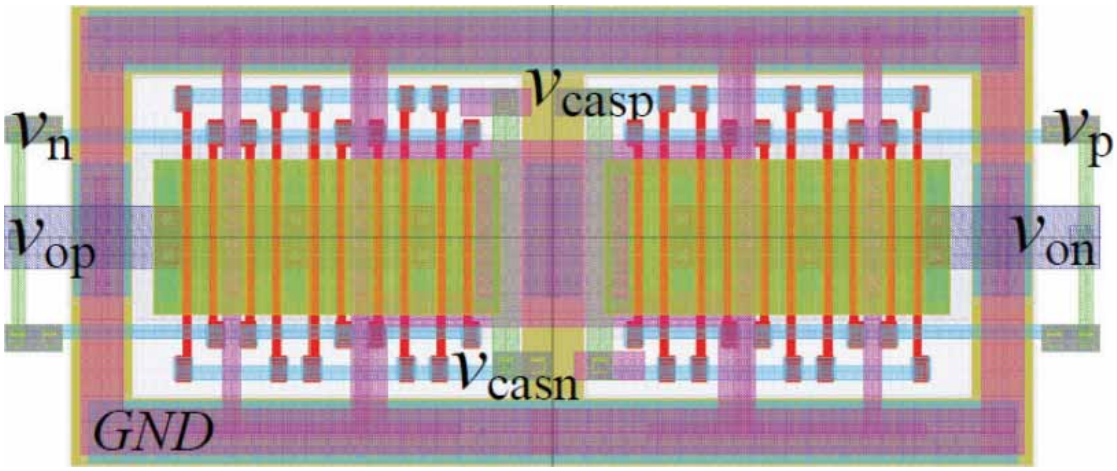


Fig. 2.1.5 The unit cell of the differential VCO buffer with five differential pairs of the cascode devices.

A differential cascode buffer has been designed to deliver a 0 dBm LO power to a 50Ω load while isolating the VCO from the load. The VCO buffer also reduces the load pull for the VCO significantly. The operating points are set for an efficient LO power delivery. As shown in Fig. 2.1.5 the diffusion regions of the input and the cascode devices have been shared to minimize the parasitic capacitances of the junctions and the routings which create significant loss and current leakage at this common node.

A transformer has been used to convert the buffer output impedance of 125 Ω, which is optimum for an efficient power delivery, to a 50 Ω level at the input of the following stages which can be a mixer and a divider. This feature together with the possibility of having shorter signal feeds to the following stages make the transformer superior to a differential inductor as the VCO buffer load. A ground grid covers all the layers of the layout, with the exceptions of the parts which introduce excessive eddy currents or couplings to the sensitive nodes. All Common- Mode (CM) nodes of the circuit have their unnecessary bandwidths suppressed by maintaining low impedance levels to the ground in all frequencies. This requires different sizes of decoupling capacitors to be used at all of the CM nodes and to be repeated in short intervals. This also improves CM noise rejection and CM stability. There are two CM nodes which do not need extra capacitors: The center tab of the inductor and the voltage control node. At the center tab of the inductor higher impedance levels can suppress the noise of the cross-coupled pair. And the voltage control node has to connect to the loop filter when the VCO is employed by a PLL.

The results of the VCO show significant improvements compared to an earlier version of the design which used only varactors. The varactor-only version measured a tuning range of 5.8% and a KVCO of 2.1 GHz/V. Table 2.1.1 presents a summary of the characteristics of this switched-capacitor VCO in comparison with other recently published mm-wave CMOS VCOs [47] and [49-53]. The table reports the worst case results of each work.

TABLE 2.1.1
SUMMARY OF THE SPECIFICATIONS OF THE DESIGN IN COMPARISON WITH RECENTLY PUBLISHED MM-WAVE CMOS VCOS

Reference	Year	Publ.	Process Technology	Freq. (GHz)	Ph.N.@1MHz (dBc/Hz)	Tuning Range%	PDC (mW)	FOM_T (dB)	Pout (dBm)
[47]	2006	RFIC	CMOS 0.18 µm	21.6	-101.7	6.25	45	-171.9	-4.2
[49]	2009	VLSI	CMOS 0.13 µm	47.9	-102.5	1.59	5.6	-172.7	-19
[50]	2009	JSSC	CMOS 90 nm	58.4	-91.0	9.32	8.1	-176.7	-14
[51]	2008	ISSCC	CMOS 90 nm	49.9	-87.0	12	10.4	-172.4	-
[52]	2009	CICC	CMOS 65 nm	60	-97.1	16.7	30	-182.3	-
[53]	2009	IMS	CMOS 90 nm	61	-90.1	9.27	10.6	-174.9	-5
This Work	2010	RFIC	CMOS 65 nm	39.9	-98.1	15.1	14.4	-182.1	0

Probing unlocked high performance mm-wave VCOs for the purpose of phase noise measurements is extremely sensitive to their natural frequency drifts. The range of the frequency drift can exceed the offset frequency range of interest which makes it hard to have reliable low-offset phase noise measurements. Elements like the illuminator's light and mechanical stress or strain are destructive to these measurements. Vibration isolation table, wide probe tips, and wafer probing, as opposed to single die probing, significantly improve the reliability of the measurements. Phase noise analysis mode of Rohde Schwartz FSUP50 has been used to measure this design. There are some settings which are vitally important. In the measurement setup, manual setting with a RBW of 0.1% increases the chance of success. Tracking and verifying the level and the frequency as well as the AFC should be turned off as they are not designed for unlocked VCOs. A combination of mechanical stability of the setup, quiet environment, and proper instrument settings can make low-offset phase noise measurements of the mm-wave VCOs reliable.

Chapter 3

ANTENNA ADVANTAGE, ANTENNA DESIGN

The Friis transmission equation, (6) says

$$\frac{P_r}{P_{t_E}} = G_t \frac{\lambda^2}{(4\pi R)^2} G_r \tag{6}$$

where P_r is the available power at the receiver (W), P_{t_E} is the available power to each of the transmitter elements (W), G_t is the transmit antenna gain (W/W), G_r is the receiver antenna gain (W/W), λ is the free space wavelength, and R is the distance between the TX and the RX antennas (m). This equation is used to perform the link budget analysis for the WPT systems. It determines the lowest level of power that needs to be delivered to each of the transmitter elements (PtE) in order to ensure that the minimum level of available power at the receiver (Pr) to reach the targeted range of the system is met. The fact that the path loss is proportional to frequency squared is a potential deterrent for adopting higher frequencies for the WPT systems. However, as (7) indicates

$$G_{t/r} = \frac{4\pi A_{t/r}}{\lambda^2} \tag{7}$$

where $G_{t/r}$ is the TX or RX antenna array gain (W/W), $A_{t/r}$ is the TX or RX antenna aperture (m^2), λ is the free space wavelength (m), the RX antenna gain (Gr) and the TX antenna gain (Gt) are proportional to frequency squared [57]. As a result, the right side of the equation (6) is proportional to frequency squared and the product of the apertures of the TX and RX antennas. Integration of the antenna with the transmitter and the energy harvester is the most advantageous feature of the 60-GHz wireless power transfer systems. Antennas can integrate on the same substrate or on package.

The antenna gains and the radiation patterns that we discuss in this chapter are all in the far-field when the beam is fully shaped. The near-filed effects are more case dependent and has to be simulated for the entire range to make sure there is no null of dip in the gain. In the designs that are mention here this is what we witnessed in the simulations and the measurements.

3.1 Microstrip Patch Antenna Design

To show possibility of realizing high gain antennas in mm-wave bands in small footprints, we start with patch antennas. Fig. 3.1.1 displays the layout of the TX and RX antennas, which are designed on a 200-um thick Rogers Duroid/RT 5880 dielectric package with a permittivity of 2.2 and a loss tangent of 0.0009. The RX antenna is a single 1.53 mm × 1.69 mm patch antenna element on a 3.1 mm × 3.7 mm package with a simulated gain of 7.85 dBi. The RX antenna dimensions have been optimized such that the antenna has a center frequency of 60 GHz and a bandwidth of

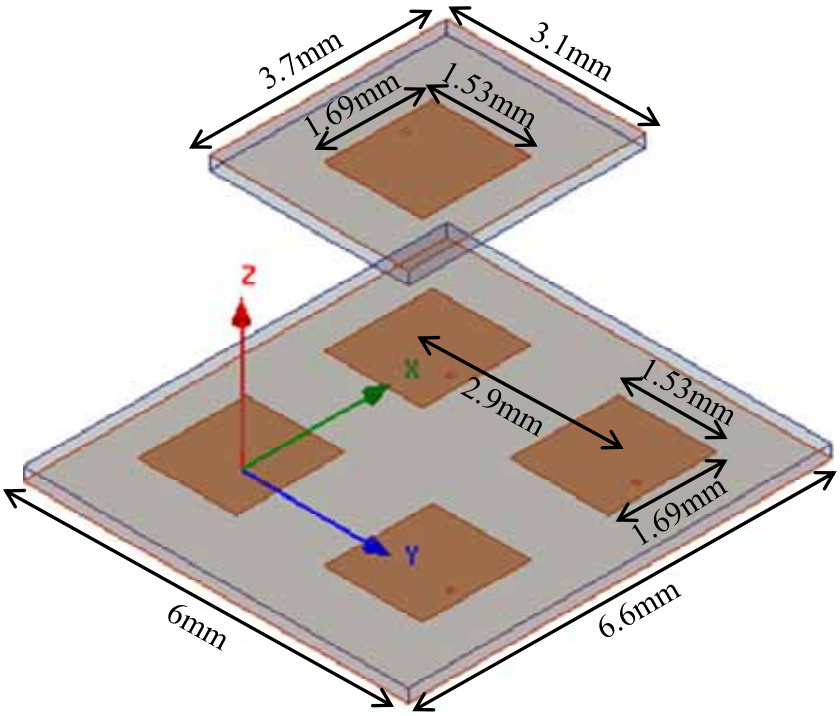


Fig. 3.1.1 The simulation setup of the coupling between RX and TX patch antenna arrays.

~2.5 GHz. The TX antenna is a 2 × 2 patch array with the same element size as the RX element which are placed on a 6 mm × 6.6 mm package with a pitch separation of 2.9 mm in both horizontal and vertical directions. The TX antenna has been optimized for maximum directivity at broadside when all elements are fed in-phased signals. The maximum simulated array gain at broadside is 12.5 dBi. Considering the aperture of the antennas, the gains of the RX and TX antenna are very competitive. The simulated 3-D radiation pattern, gain, and the S_{11} of the 60-GHz patch antenna

element based on simulation is shown in Fig. 3.1.2 and those of the 2 × 2 TX patch antenna array are depicted in Fig. 3.1.3. For 2 × 2 patch antenna array we can steer the beam by changing the polarity of the outputs of different elements with respect to each other. Fig. 3.1.3 carries the simulation results with four in-phased inputs.

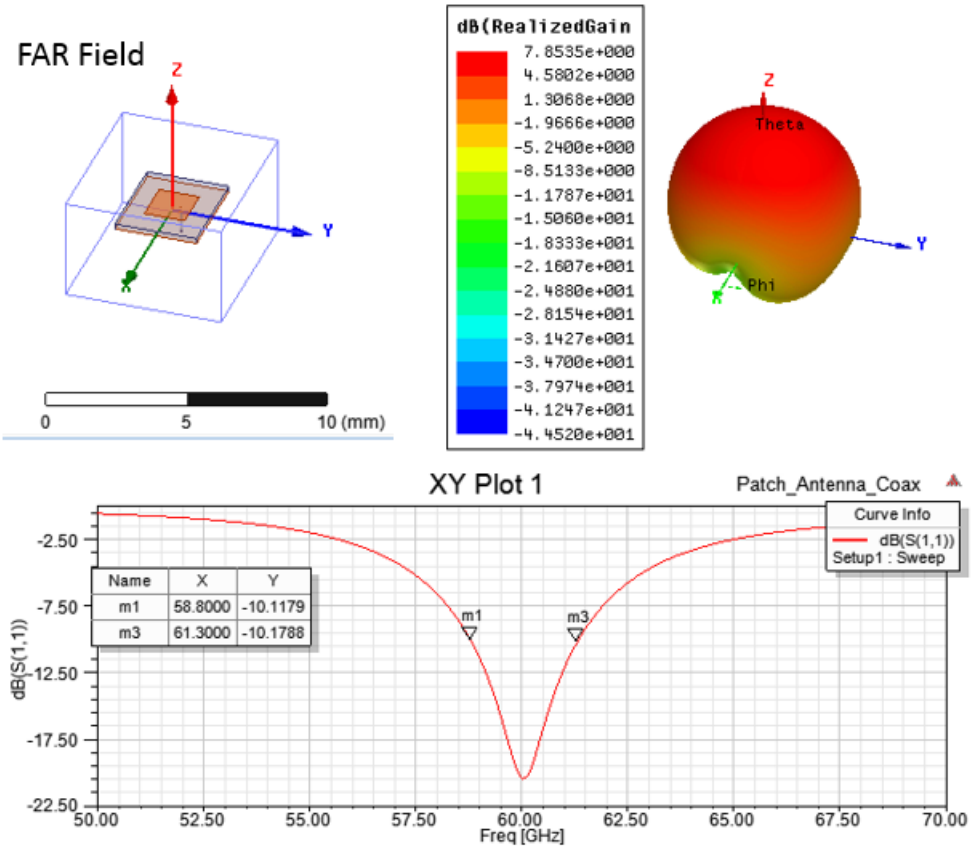


Fig. 3.1.2 The simulation setup, the 3-D far-field radiation pattern, and the S_{11} of the 60-GHz patch antenna element.

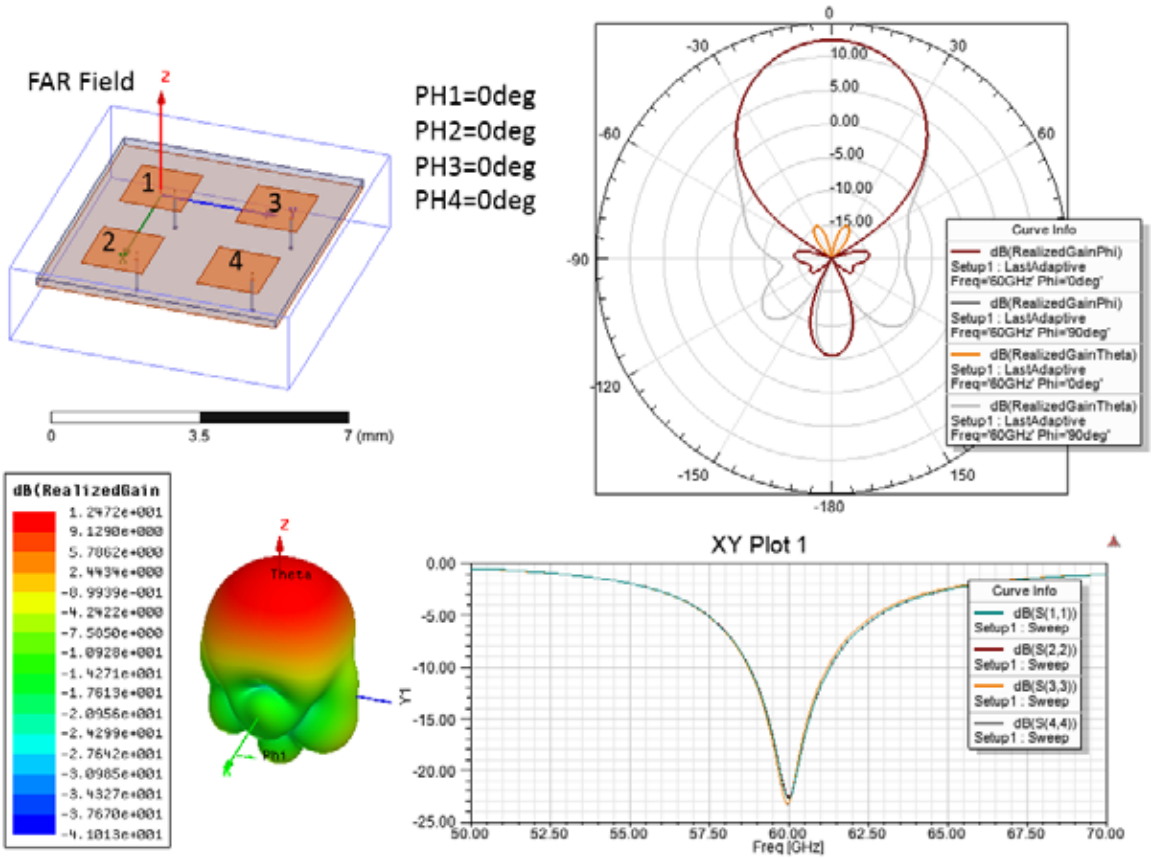


Fig. 3.1.3 The simulation setup, the 3-D radiation pattern, and the S_{11} of the 60-GHz 2 × 2 patch antenna array with in-phased inputs.

Fig. 3.1.4 displays the results of the EM simulations for the 2 × 2 patch antenna array for the case that elements 1 and 3 are out of phased with elements 2 and 4. There is a beam steering range of 70° just by changing the polarity of the inputs in the fashion that was mentioned. This means if the transmitter can support outputs that can change polarity compared to each other we can steer the beam considerably without much of front-end complexity and phase shifting challenges. Equation (7) indicates that the gain of the antenna array for a given frequency is proportional to the area of the antenna. Considering that the dimensions of the antenna elements are proportional to the wavelength of the signal, we can say that for a given footprint the gain of the antenna array is proportional to the frequency of the input frequency. We should mention that

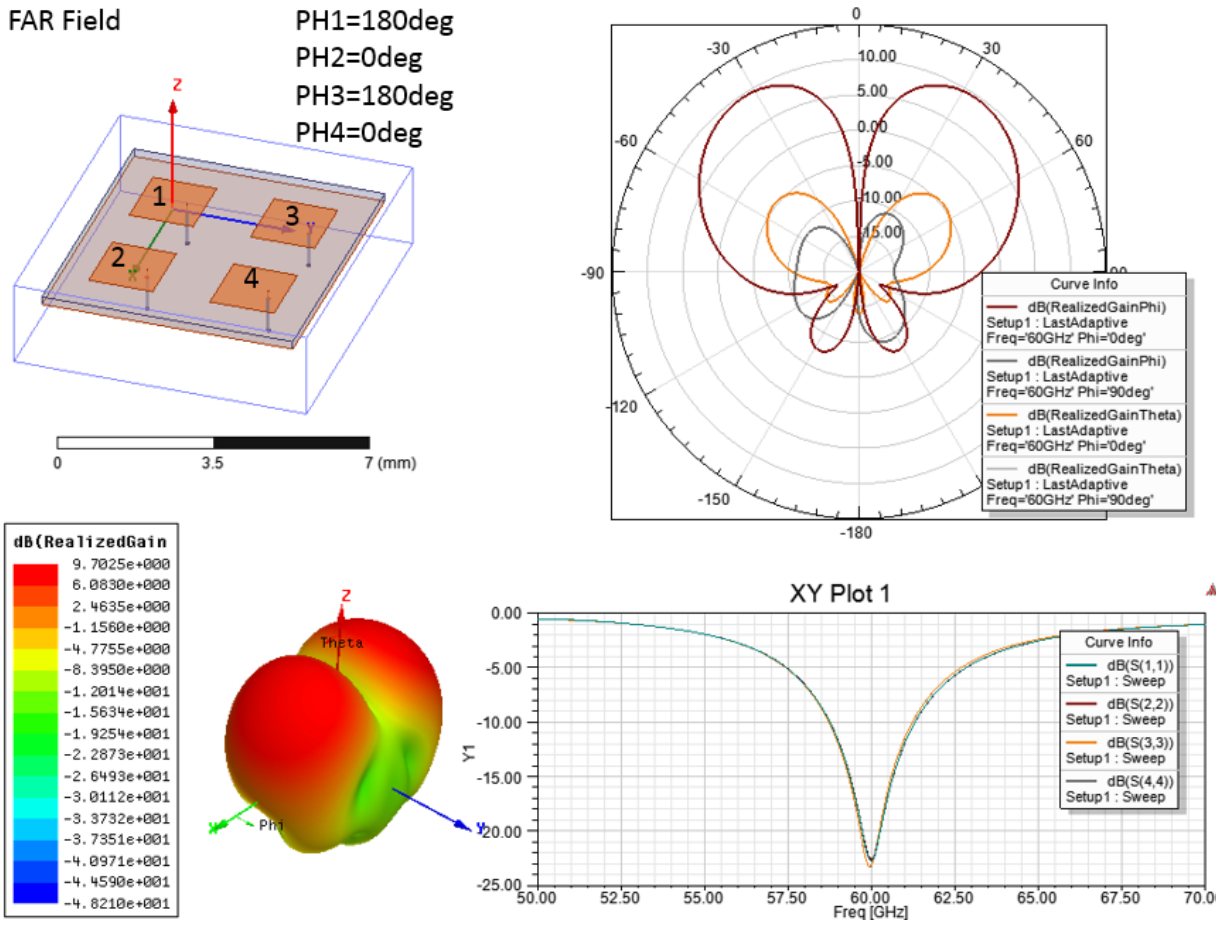


Fig. 3.1.4 The simulation setup, the 3-D radiation pattern, and the S_{11} of the 60-GHz 2 × 2 patch antenna array with out-of-phased inputs for elements 1 and 3 compared to elements 2 and 4.

this gain requires equal input powers to each of the patch antenna elements. In practice, the theoretical advantage of employing higher frequency bands on the right side of (6) may not be fully realized, especially in arrays with many elements due to high routing losses. In addition, empirical data from published PA designs in different frequencies suggest that the highest achievable P_{tE} level for a typical PA can be assumed inversely proportional to its frequency. Fig. 3.1.5 illustrate how the available input power of the receiver is related to the frequency of the transmitted output power. Based on the final equation in Fig. 3.1.5, there is an advantage to use higher frequencies for the wireless power transfer for a given size of the antenna. Assuming that the size of the antenna for a small smart device is determined based on the constraint of the

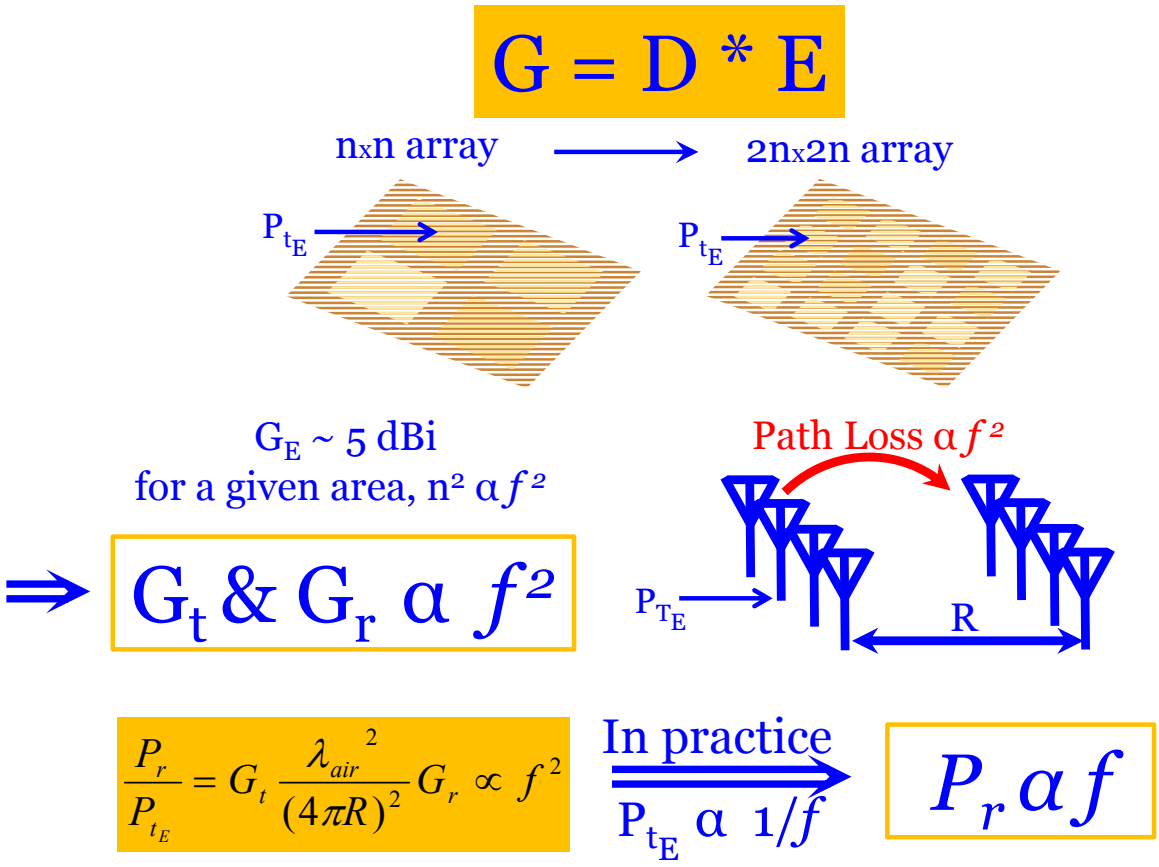


Fig. 3.1.5 Deriving the relationship between the available power at the receiver input versus the input frequency.

application, this means using 60 GHz ISM band can help us reach farther distances compared to lower frequencies. In practice the efficiency of the energy harvester at the RX side to convert RF input power to DC can reduce for higher frequencies which would affect the power rate of storing energy at the energy harvester of the receiver.

Fig. 3.1.6 shows the simulated available power level at the input of the RX antenna with respect to its distance to the TX antenna when the four TX antenna elements are fed with in-phased signals with a P_{tE} = 18.6 dBm. This is the measured power level produced by each of the four PA cores of this 60 GHz system which will be discussed in Chapter 5. The results of the calculated amount for the available power at the receiver, based on the Friis far-field path-loss equation are

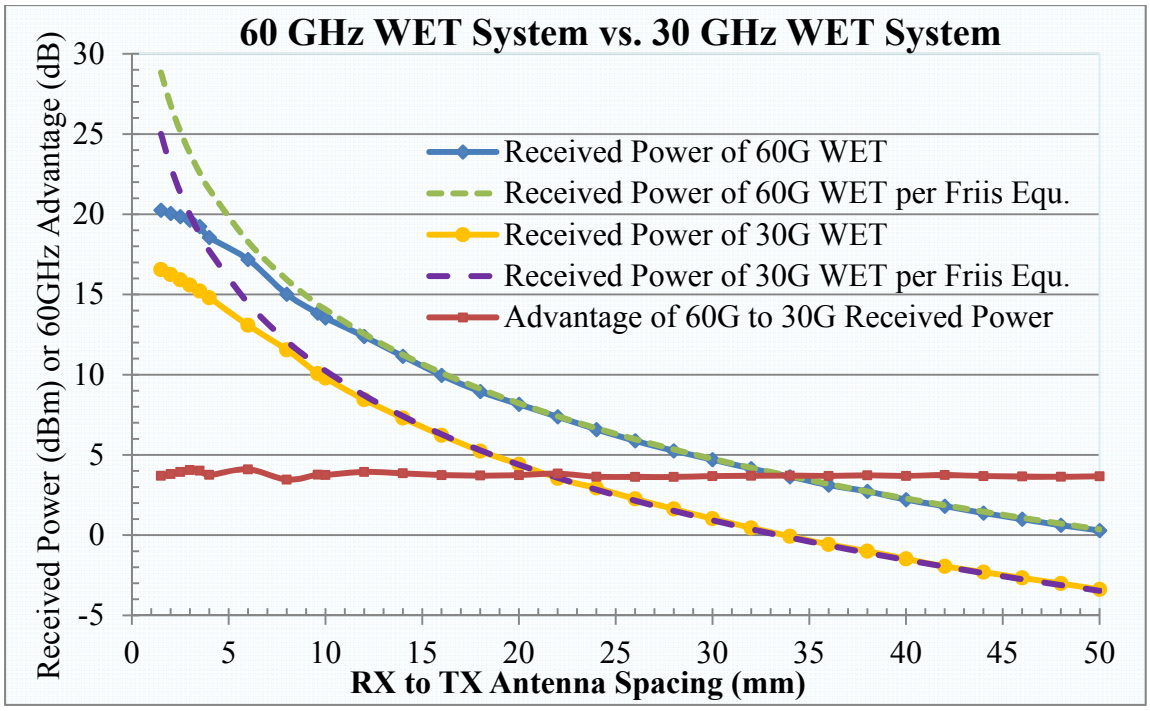


Fig. 3.1.6 Comparison between the received powers of 30G and 60G WPT sets.

also shown in Fig. 3.1.6. The distance above which the simulation curve overlays the Friis calculated curve indicates the border of the far-field region. To verify the second-order proportionality of the right side of equation (6) with respect to frequency, for given effective areas of the TX and RX antennas, the simulation results of a sample set of 30 GHz RX and TX antennas are also shown in Fig. 3.1.6. The comparison reveals that for the same total TX power and RX to TX distance, the 60 GHz antenna set transfers 3.7 dB more power from its TX antenna to its RX antenna, compared with what the 30 GHz set does. This proves that some part of the theoretical advantage in using 60 GHz band for this WPT system has been realized. But we should realize that the required total input power is 6 dB higher in the case of the 60 GHz 2 × 2 patch antenna array than the 30 GHz patch antenna element. The designated areas of the TX and RX antennas for this 60 GHz system do not fit any patch antenna element for frequencies less than 30 GHz. This limits the range of frequencies of the antenna sets to which this 60 GHz set can be compared. Fig. 3.1.6 also indicates that the received signal in the near-field does not have any nulls or dips.

In near field the power drops less with respect to distance compared to what the extension of Friis far-field path-loss equation in the near-field region predicts. There is no practical penalty in using this 60 GHz WPT solution in close-proximity ranges. The antenna gains have a second order dependency to the frequency for specific areas for the RX and TX antennas. The free-space path loss has an inverse squared relation with the frequency. Empirical study shows that the TX power delivery is proportional to inverse of the frequency. As a result of the aforementioned relationships the overall available power at the receiver has a proportional relation with the frequency. It means that it is advantageous to increase the frequency in order to produce higher power at the receiver input. Fig. 3.1.7 indicates the bandwidth of the transfer function of the power transfer from the TC to the RX for different distances between the two antennas.

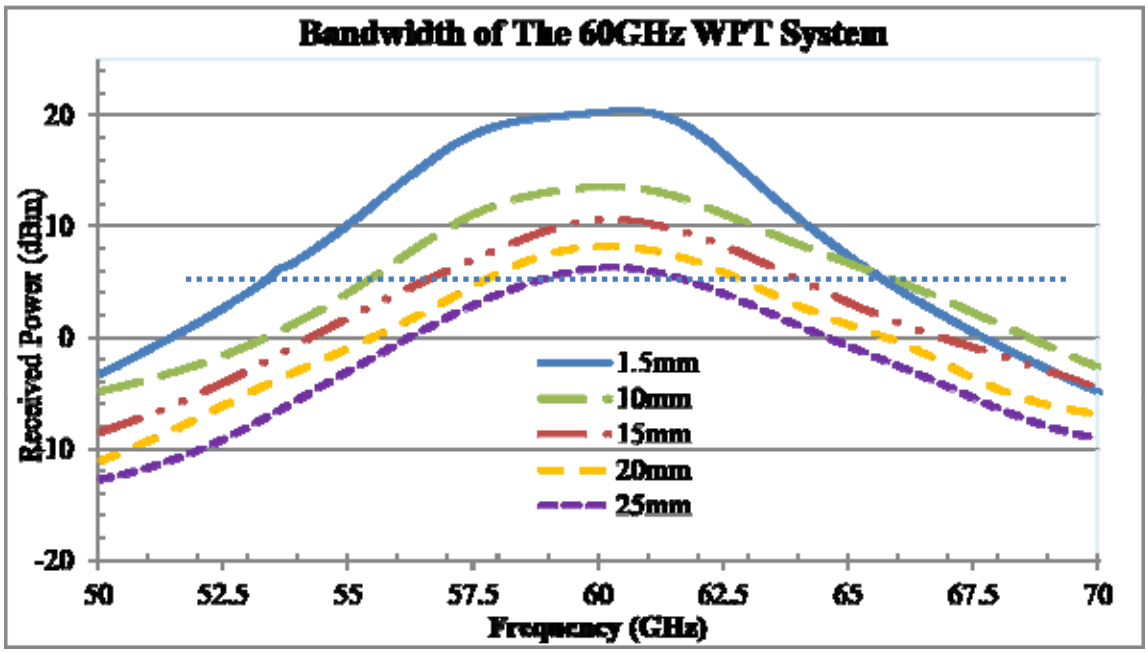
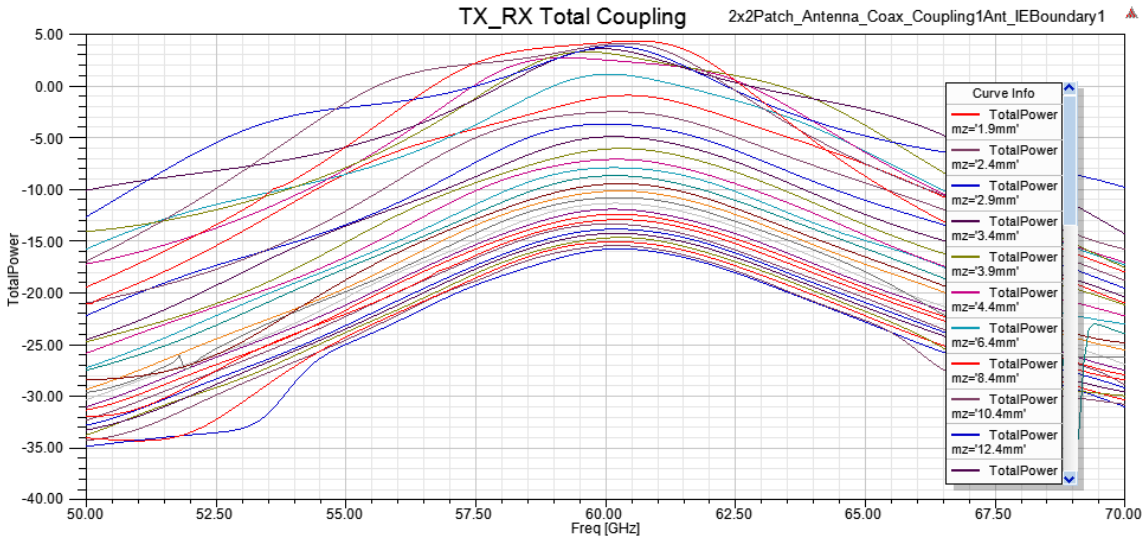


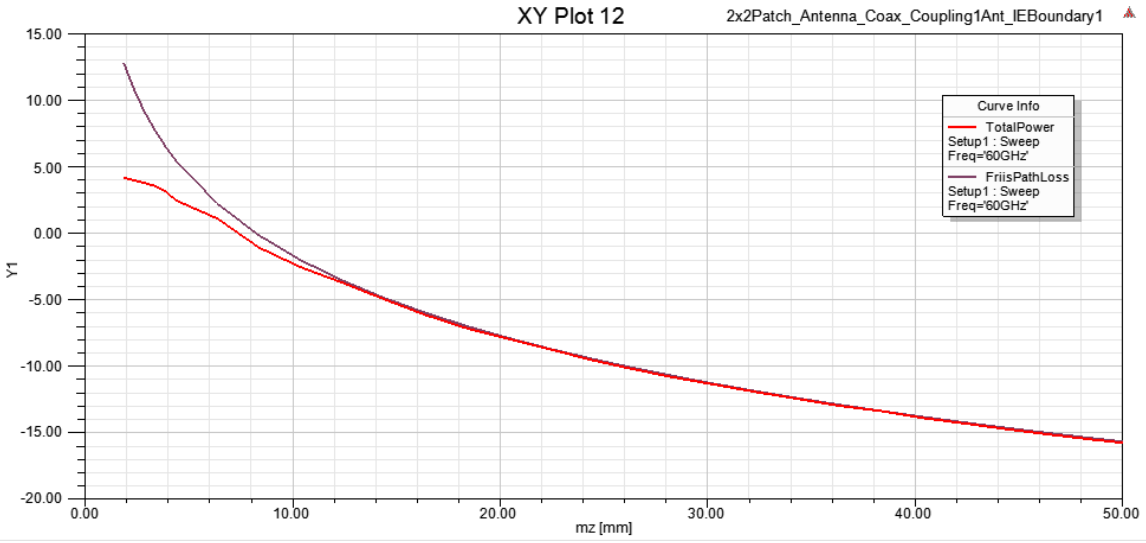
Fig. 3.1.7 The frequency behavior of this WPT system for different ranges.

Fig 3.1.8 (a) demonstrates the relation between the available power at the receiver input and the input frequency for a given aperture of the antenna over the input power of each of the antenna elements of the 60 GHz 2 × 2 patch antenna array. The bandwidth of the transfer function

for the coupling between the TX and RX antennas is in the order of 5 to 7 GHz. Fig. 3.1.8 (b) shows the available input power with respect to the distance between the two antennas. The results of the Friis transmission equation is also depicted in this figure as a result we can identify the border between the near-field and far-field regions of the radiation for the 60 GHz 2 × 2 patch antenna array of the TX. That is the distance in which the simulated available power at the receiver input and the calculated amount based on the Friis Transmission Equation diverge. For this case, this distance is 12.5 mm. The range of operation for the close-proximity WPT system is 40 mm.



(a)



(b)

Fig. 3.1.8 The Coupling between single patch antenna and a 2 × 2 patch array antenna vs. frequency and distance.

Fig. 3.1.9 shows the fabricated version of the 8 × 8 and 4 × 4 microstrip patch antenna arrays and a single patch antenna with the power harvesting chips connected to them.

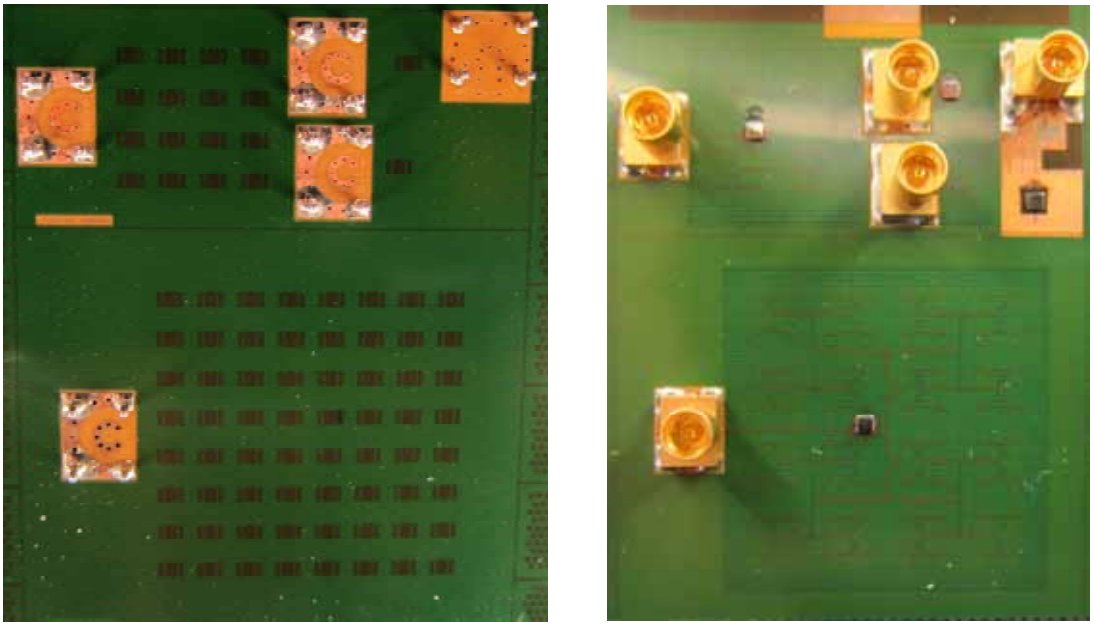


Fig. 3.1.9 The back and front sides of the fabricated 8 × 8 and 4 × 4 microstrip patch antenna arrays and the single patch antenna with the power harvesting chips connected to them.

3.2 Grid Array Antenna Design

Grid array antennas are a proper choice for the systems which operate in the close-proximity ranges and near-field region. In order to make the design phase of the grid antenna quicker, we came up with a semi-analytical model for the antenna in order to obtain the grid array radiation pattern without doing a full wave simulation of the whole structure with minimal computation power requirements. The approach is to divide the array into repeatable smaller structures that can be separately simulated using a full wave simulation tool (HFSS). In order to do that we compose the grid array by uniting the previous pieces and measure current and voltage at each interconnection node using the Designer tool. Then the radiation pattern can be computed using Matlab.

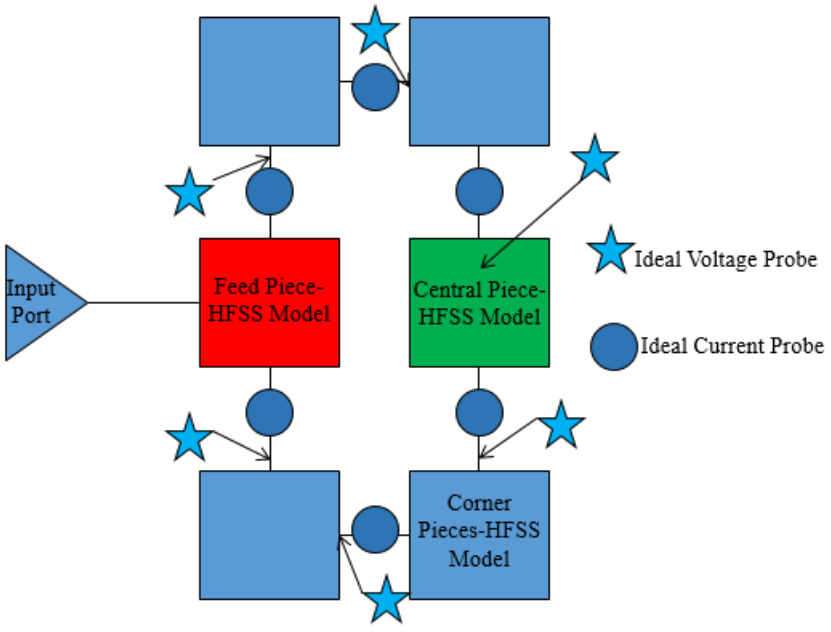


Fig. 3.2.1 Single-loop example for semi-analytical modeling of grid array antennas.

For more complicated grid antennas the model can help to make the simulation much quicker. Here is an example of how the simulation setup in Designer and HFSS look for a 60-GHz grid array antenna.

Pieces to simulate in HFSS. Then import S-parameters to Designer and unite pieces by ideal lossless wires to get the same mesh structure.

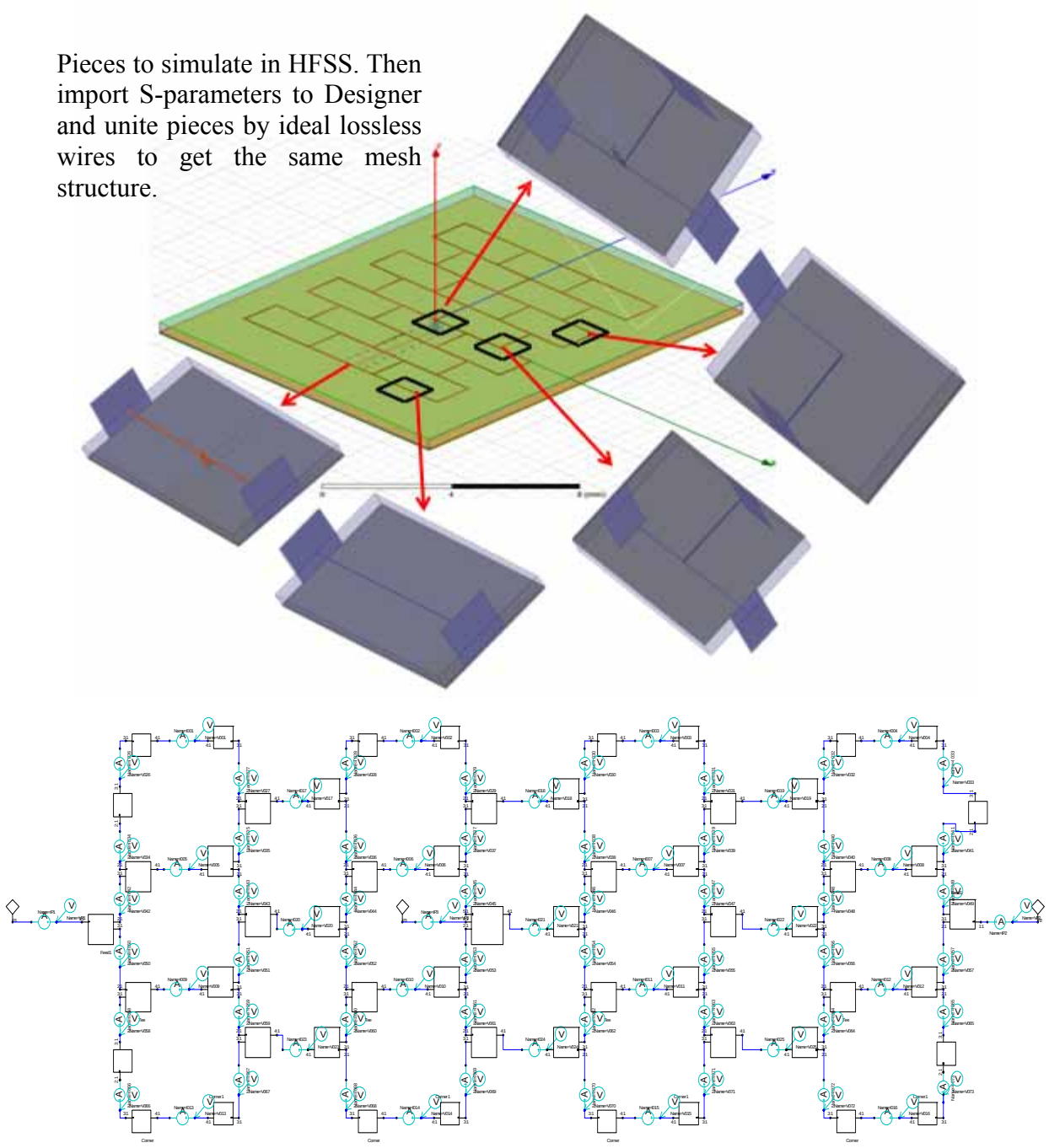


Fig. 3.2.2 Multi-loop example for semi-analytical piece-wise modeling of grid array antennas.

In order to decide on the design of the transmitter array, we need to analyze various transmitter configurations and the antenna implementations. The analysis should be based on directivity, scanning capability, system complexity, and the aperture. The options to consider are

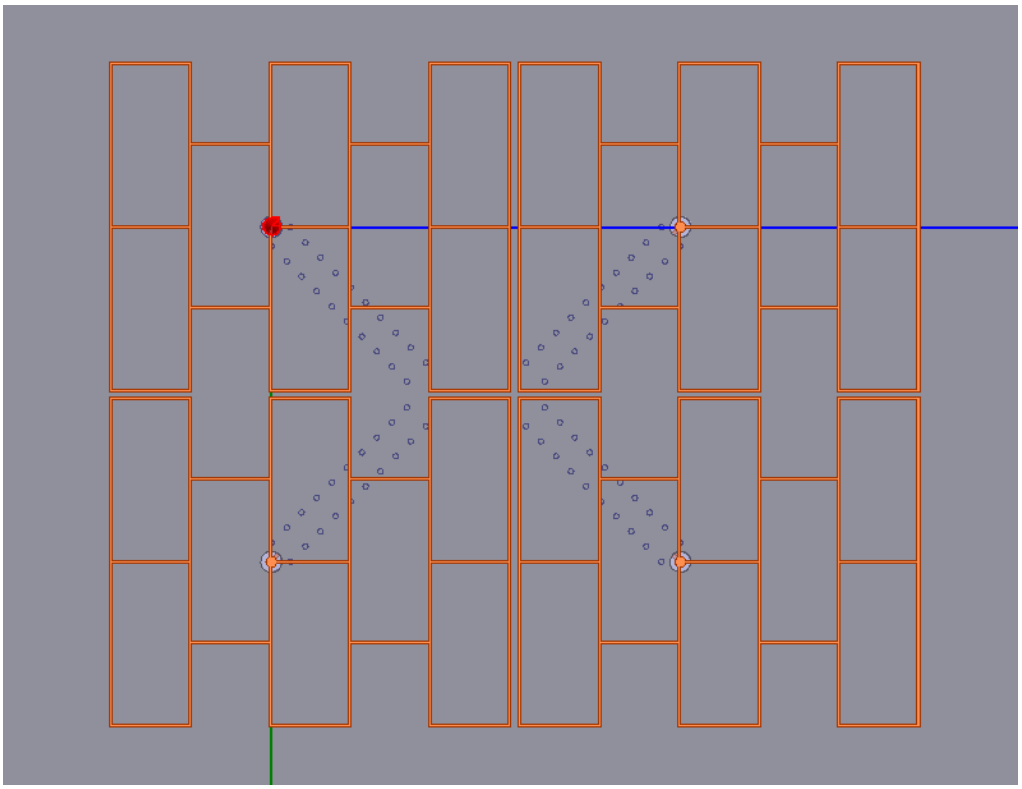


Fig. 3.2.3 A 2 × 2 grid antenna array with four independent feeds.

how many transmitter and receiver chains to be used in parallel and how to combine them. We tested three types of grid array antennas that could be beneficial: broadside grid antenna, 2 ×2 grid array antenna with a combiner at the input, and 2 × 2 grid antenna array with four independent feeds, among which the last option is displayed in Fig. 3.2.3. The best way to produce high power transmitters without violating the voltage reliability limits is to combine the power over the air. As a results the preferred antenna for the TX is an n × n array antenna. But since the ranges that is being targeted is around 4 cm and the separation of the two antennas of the TX and RX is mostly in the near-field region a 2 × 2 antenna array whose dimensions are comparable to the separation of the two antennas seems to be the best choice. On the RX side the antennas are combined with the rectifiers which convert the RF power to DC storable power. The result of such a combination is called a rectenna. The best way to operate in the RX side is to have as many as rectennas in

parallel without any interaction in the RF domain. The DC output power of each of them can be stored on the same or independent storage capacitors or batteries.

Fig. 3.2.4 shows the variation of the radiation pattern from the far-field to the near field. The level that the gain starts to reduce and the field seems not fully formed is 10 mm range. The smaller gain of the antenna in the near-filed does not necessarily mean less power at the rectenna input, since the area that is going to be exposed to the input power is larger although the phase of the intercepted signal could vary from side to side of the antenna. As a result coupling simulations should be done for different ranges in order to know the exact power at the input of the rectenna.

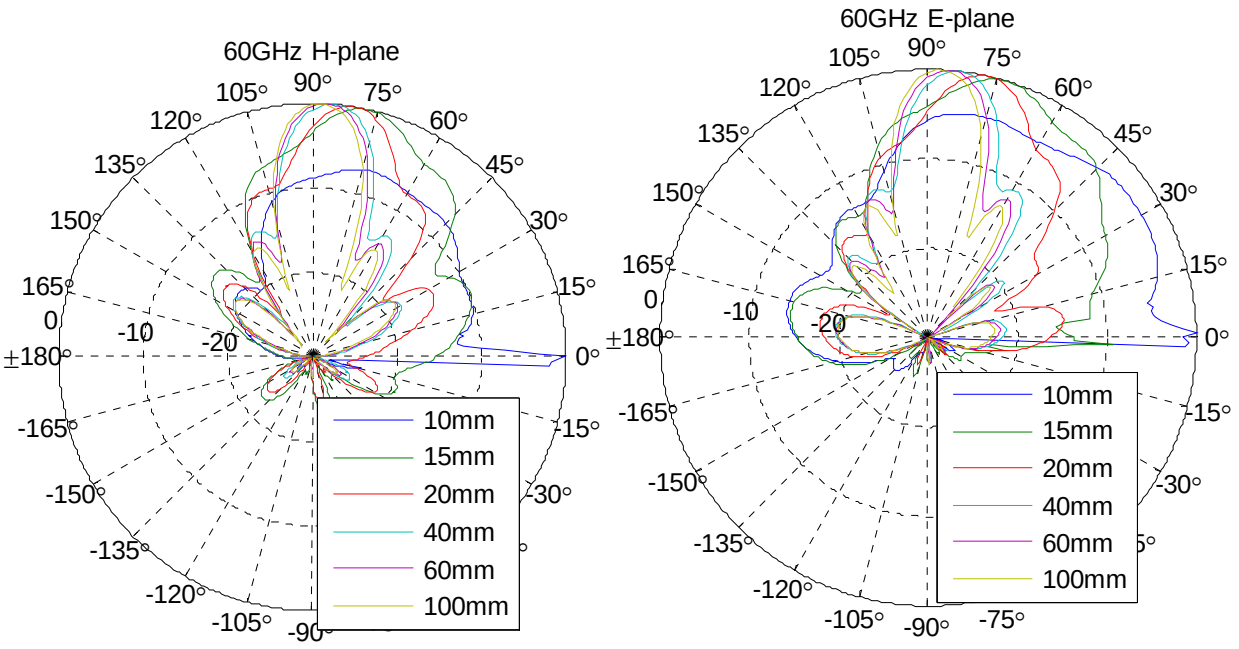
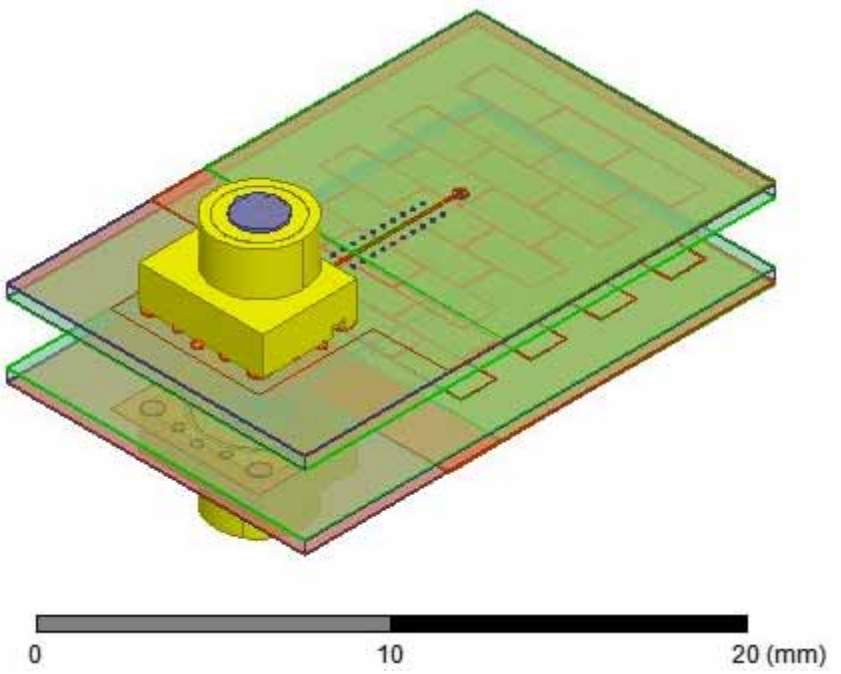
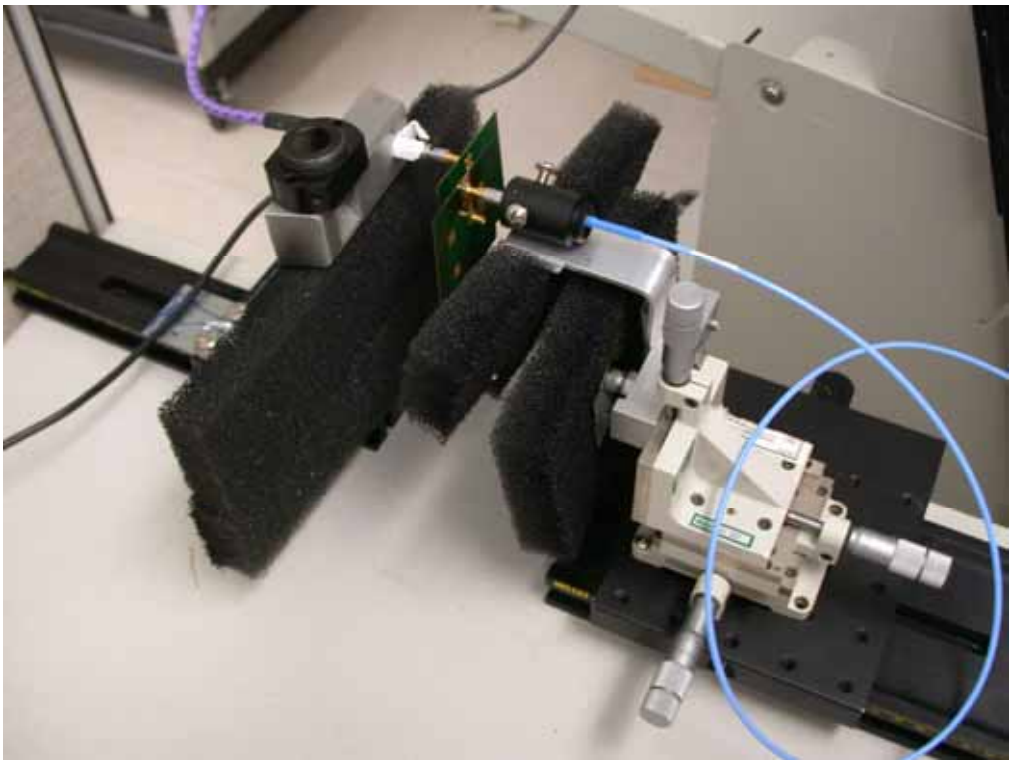


Fig. 3.2.4 The radiation pattern of the 2 × 2 grid antenna array with four independent feeds in the H-plane and E-plane, showing the changes of the pattern from far-field to the near-field.

Fig. 3.2.5 (a) and (b) show the setup for the simulation and measurement of the coupling between the two antennas. Fig. 3.2.5 (a) is related to a single gird array antenna and Fig. 3.2.5 (b) is related to a setup with a single grid array antenna pairing with a 2 × 2 grid antenna array with a combiner at the input.



(a)

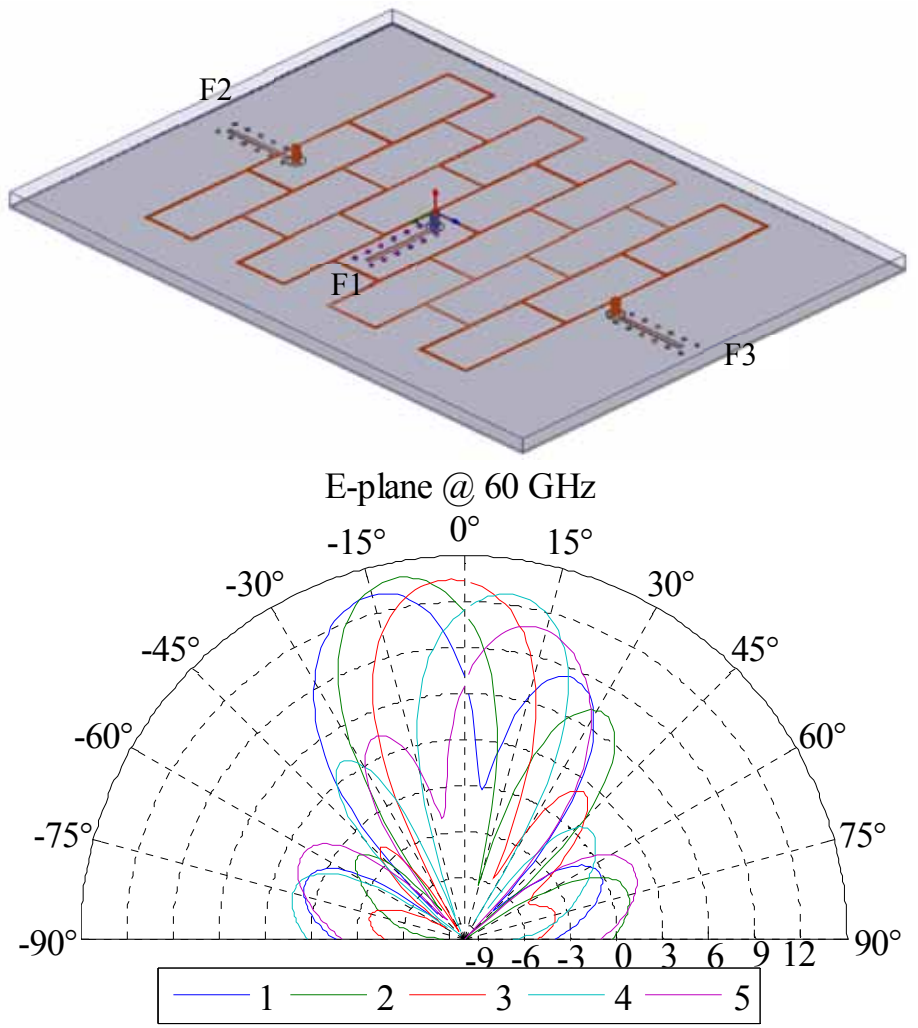


(b)

Fig. 3.2.5 The setup for (a) simulation and (b) measurement of the coupling between the grid array antennas.

Fig. 3.2.6 shows a three-feed grid array antenna that is able to steer the beam as much as 14° in the presence of quadrature-phased inputs. The table in Fig. 3.2.6 summarizes the

movement of the beam for different phase combination of the inputs. It also shows the maximum gain at the broadside direction and at the far-field region for each condition. The far-field radiation patterns in the broadside are also depicted in Fig 3.2.6.



Beam Num.	F1 (°)	F2 (°)	F3 (°)	Beam Angle (°)	Max. Gain (dB)
1	0	0	270	-14	13.3
2	0	270	180	13.6	13.6
3	0	180	180	13.7	13.7
4	0	90	90	12.6	12.6
5	0	0	90	10.9	10.9

Fig. 3.2.6 The setup for three-feed grid antenna array, the radiation pattern for it, and its beam-steering range.

Chapter 4

THEORETICAL ANALYSIS OF THE ENERGY HARVESTERS

The 60-GHz ISM band can be home to the most compact WPT systems by offering the most compact and integrated solutions without having coexistence issues [1]. In this work we present two energy harvesters that produce milliwatt-scale output powers with PCE rates in excess of 30%. The use of mm-wave frequency bands for power harvesting has been tested in recent years, [2-5], but the produced DC output power levels of these works are 0.28, 0.25, 0.003, and 0.019 mW and their peak PCE rates are 10%, 8%, 7%, and 1.2% respectively. Higher DC power delivery of our energy harvesting solutions permits a multitude of wireless systems to be able to employ them. The cascode energy harvester, which has two rectifiers in a cascode configuration to produce higher DC output power levels at the low-current regime, is the new addition to this work compared to what has been reported in [1] and [6]. For these two unique architectures, novel theoretical analyses to identify all the design tradeoffs are presented. The two 60-GHz energy harvesters convert the mm-wave input power to storable DC power which can be consumed

instantaneously or be used to charge storage capacitors or batteries. In [2] and [5] multi-stage Dickson multiplier is used as a rectifier and in [3] and [4] multi-stage inductor-peaked is presented. In this work a supply-less oscillator-like circuitry is utilized as a rectifier. As shown in Fig. 4.1(a), a supply-less differentially-driven complementary cross-coupled oscillator-like circuitry is chosen as a rectifier. The cross-coupled topology was suggested by [7, p.74], but in order to adopt it for mm-wave operation it is transformed to a tuned circuit which is similar to a relaxation oscillator without supply. This circuit, Fig. 4.1(a), is in fact a full-wave bridge rectifier in which the transistors are configured in a cross-coupled fashion instead of the diode-connected configuration as they appear traditionally. The advantage of the chosen configuration is less voltage drop on the rectifying devices which results in higher DC output power levels and PCE rates. A balun closes the bridge of the rectifier through its differential ports while its single-ended port is connected to the input port of the harvester.

The output capacitor of the single-stage rectifier, C_{STR}, is charged through M_1 and M_3 in half of the period as marked in Fig. 4.1(a) and through M_2 and M_4 in the other half. The charging current flows in the reverse direction of the transistors from the ground node towards the output node of the rectifier through the balun. The charging current produces and preserves the DC part of the voltages of the rectifier differential input nodes, OP and ON, and the rectifier output node, OUT. The unit-cells for NMOS and PMOS that are used in the entire design by replicating the same layout are low threshold (1-µm / 40-nm) devices. The replica counts of the devices are noted on the schematic diagrams of the harvesters. In both harvesters the conductances of the devices are matched by sizing them properly. A turn ratio of 1:2 is chosen for the input balun in order to increase the voltage swing at the rectifier differential inputs which results in higher V_{OUT} and PCE. Baluns with higher turn ratios suffer from higher losses and lower self-resonance frequencies. This

1:2 balun introduces 0.5 dB intrinsic loss at 60 GHz. The design considerations for this rectifier are similar to the 60-GHz oscillator that it resembles, similar to those of the mm-wave VCO design of [8]. Fig. 4.1(b) displays the micrograph of the single-stage energy harvester.

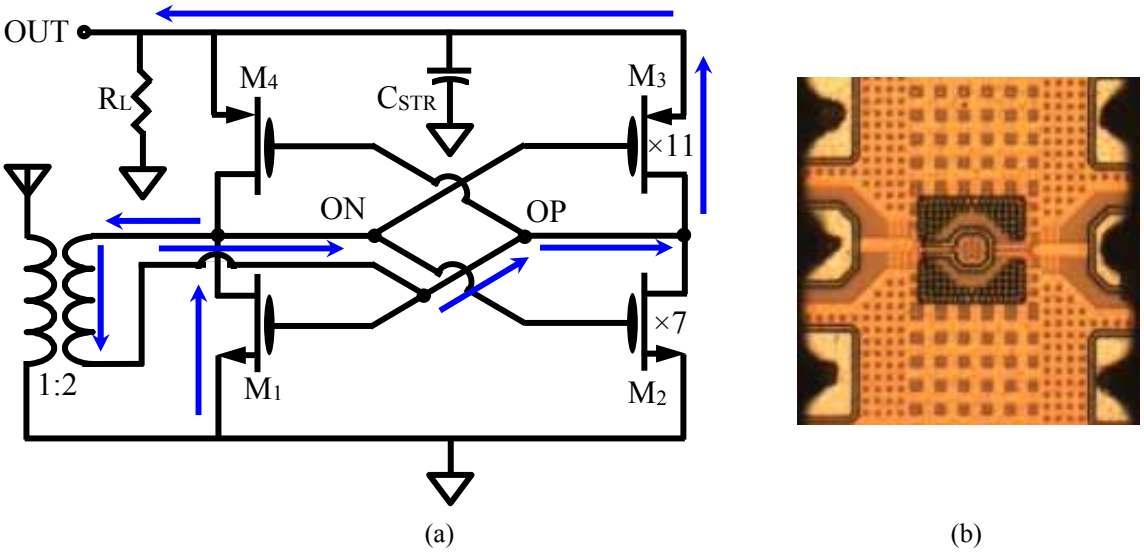


Fig. 4.1 (a) Simplified schematic diagram of the single-stage rectifier showing the path of the reverse charging current when $V_{OP} > V_{OUT}$ & $V_{ON} < 0$. (b) The micrograph of the single-stage harvester on a 60-GHz probe-station.

The second energy harvester is made of two rectifier circuitry in a cascode configuration as displayed in Fig. 4.2(a) such that the inputs of both stages are fed by a power-splitting balun, Fig. 4.2(b), which generates two similar differential signal pairs, OP & ON and OP1 & ON1, from the single-ended input. The voltage ratio for both secondary loops to the primary loop is 1:1, same as the turn ratio, but the current ratio is 1:½, due to virtually parallel operation of the two secondary coils. The impedance ratio is going to be 1:2. The NMOS devices of the upper stage suffer from higher threshold due to body effect. These 60-GHz energy harvesters are fabricated using 40-nm digital CMOS process in similar areas of 90 µm × 110 µm without pads. They can integrate with

compact antennas to form rectennas by using inexpensive packaging materials without damaging their great power conversion performances, [6].

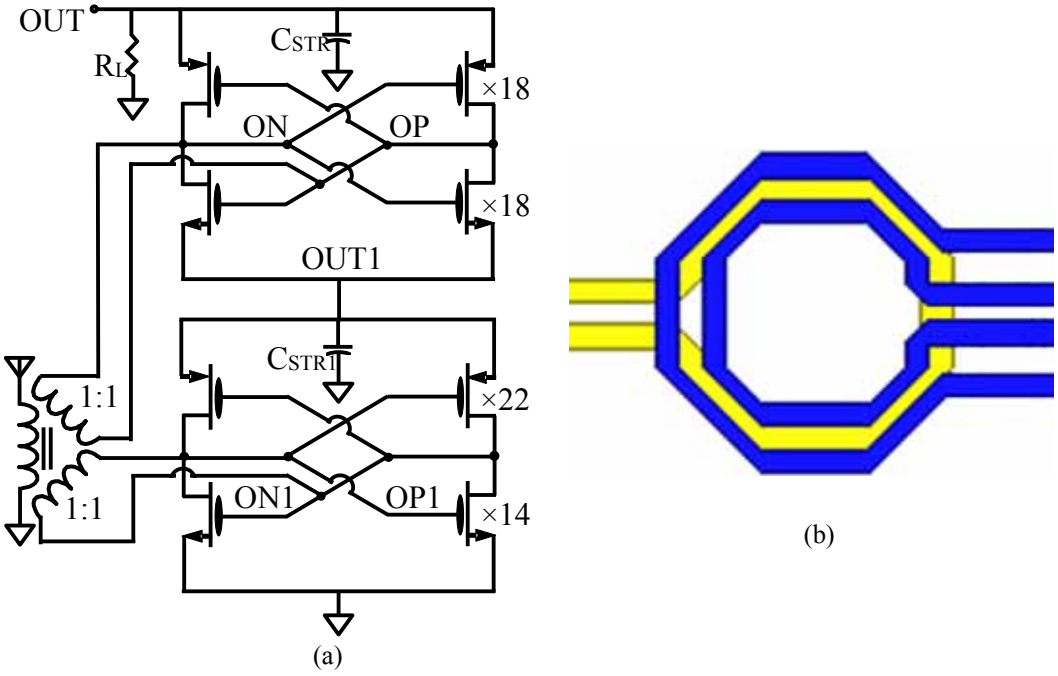


Fig. 4.2 (a) Simplified schematic diagram of the cascode energy harvester and (b) the power-splitting balun with two secondary loops, one inside the other.

4.1 Theoretical Analysis of Single-Stage Harvester

For the circuitry in Fig. 4.1(a), the transient simulation results of V_{OP}, V_{ON}, V_{OUT}, and the currents of the M_1, M_4, the sum of them, and the current of the resistive load (R_L) for the steady-state condition are displayed in Fig. 4.1.1. The results are for the input power level of 5.7 dBm, the frequency of 60 GHz, and the R_L of 1 kΩ. C_{STR} is sized such that V_{OUT} is entirely DC. The common mode voltage of the rectifier input nodes, V_{DC}, is ~ V_{OUT} / 2.

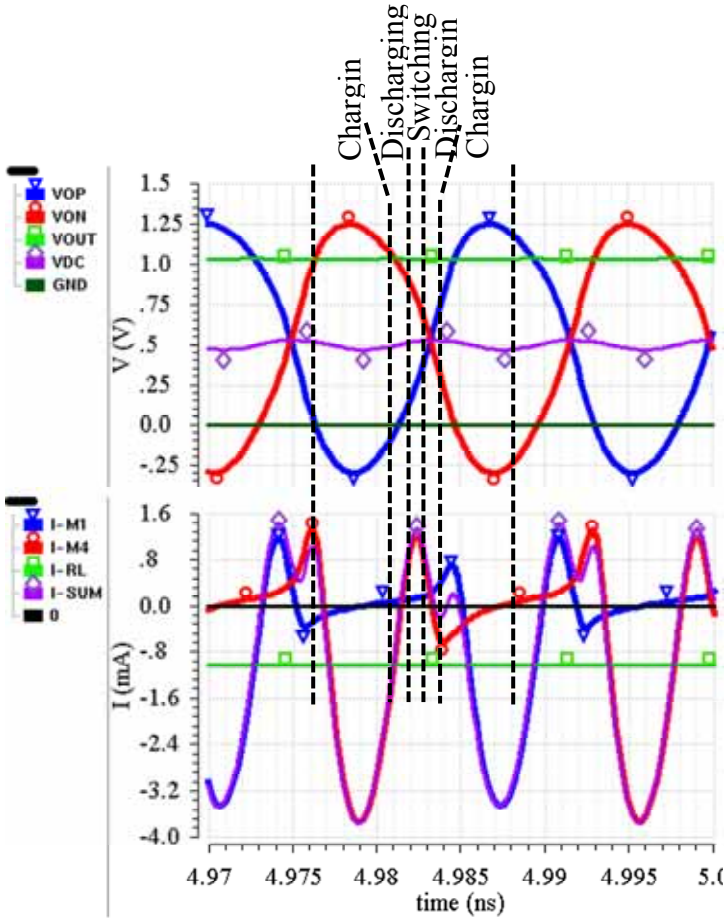


Fig. 4.1.1 The transient simulation results of all node voltages (top) and all currents of the single-stage harvester

As marked in Fig. 4.1.1, there are three regions for the rectifier operation in each period: switching, discharging, and charging. For M_1 and M_3, the charging region is when $V_{OP} > V_{OUT}$ and $V_{ON} < 0$ (ground voltage). The discharging region is when $V_{OP} < V_{OUT}$, but M_1 and M_3 are still in the triode region. The switching region is when all devices are in the saturation region and the

current is switched from one side of the rectifier to the other side. The single-ended input voltages V_{OP} and V_{ON} can be written as V_{OUT} / 2 +/- V_{PP} / 2 cos ($2\pi f_0 t$), where V_{PP} is the peak-to-peak voltage swing of V_{OP} and V_{ON} and f_0 is the input frequency. We have

where L_B is the power loss of the balun (W/W), Γ is the input reflection coefficient, Pin is the input

$$V_{PP} = \sqrt{2(1-L_B)(1-\Gamma^2)P_{in}R_{in}} \tag{8}$$

power of the harvster, and R_{in} is inverse of the real part of the differential input admittance of the rectifier. The rectifier tank is designed to operate close to the resonance condition where the parallel impedance of the tank is real and at its peak. In such a condition

$$\Gamma = \frac{R_{in}-R_S}{R_{in}+R_S} \Rightarrow V_{PP} = 2(R_{in} \parallel R_S)\sqrt{\frac{2(1-L_B)P_{in}}{R_S}} \tag{9}$$

in which R_S is the real part of the impedance seen through the differential side of the balun towards the antenna. The success of the design to tune the tank at resonance condition can be verified by the measurements when the input and output are switched around and the rectifier circuitry is biased in the form of an oscillator. In such condition, our measurement detected an oscillation frequency at 60.5 GHz. High input voltage swing is the most important factor in producing both high DC output voltage and high efficiency. In order to minimize the mismatch loss at the input, the impedance matching at the input has to be achieved by properly sizing the rectifier devices for the designated input power level. R_L is bypassed by C_{STR} and hence it is absent in (9) and does not affect R_{in} directly. However, the effect of R_L on the input impedance, input matching, and the input voltage swing is through its impact on the level of V_{OUT}.

In order to find the large signal input impedance which is needed to solve (9), we use the r_{on} of the devices since in both charging and discharging regions the rectifier devices are in triode region. For M_1, with the current, $I_{M1,}$ we have

$$r_{on}^{-1} = \frac{\partial I_{M1}}{\partial V_{DS1}} = \frac{\partial I_{M1}}{\partial V_{ON}} = \beta\left(3V_{OP} - 2V_{OUT} - V_T\right) \tag{10}$$

where V_T is the threshold voltage and $\beta = \mu C_{OX} W / L$ of M_1 which is chosen to be the same for all rectifier devices. The large-signal differential input impedance of the parallel resonant tank or the rectifier, R_{in}, is obtained by averaging r_{on}^{-1} of the devices over the charging, discharging, and switching regions. The switching region is short enough to be ignored. In the charging and discharging regions relevant transistors are in triode. In each of the two symmetrical quarter-periods ($T_0 / 4$) in which M_1 is conducting, R_{in} can be written as

$$R_{in} = \frac{2}{\frac{1}{T_0 / 4}\int_{t\left\{V_{OP}=\frac{V_{OUT}}{2}+\frac{V_T}{2}\right\}}^{t\left\{V_{OP}=\frac{V_{OUT}}{2}+\frac{V_{PP}}{2}\right\}} r_{on}^{-1}\,dt} = \frac{T_0}{2\beta\int_{t\left\{\frac{V_{OUT}}{2}+\frac{V_T}{2}\right\}}^{t\left\{\frac{V_{OUT}}{2}+\frac{V_{PP}}{2}\right\}}\left(\frac{3V_{PP}}{2}\cos\left(2\pi f_0 t\right) - \frac{1}{2}V_{OUT} - V_T\right)dt} \tag{11}$$

in which the triode condition for M_1 requires $V_{OP} > V_{OUT} / 2 + V_T / 2$. In the charging region, the real part of the impedance of the cross-coupled pair is positive due to the reverse direction of the current whereas in the discharging region it is negative. By solving (11), R_{in} can be written in the following simplified closed form which depends on both V_{PP} and V_{OUT}.

$$R_{in} = \frac{2}{\beta\left(\frac{3}{\pi}V_{PP} - \frac{1}{2}V_{OUT} - V_T\right)} \tag{12}$$

Since this full-wave bridge rectifier is balanced, the balun does not carry any DC current and the DC output current, I_{OUT}, is exclusively passing through the devices. As a result the output current is equal to the mean of the current of each device in one of the two symmetrical quarter-periods that it is on. If we neglect the current in the switching region, for M_1 we have

$$I_{OUT} = -4 f_0 \beta \left[\int_{t\left\{\frac{V_{OUT}}{2}+\frac{V_T}{2}\right\}}^{t\{V_{OUT}\}} \left((V_{OP} - V_T) V_{ON} - \frac{{V_{ON}}^2}{2} \right) dt \right.$$
$$\left. + \int_{t\{V_{OUT}\}}^{t\left\{\frac{V_{OUT}}{2}+\frac{V_{PP}}{2}\right\}} \left((V_{OP} - V_{ON} - V_T) V_{ON} + \frac{{V_{ON}}^2}{2} \right) dt \right] \quad (13)$$

in which the first term is related to the discharging region and the second term is for the charging region in which M_1 current is in the reverse direction. Since $I_{OUT} = V_{OUT} / R_L$, V_{OUT} can be found from (13) in the following simplified closed form as a function of both V_{PP} and R_{in}.

$$V_{OUT} \approx \frac{2V_{PP}\left(R_L \,||\, 2R_{in}\right)}{\pi R_{in}} \quad (14)$$

By solving (9), (12), and (14) together, V_{PP}, V_{OUT}, and R_{in} can be determined. As (14) shows, to produce larger V_{OUT} / V_{PP} smaller R_{in} / R_L is required. But in such cases, the ratio of I_{OUT} to the internal current of the rectifier is small and hence PCE is low. PCE can be formulated as (15) by using (9) and (14).

$$PCE = \frac{{V_{OUT}}^2}{R_L P_{in}} = \frac{32\left(R_L \,||\, 2R_{in}\right)^2 \left(R_S \,||\, R_{in}\right)^2 \left(1 - L_B\right)}{\pi^2 {R_{in}}^2 R_L R_S} \quad (15)$$

Maximum possible power conversion efficiency irrespective of the relations between different impedances and the input matching can be derived from (15) as illustrated in (16).

$$R_S \,||\, R_{in} \le \frac{\sqrt{R_S R_{in}}}{2} \;\&\; R_L \,||\, 2R_{in} \le \frac{\sqrt{2R_L R_{in}}}{2} \Rightarrow PCE_{\max} = \frac{4\left(1 - L_B\right)}{\pi^2} \tag{16}$$

The condition to have maximum PCE happens when $R_{in} = R_S$ and $R_{in} = R_L / 2$. In order for these two conditions to happen simultaneously, R_L should be close to 2 * R_S. In the design of the single-stage energy harvester R_S = 190 Ω, therefore an R_L around 380 Ω is the best to create maximum PCE condition. Considering that the output power is targeted to be close to 1 V, the current for this condition is around 2.5 mA. Other parameters of the single-stage harvesters are β = 16 mA/V^2, V_T = 0.44 V, L_B = 0.12 W/W. Based on (16) the highest possible PCE is going to be 35.7%. The minimum available power at the rectifier input is assumed to be 5.7 dBm and the targeted DC output power delivery is 1 mW.

4.2 Theoretical Analysis of Two-Stage Cascode

The two-stage cascode energy harvester uses the same mechanism of rectification as does the single-stage and the same analysis can be applied, provided that V_{OUT1} is about V_{OUT} / 2 and it is considerably greater than the average V_T of the devices. The input impedance of the cascode stage, R_{in}, is the parallel of the input stages of the two stages, which is approximately half of each of them. The equations (8) and (9) are still valid for the two-stage cascode harvester. But equations (10), (11), and (12) which ultimately formulate R_{in} based on V_{OUT} and V_{PP} transform to (17).

$$R_{in} = \frac{1}{\beta\left(\frac{3}{\pi}V_{PP} - \frac{1}{4}V_{OUT} - V_T\right)} \tag{17}$$

The equation (13) and (14) change to (18) which is a simplified closed form for V_{OUT}. It can be assumed that the resistive loading of R_L is split between the two stages such that each of them is loaded by $2R_L$.

$$V_{OUT} \approx \frac{V_{PP}\left(R_L \,||\, 12R_{in}\right)}{\pi R_{in}} \tag{18}$$

The PCE can be written as (19) just by using (17) and (18).

$$PCE = \frac{V_{OUT}{}^2}{R_L P_{in}} = \frac{8\left(R_L \,||\, 12R_{in}\right)^2 \left(R_S \,||\, R_{in}\right)^2 \left(1 - L_B\right)}{\pi^2 R_{in}{}^2 R_L R_S} \tag{19}$$

The absolute maximum PCE independent of the impedance levels is going to be as formulated in (20).

$$PCE_{\max} = \frac{6\left(1 - L_B\right)}{\pi^2} \tag{20}$$

The absolute maximum of the PCE of the two-stage cascode energy harvester is 50% larger than the single-stage. The condition to have the maximum PCE is when $R_{in} = R_S$ and $R_{in} = R_L / 12$ simultaneously. Considering that $R_S = 50\ \Omega$, this condition would require $R_L \sim 600\ \Omega$. For the two-stage cascode harvester $\beta = 32\ mA/V^2$, $V_T = 0.46$ V, and $L_B = 0.12$ W/W, which result in a peak PCE of 53.6% based on (20).

Chapter 5

WIRELESS POWER HARVESTING DESIGN

5.1 System Specifications

In this work the goal is to achieve a range of about 40 mm for the power transfer. This is similar to the range of the Proximity Integrated Circuit Cards (PICCs), which follow ISO/IEC 14443-4 transmission protocol and support contactless communications. The link budget analysis for the wireless power transfer is performed similar to how it is done for data transfer systems. The coupling between the TX and RX antennas is the main factor in establishing a WPT link. Friis transmission equation

$$\frac{P_{rx}}{P_{tx}} = G_{tx}\,\frac{\lambda^2}{(4\pi R)^2}\,G_{rx} \tag{21}$$

determines the required transmitter output power, P_{tx} (W) to ensure the sufficiency of the available power at the rectenna input, P_{rx} (W), when it is placed at a far-field distance of R (m) from the transmitter. The antenna coupling embeds the effects of several important factors for the WPT operation including the gains of the RX and TX antennas, the free-space path loss, and the near-

field or far-field behaviors, as in the right side of (21). Within 4 cm spacing between the designed grid antennas of the RX and TX, the measurements indicate coupling factors between -18.9 to -17.4 dB.

The defining specification of the rectenna of this WPT system is the minimum required DC power delivery which also dictates the minimum transmit power delivery specification based on (21). For this 60-GHz WPT system a minimum power delivery or storage of 1 mW is chosen which can be consumed instantaneously or be used to charge a battery or a capacitor. This power level is significantly higher than the levels targeted by the UHF WPT solutions [3-6] and mm-wave energy harvesters [8-11]. Higher DC power delivery permits a multitude of wireless systems to be able to employ this WPT solution. The design targets of this 60-GHz WPT system are to generate the highest output power at the transmitter and the highest RF-to-DC power conversion efficiency at the rectenna.

To produce 1 mW DC power at the rectenna output port about 5.5 dBm mm-wave power is required at the rectenna input port, assuming a respectable 30% PCE rate. Considering -18.9 dB coupling between the TX and RX antennas at 4 cm spacing, the transmitter needs to support an ambitious combined output power delivery of ~25 dBm. This level of TX power delivery in digital CMOS necessitates performing a 32-way (4 × 8-way) differential power combining at the end of the transmitter chain, based on what has been achieved by the references, Table 6.5.1. An array of 2 × 2 transmit chains requires an effective output power of 19 dBm from each TX chain. Fig. 5.1.1 depicts a simple block diagram of this 60-GHz WPT system that indicates expected power levels at different ports of the system and specifies the discussed targeted specifications.

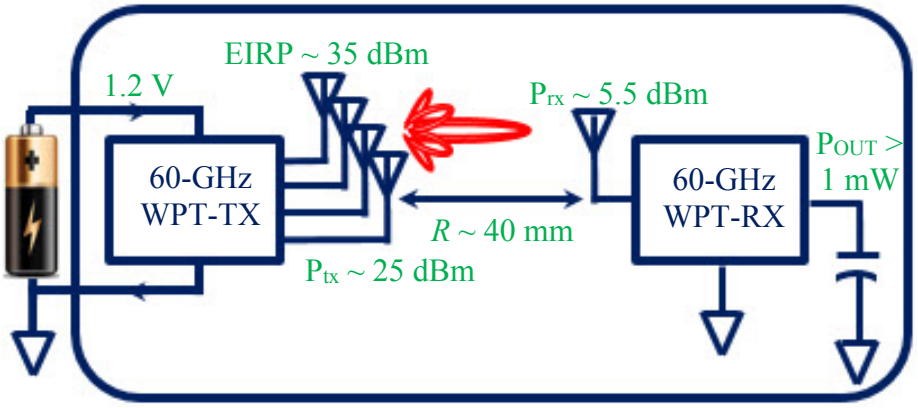


Fig. 5.1.1. A simple block diagram of the 60-GHz WPT system with targeted TX and RX power delivery specifications.

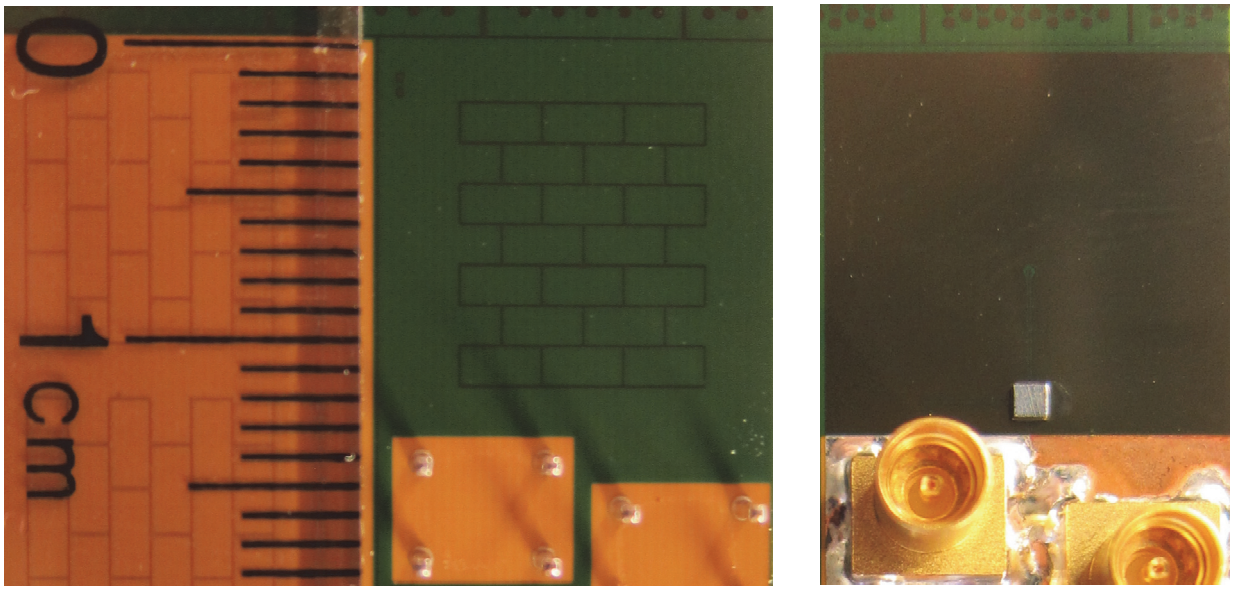
5.2 Antenna Advantage and Antenna Design

Magnetically coupled wireless power transfer solutions suffer from very limited range of operation. The coupling factor declines very rapidly with distance and misalignment. Furthermore,

$$G_{tx/rx} = \frac{4\pi A_{tx/rx(eff)}}{\lambda^2} \tag{22}$$

in close proximities, high magnetic coupling creates adverse detuning effects on the couplers [19]. Another disadvantage of the magnetic coils is that placing them in the proximity of metal planes like those of the battery, the screen, and the circuit boards of cellular phones, heavily degenerates them and they lose efficiency. This is a serious challenge in implementing couplers, but in contrast, antennas, with their ground backplanes are not affected in such conditions. Another advantage of the mm-wave antennas is that high gain antenna arrays with high directivity can be realized and integrated in small footprints. Since the aperture of the antenna is proportional to the wavelength squared, the number of antenna elements that fit in a given area grows with frequency squared. Equation (22) shows this relationship where $A_{tx/rx(eff)}$ is the effective area of the TX or RX antenna (m^2), and λ is the free space wavelength (m).

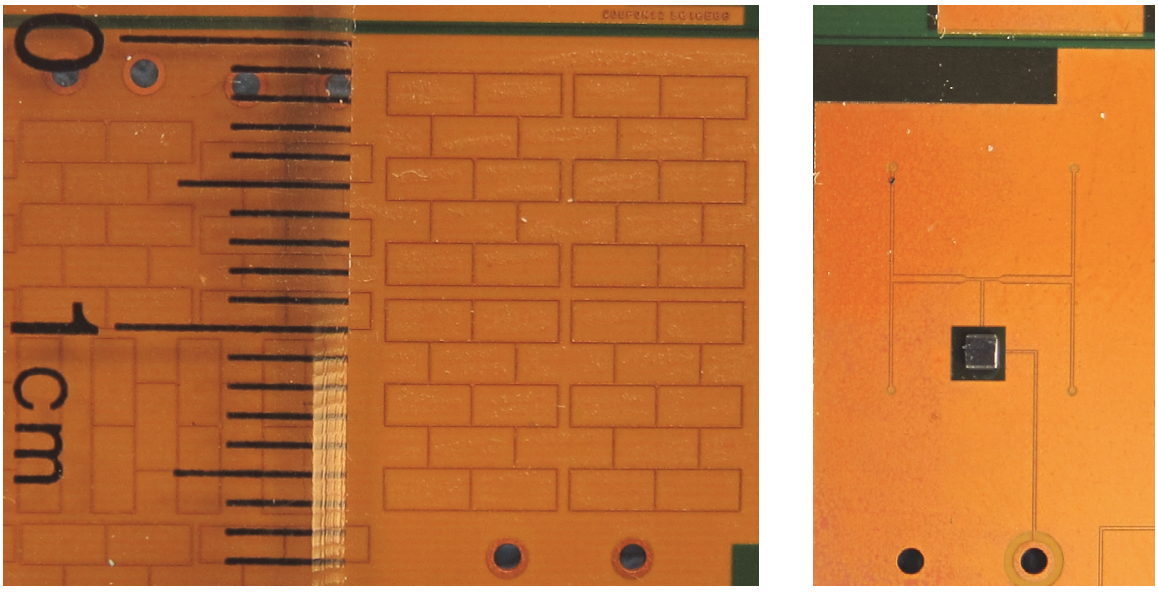
Fig. 5.2.1 displays the back and front views of the rectenna with its integrated grid antenna using a flip-chip package technology. The connectors are devised to measure the DC output power of the 60-GHz WPT system at the output port of the rectenna.



(a) (b)

Fig. 5.2.1 (a) Front and (b) back views of the integrated rectenna.

The TX antenna is a 2 × 2 grid array antenna which is portrayed in Fig. 5.2.2. In order to



(a) (b)

Fig. 5.2.2 (a) Front and (b) back views of the 2 × 2 grid array antenna of the TX.

characterize the coupling between the TX and RX antennas, a configuration of the TX antenna with a single feed is integrated with the harvester. In such case, the RX antenna is used to transmit mm-wave power. The RX and TX antennas have been optimized for maximum directivity at 60 GHz in the broadside direction. The antennas are fabricated on a CCL-HL832MG package with a permittivity (εr) of 3.36, a loss tangent (tanδ) of 0.012, and a thickness of 500 μm. The RX and TX grid antennas occupy 1.2 cm × 1.3 cm and 1.3 cm × 1.7 cm, respectively. Fig. 5.2.3 shows the setup for the RX to TX antenna coupling simulations.

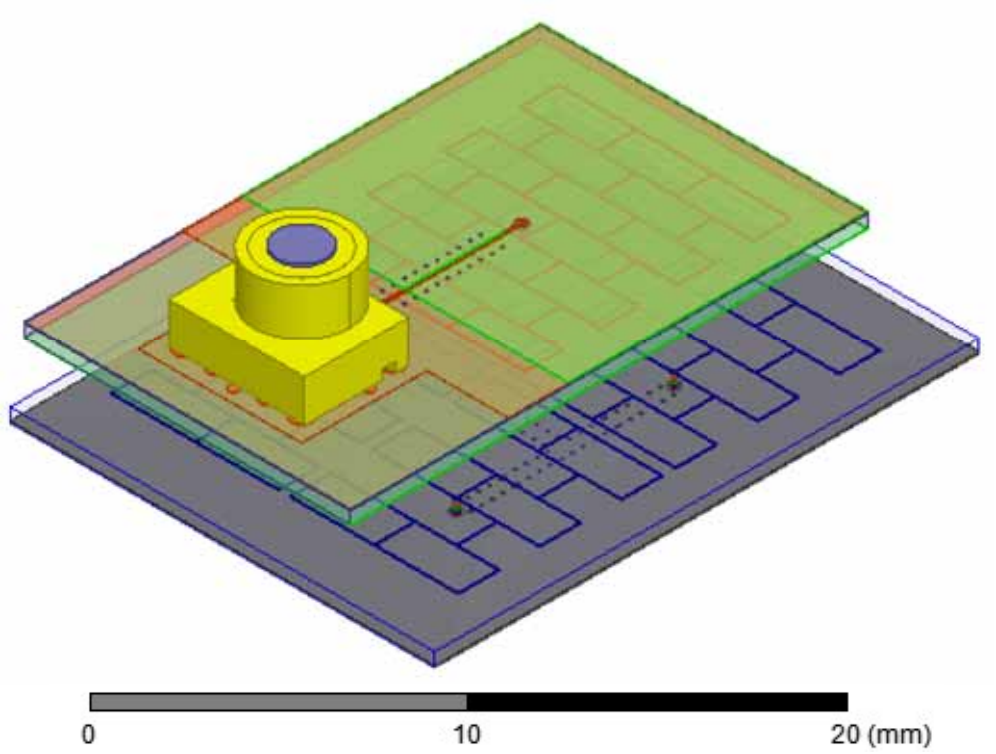


Fig. 5.2.3. The setup for coupling simulations between the RX and TX antennas.

Fig. 5.2.4 displays the results of the simulations and measurements for the radiation pattern of the TX grid array antenna. The results are for (a) E-plane and (b) H-plane at 57, 60, and 64 GHz frequencies. The measured far-field gains of the grid antennas of the TX and RX are respectively 8.9 dBi and 10.7 dBi at 60 GHz with a bandwidth of 2.5 GHz. The measured gains at 57 and 64 GHz are close to the simulation results, whereas at 60 GHz, the measurement shows ~3 dB lower

peak gain compared to the simulation. The reason for this discrepancy at mid-band is not clear, but some part of it could be related to the mismatch between the antenna elements and their feeds. Based on these result, a flatter frequency behavior from 57 to 64 GHz is expected from the measurements compared to the simulations.

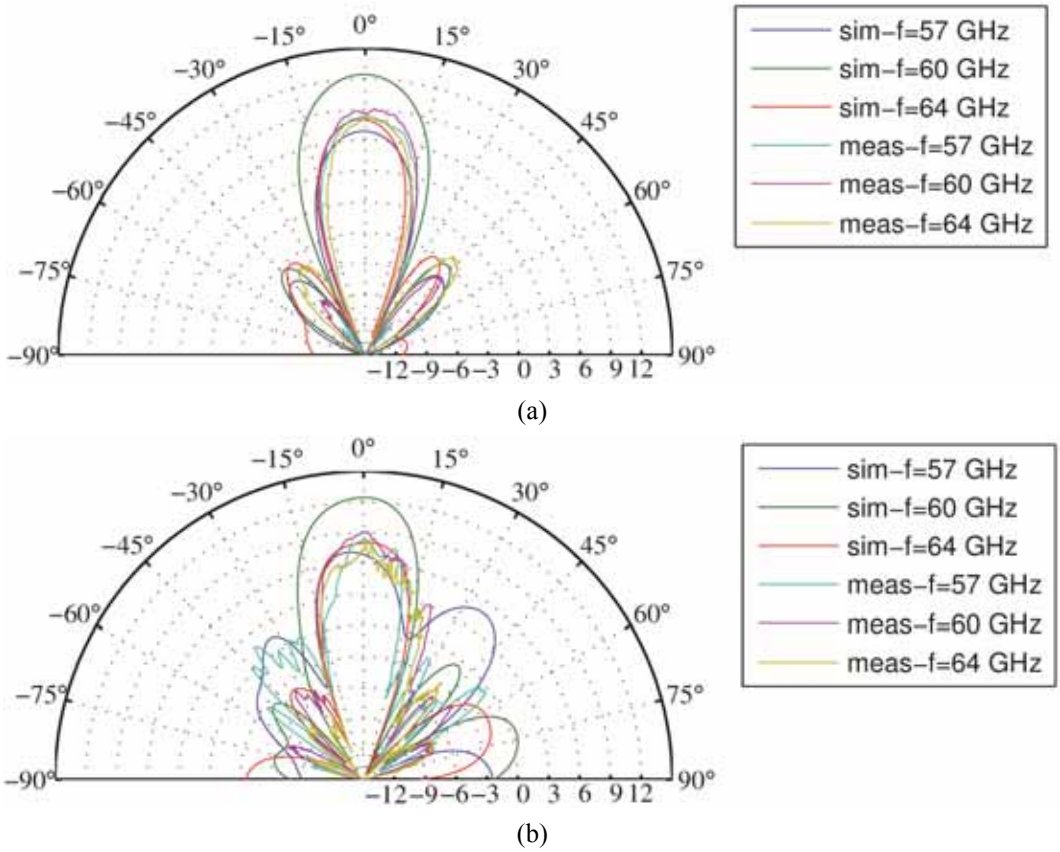


Fig. 5.2.4 The measured and simulated radiation patterns of the TX grid array antenna in (a) E-plane and (b) H-plane at 57, 60, and 64 GHz.

Fig. 5.2.5 summarizes the coupling results between the TX and the RX antennas at 60 GHz for simulations, measurements, and the theory which is based on Friis Transmission Equation. Within the 4 cm spacing, which is the targeted range of this WPT system, there is between -18.9 to -17.4 dB coupling between the two antennas and there is no significant difference between the simulation and measurement results.

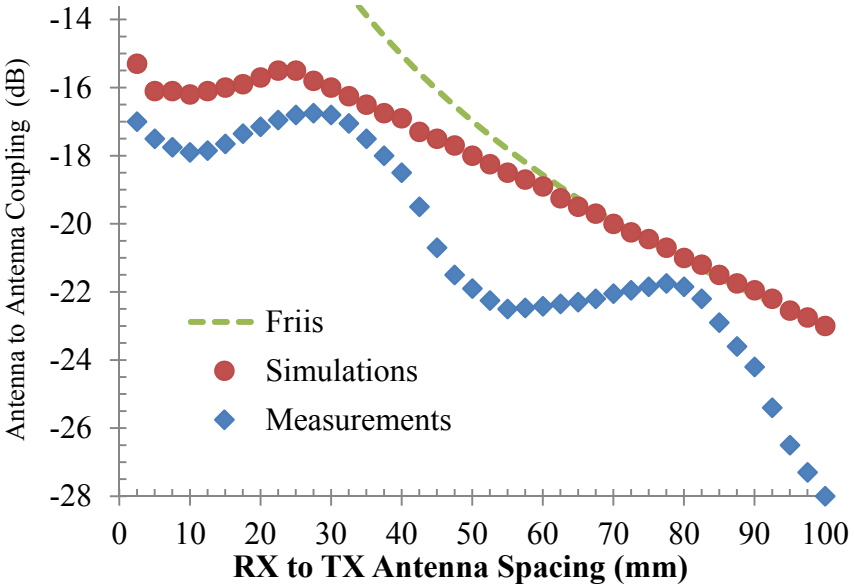


Fig. 5.2.5 Coupling between TX and RX antennas based on simulations, measurements, and Friis Transmission Equation.

5.3 Energy Harvesting Design

The energy harvester of this WPT system converts the 60 GHz input power that the rectenna receives to storable DC power which can be consumed instantaneously or be used to charge a capacitor or a battery. The mm-wave harvesters that have been reported, either use multi-stage Dickson multipliers, as in [8] and [11] or inductor-peaked which is proposed in [9] and [10]. But the DC output power levels and PCE levels generated by these energy harvesters are very low. In [10] the effort is to create the highest sensitivity and the lowest input power level to start the harvester, but the output power is extremely low. As shown in Fig. 5.3.1, a supply-less differentially-driven complementary cross-coupled oscillator-like circuitry is chosen as a rectifier. The cross-coupled topology was suggested by [12, p.74], but in order to adopt it for mm-wave operation it is transformed to a tuned circuit which is similar to a relaxation oscillator. It is capable of producing milliwatt-scale DC output power with peak PCE rates greater than 30%. This circuit

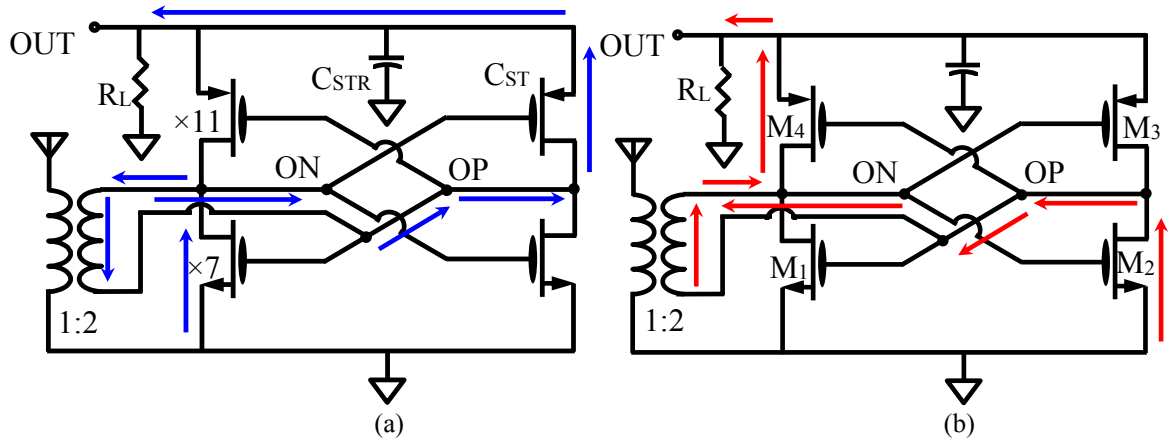


Fig. 5.3.1 Simplified schematics of the rectifier, showing the paths of the charging currents when (a) $V_{OP} > V_{OUT}$ & $V_{ON} < 0$ and (b) $V_{ON} > V_{OUT}$ & $V_{OP} < 0$.

is in fact a full-wave bridge rectifier in which the transistors are configured in a cross-coupled fashion instead of the diode-connected configuration as they appear traditionally. The advantage of the chosen topology is less voltage drop on the rectifying devices which results in higher DC output power level and higher PCE. There is a balun that closes the bridge of the rectifier through its differential ports while its single-ended port is connected to the rectenna input.

The output capacitor, C_{STR}, is charged through M_1 and M_3 in half of the period and through M_2 and M_4 in the other half. The charging current flows in the reverse direction of the transistors from the ground towards the output node of the rectifier through the balun. The charging current produces and preserves the DC part of the voltages of the differential rectifier input nodes, OP and ON, and the ultimate output port of this 60GHz WPT system, node OUT. The paths of the reverse charging currents in each half of the period are marked in Fig. 5.3.1 (a) and (b). Similar to the transmitter blocks, the unit-cell counts are noted on the schematic diagrams of each block.

The transient simulation results of V_{OP}, V_{ON}, V_{OUT}, and the currents of the M_1, M_4, the sum of those, and the current of resistive load (R_L) for the steady-state condition are displayed in Fig. 5.3.2. The results are for the input power level of 5.7 dBm, the frequency of 60 GHz, and the R_L of 1 kΩ. C_{STR} is sized such that V_{OUT} is entirely DC. The common mode voltage of the rectifier

input nodes, V_{DC}, is defined as (V_{OP} + V_{ON}) / 2 which is about V_{OUT} / 2. In order to make the rectifier balanced the conductance of the rectifier devices are matched.

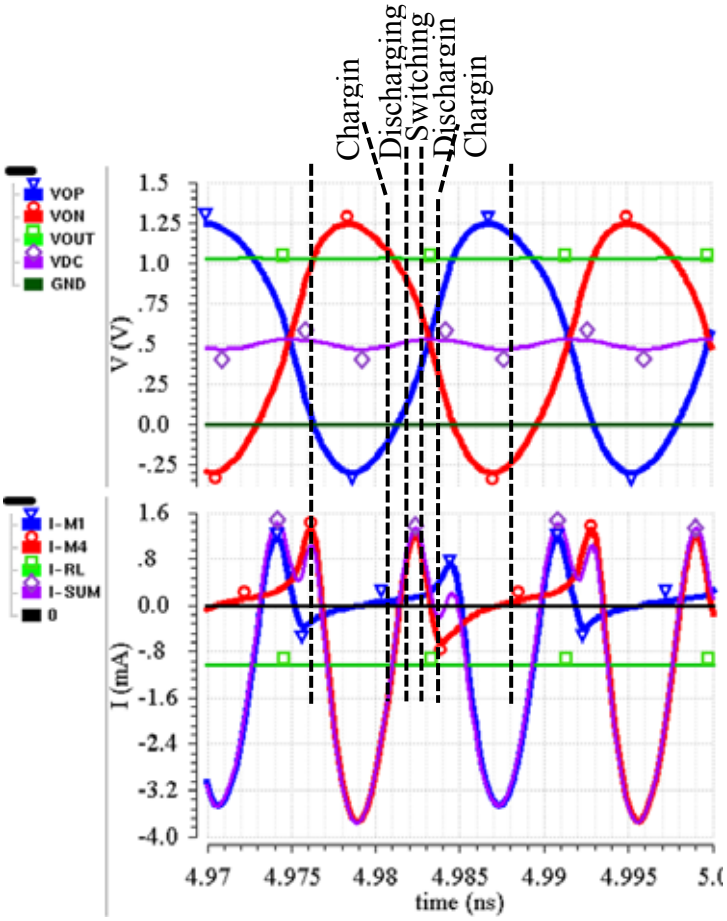


Fig. 5.3.2 The transient simulation results of all node voltages (top) and all currents of the single-stage harvester

5.4 Transmitter Architecture

All experimented architectures that have been used for high-power mm-wave PAs in digital CMOS technology include power combiners at the end of their power amplifier chains. The voltage reliability limits are such that the voltage swing levels at the output port for high power transmission is beyond what can be tolerated by the active devices. Without power combiners, the only alternative is to lower the impedance level at the output port of PAs to lower the voltage swing, but the drawbacks are low gain of such huge devices and impracticality of the antenna matching network. The references for mm-wave PAs in digital CMOS technology for frequencies higher than 60 GHz, [13-18] offer empirical data to know what is achievable with different counts of PA unit power combination. Table 6.5.1 shows the trend in the level of saturated output power (P_{sat}). The highest P_{sat} with 2-way differential, 4-way differential, and 8-way differential power combining are respectively 18.6, 20.9, and 22.6 dBm. Based on this data, without power combination of 32-way differential, achieving about 25dBm is not possible in digital CMOS with feature size of 40 nm or 65 nm. On the other hand, increasing the number of parallel PA units at the final stages faces a limit when the additional loss of the power combining structure is in the order of the additional power of the extra added PA units. For this WPT TX, a 4 × 8-way differential power combining is implemented. The factor of 4 is achieving by combining the power over the air. This is four times higher integration level than what has been achieved by any mm-wave CMOS PA design as evidenced by Table 6.5.1. As Fig. 5.4.1 illustrates, the 2 × 2 transmitter

array consists of a quad-core PA with a combiner to add up the power of the final 8 virtually-parallel differential stages.

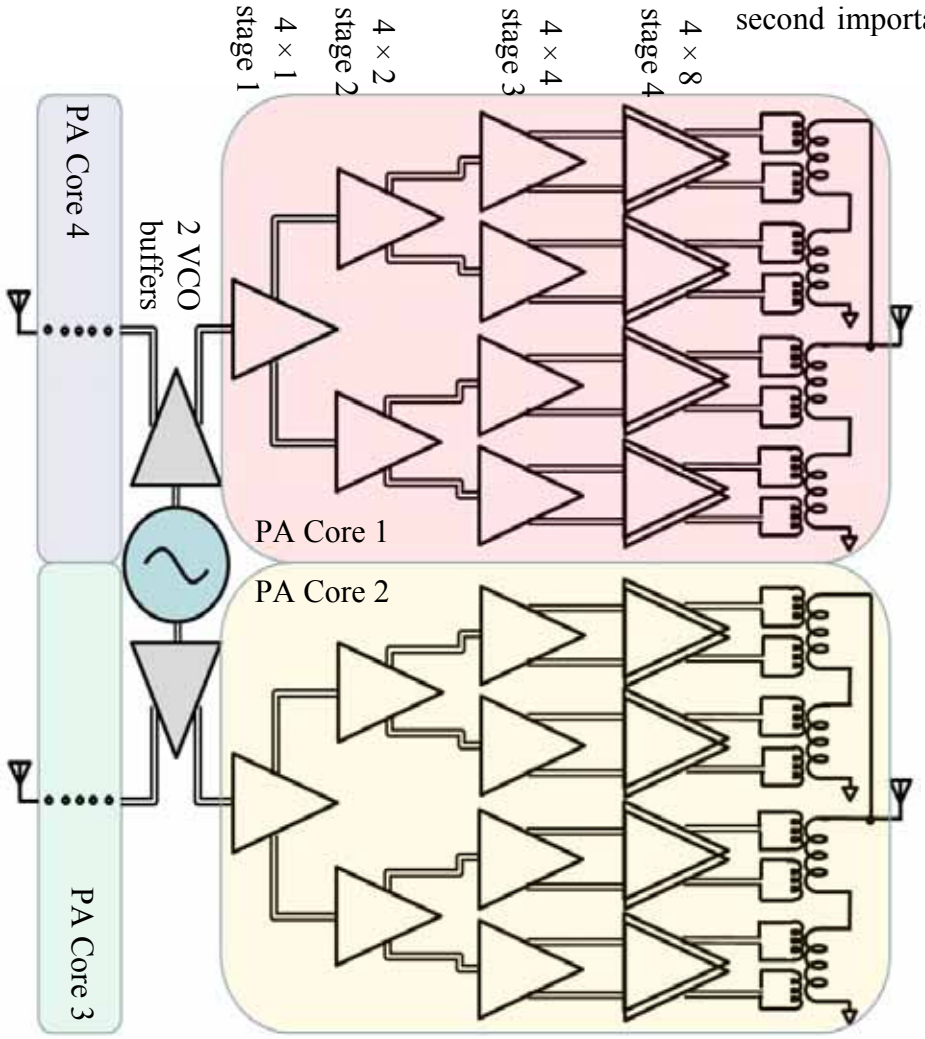


Fig. 5.4.1 Simplified TX block diagram demonstrating the binary-tree architecture and displaying two cores of the quad-core PA.

The second important decision for mm-wave CMOS PA architecture design is how to distribute the power from the common source of power which is an oscillator in this case. There are two main ways to do it: distributed PAs and virtually-parallel PA chains. In distributed amplifiers as explained in [13], [15], and [20] the power first splits into diverging paths, but gather back in a close proximity at the end of the chain to perform an efficient power combining. To implement parallel PA chains, the power first

splits into different parallel paths to feed different chains and at the end the power combiner combines the total power to be delivered to the load. This is the method that PAs in [14] and [16-18] are implemented. The floorplan of [18, Figure 23.8.6] best displays this method. In this work, a binary-tree architecture is implemented using power-splitting transformers. At the output of each stage, the power splits between two parallel chains and as a result number of parallel stages doubles from each stage to the next. A 60-GHz free-running oscillator (VCO) is located at the heart of the transmitter followed by 2 VCO buffers. Fig. 5.4.1 displays a simple block diagram of cores 1 and 2 of the quad-core amplifier. As demonstrated, in each of the four PA cores there are 1 unit of stage 1, 2 stage 2, 4 stage 3 and 8 stage 4 operating virtually in parallel, as expected from binary-

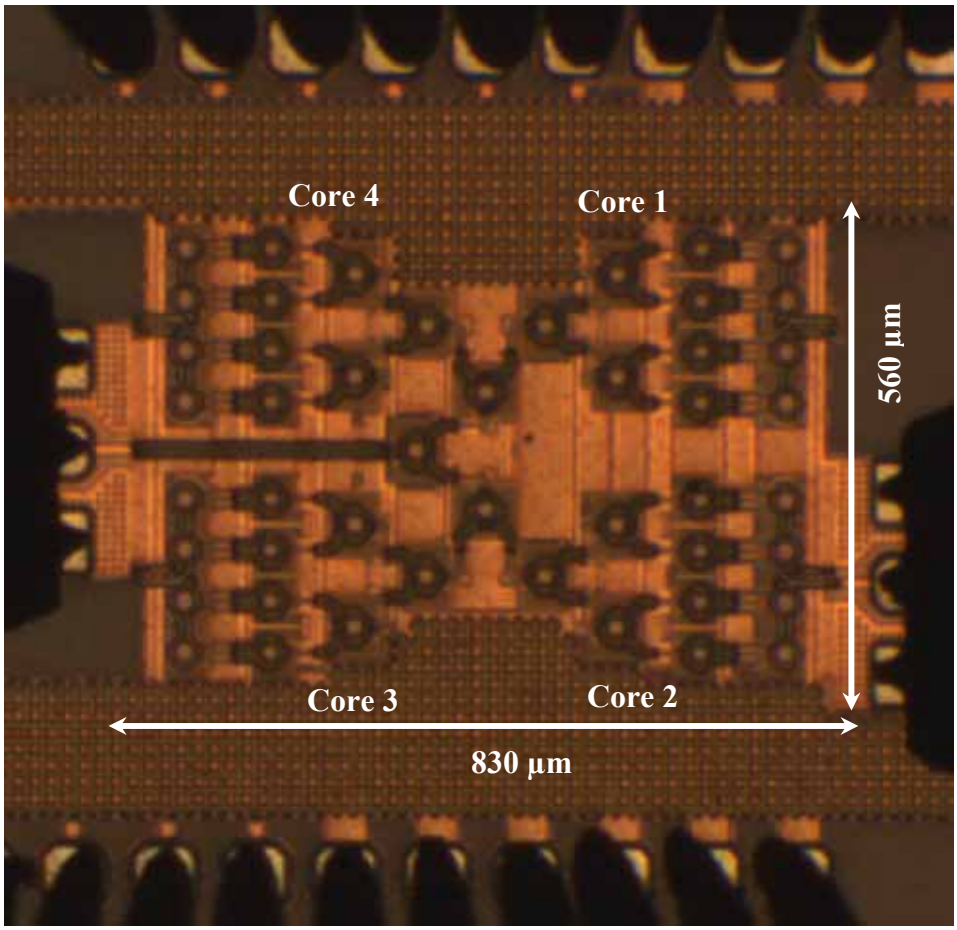


Fig. 5.4.2 The micrograph of the quad-core PA.

tree architecture. The floorplan of the transmitter can be seen in the micrograph of the quad-core PA, which occupies an area of 830 μm × 560 μm, Fig. 5.4.2.

5.5 Transmitter Block Design

The third important factor in the design of the mm-wave CMOS amplifiers is the choice of topology for the stages, although there are not significant differences in the designs in the references [13-18]. All designs are pseudo-differential NMOS-only tuned stages. Reference [16] uses transmission lines and passive components for intra-stage matching [16, Figure 15.5.7], but the other references and this design use transformers for that purpose. References [14] and [18] use cascode devices. But in this design, we found the loss at the source nodes of the cascode devices excessive. The main differentiations of this design compared to the references are utilization of the neutralizing capacitors for better stability and switched-capacitors for accurate tuning, in addition to the architectural differentiations of implementing the 4 × 8-way differential power combining and the binary-tree floorplan.

The main design objective of the 60-GHz VCO for WPT purposes is to produce high output power and the usual objective of low phase noise performance is not a factor here. But in order to build an efficient design similar considerations as in [21-24] are applied for the VCO of this project. A cross-coupled NMOS pair with transformer loading and accumulation varactors is a proper topology for such a high power VCO, since it benefits from maximum possible voltage headroom for the cross-coupled devices, Fig. 5.5.1(a). A (1-μm / 40-nm) NMOS transistor with low threshold voltage is adopted as the unit-cell for all devices of the entire design of the transmitter and also the energy harvesting receiver. For this technology, simulations and measurements show that the devices with wider finger sizes suffer from larger series gate

resistances and the ones with narrower finger sizes necessitate higher multiples which introduce higher parasitic capacitances. The counts of the unit-cell replicas are noted on the schematic diagrams of all blocks. In the VCO, 64 multiples of the unit-cell NMOS devices and 16 unit-cells of accumulation varactors are used. The power-splitting transformer of the VCO is displayed in Fig. 5.5.2. The measurement of the standalone VCO shows that it produces 6.3 dBm at each of the two secondary outputs of its power-splitting transformer.

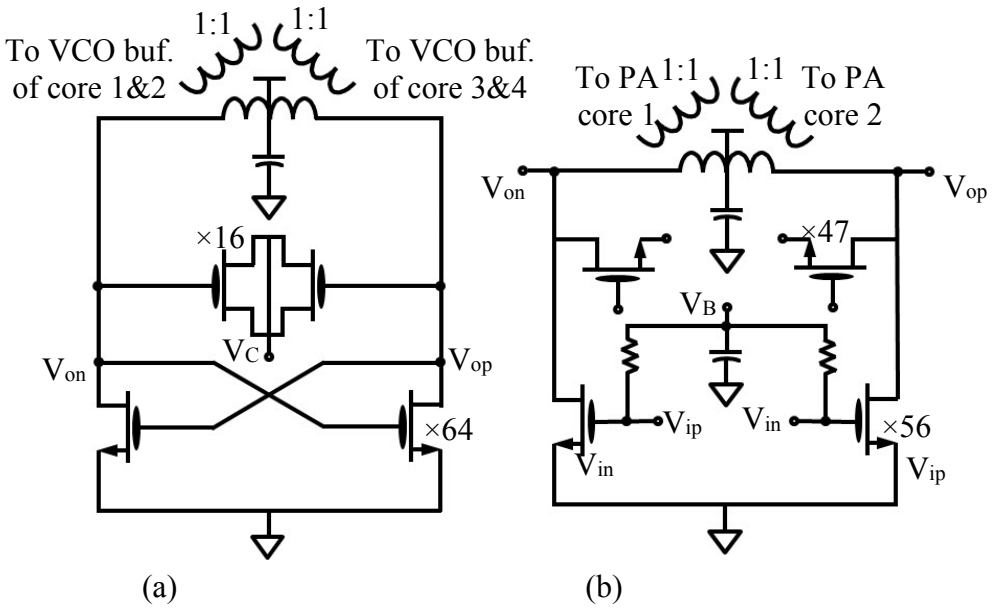
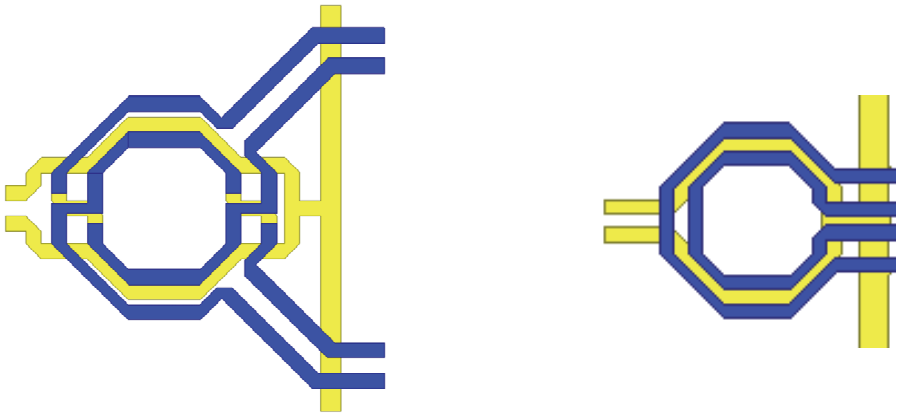


Fig. 5.5.1 Simplified schematic diagrams of (a) 60-GHz VCO, (b) VCO buffer.

All stages following the VCO, including the VCO buffers, are tuned pseudo-differential common source NMOS pairs with neutralizing capacitors and power-splitting transformers. The neutralizing capacitors, which are floating-source transistors, have 85% of the multiple counts of the main common source devices and are connected between the input and the output nodes which are in-phase. They help with the stability and strengthen the unilateral behavior of the devices of the 60-GHz power amplifier elements by cancelling out the unwanted feedback through C_{GD} of the main devices. All stages of the transmitter are tuned at 60 GHz and 2-bit switched-capacitors at the output nodes of each stage adjust the tuning. Fig. 5.5.1(b) displays the schematic diagram of

the VCO buffer. All stages of the quad-core PA have similar designs, but different device counts. The VCO buffer and stages 1, 2, 3 of each PA core have 56 units of main transistors and stage 4 has 60 of them. The DC biases of these stages are 0.6, 0.55, 0.62, 0.85, and 0.92 V, respectively. The DC bias voltages are supplied by external voltages through local RC-filters and are adjusted to maximize P_{sat} and peak Power-Added Efficiency (PAE). In order to achieve maximum P_{sat} for the amplifier, no stage should saturate before its following stages.

The design of the power-splitting transformers for the VCO, VCO buffer, and the PA core stage 1 and 2 (different variations) is depicted in Fig. 5.5.2(a). The secondary loops (the darker traces) are two intertwined one-turn loops. The voltage ratio is 1:1, the same as the turn ratio, but the current ratio is 1:½, due to virtually parallel operation of the two secondary coils. Therefore, the impedance ratio is 1:2. The transformer of the PA core stage 3, Fig. 5.5.2(b), has a pair of secondary loops such that one is placed inside the other. The same analysis for the current and impedance ratios is valid for this transformer too.



(a) (b)

Fig. 5.5.2 Power-splitting transformers with (a) intertwined one-turn secondary loops, with different layout variations, for VCO, VCO buffers, and PA core stage 1 & 2, and (b) one-inside-the-other secondary loops for PA core stage 3.

In the first stage of each PA core, as displayed in Fig. 5.5.3, two pairs of switches are placed in the source nodes of the main and the neutralizing devices. By switching them in and out, the main and the neutralizing devices switch their roles and hence the polarity of the differential output

changes. This feature offers certain distinct capabilities to this 60-GHz WPT system: beam steering and power control. Beam steering is achieved by creating different combinations of polarities for the four outputs of the quad-core PA which will be discussed later in this chapter. Power control is performed by combining different portions of in-phased and out-of-phased inputs by switching in and out different portions of the main and neutralizing devices.

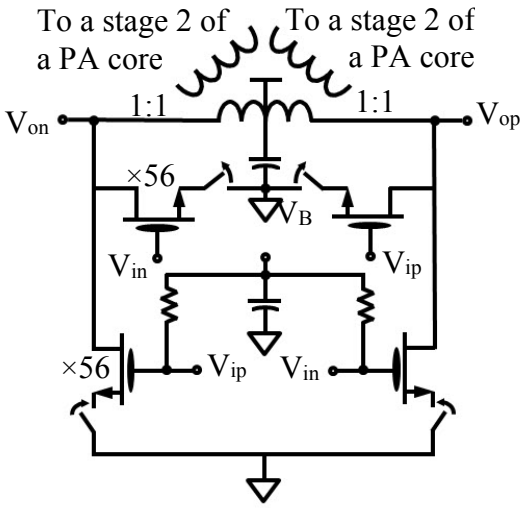


Fig. 5.5.3 Simplified schematic diagram of the stage 1 of each PA core with switchable differential pair devices.

The 8-way differential power-combiner, which is displayed in Fig. 5.5.4, is devised at the end of each PA core. It combines the power of eight pseudo-differential PA units, which comprise the stage 4 of each PA core, and delivers it to one of the four TX antenna inputs. The secondary of the power combiner (the dark-colored trace in Fig. 5.5.4) consists of two similar sets of series loops which are placed in parallel. The primary side has eight one-turn loops in four pairs of two, one inside the other, sharing the center tap connection to the VDD. The turn ratio and the voltage ratio of each primary loop to its corresponding secondary loop is 1:1. Since the eight primary loops are virtually in parallel, at each single-ended input node on the primary side, the voltage and current swings are a quarter of those of the output port and the impedance level is 50 Ω.

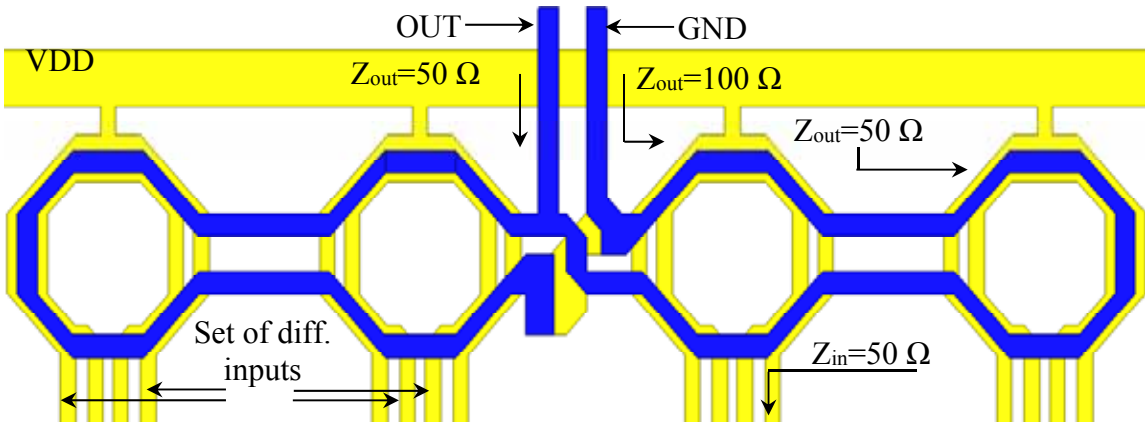


Fig. 5.5.4 The power combiner of the last stage of each PA core.

Fig. 5.5.5 portrays the micrograph of the single PA core which is individually fabricated and characterized. The layout of the power-splitting transformers of stages 1, 2, and 3, the power combiner of stage 4, and ground and supply distribution grids, and the floorplan of the PA core are visible in this figure. The area of the single PA core is 380 µm × 260 µm. Standalone VCO, standalone PA core, standalone quad-core PA, and the full transmitter have been separately

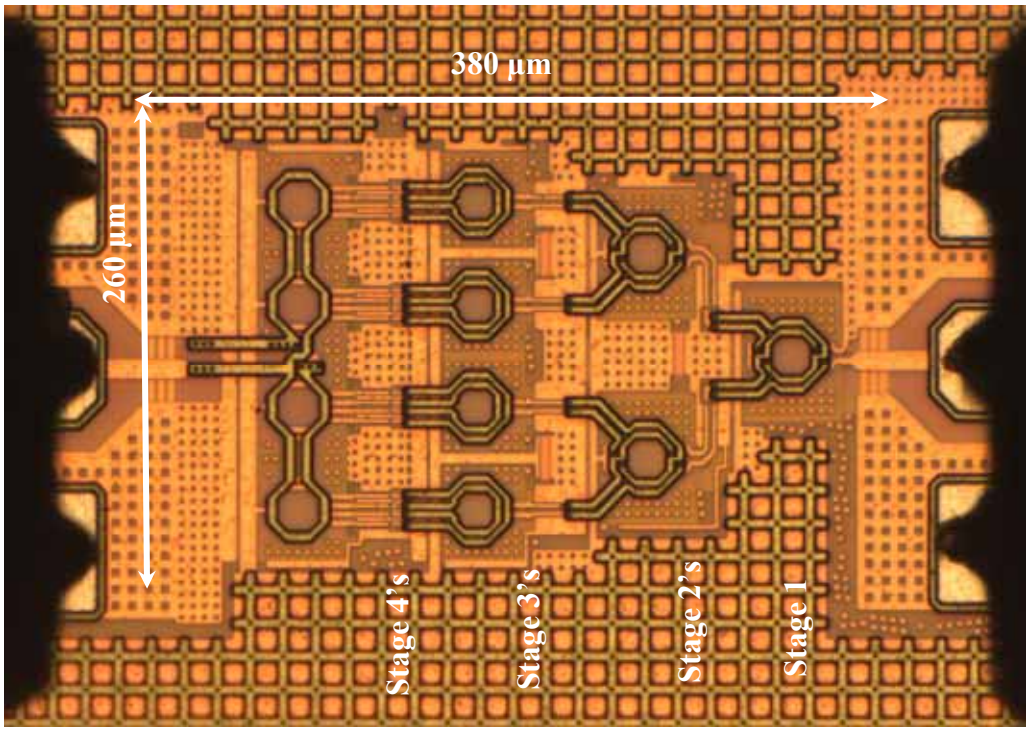


Fig. 5.5.5 The micrograph of the single PA core.

fabricated and individually measured at the mm-wave probe-station. The output of core 2 of the quad-core PA is measured while the RF input signal is delivered through the pad on the right. The DC inputs for the supply, ground, the bias voltages, and the tuning voltages are supplied through the top and bottom DC probe pads. The de-embedded measurement results of the standalone blocks and the full transmitter are in full agreement. As evidenced by Fig. 5.4.2, the full transmitter has 47 transformers and combiners in 6 cascading stages and 4 parallel chains in a binary-tree architecture.

5.6 Beam Steering

As mentioned in earlier in this chapter, the four transmitter outputs can independently change polarities by alternating the roles of the main and the neutralizing devices of the first stage of each PA core of the quad-core amplifier using two pairs of switches at their source nodes. This feature provides the transmitter with the valuable capability of beam-steering with minimal RF

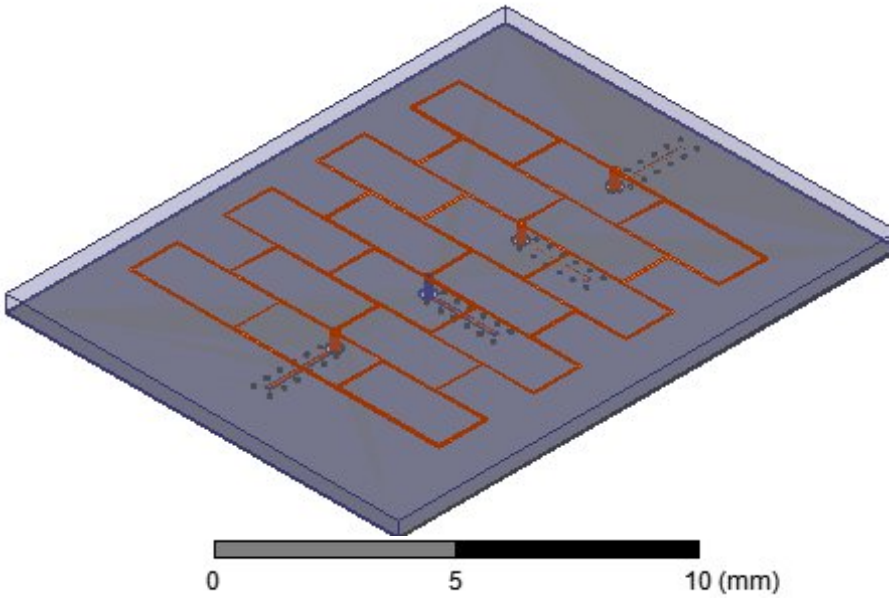
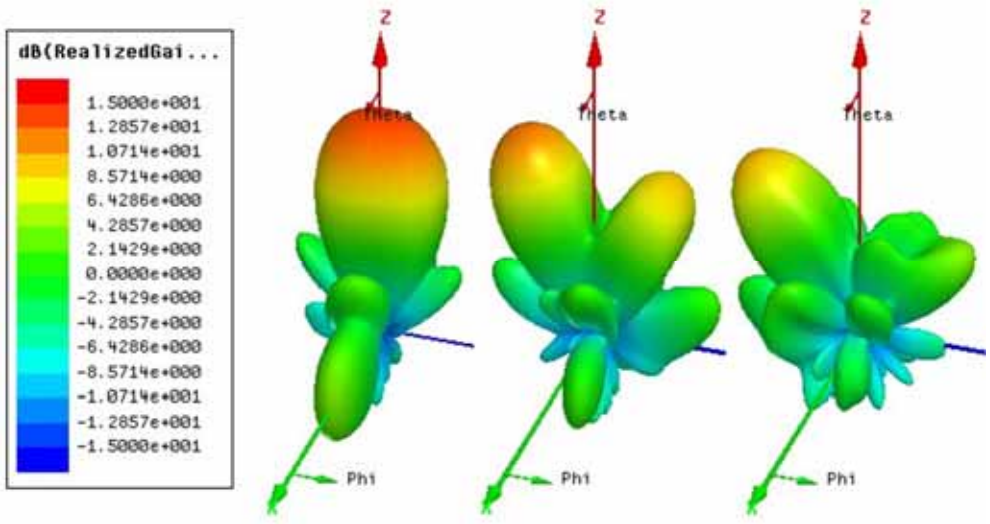


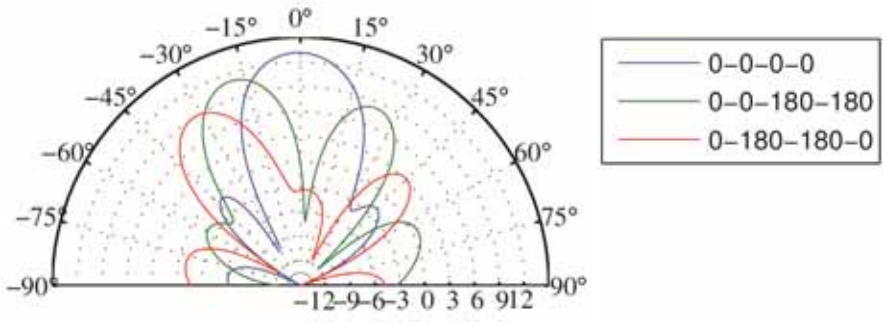
Fig. 5.6.1 The four-port grid antenna of the TX to support beam-steering.

frontend complexity. The four-port grid array antenna which is displayed in Fig. 5.6.1 is designed to realize beam-steering for the TX of this 60-GHz WPT system.

Each combination of polarities for the four TX antenna inputs steers the beam in the broadside direction by a different angle. Fig. 5.6.2 proves the effectiveness of this feature in simulation. This 60-GHz WPT offers an angular range from -35º to 35º at the broadside direction with three different combinations of polarities for the four antenna inputs. The peak gain however changes by ~ 3 dB in different scenarios and the directivity is less effective as the beam steers to the sides.



(a)



(b)

Fig. 5.6.2 The radiation patterns of the TX grid antenna for three different combinations of polarities of the four antenna inputs.

Chapter 6

PERFORMANCE CHARACTERIZATION AND RESULTS COMPARISON

6.1 Rectenna

The integrated rectenna is characterized by measuring its output power and PCE for different resistive loadings and different input power levels. Fig. 6.1.1 compares the results of the measurements, simulations, and the calculations based on the theoretical analysis, equations (14) and (15), for the DC output voltage and PCE with respect to R_L. The maximum PCE of the measurements, simulations, and theory happen around resistive loading of ~ 550 Ω. And the maximum PCE rates are 32.8%, 35.4%, and 34.5% which happen at V_{OUT} levels of 0.82, 0.86, and 0.85 V respectively. The results of the theoretical analysis is fairly close to the simulations and measurements in low R_L and high I_{OUT} region, but for low I_{OUT} region, the error grows since the neglected switching region is larger. In this design $\beta = 16\ mA/V^2$, $V_T = 0.44$ V, $L_B = 0.12$ W/W, and $R_B = 190\ \Omega$.

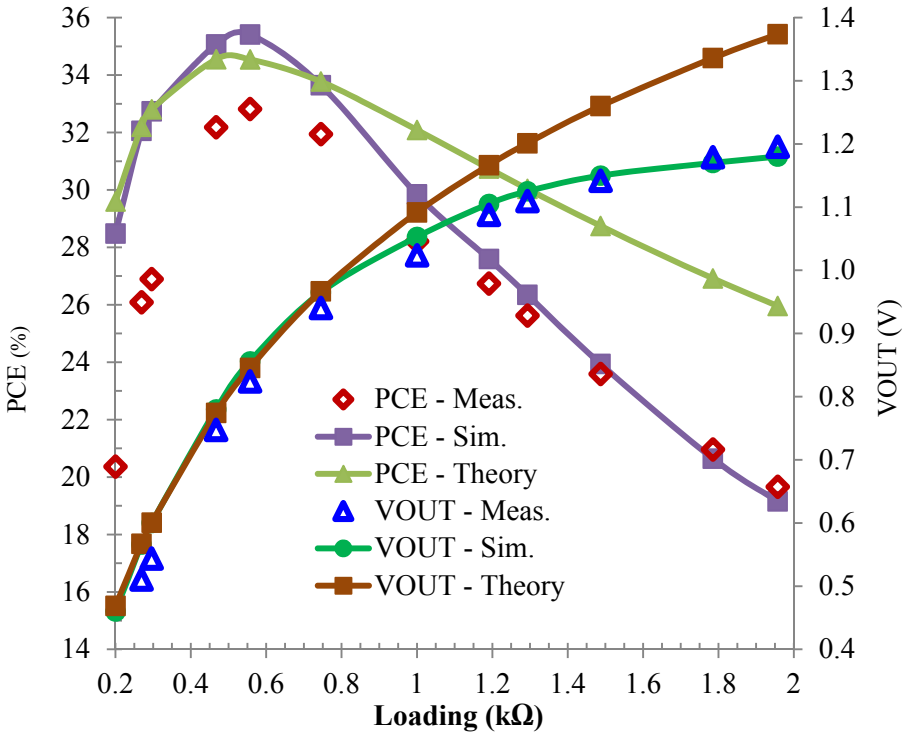


Fig. 6.1.1 The measured, simulated, and calculated PCE and V_{OUT} versus R_L.

Fig. 6.1.2 shows the measured, simulated, and calculated DC output voltage, DC output power, and PCE, with respect to the effective input power at 60-GHz input frequency and 1-kΩ resistive loading. The PCE shows a flat response for any input power level higher than 2.5 dBm. The measured, simulated, and calculated PCE of the rectenna for high input power levels are respectively 28.3%, 30%, and 32.1%. This 60-GHz energy harvester is fabricated using 40-nm digital CMOS process in an area of 90 µm × 110 µm without pads. The amount of the energy that can be stored at the rectenna output depends on the size of the storage capacitor. Larger capacitors store more energy from a given RF input power, but require longer times to charge. Hence, C_{STR} should be adjusted according to the timing and the power consumption specifications of the prospective wireless communication systems which employ this WPT solution.

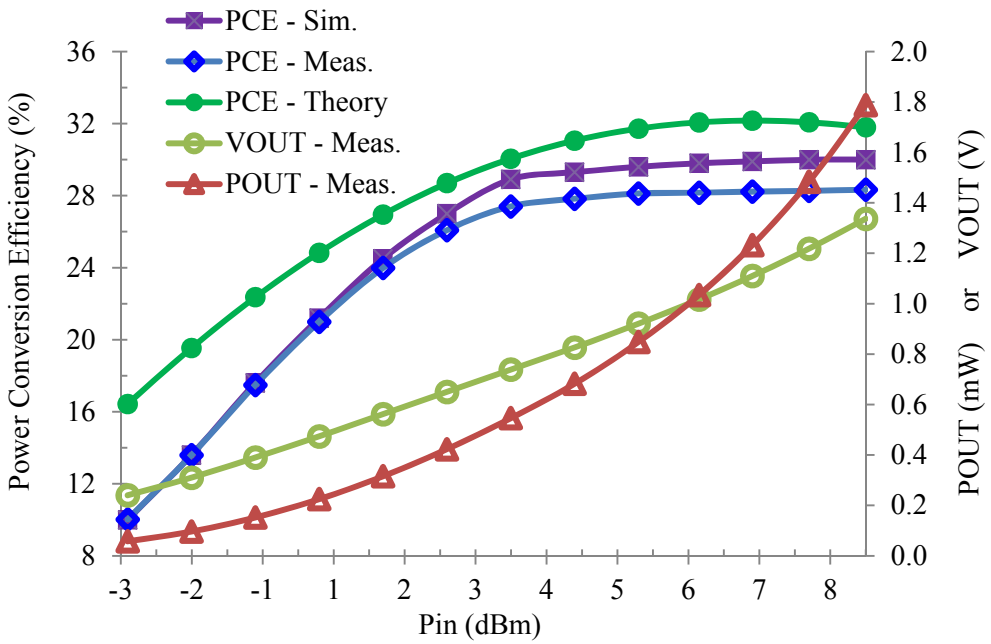


Fig. 6.1.2 Measured, simulated, and calculated V_{OUT}, P_{OUT}, and PCE vs. P_{in}.

Fig. 6.1.3 shows the frequency behavior of the measured rectenna efficiency for different effective and de-embedded input power levels, for the output loading of 1 kΩ.

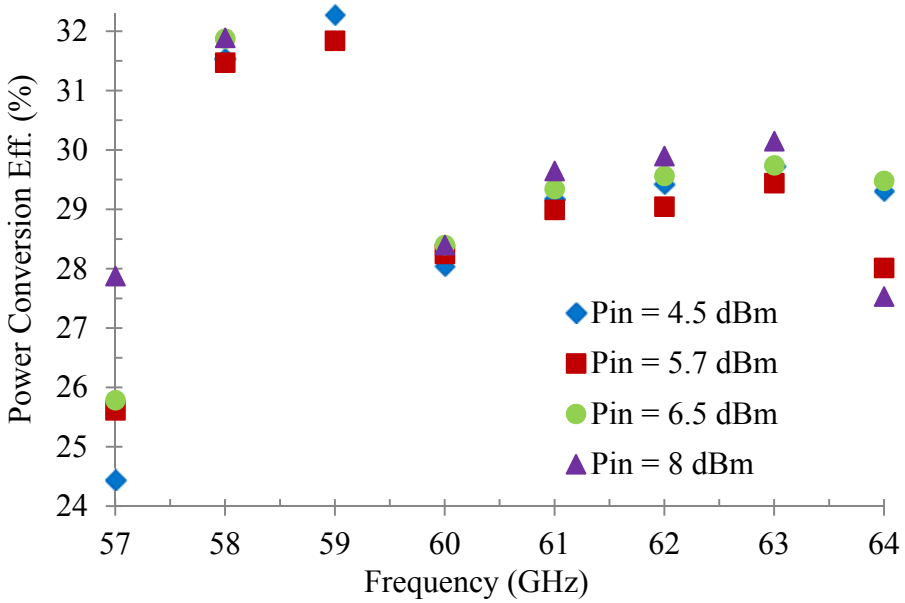


Fig. 6.1.3 The measured rectenna efficiency vs. the input frequency for different input power levels when R_L = 1 kΩ.

Table 6.1.1 compares the results of the mm-wave energy harvesters of the references with this design at the peak PCE conditions. Our condition for peak PCE is R_L = 557 Ω. In terms of the DC output power and PCE our results are remarkably higher than the ones of the references. At R_L = 1 kΩ, we have P_{OUT} = 1.05 mW, V_{OUT} = 1.02 V, and I_{OUT} = 1.03 mA.

TABLE 6.1.1
COMPARISON OF THE CMOS MM-WAVE ENERGY HARVESTING SOLUTIONS

Reference / Specification	This Work	[8] IMS 2014	[9] RFIC 2013	[10] RFIC 2013*	[11] JSSC 2010*
CMOS (nm)	**40**	90	65	65	90
P_{OUT} (mW)	**1.22**	0.091	0.25	0.003	0.019
V_{OUT} (V)	**0.82**	0.65	0.36	0.003	1.6
I_{OUT} (mA)	**1.48**	0.14	0.7	1	0.012
Peak PCE (%)	**32.8**	2	8	7	1.2
P_{in} (dBm)	**5.7**	6.6	5	-14	2
Freq. (GHz)	**60**	94	71	62	45†
Rectifier Topology	**Tuned P/N cross-coupled**	1-stage Dickson multiplier	3-stage inductor peaked	1-stage inductor peaked	10-stage Dickson multiplier

* Design with no antenna. † Designed for 60 GHz, off-tuned to 45 GHz.

6.2 Cascode Energy Harvester

The results of the measurements, simulations and the calculations based on theoretical analysis, the formulae (18) and (19), for the two-stage cascode energy harvester are presented with respect to R_L in Fig. 6.3.1, and with respect to the input power level in Fig. 6.3.2. As evidenced by these figures, the results of PCE and V_{OUT} for the measurements, simulations, and calculations are fairly close to each other. In Fig. 6.3.1, the peak PCE happens at R_L = 745 Ω in simulation, but it happens at R_L = 1 kΩ for the measurements and calculations. The peak PCE is 28.7%, 29.4%, and 31.7% for measurements, calculations, and simulations, respectively. The calculation results have

less errors in the high-current regime and lower R_L. Fig. 6.3.2 shows that the PCE rate saturates with respect to the growth of the input power at around 5.7 and 7.2 for simulations and measurements respectively. These levels are considerably higher than the levels that the PCE of the single-stage harvester saturates at. The peak PCE of the measurements and simulations is 32.2% while the calculation goes as high as 39.2% for 8 dBm input power level and does not show any sign of significant saturation.

6.3 Energy Harvesters Results Comparison

The comparison of the measurement results of PCE and V_{OUT} of the single-stage harvester and the two-stage cascode version shows that at the high-current regime, i.e. lower R_L, the single-stage creates higher PCE and V_{OUT} and at the low-current regime the cascode harvester does a better job of rectification and harvesting. At R_L = 2 kΩ, V_{OUT} and PCE are 1.15 V and 19.7% for the single-state harvester while it is 1.34 V and 24.7% for the cascode version. The PCE curves of

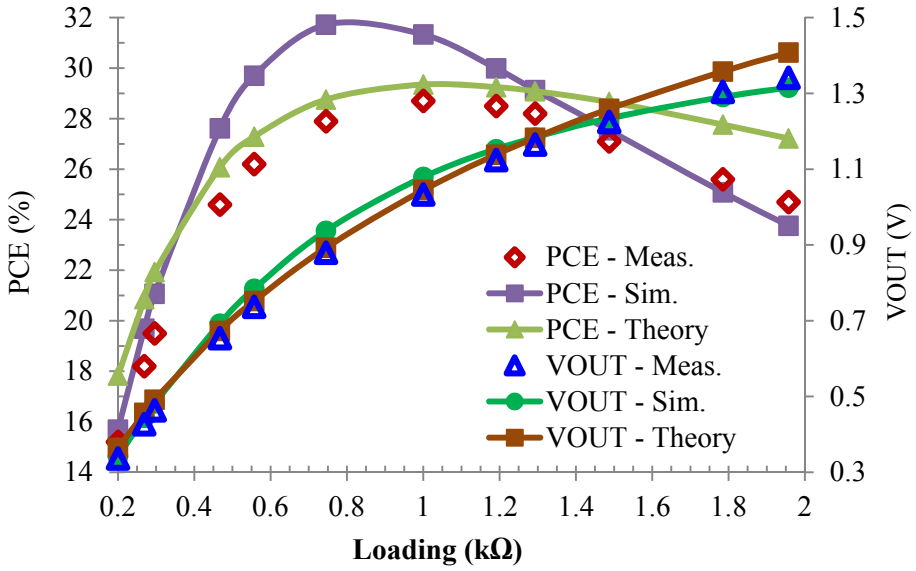


Fig. 6.3.1 The measured, simulated, and calculated PCE and V_{OUT} of the two-stage cascode energy harvester versus R_L.

the single-stage and the cascode version cross at R_L = 1 kΩ. That means for any R_L larger than 1 kΩ two-stage cascode harvester is preferred.

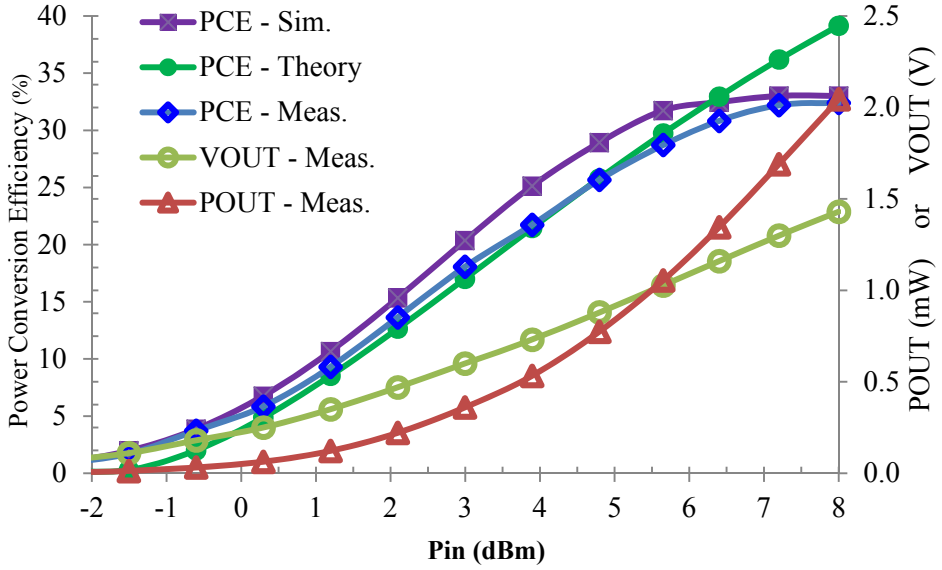


Fig. 6.3.2 Measured, simulated, and calculated PCE vs. Pin plus the measured VOUT, POUT, and PCE for two-stage cascode energy harvester.

Fig. 6.3.3 compares the measurement results of the single-stage power harvester and a cascode version for the PCE and V_{OUT}. In high current single-stage is the superior harvester and

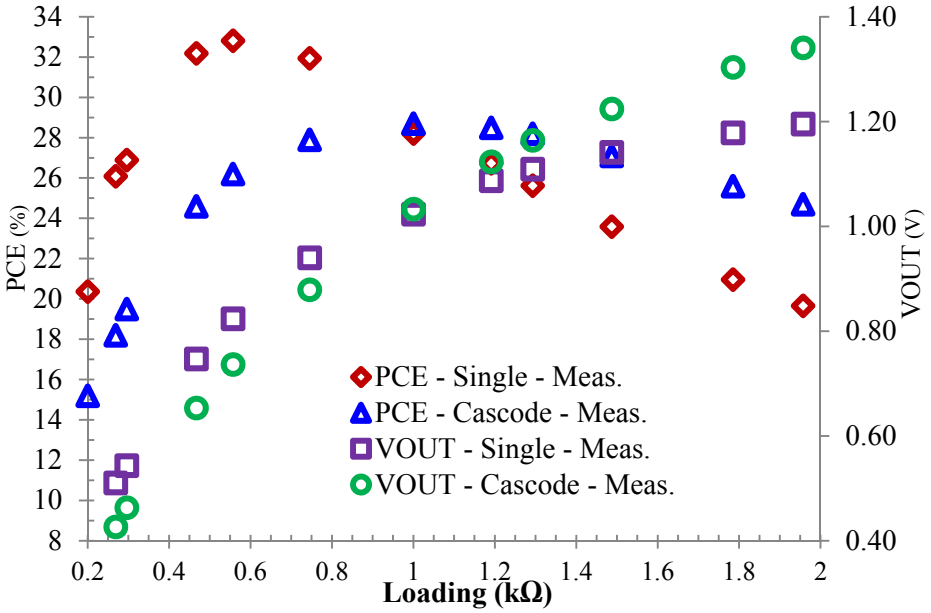


Fig. 6.3.3 The measured PCE and V_{OUT} of the two-stage cascode energy harvester compared to single-stage version versus R_L.

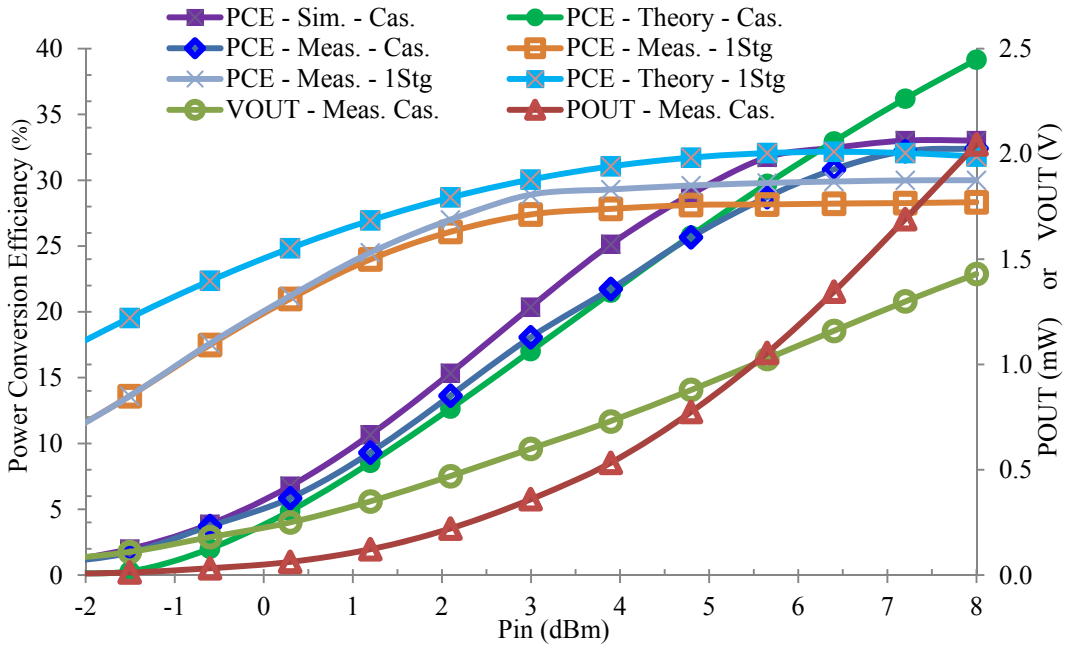


Fig. 6.3.4 The measured PCE and V_{OUT} of the two-stage cascode energy harvester compared to single-stage version versus P_{in}.

in low current regime the cascode version does a better job of producing DC conversion. Fig. 6.3.4 compared the measured PCE and V_{OUT} of the two harvesters with respect to the input power.

Table 6.3.1 compares the results of the mm-wave energy harvesters of the references with the two designs of this work at the peak PCE conditions. In terms of the DC output power and

TABLE 6.3.1
COMPARISON OF THE CMOS MM-WAVE ENERGY HARVESTING SOLUTIONS

Specification \ Reference	This Work: Single-Stage	This Work: 2-Stage Cascode	[8] IMS 2014*	[9] RFIC 2013	[10] RFIC 2013	[11] JSSC 2010
P_{OUT} (mW)	**1.22**	**1.05**	0.282	0.25	0.003	0.019
V_{OUT} (V)	**0.82**	**1.03**	1.13	0.36	0.003	1.6
I_{OUT} (mA)	**1.48**	**1.03**	0.25	0.7	1	0.012
Peak PCE (%)	**32.8**	**28.7**	10	8	7	1.2
P_{in} (dBm)	**5.7**		4.5	5	-14	2
Freq. (GHz)	**60**		94	71	62	45†
CMOS (nm)	**40**		90	65	65	90
Rectifier Topology	**Tuned P/N cross-coupled**		1-stage Dickson multiplier	3-stage inductor peaked	1-stage inductor peaked	10-stage Dickson multiplier

* Results related to the stand-alone harvester design extracted from Fig. 7.
† Designed for 60 GHz, off-tuned to 45 GHz.

peak PCE, our results are significantly higher than the ones in the references. The input power level is limited to 5.7 dBm for the reported results of this work. The results of the single-stage in Table 6.3.1 are for the peak PCE condition of R_L = 557 Ω. But in order to reach 1 mW power, R_L should be 1 kΩ, and in such condition we have P_{OUT} = 1.05 mW, V_{OUT} = 1.02 V, and I_{OUT} = 1.03 mA for the single-stage harvester. For the two-stage cascode harvester the peak PCE happens at 1 kΩ with an output power of 1.05 mW. Results of the harvester of [8] are related to the stand-alone version, extracted from Fig. 7 of this reference.

6.4 Transmitter

Fig. 6.4.1 displays the results of the simulations and the measurements of the P_{sat}, P_{1dB}, and peak PAE for the single PA core with respect to frequency. At 60 GHz, each PA core consumes 625 mA and produces a saturated output power of 18.6 dBm. These figures stand for a peak power-added efficiency of 9.4%. The P_{1dB} is 15.6 dBm and the linear voltage gain of each PA core at 60

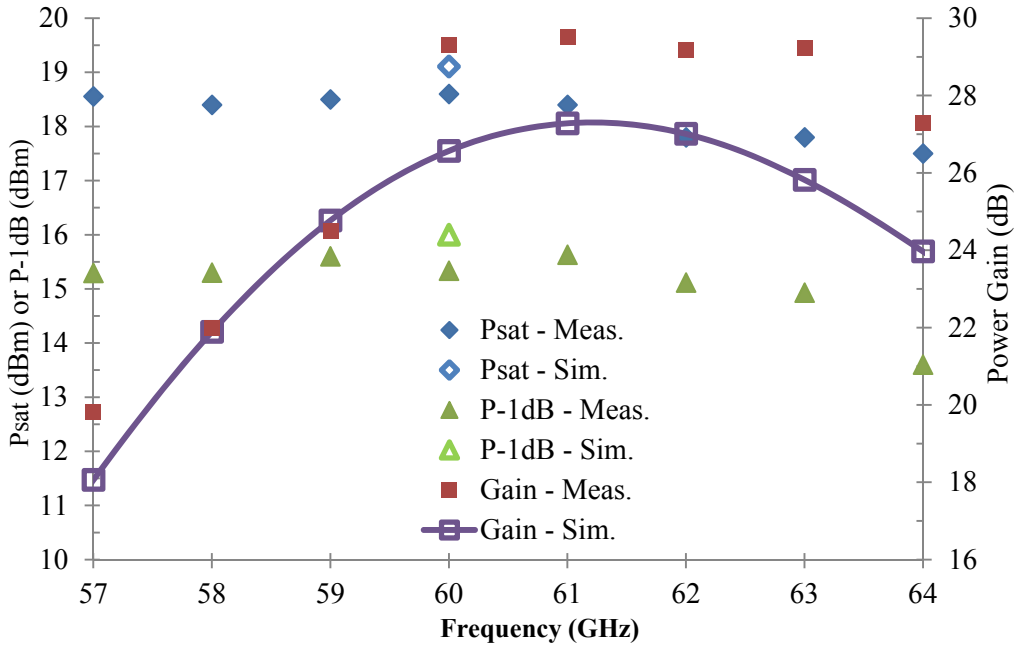


Fig. 6.4.1 The frequency behavior of the P_{sat}, P_{1dB}, and the peak PAE of a PA core, based on simulations and measurements.

GHz is 29.5 dB. P_{sat} and P1dB are fairly flat with respect to frequency, whereas the small signal power gain shows a narrow-band behavior. By using switched-capacitors, the tuning of 5 different stages of the TX are staggered to widen the overall bandwidth. This makes the 60-GHz WPT design more robust and less sensitive to random and systematic mismatches and misalignments between the TX and the RX antennas. These capacitors can help adjusting minor phase differences between different PA core outputs too.

The results of the S-parameter measurements and simulations are presented in Fig. 6.4.2. The S22 results indicate a -10 dB impedance match and the S21 results show a close agreement between simulations and measurements. The quad-core power amplifier consumes a current of 2.56 A which makes the power distribution network throughout the transmitter of vital importance. As seen in Fig. 5.5.5, two enormous power distribution grids consisting of the top two thick metal layers are implemented to supply the transmitter with power and ground signals. By proper floor-planning and careful layout implementation, a total measured resistance of 20 mΩ is achieved for the combined grids of supply and ground. The transmitter produces 24.6 dBm power at 60 GHz with 620 mW/mm^2 power generation density. The achieved power delivery is reasonably close to

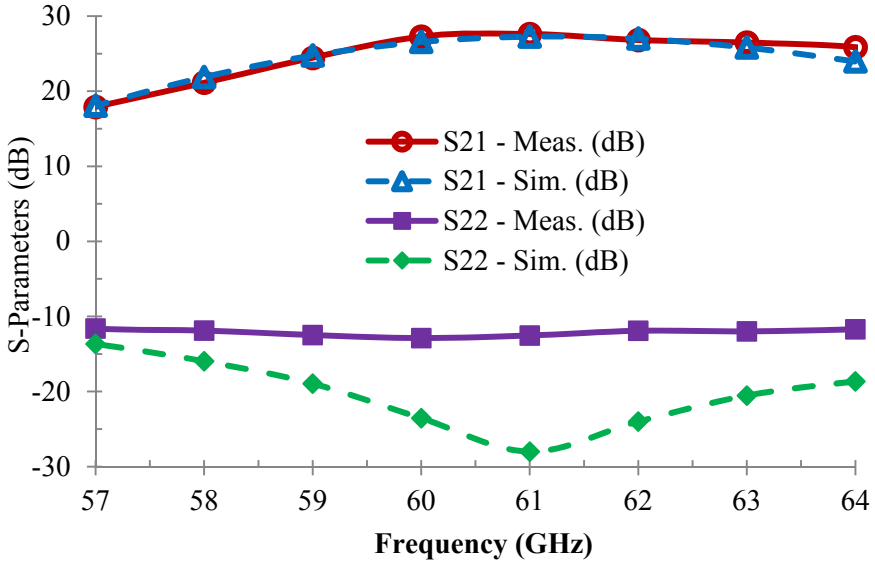


Fig. 6.4.2 The measured and simulated S-parameter results of the PA core.

the 25 dBm targeted specification and the highest reported generated power in digital CMOS technology at 60-GHz based on our study.

In Fig. 6.4.3 the measurement results of the output power, the small signal power gain, and the peak PAE of the single PA core at 60 GHz are summarized with respect to the input power. As illustrated in the figure, the P_{sat}, P_{1dB}, and the peak PAE can be derived from these results which are in agreement with the reported results in Fig. 6.4.1. The results of the simulations and the measurements are reasonably close in all TX figures.

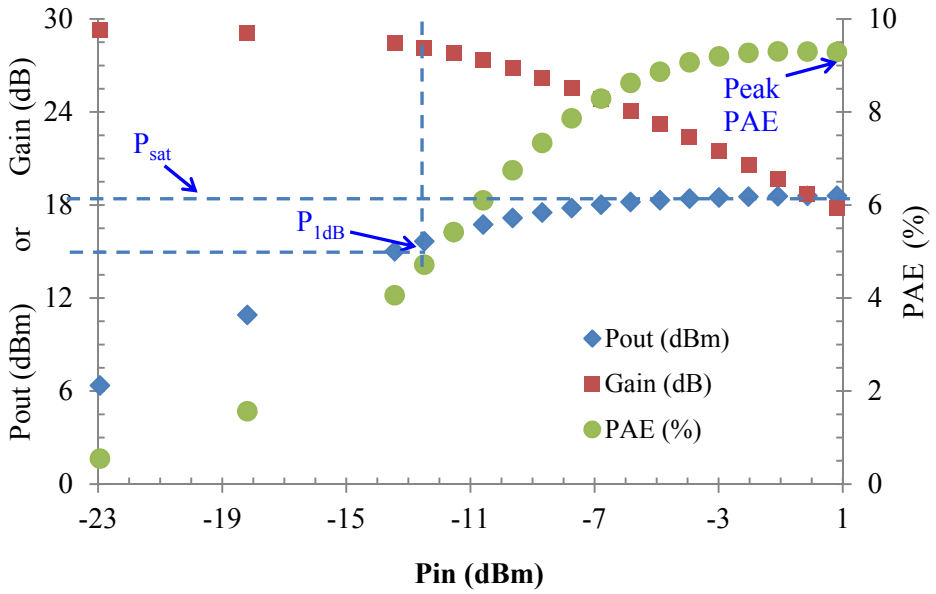


Fig. 6.4.3 The measurement results of the single PA core for the output power, small signal power gain, and PAE, at 60 GHz, with respect to the input power.

Fig. 6.4.4 shows variations of the saturated output power and the peak power-added efficiency of a PA core at 60 GHz with respect to the supply voltage level. With 1.05 V supply, P_{sat} is 17.2 dBm and peak PAE is 8.6%, whereas 1.37 V supply level creates P_{sat} of 19.4 dBm and peak PAE of 9.5%.

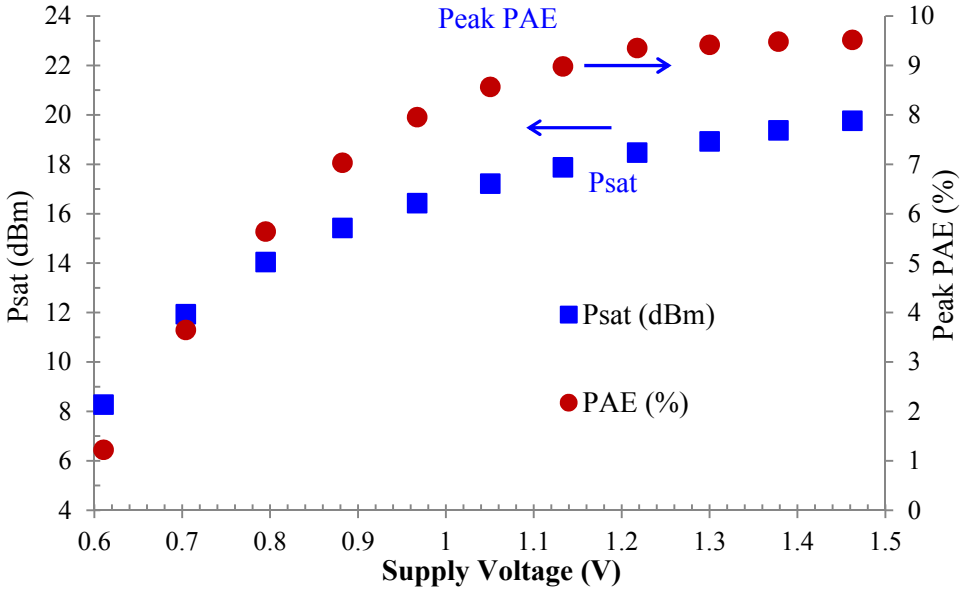


Fig. 6.4.4 The measurement results of the P_{sat} and the peak PAE for the single PA core at 60 GHz with respect to the voltage level of the power supply.

6.5 Power Amplifiers Results Comparison

Table 6.5.1 compares the measurement results of the quad-core PA of this work and other recently published PAs in digital CMOS technology in 60-GHz frequency and higher. P_{sat} and P_{1dB}

TABLE 6.5.1
COMPARISON OF PAS IN DIGITAL CMOS FOR 60+ GHZ FREQUENCY BANDS

Specification \ Reference	This Work	[13] ISSCC 2014	[14] TMTT 2013	[15] RFIC 2013	[16] ISSCC 2012	[17] ISSCC 2011	[18] ISSCC 2010
Feature Size (nm)	**40**	40	65	40	65	65	65
Supply (V)	**1.2**	0.9	2	1.2	1	1	1.2
Frequency (GHz)	**60**	70-86	77	60	79	60	53-68
Max S_{21} (dB)	**35.5**	18.1	20.9	29	24.2	20.3	14.3
P_{1dB} (dBm)	**21.6**	17.8	13	17.0	16.4†	15	11
P_{sat} (dBm)	**24.6**	20.9	15.8	22.6	19.3†	18.6	16.6
Peak PAE (%)	**9.4**	22.3	15.2	7	19.2†	15.1	4.9
PGD* (mW/mm^2)	**620**	650	180	85	100	260	100
Architecture*, Topology*, and Power Combining	**5-stage CS/BT 4x8-way diff.**	2-stage CS/DA 4-way diff.	2-stage CA 2-way diff.	5-stage CS/DA 8-way diff.	4-stage CS 4-way diff.	3-stage CS 2-way diff.	2-stage CA 8-way diff.

* PGD: Power Generation Density, CS: common source, CA: cascode, diff.: differential, BT: binary-tree, DA: distributed amplifier.
† The loss of the on-chip output balun (> 1.6 dB) was de-embedded.

of the transmitter of this 60-GHz WPT system are significantly higher than the references. Their levels of power combining integration varies from 2-way to 8-way differential. The power generation density of the quad-core PA of this work and the PA in [15] are much higher than the PAs of other references. The peak PAE of the quad-core PA is competitive, considering that it is tough to maintain high efficiency and output power simultaneously, since the voltage drop on the power distribution network naturally increases with higher output power levels.

6.6 Full-System Wireless Power Transfer Performance

The full-system measurements are done by measuring the DC voltage at the rectenna output, which is the ultimate output of the entire 60-GHz WPT system, for different RX to TX antenna spacing, different RF frequencies, and different loading resistors. In Fig. 6.6.1, the full-system measurements, simulations, and calculations based on Friis equation, for the DC output power delivery to a 1-kΩ resistor at the WPT output is reported with respect to the spacing between

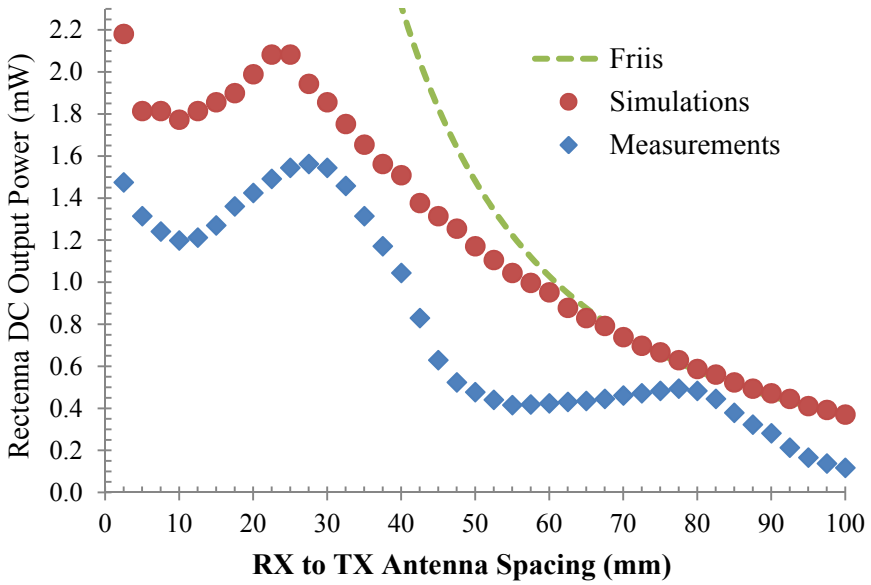


Fig. 6.6.1 The full-system results of the DC output power of the RX for the measurements, simulations, and Friis equation with 1-kΩ loading.

the TX antenna and the rectenna. At 40-mm spacing, the rectified output power is 1.05 mW which is beyond the 1-mW targeted specification for this 60-GHz WPT system. The measurements and simulations are reasonably close in 40 mm spacing range. The differences can be due to alignment of TX and RX antennas, mismatches in the TX antenna elements, and the near-field effects that are not captured by the simulations.

Fig. 6.6.2 shows the dependency of the DC power delivery to a 1-kΩ loading at the WPT output port to the spacing between the TX and RX antennas for different input frequencies. The highest and lowest rectified DC output power levels of the WPT system occur at 59 GHz and 64 GHz respectively based on the full-system measurements.

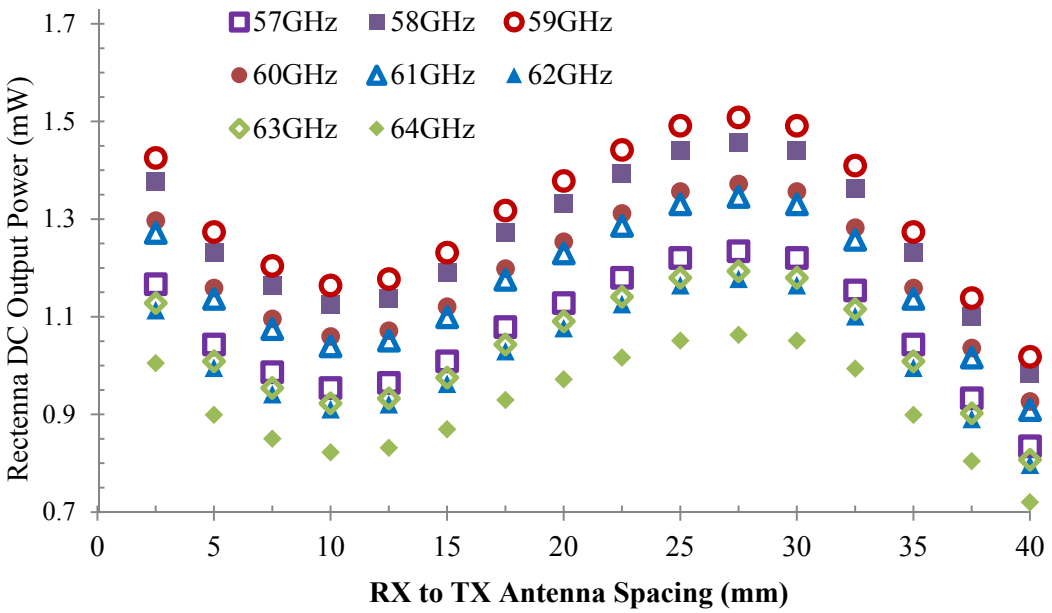


Fig. 6.6.2 The RX DC output power for different frequencies with respect to the RX to TX antenna spacing, based on full-system measurements.

Fig. 6.6.3 shows the frequency behavior of the DC power delivery to a 1-kΩ loading for different spacing between the TX and RX antennas based on full-system measurement data.

Fig. 6.6.4 shows the DC-to-DC efficiency rate in dB for the entire 60-GHz WPT system with respect to the spacing between the grid array antenna of the TX and the rectenna, based on

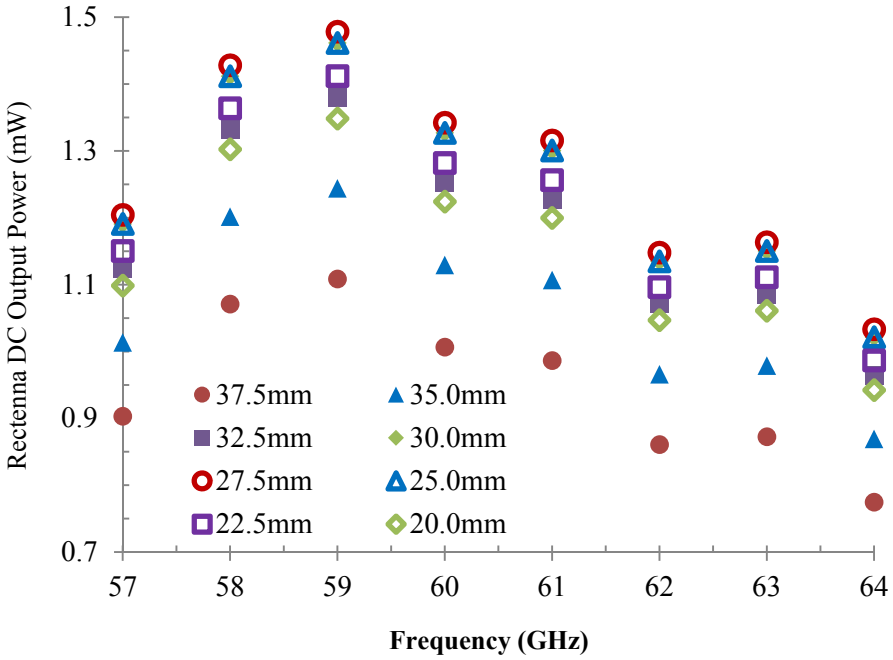


Fig. 6.6.3 The RX DC output power with respect to the input frequency, for different antenna spacing, based on full-system measurements.

the full-system measurements and simulations. There is a maximum of 1.6 dB difference between the measurements and simulations. The DC-to-DC efficiency rates from the power that is consumed from the supply of the transmitter to the DC output power of the energy harvester ranges between -34.8 to -33.3 dB within 40 mm spacing between the TX and integrated RX antennas.

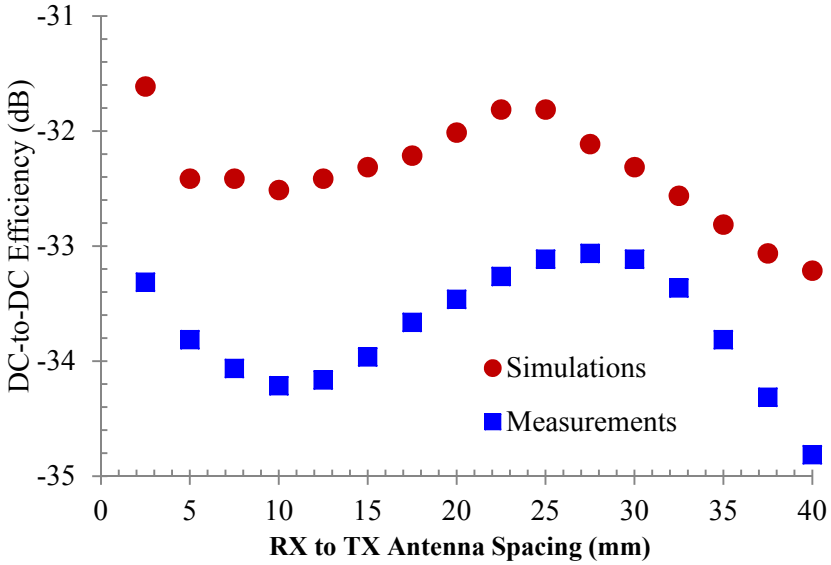


Fig. 6.6.4 The DC-to-DC efficiency rate based on the full-system measurements of the 60-GHz WPT system.

Conclusion

In this work, the entire system of a 60-GHz wireless power transfer solution to support compact smart everyday-objects has been successfully built and characterized. There has not been any precedence in literature for such level of integration for a WPT system at mm-wave frequencies per our study. Achieving high output power at the TX, high RF-to-DC power conversion efficiency rate at the RX, high gain, directivity, and coupling between the TX and RX antennas, and the antenna integration have been accomplished by this 60-GHz WPT solution. The transmitter of this WPT solution achieves the highest reported saturated output power delivery of 24.6 dBm in digital CMOS technology with a peak PAE of 9.4% and a power density of 620 mW/mm^2. The implementation of the TX achieves the highest level of power combing integration ever reported. It uses a 4 × 8-way differential power combining. The rectenna achieves a high RF-to-DC power conversion efficiency of 32.8% for 0.82 V, 1.48 mA and 1.22 mW and 28.3% for 1.02 V, 1.03 mA and 1.05 mW. A pair of compact grid antennas for the TX and RX have been implemented and integrated, using an inexpensive packaging material which makes it possible for this 60-GHz WPT system to support any size of smart device which consumes up to 1-mW power and operates within a proximity of 4 cm. The system can provide output power control and an effective 70° beam-steering range at the transmitter. The full-system measurement results of the

proposed 60-GHz wireless power transfer solution demonstrate the suitability of this mm-wave WPT systems for addressing the demand for wireless power of the battery-less and coil-free smart devices with stringent size constraints of variety of new applications like the Internet of Everything devices.

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