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Electron and Phonon Transport in Silicon Nanostructures

By

Jongwoo Lim

A dissertation submitted in partial satisfaction of the

requirement for the degree of

Doctor of Philosophy

In

Chemistry

In the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Peidong Yang, Chair
Professor Gabor Somorjai
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Fall 2013

Electron and Phonon Transport in Silicon Nanostructures

Abstract

Electron and Phonon Transport in Silicon Nanostructures

By

Jongwoo Lim

Doctor of Philosophy in Chemistry

University of California, Berkeley

Professor Peidong Yang, Chair

Understanding electron and phonon transport in silicon nanostructures is essential for developing advanced electronic and thermoelectric systems. As opposed to electrons that contribute to conduction only near the Fermi surface, phonons show broadband spectrum when they transport heat in silicon. By controlling the dimension and morphology and accounting for characteristic length scale of electrons and phonons, we can engineer their transport properties. In this work, the transport of electrons and phonons in silicon nanostructures was investigated to improve future designs of thermoelectrics as well as nanoelectronics and phononics.

Phonon scattering at boundaries in solid is considered diffusive or specular depending on the wavelength of phonons and the length scales of surface roughness. Thermal conductivity will be at minimum when the phonon scattering is purely diffusive, which is known as the Casimir limit. However, in rough silicon nanowires, the thermal conductivity was found to break the limit. Hence, the role of the roughness parameters (rms, correlation length and a_p, high frequency roughness factor) of etched VLS nanowires was systematically addressed for the suppression of thermal conductivity. The surface roughness, characterized by amplitude (rms) and lateral length scale of roughness (correlation length), is demonstrated to dictate phonon transport in such nanowires down to 5W/mK. More interestingly, high frequency spectrum window of surface roughness close to dominant phonon wavelength (1 – 10 nm) at room temperature was chosen to correlate to thermal conductivity and it showed better the trend with the high frequency roughness factor. Electroless etched (EE) nanowires regardless of their unique irregular morphologies also further have been shown to follow the trend, which indicates sub-diffusive regime of phonon is mainly governed by high frequency surface roughness.

The measurement platforms where both electrical and thermal properties can be characterized for the same holy silicon (HS) ribbon were first developed. It was unclear how the morphology, the doping concentration, and the dimensions affect the transport properties of nanostructures mainly for thermoelectric applications. Hence we developed

this platform for HS ribbons known for enhancing thermoelectric performance. Electron and phonon transport was independently controlled by tuning the neck size, which is the limiting distance between adjacent holes. Owing to accurate thermal conductivity characterization by the superior device design, the necking effect was quantified with a fixed pitch distance. The thermal conductivity in this structure was found below the incoherent phonon scattering regime due to the periodicity in nano-hole array, which possibly opens the new realm of coherent phonon scattering.

Finally, the first demonstration of ballistic phonon transport in the cross-plane direction of silicon has been shown with HS structures. We showed that long wavelength phonons can propagate ballistically up to a few hundred nanometers despite the lateral dimension of 20nm. The fundamental understanding in thermal conduction has direct relevance for heat management in silicon based electronics and thermoelectrics. Furthermore, phononic devices could potentially be realized via ballistic phonon components in silicon nanostructures.

In memory of my cousin, JungTak Woo

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Chapter 1

Introduction

1.1 Introduction to Thermoelectrics : Electrons and Phonons

Thermoelectric materials can convert thermal energy to electrical energy. This conversion process is reversible, so they can also be used as solid-state coolers. In the presence of a temperature gradient, majority charge carriers diffuse from the hot side to the cold side of the material until an electric field is formed to oppose the flow of charge. This electric field creates an open circuit voltage that is linearly proportional to the temperature gradient and is determined by a material's Seebeck coefficient (S=dV/dT).

The world uses approximately 500 quads (1 quad = 10^{15} BTU ~10^{18} J) of energy annually. This energy is mainly used for direct heating or power generation, which typically operates at 30-40% efficiency and loses unutilized energy as waste heat. Thermoelectric modules can convert this waste heat into additional electricity production, which can enhance the overall conversion efficiency. Moreover, these stationary solid-state devices are simple and silent in comparison to other waste heat recovery systems that require moving parts.[1]

Thermoelectric materials are characterized by their dimensionless figure of merit (*ZT*):

$$ZT = \frac{S^2\sigma}{k_e + k_{ph}}T \tag{1}$$

where T is the absolute temperature, σ is electrical conductivity, and k_e and k_{ph} are electronic and lattice contribution to thermal conductivity, respectively. In order to maximize the ZT value, it is desirable to have a large electrical conductivity, large Seebeck coefficient, and a low thermal conductivity. However, each parameter is dependent on one another, which makes the design of highly efficient thermoelectric materials challenging.

The Boltzmann transport equation for electron transport in solid state materials can simplify the Seebeck coefficient and electrical conductivity to[2]

$$S = \frac{1}{eT} \frac{\int \sigma(E)(E - E_f)dE}{\int \sigma(E)dE} \tag{2}$$

$$\sigma = \int \sigma(E)dE \tag{3}$$

We introduce the "differential" conductivity as

$$\sigma(E) = q^2\tau(E)v^2(E)n(E)\left(-\frac{\partial f_{eq}}{\partial E}\right) \tag{4}$$

where *q* is the unit charge of each carrier, *τ(E)* is the energy dependent scattering relaxation time, *n(E)* is the energy dependent carrier density, *T* is the absolute

temperature, E_f is the Fermi energy, f is the carrier probability distribution function, and f_{eq} is distribution function at equilibrium. $\sigma(E)$ is a measure of the contribution of electrons with energy E to the electrical conductivity. The Fermi "window" factor ($-\delta f_{eq}/\delta E$) is a bell-shape function centered at $E=E_f$ with a width of $\sim K_B T$. At a finite temperature, electrons near the Fermi level are responsible for electrical conduction. In this picture, the Seebeck coefficient is the average energy transported by the charge carriers.[2] A larger Fermi window and an asymmetric density of states with respect to the Fermi energy implies a larger $\sigma(E)$ and S, respectively. Figure 1.1a qualitatively illustrates the origin of the thermoelectric effect. Under a temperature gradient, hot electrons above the Fermi level will flow toward the colderer region, cold electrons below the Fermi level will flow toward the hotter regien. If the density of states is equal, there will not be any charge flow. However, since the parabolic nature of density of states (DOS) in bulk suggests that there are more states above the Fermi level, the net flow of electrons will be from the colder region to the hotter region for n-type semiconductors. This asymmetry in the density of states is more pronounced for low doping levels as shown in figure 1.1b, which will increase the Seebeck effect. However, the electrical conductivity will decrease with this improvement in the Seebeck coefficient. The abrupt changes in DOS observed in quantum wells or quantum wires will be discussed later.
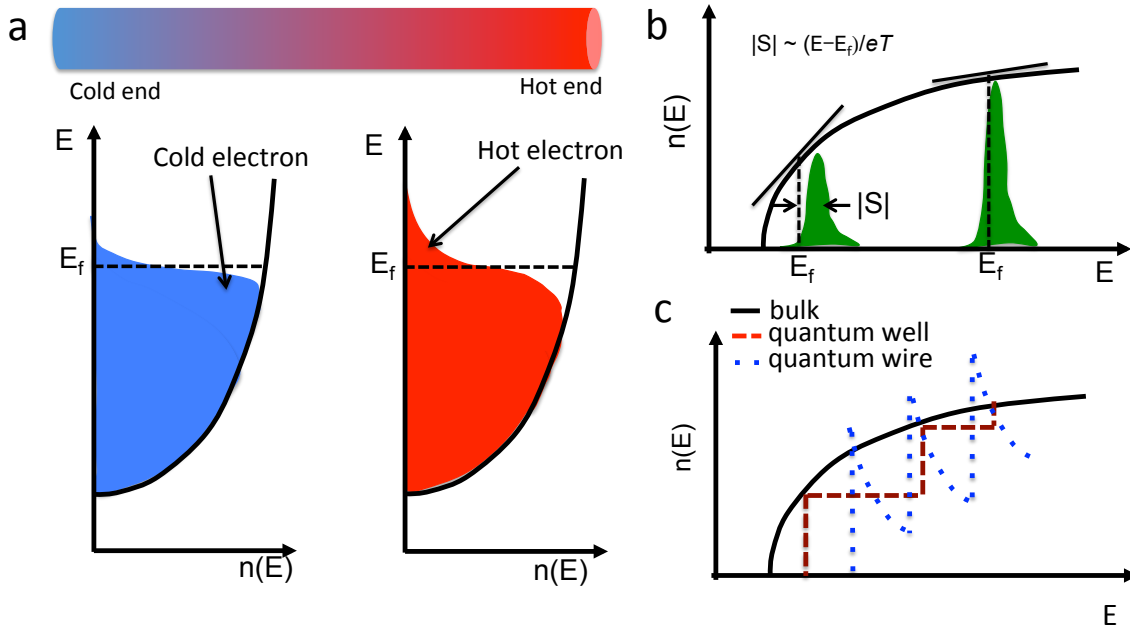
Figure. 1.1 Schematic illustration of thermoelectric effect. (a) origin of the Seebeck effect in parabolic density of state (b) the Seebeck effect depending on 'asymmetry' of density of state (c) Density of states in quantum confinement regime.

The conversion efficiency of thermoelectric generators is calculated by:

$$\eta = \eta_c \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+T_c/T_h} \tag{5}$$

where η_c is the Carnot efficiency, and T_c and T_h are the temperature of the cold and hot regions, respectively. The total efficiency as a function of temperature and ZT are plotted in figure 1.2. The thermoelectric community believes that a ZT>3 is needed for these solid-state device to be competitive with traditional mechanical energy conversion systems.[3,4] However, the best known thermoelectric materials such as Bi_2Te_3, PbTe, and Si/Ge alloys have only produced ZT values of ~1 at 300K, 700K, and 1000K, respectively and their use is limited due to poor efficiency, poor stability, and large manufacturing costs. In the last decade, there has been a large effort to increase the ZT value through heavy element alloying or point defect/interface engineering, but neither of these strategies have reached a *ZT* that is greater than 3 yet.[5-10]
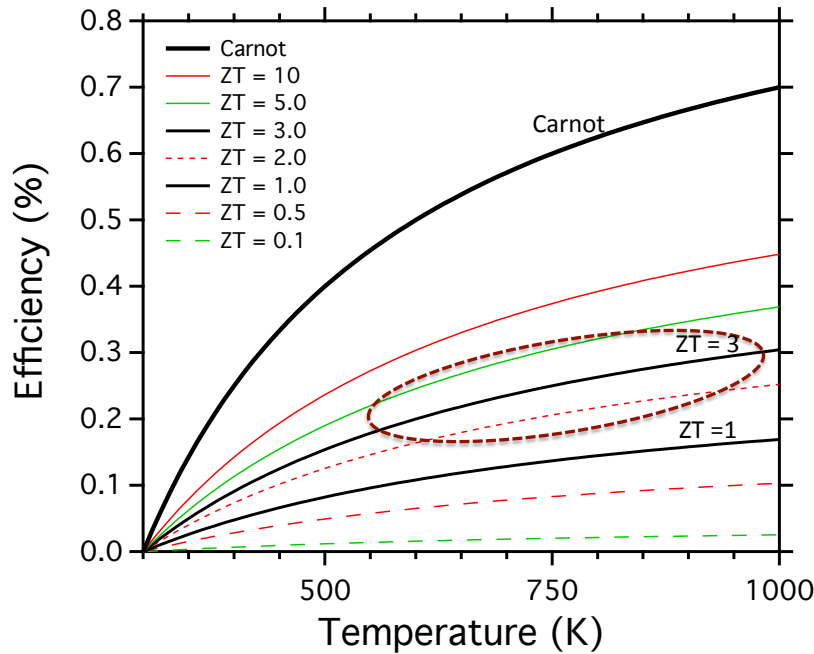
Figure 1.2 Total thermoelectric efficiency with temperature for specific ZT values. Red circle indicates our targeting ZT

1.2 Strategies in thermoelectrics : toward high ZT

1.2.1 Nanowires

The nanowire geometry has two principal advantages for thermoelectrics. First, the power factor ($S^2\sigma$) can be increased when nanoscale diameters introduce quantum confinement effects that modify the density of states.. Second, phonon scattering off the radial boundary can effectively reduce the thermal conductivity below the values observed in bulk materials. In 1993, Hicks and Dresselhaus predicted that an electronic band structure tuned by quantum confinement effects in nanostructures should dramatically increase the power factor ($S^2\sigma$) for quantum wires or quantum well

structures. For example, a *ZT* of14 was predicted for Bi_2Te_3 quantum wires.[11-13] In a 1-D structure, the sharp increase in the DOS near the Fermi level may enhance the electrical conductivity and the 'asymmetry' of its band structure,leading to a larger Seebeck coefficient.(Figure 1.2c)[2]Additionally, modifying the band structurel by introducing resonant states or high valley degeneracy can also enhance the power factor, but these approaches have not been applied to nanowire to the best of my knowledge.[14-16]

While observing an enhancement in the power factor in nanowires has been limited, it is clear that the thermal conductivity decreases in nanowires via enhanced phonon boundary scattering. The thermal conductivity of materials is given by

$$k = \int \frac{C(w)v(w)l(w)}{3} dw \qquad (6)$$

where *w* is phonon frequency, *C(w)* is frequency-dependent heat capacity, *v(w)* is group velocity, and *l(w)* is mean free path (*mfp*) of phonons. Unlike electrons, the wavelengths of heat carrying phonons are spectrally broadband, and, for example in bulk silicon the *mfp* of phonons ranges from roughly 10nm to 10μm due to their frequency dependent relaxation rate. A recent first principles calculation revealed that approximately 90% of heat conduction is conducted by phonons with a mfp of 40nm – 10μm.[17,18] Due to this relatively long *mfp*, bulk silicon, with a conductivity of ~150 W/mK at room temperature, is one of the most thermally conductive materials.

In fact, the power factor of an optimally doped silicon is comparable to that of an optimally doped Bi_2Te_3. Furthermore, because the bandgap of Si (1.1 eV) is larger than that of Bi_2Te_3, the power factor does not drop at higher temperatures. In 2008, Boukai *et al*. and Hochbaum *et al*. demonstrated that silicon nanowires could be an efficient thermoelectric material.[19,20] Boukai e*t al*. observed a ZT value as high as 1.0 for thin silicon nanowires (10 – 20nm) prepared by the superlattice nanowire pattern transfer (SNAP) technique due to an enhanced Seebeck coefficient. [20] The authors explained that the thin nanowire geometry confines phonons, which enhances the Seebeck coefficient via phonon drag. Hochbaum *et al*. measured a *ZT* value as large as 0.6 for rough silicon nanowires at room temperature, which had thermal conductivity values as low as the amorphous limit. The rough silicon nanowires were prepared via an electroless etching method (EE).[19] Because phonon scattering at the smooth surfaces of VLS nanowires is known to be diffusive (close to the Casimir limit), conventional models which consider phonons as particles cannot explain this sub-diffusive phonon transport regime from the enhanced boundary scattering.[21,22]A number of research groups proposed models to explain these phenomena; however, their validity is still a matter of debate.[23-30]

Nanowires have been made from various elements such as Si-Ge, metal silicides ,and Bi/Pb charcogenides. While the electrical properties of many of these wires are poor due to low crystal qualities, the thermal conductivity reduction was consistently observed.[31-41] Specifically, the nanowire geometry is clearly advantageous for the Si-Ge alloy. According to Rayleigh scattering theory, atomic scale defects in Si-Ge alloy bulk systems scatter short wavelength phonons effectively. In Si-Ge alloy nanowires, long wavelength phonons scatter at the nanowire boundaries as well, which decreases the thermal conductivity even further.[37,39-41]

In summary, even though nanowires possess several theoretical advantages for thermoelectric applications, synthetic challenges still limit the figure of merit, which remains lower than to their bulk counterparts. Improved control of crystallinity, defects,

and dopants is still required to improve nanowire power factors, especially for thinner wires. Interestingly, it has been shown that thermal conductivity can be suppressed in various nanowire structures including rough silicon nanowires. Although the underlying mechanism is not well understood, roughened nanowires represent a potential advantage of the nanowire geometry and will be an important consideration when designing improved nanowire thermoelectric devices in the future.

1.2.2 Other Structures

Predicted by Dresselhaus *et al.*, quantum well structures can lead to a large increase in ZT due to an enhanced Seebeck effect.[12] Superlattices have been widely studied\ for many compositions, and a giant Seebeck effect has been shown for $SrTiO_3/SrTi_{0.8}Nb_{0.2}O_3$, where the active channels ($SrTi_{0.8}Nb_{0.2}O_3$) are thinner than 3nm. [9,42-44] However, Increasing scattering rate of charge carriers in these small channels will restrict the power factor ($\sigma 2S$). Therefore, the increased ZT values found in most of superlattice films such as Bi_2Te_4/Sb_2Te_3, $PbTe/PbSe_xTe_{1-x}$, Si/SiGe, and $GaAs/Al_xGa_{1-x}As$ were mainly ascribed to a reduced cross-plane thermal conductivity. Traditionally, for thermoelectric applications, thermal conductivity is suppressed by alloying, which introduces atomic scale defects to scatter phonons. However, there can be a number of reasons for the reduced thermal conductivity in superlattice structures. Phonons may scatter at interfaces due to dislocations or an acoustic mismatch between two compositions. Furthermore, the phonon dispersion curve can be tuned by the periodicity of the supperlatice, which may reduce the group velocity or create a phononic stop band. It has also been demonstrated that cold electrons can be effectively filtered by an energy barrier layer ($1\sim10 \times k_bT$) such that only hot electrons can be transmitted, which enhanced power factors for superlattices such as $In_xGa_{1-x}As/Al_yIn_zGa_{1-y-z}As$. [43]

Other types of nanostructures such as imbedded nanodots in solid matrices and sintered polycrystalline materials with nanoscale grains have been developed from mixtures of heavy. [6,7,10,45-50] The enhanced thermoelectric property is attributed to the decrease in lattice thermal conductivity rather than an increase in the electrical power factor. With these embedded nanoscopic features, phonons start to efficiently scatter at defects, nanodots, and interfaces while electron mobility remains relatively preserved. This phenomena is observed because phonons are broadband and their scattering properties heavily depend on their wavelength and the size of scattering sites. The Rayleigh scattering picture argues that the scattering time, τ, scales as d^6/λ^4, where d is the nanodot diameter and λ is the phonon wavelength. Hence, atomic defects can effectively scatter short wavelength phonons and mid-long wavelength phonons can efficiently scatter at nanodots. [4]

Power factors can also increase by modifying the electronic band structure.[16] Larger effective band masses are disadvantageous to the electrical conductivity because the mobility ($\mu = \tau e/m_i^*$) is inversely proportional to intertial mass, m_i, and moreover, the scattering time, τ, also decreases with effective band mass, m_b^* when the charge carriers are predominantly scattered by phonons. [16] Because $m_d^* = N_v^{2/3}m_b^*$, the valley degeneracy, N_v, can increase by converging bands from different energy levels with m_b^* and the high degeneracy will increase the density of states effective mass, m_d^*. Further, assuming a negligible inter-valley scattering, the effective mass will be maintained at m_b^*

while producing a large electrical conductivity. The Snyder group showed that the valence band in $PbTe_{1-x}Se_x$ alloy can effectively converge to $N_v = 12$ at 800K, leading to a ZT value of 1.8.[15] The band structure can also be tuned by introducing resonant doping states. These additional states in the host band increases the total DOS and decreases the Femi level for a given carrier concentration, which serve to increase the Seebeck coefficient. Currently, the materials of highest interest are Tl and Al doped PbTe and PbSe systems, respectively. [14,16]

1.3 Thermoelectric Property Measurement Techniques

There has been a significant effort toward characterizing the thermoelectric properties of single nanowires. The measurements of the electrical conductivity and the Seebeck coefficient of single nanowires are relatively common and they can be measured by conventional photolithography techniques such as 4-point probe electrodes, which can also work as thermometers for the Seebeck coefficient measurement. The thermal conductivity measurement, however, is more challenging because only the heat conduction through the nanowire should be probed without the influence of parasitic environmental heat convection or radiation. The Majumdar group at Berkeley first pioneered the measurement platform and it has been refined and optimized with different measurement schemes since 2003.[51] Briefly, two suspended membranes with platinum resistive thermometers (PRTs) are thermally isolated and bridged by a nanowire, which is the only heat channel between the two membranes. (figure1.3)
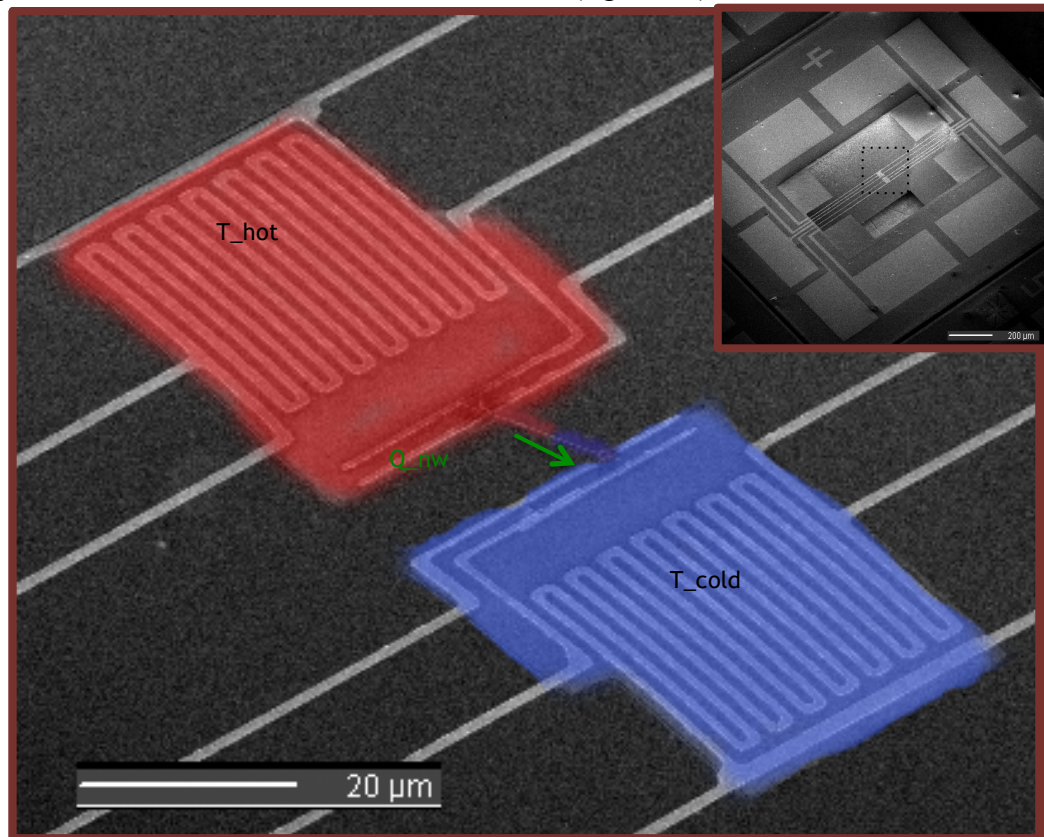
Figure 1.3. Microfabricated thermal and thermoelectric property measurement device with a nanowire suspended between the membranes. Inset shows a low magnification image of the device.

A DC current (5-10 µA) is passed through the PRT on one of the membrane to generate a temperature, ΔT_h, above the ambient temperature, T_0, which induces a heat flow Q_nw through the nanowire to heat the other membrane to ΔT_s. At the same time, a much smaller AC current (~0.5 µA) is passed through the PRTs on the both membrane to measure 4-probe electrical resistance, which is then calibrated to temperature given that the electrical conductivity is linearly proportional to temperature. After accounting for the heat loss through the identical supporting legs to environment and solving thermal resistance circuit, the thermal conductance through the nanowire is given by (figure 1.4)

$$G_s = G_b \frac{\Delta T_s}{\Delta T_h - \Delta T_s}$$

$$G_b = \frac{Q_h + Q_L}{\Delta T_h + \Delta T_s}$$

where G_s and G_b are the thermal conductance of nanowire and supporting legs, respectively. Q_h and Q_L, the Joule heat generated by DC current on the heating PRT and the two supporting legs, respectively, can be calculated from the DC current and the voltage drops across the PRT and the supporting legs[51]

AC current (~500nA) $Q_h + 2Q_L = Q_1 + Q_2$

DC current (5~10µA) $Q_2 = G_b(T_s-T_0) = G_s(T_h-T_s)$
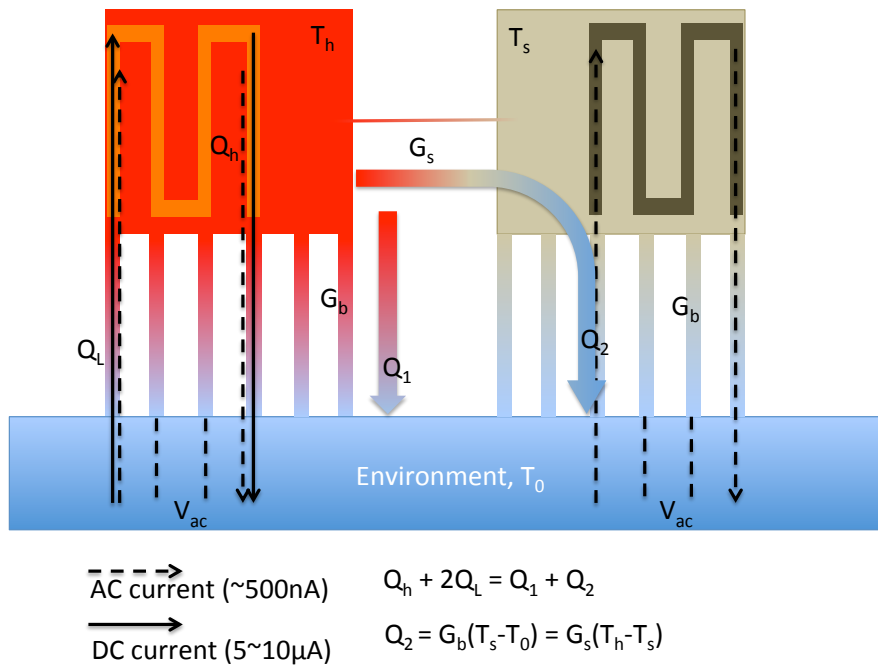
Figure 1.4. Schematic diagram of experimental setup. Redrawn based on figue 4 in ref. 51.[51]

The conductance in the measurement platform inherently includes the thermal contact resistance at the nanowire and device junction. Rs = Rnw + Rc where Rs, Rnw, and Rc are total thermal resistance calculated from the platform and thermal resistance of

nanowire and contact, respectively. There are two general ways to minimize the contribution of thermal contact resistance. First, a thermally conductive platinum/carbon composite is deposited on both ends of the nanowire using electron beam induced deposition (EBID). Second, the nanowire geometry is carefully selected to increase the thermal resistance of the nanowire itself. We experimentally estimate the contact resistance by plotting the total thermal resistance with respect to nanowire length, which is shown below.
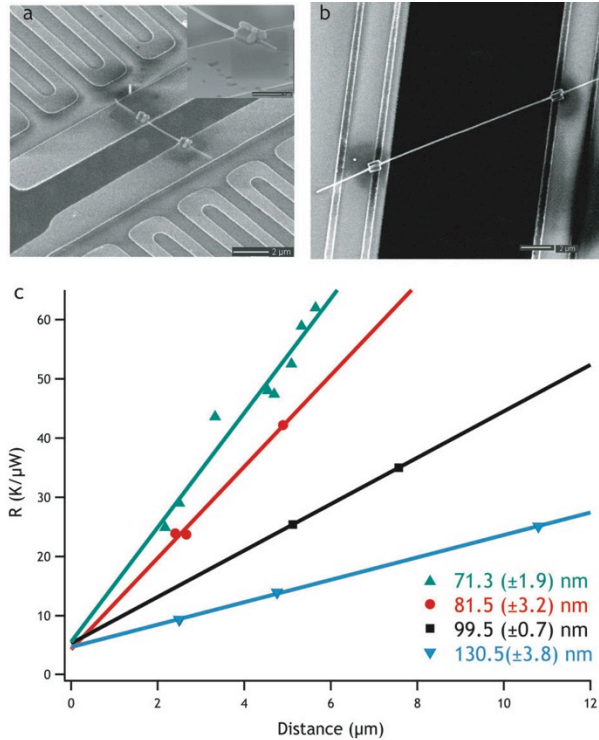
Fig 1.6 (a,b) SEM images of VLS SiNWs with various lengths on prefabricated MEMS devices for thermal conductivity measurement. The inset of (a) is a magnified image of a Pt/C composite on the end of SiNW. (c) Thermal resistance of VLS Si nanowire with various length and diameter. The intercept on Y axis indicates an average contact resistance ~ 4.5 K/uW, which is less than 10% of the measured value for VLS NWs with 71.3 nm diameter and 5 um length. Reproduced from J. Lim et. al.[52]

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Chapter 2

Impact of Surface Roughness on Thermal Conductivity of Silicon Nanowires below the Casimir Limit

Although it has been qualitatively demonstrated that surface roughness can reduce the thermal conductivity of crystalline Si nanowires (SiNWs), the underlying reasons remain unknown and warrant quantitative studies and analysis. In this work,vapor-liquid-solid (VLS) grown SiNWs were controllably roughened, and then thoroughly characterized with transmission electron microscopy (TEM) to obtain detailed surface profiles. Once the roughness information (root mean square (rms), σ, correlation length, L and power spectra) was extracted from the surface profile of a specific SiNW, the thermal conductivity of the same SiNW was measured. The thermal conductivity correlated well with the power spectra of surface roughness, which varies as a power law in the 1-100 nm length scale range. This correlation was also verified to electroless etched (EE) SiNWs, suggesting that phonon transport in SiNWs is governed by the characteristic power spectra of surface roughness These results suggest a new realm of phonon scattering from rough interfaces, which restricts phonon transport below the Casimir limit. Insights gained from this study can help develop a more concrete theoretical understanding of phonon – surface roughness interactions, as well as aid the design of next generation thermoelectric devices.

2.1 Introduction

Recent studies have employed various methods to suppress phonon propagation as a strategy towards realizing efficient and cost-effective thermoelectric devices.[1-6] Chiritescu and Cahill et. al. demonstrated that disordered layers of WSe_2 exhibited dramatically low thermal conductivity due to interface phonon scattering from random stacks of adjacent layers[4], while Kim et. al. were able to reach a thermal conductivity below the 'alloy limit' by embedding ErAs nanoparticles in crystalline $In_{0.53}Ga_{0.47}As$ to efficiently scatter a broad range of phonons at the heterogeneous interfaces.[5] While those studies used relatively exotic materials, Chen et et al. showed that even nanostructured bulk (nano–bulk) Si/Ge alloys exhibit reduced thermal conductivity via increased phonon scattering at grain boundaries.[6]

Similar to nano-bulk Si/Ge alloys, single-crystalline Si nanowires (SiNWs) have also shown depressed thermal conductivity due to phonon scattering from the nanowire surface. However, unlike previously mentioned systems, all of the factors that can influence phonon propagation have not been quantitatively studied. It has previously been reported by Li et. al. that when the diameter of smooth single-crystal SiNWs that are grown by the vapor-liquid-solid (VLS) process reduces below 150 nm, the thermal conductivity is significantly lower than the bulk value, and can closely follow predictions based by Boltzmann transport theory assuming diffuse boundary scattering as the dominant phonon scattering mechanism.[7] Specifically, the thermal conductivity at 300 K ranges from 40 to 9 W/m-K for SiNWs with diameters of 115nm to 22nm, respectively. To help explain this dependence, Mingo et. al. proposed that despite the smooth surface nature of VLS SiNWs, phonon-surface boundary scattering is diffusive rather than specular.[8] This diameter-limited thermal conductivity based on diffuse phonon scattering at surfaces follows what has been described as the Casimir limit. Although the smooth VLS SiNWs show thermal conductivity reduction, roughened SiNWs produced by electroless etching of Si wafers (EE-SiNWs) were found to produce even lower thermal conductivity, as low as 1.6 W/m-K for a SiNW of 56 nm diameter at 300K.[1] This surprising result of thermal conductivity below the Casimir limit cannot be explained and warrants more quantitative study.

While the exact mechanism of phonon-roughness scattering is not clearly understood, there have been various attempts at developing theories behind such interactions.[9-16] One such study by Martin et al. employed the Born approximation toward phonon scattering to explain the large suppression in thermal conductivity.[9] They proposed that the roughness causes an alteration in the phonon dispersion and used perturbation theory to explain the enhanced scattering. Carrete and Mingo et al, however, believe the Born Approximation is invalid at phonon wavelengths similar to the size of the scatterer.[10] Instead, they used an atomic level investigation for 2.2 nm diameter SiNWs with surface disorder to conclude that reducing the thermal conductivity by one order of magnitude is difficult. Using another approach, Moore et al. proposed a backscattering mechanism by using Monte Carlo (MC) simulations of SiNWs with sawtooth structures, but could still not fully explain the large decrease in thermal conductivity.[11] More recent indirect MC simulation by Wang et al. proposed multiple scattering of phonons at the rough surface, while also accounting for impurity scattering, in order to fit their simulation to the experimental data of Hochbaum et. al.[12,17] However, the random nature of roughness on the EE-SiNWs was not taken into account, which presumably could lead to frequency-dependent scattering from the surface. While these theoretical works shed some light on the dependence of thermal conductivity on rough surfaces, experimental determination of the dependence of thermal conductivity on surface roughness of SiNWs is still lacking.[18,19]

This work introduces a quantitative correlation between thermal conductivity and surface roughness by considering the full length of SiNWs under measurement. This correlation was first established by roughened VLS SiNWs as a model system, and further supported by the work with EE-SiNWs.

As opposed to EE-SiNWs, which are prepared from doped wafers, Intrinsic VLS-grown SiNWs were etched in a controlled manner to create roughened surfaces. Since VLS-grown SiNWs have uniform morphologies with hexagonal cross section with minimal impurities, they can be good model systems to study the roughness effect. With this approach, the possible effects of impurity–phonon scattering are eliminated.[1,7,8] We characterize the roughness on the roughened SiNWs by Transmission Electron Microscopy (TEM) and statistically extract parameters to quantify the roughness on the surface. We found that root mean square (σ) and correlation length (L) of surface roughness do not individually correlate that well with the thermal conductivity. We introduce in this work a coefficient obtained from power law behavior of the roughness power spectrum at higher frequencies (α_p), which seems to correlate well with thermal conductivity reduction in single crystalline SiNWs.

EE-SiNWs are considered as good candidates for wafer scale thermoelectric modules with low cost. First, there is no limitation on the length of nanowires under wafer thickness. Second, the density of nanowires are much greater than that of VLS-SiNWs. Third, as-made wires are vertically aligned on wafer and ready for device fabrication. However, the surface roughness or morphologies of EE-SiNWs, etched from the doped wafers, may not be much controlled and thermal conductivity was not easily predicted for each nanowires. Hence, we also applied the same methodologies from roughened VLS-SiNW studies to EE-SiNWs to investigate the surface roughness effect on thermal conductivity.

2.2 Rough nanowire synthesis

2.2.1. Roughened VLS nanowires
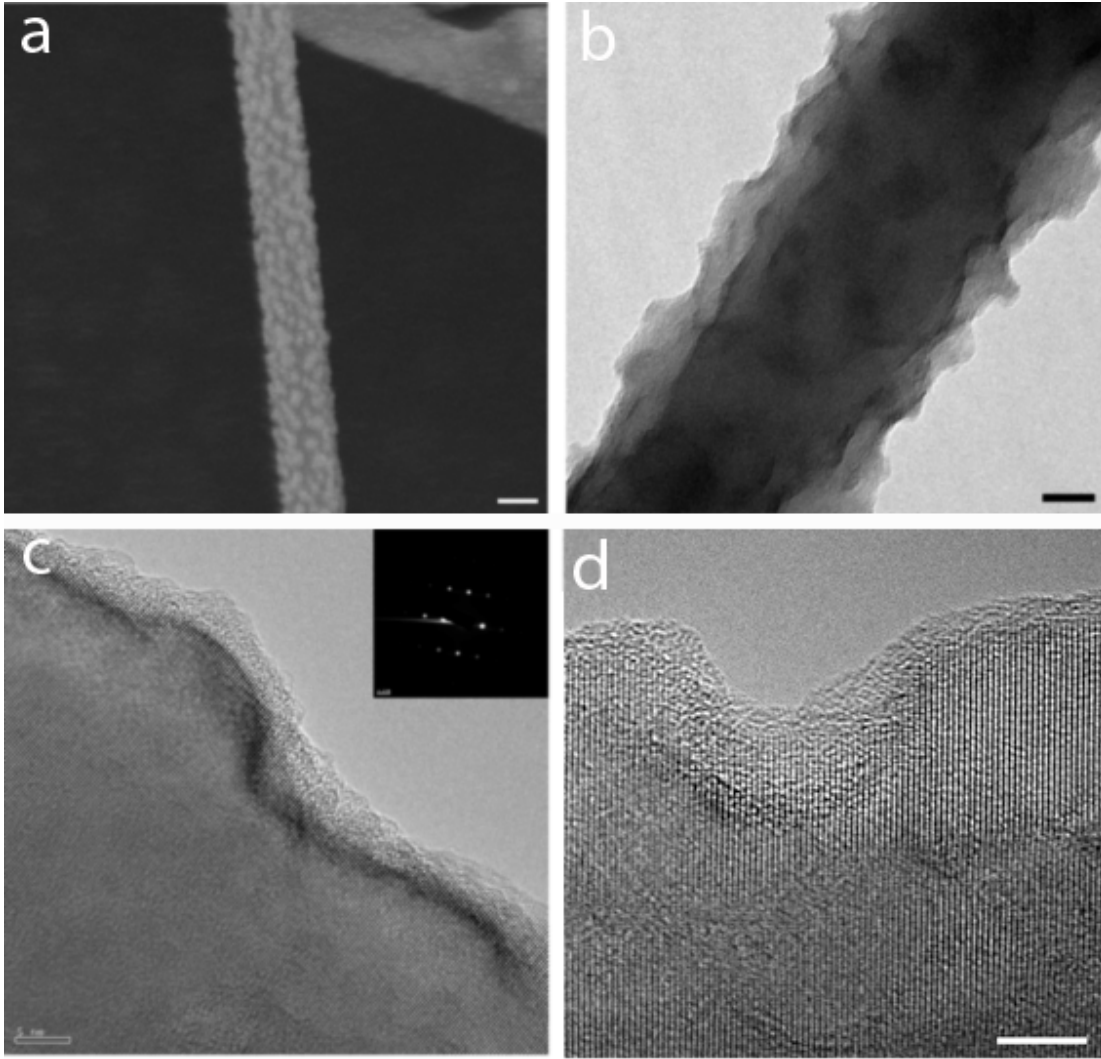
Fig. 2.1 Various surface morphologies of Si nanowires from two different etching methods(a) SEM image of a VLS SiNW with Ag nanoparticles on the surface (b) TEM image of a VLS SiNW after Ag removal in the etching method #1. (c,d) HRTEM image of roughed VLS SiNWs from etching method #1 and #2, respectively. The inset of (c) is the selective area electron diffraction pattern (SAED). Scale bars for a, b, c, d, are 1 um, 20 nm, 5 nm, 2 nm, respectively.

SiNWs having smooth surfaces were grown via the vapor-liquid-solid (VLS) growth mechanism using Au nanoparticles. Briefly, mono-dispersed Au nanoparticles were used as catalysts on a Si(111) wafer. The wafer was heated to 850 ℃ while a mixture of $SiCl_4$ and H_2/Ar (1:9) was flown into the system. This synthesis process produced single-crystal Si nanowires with smooth surfaces grown along the <111> direction. More details about SiNW growth and conditions can be found elsewhere.[20,21] After growth, the Si die was immersed in Buffered Hydrofluoric Acid (BHF, Ammonium Fluoride: Hydrofluoric Acid = 5:1), rinsed in Deionized (DI) water, then immersed in KI/I_2 solution to remove the Au residue. To induce roughness, two different processes

were employed, each showing distinctly unique roughness features (Figure 2.1), which enabled us to study a variety of rough surfaces of SiNWs.

Surface Roughening Process 1. Prior to the surface roughening steps, the native oxide on the SiNWs was etched in HF vapor, and the collection of SiNWs was sonicated with DI water. When added to a mixture of $AgNO_3$ (1.74×10^{-3} M) and HF (3.53 M), the following reactions took place: The SiNW surface becomes oxidized as a result of a galvanic displacement reaction between Ag^+ ions and Si, which is then subsequently etched by HF. Metallic Ag nanoclusters grow on the surface where the initial reduction of Ag^+ ions took place thereby indicating where Si was etched.[22-24]

$$4Ag^+_{(aq)} + Si_{(s)} + 6F^-_{(aq)} \longrightarrow 4Ag_{(s)} + SiF_6^{2-}_{(aq)} \quad (1)$$
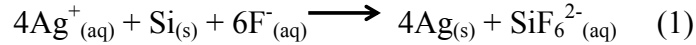
After 2 minutes, the reaction was quenched with excessive amounts of DI water, and then the solution was centrifuged to separate the SiNWs. Once isolated, they were immersed in concentric nitric acid for 30 minutes to remove residual Ag nanoclusters. Suspended SiNWs were retrieved after repeating the centrifuge and rinsing process (Supplementary Information Figure 1).

Surface Roughening Process 2. SiNWs were immersed in a mixture of $AgNO_3$ (1.74×10^{-5} M), HF (3.53 M) and H_2O_2 (5.57 M) solution for 3 minutes.[22] The reaction was followed with a DI water rinse and immersion into concentric nitric acid for residual Ag nanoparticle removal. Since the Ag nanoparticles are abundant and etching occurs only locally around them, the surface of SiNWs in both etching conditions showed a random, rough morphology (Supplementary Information Figure 1). After treatment, roughened SiNWs were transferred to a TEM grid for surface analysis and physical manipulation.

2.2.2. Electroless etched (EE) nanowires

The Electrolessly Etched wires were made by a similar process to that which has been used in Hochbaum *et. al.*[1] and has been described in detail in Peng et. al.[23] Briefly, (100) oriented Silicon wafers with varying starting resistivity levels (0.04-10 Ω-cm) were dipped in an aqueous solution of $AgNO_3$ and HF acid. The Ag^+ ions are reduced on the surface forming Ag nanoparticles, while the Silicon is oxidized along the edges of the subsequently formed nanowires. This SiO_2 is etched away by the HF acid present in solution, while additional reduction occurs on the top of Ag nanoparticles producing Ag dendrites. The nanowires used in this study are etched up to 100μm long and the resulting Ag dendritic 'cloud' formed in solution is etched away using a HNO_3 solution for more than a couple of hours. The roughness along the length of the nanowire was checked under TEM and found to be consistent. After the Ag removal step, silver nanoparticles were found on the edges of some nanowires. Such nanowires were not used for thermal conductivity measurement incase this indicated local stresses or additional reduction on the surface which might result in defected nanowires. The diameter of the nanowires synthesized varied anywhere between 30 to 200nm across the wafer. However, the roughness of nanowires from the same wafer undergoing the same etching process was not uniform. While selecting the starting wafer resistivity can control

porosity and rms roughness, it was found that the broadband roughness of two different wires from the same batch of nanowires could be different. (Figure 2.5) Tapering for a length of wire that is ~10μm is not significant, but can be a few nanometers at most depending on the diameter of the nanowire. Energy Dispersive X-Ray Spectroscopy (EDS) was performed on the nanowires inside a Transmission Electron Microscope (TEM) to ensure that there was no residual silver in the nanowires (Data not shown).

2.3 Surface morphology characterization

2.3.1. Atomic Force Microscopy (AFM) Study

The surface roughness of SiNWs was characterized by Atomic Force Microscopy (AFM). Rough nanowires were drop cast or manipulated on clean and flat silicon substrate and individual nanowires were aligned to the scan direction. Surface roughness information was collected in the middle of width and along the length of nanowires.
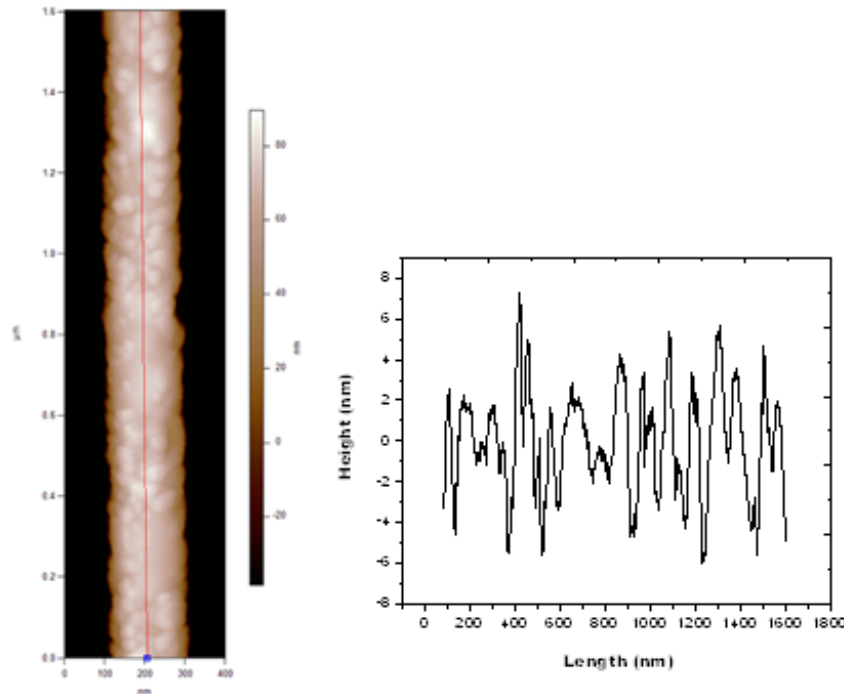

Fig 2.2(A) Atomic force microscope (AFM) image of a rough VLS nanowire. (B) Line profile along the length of the nanowire.

The surface roughness profile was characterized by TEM and then transferred to silicon substrate for AFM measurement. The surface roughness (root-mean-square, rms) information of the same nanowires by two different techniques was compared in figure 2.3.
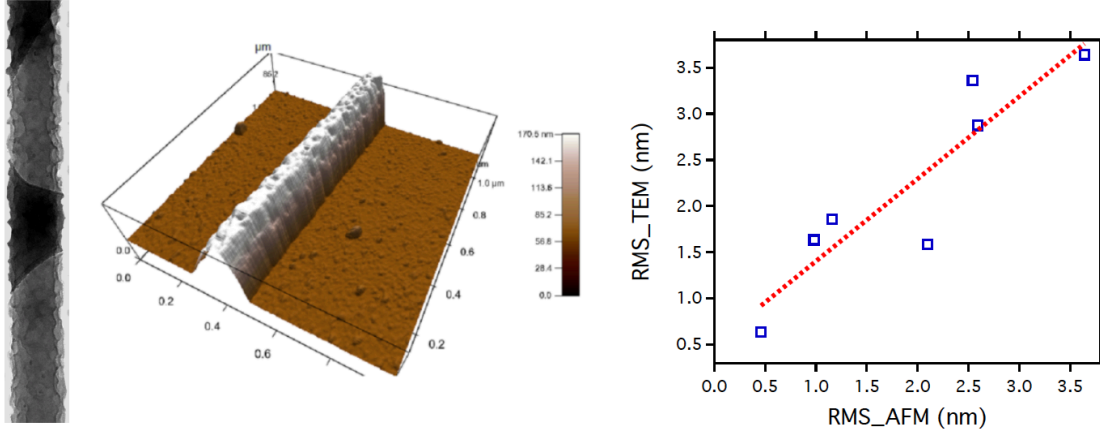
Fig. 2.3 TEM and AFM images of a rough nanowire. rms values of the same nanowires were correlated.

Although AFM image proved a great capability to characterize the surface roughness, several issues made AFM not ideal for the study. The tip radius, R has to be much less than the feature curvature radius, r and the lateral resolution is given as $d = \sqrt{8(R+r)\delta Z}$ where R is curvature radii of tip, r is curvature radii of resolved objects, and δZ is the vertical resolution limit. Hence, in order to resolve very rough surface with small curvature radius < 1nm, R has to be also smaller than 1nm, which makes AFM technique for this application impractical. Moreover, transferring nanowire laid on silicon substrate to pre-fabricated microdevice for the direct thermal conductivity measurement is challenging.

2.3.2. Transmission Electron Microscopy Study: TEM and STEM

The surface roughness of SiNWs was characterized by TEM. A series of images at 80,000x magnification were taken along the length of each SiNW and then stitched together, which enabled us to obtain information about the surface roughness along the entire length (Figure 2.4 a). The diameter is obtained from the TEM images and defined by assuming a circular cross section at each point along the SiNW. Therefore, the average diameter of the entire SiNW is obtained from the average of all the individual cross sections. After TEM characterization, those specific individual SiNWs were manipulated onto pre-fabricated microdevices to measure the thermal transport properties (Figure 2.4 b).[25] To reduce the thermal contact resistance, a Pt/C composite was deposited on both ends of the nanowire using Electron Beam Induced Deposition (EBID) inside a FEI-Strauss Dual Beam FIB (Figure 2.6). This method was used previously in literature and was successful in reducing thermal contact resistance for different materials.[26,27] Since only a 2-6 μm long section of the wire bridges the thermal device, only the roughness of that specific active segment between the contacts was considered in all calculations. Additionally, since curvature of even a 2-6 μm segment can affect the roughness measurement, surface profiles were sequentially analyzed along the length in 1 μm segments at a time (Figure 2.4 c). To remove any marginal curvature effects, a fifth-order polynomial was used to subtract any background curvature. This procedure was insensitive to the order of polynomial chosen, as any polynomial higher than 5 produced

the same quantitative result. After background subtraction, the rms and the power spectrum of each 1 μm section was averaged to generate the entire nanowire's rms, σ and power spectrum, *S(q)* respectively (Figure 2.4 d).
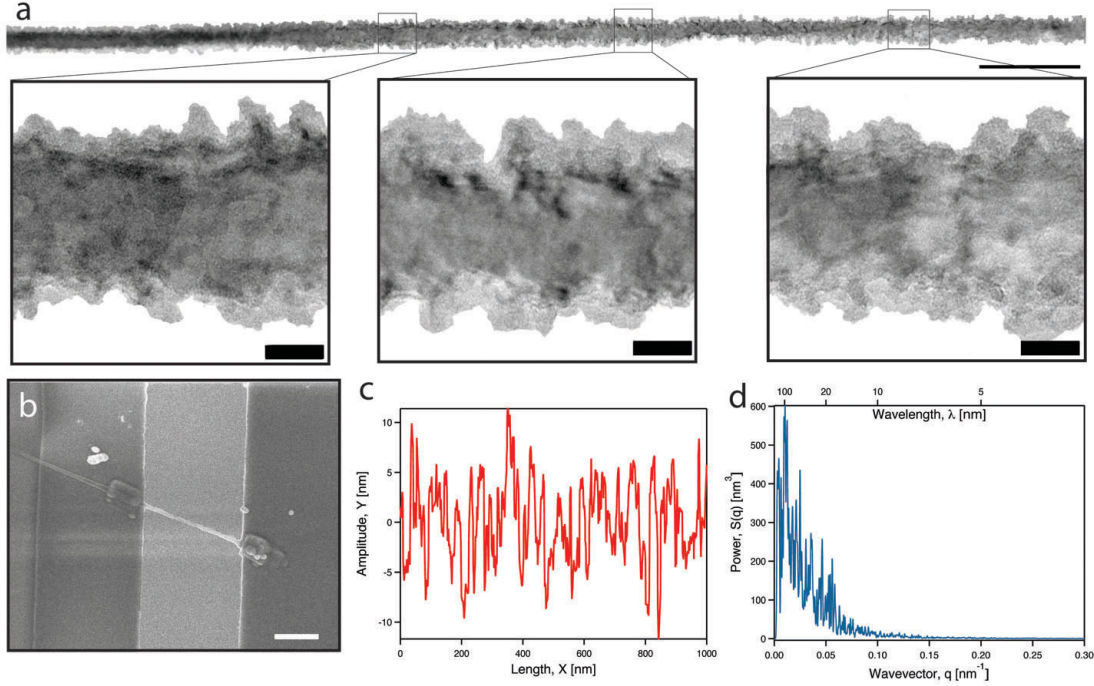
Figure 2.4. Surface roughness characterization. (a) Serial TEM images of SiNWs along the length with zoom-in images at different position. (b) SEM image of the identical nanowires from (a) on thermal measurement device. (c) Surface profiles from serial TEM images. Full length is sectioned by 1μm followed by fifth-order background elimination. (d) Averaged power spectrum from sectioned surface profiles. Scale bars for panel a are 500 nm and 20 nm, panel b is 1 μm.

On the other hands, there are quite a lot of distribution in crystal quality and morphologys within a batch of EE SiNWs samples. It has previously been shown that the electroless etching technique can be used to produce silicon nanowires with pores that have a crystalline silicon scaffolding as demonstrated by selected area electron diffraction (SAED) pattern.[28] The porosity for a single step electroless etching procedure can be controlled by the silicon wafer doping level to produce pore sizes varying between 4-16 nm depending on the concentration of $AgNO_3$ used for etching.[29] The pores are clearly visible under bright field TEM. However, one can imagine that wires that have pores inside the core have a phonon mean free path that is limited not by the diameter of the wire, but the pore-to-pore distance instead. Hence, the diffusive mean free path is less than the diameter, $\ell_{eff,boundary} < D$. We have established two levels of control to ensure that the nanowires studied in this work are continuous and without pores. Firstly, we grew the nanowires from high resistivity (>4 mΩ-cm) wafers using a AgNO3 concentration of 0.02M, which should produce non-porous wires based our own and previous studies. [28,29]

Secondly, we directly imaged the measured nanowires with STEM with a high angle annular dark field (HAADF) detector on a 200kV FEI Tecnai F20. In this mode, a highly converged electron probe (< 5Å) is rastered across the sample and only the highly scattered transmitted electrons are collected. Image contrast is based on incoherent elastic scattering and varies approximately linearly with thickness and with the atomic number squared (Z^2) of the constituent material.[30,31] STEM contrast of the single phase Si nanowires is thus capable of estimating the projected thickness of the nanowires, and pores (if they exist) are clearly seen as shown in Figure 2.5 b. Also, highly scattering Ag atoms (Z = 47) are extremely bright compared to the Si (Z = 14) nanowires in STEM images and Ag impurities/nanoparticles are easy to identify.

For non-porous wires, we calculate the approximate cross-sections of the nanowires used for phonon measurement from STEM images The intensity contrast provided by STEM allows an estimate of the relative thickness across the wire and hence the wire cross-sectional area. STEM clearly shows that the wire cross-sections are non-circular with important implications for phonon scattering. The clearest indication is provided by STEM tomography, where the 3D shape and surface roughness of the nanowire can be reconstructed from a series of projection images with nm-scale resolution (Figure 2.5 a). In fact, pores as small as a 2-3 nanometers in diameter are visible in a tomographic reconstruction. The importance of accurately measuring the cross-sectional area is shown using the electron tomography data. A single measurement from the projection image shown in Figure 2.5 c gives a lateral width w of 65 nm. Assuming a circular cross-section, as most other experiments have done previously, with this diameter the nanowire has an apparent area that is 30% larger than the actual cross-section as measured from the 3D electron tomography data. Electron tomography is difficult and time consuming to apply to numerous wires, however, and we instead apply the above technique of assuming a linear relationship between thickness and STEM intensity normalized by the beam current. This technique gives a similar result for the cross-sectional area as the tomography data, and is much easier to apply on many wires. In order to estimate the cross-sectional area from single STEM projection images, we integrate the intensity under a line profile across the lateral width of the nanowire. The integrated area is calibrated with respect to the total current of the incident electron probe to allow for variations on different microscope sessions. The cross-sectional area of a smooth vapor-liquid-solid (VLS) nanowire, which is assumed to be circular, was first used to test such a calibration for this method as seen in Figure 2.5 d. From electron tomography, we know that EE wires are not in general round in cross-section, and the width measured from a projection image from a random orientation of the wire sitting on a substrate will give very different estimates of cross-sectional area if assumed circular. Further, STEM can be used to identify defects such as necks and junctions, although such nanowires are not used in this study for thermal measurement. Finally, the cross-section for measured wires is checked at different points along the length of the suspended nanowire to confirm that the cross-sectional area does not vary significantly.
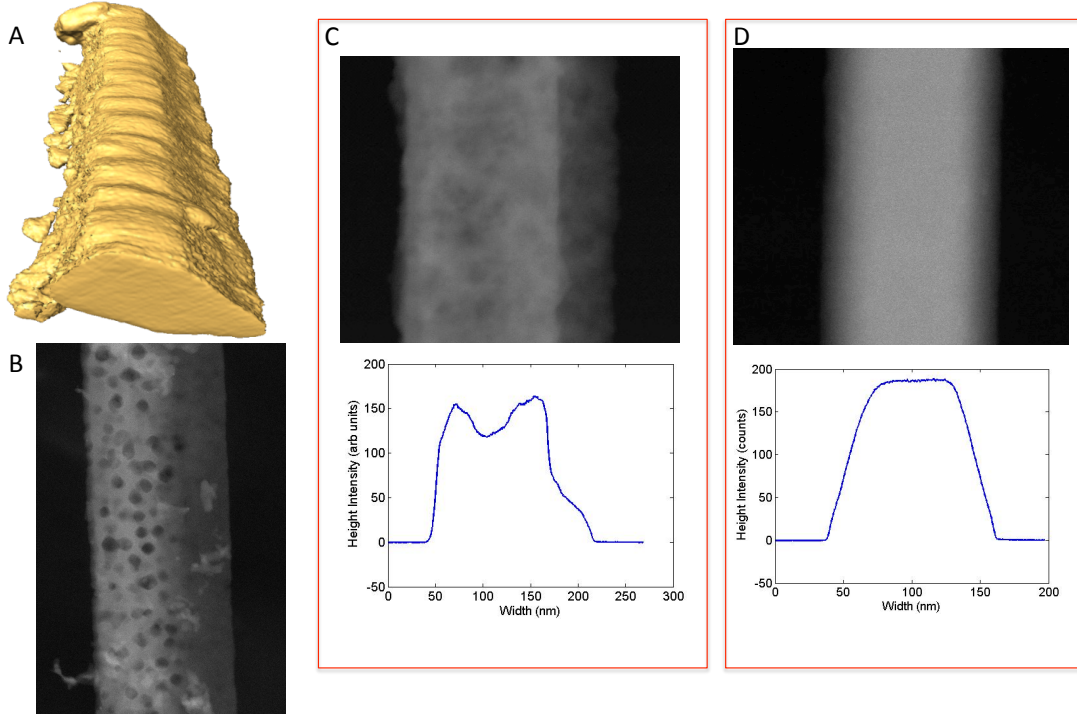
Figure 2.5 Morpholohy of EE nanowires (a) Three dimensional tomogram by STEM showing a non-circular cross-section and roughness along the edges of the nanowire. (b) Porous nanowire with nanoscopic pockets imaged with STEM from a wafer with starting resistivity ρ <0.03Ω-cm (c) STEM profile for a non-circular cross-section EE nanowire. (d) STEM profile for a circular cross-section smooth VLS nanowire.

2.4 Results and Discussion

2.4.1 Roughened VLS-SiNWs

Martin et. al. postulated based on the Born Approximation[9] that the frequency dependent boundary scattering rate $\tau_{i,j}^{-1}(E)$ can be represented by a surface integral in energy, $S(E')$ where the integral is taken over the area of the surface of constant energy, E' as:

$$\tau_{i,j}^{-1}(E) \propto \int_{E'=E_i} \frac{S(q)}{\nabla_{k'} E'(k')} dS_i(E'), \quad q = k' - k \qquad (2)$$

Here they considered a phonon with wavevector k from branch i scattering to a phonon with wavevector k' from branch j. Also, $S(q)$ is the Fourier transform of the spatial autocorrelation function, or in other words, the power spectrum, the dilated rough surface that scatters the phonons, which constitutes the perturbed Hamiltonian H'

allowing for the transition from the incoming wavevector, k to the scattered wavevector k'. Sadhu and Sinha, using a wavelike phonon transport approach, considered coherent scattering of phonons from a rough surface, and presented that for modes at frequency ω: [17]

$$l_{mn}^{-1}(\omega) \propto \sum_{pq} S(q), \quad q = k_{mn} - k_{pq} \qquad (3)$$

where $l_{mn}^{-1}(\omega)$ is the mean attenuation length for those phonons scattering from incident direction k_{mn} to a scattered direction k_{pq} and $S(q)$ is the power spectrum. Thus, in order to understand scattering of phonons from a rough surface, experimental determination of $S(q)$ is crucial.

It is common to assume that the autocovariance function of a random rough surface to follow an exponential curve given by $C_E(r)$ as also evidenced in literature shown in Equation (4) below[9,32-35]

$$C_E(r) = \sigma^2 e^{-r/L} \qquad (4)$$

where $C_E(r)$ is the autocovariance function of the Si surface roughness, $\Delta(r)$ is the extracted surface profile, and σ is the rms value of $\Delta(r)$, L is the correlation length, which is a statistical parameter that determines the decay of the autocovariance and is related to the lateral length scale of the roughness. By convolution theorem, the power spectrum is the Fourier transform of the autocovariance function, yielding a Lorentzian form given by:

$$S_E(q) = 2L\Delta^2 \frac{1}{\left[1 + (2\pi Lq)^2\right]} \qquad (5)$$

In this study, 1-D power spectrum derived from the Fast Fourier Transform (FFT) was calculated for the surface profile with ordinary wavevectors given by q in units of nm^{-1}. As a first approximation, since previous theoretical work has assumed an exponential autocovariance fit for calculating surface roughness, the Lorentzian defined in Equation (5) is used to extract L from the total power spectrum, $S(q)$.[9,32,33]
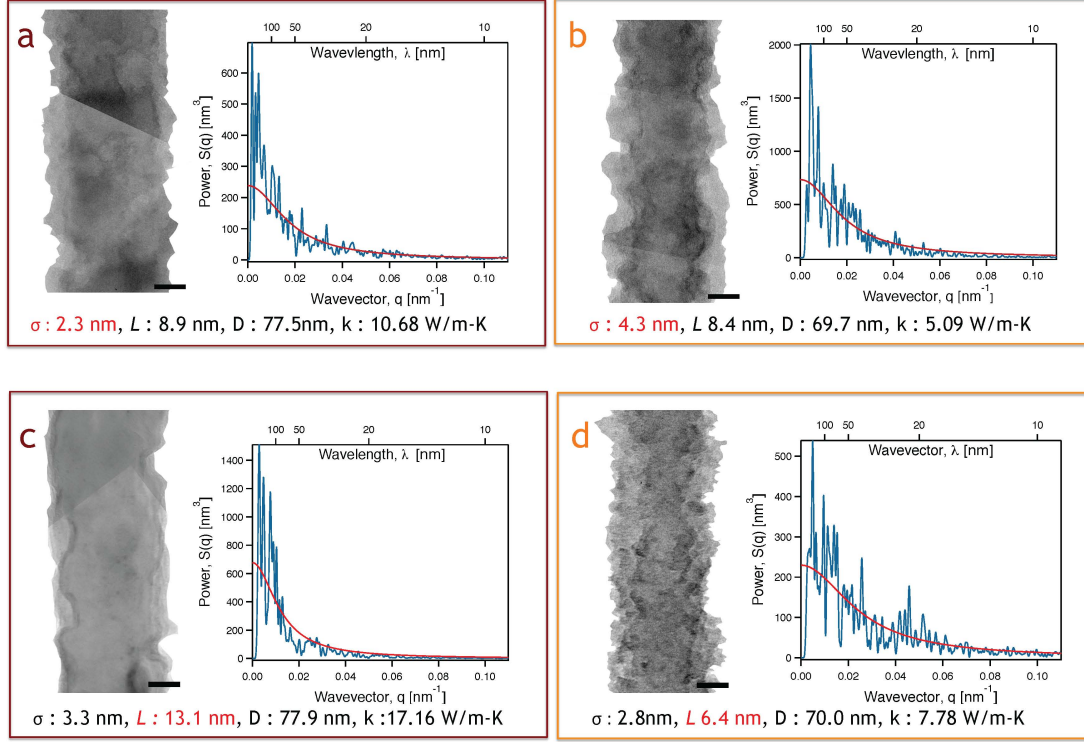
Figure 2.6. Extraction of σ and L from TEM images and their effect on thermal conductivity. (a-b) rms (σ) effect on thermal conductivity, (c-d) Correlation length (L) effect on thermal conductivity. All scale bars are 1μm.

As seen in Figure 2.6, this method produced σ and L values from TEM images of individual rough SiNWs. Two SiNWs with comparable L (8.9 nm and 8.4 nm) and similar D (77.5 nm and 69.7 nm) are shown in Figures 2a and 2b, respectively. The TEM images clearly depict the significantly different rms values of the two SiNWs (σ = 2.3 nm and 4.3 nm), which lead to their correspondingly different thermal conductivities (10.68 W/m-K and 5.09 W/m-K, respectively). In Figures 2.6c and 2.6d, on the other hand, the nanowires have comparable diameters D (78 nm and 70 nm) and σ values (~ 3.3 nm and ~ 2.8 nm) respectively. However, the SiNW in Figure 2d has roughness with L ~ 6.4 nm, which is half the value of that for the SiNW in Figure 2c (L ~ 13.1 nm). A smaller value of L corresponds to roughness features occuring at a.shorter length scale, which scatter broadband phonons more effectively.[9,15,32,33] The resulting thermal conductivity at 300 K of the SiNW in Figure 2.6d (7.78 W/m-K) is lower than that of the nanowire in Figure 2.6c (17.16 W/m-K). This provides evidence towards enhanced phonon-surface scattering in SiNWs with shorter L.

The thermal conductivities of these and other SiNWs are plotted as a function of temperature in Figure 2.7. Nanowires with comparable L (8.4 – 8.9 nm) and D (67.9 – 79.8 nm) were selected in Figure 2.7a, while nanowires with comparable rms (σ = 2.8 – 3.3 nm) and D (70 – 77.9 nm) were chosen in Figure 2.7b. Clearly, the increase in rms from σ ~ 0 (as-grown) to 4.3 nm drops the thermal conductivity from 25 W/m-K to 5.09 W/m-K at 300K. Similarly in Figure 3b, as σ remained comparable and L decreased

(down to 6.4 nm), a drop in thermal conductivity from 24.63 W/m-K to 7.78 W/m-K was observed. Thus, utilizing the full power spectrum of the roughness profile and looking at the σ and L values, we can predict that rougher wires with higher σ and lower L tend to have a lower thermal conductivity.
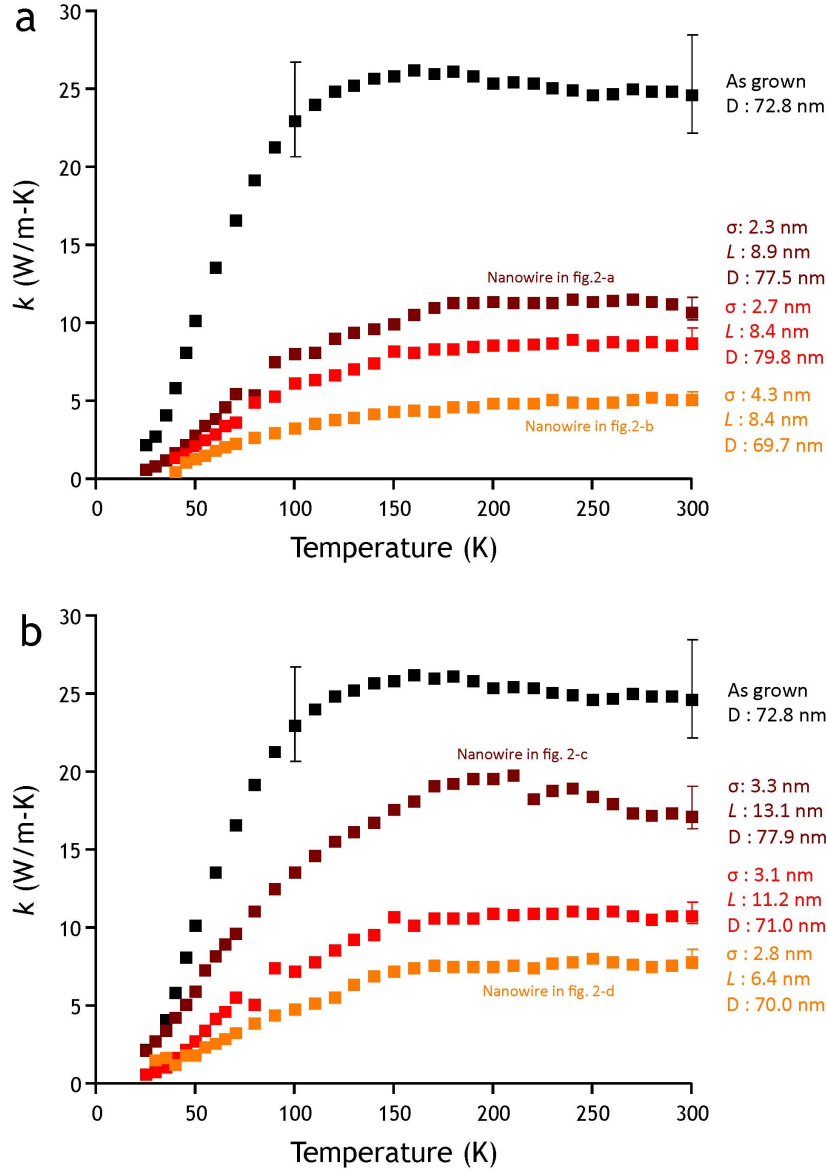
Figure 2.7. Thermal conductivity with temperature as a function of L and σ. (a) Thermal conductivity dependence on σ with controlled σ and diameter. (b) Thermal conductivity dependence on correlation length L with controlled L and diameter.

However, in order to understand the nature of scattering from the surface of the nanowires, we need to consider phonon wavelengths as well, which previous studies have lacked. In using the kinetic theory for phonons, we can consider that at any temperature, the order of magnitude estimate for a dominant wavelength carrying the heat is given by

$\lambda_{dom} \sim \dfrac{2hv_g}{k_B T}$, where v_g is the average group velocity of the phonons at thermodynamic

temperature T.[36,37] At 300K, λ_{dom} is ~ 1nm. However, in reality, there is a large spectrum of phonon wavelengths that contribute to the thermal conductivity. As shown in Figure 2.8a (reproduced with permission from A. Henry et. al. and publishers Journal of Computational and Theoretical Nanoscience[38]), a strong spectral dependence of the contribution of phonons to thermal conductivity exists and up to 80% of the thermal conductivity at 300K in bulk Si can arise from phonon wavelengths ranging from 1-100 nm. Using this as a starting point for analysis and taking a careful look at this wavelength bandwidth of the roughness power spectrum, $S(q)$, it is found that a power law fit captures the power spectrum more accurately (with a least squares fit of >0.9 for all nanowires measured) than a Lorentzian, as shown in Figure 2.8b.[39] The fit used to then define the roughness is given by:

$$S(q)_{10^{-2}\rightarrow 10^0} = \alpha_p \left(\frac{q_0}{q} \right)^n$$

$$(6)$$

where only wavevectors, q of the roughness from 10^{-2} to 10^0 nm^{-1} (1-100 nm) are considered. α_p and n are parameters derived from the fit, and $q_0 = 1/0.313$ nm is the

inverse of the lattice constant of Si in the <111> direction. The exponent n is related to the nature of the roughness and is roughly the same for all nanowires measured in this study, and was determined to be $n_{rms} = 2.77$ and $n_{standard\ deviation} = 0.075$ (Table1). This indicates that the intentional etching of the VLS nanowires described in the earlier section produces a certain type of roughness where the relative amplitudes at different wavelengths or the ratio of amplitudes at different wavelengths, represented by the exponent n, remain roughly the same. On the other hand, α_p is related to the broadband

roughness amplitude parameter of the nanowire surface at these relevant wavelengths. We expect a larger α_p for a rougher nanowire. Thus, the thermal conductivity is

anticipated to be lower when the value of α_p is higher, while the exact functional

dependence is difficult to ascertain.
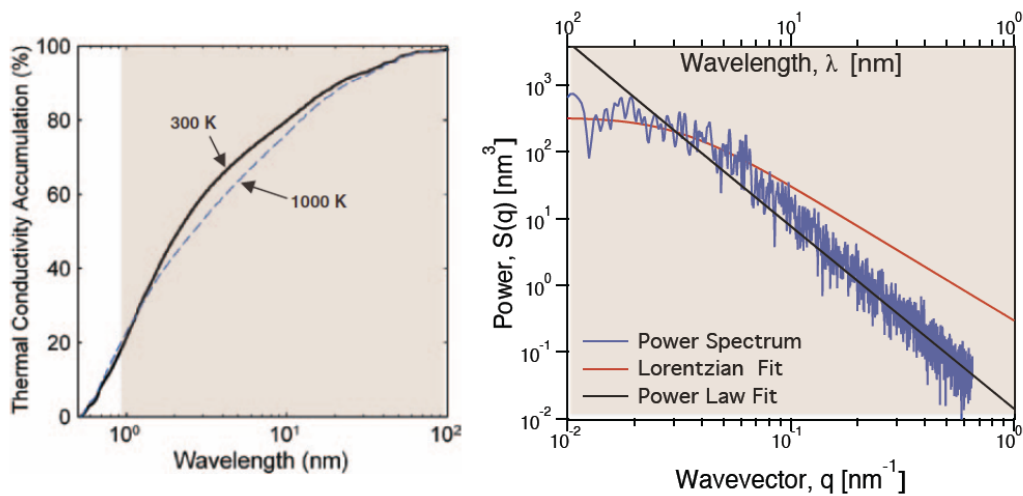
Figure 2.8. (a) Thermal conductivity accumulation as a function of wavelength at 300K and 1000K (reproduced with permission from the authors and publishers in Journal of Computational and Theoretical Nanoscience.[38] Roughly 80% of contribution to thermal conductivity at room temperature comes from phonons with wavelength between 1 and 100nm. (b) Roughness Power Spectrum at the selected length scales (1-100nm). While the actual Power Spectrum is shown in blue, the Lorentzian fit used to extract σ and L is shown in red to be a poor fit at the relevant length scales. The power law fit shown in black captures the roughness better.
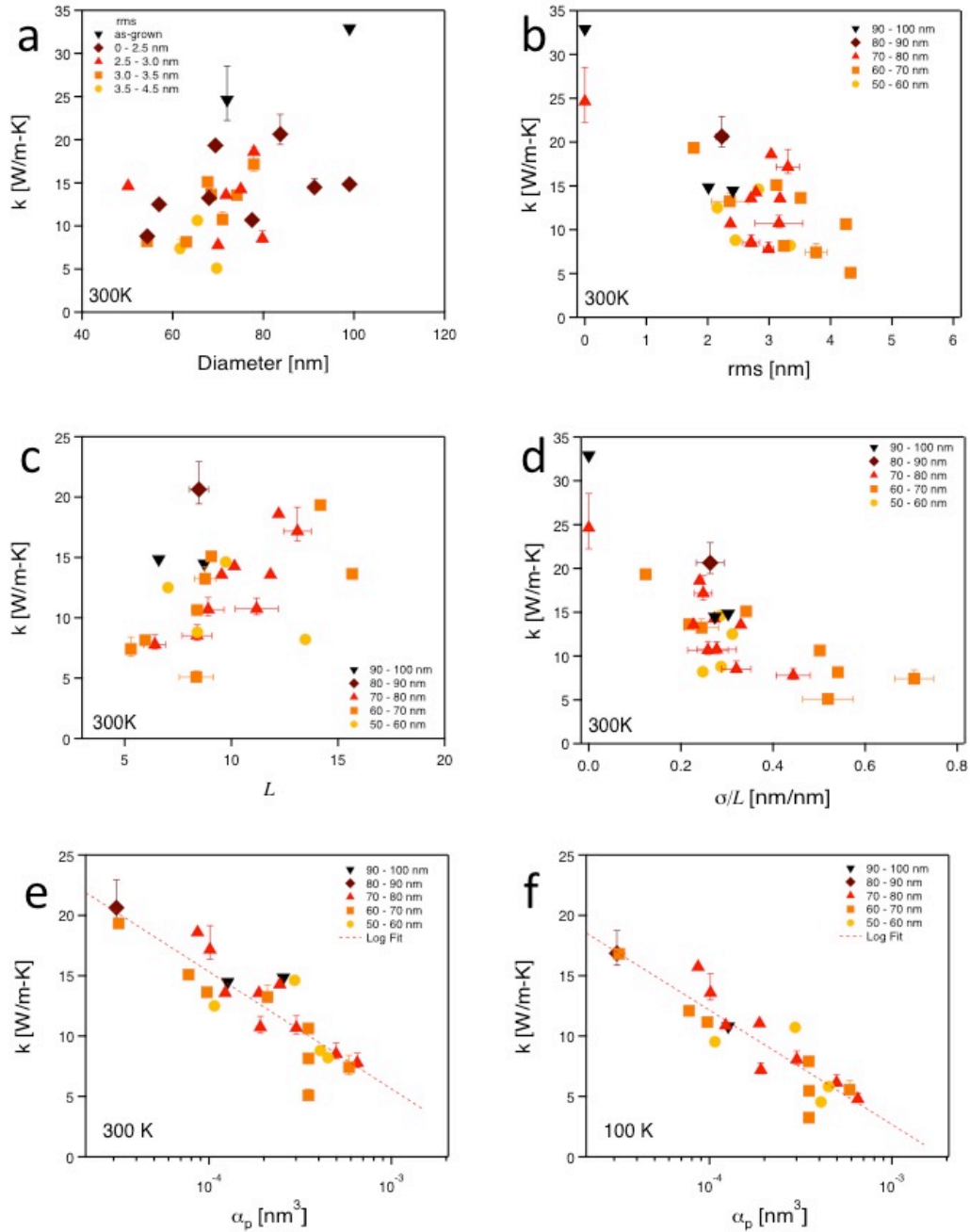
Figure 2.12. Thermal conductivity as a function of three roughness factors (σ, D and L). (a). Thermal conductivity at 300 K as a function of rms with different range of diameter. (b). Thermal conductivity as a function of diameter with different range of rms. (c). Thermal conductivity as a function of diameter with different range of L. (d). Thermal conductivity as a function of σ/L for 300K.Correlation between thermal conductivity and σ/L gets stronger than rms or D only. (d) has a trend similar to Ref. 8 figure 3a except the discrepancy in L. (e,f) Thermal Conductivity as a function of α_p (plotted on a log scale) at 300 K and 100 K, respectively. As α_p increases, the wires are rougher, with wavelengths in the 1-100nm range and the thermal conductivity drops significantly.

In order to better understand the individual roles played by rms, diameter, correlation length, and the high frequency amplitude term, α_p, towards reducing phonon propagation, the room temperature thermal conductivity of SiNWs as a function of different parameters are plotted in Figures 2.9a-f. Comparing Figures 2.9a and 2.9b, it can clearly be seen that rms exhibits a more pronounced impact on the thermal conductivity than the diameter. This clearly indicates that for rough nanowires, rms, rather than diameter (within the range measured), is the major limiter of phonon propagation. Further, as illustrated in Figure 2.9c, there is no clear dependence of thermal conductivity purely on the correlation length L, which indicates that L by itself doesn't capture the surface roughness accurately. The fact that the rms rather than the diameter has more influence on phonon transport is qualitatively different from the trend observed with smooth SiNWs, where boundary scattering occurs in the diffusive regime.[7,8] In this diffusive picture, the nanowire surface absorbs all phonons impinging upon it and thermalizes it; then, behaving as a blackbody (to ensure elastic scattering), re-emits the phonons at a rate proportional to the local temperature of the surface. In this new sub-diffusive regime, where the thermal conductivity, k is lower than the Casimir Limit, we first propose a dimensionless roughness correlation factor to define the total roughness, σ/L, which is based upon the following physical intuition: the magnitude of the roughness is (1) proportional to σ and (2) inversely proportional to L at 300K (Figure 2.9d). While it is clear that σ and L are the important parameters that define the roughness of the surface, they do not directly represent the roughness parameter that is relevant for phonon scattering. Therefore, it is not surprising that although there seems to be a better trend of thermal conductivity with σ/L as opposed to that with σ or L individually, the correlation is not very strong and shows scatter.

Looking back at Figure 2.8b in detail, the Lorentzian fit doesn't capture roughness spectrum at the relevant wavelengths (1-100nm) very well. Also, the roughness length scales that are relevant for phonon scattering are better captured in the power spectrum, which is represented by two parameters α_p and n. Since n is a constant across all the etched wires, what captures the roughness structure over the relevant phonon scattering band is the parameter α_p. Figure 5e plots the thermal conductivity as a function of α_p for various wires at 300K, and what is observed is a much better fit. This indicates that directly relating the lateral length scale of the roughness to the wavelength bandwidth of phonons contributing to thermal conductivity is key to understanding the physics of

roughness boundary scattering. Figure 2.9f plots the thermal conductivity as a function of α_p for the same wires at 100 K, which is a marginally better fit.

The enhanced scattering of phonons from rough surfaces observed in this study qualitatively follows predictions from earlier theoretical work. Separately, both Alvarez *et. al.* and Moore *et. al.* predicted stronger backscattering of phonons at periodically rough surfaces with longer σ and shorter L by using phonon hydrodynamics and Monte Carlo simulations, respectively.[11,13] However, direct application of this analysis is hindered by the non-uniform roughness profile obtained from the electrochemical etching technique, which may behave differently than the periodic structure. A possibly more applicable theory by Wang *et. al.* [12] suggested that phonons are localized at the rough surface due to multiple boundary scattering occurrences within a single roughness feature on the surface. They pointed out that thermal conductivity decreases as features becomes sharper, which can be interpreted as a shorter L and higher σ. However, they did not look at the effect of high frequency roughness that may selectively scatters phonons more effectively than the low-frequency ones.[12] Martin *et. al.* [9] and Santamore *et. al.*[35] use a perturbative approach due to the change in potential at the surface resulting in enhanced boundary scattering, however it remains to be seen if these claims are valid given the range of correlation lengths and rms we have observed in our work. While their study used a correlation length, $L = 6$ nm, our observed L varies from 8.6–22.3 nm with rms values range from $\sigma = 1.8$ nm to 4.3 nm. Sadhu *et. al.* used a broader range of correlation lengths that fit the power spectrum and used a Green Kubo analysis coupled with the Landauer Formalism to extract attenuation lengths for all phonon modes. [17] Some modes had reduced phonon group velocity in their analysis, which they postulated resulted in a lower thermal conductivity.

 However, none of these theoretical studies looked at the wavelength dependent conductivity with scattering from the surface for a selective range of roughness wavelengths. To our best knowledge, our experimental work provides first evidence for frequency dependent phonon scattering from rough surfaces. We hypothesize that as high-frequency roughness of the nanowire surface increases, there is enhanced boundary scattering, thus reducing the thermal conductivity significantly. This experimental study warrants further theoretical exploration of scattering of phonons from a rough boundary at specific relevant wavelengths in order to understand the exact correlation between the statistically defined α_p parameter and the thermal conductivity.

Every attempt was made at obtaining the most accurate and certain data possible, but there are, however, limitations to our method of characterizing roughness. First, TEM images are 2-dimensional projections of a 3-dimensional material. Therefore, roughness profiles from the projected surface images neglect hidden roughness features not occurring at the respective edge of the sample. But due to the isotropic nature of the etching process and the large number of samples measured, the determined relations found here are statistically meaningful. Second, the fitting curve to power spectrum is strongly sensitive to low frequency peaks which account for not only rough surface but also the curvature of the SiNWs. Hence, the choice was made to fit a power law to the high frequency section of the power spectrum only. Third, since L is calculated using the assumption that the autocovariance of the surface profile is an exponential, the uncertainty of L can be estimated based on the coefficient of determination from a least-

squared fit, R^2 when equation (5) is used to fit the original power spectra. Hence, only the Lorentzian fitting functions where R^2 is larger than a certain value (0.63) are strictly chosen. Despite the relatively large uncertainty in L, as can be seen in Figure 5d, trends of the dependence of thermal conductivity, k with σ/L are clearer than that of thermal conductivity purely with rms. In terms of the power law fit, the choice of frequency limits was informed from A. Henry et. al.[38]. First principle calculations, however, show a tighter phonon wavelength bandwidth contributing to thermal conductivity and this bandwidth can also be significantly temperature dependent. [40,41] The thermal conductivity strongly correlates with the parameter, α_p, extracted from a power law fit of the roughness power spectrum, which opens up a new way of not only characterizing rough surfaces but also shed some light on the possible physics at work.

Table 1. Roughness parameters with measured thermal conductivity at various temperature.

Dia.	rms_right	rms_left	rms_ave.	Corr. Leng.	rms/L	Power Law ($\alpha(q0/q)^n$)		Therm. Cond. (W/m-K)		
D (nm)	σ_R (nm)	σ_L (nm)	σ_Ave (nm)	L_Loren (nm)	σ/L	n	α (nm^3)	k(300K)	k(200K)	k(100k)
50.2	2.5	3.0	2.8	9.73	2.86E-01	2.59	2.95E-04	14.6	13.9	10.7
57.0	2.2	2.1	2.2	7.03	3.07E-01	2.80	1.07E-04	12.5	13.0	9.5
54.4	3.4	3.3	3.3	13.47	2.48E-01	2.65	4.50E-04	8.2	7.9	5.8
54.4	2.1	2.8	2.4	8.41	2.87E-01	2.65	4.08E-04	8.8	6.1	4.5
65.4	4.1	4.3	4.2	8.40	5.02E-01	2.67	3.50E-04	10.6	10.3	7.9
67.7	3.0	3.2	3.1	9.05	3.42E-01	2.82	7.73E-05	15.1	15.5	12.1
69.4	1.8	1.8	1.8	14.18	1.24E-01	2.90	3.20E-05	19.3	20.6	16.8
68.5	3.0	3.9	3.4	15.66	2.18E-01	2.80	9.74E-05	13.6	13.7	11.2
68.0	2.6	1.7	2.1	8.77	2.45E-01	2.70	2.09E-04	13.2		
63.0	3.5	3.0	3.2	5.96	5.41E-01	2.74	3.51E-04	8.2	7.6	5.5
61.6	4.0	3.5	3.7	5.29	7.07E-01	2.72	5.86E-04	7.4	7.5	5.6
69.7	4.0	4.6	4.3	8.36	5.14E-01	2.76	3.51E-04	5.1	4.8	3.2
71.8	2.9	2.5	2.7	11.83	2.27E-01	2.73	1.23E-04	13.6	13.4	10.9
77.9	3.5	3.0	3.3	13.10	2.49E-01	2.82	1.01E-04	17.2	19.6	13.6
74.2	3.2	3.1	3.1	9.54	3.30E-01	2.70	1.88E-04	13.6	12.9	11.0
77.9	2.4	3.5	2.9	12.22	2.41E-01	2.81	8.66E-05	18.6	19.4	15.7
71.0	2.5	3.7	3.1	11.19	2.78E-01	2.72	1.91E-04	10.7	10.9	7.2
77.5	2.8	1.8	2.3	8.91	2.59E-01	2.67	3.01E-04	10.7	11.4	8.1
79.8	2.9	2.5	2.7	8.39	3.20E-01	2.60	4.98E-04	8.5	8.5	6.1
75.0	2.7	2.8	2.8	10.14	2.73E-01	2.70	2.45E-04	14.3		
70.0	2.7	3.0	2.8	6.41	4.44E-01	2.63	6.50E-04	7.8	7.5	4.8

83.7	2.1	2.4	2.2	8.48	2.63E-01	2.97	3.11E-05	20.6	21.6	16.9
91.3	2.4	2.4	2.4	8.73	2.74E-01	2.85	1.27E-04	14.5		
99.0	1.9	2.1	2.0	6.60	3.03E-01	2.66	2.56E-04	14.8	14.2	10.8

2.4.2 EE-SiNWs

Thermal conductivity of EE-SiNWs are now considered. The surface roughness of 7 different wires was characterized by TEM and their thermal conductivity was directly measured. We plot the thermal conductivity as a function of diameter, d, rms, σ and power spectra, α_p in Figures 213a, b and c respectively. While the rms roughness, σ is sensitive to roughness from the total spectral range of the surface profile, the power spectra is only for a spectral range q=0.01 to 1 nm^{-1}. In order to drive home the observation that phonon scattering physics depends on the roughness, we have also provided a direct comparison with roughened VLS SiNWs in the figure 2.12 As seen in Figure 4a, the thermal conductivity does not depend strongly on the diameter, a trend that was also observed in the VLS NWs. This is the first indication of a possible deviation from diffusive transport of phonons, since the mean free path is not limited by the diameter, but something lesser. While there is a weak dependence of the thermal conductivity on rms roughness for the roughened-VLS wires, the dependence disappears for the EE wires.(Figure 2.13b) On the other hand, the dependence of measured thermal conductivity on α_p follows the same trend as that observed for the roughened-VLS nanowires (Figure 2.13c). The agreement on this trend suggests that characterizing the roughness requires paying attention to the dominant wavelength of phonons carrying heat at any particular temperature.
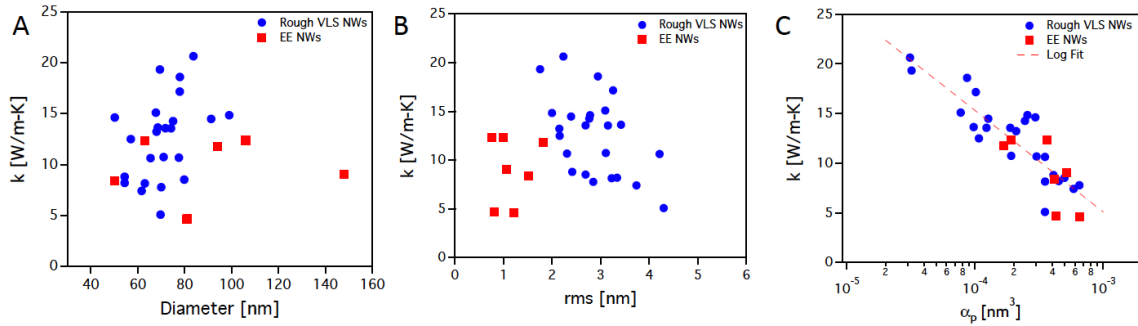

Figure 2.13 Correlation between roughness factors and thermal conductivity of EE NWs and rough VLS NWs as comparison. (A) Thermal conductivity vs. diameter (B) vs. rms (C) vs. α_p

2.5 Conclusion

In conclusion, this study has experimentally shown that surface roughness can be captured accurately by applying spectral techniques to the profile obtained from high-resolution TEM images. The study suggests that the surface roughness interacts with a broadband spectrum of phonons in SiNWs, resulting in decreased thermal conductivity due to frequency dependent scattering. Additionally, the quantitative relationship between three independent roughness parameters, σ, L and α_p has been measured and shown to have a greater effect on the thermal conductivity of SiNWs than diameter. Specifically, the power spectra of the roughness with a power law fit in the wavelength range of 1-100nm scales strongly with the reduction in thermal conductivity. Additionally, the fact that EE SiNWs also have shown good agreement on this correlation firmly supports our findings. With these results, it is clear that quantifying the surface roughness is crucial to both understanding the fundamental physics of phonon transport as well as engineering practical thermoelectric devices.

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Chapter 3

Integrated Holey Silicon Microdevices for All-in-One Thermoelectric Performance Characterization

It has been shown that the thermal conductivity of single-crystalline silicon nano-membranes significantly decreases upon addition of holey structuring without damaging the electrical properties. However, limited experimental evidence exists in aiding to elicit the underlying mechanism of the changes in phonon transport in this Holey Silicon (HS) material. Using fully integrated microdevices, we have performed simultaneous measurements of the thermoelectric properties (the Seebeck coefficient, electrical and thermal conductivity) to independently investigate electron and phonon transport associated with the neck size (i.e., the porosity) of the HS devices with varied carrier doping concentrations. Specifically, we observed thermal conductivity reduction below the incoherent phonon regime in HS with neck sizes in the range of 20 ~ 35 nm on the, leading to a new realm of the coherent phonon interaction. We also demonstrate that phonon and electron transport can be independently controlled, with a net effect of enhanced ZT. These results provide a fundamental understanding of the "phonon – periodic boundary" interaction, which can help provide design principles towards all-silicon thermoelectric devices.

3.1 Introduction

Upon the advent of exploiting unique nano-structured material properties, interest in thermoelectric energy conversion devices with the capability of harvesting thermal energy from solar, automobile, and industrial heat sources has been renewed.[1,2] The heat-to-electricity conversion efficiency of thermoelectric modules is dependent on the material-associated figure-of-merit, $ZT = \sigma S^2 T / \kappa$, where σ, S, κ, and T are electrical conductivity, the Seebeck coefficient, thermal conductivity, and absolute temperature, respectively. The Seebeck coefficient is an open-circuit voltage induced on a semiconductor under a thermal gradient, and scales inversely with the carrier concentration.[3,4] The thermal conductivity contains contributions from two species: quantized lattice vibrations (phonons) and electrons. In order to draw power from electricity producing devices, relatively high electrical conductivity, hence, carrier concentrations are required ($\sim 10^{19}$-10^{20}), thereby directing research focus on reducing phonon propagation to attain efficiency enhancement. If affecting phononic transport is done without affecting the corresponding electrical properties (Seebeck coefficient and electrical conductivity) ZT is no

longer constrained by the adverse interplay of parameters and power generation with thermoelectric modules would become a more viable avenue for thermal energy scavenging. [4,5]

Bulk Bi_2Te_3, the most widely used thermoelectric material, has ZT of ~1 at room temperature, but the large-scale production of Bi_2Te_3-based technologies is limited by high manufacturing cost, poor thermal stability, and relatively low abundance.[6] Silicon is the most abundant and widely used semiconductor with a vast industrial infrastructure. It has a high thermoelectric power factor (σS^2) comparable to that of Bi_2Te_3 when appropriately doped. However, the overall thermoelectric performance is poor (ZT ~ 0.01 at 300 K) due to the high thermal conductivity (~150 $Wm^{-1}K^{-1}$ at 300 K). Based on the fact that the phonon mean free path (MFP, 300 nm) is much longer than the electron MFP (5 ~ 10 nm) for degenerately doped bulk silicon, nanostructures could effectively dampen phonon transport without the addition of severe electron scattering, making silicon an unexpectedly useful thermoelectric material. Notably, Hochbaum $et~al.$ discovered that rough silicon nanowires could enhance ZT up to 0.6 at 300 K due to a large suppression in thermal conductivity with moderate deterioration in power factor. [7] Later, Lim $et~al.$ experimentally demonstrated that the high frequency surface roughness plays a key role to the suppression in thermal conductivity.[8] Unfortunately, the nanoscale surface roughness control on large-scale silicon nanowire devices remains problematic for realizing high performance silicon nanowire thermoelectric modules.

The holey silicon (HS) ribbons also achieved a nontrivial ZT ~ 0.4 at room temperature, due to the same effect of a thermal conductivity reduction, as reported by Tang $et~al.$ [9]Using block copolymer lithography, 100 nm-thick silicon membranes with nanoscopic hole arrays (pitch/neck ~ 55/23 nm) were demonstrated. This holey structure is more advantageous than the rough nanowire in terms of a large-scale fabrication, thanks to the controllability and scalability of block copolymer lithography and the compatibility with standard photolithography-based microfabrications. The HS thermal conductivity was significantly reduced down to ~ 2.03 $Wm^{-1}K^{-1}$ at room temperature, which was attributed to the "necking effect", where phonon with MFP longer than the pitch size of adjacent holes are trapped behind the hole based on Hao $et~al.$'s Monte Carlo (MC) simulation.[9,10] The thermal conductivity suppression in HS is comparable with the one in rough silicon nanowires and the degradation in thermoelectric power factor remains mild. Up to date, thermal conductivities of either HS ribbons or rough nanowires were characterized with devices different from the ones used for characterizing electrical conductivity and the Seebeck coefficient, due to the measurement and sample preparation limitation. However, the detailed nanometer-scaled morphology of HS could significantly alter all three thermoelectric properties (σ, S, and κ), and thus simultaneous thermoelectric property characterization is highly demanded for quantitative analysis of the "necking effect" of HS.

The significant reduction of silicon thermal conductivity was also observed in similar holey structures with various hole pitch/neck sizes, as reported by several other groups.[11-14] Although the molecular dynamics (MD) simulation indicated that phonons with MFP longer than 20 nm (i.e., comparable with the HS neck size) contribute more than 95% of heat conduction in bulk silicon, the underlying mechanism is still controversial as the "phonon – boundary scattering" could be incoherent or coherent (or even both) in a periodic holey structure with sub-100 nm hole feature.[15] El-Kady $et~al.$ reported thermal conductivities of 33 ~ 80 $Wm^{-1}K^{-1}$ at room temperature for 250 nm-thick silicon membranes with pitch/neck sizes of 500~900 /

200~450 nm.[12] Yu *et al.* obtained a much lower thermal conductivity of 1.9 Wm^{-1}K^{-1} for 20 nm-thick silicon nanomesh with pitch/neck size of 34/18~23 nm.[14] Both groups ascribed the thermal conductivity reduction to a phononic crystal, in which phonons coherently interact with periodic holey boundaries, and the phonon dispersion curve and the phonon group velocity are modified accordingly. In the MC simulation, Jain *et al.* predicted thermal conductivities that match well with El-Kady *et al.*'s experimental data, but both Tang *et al.*'s and Yu *et al.*'s experimental data (i.e., for HS with much smaller hole features, such as a neck of ~20 nm) clearly deviates from this prediction.[16] Notably, the MC model does not consider the coherent interaction and only suggest that phonons could scatter at holey boundaries diffusively and lose their wave information. This implies that a coherent boundary scattering needs to be taken into account to explain phonon transport in HS with hole pitch/neck of ~55/23 nm or smaller. Recently, Dechaumphai *et al.* postulated that the phononic Brillouin zone could be folded due to the periodicity of pores, and the model considered that phonons with MFP longer than neck size would scatter specularly at pore boundaries and obey the zone-folded dispersion curve. Although this model predicted thermal conductivities of HS with sub-100 nm features very well, the assumption that phonons scatter at surfaces specularly is somewhat aggressive and remains to be proven.[17] Hence, more detailed and accurate experimental studies are needed to understand the phonon transport mechanism in the unique holey structure.

In this report, HS ribbons were fully integrated into microdevices. Using this platform, the three thermoelectric parameters (σ, S, and κ) could be obtained from the same HS devices to assess the influence of various parameters, such as neck size, defects, doping level, and ribbon length to aid the design of silicon thermoelectric module. The monolithic contacts significantly limit parasitic thermal contact resistance, allowing for the precise measurement of thermal conductance. The neck size of HS with the same pitch of ~60 nm was also varied via the block copolymer lithography, which gave way for investigations on its effect on the thermal conductivity. Our data show that the decrease in thermal conductivity is well below the classical incoherent phonon regime, and matches better with the coherent phonon transport in such periodic holey structures. Consequently, by systematically tuning the electron and phonon transport, ZT enhancement was realized in HS devices.

3.2 Fabrication of HS Device

In order to achieve simultaneous thermoelectric property measurements, the HS microdevices based on the microdevices developed for thermal conductivity measurement by Shi *et al.* and Hippalgaonkar *et al* were re-designed. Figure 3.1 shows the schematic of the structures of the novel microdevice for HS ribbons as well as control silicon ribbons (i.e., without holes). Briefly, the fabrication was carried out using the standard 4" microfabrication facility, including nine photolithography steps, six dry etching processes, two wet-etching processes, one chemical vapor deposition of low-stress SiN$_x$, two metallizations, and one critical point drying. The 4" prime silicon-on-insulator (SOI) wafers were purchased from Soitec, and the ion implantations were conducted at Core Systems. For the study here, carrier concentrations at three different levels, 3.1 $\times 10^{18}$, 2.0 $\times 10^{19}$, and 6.5 $\times 10^{19}$ cm^{-3}, were obtained using boron as dopants. The thickness of the silicon ribbons is 100 nm and it varies ±10 nm depending on the fabrication conditions. The biggest challenge of the mirocdevice fabrication was the release of the silicon ribbon microdevices from the buried oxide layer and Si handle of the SOI wafers. We first

performed the deep reactive ion etching (DRIE) to etch through the handle wafer, and the fluorocarbon-based dry etching (CHF$_3$/Ar=80/4 SCCM, 150W) to etch-off the buried oxide. The high SiO$_2$/Si selectivity (>30/1) of fluorocarbon-based dry and the slow etching rate (20 nm / min for SiO$_2$) was applied, and the end point was determined by optical observation of oxide color and carefully confirmed by Scanning Electron Microscopy (SEM). We have achieved a ~30% yield rate of the microdevices after the releasing process.
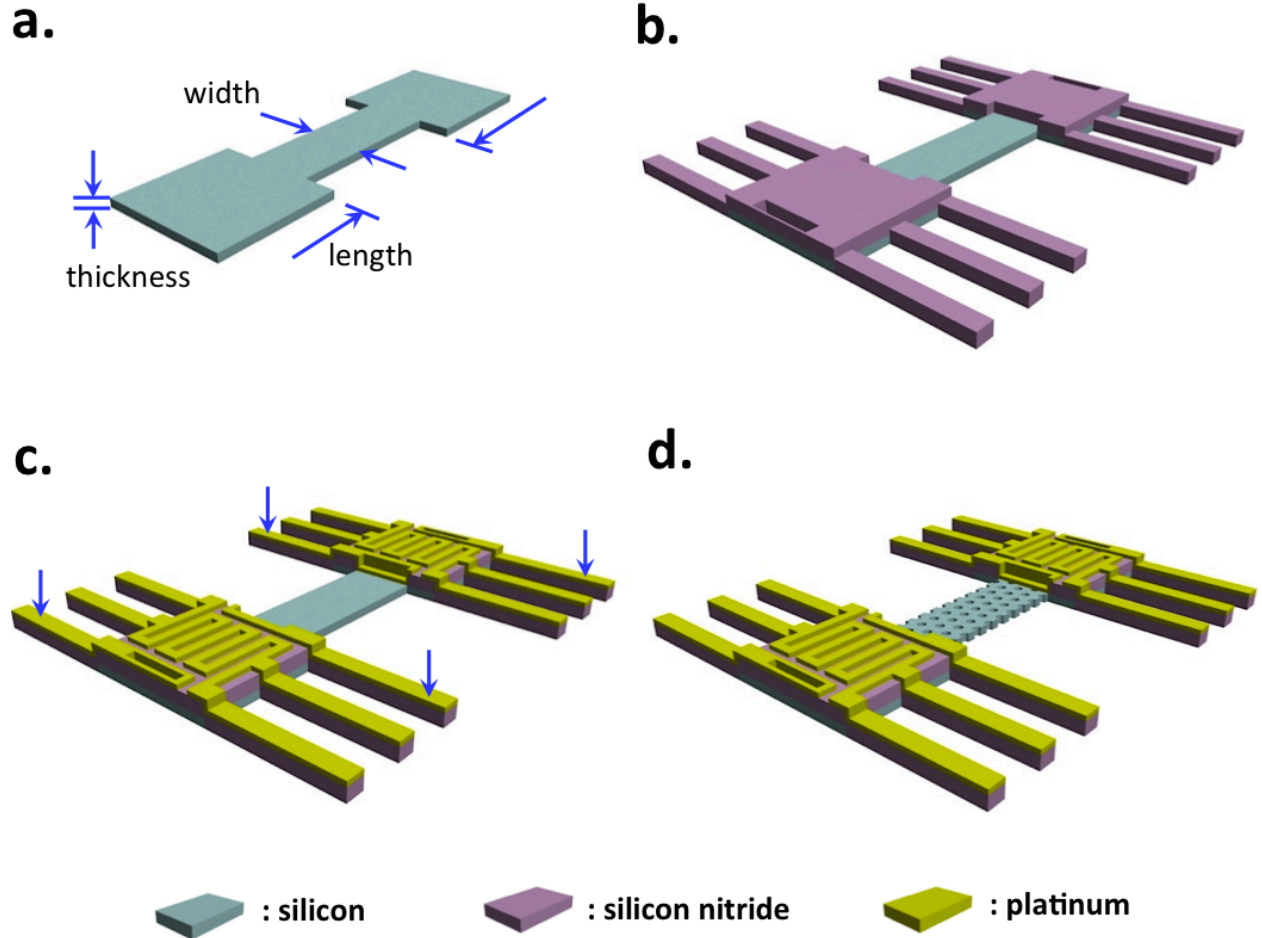
Figure 3.1 Schematic of the all-in-one microdevice. **(a)** A silicon ribbon consists of two end-pads (30×40 μm) for making thermal contacts with low stress SiN$_x$ pads. The length, width, and thickness of the silicon ribbon are as defined. **(b)** The thermoelectric measurement platform consists of two of Si/SiN$_x$ covalently bonded pads and the Si ribbon. The six legs of low stress SiN$_x$ for each end-pad are used to suspend the silicon ribbon. **(c)** A control silicon ribbon (without holes) microdevice. Four-point ohmic contacts (Cr/Pt=2/30 nm), marked by the blue arrows, are made to the silicon ribbon for electrical measurements. The rest legs are four-point contacts of the two PRTs. **(d)** A HS ribbon microdevice. A nanometer hole array are fabricated using the block copolymer lithography. Color codes are for Si, SiN$_x$, and Pt.
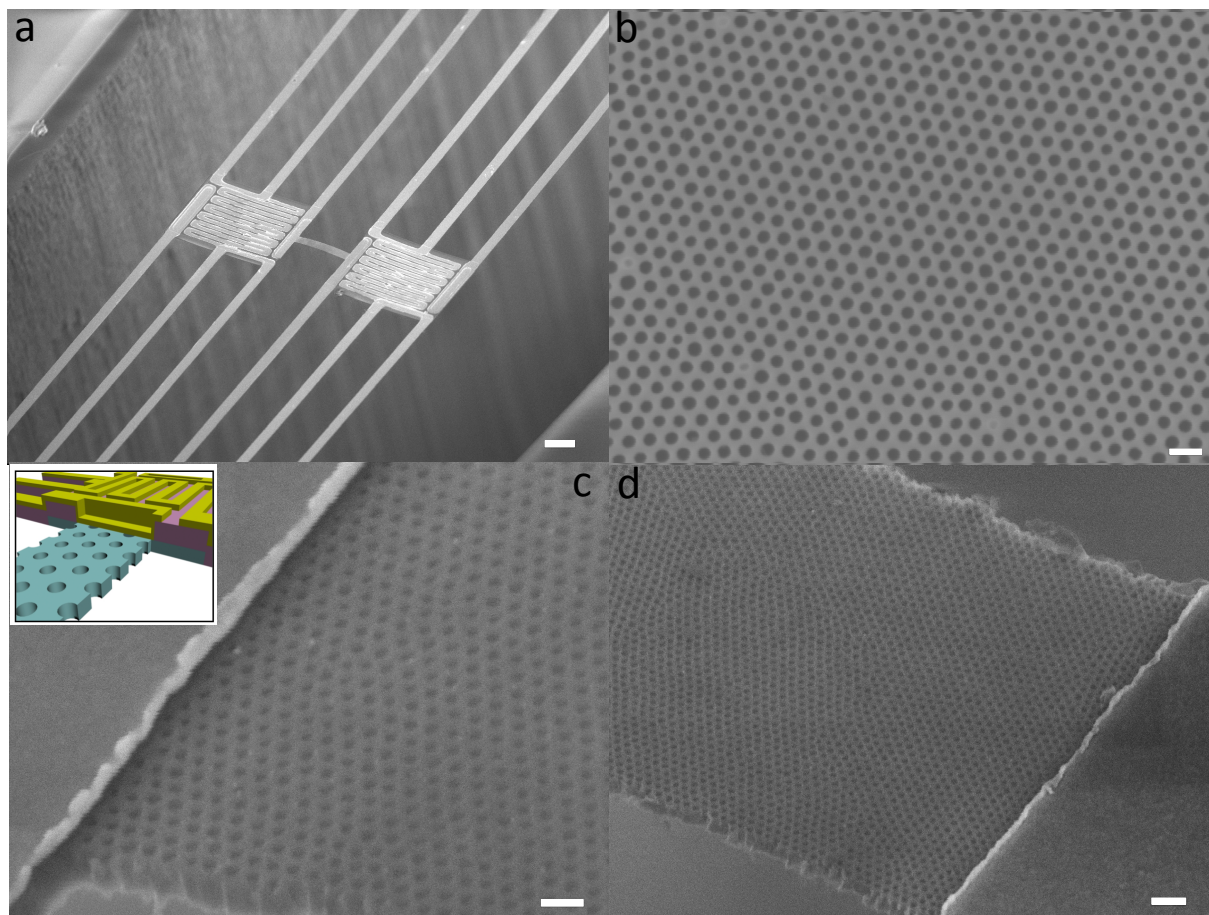
Figure 3.2 SEM images of the all-in-one HS ribbon microdevice. **(a)** The low magnification SEM image at a tilted angle of 60 degree. Inset is a schematic of a HS ribbon microdevice. **(b)** The SEM image of the top view of the HS ribbon. **(c)** The SEM image shows the holey structure with the monolithic Pt ohmic contact. Inset is a schematic for a comparison. **(d)** The SEM image shows the long-range order of the holey structure for the HS ribbon. Scale bars are 10, 20, 10, and 5 μm, respectively

In the integrated HS microdevices shown in Figure 3.1 (c) and (d), two end-pads of a silicon ribbon are monolithically integrated with two platinum resistance thermometers (PRT) through the low stress SiN_x pads. The covalent bonding between silicon ribbon end-pad and low stress SiN_x pad essentially eliminate the thermal contact resistance that is frequently observed in Pt/C composite bonding for nanowire or microribbons using electron beam induced deposition of focused ion beam (FIB) systems, or metal (such as Ni) bonding using e-beam evaporation through a shadow mask.[7-9] In additions, four-point ohmic contacts are made via e-beam evaporated Cr/Pt (2/30 nm), which allows to measure the Seebeck coefficient and electrical conductivity as well..

Figure 3.2 shows the SEM images of the fabricated HS microdevice. Poly(styrene-block-2-vinylpyridien) (PS-b-P2VP) block copolymer with molecular weight of 183.5kg mol^{-1} (M_n^{PS} =125 kg mol^{-1}; M_n^{P2VP}=58.5 kg mol^{-1}) and the molecular weight distribution of 1.05 was spun on a 300 nm thick silicon oxide chip, followed by solvent annealing for approximately 3 hours to enhance the lateral order of micellar arrays.[18] This highly ordered film was soaked in

ethanol for 30 minutes to produce nanopores by reconstructing the P2VP regions. (figure 3.3A) A thin chromium (Cr) film was deposited on the reconstructed block copolymer film at 60 degree, by which Cr could not block the holes of the block copolymer patterns, and a Cr holey mask was fabricated. To transfer the Cr holey mask from the oxide chip to the pre-fabricated microdevices, the Cr holey mask chip was first protected with an additional layer of block copolymer film, and then was immersed in <3% dilute HF bath. As the 300 nm SiO_2 was etched away, the protected Cr holey mask floated on the surface of the aqueous bath. The floated mask was transferred to clean DI water bath and picked up by a pre-fabricated microdevice chip. (Figure 3.3B) Oxygen plasma was then applied to remove block copolymer film and the holey Cr mask remained for etching the holes with DRIE. We could control the neck width (or porosity) by tuning both DRIE conditions and the Cr mask thickness. After the DRIE, Cr holey mask was etched away by a commercial Cr etchant, CR-7, for 1 minute. Finally, the HS microdevice could be suspended by the same procedures for releasing control silicon ribbon microdevices. Even though the block copolymer/Cr pattern does not damage or deform during the transfer to microdevices, it could tilt or lift slightly. As a result, the average pitch length of the holey structure decreased to 59 ± 2nm while that of block copolymer pattern is ~ 62 ± 2nm. (Figure 3.4)
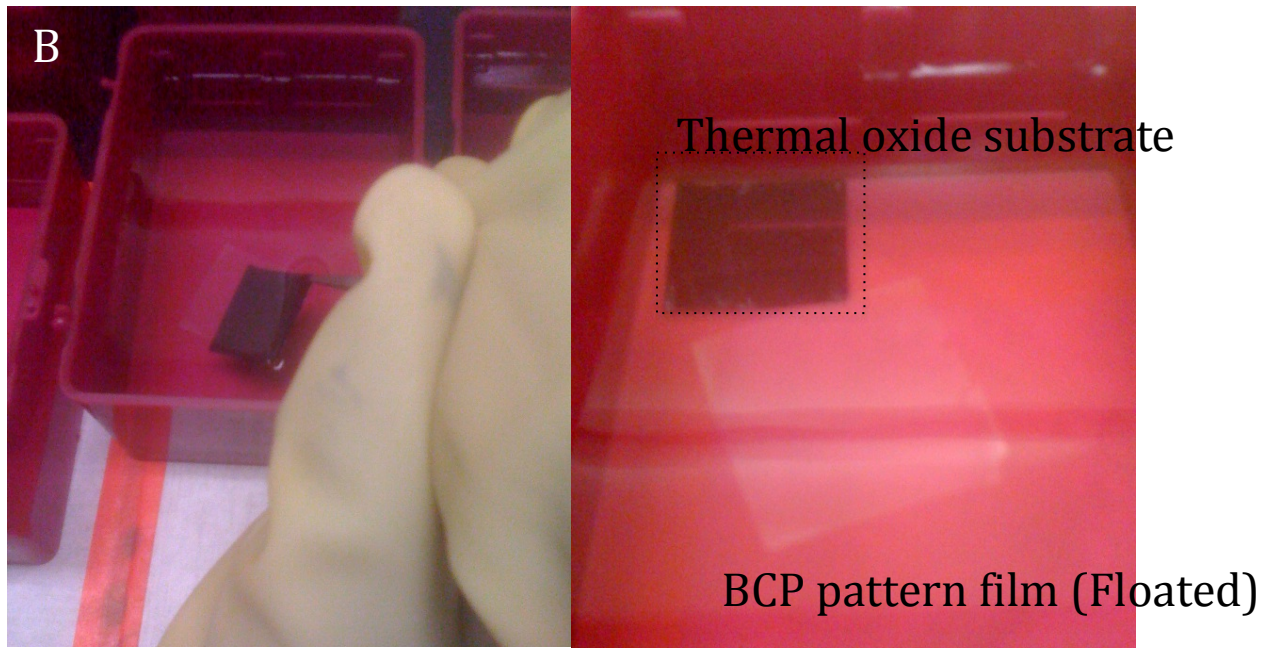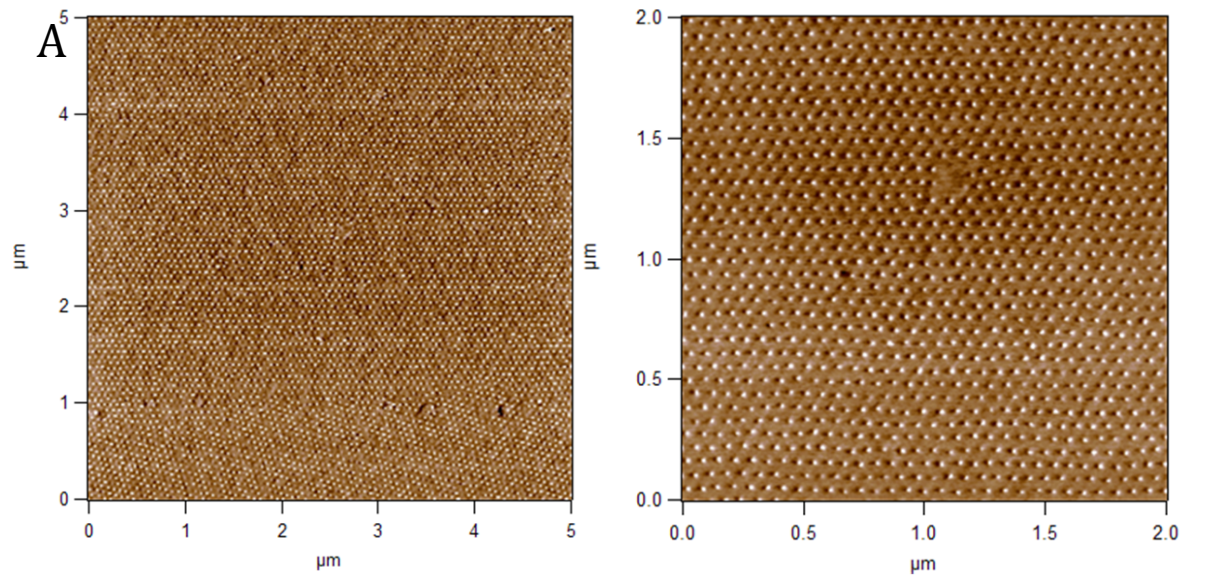
Figure 3.3 AFM images of block copolymer pattern (A) and pattern film transfer in dilute HF bath.(B) Thermal oxide layer on silicon substrate dissolves, floating the hydrophobic polymer layer on water surface. This film is transferred onto Fabricated microdevice.
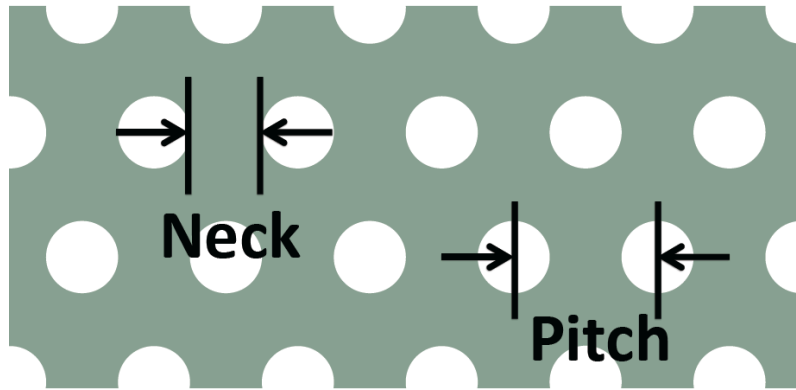
Figure 3.4 Schematic image of HS geometry. Neck is defined as closest distance between two adjacent holes. Pitch is the average periodicity of holes and measured from the center to the center.

3.3 Simultaneous Thermoelectric Measurements

The schematic of the simultaneous measurement is shown in figure 3.5. For each temperature, thermal conductivity and the Seebeck coefficient were measured simultaneously from the same HS microdevice. The thermal conductivity measurement technique can be found in Shi *et al.* report.[19] Briefly, a DC bias is applied to one PRT, creating a Joule heating and increases temperature of the PRT pad. A part of heat flows through the HS ribbon and raises the temperature of the other PRT pad. Thermal conductance can be obtained by calculating the heat flux through the HS ribbon and measuring the induced temperature difference between hot and cold PRT pads. Under the same temperature difference, open circuit voltage (i.e., the Seebeck voltage) was also measured across HS ribbon between the two inner ohmic contacts to extract the Seebeck coefficient ($S = -\Delta V/\Delta T$) at each temperature. In a separate run, the four probe I-V measurement was conducted at the same temperatures. The dimension and porosity/neck of HS ribbons were examined using SEM to calculate the thermal conductivity and electrical conductivity.

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a. thermal and Seebeck measurement
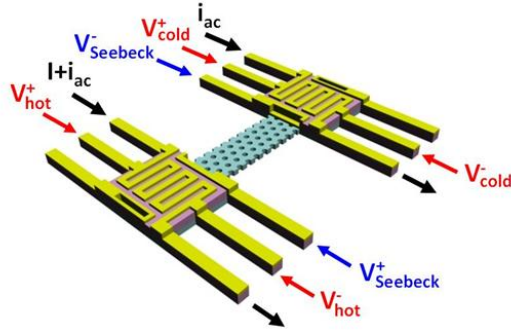
b. 4 probe electrical measurement
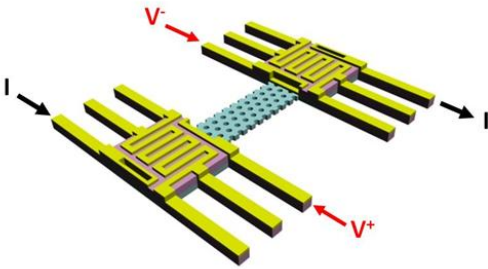
Figure 3.5 Schematic of the all-in-one measurements. **(a)** Electrical configuration for the thermal conductivity and Seebeck coefficient measurements. **(b)** Electrical configuration for the electrical conductivity measurements

3.4 Results and Discussion

Figure 3.6(a) and (b) shows the temperature dependence of the thermal conductivity of the HS ribbons, with varying necks and three different doping concentrations: 3.1×10^{18} cm^{-3} (low-doped), 2.0×10^{19} cm^{-3} (mid-doped), and 6.5×10^{19} cm^{-3} (high-doped), as well as the control silicon ribbons with the same three different doping concentrations. The thermal conductivity was calculated by normalizing the porosity (φ): $\kappa_{HS}/\kappa_{measured} = 1/(1-\varphi)$. The thermal conductivities of control silicon ribbons matches well with Goodson *et al.*'s data, which measured the thermal conductivity of thin silicon layer of SOI wafer.[20-22] The monolithic contact between the silicon end-pad and SiN$_x$ end-pad has improved the accuracy of the thermal conductivity measurement owing to the negligible parasitic thermal contact resistance, consistent with Hippalgaonkar *et al.*'s report.[23] The thermal conductivity of low- and mid-doped control silicon ribbons is comparable across the entire temperature range, despite the difference in doping levels. Matthiessen's rule suggests the total relaxation time, $\tau^{-1} = \tau_U^{-1} + \tau_{imp}^{-1} + \tau_B^{-1}$, where the subscripts U, imp, and B refer to Umklapp, impurity, and boundary scattering, respectively. Our data suggests that for low- and mid-doped samples, the total relaxation time is dominated by both the "Umklapp" and "phonon – boundary" scattering, but the "phonon – impurity" scattering is not significant. However, the thermal conductivity of the high-doped control sample is merely half of the thermal conductivity of low- or mid-doped sample, suggesting that the "phonon – impurity" scattering contributes a notable portion to total

relaxation time at this doping level. It should be noted that the defects induced by the ion implantation could also impede the phonon transport of our samples. Remarkably, the holey structure has dramatically reduced the thermal conductivity for the three doping levels. The fact that thermal conductivity of HS devices is lower than that of nanowires for given limiting dimensions, neck and diameters (~17 and 7 Wm^{-1}K^{-1} for 37 and 22 nm in diameter, respectively) is intriguing. Surface to volume ratio (nm^{-1})of HS is smaller than those of nanowires. Those of HS devices and nanowires are 0.09 and 0.11 for 37nm and 0.14 and 0.18 for 22nm, respectively. Scalloping was also minimized by the optimized DRIE recipe, which was confirmed from the cross-section SEM images. (Figure 3.B2) Thus, the suppression could not be fully explained by the classical BTE calculations which only consider incoherent phonon scattering.[17]
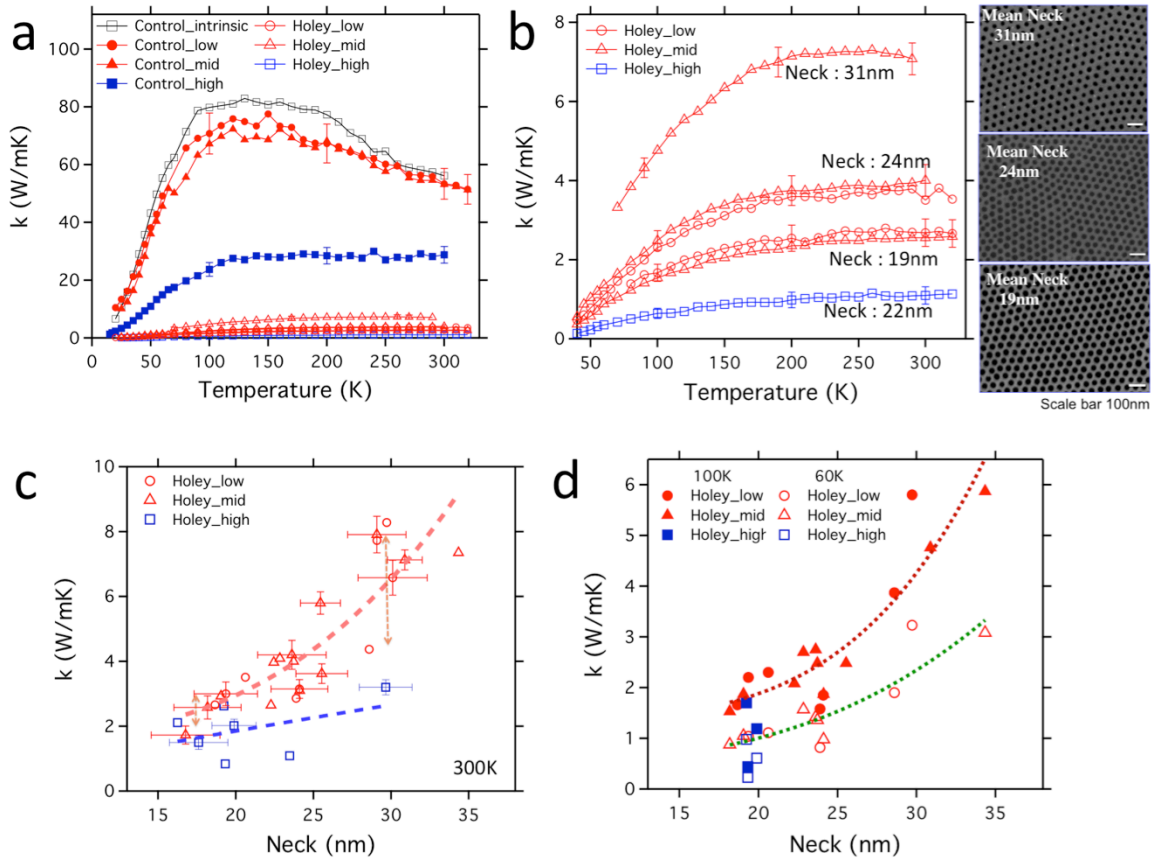
Figure 3.6 The thermal conductivities of the control and HS ribbons that are boron-doped with different doping levels: 3.1×10^{18} cm^{-3} (red circle), 2.0×10^{19} cm^{-3} (red triangular), and 6.5×10^{19} cm^{-3} (blue square). Solid circles, triangles, and squares are for control silicon ribbons. Open circles, triangles, and squares are for HS ribbons. **(a)** The temperature-dependent thermal conductivities of control silicon and HS ribbons with varied doping concentrations. The intrinsic control ribbon is also measured as a comparison. **(b)** The magnified temperature-dependent thermal conductivities of HS ribbons with different neck sizes. The mean necks were estimated from the porosities based on SEM images thought the entire ribbons. Inset: the SEM images of three different mean neck size (scale bar = 100 nm). **(c)** The plot of HS thermal conductivities at 300 K as a function of the neck size for different doping levels. (d) The thermal conductivity vs.

neck plot at cryogenic temperature with fitted line to low and mid doped HS devices at 100K (red) and 60K(green)

As previously explained, there are two main approaches to explain thermal conductivity in holey structures, coherent, incoherent, and a mixed mechanism. To systematically probe the incoherent phonon – boundary scattering, we keep the pitch of the holey structure the same across all HS samples, by which the alteration to phonon dispersion curve would maintain (Brillouin zone reduced from π/a to π/P, a : lattice constant of silicon and P : pitch size), if coherent phononic crystal effect exists. Using the average pitch size of 59 ± 2nm, we carefully tuned the neck width from ~16 nm to ~35 nm with 2~3 nm of standard deviation In this systematic manner, contribution of incoherent "phonon – boundary scattering" to the thermal conductivity is mostly measured while the coherent phonon interaction as the thermal conductivity varies prominently with varying the neck size. This is consistent with Dechaumphai *et al.*'s simulation work where they separately define 'coherent' phonons (MFP > neck size) and 'incoherent' phonons (MFP < neck size).[17] The coherent phonons are modeled using zone-folded dispersion curve and incoherent phonons was considered to scatter at boundary diffusively like particles with no change in dispersion curve. The total thermal conductivity, as a sum of coherent and incoherent phonons, decreases monotonically as the neck size decreases. For instance, coherent phonons contribute ~ 1 $Wm^{-1}K^{-1}$ to thermal conductivity while the contribution of incoherent phonons varies 0.36 to 2.51 $Wm^{-1}K^{-1}$ as neck size increases from 18 to 31 nm with fixed pitch at 34 nm. As shown in Figure 3.4(c) and 3.4(d), the neck size plays a significant role in reducing thermal conductivity in holey silicon. As the neck size varies from 16 to 31 nm, the thermal conductivity varies from 0.8 and 8.3 $Wm^{-1}K^{-1}$. The low temperature (100K and 60K) plot shows better correlation with clearer trend since boundary scattering is more dominant in the temperature regime. For the same neck size, the thermal conductivities of the low- and mid-doped HS ribbons are very comparable. The high-doped HS ribbons (neck = 25 ~ 35 nm) in general show a lower thermal conductivity than samples with other doping levels, suggesting that the "phonon - impurity scattering" still plays a key role. When the neck size decreases (neck = 18 ~ 25 nm), the thermal conductivity shows no dependence on the doping levels, suggesting that "phonon - boundary scattering" dictates the thermal conductivity. It should be noted that even though we plot the thermal conductivity as a function of neck size, there could be other minor effects on phonon scattering in our HS systems, such as the distribution of neck size, degree of ordering, ion implantation defects, and surface states.

We tentatively attribute this thermal conductivity reduction to a combination effect of coherent and incoherent phonon. The decrease in thermal conductivity became less sensitive as the neck width became shorter than 25nm and this trend is much clearer at low temperature (100K) in boundary scattering dominant regime.(Figure 3.6d) This may suggest that the HS structure is not longer within incoherent dominant regime but coherent regime where the phonon transport is affected by the pitch size. Thus, the thermal conductivity should not change much with fixed pitch size (~60 nm) although the neck size decreases (25 – 16 nm) in this regime.[17] Similar to HS, Yu *et al.* ascribed the low thermal conductivity of silicon nanomeshes to a coherent phonon scattering for the nanomesh structure with pitch/neck size of 34/18~23.[14] With the neck similar to our system, their shorter pitch may enhance coherent phonon scattering leading to a lower thermal conductivity.[17] Even though the coherent scattering mechanism seems to reasonably explain the experimental data, many questions remain to be answered. First, one or

two nanometer variation in periodicity of a holey array may disturb the coherent effect since most of phonon wavelength is order of 1 ~ 10nm.[15] However, Asegun *et al.* argued that the range of wavelength can be broader up to 100 nm and a few nanometer variations in pattern may not damage the coherency severely.[24] Second, phonons with MFP longer than neck size do not necessarily scatter at boundary specularly.[8,25-27] Although wavelength-dependent boundary scattering is actively investigated it has not came to concrete conclusion on accurate scattering mechanism. Hence the assumption that phonon scatter at boundary specularly needs more investigation.[25]

More theoretical studies on similar nano-porous structures to predict thermal conductivity also exist.[10,16,28,29] He *et al* conducted molecular and lattice dynamics calculations for nano-pores smaller than 10 nm and predicted about two order of magnitudes lower thermal conductivity than that of bulk.[28] They found that non-propagating vibrational modes (diffusons) appear more dominantly when pitch became smaller and the surface boundary became disordered. Although their results qualitatively explain our trend, their calculation is limited to sub 10 nm features and hence diffusons may not appear in our HS devices. Previously, Tang *et al* postulated the 'necking effect' where phonons with MFP longer than spacing between adjacent holes are trapped behind the hole based on the Monte Carlo simulation by Hao *et al.*[9,10] In their modeling work, when the spacing between holes are smaller than MFP of phonons, ballistic phonon transport prevails and thermalizes the boundary of hole facing the incoming heat flow. This region will be locally hotter than other area thermalized by diffusive phonon transport. Similarly, the opposite side of hole will be locally cooler and the local inverse temperature gradient can form. However, the model still overestimates experimental data.
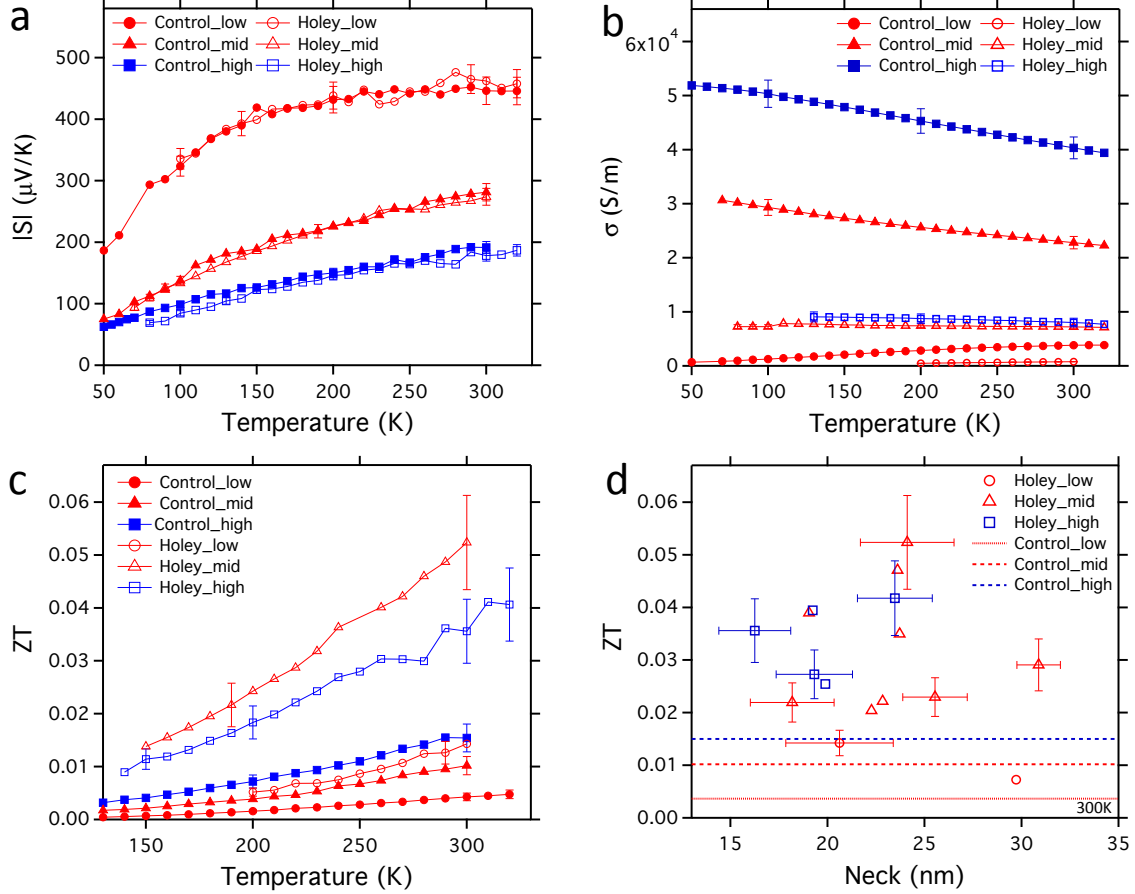
Figure 3.7   The temperature-dependent (a) Seebeck coefficient, (b) electrical conductivity, and (c) overall ZT of the control silion ribbons and HS ribbons. (d) Plot of ZT with respect to the neck size at 300 K. The ZT of control silicon ribbons (dashed lines) are also provided for a comparison

As seen in Figure 3.7(a), the average Seebeck coefficients of mid- and high-doped HS ribbons are 270 ± 12 and 197 ± 12 µV/K at room temperature, which are comparable to that of mid- and high-doped control silicon ribbons, 280 and 190 µV/K, respectively. In the simplified picture, the Seebeck coefficient is a measure of asymmetry of density of state near the Fermi level, which can be described by the equation:

$$S = \frac{1}{eT} \frac{\int \sigma(E)(E-E_f)dE}{\int \sigma(E)dE}$$

where e, σ, E, and E_f are charge of a electron, electrical conductivity, energy of electrons, and the Fermi level, respectively. It suggests that the change in the band structure due to the periodic holes was negligible or not big enough to be measured in the Seebeck coefficient.[30] However, low-doped HS ribbons shows ~5% increase in the average Seebeck coefficient from 446 µV/K to 470 ± 12 µV/K. It is demonstrated that the surface states depletes the mobile charges and further lower the Fermi level in the p-type HS ribbons.[31] The electrical conductivity of control silicon and HS ribbons are plotted in figure 3.7 (b), which clearly shows that the electrical conductivity is also substantially decreased by the holey structure. The silicon dangling bonds at Si-SiO$_x$ surfaces have positive charges, which induce depletion layer to reduce the charge conduction channel within HS.[31] The depletion width is inversely proportional to carrier concentration, so

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low-doped HS samples suffer more severely than high-doped samples, leading to increase in the Seebeck coeffcient..Although the surface states can be removed by forming a thin thermal oxide, it cannot be an option for the HS devices because the metalized electrical contact could not survive at an oxidation temperature. Instead, we passivated HS with 3 ~ 5 nm-thick Al_2O_3 layer by atomic layer deposition (ALD), followed by annealing at 500 °C for 30 minutes.[32,33] The electrical conductivity increased by ~30% for mid doped HS as shown in figure 3.8. Further, the lattice sites damaged during the ion implantation may additionally block charge carrier transport when the neck size is as small as tens of nanometers.[34] The overall ZT of the HS ribbons are shown in figure 3.7 (c) and 7(d). We obtained the optimal ZT with a carrier concentration of 2.0 $\times 10^{19}$ cm^{-3} and a neck size of 25 nm. We believe that the ZT can be further improved from several aspects, such as using a thermal diffusion to prevent the ion implantation defects, passivating surface dangling bonds by a high temperature dry oxidation, reducing the pitch and/or neck of the holey structure to further reduce thermal conductivity. The band gap of silicon is ~ 1.1eV and it is expected to show maximum ZT at 400~600 °C. Our HS microdevices have the monolithic thermal contact between silicon and silicon nitride pad, and the Pt ohmic contact is also suitable for high temperature measurements up to 600 °C. It is currently under the investigation to probe thermoelectric properties of HS devices at the high temperature region.
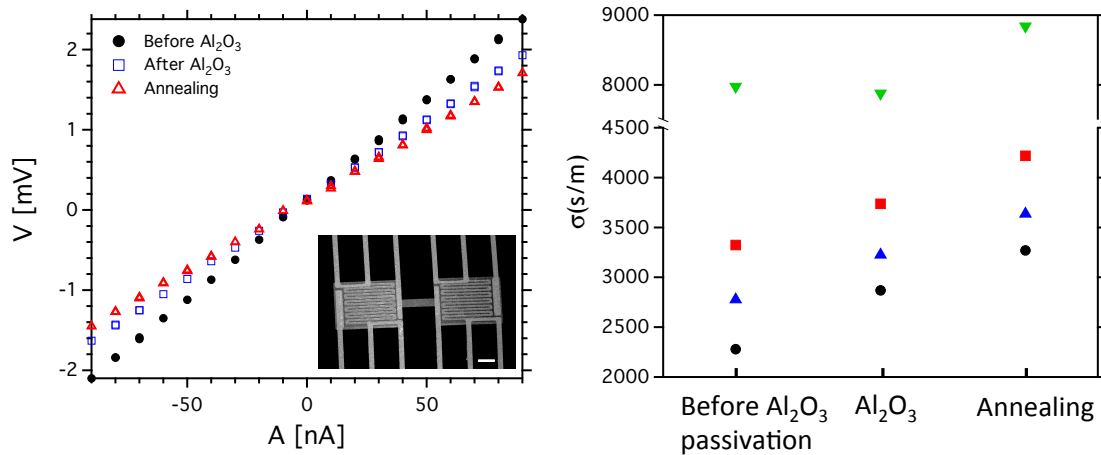

Figure 3.8 . Conductivity of HS devices before and after passivation with Al_2O_3 layer by atomic layer deposition (ALD) and followed by annealing at 450 °C for 30min in Ar/H_2 gas **(a)** 4 probe I-V curve. The inset shows an SEM image of the measured device. Scale bar is 10μm. **(b)** Change in electrical conductivity for multiple devices. 13% increase after passivation only and 28% increase with passivation and annealing combined.

3.5 Conclusion

In conclusion, we have integrated HS ribbons to the microdevices where three thermoelectric properties were measured from the same sample. The integration between block-copolymer based nanofabrication and conventional microfabrication opens the possibility for all-silicon based thermoelectric devices. The monolithic silicon thermal contact in the devices allowed the precise characterization of thermal conductivity. The necking effect on thermal conductivity reduction is well below incoherent phonon regime and sheds light on new types of

phonon scattering in periodic boundary structures in coherent phonon regime. Furthermore, we demonstrated decoupled electron and phonon transport using the holey nanostructure, with ZT enhanced 2~5 folds. With these results, it is clear that quantifying the necking effect is crucial to both understanding the fundamental physics of phonon and electron transport as well as engineering practical thermoelectric devices.

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3.7 Appendix A : Raman spectroscopy studies
- Checking anharmonicity of lattices

For Raman spectroscopy studies, the holey silicon layers were released from the SOI substrates and transferred to other substrates correspondingly. The buried oxide layer was first removed by vapor HF and then the silicon layers were detached from the substrates using a manipulator. For Raman measurements, both holey silicon and thin-film silicon layers were transferred onto a silicon substrate covered with a tungsten layer. Tungsten was chosen because of its high silicide formation temperature. Confocal Raman spectroscopy (HORIBA LabRAM HR Evolution) was performed in backscattering configuration with a helium–neon laser (632.8nm wavelength) and a 100x 0.9NA objective. The laser power was set to 6.1 μW and the laser spot size was smaller than 1μm. The samples were heated using a hot stage for the measurements in ambient air.
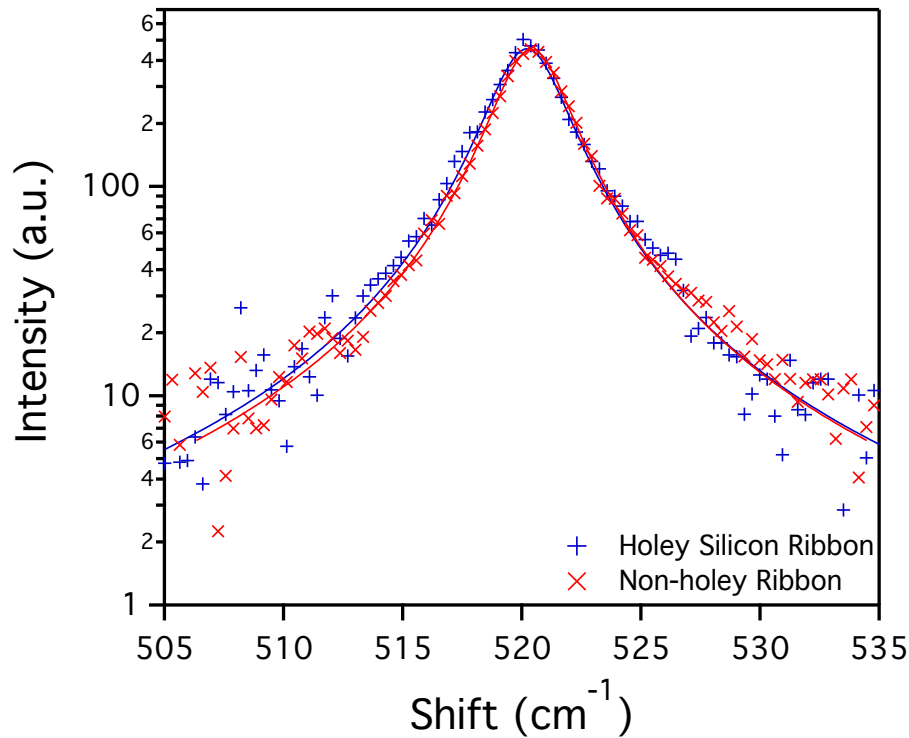
Fig. 3.A1. Raman spectroscopy data at 50 °C. The full-width at half-maximum (FWHM) is 3.33 cm[-1] for holey silicon and 3.27 cm[-1] for thin-film silicon here, but their difference is within the measurement uncertainty.

   Raman spectroscopy has been performed on both holey silicon and thin-film silicon samples to investigate potential impacts of dry etching and creating nano-holes on phonons, i.e. phonon localization, changes in anharmonicity, and strain effects.[1-3] For examples, phonon localization effect may red-shift and broaden Raman peaks by a relaxation of the fundamental phonon selection rule at the zone center.[4] Reactive ion etching processes may create nanocrystalline domains near the etched boundaries, which also lead to red-shifted and broadened Raman peaks.[2,5] However, our Raman data on holey silicon samples do not show a significant peak shift or broadening compared to that of thin-film silicon samples. This indicates that our holey silicon may not have appreciable amounts of nanocrystalline domains or defects, which is also consistent with HRTEM images. Since Raman peaks are sensitive to temperature, the temperature of the sample is carefully controlled by a heater stage and the excitation laser power is kept low to minimize local heating. The local heating effect is subject to the thermal conductance and the thermal contact resistance of each sample, and this can lead to a variation in Raman spectrum. The peak position and the full-width at half-maximum (FWHM) values of thin-film silicon samples are 520.45 ± 0.02 cm[-1] and 3.27 ± 0.01 cm[-1], respectively. The peak position and the FWHM values of holey silicon samples are 520.18 ± 0.10 cm[-1] and 3.53 ± 0.18 cm[-1], resepctively. The stage temperature was at 50°C. The difference between the two samples is within the measurement uncertainty, and we assume the Raman red-shfitng or broadening effects is not significant in our samples. We also studied temperature dependence of the Raman spectra of individual HS ribbons in the temperature range of about 30°C to 300°C. (Figure 3.A2 and A3)
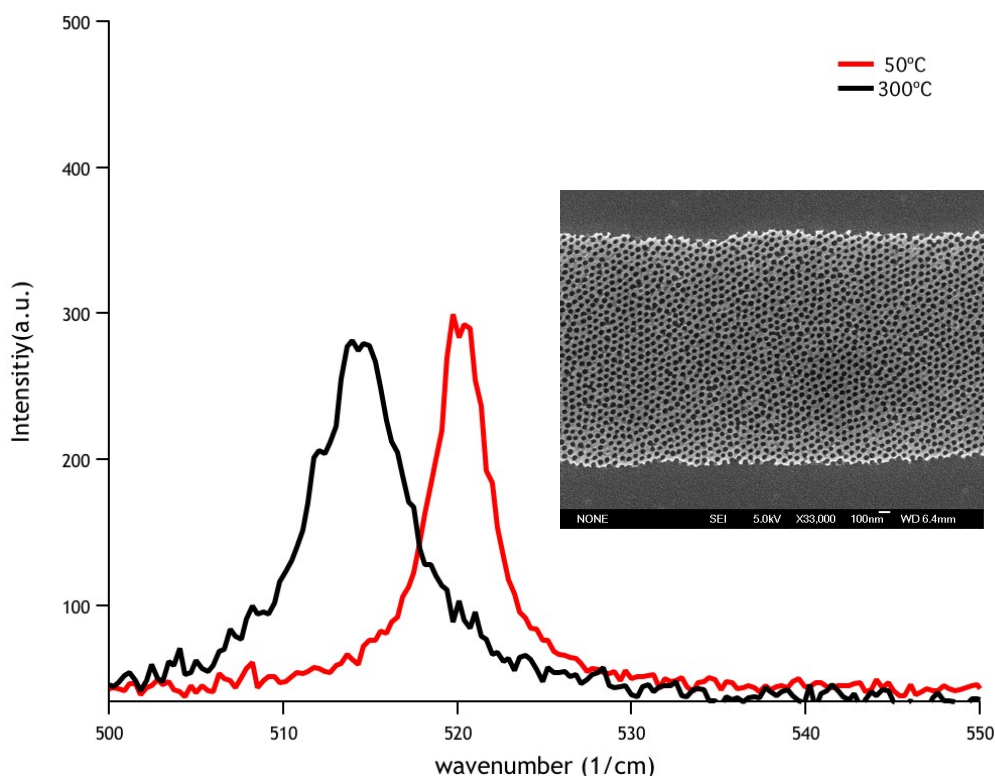

49

Fig. 3.A2. Raman spectra of HS ribbon at 50°C and 300°C. Inset shows the SEM image of HS ribbon in this study.

The peak position shifts with temperature and the relation is given as follows.
$W(T) = W_0 + \Delta_{TE}(T) + \Delta_A(T)$
Where W_0 : frequency at 0K, $\Delta_{TE}(T)$: frequency shift due to thermal expansion , and $\Delta_A(T)$: frequency shift due to anharmonic phonon-phonon decay (Three phonons – Four phonons.
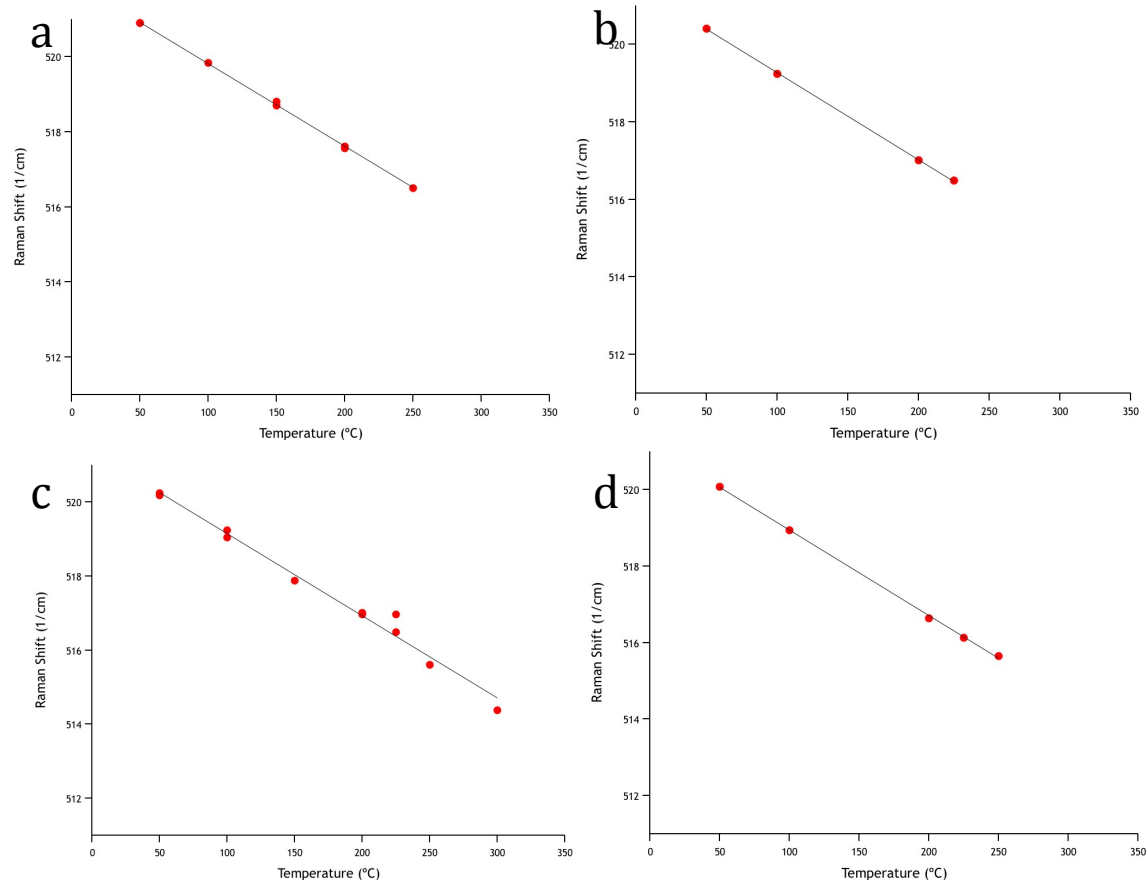
Fig.3.A3 Raman peak as a function of temperature (a) bulk silicon (b) silicon thin film (c)(d) HS ribbon1 and 2.

The slopes of Raman peaks are found -.0220 ±0.0002, -0.0224 ±0.0002, -.0228 ±0.0006, and -.0233 ±0.0003 cm^{-1}/K for bulk silicon, thin film, HS ribbon 1 and 2, respectively. Even though the slope of HS1 and 2 are ~6% steeper than bulk, suggesting that anharmonicity of lattice may slightly increase, this difference is still within the measurement uncertainty and match to the bulk value and further investigation is being undertaken. [37]

3.8 Appendix B

Microdevice Fabrication Detail

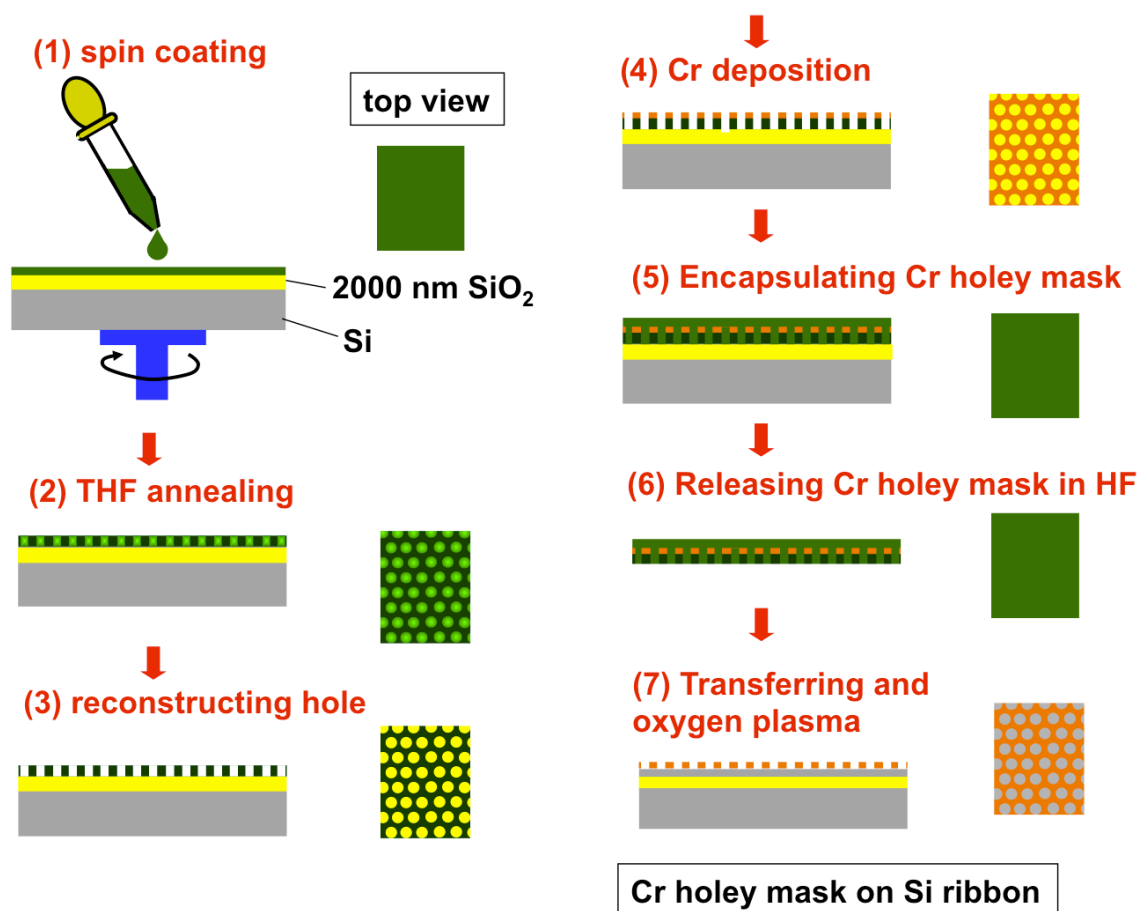The fabrication processes for the all-in-one microdevices were performed in UC Berkeley Microfabrication Laboratory or Marvell Nanofabrication Laboratory, except that the low-stress silicon nitride (SiN_x) was grown using Stanford Nanofabrication Facility. Figure 3.1 shows the schematic of the device fabrication process. For simplicity, the schematic of the device only at a few fabrication stages are showed here. The fabrication processes were carried out using the standard 4" microfabrication processes, including nine photolithography steps, six dry etching processes, two wet-etching processes, one chemical vapor deposition of low-stress SiN_x, two metallizations, and one critical point drying. As illustrated in Figure 3.1a, the silicon ribbons were first defined using the photolithography (gcaws2), and the deep reactive ion etching (DRIE) was performed to tailor the ribbon (2 cycles of passivation/etching by sts. For passivation: C_4F_8= 100 SCCM, 600 W, 7 seconds; for etching: SF_6/O_2=130/10 SCCM, 600 W, 9 seconds). The ~300 nm-thick low-stress SiN_x, required for suspending the microdevice, is then deposited (SiH_2Cl_2/NH_3=100/25 SCCM, 140 mTorr, 835°C, 90 minutes, by tylannitride at Stanford). The covalent bonding between low-stress SiN_x and silicon ribbons results a low thermal resistance at the SiN_x/Si interface, which greatly improves the accuracy of the thermal conductivity measurement, particularly for control silicon ribbons as shown in our thermal measurements. The reactive ion etching (CHF_3/CF_4=30/90 SCCM, 100W, 250~400 seconds, by ptherm), followed by a HF etch, was performed to open the top surfaces of the silicon ribbons and to open the windows for the four-point metal contacts; the micodevice at this stage can be illustrated by Figure 3.1b. Chromium/Platinum (Cr/Pt = 2/40 nm, by ultek) was then e-beam evaporated to make contacts to the silicon ribbons. Cr/Pt (2/30 nm, by ultek) was deposited again to make the platinum resistance thermometers (PRT, also used as Joule heating element). The rapid thermal annealing (630 °C for 30s, by heatpulse2) was conducted to ensure the ohmic contacts to the doped silicon ribbons. The microdevices were then patterned (gcaws2) and subjected to the reactive ion etching (CHF_3/CF_4=30/90 SCCM, 100W, 600 seconds, by ptherm) to from two PRT supporting pads and to remove the un-wanted low-stress SiN_x. At this stage, the microdevices were finished for control silicon ribbons, as illustrated by Figure 3.1c, except that the microdevices were still attached to the SOI substrate.
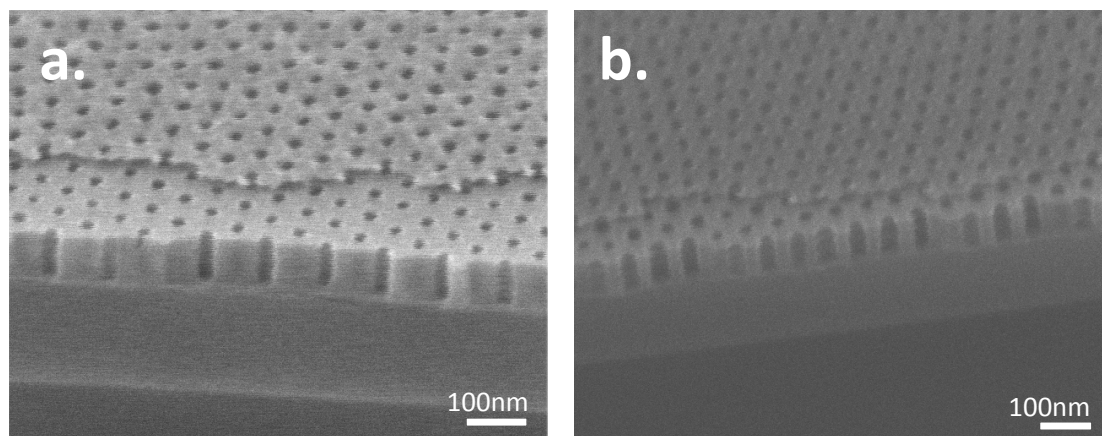
To release the microdevices from the buried oxide and the handle wafer, the back-side etching windows were defined by photolithography and reactive ion etching (CHF_3/CF_4=30/90 SCCM, 100W, 600 seconds) was performed to etch away SiN_x to form etching windows. The 4" wafers were then diced into 8×8 cm-sized chips (as shown in Figure 3.B3a), consisting of 72 ZT devices, for the through wafer etching (i.e., the releasing process). The thick photoresist (SPR-220, 1.8k rpm, hot-baked at 120°C for 30 mins) was used as the etching mask, and the etching window was opened again by photolithography. Prior to the through wafer etching processes, the chip front-side (i.e., the device side) was coated with regular photoresist (g-line, OCG 825 35CS) to protect the silicon ribbons, and the chip was then bonded, back-side up, to a 4" handle wafer. For the through wafer etching, the DRIE (565 cycles of passivation/etching by sts, For passivation: C_4F_8= 100 SCCM, 600 W, 7 seconds; for etching: SF_6/O_2=130/10 SCCM, 600 W, 9 seconds) was performed to fully etch away the 450 μm-thick handle wafer of the SOI sample. Utilizing the high etching selectivity (SiO_2:Si > 30:1) and the ultra slow etching rate (20 nm / min for SiO_2), the fluorocarbon-based dry etching (CHF_3/Ar=80/4 SCCM, 150W) was performed to etch way the buried oxide of the SOI sampls. The devices were finally suspended by dissolving the protective photoresist in the commercial photoresist stripper (PRS-3000, 80°C for 12 hours), and then dried in carbon dioxide critical fluid. A released all-in-one microdevice with a control silicon ribbon can be illustrated in Figure 3.1c.

For HS ribbons, we developed a scalable nanolithography process based on block co-polymer (BCP) assembly, as shown in Figure 3.B1. Poly(styrene-block-2-vinylpyridien) (PS-b-P2VP) block copolymer with molecular weight of 183.5 kg mol^{-1} (M_n^{PS}=125 kg mol^{-1}; M_n^{P2VP}=58.5kg mol^{-1}) and molecular weight distribution of 1.05 was spun on 2000 nm-thick silicon oxide substrates, followed by a vapor phase toluene annealing for approximately 3 hours to enhance the lateral order of micellar arrays.[2] The highly ordered film was soaked in ethanol for 30 minutes to produce nanometer-sized pores by reconstructing the P2VP regions. A thin Cr film was deposited using e-beam evaporation (ultek) on the reconstructed BCP film at 60 degree, by which chromium could not block the holes of the BCP patterns, and consequently a Cr holey mask was made.

To transfer the Cr holey mask from the oxide chip to the pre-fabricated microdevices, the chip was first protected with an additional layer of BCP film, and then was immersed in a dilute HF (<3%) bath. As the 2000 nm-thick SiO_2 was etched away, the protected Cr holey mask floated on the surface of the aqueous bath due to its hydrophobicity, and was rinsed and picked up by a pre-fabricated microdevice chip. A oxygen plasma was then applied to remove the BCP film, so the holey Cr mask remained for following the holey structure etching. Using DRIE, we could control the neck width (or porosity) of the holey silicon by tuning the etching parameters and changing the Cr mask thickness, as shown Figure 3.B2. After the DRIE, the Cr holey mask was etched away by dipping in a commercial Cr etchant, CR-7, for 1 minute. Finally, the HS microdevices were suspended using the same procedures for releasing control silicon ribbon microdevices. A released all-in-one microdevice with a holey silicon ribbon can be illustrated in Figure 3.1d. We have achieved a yield rate of ~30 % for releasing HS microdevices, as shown in Figure 3.B3.

(1) spin coating

top view

2000 nm SiO₂

Si

(2) THF annealing

(3) reconstructing hole

(4) Cr deposition

(5) Encapsulating Cr holey mask

(6) Releasing Cr holey mask in HF

(7) Transferring and oxygen plasma

Cr holey mask on Si ribbon

Figure 3. B1.   Schematic of the block copolymer based lithography.

a.

100nm

b.

100nm

Figure 3. B2   SEM images (tilted by 60 degree) of the two different HS membranes right after the DRIE etching. The Cr holey mask, as the top layer, remained. Using different SOI substrates (device layer =100 nm; buried oxide = 200 nm), the DRIE calibration was conduct to determine the targeted HS porosity/neck, and the DRIE was then performed to make HS microdevices. **(a)** The porosity is ~ 20%, which was achieved by the DRIE (2 cycles of passivation/etching by sts.

For passivation: C_4F_8= 100 SCCM, 600 W, 7 seconds; for etching: SF_6/O_2=130/10 SCCM, 600 W, 9 seconds) and a thicker Cr mask (10 nm). **(b)** The porosity is ~ 34%, which was achieved by the DRIE (2 cycles of passivation/etching by sts. For passivation: C_4F_8= 100 SCCM, 600 W, 7 seconds; for etching: SF_6/O_2=130/10 SCCM, 600 W, 9 seconds) and a thinner Cr mask (7 nm).
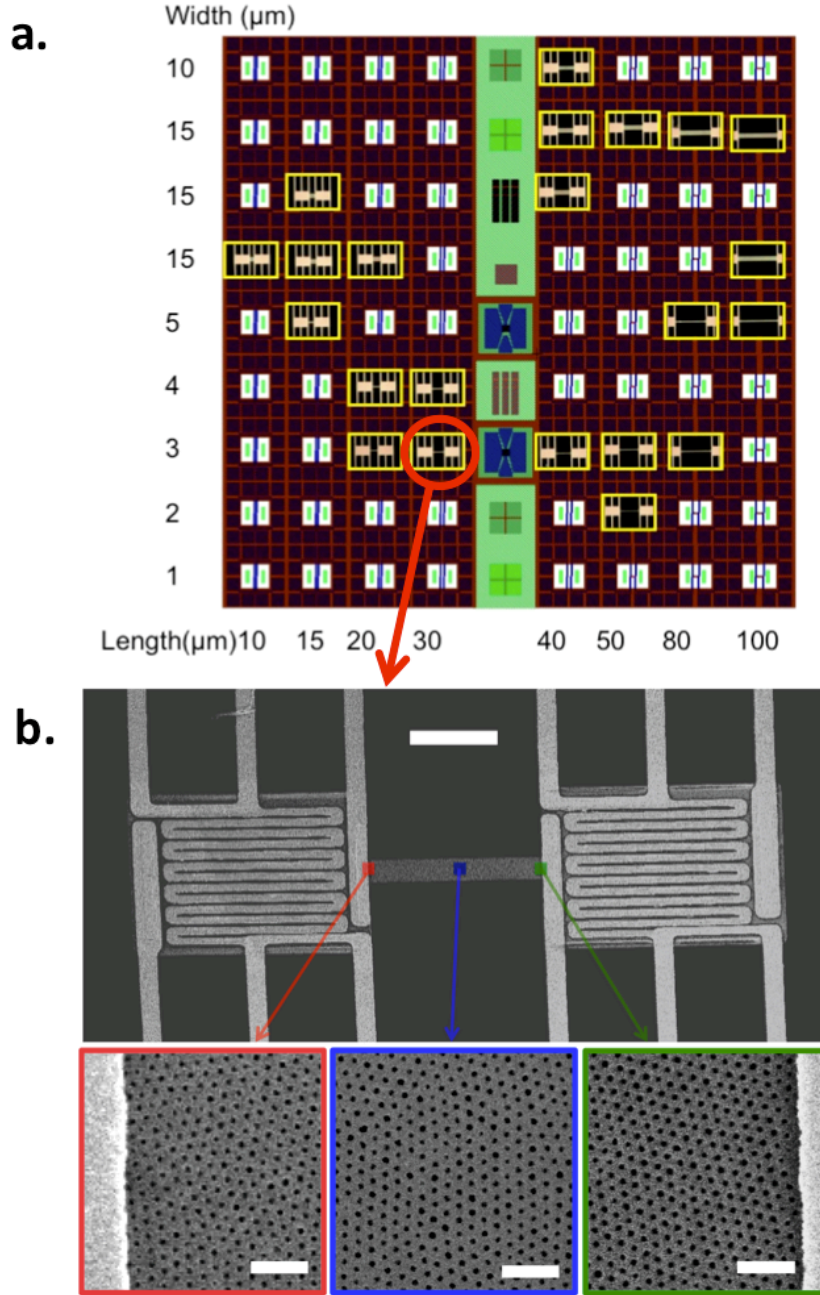
Figure 3 B3   **(a)** L-edit layout of the all-in-one microdevice chip (~ 8×8 mm), consisting of 8×9 HS mircodevices. The optical images of the released HS mircodevices are placed on the layout, corresponding to the individual ribbon length and width. For this chip, the yield for releasing HS mircodevices is ~30%.   **(b)** SEM images of the HS microdevice (ribbon width= 3 μm; length =30 μm) from the same chip. The holey structure was characterized through the

entire ribbon to ensure the morphology uniformity. The porosity (~17%) and average neck (35 nm) of this HS ribbon was extracted from the SEM images.

3.9 Reference

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(3)   Doerk, G. S.; Carraro, C.; Maboudian, R. *Physical Review B* **2009**, *80*, 073306.
(4)   Sui, Z. F.; Leong, P. P.; Herman, I. P.; Higashi, G. S.; Temkin, H. *Applied Physics Letters* **1992**, *60*, 2086-2088.
(5)   Adu, K. W.; Gutierrez, H. R.; Kim, U. J.; Sumanasekera, G. U.; Eklund, P. C. *Nano Letters* **2005**, *5*, 409-414.

Chapter 4.

Cross-plane Thermal Conductivity Measurement of Holey Silicon : Ballistic Phonon Transport

When the size of semiconductors is smaller than the phonon mean free path, the Fourier Law of heat conduction breaks down and phonons can carry the heat without losing energy. The ballistic phonon transport has received great attention for understanding heat conduction in nanomaterials and for managing heat dissipation in nanoelectronics.[1-7] Recent experiment showed the ballistic thermal conductivity in SiGe nanowires in the length scale of 1-8 μm.[7] However, the thermal conductivity demonstration in the length scale of 10-100 nm range, or below the phonon mean free path in silicon, is not available despite its direct relevance to nanoscale transistors. Here we show ballistic transport prevails in the cross-plane direction of holey silicon in the length scale of 40-200 nm. The thermal conductivity scales linearly with the length when the lateral dimension is as narrow as 20 nm. We assess the impact of long-wavelength phonons and predict a transition from ballistic to diffusive regime using scaling models. Our results provide pathways for engineering the thermal conductivity of thermoelectric materials and for manipulating long-wavelength phonons to realize information-processing phononic devices.

4.1 Introduction

Thermal conductivity reduction in silicon nanostructures has been one of the major themes of thermoelectrics research over the past decade.[8-22] VLS nanowires provided lateral spatial confinement below the phonon mean free path and reduced the thermal conductivity by an order of magnitude compared to bulk silicon.[8,10] The crystalline nanowires with induced surface roughness demonstrated the thermal conductivity approaching the amorphous limit.[9-16] While many versions of silicon nanowire thermal conductivity data sets exist, length dependent studies below the phonon mean free path are not available due to sample preparation and measurement challenges. The past thermal conductivity measurement for silicon nanowires of varying length from 3 μm to 50 μm did not show any appreciable dependence.[12] When the length scale in the direction of temperature gradient is shorter than the mean free path, phonons travel through the medium with no internal scattering, which is known as ballistic transport. In

such a case, the thermodynamic equilibrium does not exist, and the Fourier Law of heat conduction becomes invalid. Past work on ballistic phonon transport focused on the theoretical development of non-Fourier heat conduction and the reduced thermal conductivity in nanoscale geometry.[1,2] Goodson et al. provided evidence of ballistic phonon transport in silicon membranes and discussed its possible impact on hotspots in nanoscale transistors.[3,4] The ballistic phonon transport has also drawn attention for its potential application in phononic devices.[23-25] The phononic devices, analogous to electronic devices, aim to process information by manipulating heat flow.[24] This has not been possible partly due to inelastic scattering that destroys phonon wave characteristics. Only recently, several experiments demonstrated the presence of ballistic phonon transport through novel techniques using ultrafast X-ray beams,[5] transient thermal gratings[6], and homogeneously-alloyed nanowires.[7] Simple demonstration of ballistic transport requires the measurement of thermal conductivity that scales linearly with sample length. The challenge at room temperature is to find a material with ballistic phonons persisting in long sample length or to obtain required measurement sensitivity in short sample length. Chang *et al.* utilized alloy filtering of high-frequency phonons in SiGe nanowires and successfully measured the ballistic thermal conductivity in the range of 1-8 μm.[7] However, the ballistic thermal conductivity demonstration in the length scale of 10-100 nm range is not available. The submicron length scale is particularly important for silicon and the relevant for electronics and phononics applications because the effective mean free path of dominant phonons in bulk silicon is about 200-300 nm.[30-32] Here we utilize an inverse-nanowire system, i.e. holey silicon, to study ballistic phonon transport and characterize the cross-plane thermal conductivity in the length scale of 40-200 nm. Holey silicon nanostructures have demonstrated great potential for recovering waste heat energy.[17-22] Our cross-plane data is vital for general device applications where most temperature gradients occur across layers. We assess the transition from ballistic to diffusive transport using scaling models and discuss its implications for thermoelectric devices as well as electronics and potential phononics applications.

4.2 Experimental method

4.2.1 Holey silicon device fabrication for 3ω measurement
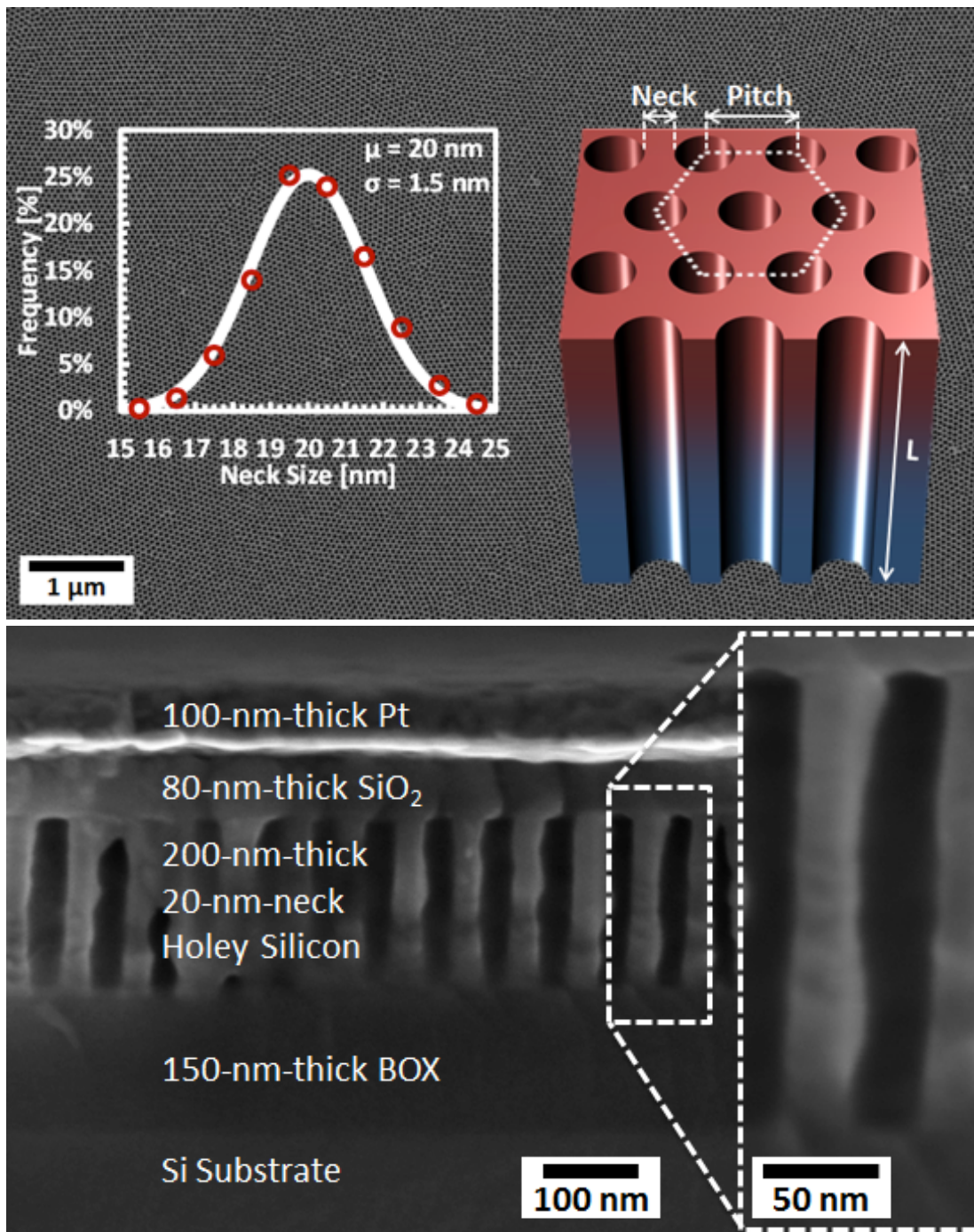
Figure 4.1 Top-view (a) and cross-sectional-view (b) SEM images of holey silicon devices, fabricated using block copolymer lithography. The PS-b-P2VP block copolymer, with controlled chemistry, provides uniform patterning of nanoholes over a large area (> 1 mm^2). After the pattern transfer on SOI substrates, the DRIE process creates silicon trenches of 20 ± 1.5 nm neck and 41 nm ± 1.9 nm hole diameter. Given the small aspect-ratio (< 5), the etch scallops are undetectable. The etched surfaces are further treated with post-annealing at 800 °C in Ar.

Figure 4.2 HRTEM images of HS shows completely etched hole (a) with a smooth boundary (b)
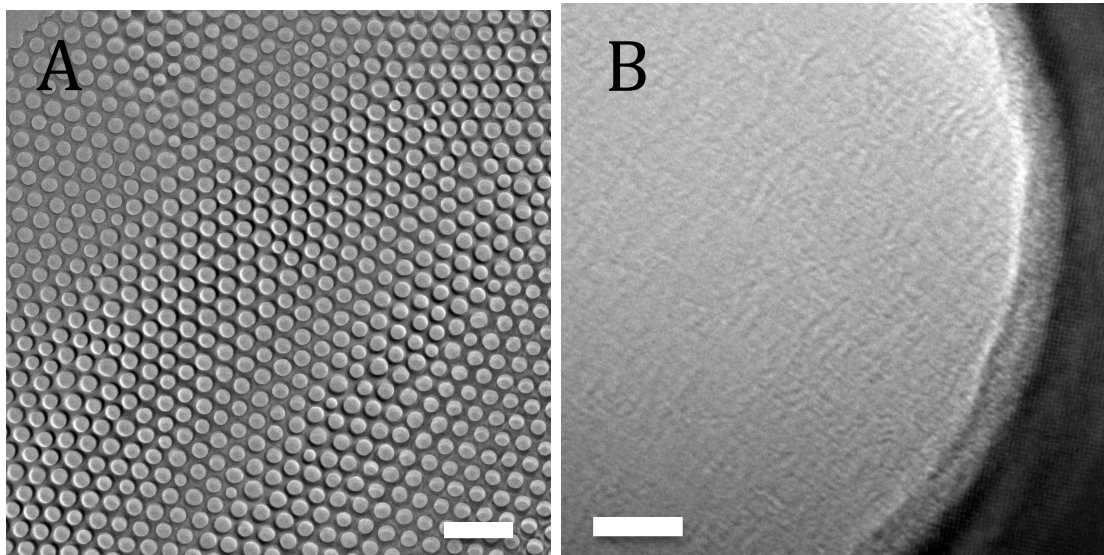
Holey silicon devices are fabricated on commercial Silicon-on-Insulator (SOI) substrates (SOITEC) with a 200-nm-thick silicon device layer and a 150-nm-thick buried oxide layer. The silicon layer is p-type with a negligible doping concentration ($\sim 10^{15}$ cm^{-3}) and the crystal orientation is in the (100) direction. In order to vary the silicon layer thickness, the silicon was consumed by thermal oxidation and subsequently removed by wet etching. The thermal oxide layers were grown at 1000 °C for varying duration to provide 150 nm, 100 nm, 70 nm, and 40 nm thick silicon layers on the same SOI substrates. The varying thickness samples are then treated with identical processes in the following.

For patterning nano-holes over a large area, we utilized the same block copolymer used in All-in-one ZT device in chapter 3. Briefly, PS-b-P2VP block copolymer with molecular weight of 183.5kg mol^{-1} was dissolved in toluene and stirred overnight. The polymer solution was spun cast on the SOI substrates. 300 ml toluene was used in a 200 ml jar as a solvent annealing method to induce lateral ordering of micro-domains. It was immersed in methanol for thirty minutes in order to reconstruct the P2VP part in the film and then blown by a nitrogen gun. Then chromium layer was deposited by e-beam evaporator at 60 degrees. The block copolymer layer under the chromium was removed by oxygen plasma generated at 50 W for 1 minute. Silicon trenches were then created by DRIE. The chromium was removed by immersing the samples in a chromium etchant solution (CR-7 from Cyantek) and also with oxygen plasma to ensure a clean surface. Even though any defects were not observed due to the etching process by Raman spectroscopy (chapter 3.7) and HRTEM (figure 4.2), the samples were post-annealed at 800 °C in argon for two hours to insure the defect free surfaces. Since the thermal conductivity measurement requires electrical isolation, we sputtered an 80-nm-thick silicon oxide layer over the holey silicon. The sputtered oxide also provides a smooth surface for subsequent processes. We confirmed with SEM that the sputtered oxide did

not penetrate through the silicon trenches. Four-probe fabricated platinum electrodes were then fabricated using standard photolithography followed by metal deposition using an evaporator and lift-off in acetone. Using the platinum as a mask, we removed the oxide and the holey silicon outside the electrode using anisotropic dry etching processes. The sputtered oxide and holey silicon layers were first removed by CHF_3/Ar (80 sccm/4 sccm) under 80 mtorr at 150W, and the remaining holey silicon or thin film silicon layers were removed by DRIE. Potential CFx polymer residues were removed by oxygen plasma.

4.2.2 Thermal conductivity measurement by 3ω technique

We characterize the cross-plane thermal conductivity of holey silicon using the 3ω method.[26,27] When the platinum electrode transmits current at frequency ω and generates Joule heating at 2ω, the resulting change in the electrical resistance creates a 3ω component in the voltage. A circuitry of differential amplifiers extracts the 3ω voltage and a lock-in amplifier (SR830) detects the in-phase signal with high sensitivity. (figure 4.3) The 3ω voltage captures the amplitude of temperature rise in response of underlying materials. We fit the data to a multilayer heat conduction solution that accounts for the thermal conductivity, the anisotropy ratio, the boundary resistance, and the heat capacity of each layer using recursive matrix formulation.[27] The solution is more sensitive to the holey silicon layer when the heater is narrower. However, the narrower heaters are also more susceptible to lateral heat spreading. We maximize the sensitivity by forcing the heat conduction in the cross-plane direction by removing the silicon and oxide layers that are outside the narrow heater. Differential measurements with control devices, that are identical to holey silicon devices except for the absence of holes and silicon layer respectively, minimize the uncertainty in unknown properties of surrounding materials. The sensitivity to holey silicon also increases when the porosity is higher because the effective thermal resistance is much greater than that of silicon films. For porosity 30% or higher, the uncertainty in differential analysis is 6% or lower. The thermal conductivity was calculated by normaling the porosity (φ): $\kappa_{HS}/\kappa_{measured} = 1/(1-\varphi)$.
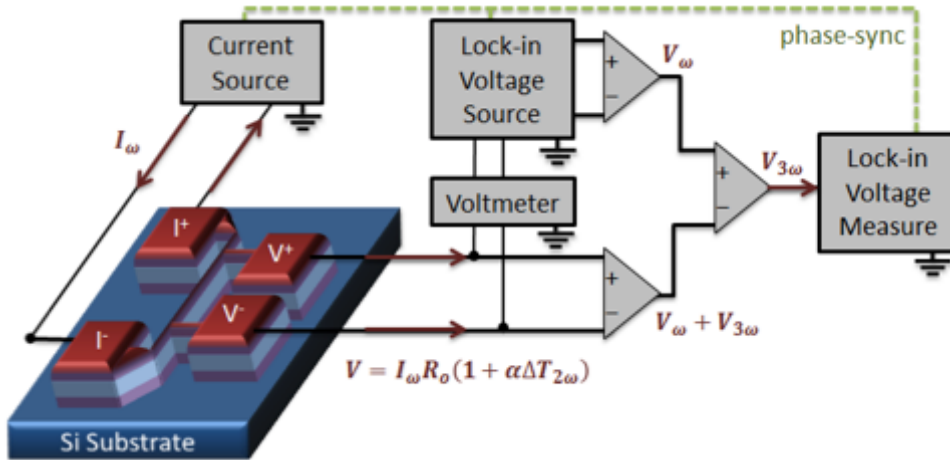

Figure 4.3 The schematic image of 3ω experiment setup. 3ω voltage ($V_{3\omega}$) captures the surface temperature rise in the platinum heater, which is a function of the thermal

properties of the underlying materials. The differential measurements of holey silicon devices and silicon thin film devices provide the thermal conductivity of holey silicon.

4.3 Results and discussion

Figure 4.4 shows the room-temperature thermal conductivity of 20-nm-neck holey silicon nanostructures. The thermal conductivity increases linearly from 1.5 ± 0.2 Wm^{-1}K^{-1} to 2.7 ± 0.4 Wm^{-1}K^{-1}, 3.9 ± 0.6 Wm^{-1}K^{-1}, and 8.0 ± 1.0 Wm^{-1}K^{-1} for varying length from 40 nm to 70 nm, 100 nm, and 200 nm respectively. The strong linear dependence indicates that ballistic transport dominates heat conduction in the cross-plane direction of holey silicon. The presence of ballistic phonons in the length scale of 40-200 nm may have been expected, but the fact that the lateral dimension is as narrow as 20 nm and smaller than the length is provocative. While classical models in phonon boundary scattering predict the smallest dimension, i.e. neck, limits the phonon mean free path, the data suggests otherwise.

In general, the Boltzmann Transport Equation (BTE) is a great resource to understand phonon transport in semiconductors. The thermal conductivity can be expressed in spherical coordinates as,

$$\kappa = \frac{1}{8\pi^2}\sum_n \int_0^{k_o} \int_0^{2\pi} \int_0^{\pi} C_{ph}\, v_g^2\, \tau\, k^2 \sin\theta\, d\theta d\phi dk \qquad (1)$$

where the heat capacity (C_{ph}), group velocity (v_g), total relaxation time (τ), are each dependent on the phonon frequency (ω) and the wave vector (k). The total relaxation time ($\tau^{-1} = \tau_U^{-1} + \tau_D^{-1} + \tau_{bl}^{-1} + \tau_{bv}^{-1}$) accounts for the Umklapp scattering (τ_U), point-defect scattering (τ_D), lateral boundary scattering (τ_{bl}) and vertical boundary scattering (τ_{bv}). The relaxation time due to the Umkapp scattering can be expressed as $\tau_U = AT\omega^2\exp(-B/T)$ where $A = 1.4\times10^{-19}$ s/K and $B = 152$ K are the fitting parameters that reproduce the bulk silicon thermal conductivity.[20] The relaxation time due to phonon-defect scattering can be expressed as $\tau_D = D\omega^4$. For nearly pure silicon, the parameter D mainly depends on the isotope concentration and has been determined as $D = 1.32$ x 10^{-45} s^3.[36] The relaxation time due to cross-plane boundary scattering is $L/(2\, v_{ph} \cos\theta)$ where $v_{ph} = \partial\omega/\partial k$. In the worst-case scenario, phonons scatter completely diffusely at the lateral boundaries defined by the neck, as if they are passing through nanowires of the diameter equivalent to the neck size. The nanowire analogy provides the lower bound thermal conductivity. However, the thermal conductivity of holey silicon is even lower than the calculations for 20-nm-wide nanowires, and shows more pronounced length dependence.
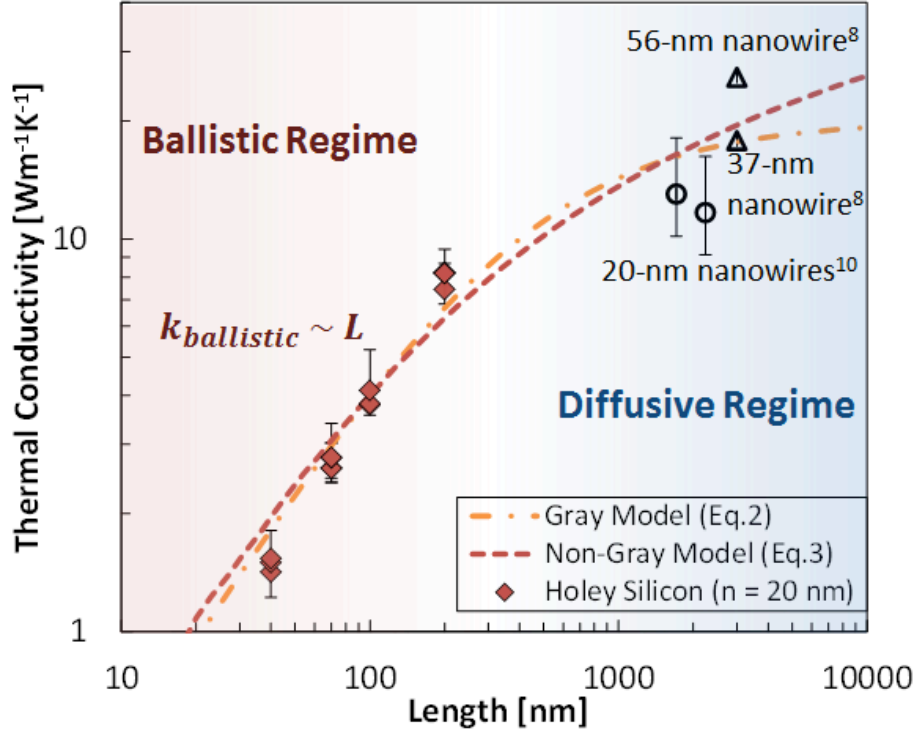
Figure 4.4 Room-temperature thermal conductivity of 20-nm-neck holey silicon of varying length from 40 nm to 200 nm. The strong length dependence indicates dominant presence of ballistic phonon transport. A simple scaling model (Eq. 2) using the average mean free path of bulk silicon ($\lambda = 200$ nm) predicts the thermal conductivity may approach 20 $Wm^{-1}K^{-1}$ in the infinitely-long limit. This coincides with the reported data for a nanowire [8], which has the equivalent cross-sectional area. A non-gray model (Eq. 3) accounting for long-wavelength phonons predicts higher thermal conductivity. The reported values are material thermal conductivity that is numerically independent of the boundary resistance and the porosity.

The length dependent thermal conductivity in silicon nanostructures, while not observed in any experiment, has been investigated by many theoretical studies.[39-46] One popular approach is using a gray model, which has been reported to reproduce the values from the Green-Kubo calculations and used to study the length dependent thermal conductivity in silicon nanowires.[39,43,46] The thermal conductivity scaling in gray model can be expressed as,

$$k_{gray} = k_{\infty} \left(1 + \frac{\lambda_{\infty}}{L/2}\right)^{-1} \qquad (2)$$

where k_{∞} and λ_{∞} are the thermal conductivity and phonon mean free path of an infinitely-long system. This requires information about the average mean free path as a fitting parameter. The average mean free path estimation based on the kinetic theory ($\lambda = 3k/Cv$)

is about 40 nm for bulk silicon, but this method grossly underestimates heat conduction at room temperature. Not all phonons contribute equally to heat conduction because the most phonon population is near the zone boundary and optical phonons have substantially small group velocity compared to acoustic phonons. The average mean free path accounting for the spectral dependence ($\lambda_{zn} = 3k/\int Cvd\omega$) is about 200 nm.[1,32,49] The average mean free path that best matches the data for silicon thin films and VLS silicon nanowires is also reported as 200~300 nm.[30,31] By using the average mean free path 200 nm and the gray model (eq. 2), the thermal conductivity in the infinity converges to 20 $Wm^{-1}K^{-1}$, which closely matches the reported data for the 37-nm-wide VLS nanowire.[8] This implies that the phonon transport in the inverse nanowire holey silicon system resembles that in nanowires of the equivalent cross-sectional area.

While the gray scaling model (Eq. 2) captures the holey silicon data with the use of average mean free path, a number of recent studies emphasize the use of non-gray modeling and accounting for the broad spectrum of phonons in silicon.[6, 42, 47-49] For bulk silicon at room temperature, phonons with the mean free path greater than 1 μm contributes about 50% of heat conduction (Figure 4.5). The median mean free path is several factors larger than the average mean free path, and this provides a more complete picture in analyzing the thermal conductivity size effect.[47-49] A non-gray scaling model accounting for the frequency dependence of the phonon mean free path can be express as,

$$k = \int_{y}^{\omega_0} k_\infty(\omega)\left(1 + \frac{\lambda_\infty(\omega)}{L/2}\right)^{-1} d\omega \qquad (3)$$
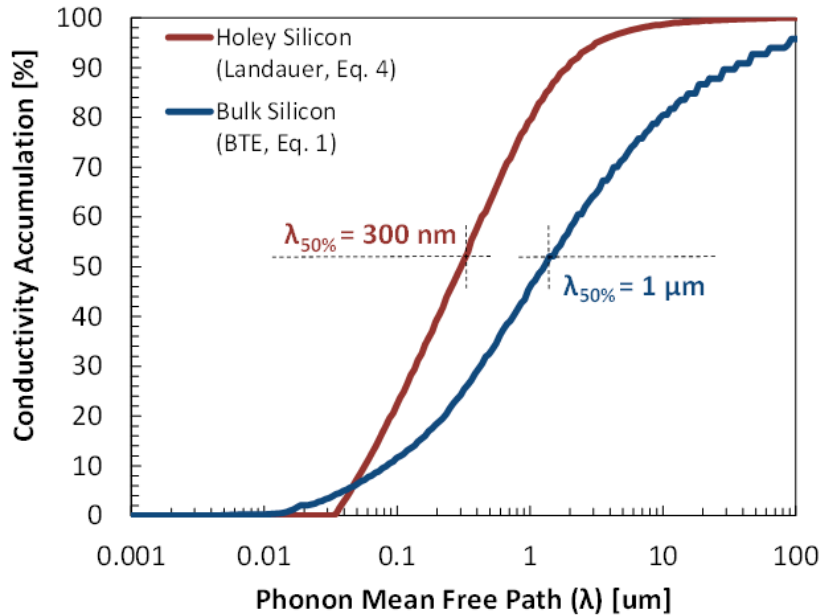
Figure 4.5 Phonon mean path contributions to the thermal conductivity in bulk silicon and in the 20-nm-neck holey silicon. The BTE calculations (Eq. 1) accounting for full dispersion in bulk silicon predicts the median mean free path ($\lambda_{50\%}$) is about 1 μm. This implies that ballistic phonon transport dominates the thermal conductivity in our holey silicon of the length scale 40-200 nm. The Landauer Formalism estimates the mean free

path in holey silicon by assuming the 20-nm-neck holey silicon has the equivalent cross-sectional area with a 40-nm-wide nanowire. This accounts for specular scattering by long wavelength phonons and predicts the median mean free path is about 300 nm. This is consistent with the strong size effect observed in the holey silicon thermal conductivity data (Fig. 4.4).

This requires functional forms of the thermal conductivity and the mean free path in the infinitely-long system. As mentioned earlier, the classical modeling based on the BTE (Eq. 1) cannot explain the length dependence in holey silicon because the mean free path is limited by the neck size. We find the mean free path in holey silicon can be greater than the neck size in the framework of Landauer Formalism, developed by Moore et al and Chen et al,[10, 33]

$$G_r = \frac{k_B}{2\pi} \int_0^{\omega_D} \left(\frac{N_1}{1+L/l} + \frac{N_2}{1+L/d} \right) \frac{x^2 \exp(x)}{(\exp(x)-1)^2} \, d\omega \qquad (4)$$
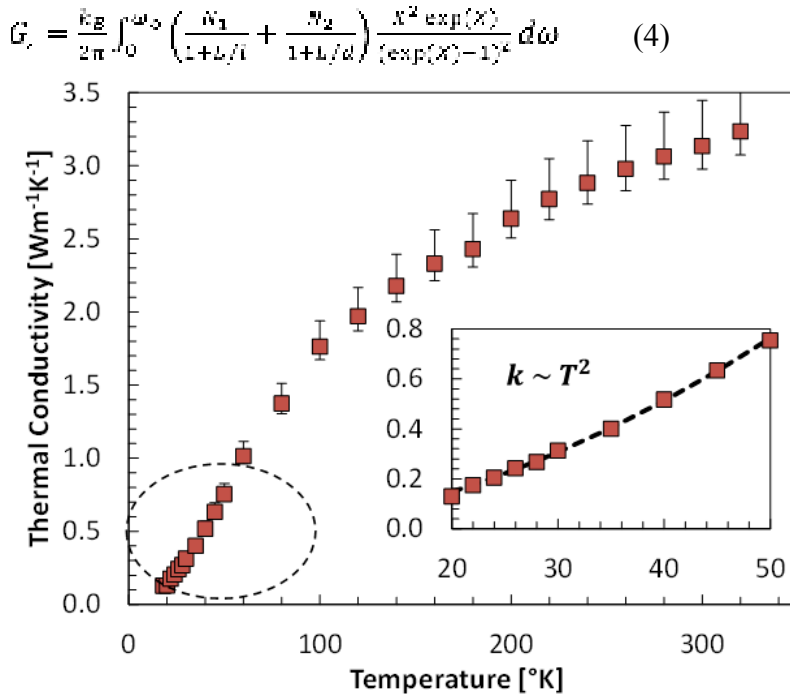

Figure 4.6 Temperature dependent thermal conductivity of 20-nm-neck and 70-nm-long holey silicon from 20 K to 320 K. The thermal conductivity data at 20-50 K deviate from the classical law governed by the heat capacity (k~T³). Landauer Formalism accounting for the frequency dependent boundary scattering explains the non-classical dependence and also predicts increased contribution of specular phonons in narrow silicon nanostructures. The thermal conductivity increases with the power of 2 at low temperature and then begins to slow down near the room temperature. The absence of negative slope indicates the Umklapp scattering is never a dominant factor throughout the temperature range presented here.

where L is the length, A is the cross-sectional area, d is the diameter, l is the frequency dependent mean free path, N_1 is the number of modes with the mean free path l, and N_2 is the number of modes with the mean free path limited to d, and $X = \hbar\omega/k_B T$. They found the contribution of specular phonons, which has the mean free path scaling by ω^{-4}, increases

in nanowires with smaller diameter.[10, 33] This frequency dependence resembles Rayleigh scattering, and the model treats surface disorder as a collection of point-like impurities. Although the original model was developed in the ballistic limit, here we have included Umklapp scattering and applied the cut-off frequency suggested by Mingo to obtain the effective mean free path contributions (Figure 4.5).[36] Combining the Landauer model (Eq. 4) and the non-gray scaling model (Eq. 3), we can explain the scaling trend (Figure. 4.3) without using the thermal conductivity or the mean free path as a fitting parameter. The non-gray scaling model predicts the thermal conductivity in the infinity approaches a higher value than the prediction based on the gray model. This is because the Landauer model accounts for long-wavelength phonons that are specular scattering with lateral boundaries. The transition from ballistic to diffusive transport also occurs at a longer length scale (~300 nm). This implies that the long-wavelength phonons are responsible for the mean free path greater than the neck size and the strong size effect observed in holey silicon. We can also infer that short wavelength phonons are effectively filtered by the surface disorder and the ballistic phonon transport is predominantly due to long-wavelength phonons.

The long-wavelength phonons also play an important role in analyzing the temperature dependent data. Figure 4.6 shows the temperature dependent thermal conductivity of holey silicon down to 20 K. At cryogenic temperatures, or when the dominant phonon wavelength is greater than the size of impurities, the thermal conductivity should scale by the power of 3 ($k \sim T^3$), based on the classical law for heat capacity. However, the holey silicon thermal conductivity data in the range of 20-50 K show the temperature dependence scaling by the power of 2 ($k \sim T^2$). This non-classical observation is not new for silicon nanowires. Li *et al*. and Chen *et al*. showed VLS nanowires of diameter in the range 20-40 nm exhibit unusual temperature dependence ($k \sim T^{1 \sim 2}$) at low temperatures (20~60K).[8,10] One perspective is to consider quantum confinement effect, which changes phonon dispersion relation in the order of 10 nm.[34-37] However, several studies argue the confinement effect is only relevant for temperatures below 10 K because roughness destroys coherence for short-wavelength phonons.[32,38] Another perspective is to consider increased contribution of surface disorder and account for frequency boundary scattering which is consistent with our explanation for the ballistic transport at room temperature. Moore et al. explains that the combined contributions of specular and diffusive transport depending on the phonon frequency with respect to the length scale of surface disorder can result in thermal conductance that is approximately linear in temperature up to about one-fifth of the Debye temperature. [33]

4.3.1 Implication for thermoelectrics, electronics, and phononics

The thermal conductivity data and the scaling models presented here have direct implications for thermoelectric applications. Holey silicon nanostructures are potentially great thermoelectric materials.[17-22] Tang et al. demonstrated the block copolymer based holey silicon can have the thermoelectric figure of merit (*ZT*) up to 0.4 in-plane direction at room temperature.[18] The cross-plane data is directly applicable for planar devices where temperature gradients occur across layers. Holey silicon nanostructures are also

more attractive in such integrated systems compared to nanowire arrays because of mechanically and electrically better contact quality. One of major technological challenges for holey silicon thermoelectric devices would be scaling up to higher-aspect-ratio structures while keeping the thermal conductivity low. The scaling models developed here predict the thermal conductivity to reach a plateau when the length is sufficiently larger than the phonon mean free path. Past studies on the roughness suggest the phonon mean free path in silicon can be strongly suppressed by various methods of surface treatment.[9-16] In such roughness-induced holey silicon, the transition from ballistic to diffusive transport may happen in a shorter length scale, which would be more favorable for thermoelectric applications. The results here also suggest that keeping the neck size small is important. Ongoing development of etching process can shed light on fabricating higher-aspect-ratio holey silicon nanostructures, which may become a commercially viable thermoelectric material particularly at high temperatures.

The silicon thermal conductivity data in the length scale of 40-200 nm has immediate implications for nanoscale electronic systems. With the rapid scaling trend in transistors, heat generation in reduced geometry is of ever-increasing importance for both device performance and reliability. We expect the thermal conductivity of silicon to scale linearly down with the reduced dimension in transistors. The ballistic phonon transport would be responsible for hotspots in nanoscale systems and the heat generation would be beyond the predictions based on classical size effect models.

Although the impact is not as immediate as on electronic applications, the strong ballistic transport at room temperature we observed in holey silicon is very promising for phononic applications. Our work suggests that thermal diodes or potential phononic waveguides can benefit from the persistent long-wavelength phonons in silicon nanostructures even when the limiting dimension is down to 20 nm and the fabrication involves conventional etching processes. The fact that surface disorder filters high-frequency phonons and increases the contribution of low-frequency phonons is analogous to the alloy scattering scheme in SiGe nanowires and SiGe phononic crystals.[25, 50] We expect that the scaling trend of transistors would be more favorable for potential integration of nanoelectronics and phononics because the mean free path of long-wavelength phonons exceeds typical dimensions of commercial transistors, leading to ballistic phonon transport. The fact that silicon has excellent electrical and thermal properties is a great advantage for the development of phononic devices. Holey silicon nanostructures, presented here, show great potential to become a building block of future phononics.

4.4 Conclusion

The fundamentals of heat transfer governed by Fourier Law break down at nanoscale, specifically when the length scale is smaller than the carrier mean free path. This work provides a self-consistent data set of holey silicon in the length scale below the phonon mean free path in silicon. Ballistic phonon transport dominates heat conduction across the holey silicon. The scaling models predict the transition from ballistic to diffusive transport to occur at the length scale much greater than the physically limiting dimension because of long wave-length phonons. The frequency dependent boundary

scattering, accounting for specular scattering with surface disorder, is responsible for the strong size effect and the non-classical low temperature dependence. These results are particularly important for managing heat generation in silicon transistors that are scaling much below the phonon mean free path. The holey silicon is providing pathways for engineering the thermal conductivity in silicon nanostructures, which can lead to cost-effective thermoelectric devices and could potentially be a breakthrough for phononic devices.

4.5 Reference

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4.6 Appendix C
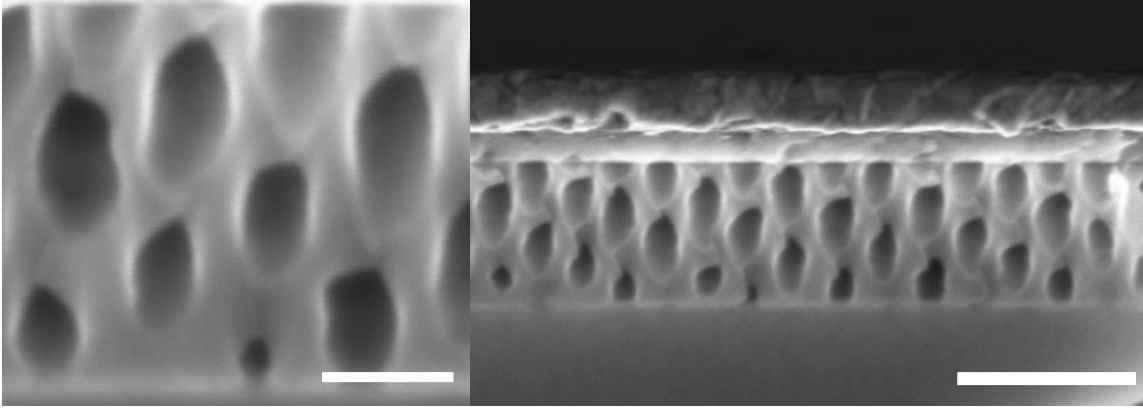
SEM Images of HS Device

Figure 4.C1 SEM images of the diagonally cut HS device. Side view SEM images demonstrating smooth boundaries of HS after DIRE. The SEM images do not show any scallops or rough boundaries in HS, and we assume that it does not have any appreciable roughness that is relevant for long-wavelength phonons. Scale bar : 50 nm (left) and 200nm (right)

4.7 Appendix D

BTE Modeling (Classical Diffusive and Ballistic Regimes)

In this work, we use a polynomial phonon dispersion,[1] for silicon, which is very close to its real dispersion relation. We consider phonon dispersion in silicon along the(100) direction considers LA, TA, LO, TO modes separately. Each phonon dispersion branch is treated with the isotropic approximation. We can solve the BTE under the relaxation time approximation and use the Matthiessence's Rule to capture various scattering events.

For the cross-plane thermal conductivity, angle dependence has been taken into account,

$$K = \frac{1}{8\pi^2}\sum_n \int_0^{k_0} \int_0^{2\pi} \int_0^{\pi} C_{ph}\, v_g^2\, \tau\, k^2 \sin\theta\, d\theta d\phi dk$$

where the heat capacity (C_{ph}), group velocity (v_g), relaxation time (τ), are each dependent on the phonon dispersion relations (ω, k).

$\tau^{-1} = \tau_U^{-1} + \tau_D^{-1} + \tau_{bl}^{-1} + \tau_{bv}^{-1}$. In the worst-case scenario, phonons scatter diffusely at the boundaries defined by the neck size, as if they are passing through nanowires of the

diameter equivalent to the neck size. The nanowire analogy provides the lower bound thermal conductivity, and the lateral phonon boundary scattering term becomes $\tau_{bl} = (4/3\pi)\, n/(v_{ph}\sin\theta)$. The vertical phonon boundary scattering term, bounded by the length is $\tau_{bl} = L/(v_{ph}\cos\theta)$.

The relaxation time due to phonon-defect interaction is written as $\tau_D = D\omega^4$. For nearly pure silicon, the parameter D mainly depends on the isotope concentration. Assuming that this concentration is constant, D should be a constant and has already been determined ($D = 1.32 \times 10^{-45}$ s^3).[2]
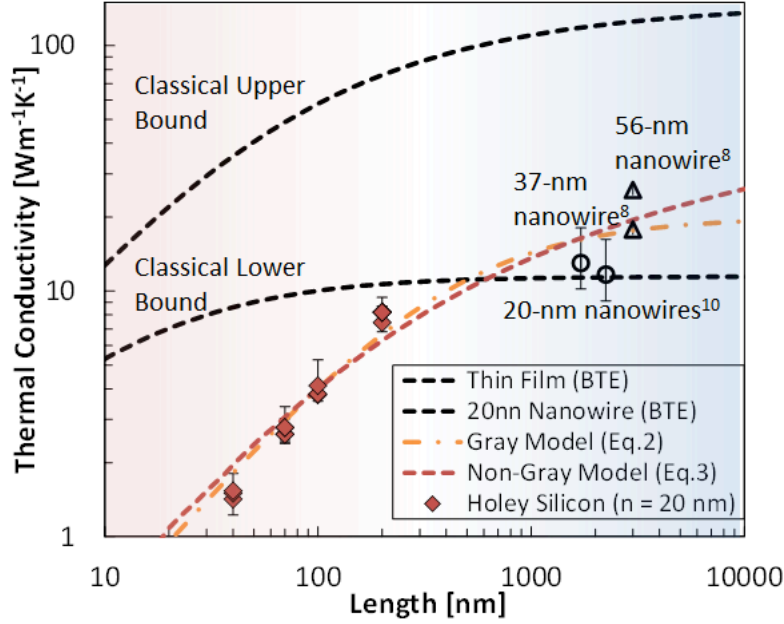

Figure 4.D1 Room-temperature thermal conductivity of 20-nm-neck holey silicon of varying length from 200 nm to 40 nm. The classical upper bound is the cross-plane thermal conductivity in thin films. The classical lower bound is the thermal conductivity in 20-nm-wide nanowires. The thermal conductivity of holey silicon demonstrates stronger size effect than the classical predictions.

4.8 References

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