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200 mm Sensor Development Using Bonded Wafers

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ABSTRACT: Sensors fabricated from high resistivity, float zone, silicon material have been the basis of vertex detectors and trackers for the last 30 years. The areas of these devices have increased from a few square cm to 200 m² for the existing CMS tracker. High Luminosity Large Hadron Collider (HL-LHC), CMS and ATLAS tracker upgrades will each require more than 200 m² of silicon and the CMS High Granularity Calorimeter (HGCAL) will require more than 600 m². The cost and complexity of assembly of these devices is related to the area of each module, which in turn is set by the size of the silicon sensors. In addition to large area, the devices must be radiation hard, which requires the use of sensors thinned to 200 microns or less. The combination of wafer thinning and large wafer diameter is a significant technical challenge, and is the subject of this work. We describe work on development of thin sensors on 200mm wafers using wafer bonding technology. Results of development runs with float zone, Silicon-on-Insulator and Silicon-Silicon bonded wafer technologies are reported.

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1 Introduction

Particle Physics collider experiments are increasingly dependent on silicon diode detectors for tracking, vertexing, and calorimetry. These detectors can provide precise position and energy information and are sufficiently radiation hard for the challenging environment of the High Luminosity LHC. ATLAS[2] and CMS[6] trackers at HL-LHC plan silicon tracking systems of $\approx 200m^2$ each. The CMS high granularity calorimeter[5] plans a detector of $600m^2$ area tiled with planes of sensors diced from 8" wafers. In addition silicon-based sensors are increasingly utilized for x-ray imaging and other applications that will require large areas of sensors. Modern technologies such as 3-D integration often can only be affordably implemented on larger wafers. These needs motivate the development of technologies to move sensor wafer fabrication from 6" to 8" wafers [4].

Sensors for high energy physics must have thin (100-300 micron) active regions for radiation resistance and low mass. Typical 200 mm wafer processing equipment requires thicker (775 micron) material for automated handling and to limit breakage. These thick wafers must be thinned after topside processing to the 100-300 microns needed for HEP detectors. Good sensor performance with low leakage current requires a high quality backside contact. This requires a p+ or n+ implant and associated annealing, metalization, and sintering. The standard high temperature annealing process precludes the presence of topside metalization before the anneal. There are several possible process solutions to this:

- The topside can be completely patterned and oven-annealed, topside metalization deposited. The wafer is then thinned, implanted and annealed using a laser that locally melts the backside implanted region[11].
- The wafer can be implanted on front side, thinned, implanted on the back side, annealed, and metal deposited and patterned on the front side. This involves handling and patterning a thin wafer during the final steps.
- Use of alternative low temperature annealing processes such as microwave annealing[8][7].
- The sensor (float zone) wafer backside can be implanted, polished, then Silicon-on-Insulator (SOI) bonded to a handle wafer for processing. The top (device) wafer is then thinned to the required thickness and polished. After the topside process is complete the backside handle and oxide are removed and an aluminum backside contact electrode is deposited.
- The sensor wafer can be Silicon-Silicon (SiSi) bonded to a low resistivity handle wafer of the same type. The topside can be thinned to the appropriate thickness, polished and fully processed. The resulting stack can then be thinned to the required physical thickness. No backside processing other than metalization is necessary.

We have chosen to explore the last two technologies as part of a US Small Business Innovative Research (SBIR)-funded development project aimed at production of large area, thinned, radiation hard silicon detector systems. The initial runs used the Novati foundry in Austin, Texas and the final run used the NHanced foundry in Morrisville, North Carolina.

2 Detector Requirements

This development was guided by the need for radiation hard detectors for Particle Physics. Designs are driven by radiation induced effects, including the increase of acceptor levels, which require an increase in operating voltage, and the increase in leakage current[12]. These effects can be mitigated by making the detectors thin and operating them at low temperature. The detectors planned for HL-LHC trackers are based on n-on-p diodes, thinned to a volume compatible with acceptable signal to noise after irradiation [14]. At the end-of-life the devices also must withstand bias voltages up to 1000 volts. The CMS HGCAL application required only DC-coupled pad sensors. Tracker sensors incorporate AC coupling capacitors and polysilicon bias resistors on the microstrip sensors.

Run	Substrate	Active/Physical Thickness (μm)	Process	Splits	Date
1	FZ	725,500/725,500	DC	p-stop, oxide	4/2015
2	SOI, FZ	200,500/700,500	DC	p-stop, oxide	3/2016
3	SOI	275/275	AC	p-stop,n+	11/2017
4	SiSi	200/700	DC	p-stop	3/2019

Table 1. Summary of process runs, substrates used and process splits. Oxide splits used either wet or dry oxydation. P-stop splits varied the p-stop doping

3 Process Development

The fabrication process is based on processes developed at SLAC and LBNL[10]. These processes were adapted for the foundry process at NHanced. The process steps, including implantation and annealing were modeled using Silvaco tools[13] at Fermilab. In total there were four runs, summarized in Table 1. The first run used bulk float zone wafers to establish the overall process. Runs 2 and 3 used SOI stacked wafers and the last used SiSi wafer stacks. Initial development runs were DC-coupled diodes processed using full thickness wafers. For the float zone wafers the minimum final thickness was 500 microns due to the fragility of thinner wafers. The initial runs were used to understand leakage current and breakdown characteristics, explore guard ring variants, and explore process splits such as p-stop dose and wet or dry oxidation. These also helped to inform the development of design rules for subsequent fabrications. The third run added AC coupling and polysilicon resistors.

The overall process flow for DC and AC coupled variants is given in table 2. An initial sacrificial oxide is grown to getter out impurities. Combined p-spray and p-stop isolation was used in the first run, and p-stops in the other runs. Another sacrificial oxide layer is used to provide the mask for all of the topside implants, providing good relative registration. The specific p, p+, or n implants are then defined by photoresist. The AC process includes steps to define the polysilicon resistors and coupling capacitors. The relative alignment of the mask layers is better than 3 microns. Figure 1 shows the result of a process simulation of the full AC/polysilicon process.

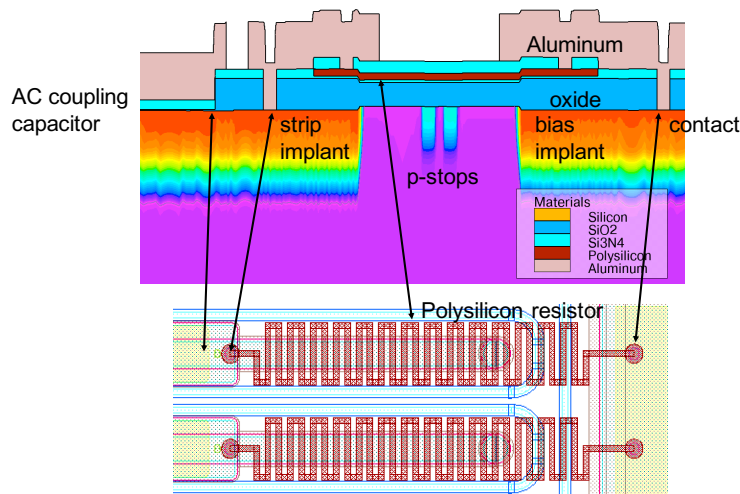


Figure 1. Results of a simulation of the full AC wafer fabrication process with the corresponding structures on a typical silicon strip detector.

The SOI runs were fabricated with a 200 or 250 micron thick float zone device layer bonded to a 500 micron thick handle layer with ≈ 1 micron of oxide separating the two layers. A thick float zone wafer is backside implanted and then bonded to the handle. The wafer stack is annealed at 1200 deg. C. This anneal is also used to getter the sensor. After bonding the top wafer is polished down to the final active thickness. The wafer stack front side is then processed normally. Run 2 used a DC-coupled process and wafers were delivered with the handle attached. These parts were

Process steps	DC	AC	Comments
Initial SOI, SiSi wafer preparation	•	•	Implant (SOI), bond to handle
Grow/Remove gettering oxide	•	•	Getter impurities
Blanket p-spray implant	•		Not used for runs 3,4
Grow masking oxide	•	•	
Pattern n and p implants in SiO_2	•	•	Oxide openings define n+ and p
Pattern and implant top	•	•	n+, p-stop, p-edge
anneal	•	•	Remove implant oxide
Grow final oxide	•	•	
Dep/pattern/etch polysilicon		•	
Pattern/etch Capacitor Oxide		•	Remove oxide for AC coupling
Dep/pattern/etch capacitor		•	$SiO_2 - SiN - SiO_2$ dielectric
Pattern/etch contacts		•	Bias and resistor contacts
Dep/pattern/etch aluminum	•	•	Top metal
Dep/pattern/etch passivation	•	•	Top SiO_2
Bond to top handle		•	Thinned SOI process
Remove back handle, etch BOX		•	Thinned SOI process
Deposit backside Al, remove handle		•	Thinned SOI process

Table 2. Summary of process flows for DC and AC runs

biased from the topside contacts. Topside contacts are acceptable for applications with moderate radiation requirements. At high radiation exposures the resistivity of the topside contact increases and may make topside bias connections problematic[3]. In run 3 a topside handle was attached, the backside handle wafer was removed, and the SOI buried oxide (BOX) was etched away. The backside was then metalized. In both cases standard float zone wafers were processed in parallel as control samples.

The last run used a Silicon-Silicon (SiSi) bonded substrate. This consists of a high resistivity wafer directly bonded to a low resistivity handle such that the interface is transparent to charge carriers. This construction has the advantage that the ohmic backside contact is built-in as part of the bonded wafer interface. It eliminates the pre-bonding backside implant step and the post process backside handle removal and BOX etch steps needed for the SOI devices. The wafer simply needs to be ground down to the desired physical thickness and aluminized. Silicon-Silicon bonding is, however, a less well-established and controlled process.

Full investigation of the SiSi process was interrupted by the sale of the Novati foundry where Runs 1-3 were fabricated. This required re-qualification of the process at the NHanced foundry in North Carolina. The initial NHanced run (Run 4) had poor oxide quality and large leakage currents. Therefore we were not able to fully qualify the SiSi process within the constraints of the R&D program.

4 Sensor and Test Structure Designs

A 200 mm wafer provides ample space for both test structures and prototype designs. For Runs 2 and 3 we included a variety of designs from the High Energy Physics (HEP) and Basic Energy Sciences (BES) communities. These included strip and pixel detectors for HEP and pixel sensors for x-ray imaging. We also included a variety of test structures including pad diodes with guard ring variants, MOS test structures, and resistor and capacitor structures in the AC run. Figure 2 shows the overall layout of the wafers. Full size ($\approx 5 \times 10\text{cm}$) strip and macro-pixel sensors intended as prototypes for the CMS inner tracker pixel-strip (PS) module were included in runs 2 and 3. Run 4 was dedicated to a prototype full-wafer CMS High Granularity Calorimeter design.

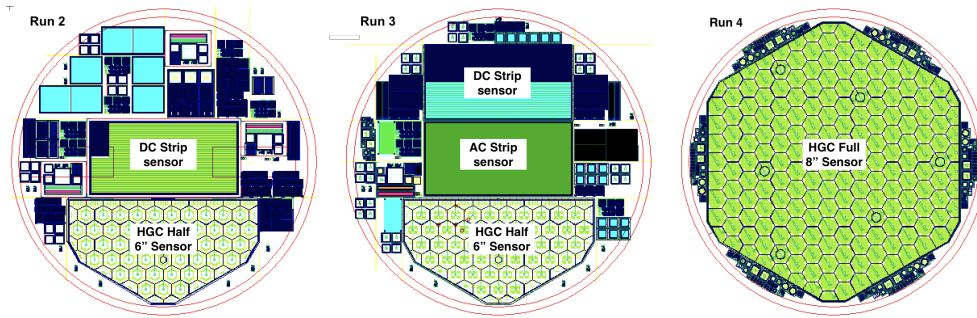


Figure 2. Layouts for the three bonded wafer submissions.

5 Characterization Results

5.1 Depletion Voltage and Leakage Currents

Here we consider only the devices from Runs 2-4, which incorporated wafer bonding technologies. The primary characterization tools were test structure diodes of $\approx 1\text{cm}^2$. Samples of these diodes were VI and CV tested for several wafers in each run. Test structure diodes were IV tested to 600 or 800 V. Test structures with currents exceeding $10\mu\text{A}$ were considered to be in breakdown. We found substantial variations in breakdown voltage within a wafer, especially in Run 2. This made it difficult to establish statistically significant optimum values for the various process splits.

5.1.1 Run 2 Wafers

Run 2 consisted of SOI wafers with the backside handle wafer intact. The sensors on these wafers had to be biased from the topside contact since the backside implant is not accessible. Diode CV tests showed a full depletion voltage of 60 ± 10 Volts (figure 3). The measured active thickness is 200 microns. The calculated effective doping concentration is $2.0 \pm 0.3 \times 10^{12}/\text{cm}^3$.

The leakage current at full depletion ranged from 0.5 to $0.75\mu\text{A}/\text{cm}^3$. The range of breakdown voltage varied considerably from diode to diode within a wafer (figure 4). The devices processed with dry oxidation and p-stop implant dose of 5×10^{11} had the best overall performance. In addition, some devices were observed to have hysteresis in the breakdown voltage, with the breakdown usually decreasing in subsequent iterations of the test. Devices with the single guard ring design generally had higher breakdown voltages by ≈ 100 Volts with respect to the multi-guard designs tested.

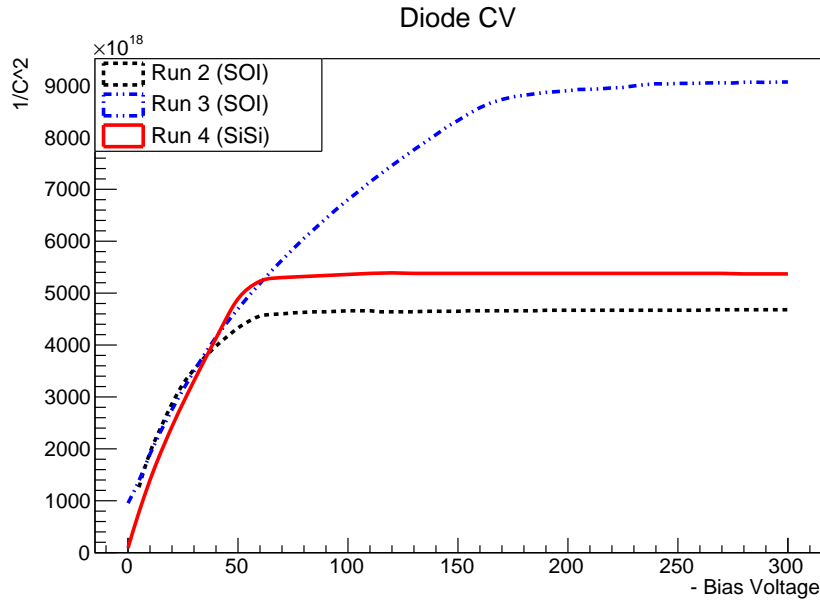


Figure 3. $1/C^2$ vs V_{bias} of Run 2, 3 and 4 test diodes. These are typical of diodes in each run.

5.1.2 Run 3 Wafers

Run 3 wafers were physically thinned and measured to have an active thickness of $250\mu m$. These depleted at 170 ± 15 Volts, giving an effective doping concentration of $3.2 \pm 0.28 \times 10^{12}/cm^3$. The average leakage current at full depletion ranged from 0.18 to $0.3 \mu A/cm^3$, considerably better than the Run 2 structures. In general the breakdown voltage for these devices was higher and more uniform than the Run 2 sensors (figure 4) and did not show hysteresis. We did not see a clear systematic difference between the various n-implant and p-stop process splits.

5.1.3 Run 4 Wafers

Run 4 wafers were fabricated as a stack of low and high resistivity silicon. The high resistivity active region was measured to be 200 microns thick. Depletion voltage for these sensors was 60 ± 10 Volts (figure 3). The calculated doping concentration for the float zone layer is $2.0 \pm 0.3 \times 10^{12}/cm^3$. The leakage current is shown in figure 4c. It is around $10\mu A/cm^2$ at 20V above depletion, roughly a factor of 10 higher than the SOI devices. The test diodes also show a rapid increase in current at 100-150 V, increasing to 0.1 mA at 500 V. The increase does not have the extremely sharp rise characteristic of avalanche breakdown. This may be due to fields penetrating into the low resistivity wafer and the bond interface, drawing current from defects in these regions. A pre-bonding p+ implant in the float zone wafer could reduce this issue, but would also make the process more complex.

5.2 Surface and Interstrip/Pad Characteristics

Metal Oxide Semiconductor (MOS) test structure CV measurements are shown in figure 5. These measurements provide indications of the overall surface quality, including oxide and interface charges. The first three runs show distinct patterns. The first and third run show abrupt transitions

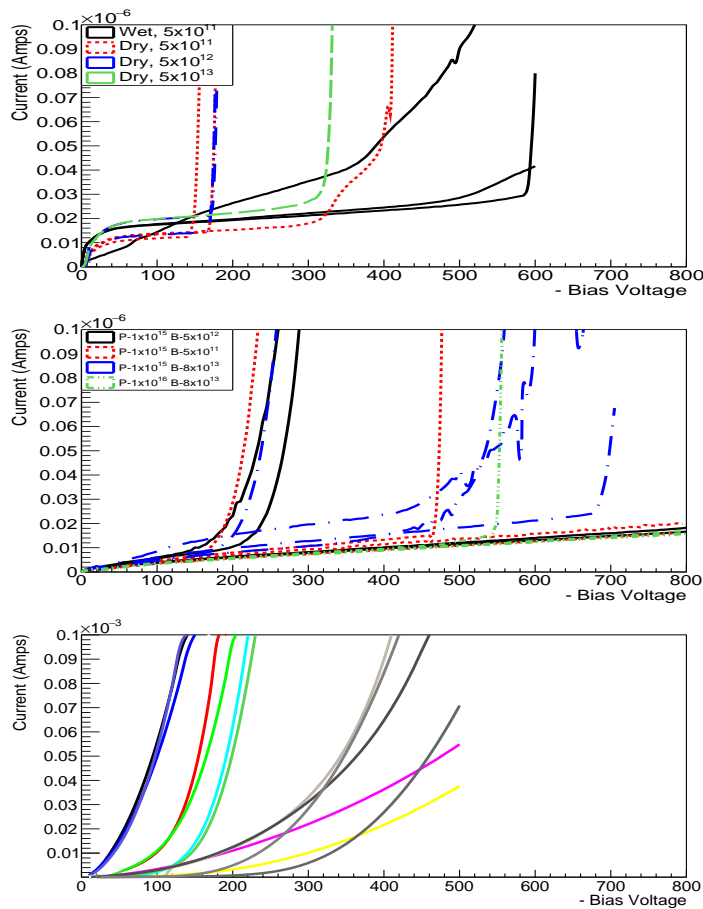


Figure 4. One cm^2 test diode current vs voltage characteristics for diodes with a single guard ring for wafers from Runs 2 (SOI, top), 3 (SOI, middle) and 4 (SiSi, bottom). Note the compressed scale on the SiSi VI plot.

between depletion and accumulation regions, indicating good interface quality. The small slope in the Run 2 CV curve is indicative of problems in the bulk-oxide interface. Run 1 had a large 6 Volt flatband voltage, indicating significant oxide charge density. This was improved for Run 3, with a 2.7 Volt flatband voltage corresponding to an oxide charge density of $1.2 \times 10^{11}/\text{cm}^2$. The MOS structures for the wafers in Run 4 did not show a clear distinction between the accumulation and depletion regions in the MOS test structures. Therefore the oxide charge could not be determined. This is true for both the Si-Si devices and float-zone controls. This is an indication of a poor silicon bulk to oxide surface interface.

5.3 AC Coupling Measurements

Run 3 included polysilicon bias resistors and AC coupling capacitors. The polysilicon structures were implanted with a nominal phosphorous dose of $1 \times 10^{15}/\text{cm}^2$. The resistance of the polysilicon resistors ranged from 750 to 1000 Ohms per square. Serpentine resistors on the CMS PS-s sensors measured $207 \pm 4 \times 10^3 \Omega$, at the low end of the acceptable range for sensors of this type. AC coupling capacitors were designed with both oxide and nitride layers. For these devices the relevant quantity is capacitance per unit length. These capacitors were measured to have a capacitance of

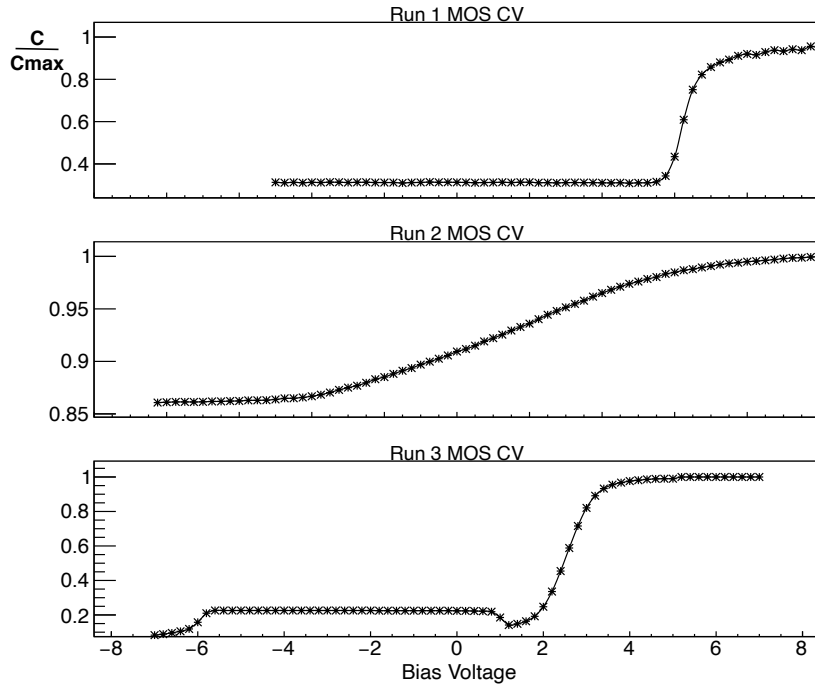


Figure 5. MOS CV curves for Run 1,2 and 3 test structures. Capacitance values are scaled to the maximum value for each structure. Note the small range for the Run 2 structure. Run 4 structures did not yield a meaningful CV curve.

80.9 ± 0.2 pF/cm. This is higher than the usual value of ≈ 20 pF/cm, indicating a thin oxide/nitride dielectric.

5.4 Irradiation Results

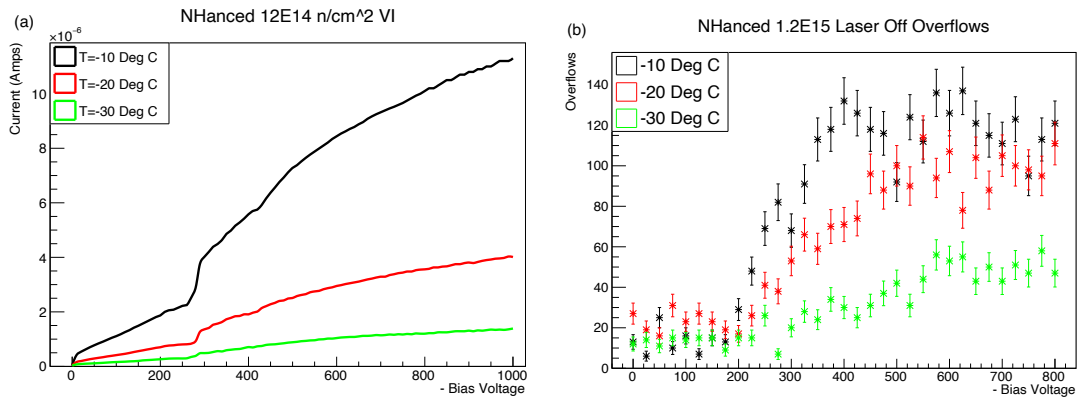


Figure 6. a) Current as a function of bias and temperature for an irradiated SOI HGAL sensor. All curves show a break at about 300 V. b) Number of events with signal beyond 3σ of the pedestal for various sensor temperatures for the HGAL sensor in a. There is a rapid increase in noise in the same region

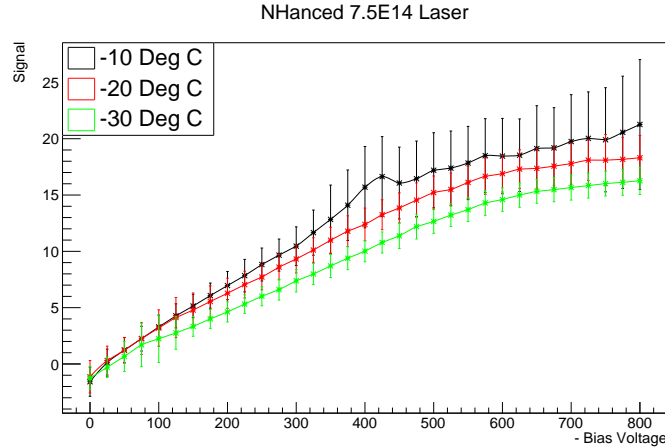


Figure 7. Laser signal as a function of voltage for three values of detector temperature.

A Run 3 HGC half-sensor was included in an neutron irradiation run at the RINSC reactor in Rhode Island. This run had an estimated 1 MeV neutron equivalent fluence of $1.2 \times 10^{15} n/cm^2$. In addition to the usual VI tests these devices were tested for charge collection with a 1064 nm laser and transimpedance amplifier. A 200 mm semi-automatic probe station equipped with a thermal chuck was used. A seven pin probe card provided contact to the central pad of the hexagonal array while maintaining ground potential in the six surrounding pads. Non-Gaussian noise is measured by counting events beyond 3σ of the pedestal. This is an indication of possible breakdown.

Voltage-current curves for the irradiated Run 3 sensor are shown in Figure 6a. The current ratios are consistent with the standard temperature dependence of leakage current. Figure 6b shows the number of non-Gaussian noise events in runs with the laser off. There is a increase in noise in the region between 200 and 300V. We note that this corresponds to a break in the leakage current VI curves in that region. We conclude that there is a possible onset of breakdown in this region.

Laser test charge collection results for the Run 3 sensor are shown in figure 7. We believe that the variation in charge collected with temperature is due to the temperature variation of the absorption coefficient for infrared light at this wavelength[9][1]. The charge collection appears to plateau at 600-700 Volts. The calculated in depletion voltage is ≈ 750 V for this fluence, including an estimate of the annealing in the reactor during exposure.

6 Conclusions

We have demonstrated the fabrication of 8" sensors with thin active regions using both SOI and SiSi bonded wafers. SOI bonded wafers with the handle wafers removed (Run 3), provided the best results, with acceptable leakage currents and breakdown voltage values and consistency. This run also demonstrated AC coupling resistors and capacitors with acceptable characteristics. A sample of Run 3 sensors were irradiated to $1.2 \times 10^{15} n/cm^2$. These showed the expected leakage current and depletion characteristics. Evidence was found for a non-Gaussian component of the noise above 300 Volts. We were unable to qualify the Si-Si process in these studies due to changes in fab site

and processing. The SOI process worked well and shows promise for future development of sensors with thin active layers.

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