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An Up/Down Converter for an LTE-A Transmitter in 0.18 um BCD

THESIS

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In Electrical Engineering

by

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Professor Michael Green, Chair
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I would like to thank MaXentric Technologies, LLC, who helped me with simulations and provided me the tools and equipment to fabricate and test my chips.

I thank my parents for allowing me to realize my own potentials and supported me toward fulfilling my dreams.

ABSTRACT OF THE THESIS

An Up/Down Converter for an LTE-A Transmitter in 0.18 um BCD

By

Pouria Khaliliadl

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Professor Michael Green, Chair

A new up/down converter system for LTE-A transmitter was presented. The chosen architecture eliminates the problem of LO-RF feedthrough in heterodyne transmitters. Using passive mixers and high bandwidth circuitry, acceptable gain flatness and linearity is achieved, making this system suitable for polar modulation. The circuit incorporating a number of elements in the system was fabricated in a 0.18μm BCD process that provides both high-voltage MOSFETS as well as low-voltage, high-speed MOSFETS, allowing implementation of both the PA and converter onto a single chip.

Chapter1: Introduction

The demand for higher data speed has increased tremendously during the 21th century. Significant research investment is ongoing to generate new standards and implementations in order to achieve a higher date rate for each user. The latest generation of mobile communication technology, i.e. 4G, requires a peak speed limit of 100Mbit/s downstream for high-mobility communication and 1 Gbit/s downstream for low-mobility communication, which is 10 times higher than the previous generation [1]. In order for Long Term Evolution –Advanced (LTE-A) to be considered as a candidate for 4G, a bandwidth as high as 100MHz is needed to support high-speed rates, which is five times higher than its previous generation, LTE. Implementing a transmitter that supports the 100MHz channel bandwidth, meets the linearity standards, and attains the desired efficiency is a significant challenge and a motivation for this thesis.

The other growing demand for cellular applications is to reduce the size and weight of the base stations while improving their efficiency. A desirable solution to reduce the form factor is to integrate the entire RF front-end, including envelope detector, envelope amplifier, power amplifier, mixers, and filters, onto a single chip. Among these various circuit blocks, the power amplifier and the envelope amplifier require a high-voltage process for implementation, such as the TSMC BCD (Bipolar, CMOS, DMOS) process [2], whereas the other blocks require circuitry capable of high speed. Thus in order to combine all these blocks using the same process, extra consideration in modeling and implementation should be made [3].

Implementing a System on Chip (SoC) transmitter as part of a microcell base station will also reduce its cost, thereby allowing more of them to proliferate on the network. A microcell is a mobile phone network cell served by a cellular base station covering a small area such as a

college or a hotel [4]. The data transfer rate will be faster in densely populated areas using microcells to improve the network capacity. In addition, a macrocell can be replaced with a number of microcells to improve the speed and reduce the power consumption. A macrocell is a mobile phone network cell served by a high-power cellular base station covering a large area such as a highway [5].

This thesis addresses the upconverter and downconverter stages, including the mixers for an LTE-A transmitter, and implements them in a 0.18μm BCD process, so that they can be implemented with other blocks into a single chip. This thesis is a joint effort with MaXentric Technologies, LLC, where a 5-watt envelope amplifier has already been implemented in the same process.

In Chapter 2 of this thesis, the structure and the frequency plan of the LTE-A up/down converter and different implementation methods are discussed. Chapter 3 focuses on the circuit level design and optimization. Chapter 4 describes the layout, fabrication, and the considerations one should make to implement an RF circuit in a BCD process. In Chapter 5, the RF PCB design, including the challenges of bonding the die directly to the PCB, is presented. The test results are also provided in this chapter. Chapter 6 concludes the thesis and provides suggestions for future research topics.

Chapter 2: Structure and Frequency Plan

Various topologies are available to be considered as a candidate for an LTE-A transmitter system. However, it is beneficial to divide these structures into to sub categories: Heterodyne conversion and direct conversion [6].

Heterodyne Conversion

The frequency plan of a basic heterodyne upconverter for an LTE-A system is provided in Fig. 2.1. The IF center frequency is at 50MHz to support 100MHz bandwidth. This frequency plan, which has the benefit of simplicity compared to multistage converters, is usually a candidate when there is not a hard requirement on the LO feed-through and image rejection. In fact, a major drawback of this structure is that the LO frequency exists within the RF signal band. As a result, the upconverter LO feedthrough might appear in the output spectrum and prevent the system from meeting the ACPR and spectrum mask standard requirements. Dealing with LO feedthrough becomes more severe in a passive mixer where rail-to-rail swing is desired to improve the linearity. It is beneficial to mention that filtering cannot be used to solve this problem since the LO is placed exactly at the edge of the signal, as shown in Fig. 2.2 (However putting a BPF will help to get rid of the image).

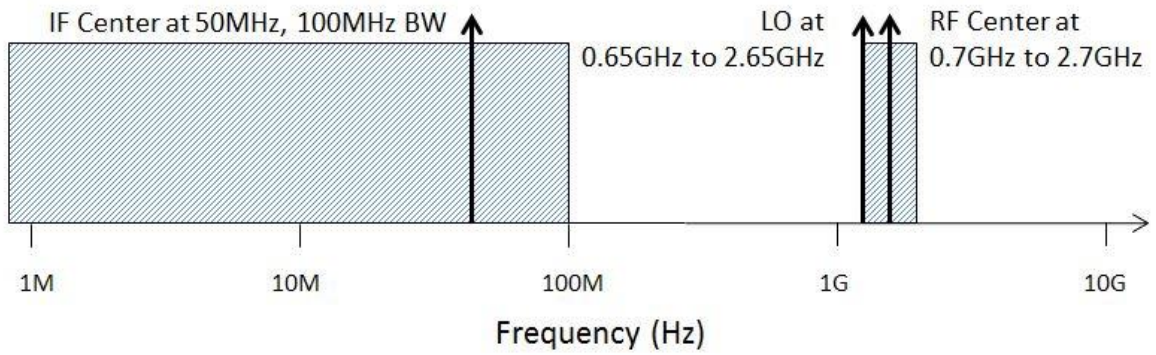


Figure 2.1. Frequency plan of a basic heterodyne upconverter.

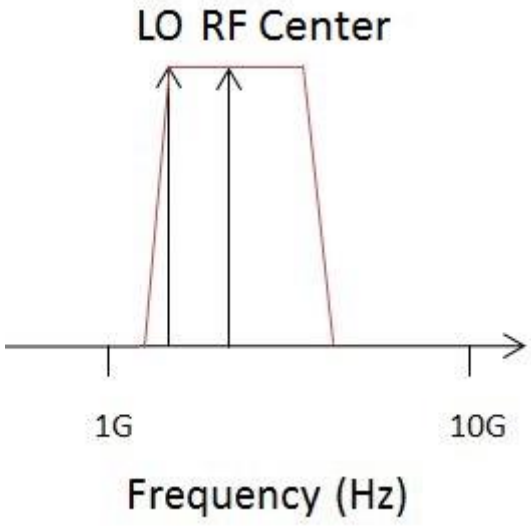


Figure 2.2. The effect of BPF on a basic heterodyne upconverter.

One solution for this problem is to generate the IF signal at a higher frequency so that LO is located outside of the signal bandwidth and then filter the LO with a tunable bandpass filter (BPF) as illustrated in Fig. 2.3. However, a sharp tunable BPF is not easy to design and has its own challenges. In addition, there is a trade-off between the maximum IF frequency and the speed of the digital-to-analog converter (DAC) creating the IF signal. Based on the Nyquist theorem, The DAC speed should be at least twice the maximum IF frequency. In Fig. 2.1 the maximum IF frequency is 100MHz. Thus, a DAC operating at 200MSPS is needed. Low cost, low power DACs currently available have a maximum speed of 250MSPS [7]. Therefore, the maximum IF frequency should not go above 125MHz, and for a 100MHz bandwidth signal, the relevant maximum center frequency is 75MHz, which gives a margin of 25MHz for the BPF to attenuate the LO feed-through.

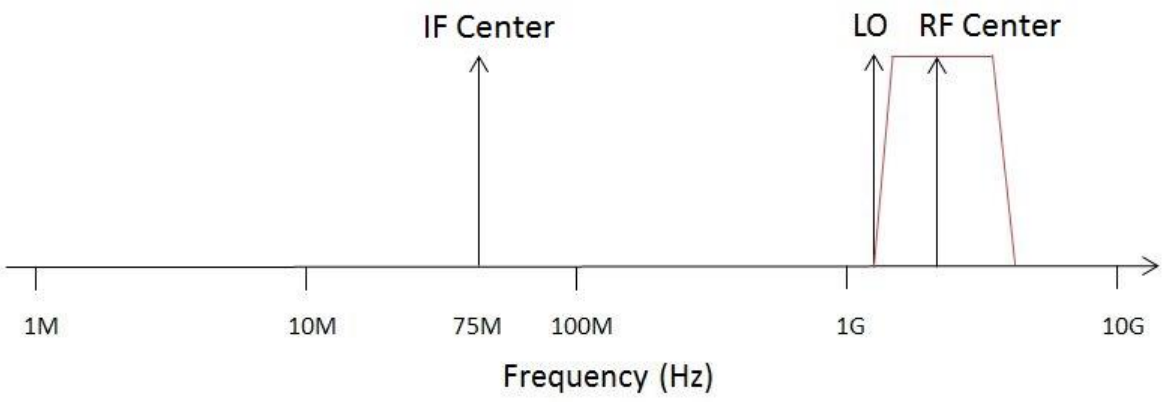


Figure 2.3. The effect of BPF when IF center frequency is shifted to 75MHz.

LO feedthrough does not have the same effect in downconversion since it is placed outside of the band of interest. Nevertheless, the effect of the 3rd-order nonlinearity must be considered.

The block diagrams of the entire microcell up-down converter for both 50MHz and 75MHz center IF frequency are shown in Figs 2.4 and 2.5, respectively. An IF of 75MHz is a more appropriate candidate here since it provides better LO isolation.

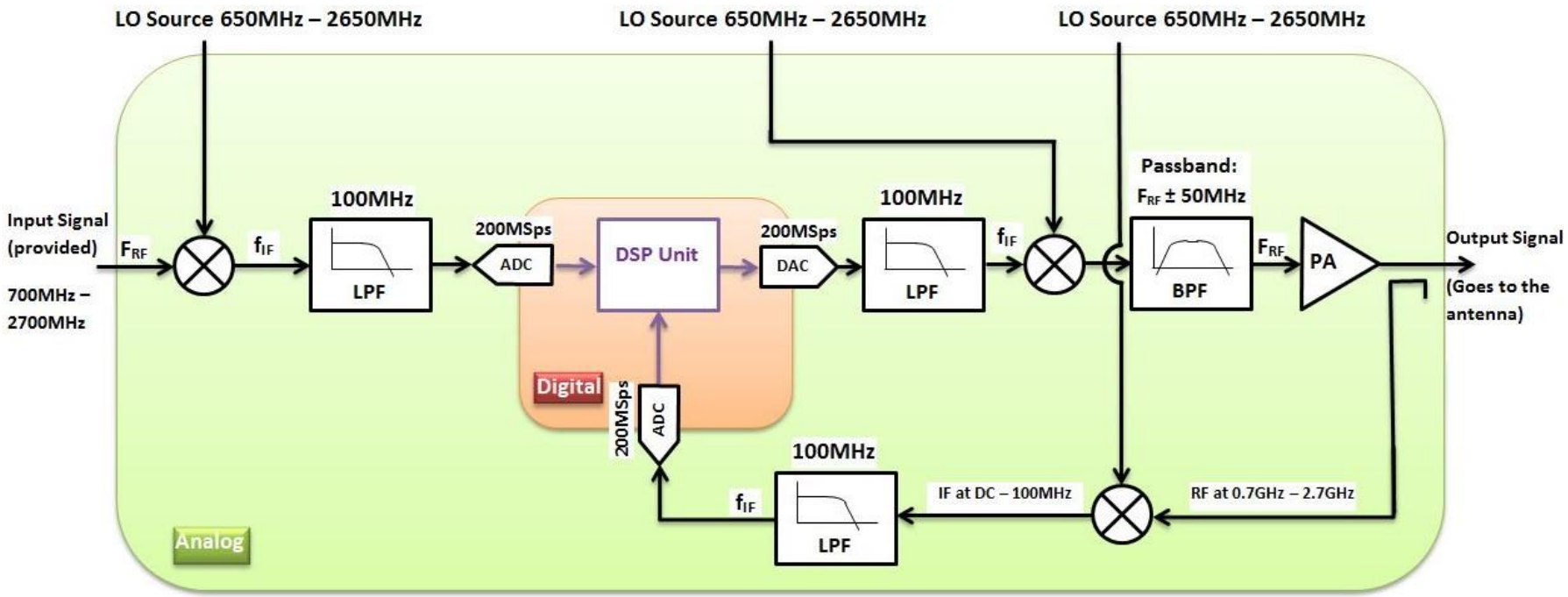


Figure 2.4. Block diagram of microcell with IF center frequency at 50MHz.

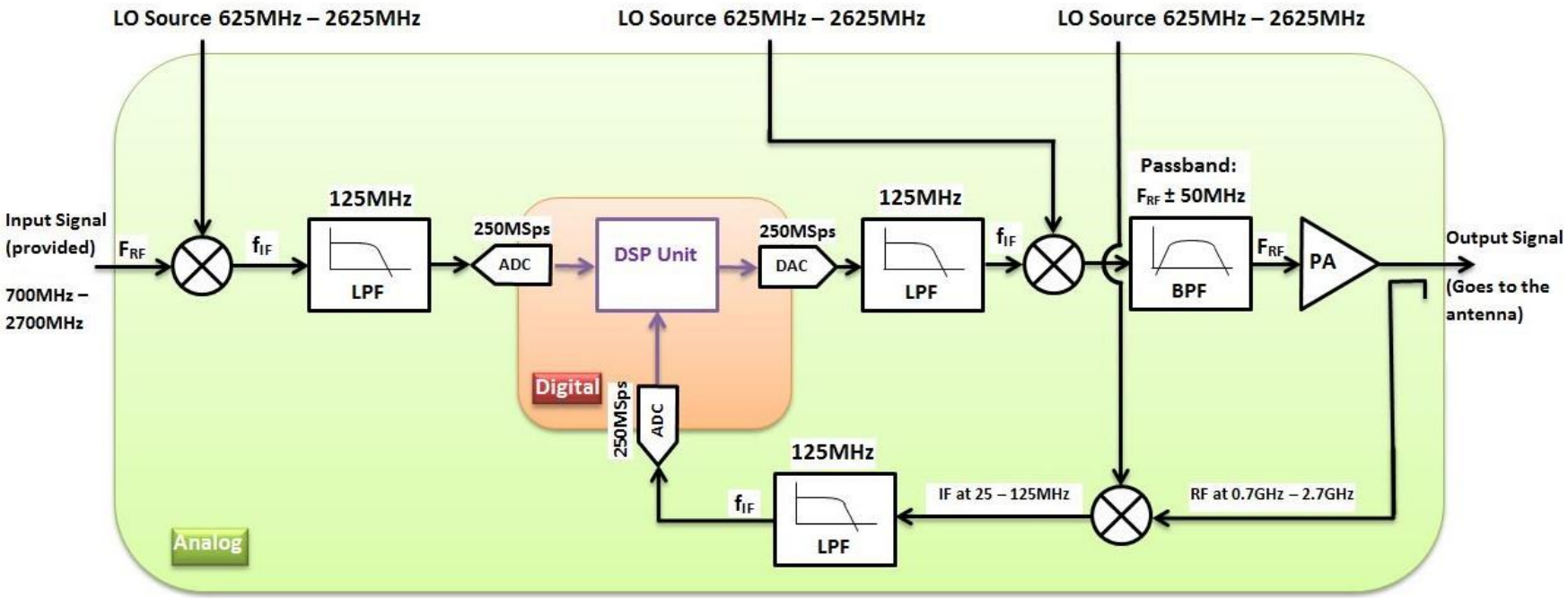


Figure 2.5. Block diagram of microcell with IF center frequency at 75MHz.

Direct Conversion

The frequency plan of a basic direct upconverter is shown in Fig. 2.6. One of the main advantages of this structure over the heterodyne transmitter is the absence of spurs in the output spectrum. However, direct conversion has many other issues, such as more complexity (i.e. two chains required instead of one chain), LO feed-through (since LO and RF are located at the same frequency, it is not possible to filter out the LO), and LO pulling. Since the main target of this thesis is to eliminate the LO feed-through, and polar modulation is used (no I/Q channels), this structure is not applicable.

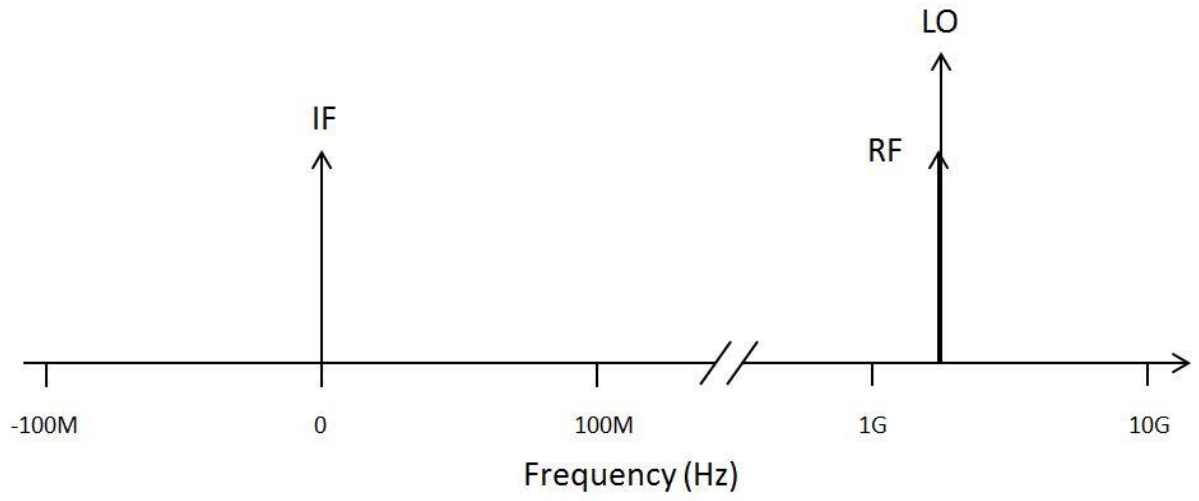


Figure 2.6. Frequency plan of a basic direct upconverter.

Two-Step Heterodyne Conversion

In this method, instead of upconverting the IF signal directly to the desired frequency, the IF signal is first upconverted to another intermediate frequency, and then it is converted to the desired frequency through a second converter. This method can have different benefits based on the way it is implemented. This method provides more flexibility in choosing the LO frequencies, which results in control over spurs frequencies. However, this structure consumes more power and generally need two LO synthesizers. In special cases, where LO_2 is a multiple of LO_1, one synthesizer can be used. The frequency plan for a 75MHz IF is provided in Fig. 2.7, where the IF signal is mixed with LO_1 to achieve $IF_1 = IF + LO_1$. Then, IF_1 is mixed with LO_2 to get the desired $RF = IF_1 + LO_2$.

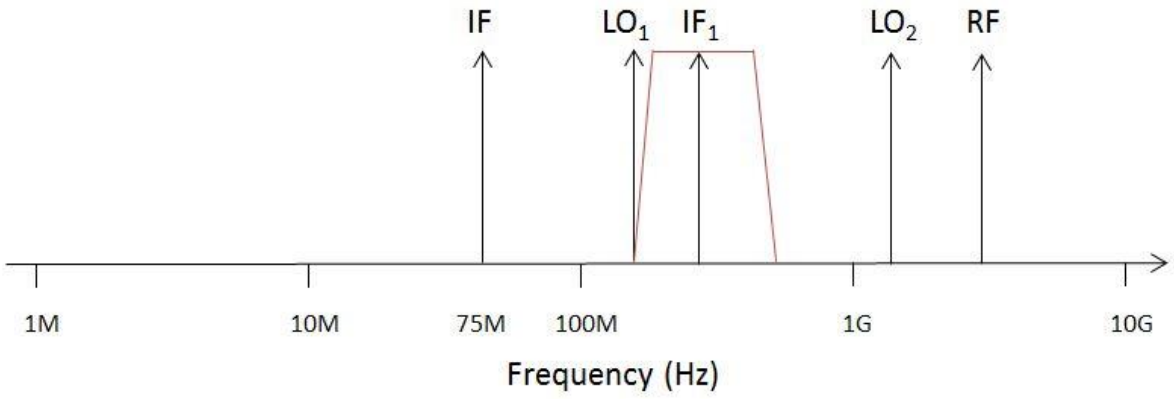


Figure 2.7. Frequency plan of a two-step Heterodyne upconverter.

Based on LO_1 and LO_2, different spurs may exist in the output spectrum. However, in order to choose LO_1 and LO_2 appropriately, considering the LO feed-through, a reasonable approach is to consider the following cases:

1. IF_1 < 225MHz: In this case LO_1 feedthrough will be added to the IF signal in low-side injection mode (i.e. LO < IF_1), which is undesirable. Even if high side injection mode (LO > IF_1) is used, IF to IF_1 feed-through is still undesirable.
2. 225MHz < IF_1 < 725MHz: In this case LO_1 feed through can be suppressed by a BPF, but with the existence of LO_2 for some frequencies within the band of interest, (i.e. 700MHz ~ 2700MHz), this frequency plan is not a complete solution. For example, if the target RF frequency is 1.8GHz, IF_1 must be set somewhere between 1050MHz ~ 2550MHz. It is possible to divide the desired band into two or three sub-bands and use multiple converter chains in parallel to solve this issue. However, this method will add to the system complexity.
3. 725MHz < IF_1 < 2625MHz: In this case LO_1 is within the band of interest. It is possible to use a BPF to suppress LO_1 feed-through. But, for RF frequencies near LO_1, LO_1 to RF feed-through will be problematic.
4. 2625MHz < IF_1: In this case, LO_1 can be placed at a frequency higher than 2700MHz, (for 2625MHz < IF_1 < 2775MHz only high-side injection is applicable) and can be attenuated by a fixed BPF. LO_2 will be placed inside the band of interest if low side injection is used in the second conversion. But, in case the high-side injection mode is used, LO_2 will also be outside the band of interest. For example the frequency plan for this mode is shown in Fig 2.8 for IF_1 = 3GHz.

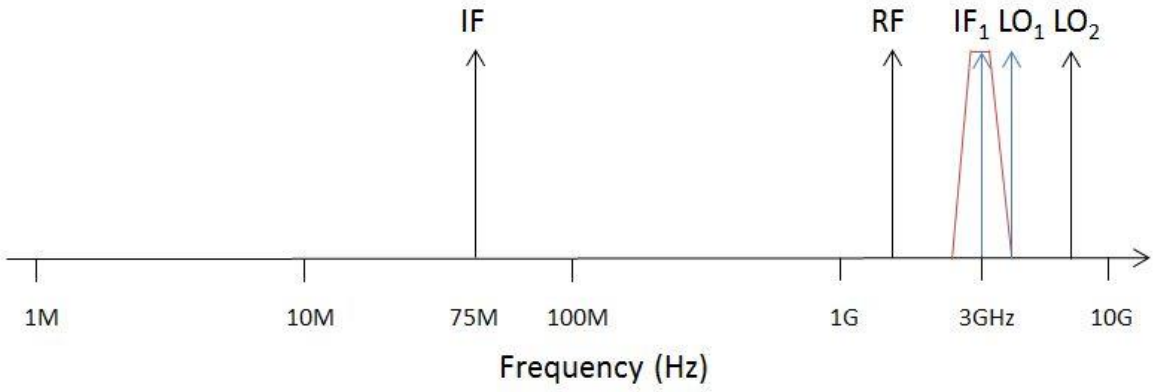


Figure 2.8. Frequency plan of a two-step Heterodyne upconverter with IF_1 at 3GHz.

Based on the above explanations, the fourth case seems to provide the best result. But there are a few points needed to be mentioned as follows:

1. Since a 0.18um BCD technology is used in this project, it is not desirable to increase the maximum frequency of the system, which is determined by LO_2. For the lowest frequency solutions, LO_2 frequency goes up to roughly 6GHz. Thus it is desirable to keep LO_1 as low as possible.
2. A tunable BPF or LPF might still be needed after the second converter to suppress the spurs. But there is no need to make it as sharp as the case only one converter is used.
3. At least two synthesizers are needed for upconversion. The downconversion LO can be derived by mixing upconverter LOs or by a third synthesizer.
4. For testing purposes, LO_2 cannot be applied off-chip through an FR4 PCB. Dielectric material with better high frequency performance (i.e. lower loss) is needed, which increases the cost. For this thesis, Rogers 4003 is used.

A block diagram of the microcell with a two-step upconverter is shown in Fig. 2.9. This thesis focuses primarily on the mixers and the BPF filter is implemented off-chip.

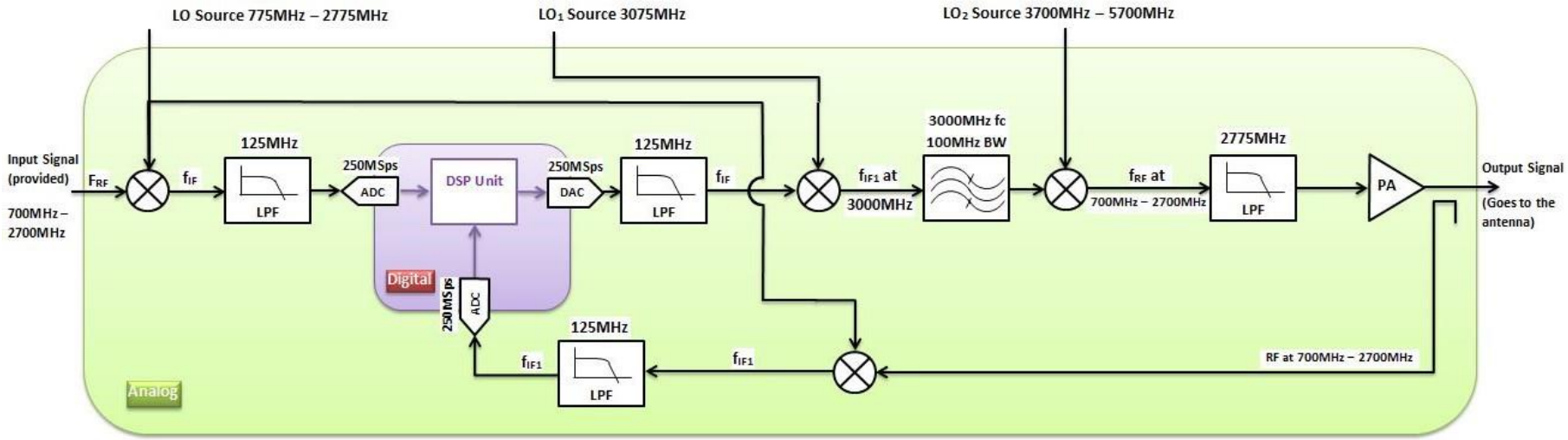


Figure 2.9. Block diagram of the microcell with a two-step upconverter and IF center frequency at 75MHz.

Chapter 3: Mixer Structure and Design

There are many mixer candidates for the LTE-A up/down converter. To choose the suitable structure, various factors must be considered. In this chapter these factors and the design trade-offs are discussed.

Passive vs Active Mixers

Mixers are usually divided into two types: active mixers and passive mixers [8]. Examples of each one are provided in Fig. 3.1(a) and (b), respectively. Generally speaking, the following criteria can be used to determine which mixer type is more suitable for this application.

1. Linearity: passive mixers are normally more linear than active mixers. Active mixers linearity is limited by their gain compression.
2. Bandwidth: passive mixers usually provide wider bandwidth than active mixers. The frequency response of the active mixers is limited to $R_{output} \times C_{output}$, whereas passive mixer output can be connected to the gate of a transistor.
3. LO swing: passive mixers require high LO swing to turn the mixer transistors on and off, preferably rail-to-rail, whereas active mixers can operate with low LO swing.
4. Gain: mostly, active mixers can provide voltage gain whereas passive mixers cannot.

Since one of the targets of this thesis is to improve the linearity, the passive mixer is chosen, and the other drawbacks are compensated. Since high LO swings are not usually available, LO buffers are designed so that they can provide enough current to turn the mixer transistors on and off (more details are provided in the "LO Buffer" session). Also, a differential amplifier stage is added after the mixers to compensate for the mixers losses [6]. By introducing this post-amp, the

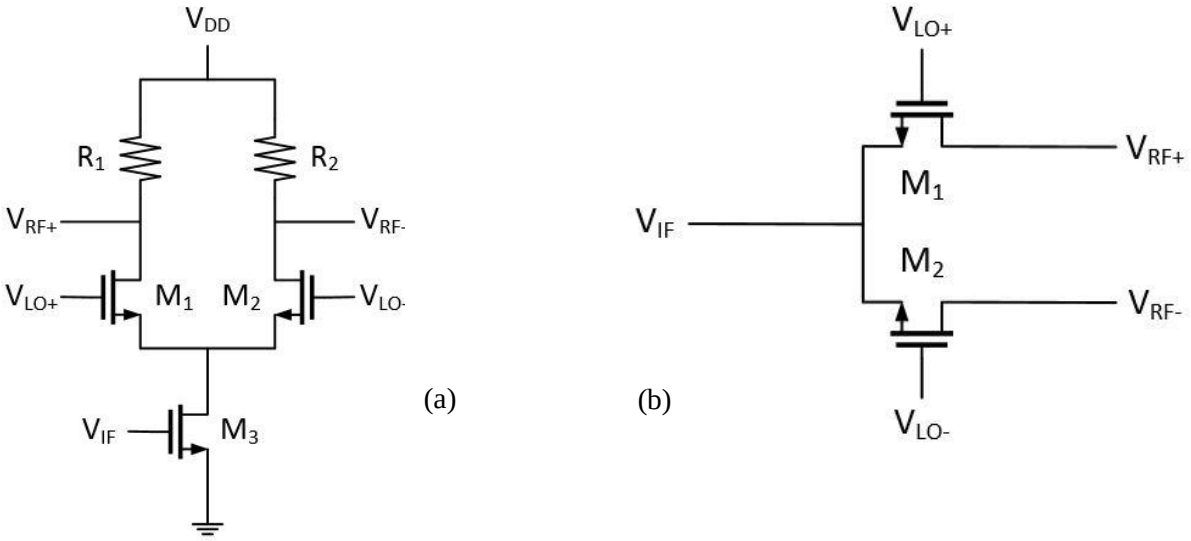


Figure 3.1. Single-balanced mixers (a) active (b) passive

load of the mixer becomes pure capacitive. Considering these facts, the mixer structure is improved as shown in Fig. 3.2.

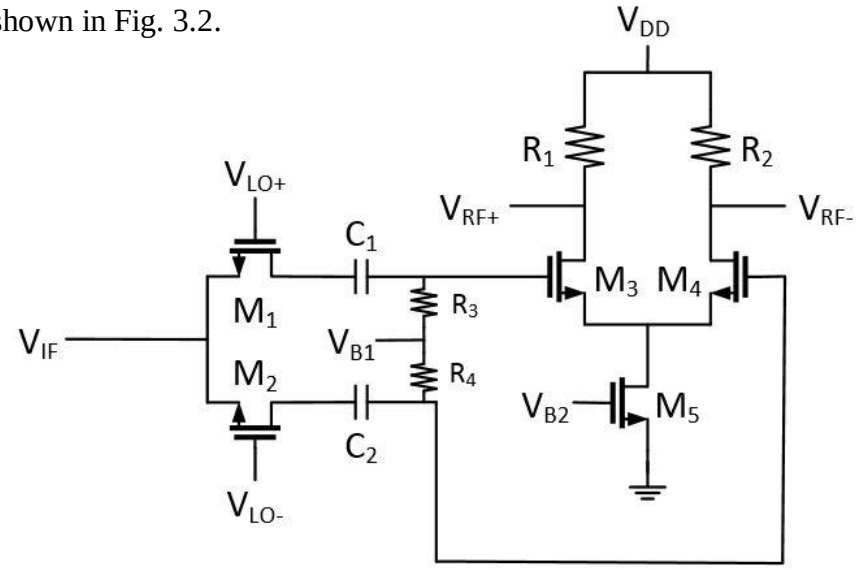


Figure 3.2. Passive mixer with post-amp (single-balanced).

Single-Balanced vs Double-Balanced Mixers

The structures shown in the previous section are known as single-balanced, which has a major disadvantage, which can be problematic in meeting the spectrum standards. Assuming a coupling between $V_{LO+/-}$ and $V_{RF+/-}$ equal to $+/-\alpha V_{LO}$ results in an LO feed-through equal to $2\ \alpha V_{LO}$, which

is called LO-RF feedthrough [6]. A good solution for this problem is to use the double-balanced structure, as shown in Fig 3.3 [8]. The idea is to use two single-balanced mixers, shown in Fig. 3.1(b), in parallel with opposite feedthrough so that they cancel out each other. One drawback of this structure is the need for differential input, where a differential DAC might not be always available. Thus, an extra on-chip single-to-differential converter stage or an off-chip balun is needed. The other drawback is that the capacitance at RF+/- becomes larger due to the presence of more transistors. Thus the current driving capability of the LO buffer must be higher compared to the single-balanced structure. Due to the better LO isolation, the double-balanced structure is chosen over the single balanced mixers and an appropriate LO buffer is designed. An off-chip balun is used to generate V_{IF}+/-. Based on [1], the maximum conversion gain of a passive double balanced mixer is $2/\pi$, or -3.92dB. For an upconverter, conversion gain is defined as the ratio of the rms voltage of the RF signal to the rms voltage of the IF signal.

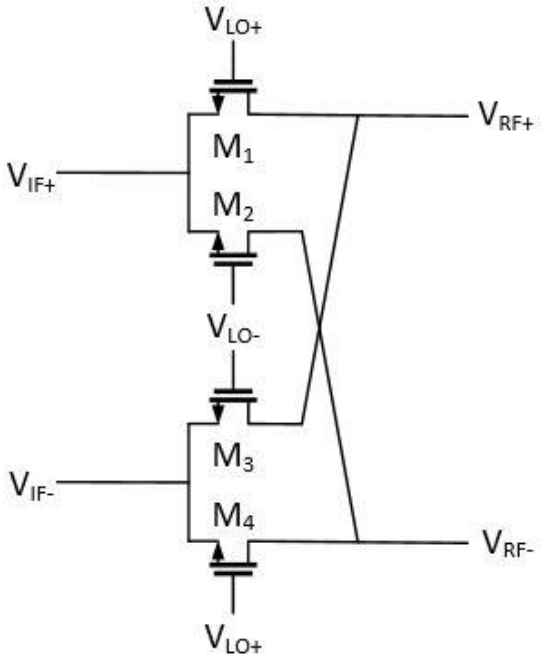


Figure 3.3. Double balanced passive mixer without post-amp.

LO Buffer

Since the passive mixer structure is used, it is more desirable to have square wave LO to turn the transistors on and off faster. An LO buffer has the benefit of providing more driving capability as well as representing fast transitions so that the LO signal after the buffer is closer to square wave. The structure is realized as a differential amplifier with a cross-coupled pair of transistors connected to the output, which is similar to a CML latch. For linear buffers such as the differential stage, t_{rise} and t_{fall} at the output are limited to t_{rise} and t_{fall} of the input signal. Thus, for a sinusoidal input, there will be a sinusoidal output. Utilizing a transistor cross coupled pair at the output with the differential stage helps in making the transitions faster by introducing a positive feedback and making the buffer nonlinear. It is beneficial to point that the sizes of the cross-couple pair transistors should be smaller than the common source ones to avoid latch-up. In addition, the output capacitance increases by adding the cross coupled pair, reducing the bandwidth. The size of both differential stage transistors and cross-coupled pair transistors are optimized by simulations so that the minimum rise-time and fall-time is achieved in time domain. The schematic of the buffer including the numeric design is provided in Fig. 3.4.

To design the LO buffers, one of the important points is to make sure that the buffer is capable of driving the mixer transistors at the maximum frequency of interest. It is also desired to generate a square wave LO [6]. However, due to technology speed limitations, such as transistors t_{rise} and t_{fall}, at high frequencies, the buffer output is similar to a sine wave rather than a square wave. The transient response of the buffer at 5.7GHz is shown in Fig 3.5. Simulations also show that for $V_{B1} = V_{B2} = 750mV$, and $V_{in,Bias} = 1.0V$, the fastest transition with adequate swing range, up to

600mV, can be achieved. Using these voltages, the current consumption of the LO buffer is 5.16mA.

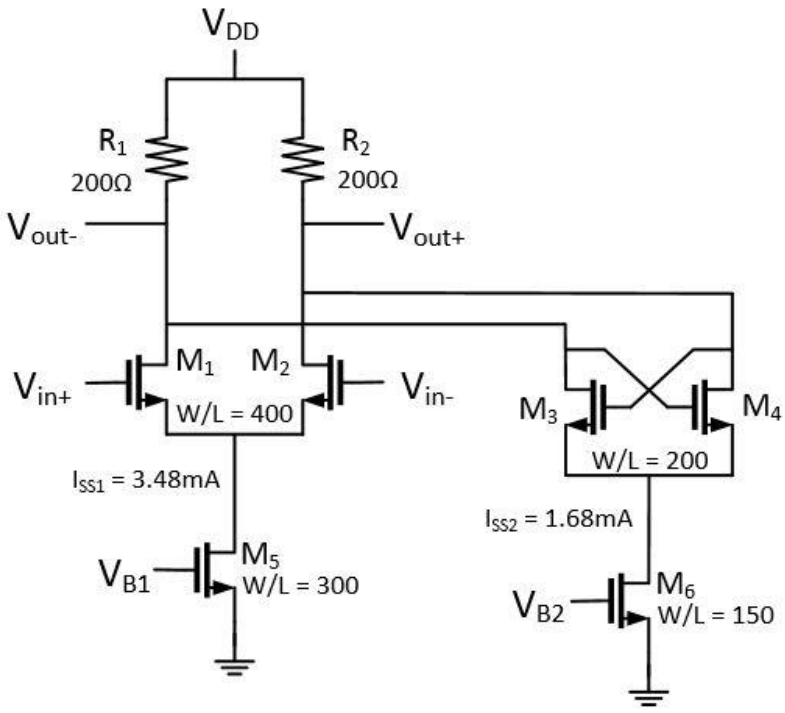


Figure 3.4. LO buffer schematic with numerical design.

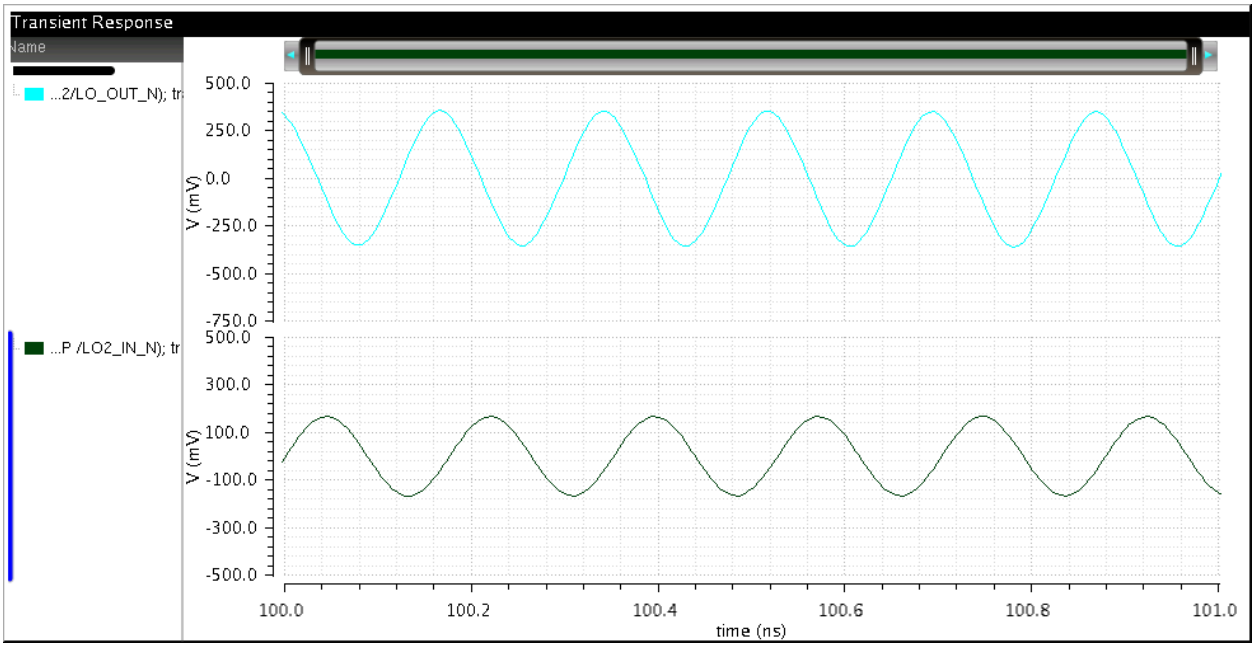


Figure 3.5. LO buffer transient response for 5.7GHz.

Post-Amp Differential Cascode Structure vs Differential Structure

Instead of differential amplifier as the post-amp as shown in Fig 3.2, it is possible to use a differential cascode structure, as shown in Fig. 3.7. Using the cascode structure exhibits improved input-output isolation [9]. In addition, a cascode structure provides more gain robustness over the RF band of interest since its output resistance is higher by a factor of $g_m \times r_o$ and it has less effect on the gain when it is connected in parallel to the load. It is also beneficial to mention that PMOS active load cannot be used for these post-amps due to their bandwidth requirement. The main problem with the cascode structure is the voltage headroom. For 0.18um CMOS technology, where V_{DD} = 1.8V, and large signal input, using cascode requires inductive load instead of resistive load to bias the output DC voltage close to V_{DD} [10]. Chock inductors can be used on-chip or off-chip; the following issues should be considered:

1. On-chip inductor models are not available in the BCD process. Thus EM simulations are required to obtain an appropriate model.
2. In the BCD process, unlike the RFCMOS processes, the thickness of metal 6 is not high enough to achieve high-Q inductors.
3. An Off-chip inductor can provide much higher Q than on-chip inductor.
4. The use of an inductor can put stress on the post-amp transistors. In particular, the drain voltages of the output transistors will go above V_{DD}.
5. The post-amp frequency can go up to 3GHz. Therefore, the resonance frequency of the inductor should be higher, and the inductor should have high Q for frequencies up to 3GHz.
6. For the off-chip inductors, to achieve a higher resonance frequency, the inductor should become smaller. But there is a physical limitation on how small it can become. Normally

0201, 0402, and 0603 packages are the smallest common ones available. For these packages, the maximum available inductor value is about 10 ~ 20nH.

7. The inductors can be considered as part of the output matching network. In particular, an inductance value of 10-20nH can affect the matching performance slightly. It is important to mention that narrow band matching is required for the first upconverter, and wideband matching is needed for the second upconverter.

With the above considerations, off-chip inductors were chosen. A schematic of the final mixer and post-amp is shown in Fig. 3.6.

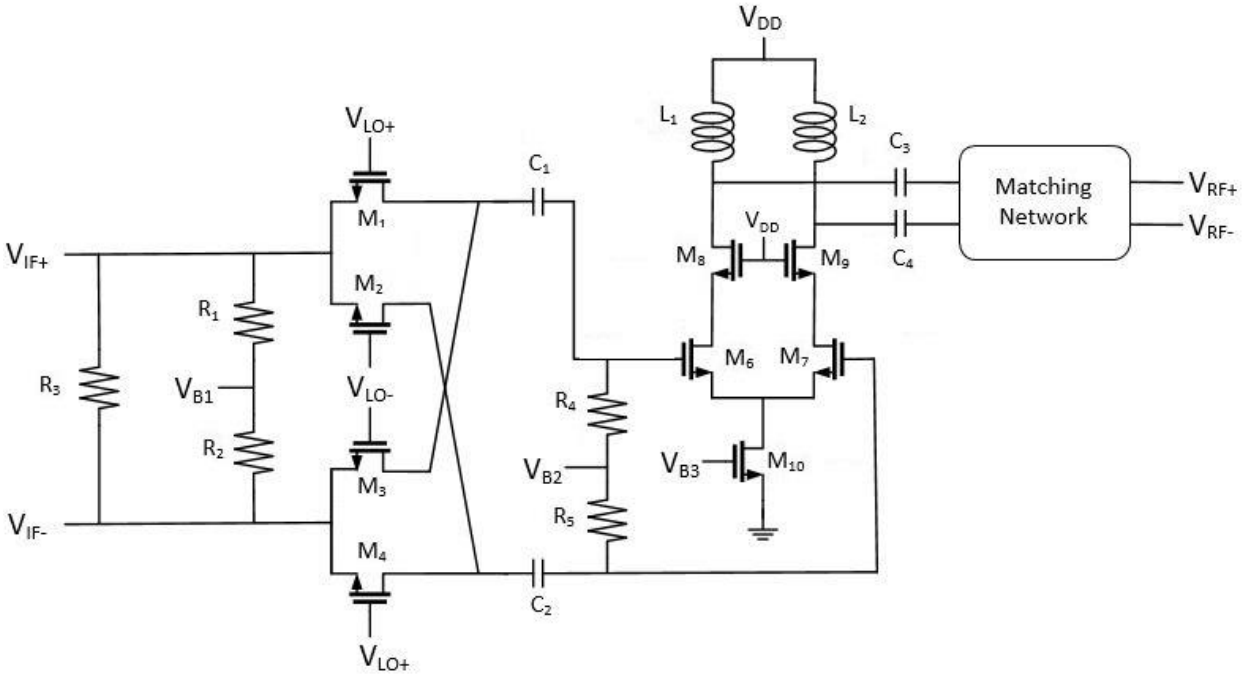


Figure 3.6. Double balanced passive mixer and cascode post-amp.

Gain Budget and Matching

Now that the structure of the mixer has been finalized, it is useful to discuss the following facts in determining the power levels and power consumption.

1. Since the RF frequency is not too high, it is possible to use 50Ω resistive termination directly at the input without the need for a matching network. In particular, assume a worse case capacitance of 0.3pF at 6GHz. The equivalent impedance of this capacitor can be derived as:

$$|Z_C| = \left|\frac{1}{jC\omega}\right| \Rightarrow \tag{3.1}$$

$$|Z_C| = \frac{1}{2\pi \times 0.3p \times 6G} = \frac{1000}{1.8\pi} = 177\ \Omega >> 50\ \Omega \tag{3.2}$$

2. It is beneficial to have an idea of how high the mixer gain can be. To have a good understanding, the first and second mixers should be analyzed separately. For the first mixer, narrowband output matching can be used at the output. Thus it is possible to increase the impedance seen at the output of the upconverter post-amp by proper LC matching. However, the following considerations should be made.
   a. First, the signal after the matching is the signal of interest. Considering the fact that the matching network is equivalent to a n:1 transformer at the frequency of interest, the voltage gain of the post amp is increase by n^2 whereas the output voltage of the post amp is divide by a factor of n. Thus, increasing the ratio of the matching network by n will result in a $\sqrt{n}$ increase in power gain (the output resistance of the post-amp is assumed to be much larger than $n^2 \times R$).
   b. A π-matching network is used for the first converter output matching, with two parallel capacitors and a series L, as shown in Fig 3.9(b). This structure has two main

benefits over a two-element LC structure. First, due to the presence of an extra passive element, there is more degree of freedom in the design. Second, the output capacitance of the first converter and input capacitance of BPF can be considered as part of the first and the second capacitors, respectively. As a result, the effect of ESD protection capacitance and packaging capacitance is minimized.

c. There is an upper limit for the impedance ratio of the output matching network due to the availability of the matching elements. Also if the parallel capacitors value become comparable with chip output capacitance, the idea of absorbing the output capacitance will not be as effective since its value cannot be determined accurately. At the frequency of interest, i.e. 3GHz, a ratio of 2:1 is acceptable, but higher ratio is problematic (It will be shown later on this chapter that a ratio of higher than 2:1 will result in an input capacitance of less than 800fF). This ratio results in an output impedance of 200Ω for the post-amp (The reason why the output resistor is chosen to be 200Ω is discussed later in this chapter).

3. To have a gain of at least π/2 to compensate for the mixer loss, g_m of the post-amp transistors should satisfy the following criteria for a 200ohm load.

$$Gain_{post-amp} = g_{m,1,2} \times R_{out} \quad where \tag{3.3}$$

$$R_{out} = (r_{o.3,4} \times (1 + g_{m,3,4}\, r_{o.1,2})) \,||\, 200\Omega \approx 200\Omega \quad => \tag{3.4}$$

$$g_{m,1,2} \geq 7.85mS \tag{3.5}$$

4. The PA of the microcell requires single-ended 0dBm input and 50Ω matching. The relevant voltage swing can be calculated as:

$$P_{dBm} = 10 \times \log \frac{P}{1mW} \quad => \tag{3.6}$$

$$P_{dBm} = 10 \times \log \left(\frac{V_P^2}{2R} \times 1000\right) \quad \& \quad R = 50\Omega \quad =>$$

$$P_{dBm} = 10 \times \log\,(10 \times V_P^2) \quad =>$$

$$P_{dBm} = 10 + 20 \times \log V_P \quad => \tag{3.7}$$

$$0 = 10 + 20 \times \log V_P \quad => \quad V_P \approx 316\,mV \tag{3.8}$$

5. Considering the fact that this high g_m requires large transistors, the limitations on how large the transistors can get (more discussed in the layout section), and the large required output swing, it is concluded that 0.18um CMOS is not suitable to derive a 0dBm input PA, and pre-amps are needed in between.
6. There is an indirect trade-off between the power consumption and the linearity. It is possible to lower the power levels for the mixers and use more gain in the pre-amp to achieve 0dBm. However, more gain means consuming more power.
7. On important issue is that the PA output power is 5W for a 10W power consumption, roughly. Thus the PA efficiency is about 50% without the up/down converter. Consuming more power reduces the PA efficiency. For example 1W more power consumption drops the PA efficiency to 45.45%, about 4.55% less.

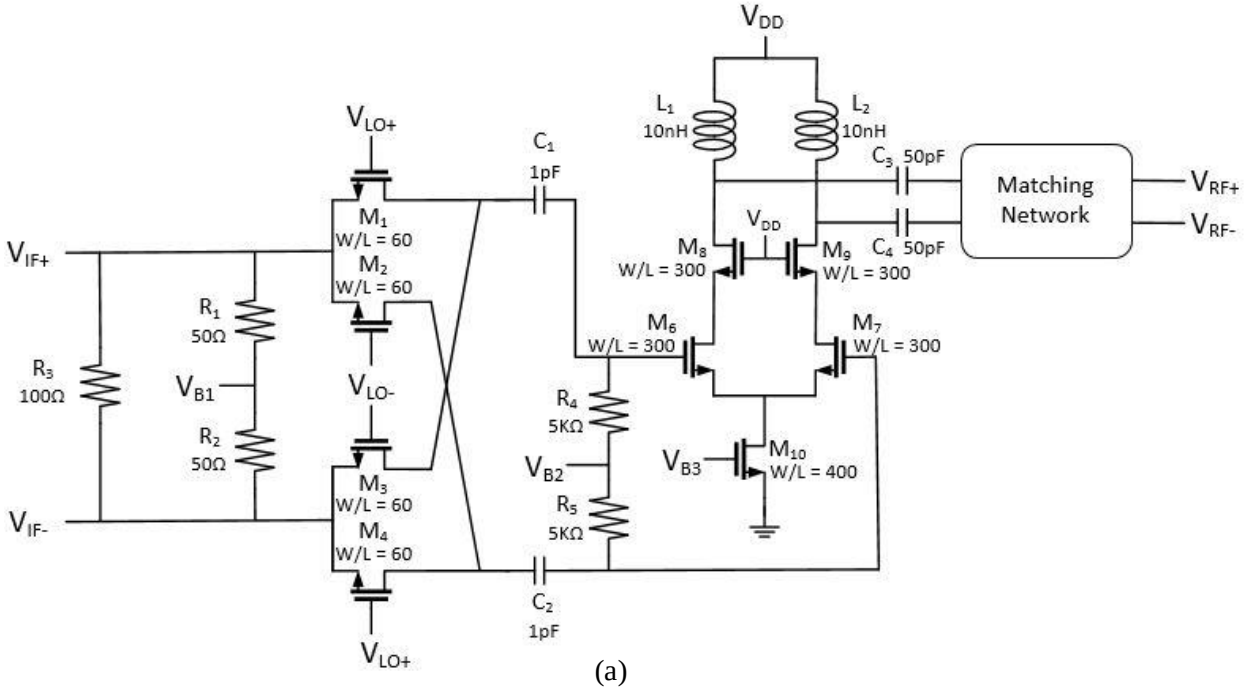
Mixer Design

Designing a passive mixer is not a simple process and has its own challenges. Several simulations are required to optimize the mixer to achieve appropriate results. The goal of the design and optimization should be set accurately to have fair comparisons. The following criterion is the main rule used to design the mixer in this thesis.

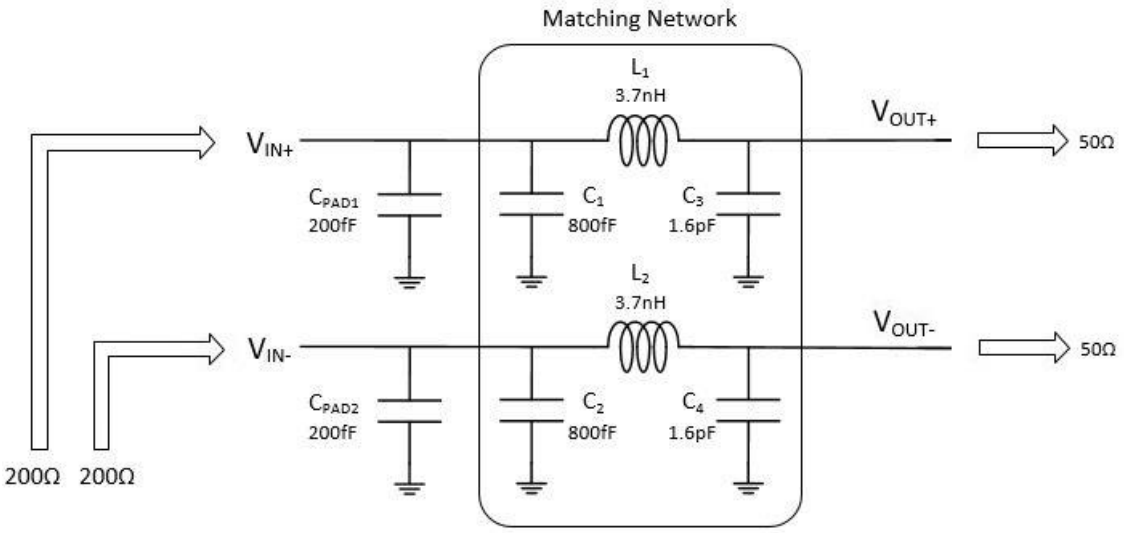
The mixer is optimized to achieve the best linearity over the desired frequency range while keeping its conversion gain close to maximum, i.e. 2/π. The optimization for the linearity can be accomplished by achieving the sharpest t_{rise} and t_{fall} for the mixer output at

maximum frequency. The input impedance of the mixer should remain much higher than 50Ω to be considered negligible.

The ratios of the final design of the first up-mixer are provided in Fig. 3.7(a). The input resistors R_1 and R_2 are implemented on-chip and R_3 is placed off-chip. In this case, it is possible to remove R_3 and use only one of the branches as a single-balanced mixer for testing purposes. The second up-mixer has a similar structure. However, R_1 and R_2 are omitted due to 50Ω input matching and there is no output matching circuit to provide wideband output matching. A useful point is that for a passive upconverter, achieving a maximum gain of $2/\pi$ is equivalent to have the envelope amplitude of the output similar to input signal itself, as demonstrated in Fig. 3.8. Based on the simulations, there are optimum bias voltages to achieve the best linearity. For the double balanced passive mixer, V_{GS} of the switches should be set close to V_{th} for optimum switching so that only two of the four switches are on. The optimized DC voltages are derived as V_{B1} = 150mV, $V_{LO,bias}$ = 750mV, V_{B2} = 1.4V, and V_{B3} = 840mV.



(a)



(b)

Figure 3.7. (a) First upconverter schematic with transistors ratios and passive values (b) Designed off-chip matching network.

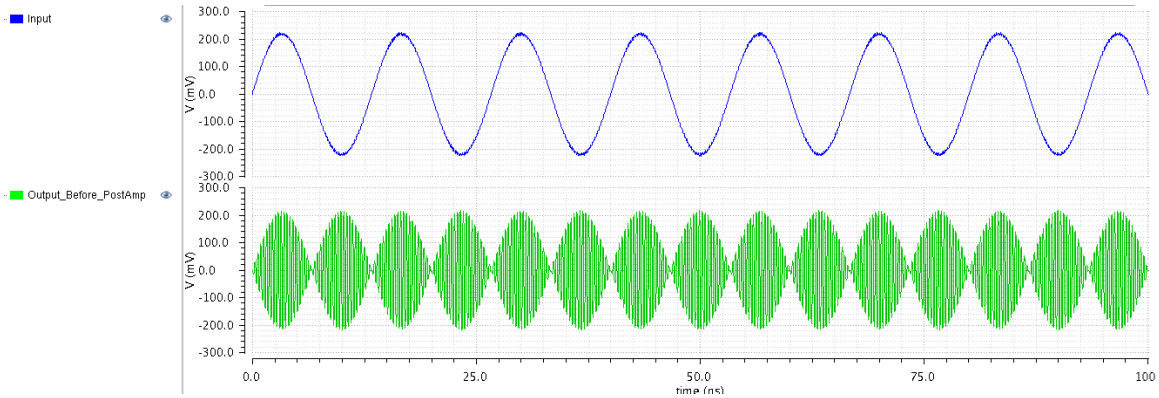


Figure 3.8. Transient response of the passive part, image signal not filtered.

The buffer stage (post amp) can provide a gain of at least π/2 to compensate for loss in the passive mixer. There is a trade-off between the gain of the post-amp and the power consumption [9]. In this project, the total gain of the first upconverter is measured to be 1.20 V/V for a 1.69mA post-amp current and 200Ω output resistance (output resistance choice is discussed more in the next page). Also the gain of the post-amp should remain constant for the IF signal range of 25-125MHz. The simulation result of the gain flatness is provided in Fig. 3.9.

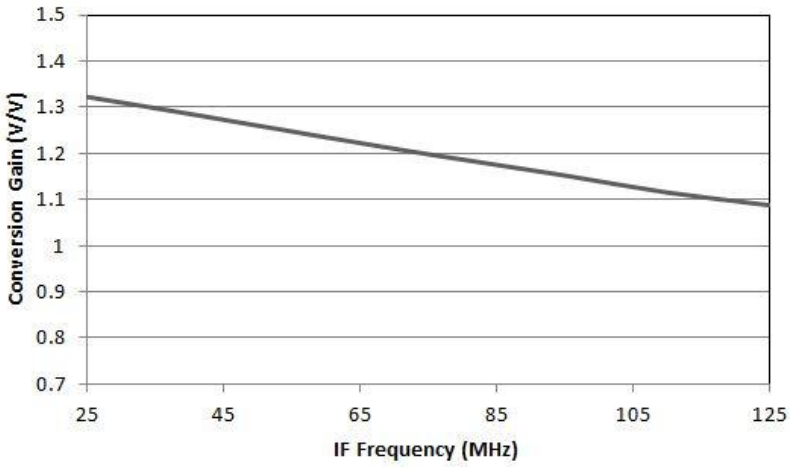


Figure 3.9. Gain Flatness over the frequency.

The above figure demonstrates 0.35dB gain flatness for a 20MHz signal bandwidth centered at 75MHz. The BPF response can compensate for part of the gain variation if its response is the opposite to the upconverter.

The input impedance of the BPF used after the upconverter is generally 50Ω. Also a maximum ratio of 2:1 can be achieved due to physical off-chip element limitations. The structure of the matching network with numerical values is shown in Fig. 3.7(b). Increasing the ratio more than this value increases the risk on degrading the matching performance at the output since the smaller elements introduce larger tolerances and C_1 and C_2 values become closer to the pads capacitances in the mixer chip (This capacitor value cannot be predicted accurately because of packaging and bondwiring effects). A ratio of 2:1 results in an output capacitance of $50\Omega \times 2^2 = 200\Omega$ output resistance. To achieve a gain of at least $\pi/2$ in the post-amp, a minimum g_m of 7.85mS is required, which corresponds to 1.69mA total current consumption when optimizing the solution for the best linearity.

As mentioned before, the first upconversion has a fixed output frequency, 3GHz. However, the second conversion should provide solution for the wide range. The frequency response of the

whole chain (1st upconverter-BPF-second upconverter) is shown in Fig 3.10. A -12dB gain drop is caused due to the 50Ω output resistance (instead of 200Ω) in the second upconverter.

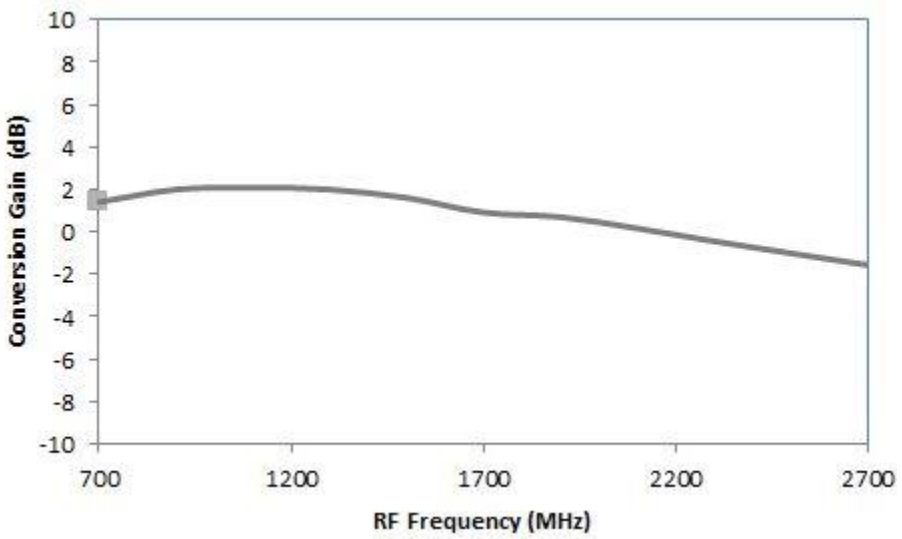


Figure 3.10. Gain flatness vs carrier frequency, 10V/V gain block is added at the output.

The output spectrum after the second upconverter at 2.1GHz carrier frequency is shown in Fig. 3.11.

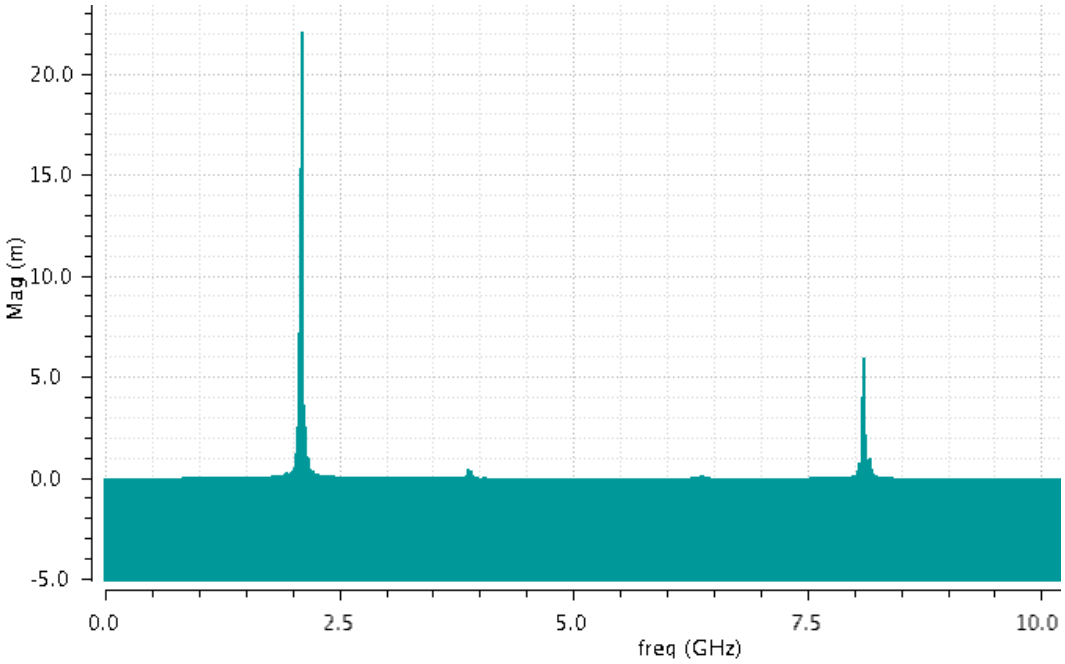


Figure 3.11. Spectrum for 2.1GHz carrier frequency, spurs only exist output of band.

To measure the mixer linearity, the Quasi-Periodic Steady State (QPSS) analysis was performed for the first upconverter to measure P_{1dB}. The result, shown in Fig. 3.12, demonstrates that a P_{1dB} of 2.1dBm was achieved.

From Fig. 3.14 the calculated IIP3 and OIP3 are calculated as follows:

$$IIP3 \approx P1dB + 9.6dB \Rightarrow IIP3 \approx 11.1dBm \quad (3.9)$$

$$OIP3 \approx IIP3 + Gain \Rightarrow OIP3 \approx 11.1dBm + 20\log(1.2) = 12.7\text{dBm} \quad (3.10)$$

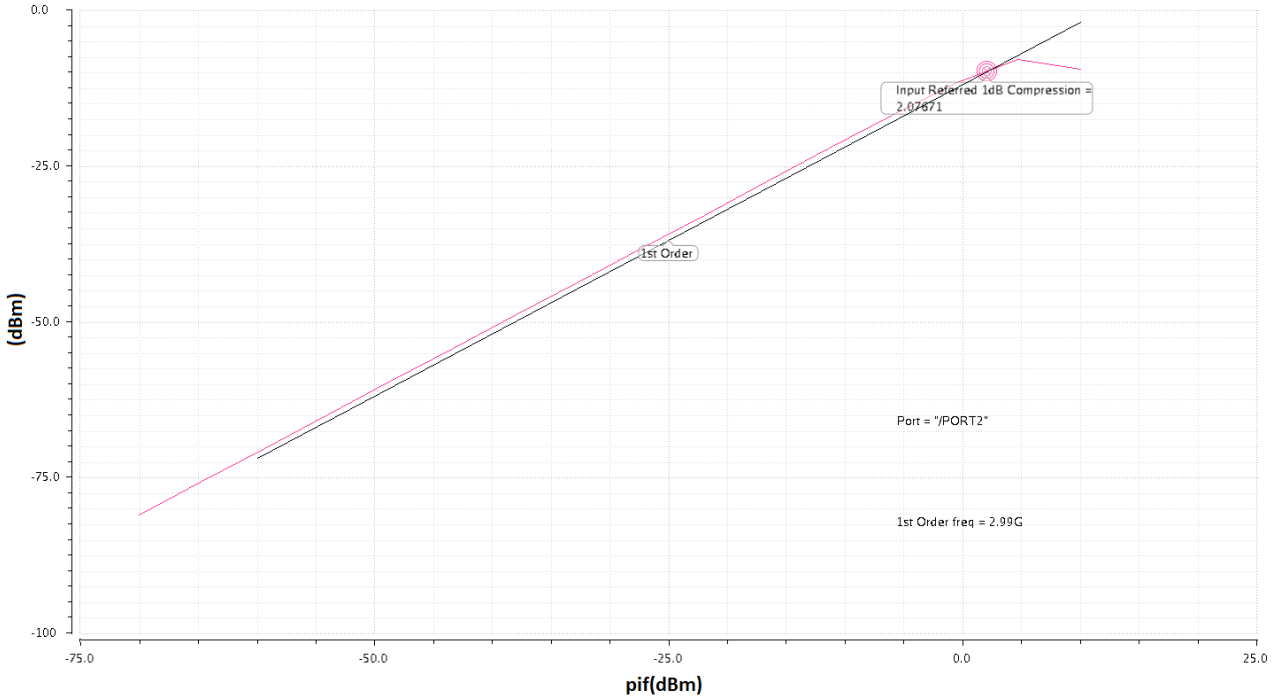


Figure 3.12. P_{1dB} simulation for the first upconverter.

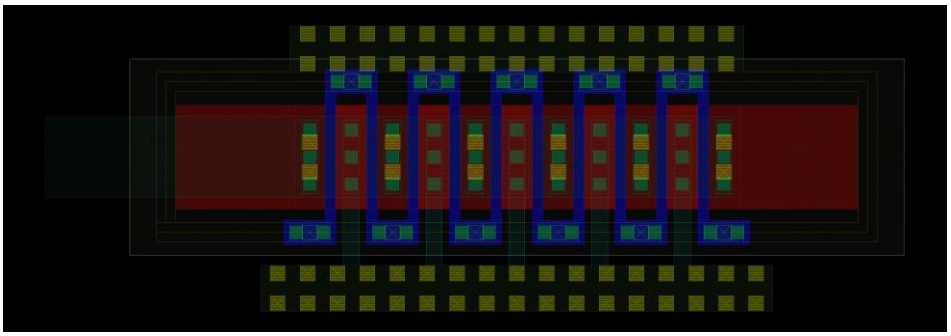
Chapter 4: Layout and Fabrication

This chapter focuses on the layout and the tape-out of the mixer chips. The considerations of doing the RF layout in the BCD process are discussed in details.

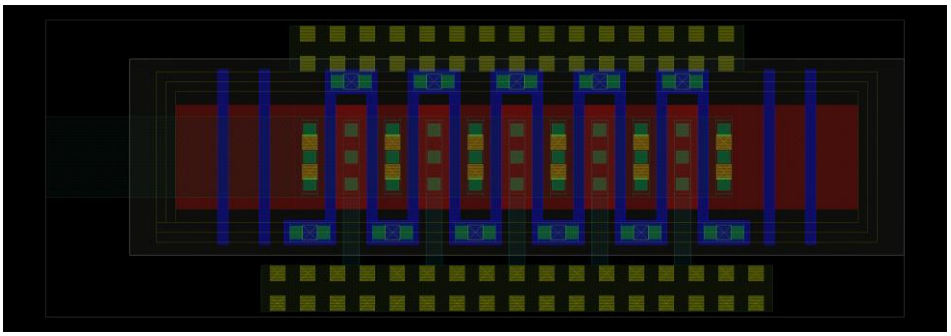
Available Processes

There are various processes available to fabricate the designed RF chips. A convenient option is the RF CMOS process where the model of the RF MOS transistors as available in addition to the normal MOSFET. There are three major differences between an RFMOS and a normal MOS as follows [9, 11]:

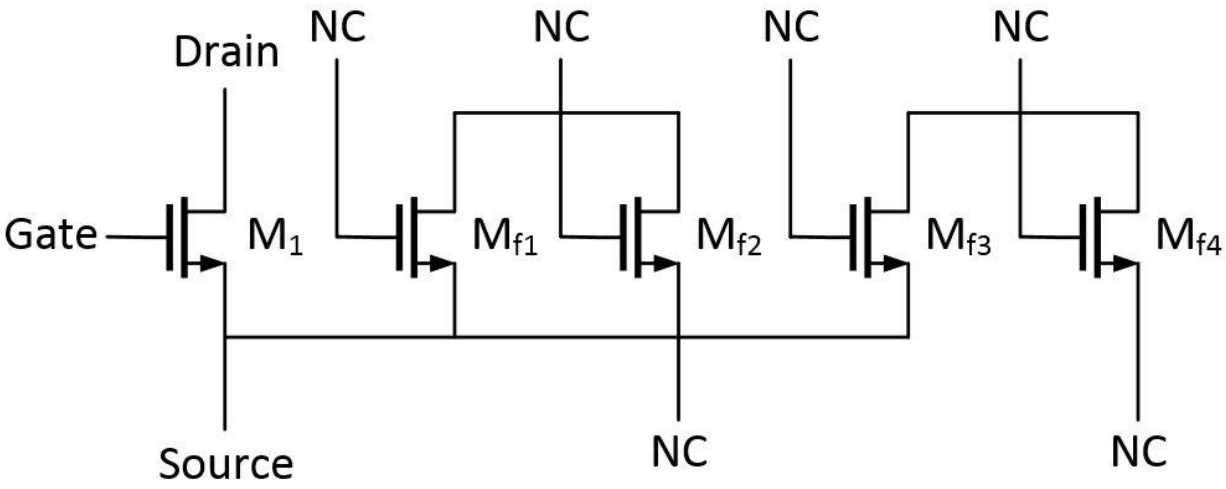
1. Dummy Fingers: Using fingers instead of a wide transistor for large W/L ratios has the benefits of lowering the drain junction capacitance as well as lowering the gate resistance. One problem with using the fingers is that the environmental effect is different for the middle fingers and side fingers. This fact can make the transistor model inaccurate and generate mismatch between the fingers. In order to provide more symmetry, additional dummy fingers are added at each side of the transistor so that the performance of the side fingers will be similar to the middle fingers. Fig. 4.1(a) and Fig. 4.1(b) show an NMOS transistor without and with four dummy fingers, respectively. Fig 4.1(c) demonstrates the equivalent schematic of the transistor with two dummy fingers at each side.



(a)



(b)



(c)

Figure 4.1. NMOS transistor (a) layout without dummy fingers (b) layout with dummy fingers (c) schematic equivalent for (b).

2. Guard Ring: Adding a guard ring around the MOSFET provides isolation for the substrate noise and prevents latch-up in mixed-signal circuits. In this process, the guard ring is implemented by putting a P+ ring around each NMOS transistor and an N+ ring around each PMOS transistor, thus connecting the ring to ground or VDD, respectively.

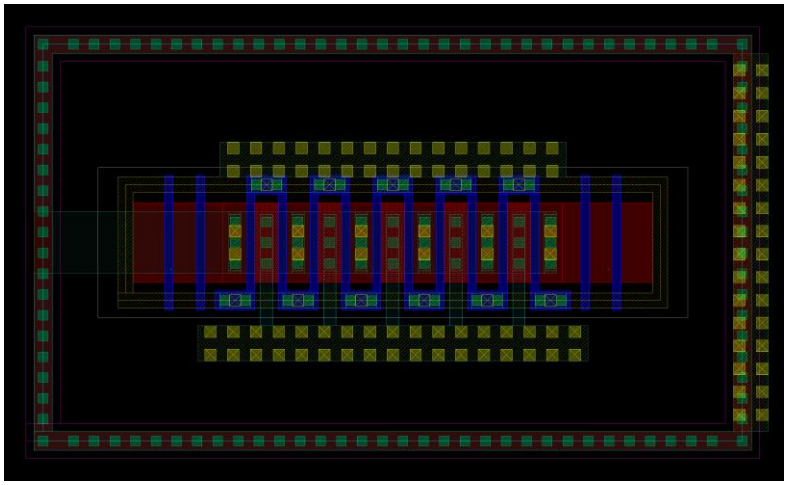


Figure 4.2. NMOS Transistor with P+ guard ring.

3. Deep N-Well: Implementing NMOS transistors on an N+ region also isolates its p-substrate from other transistors substrates (PMOS substrate is already isolated from other PMOS transistors). By using deep n-well different transistors can have different substrate voltages. Fig. 4.3 shows the layout of a NMOS with P+ guard ring and deep n-well.

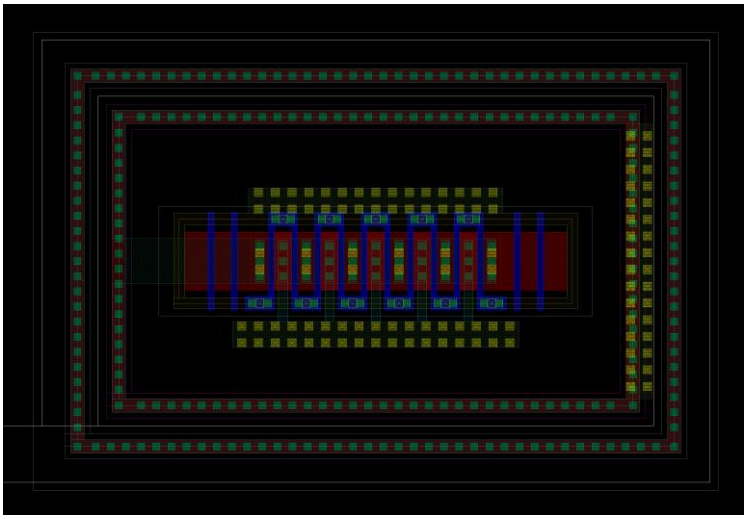


Figure 4.3. NMOS Transistor with P+ guard ring and DNW.

The BCD process, which is used for this design, provides CMOS, Bipolar, and DMOS (high voltage MOS). The BCD process, although suitable for PA design, does not support the deep n-well option, not does it provide RF models for the transistors. Since the up/down converter in this thesis will be implemented with a PA on a single die in future, the BCD process is chosen. Table 4.1 compares the processes, their relative prices and applications. As mentioned, BCD process in more expensive due to the extra masks and process steps to generate the high voltage MOS. In particular, there are two poly layers available. The first one is allocated specifically to implement the high voltage devices, and the second poly layer is used to implement the low voltage MOS.

Table 4.1 Fabrication Process Comparison.

Process	Available Technology	Price	Application Example
CMOS	CMOS	Low	Low Power Design, Digital IC
BiCMOS	CMOS/Bipolar	Medium	RF IC, radar, High SNR circuits
BCD	CMOS/DMOS/Bipolar	High	Envelope amplifier, PA

Using the BCD process for low-voltage applications adds a few design rules to the layout criteria, the most important of which is that low-voltage devices should be isolated from high-voltage devices by high-voltage diodes. This separation can be either for each individual device or for the whole chip. In the former case HV isolation ring is used for the entire chip, with a contiguous p-substrate. Later, it will be shown that low voltage transistors are used to provide ESD protection in the pad ring. Thus, the latter option is used.

Passive Components

Resistors

There are four different types of resistors available in the process being used: poly resistors, diffusion resistors, N-well resistors, and metal resistors. Choosing the right resistor type can help in improving the performance of the circuit. Table 4.2 provides a comparison among them. For the diffusion resistors, the doping process does not affect the flatness of the substrate. Moreover, the resistors are surrounded by oxide with does not conduct heat well. In cases where high accuracy is needed over PVT, poly resistors are preferred [13, 14].

Table 4.2 Resistor categories and their advantages.

Type	Poly (without Salicide)	Poly (with Salicide)	Diffusion (without Salicide)	Diffusion (with Salicide)	N-Well	Metal (M1:M5)
Resistive Value per Square (Ω)	n-type 292 / p-type 311	7.89 / 7/9	59 / 133	6.82 / 7.76	927	0.078
Advantages	High Accuracy, low temperature coefficient		Flatness of the substrate, low susceptibility to overheating		Providing large resistance	Providing very low resistance

Capacitors

There are two capacitor types available: Metal-Insulator-Metal (MIM) cap and PMOS cap. A MIM cap is implemented using metal 5 and metal 6 and adding the CTM layer in between to reduce the space between the two plates, as shown in Fig. 4.4. Such capacitors are used where high accuracy is needed. A PMOS cap is simply the capacitor between the gate and substrate of a PMOS transistor. This capacitor provides more capacitance per unit area, but it is nonlinear.

Thus it is suitable for the condition when the capacitance accuracy is not of great importance, such as decoupling capacitors for VDD.

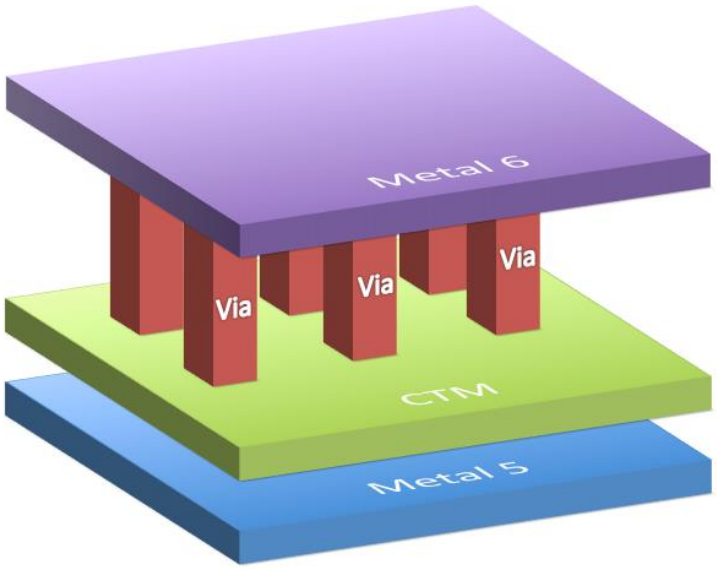


Figure 4.4. Mimcap structure.

Inductors

High-performance inductors are not available in the BCD process. In most RF CMOS processes, the top metal thickness is increased to reduce its loss, and as a result it provides higher quality factor for the on-chip inductors. However, in the BCD process, metal 6 thicknesses remains the same as normal CMOS technologies.

Routing Tips

There are a number of concerns for the RF routing provided below:

1. The first issue is to choose the best metal layer for RF routing. Usually, the thickness of the metal layers increases as moving to the top layer. Consequently, the top layer provides less loss. Although, in order to go to this layer for routing, a number of vias are

needed since resistors and transistors pins exist in lower metal layers. Using a number of vias in parallel can help reducing their total equivalent resistance. Another important factor is that by increasing the thickness of the metal, its side fringing capacitor value also increases. Considering this fact, metal 4 and metal 5 are the best metals for RF Another important issue for the routing is the current-carrying capacity of the routes. The metal routes on each metal layer have a maximum current per width specification (1mA/um for M_1-M_5, 1.6mA/um for M_6) to reduce electromigration. Thus the width of the metal lines carrying high currents should be increased accordingly.

2. When the route widths becomes wider than certain values specified in the documentations (50um here), slots are required in the route for releasing the stress.
3. L and U turns are not recommended for RF routing due to the reflection effects. Instead, routing options in Fig. 4.5 can be used.

Figure 4.5. From left (a) not recommended L (b) recommended L alternative (c) not recommended U (d) recommended U alternative.

4. RF signals should not cross each other on adjacent metal layers. Wherever the crossing is unavoidable, such as in double-balanced mixers with high frequency IF, LO, and RF, the cross-section should be perpendicular to minimize the cross talk. Also it is beneficial to estimate the cross-talk by calculating the added capacitance between the two routes.

5. For double-balanced mixers, layout symmetry is very important. Asymmetry in a pair of devices can cause mismatch, which will result in LO-RF feedthrough (in the upconverter). To reduce this feedthough, the mixer transistor pair should have the same orientation, be close to each other as much as possible, and have similar routings. A picture of the layout of the mixer is shown in Fig. 4.6.

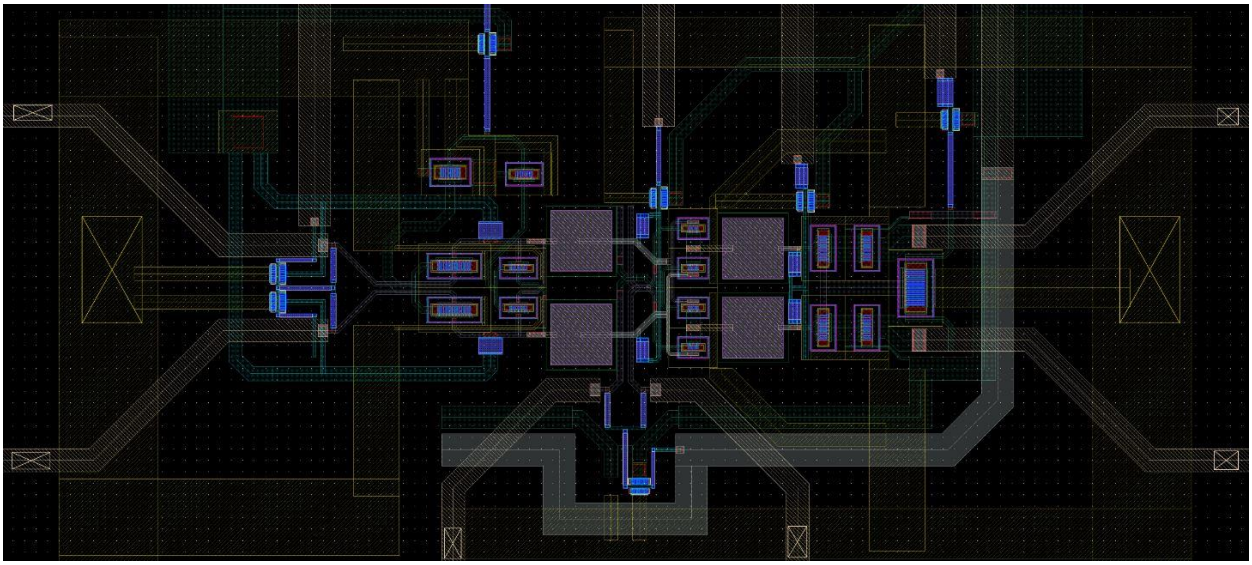
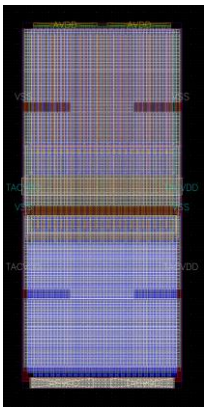
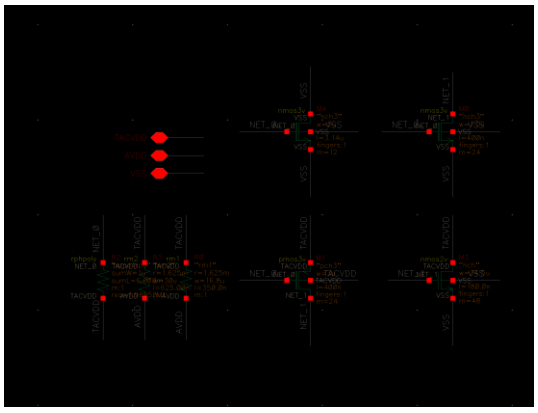
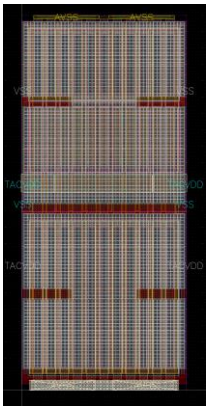
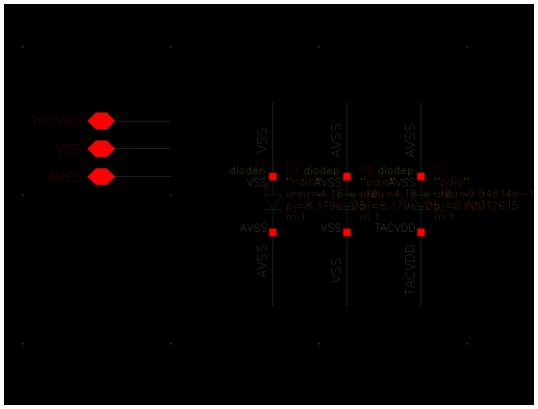
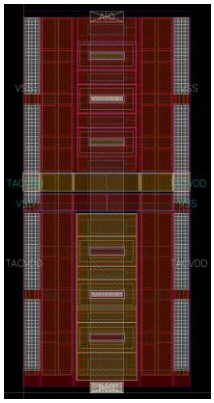
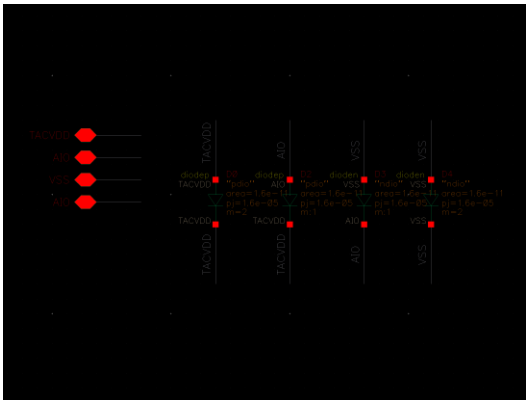


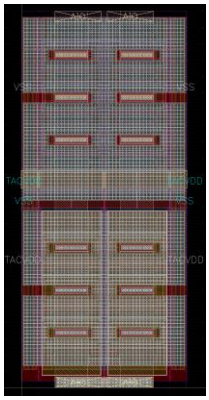
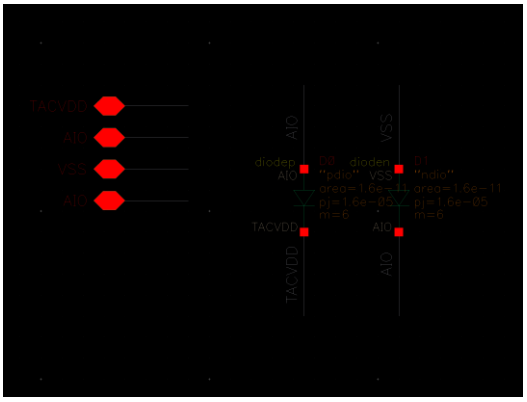
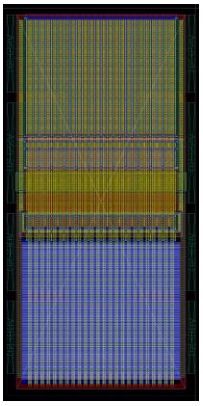
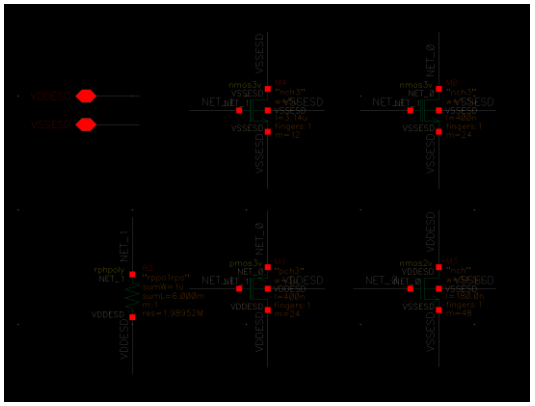
Figure 4.6. Mixer layout.

Pad Ring, ESD Protection, and Bond Pads

The pad ring is needed to provide ESD protection for the chip. It is designed with the help of RF CMOS pad libraries. Table 4.3 provides information regarding the main pad cells, their equivalent circuit, and their purpose. In addition to this table, filter pads and cut pads are used.

Table 4.3 Pads types and their descriptions.

Pad Name	Layout	Equivalent Circuit	Purpose
PVDD3AC			V_{DD} pad, power source for both analog macro and analog I/O power rail, provides ESD protection
PVSS3AC			Ground pad, ground for both analog macro and analog I/O power rail, provides ESD protection
PDB1AC			Analog Pad, optimized for minimum input capacitance, ~100fF, used for RF pads

PDB3AC			Analog pad, optimized for both ESD robustness and EM (current) capacity, ~600fF, used for bias pads
PCLAMP			Core-clamp cell, provides ESD robustness in the core-voltage analog domain

In addition to the ESD protection provided by the pads, secondary ESD is required if a MOS gate or drain is to be connected to a pad. This extra protection can be applied using the circuit in Fig. 4.7.

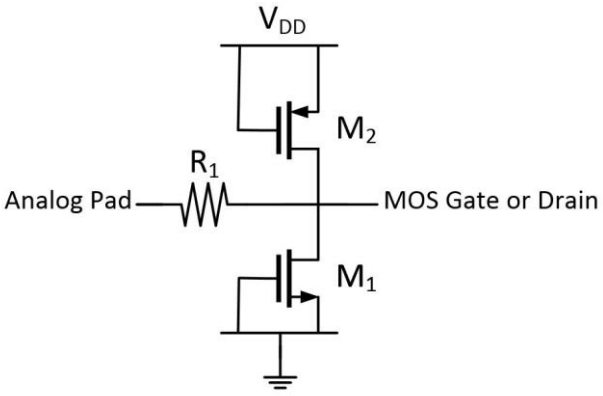


Figure 4.7. Secondary ESD protection for accessing MOS gate or drain off-chip.

Due to the large size of the I/O ring, compared to analog core, reducing the chip area is pad-limited other than core-limited. The extra area in the I/O ring can be used for V_{DD} decoupling capacitors. Although a PMOS cap has more capacitance per unit area, a MIM cap is used to satisfy the CTM layer minimum coverage area requirement.

Each of the pads in Table 4.3 are compatible a few bond pads. There are different kinds of bond pads available based on their structures, such as OBV (one big via) and TRL (triangle) structures. The RF bond pads are built only using metal 5 and metal 6 to reduce their capacitance. Low-frequency bond pads, V_{DD}, and Ground bond pads are built using M1-M6. For ultra-compact layouts CUP (circuit under pad) method is used. A picture of the I/O ring with 16 bond pads is provided in Fig. 4.8.

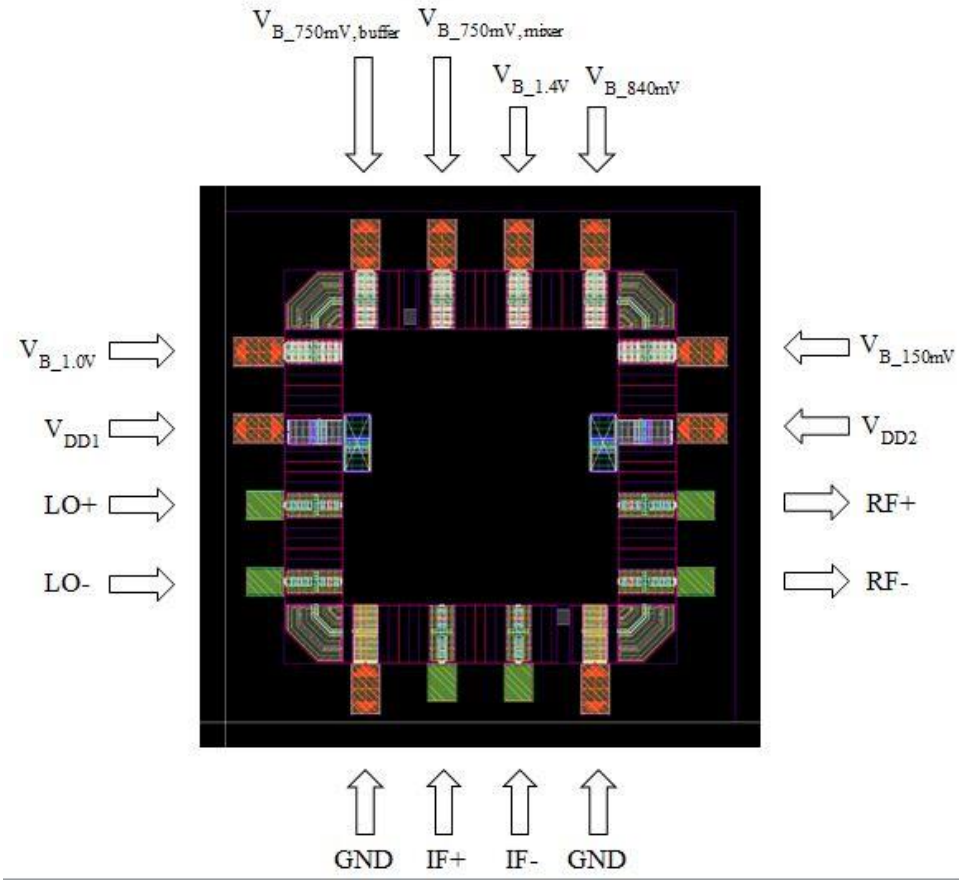


Figure 4.8. I/O Pad and bond pads

Pre Tape-Out Steps

The following steps are passed before sending the chip for tape-out.

1. DRC (Design rule check)

   This step is necessary to make sure all the process rules are satisfied. In addition to the rules mentioned in this chapter, there are extra rules regarding the minimum coverage area for each layer, which need to be satisfied. Fill scripts are used for this purpose. However, for RF chips, one should make sure that the RF routes remain untouched after filling the chip with dummy material. Fill errors are usually debugged after passing DRC (ignoring area coverage errors), LVS, and ERC.

2. LVS (Layout vs Schematic)

   LVS should be run to make sure the schematic matches the layout. The LVS run compares the layer stacks and determines the generated devices. Then it compares them with the schematic.

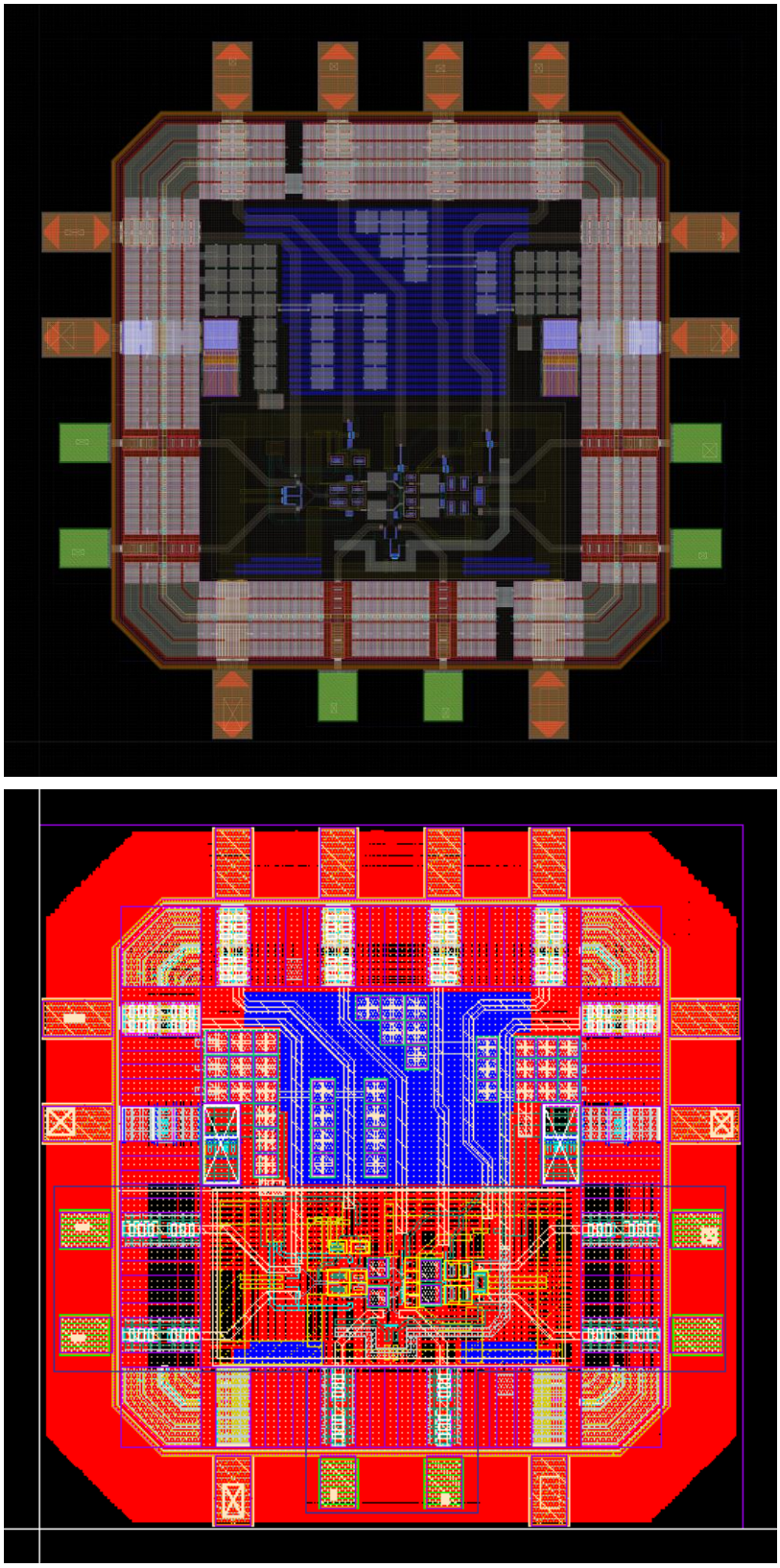
3. ERC (Electrical Rule Check)

   This step determines if there are any electrical errors in the layout, such as antenna effect, shorts, floating metal or poly, latch-up, etc.

4. Extraction (Optional)

   The “Extraction” step generates an equivalent schematic for the layout. There are different kinds of extractions available, such as R extraction (only considers parasitic resistors), C extraction (only considers parasitic resistors), or RC extraction. Running this step is recommended to make sure there is no parasitic element which will affect the chip performance.

The layout of the entire chip are provided in Fig. 4.9.

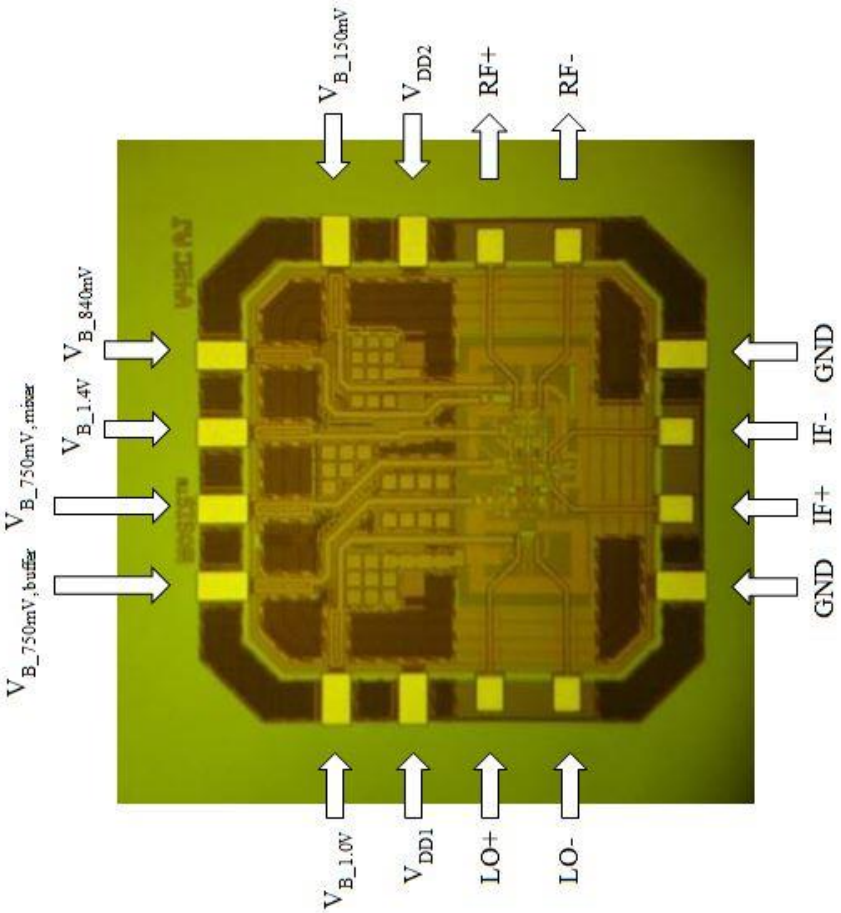


(a)

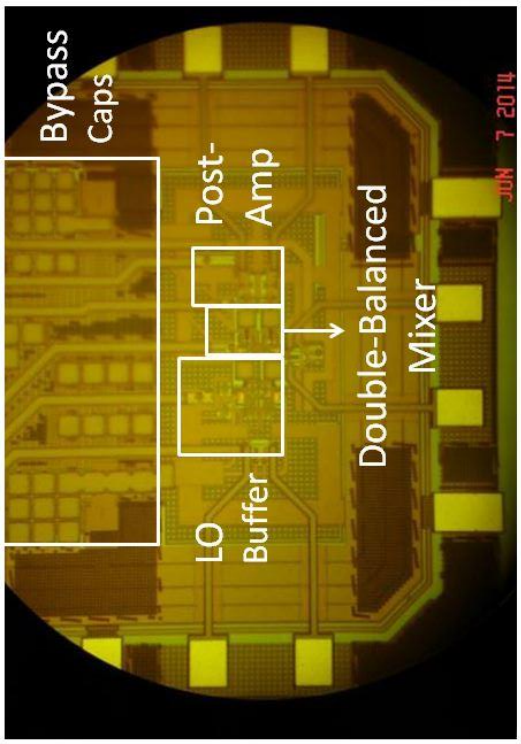
(b)

Figure 4.9. Pictures of the entire chip (a) before running the Fill scripts (b) after running the Fill scripts.

Two photos of the fabricated chips are provided in Fig. 4.10.



(a)



(b)

Figure 4.10. Photos of the fabricated chips (a) entire chip (b) core circuit

Chapter 5: PCB Design, Test, and Measurements

This chapter is focused on the printed circuit board (PCB) design, to be used in the test and evaluation of the mixer chips. In particular, the required steps after the tape-out to test the chips are described. In the board design section, the general PCB design is discussed as well as additional concerns regarding RF PCB layout. In the second section, the performed tests and the results are provided.

Board Design

To design a PCB for an RF chip, a number of factors, listed below, should be considered. Since the chip described here is going to be bonded directly to the board, with no package, other criteria regarding connection of bond wires and chip placement are also considered:

1. Dielectric Material: The material of the dielectric should be chosen based on the maximum frequencies of the signals on the board. Good dielectric materials provide low loss at high frequency and constant relative dielectric (ε_r) over a wide frequency range. Two materials were considered for this thesis: FR4 and Rogers 4003. The loss vs. frequency plots of both materials are provided in Fig. 5.1. Due to the increase in loss, FR4 is appropriate only for frequencies up to 2-3 GHz whereas Rogers 4003 is suitable for the entire frequency range of this chip, up to 5.7 GHz. However, if the second LO route is short so that the 0.6dB/inch loss at 5.7GHz is tolerable, FR4 can be used. Using FR4 reduces the cost of the board. However, in this thesis, in order to provide accurate measurements, Rogers 4003 is used [15].

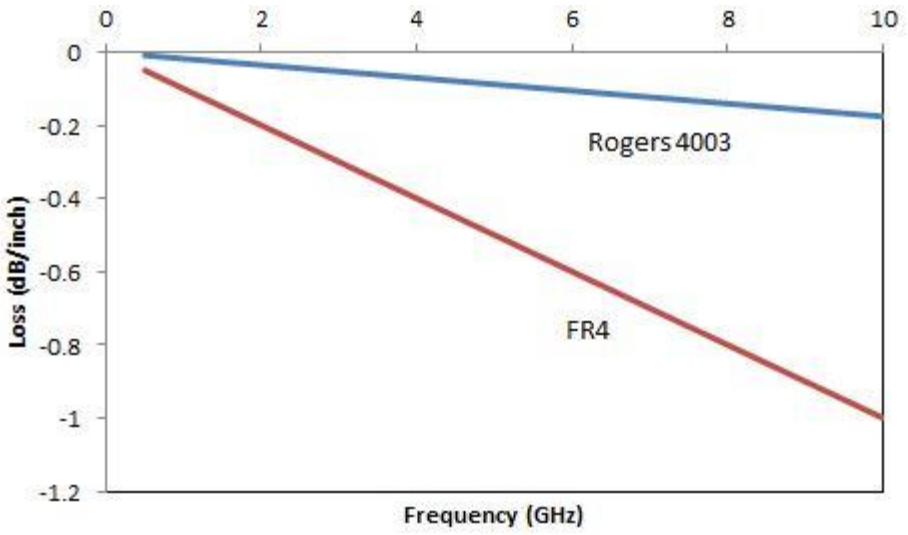


Figure 5.1. Loss vs. frequency curves for Rogers4003-30mil and high performance FR4-20mil.

2. Transmission Line and Matching: At high frequencies, impedance matching becomes quite important, as it results in maximum power transfer as well as device protection, i.e. no reflected power. There are various transmission line methods to provide such matching. The two most common methods are microstrip line and grounded coplanar wave guild (GCPW). An illustration of each method is provided in Fig. 5.2. GCPW is a more complex design, but it helps to reduce the size of the board, due to its thinner traces, and can provide a more robust matching since it does not suffer from any parasitic components in the top ground plane. This method is chosen for RF routing. Generally, the PCB manufacturer requires a minimum routing width of 4-5mil. Based on the Rogers Corporation Impedance Calculator [16], for Rogers 4003, 32mil thickness, 30mil conductor width, and 4mil ground space a 50Ω matching can be achieved [17, 18. 19].

3. Ground Plate and Guard Ring: In RF boards, in order to protect the on board signal from external unwanted signals, a grounded guard ring is usually placed around the board in

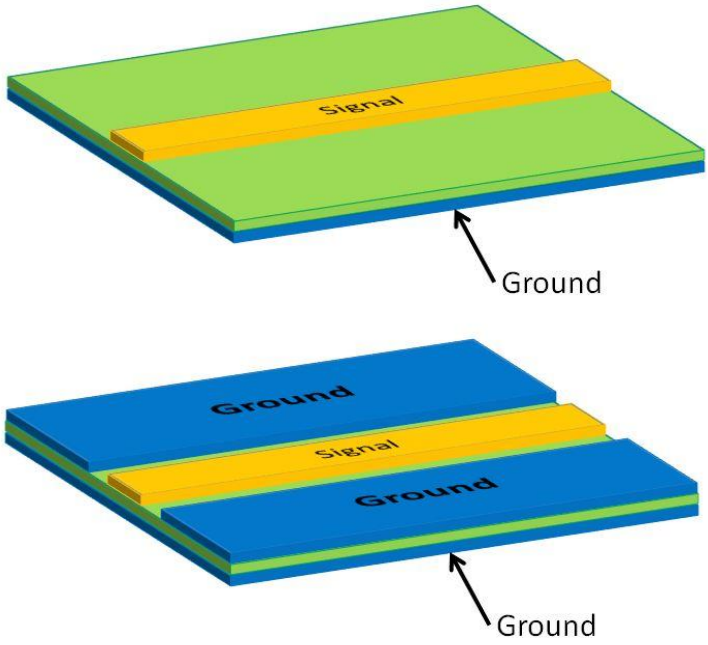


Figure 5.2. Microstrip line (top) and coplanar waveguide (bottom) structures.

all layers, all connected together using vias, as shown in Fig. 5.3. Also, in order to improve the ground performance, additional vias are placed near the ground pin of the components. To improve the performance of the chip, it is beneficial to make sure that the ground plates will isolate the various RF paths.

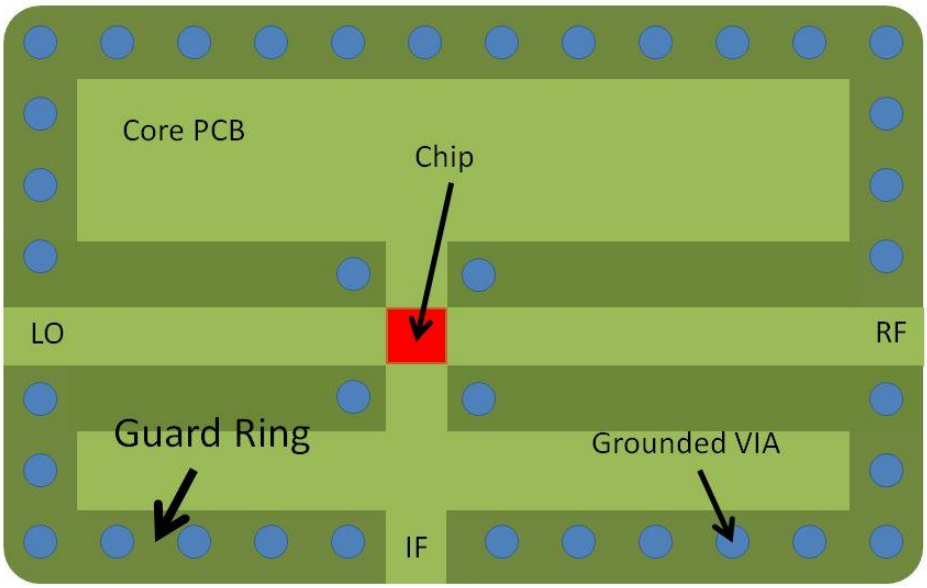


Figure 5.3. Grounded guard ring and RF signal isolation.

4. Chip Placement and Bondwiring: The first fact to consider is to decide whether the die will be place on top of the PCB or cavity die bonding method will be used. The second method has two major benefits:
   a. The bondwires are more horizontal. As a result, their lengths are smaller, they are straighter, and their effect on the matching is minimized.
   b. Placing the chip inside the PCB is provides more protection during board assembly.

   However, for the sake of simplicity and cost reduction, the first method is chosen.

   There are various methods to attach the die to the PCB. Two of the common methods are using either solder paste, or silver epoxy. The latter provides very firm connection between the PCB and the board, and it allows connection of the ground pads to the middle path (under the chip) since it does not spread. But one disadvantage is the difficulty of replacing the chip. On the other hand, solder paste provides a weaker thermal and electrical connection to the ground, but allows for easily replacement of the die. Based on the above discussion, it was decided to use silver epoxy.

   In order to be able to bond the chip pads to PCB, the material of the bondwire, chip pad, and PCB pad must be compatible. Gold bondwire and gold pads are chosen accordingly. Since a soldered pad cannot be connected to a bondwire, separating the soldered pads and bondwire pads is strongly recommended. A picture of the chip that has been placed and connected to bond wires is shown in Fig. 5.4.

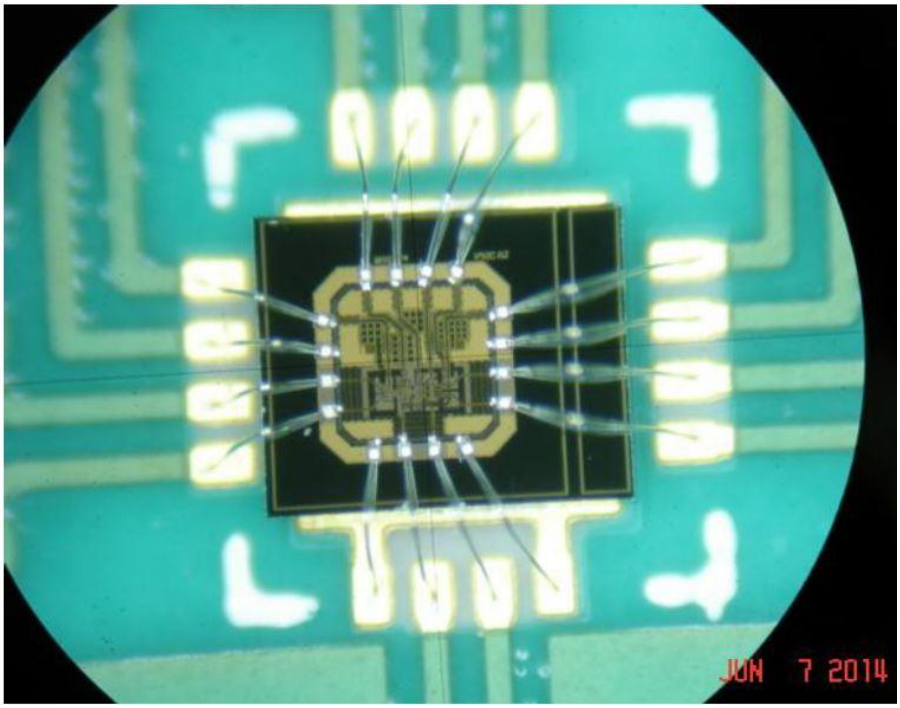


Figure 5.4. Attached and bondwired die to the PCB.

5. RF Routing: Normally only the top layer is used for routing of RF signals due to the following reasons:
    a. The chip pads are going to be bondwired and surface mount elements are going to be soldered to the top layer. Thus, routing in other layers requires using vias which adds to the routes impedance.
    b. Using only the top layer for routing results in using only one high-performance dielectric material to implement the transmission lines. The RF routes should be as straight as possible to avoid reflection, and L-shape and U-shape routings should be avoided in favor of 45° routes.
6. For each applied DC voltage, a decoupling capacitor to ground is recommended, with a via near its ground. In case noise is observed on the DC voltages during the tests the capacitor value can be adjusted to improve the noise performance.

7. High-frequency baluns are used as single-to-differential and differential-to-single converters. These baluns structures usually do not provide decoupling. Thus decoupling capacitors must be placed in the signal paths.

A picture of the design PCB is shown in Fig. 5.5. The wires on the top are connected to the bias voltages. For testing purposes the matching network is shorted so that the output resistance of the chip, which is actually a differential cascode post-amp stage, is 50Ω instead of 2×200Ω = 400Ω. This fact creates a 1/8 offset factor in the voltage gain, or 18.1dB offset.

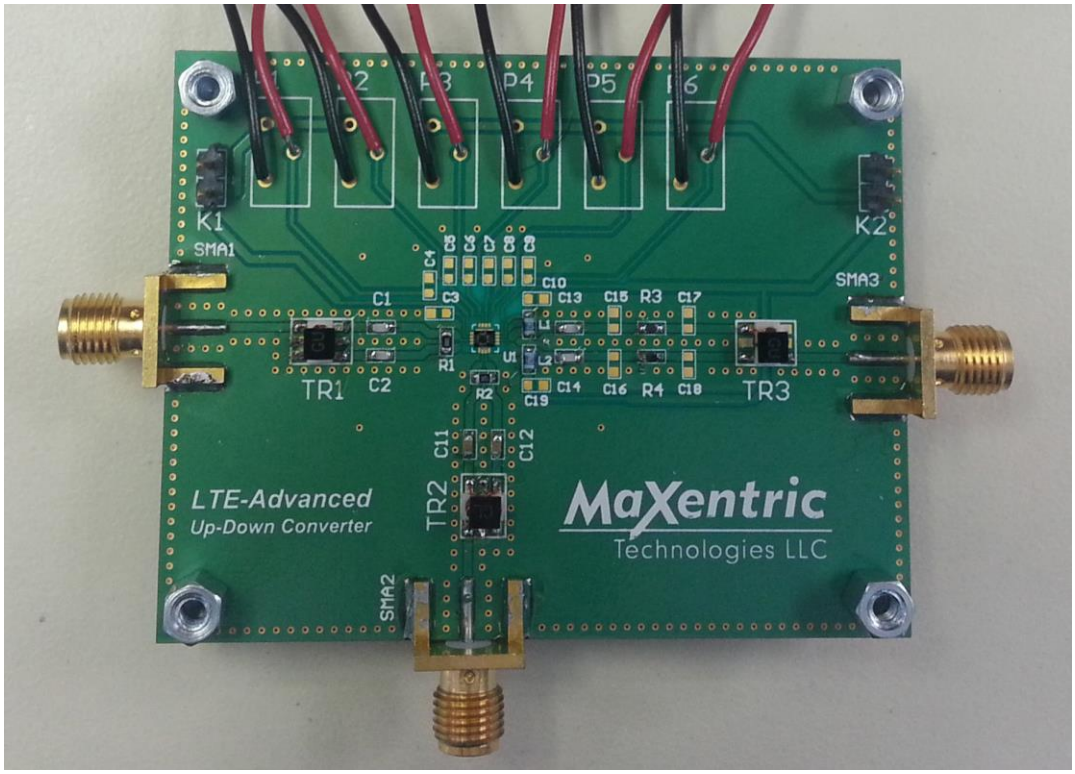
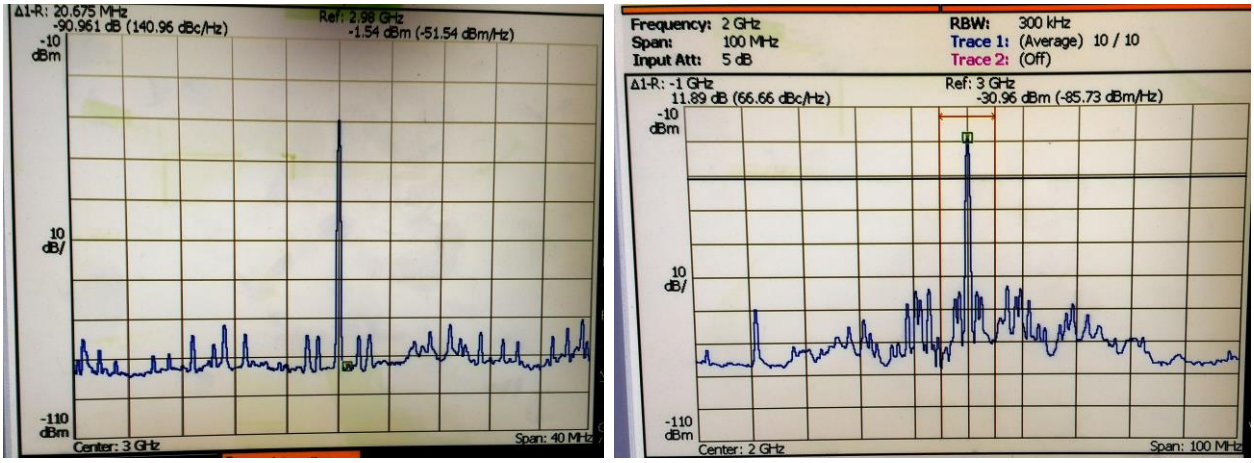


Figure 5.5. Testing PCB for the first upconverter.

Measurement Results

Different tests are performed to verify the performance of the chip. The main tests and the result are provided in this session.

Single Tone: To measure the conversion gain of the first upconverter, a single tone at 75MHz and a single LO tone at 3.075GHz are applied with the output power measured at 3GHz. The measured spectrum is provided in Fig. 5.6(a) using the Tektronix RSA 3408A spectrum analyzer. The output power is -11.67dBm (after applying 18.1dB offset) which is about 12dB lower than the value predicted by the simulations. For the second upconverter, the same measurement was done with the IF at 3 GHz and the LO at 5 GHz. The measured output power is -19.05 dBm. Thus in case the output is matched to 400Ω, the gain is about -1dBm, which is 4dB lower than simulation. The result is shown in Fig. 5.6(b). The gain error in both tests could be due to the loss in the baluns, the board, the coaxial wire, etc. Another important fact is that spurs exist at -42 dBc. This could be due to blockers and interference or noise. It is beneficial to mention that these spurs exist at -72dBm. Therefore, in order to verify the source of the spurs, the circuit should be modified for a higher gain.



(a) (b)

Figure 5.6. Single tone test (a) first upconverter (b) second upconverter.

Gain Flatness: Unlike the first upconverter, the second upconverter operates with a variable LO. Fig. 5.7 shows the measured gain flatness of the second upconverter, demonstrating a gain flatness of 1dB for the RF frequency range of 1GHz – 2.3GHz. The primary cause of this

variation is the non-uniform loss of the baluns; at the low- and high-frequency edges, the baluns exhibit more loss and there is also more variation of trace characteristic impedance. Half of the extra loss at high frequencies is due to the bandwidth of the post-amp being limited to 5.7GHz.

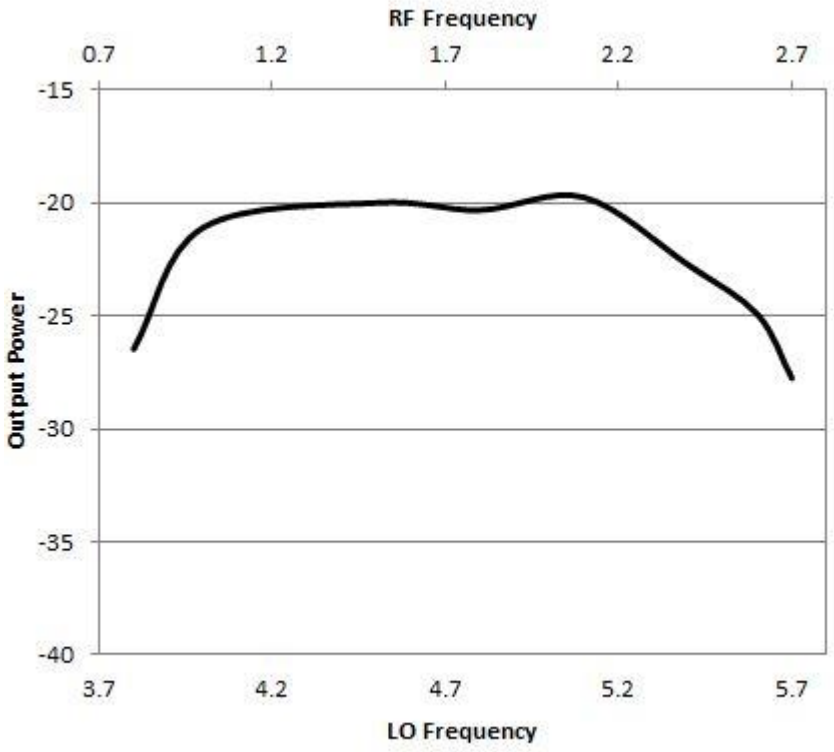


Figure 5.7. Gain flatness of the second upconverter vs LO and RF frequency.

Another useful test is to measure the gain flatness of the first upconverter while changing the IF. For this measurement, a 100 MHz BW, 75 MHz center frequency, 64-tone signal is applied as the IF while the LO frequency is set to 3.075 GHz. The output spectrum is shown in Fig. 5.8. The gain flatness is 3 dB for the entire 100 MHz bandwidth and 2 dB at a 20 MHz bandwidth centered at 3GHz. It can be seen that there is a 1-2dB increase in output power at higher frequencies. This may be caused by some of the bypass capacitors (either on- or off-chip) not being large enough and thus having a small impact on the response at low frequencies. The loss

variation of the balun over frequency could also be a factor. This measurement is also done by using the Tektronix spectrum analyzer.

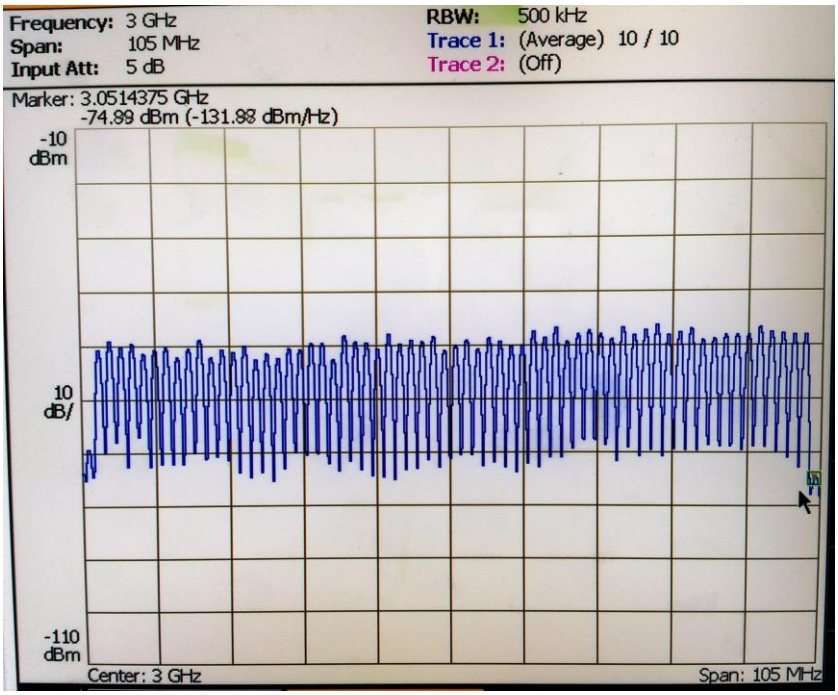


Figure 5.8. Gain flatness of the first upconverter vs IF frequency.

Linearity: To test the linearity, the input power is swept and P_{1dB} is measured as shown in Figs. 5.9 and 5.10 for the first and second upconverters with their P_{1dB} measured to be 0.0 and -1.8dBm, respectively. The following calculation can be made to calculate the IIP3 and OIP3 where it is assumed that the main source of the nonlinearity is the mixer and the post amp is linear [6].

For the first upconverter: $IIP3 \approx P1dB + 9.6dB \Rightarrow IIP3 \approx 9.6dBm$ (5.1)

$$OIP3 \approx f(IIP3) + 20\log\left(\frac{400\Omega}{50\Omega}\right) \Rightarrow OIP3 \approx --13.9dBm \quad (5.2)$$

For the second upconverter: $IIP3 \approx P1dB + 9.6dB \Rightarrow IIP3 \approx 7.8dBm$ (5.1)

$$OIP3 \approx f(IIP3) \Rightarrow OIP3 \approx -23dBm \quad (5.2)$$

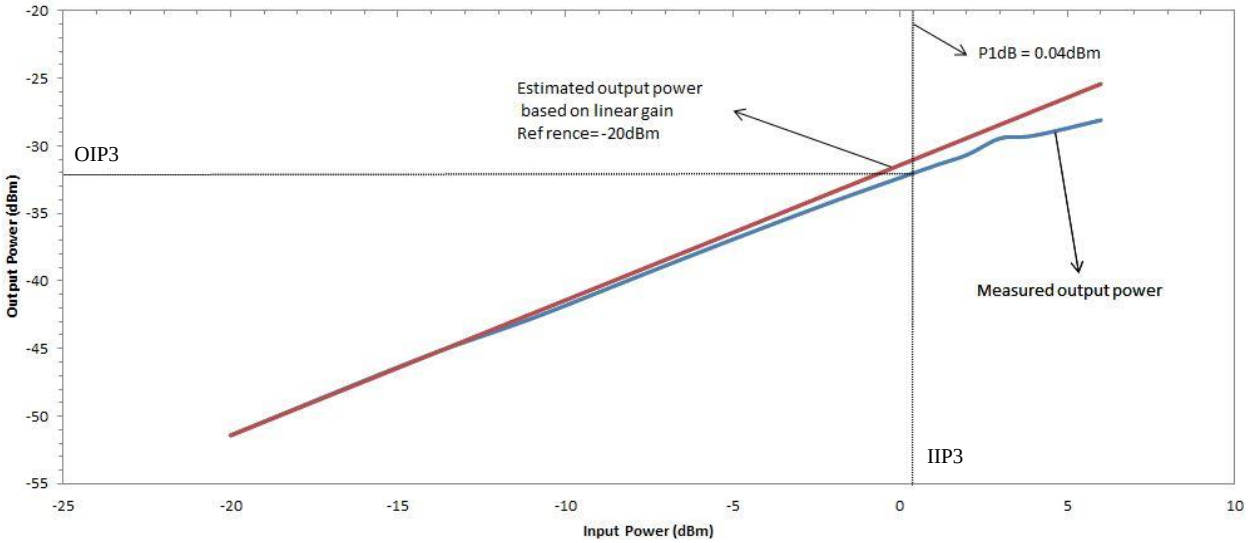


Figure 5.9. P_{1dB} measurement of the first upconverter.

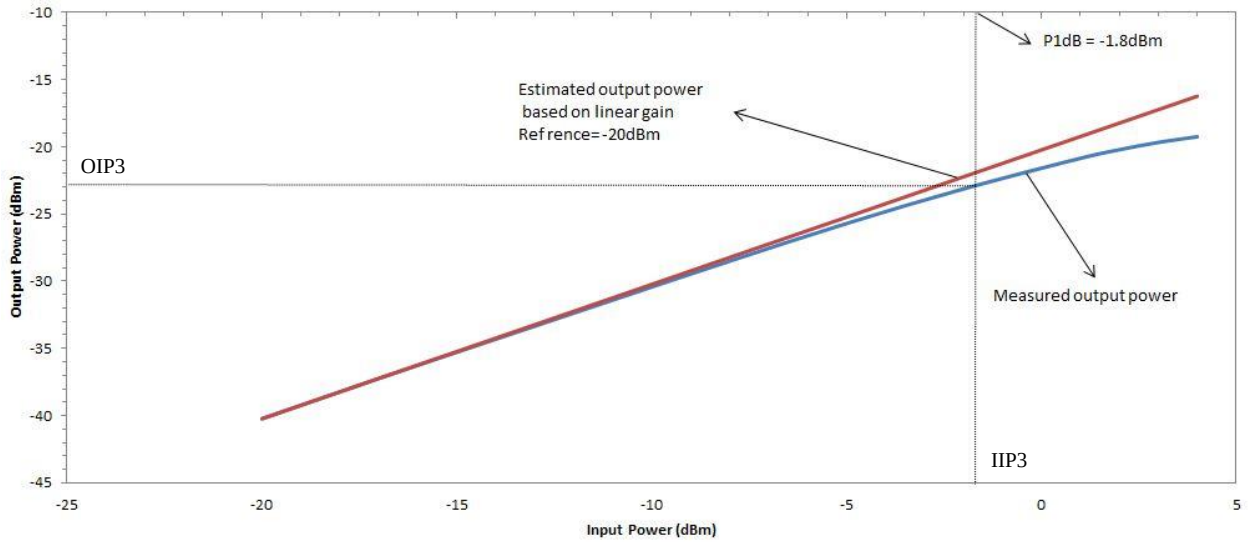


Figure 5.10. P_{1dB} measurement of the second upconverter.

It is beneficial to mention that OIP3 calculations are not accurate due to the existing error in the gain. According to the source of such error, the OIP3 calculation error is somewhere between 0dB and 12dB/4dB for the first/second upconverter, respectively. However, the IIP3 calculations based on P_{1dB} measurement provide close results to the simulations.

Chapter 6: Conclusion

This thesis has described a new system for an LTE-A up/down converter and implemented it in a 0.18um BCD process. The implementation includes the design , fabrication, and test of the converter chips mounted on RF PCB boards. The proposed system solves the problem of the LO feedthrough of the passive mixers and based on its performance could be used for future heterodyne microcell designs of an LTE/LTE-A transmitter. The system is designed for a 100 MHz IF bandwidth and 0.7-2.7 GHz RF carrier frequency. Measured results of the P_{1dB} for the first and second upconverters give 0 dBm and -1.8 dBm, respectively.

Chapter 1 gave an introduction to the thesis and discussed the applications of the circuit blocks being designed. In Chapter 2, a novel system for an LTE-A transmitter was presented. The main idea is to upconvert the IF signal to an out-of-band frequency, higher than the band of interest, then mix the signal with a high-side injection LO to convert it back within the band of interest. In this system, both LO frequencies are located out-of-band and the LO feedthrough can be canceled out conveniently through a band-pass filter. Chapter 3 discussed implementation of the circuit-level design and simulations. Chapter 4 discussed the challenges of doing the layout of an RF chip, particularly the passive mixers. Chapter 5 explored the PCB design and provided the test and evaluation results for the fabricated chips and PCB.

For future studies and research in this domain, two paths are suggested as follows:

1. Implement the system with single-sideband double balanced passive mixers to cancel the image signals and relax the specifications of the bandpass filter.
2. Implement a sharp BPF filter in the same process so that the whole system can be implemented into a single chip.

The writer of this thesis would like to take the opportunity again to thank Professor Michael Green, Isabelle Telliez, and all the other people in University of California, Irvine and MaXentric Technologies, LLC who helped him in accomplishing the goals of this thesis.

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