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Low-Cost and Low-Topography Fabrication of Multilayer Interconnections for Microfluidic Devices

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Abstract

Multilayer interconnections are needed for microdevices with a large number of independent electrodes. A multi-level photolithographic process is commonly employed to provide multilayer interconnections in integrated circuit (IC) devices, but it is often too expensive for large-area or disposable devices frequently needed for microfluidics. The printed circuit board (PCB) can provide multilayer interconnection at low cost, but its rough topography poses a challenge for small droplets to slide over. Here we report a low-cost fabrication of low-topography multilayer interconnects by selective and controlled anodization of thin-film metal layers. The process utilizes anodization of metal (tantalum in this paper) or, more specifically, repetitions of a partial anodization to form insulation layers between conductive layers and a full anodization to form isolating regions between electrodes, replacing the usual process of depositing, planarizing, and etching insulation layers. After verifying the electric connections and insulations as intended, the developed method is applied to electrowetting-on-dielectric (EWOD), whose complex microfluidic products are currently built on PCB or thin-film transistor (TFT) substrates. To demonstrate the utility, we fabricated a 3 metal-layer EWOD device with steps (surface topography) less than 1 micrometer (vs. > 10 micrometers of PCB EWOD devices) and confirmed basic digital microfluidic operations.

Keywords—Multilayer interconnection, TFT microfluidics, PCB microfluidics, EWOD, electrowetting.

1. Introduction

For many micro electro mechanical systems (MEMS), one needs to address a large number of electrodes independently on a device, requiring multiple layers of interconnecting electrodes. The multi-level lithography of integrated circuits (IC) may be adequate to fabricate most of the conventional MEMS devices [1-3] but not others, such as non-silicon (e.g., glass) substrate, large area (e.g., > 50 mm) devices, or very low cost (e.g., disposable) products. Currently, there is no multi-layer interconnection fabrication method that is both comparable to the IC fabrication in terms of the resulting specifications and economic enough to provide large devices for disposable applications. In this paper, our main interest is for the EWOD-based digital microfluidic devices [4], which are usually large and often made to be optically transparent and disposable. Although most of the academic research can avoid the multi-layer interconnection by designing EWOD devices of single-layer electrodes to satisfy their own specific needs, most commercial devices use multi-layer interconnections to control the many (typically more than 100) electrodes needed for high functionality and throughput in their operations.

Currently there are two types of successfully commercialized EWOD devices with a multi-layer interconnection: one is built on PCB [5], [6] and the other is built on active-matrix TFT plate [7]. The advantage of the PCB type is its low cost, which allows large area and disposable devices. However, the surface topography of a PCB substrate (typically step heights > 20 μm) hinders the droplet translation on such a device. One solution is to planarize the PCB device by polishing its rough surface down, but it is difficult and expensive to polish a large and flexible board evenly [8], [9]. Furthermore, the horizontal gap between copper electrodes on PCB is normally large (e.g., 70 μm), challenging droplet translations between neighboring electrodes. Fortunately, the topography issue can be overcome if the PCB EWOD device is filled with an oil, so that aqueous droplets can slide with little friction [10]. The advantage of the TFT type, called active matrix EWOD (AM-EWOD) devices [11], [12], is its smooth surface as well as high resolution electrodes. However, since the manufacturing process is still complex and expensive, the devices are relatively small, limiting applications and test throughputs (i.e., the number of experiments that can run concurrently). Although not found in commercial devices, similar active-matrix approach was reported earlier for dielectrophoretic (DEP) actuation of droplets on CMOS devices [13], [14].

Considering the limitations of the PCB-EWOD devices and the AM-EWOD devices, one would desire a low-cost method to fabricate EWOD devices with multi-layer interconnection and good planarity. To obtain such a goal, we turn our attention to the anodic process once explored for metallization for multilevel ICs [15]. For our development in this report for EWOD devices, we use tantalum (Ta) for the metal, following Parkes et al. [16]. However, other valve metals (metals with current rectifying properties on which metal oxides can be anodically grown) such as aluminum, titanium, and hafnium can be used instead. The connection lines are formed by depositing a thin film of tantalum and selectively anodizing it into tantalum pentoxide (Ta_2O_5); and the insulations between the metal layers are formed by anodizing only the top half of the tantalum layer into tantalum pentoxide, keeping a good planarity while eliminating the need to deposit and pattern

dielectric layers. In this report, we explore successive repetition of patterned partial and full anodization to obtain multilayer interconnections.

2. Device Fabrication

2.1. Overall procedure

Anodized metal such as tantalum pentoxide is an electrically stable (dielectric strength = 6-7 MV/cm) material with high corrosion resistance that is used in high performance capacitors [17] and microelectronics [18]. The proposed process of multilayer metal interconnections [19] relies on partial anodization of blanket-deposited metal layers to form insulation layers between them and full anodization to form an isolating pattern that defines electrodes. The following three steps are repeated for each level of the interconnections: (1) blanket deposition of a valve metal layer, (2) selective, full oxidation of the metal, using defined photoresist (PR) as the mask and through-metal anodization, and (3) selective, partial oxidation of the metal, using defined PR as the mask and time-controlled anodization. Although other valve metals can be used as well, such as aluminum, in this paper we developed three-level interconnections made of tantalum because of its particular advantage for EWOD devices [16], following the process flow presented in Figure 1.

2.2. Lithographic steps

In Figure 1(a), the first metal layer (indicated as M1) was deposited by sputtering (in Denton Discovery 550 Sputtering System) 250 nm of tantalum on a 0.7 mm-thick, 100 mm-diameter glass wafer (Schott BOROFLOAT®). In Figure 1(b), a 12 µm-thick PR (MicroChemicals AZ4620) was spin-coated and patterned (indicated as PR1) using the first photomask in a contact aligner (Karl Suss MA6). We used transparency photomasks with minimum feature size ~ 10 µm (CAD/Art Services, Inc.), which are normally used for PCB manufacturing, to trade-off device performance for low cost and large area capability. To prevent peeling of the PR during the subsequent anodization step, it was important to ensure good adhesion. Before the PR coating, the substrate was dipped into Piranha solution (2:1 mixture of 96 wt% H_2SO_4 and 30 wt% H_2O_2) quickly (only a few seconds) followed by rinsing in deionized (DI) water and drying on a hot plate (150 °C, 2 min). To prevent any electrochemical reaction (e.g., electrolysis) on the tantalum under the PR during the subsequent anodization, a thick (12 µm) PR was used and hard-baked extensively (30 min on 120 °C hot plate). Slow cool down (turn off the hot plate with the wafer on and wait until room temperature is reached) was preferred to avoid PR cracking. With the patterned PR (indicated as PR1) as an anodization mask, the exposed tantalum was fully anodized to tantalum pentoxide (indicated as Ox1) in 0.01 wt% KI solution using a platinum sheet as the cathode. The bias voltage applied between the anode wafer and the cathode sheet was gradually increased to 300-350 V to obtain full anodization. The full anodization through the entire thickness of the metal layer was critical because this anodized material (i.e., insulator) electrically separates (isolates) all the electrodes within the given conductive layer. This fully anodized isolating pattern (Ox1) defined the conductive pattern made from the first metal layer (M1).

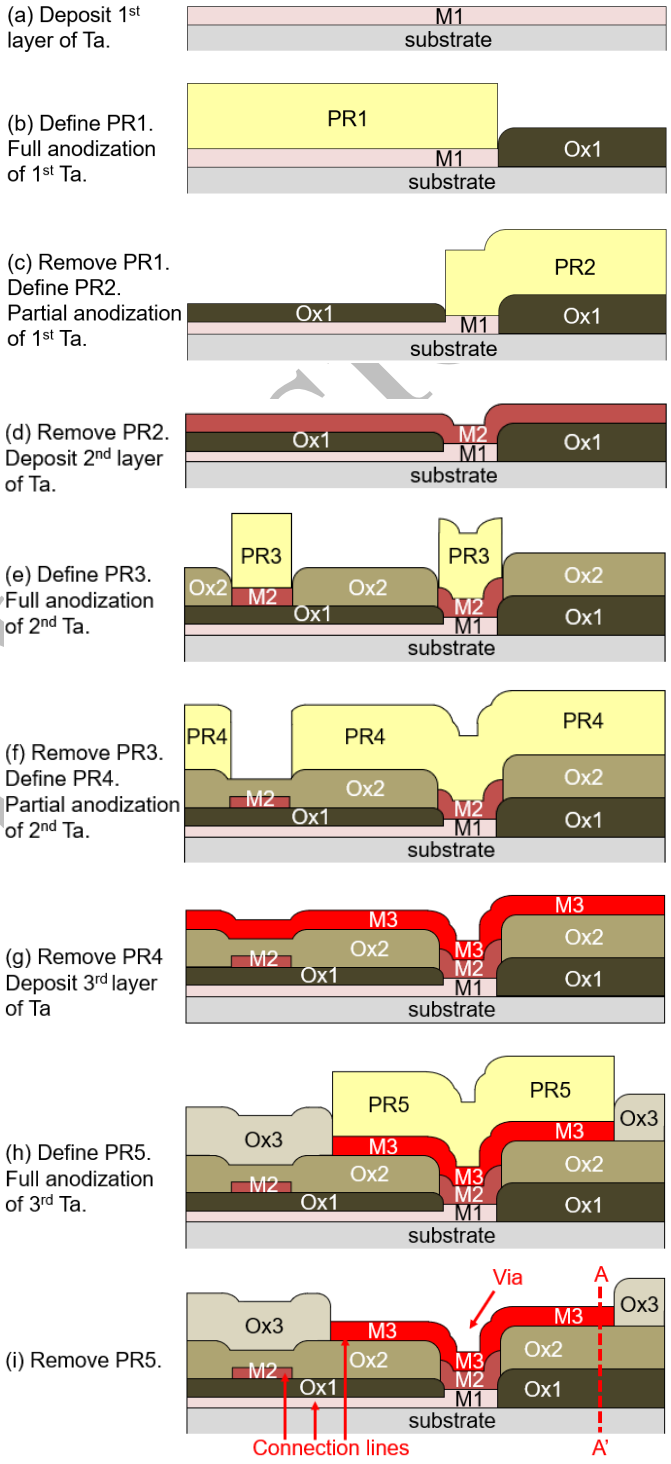

Figure 1. Process flow to fabricate the proposed multilevel interconnections, drawn for three layers. Each anodization step was performed while masked by defined PR. Tantalum was used in the current report for the metal layers. M1: first Ta layer; M2: second Ta layer; M3: third Ta layer; Ox1: first Ta_2O_5 layer; Ox2: second Ta_2O_5 layer; Ox3: third Ta_2O_5 layer. Drawn with exaggerated topography for clarity.

In Figure 1(c), the existing PR (PR1) was removed, and another 12 µm-thick PR was spin-coated and defined (indicated as PR2) using the second photomask, following the same PR preparation as above. This time, the exposed tantalum (M1) was partially anodized using 100 V to grow an insulation layer on top (indicated as Ox1 on M1). The 100 V voltage was applied for 1 hour [20] to form ~200 nm-thick tantalum pentoxide, leaving ~150 nm-thick tantalum as the first electrode layer of the eventual multi-layer interconnection. The thickness of the tantalum pentoxide layer was approximately in linear proportional to the voltage level applied. We kept the voltage long enough to ensure the anodization process is self-terminated over the entire device area. The regions of the metal layer protected by both PR1 and PR2 were never anodized and would become conductive vias later. PR2 was, then, removed.

In Figures 1(d)-1(i), similar steps were repeated to fabricate the second layer of interconnection. After depositing the second metal layer (indicated as M2) in Figure 1(d) and coating and defining PR (indicated as PR3) using the third photomask, the exposed tantalum was fully anodized to tantalum pentoxide (indicated as Ox2), which defined the conductive pattern made from the second metal layer (M2), as shown in Figure 1(e). After coating and defining another PR (indicated as PR4) using the fourth photomask, the exposed second metal layer was partially anodized to grow an insulation layer on top (indicated as Ox2 on M2), as shown in Figure 1(f). The regions of the second metal layer protected by both PR3 and PR4 were never anodized and participated in forming the conductive vias. In Figures 1(g) and 1(i), the final, third layer of interconnection was fabricated. After depositing the third metal layer (indicated as M3) in Figure 1(g) and coating and defining PR (indicated as PR5) using the fifth photomask, the exposed tantalum was fully anodized to tantalum pentoxide (indicated as Ox3), which defined the conductive pattern made from the third metal layer (M3), as shown in Figure 1(h). The final metal layer (M3) is usually not insulated on top, as shown in Figure 1(i).

2.3. Anodization and protection from anodization

All the anodization processes (Figures 1(b), 1(c), 1(e), 1(f), 1(h)) were performed on a Ta-coated glass wafer in a glass beaker (~ 1 L) containing 0.01 wt% KI solution (diluted from 0.1 M KI solution from Sigma Aldrich), as schematically illustrated in Figure 2. The wafer was placed facing parallel to the Pt foil (ESPI metals, 0.002'' in thickness) with distance of ~30 cm. The foil was similar to or larger than the anodization area on the wafer. For each tantalum layer, a large ribbon pattern was added next to the device to help current flow evenly to the device during anodization. The wafer was clamped on the metal ribbon and connected to high-voltage DC power source (Keithley 2425 and Trek PZD700). A copper tape was applied on the clamp and the metal ribbon to further reduce the resistance and even the current distribution during anodization. The clamp, the metal ribbon, the copper tape and portion of the device are kept above the KI solution. The region of the metal ribbon on the wafer was diced off after the device fabrication because otherwise the ribbon would have shorted all the electrodes on the device. During the anodization, the region being anodized turned from

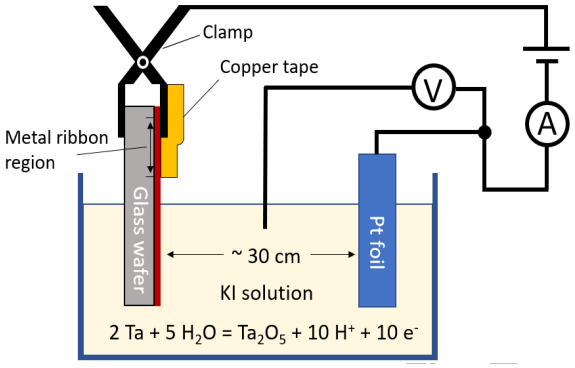

Figure 2. The anodization process setup. Sample (wafer) is connected to the anode and platinum foil is connected to the cathode of a high-voltage DC power supply. The electrode immersed in KI solution reads the voltage between the solution and platinum foil to help monitor the progress of anodization.

opaque to translucent and to transparent, which indicated full anodization. The progress of anodization was also monitored by measuring the current from the DC supply as well as the voltage between the Pt foil (cathode) and KI solution [20]; the current and voltage drop as the anodization nears completion.

During the anodization processes in Figures 1(b), 1(e), and 1(h), the patterned PR needed to protect the tantalum underneath from being anodized at a bias up to 300-350 V. We used AZ 4620, a general-purpose PR not designed to withstand high voltage, only for convenience; a different protection material with higher electrical strength would be desired in the future. In this report, we successfully repeated deposition and anodization of 250 nm-thick tantalum three times to obtain a total of 750 nm-thick tantalum at the thinnest and 1.5 µm-thick tantalum pentoxide at the thickest portions on the glass substrate. On the completed device, as illustrated in Figure 1(i), the height difference between the lowest and the highest point was around 750 nm, which is smooth enough for many microdevices over a wide range of applications without calling for planarization. This topography is similar to that of the active-matrix microdevices (< 1 µm) and significantly smaller compared with the rough topography (> 10 µm) of PCB-based microdevices.

3. Confirmation of Partial and Full Anodization

3.1. Confirmation by surface topography

Topography of the multilayer connections fabricated above is presented with Figure 3. Figure 3(a) shows an optical picture of a 2 cm x 2 cm electrode pad of M3 on Ox1/Ox2 (shown dull green) separated from neighboring pads by the isolating lines of Ox1/Ox2/Ox3 (shown bright green). In the picture, the faint circle at the center of the square pad is the circular via of M1/M2/M3, and the two pairs of faint lines running up and down on the right half of the square pad are the two connection lines of M1 under Ox1 and M2 between Ox1 and Ox2, as shown in the cross-sectional schematic of Figure 3(b) that matches the picture of Figure 3(a). The topography was obtained, using a profilometer (Dektak 6M) with 12.5 µm tip radius, by profiling the surface of the electrode pad along the horizontal line (red and broken), i.e., across the circular via and the two connection

lines, and presented by overlaying the profile on the bottom half of the electrode pad in Figure 3(a). The obtained profile in Figure 3(a) matches the expected topography presented in the cross-section schematic in Figure 3(b). Compared with the surface of typical device electrode region (Ox1 + Ox2 + M3), the via (M1 + M2 + M3) was designed to be 500 nm lower and measured to be 420 nm, while the isolating lines between electrodes (Ox1 + Ox2 + Ox3) was designed to be 250 nm higher and measured to be 200 nm higher. Similarly, the top surface over the two imbedded tantalum lines were designed to be 125 nm lower and measured to be 100 nm lower. We believe about a half of the difference in the designed vs. obtained thicknesses was due to a thinner sputtered tantalum (~220 nm) than intended (250 nm). The uncertainties by the anodization processes alone are estimated to be within 10%.

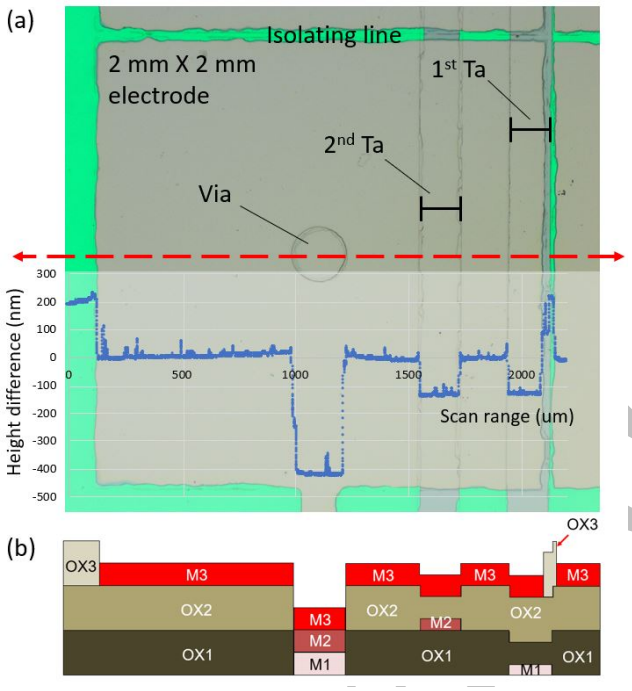

Figure 3. Measured topography of the fabricated multilayer interconnections. (a) Picture of one electrode pad surrounded by isolating lines. The surface profile along the horizontal broken line (red) is overlaid on the bottom half of the picture. (b) Cross-sectional schematic corresponding to the picture and profile.

3.2. Confirmation by electrical measurement

Because all the insulations between the electrodes are provided by anodizing metals rather than adding insulation materials in the reported process, it is important to confirm all the anodization processes provided the necessary insulations (vertically between the deposited conductive layers as well as horizontally between the lithographically-patterned electrodes) as intended. After the partial anodization, which is to form a tantalum pentoxide layer between tantalum layers, the remaining tantalum should reach a proper sheet resistance. Noting the sheet resistance is determined by the thickness of the remaining tantalum after partial anodization, which is affected by various local process parameters, such as current density of anodization, ionic concentration of the anodizing solution, temperature of the process, etc., we performed a series of characterization tests.

As illustrated in Figure 4, we exposed the two ends of test connection lines to facilitate resistance measurement using a probe station. As shown in Figures 4(a), the connection lines in the 1st tantalum layer were formed by turning the top half of the deposited tantalum layer into tantalum peroxide, i.e., an insulator. The situation is similar for the connection lines in the 2nd tantalum layer, as shown in Figure 4(b). The connection line in the 3rd tantalum layer was expected to be as thick as the deposited tantalum and twice as thick as the connection lines in the 1st and 2nd tantalum layers, because no partial anodization process was needed for the top layer. Because one half of the tantalum thickness was to be consumed for the partial anodization, the resistance of the connection lines in the 3rd tantalum layer was expected to be one half of that in the first and second tantalum layers. In the characterization tests, the resistances of the connection lines were measured to be 2.5-16 kΩ (sheet resistance ~ 62.7 Ω/Sq) for the 1st (bottom) tantalum layer, 2.7-13.8 kΩ (sheet resistance ~ 72.6 Ω/Sq) for the 2nd (middle) tantalum layer, and 0.6-7.3 kΩ (sheet resistance ~ 40.5 Ω/Sq) for the 3rd (top) tantalum layer, confirming the connectivity and successful insulation by the partial anodization. With the same width and thickness across the device, resistances of connection lines in the same tantalum layer varied by their lengths.

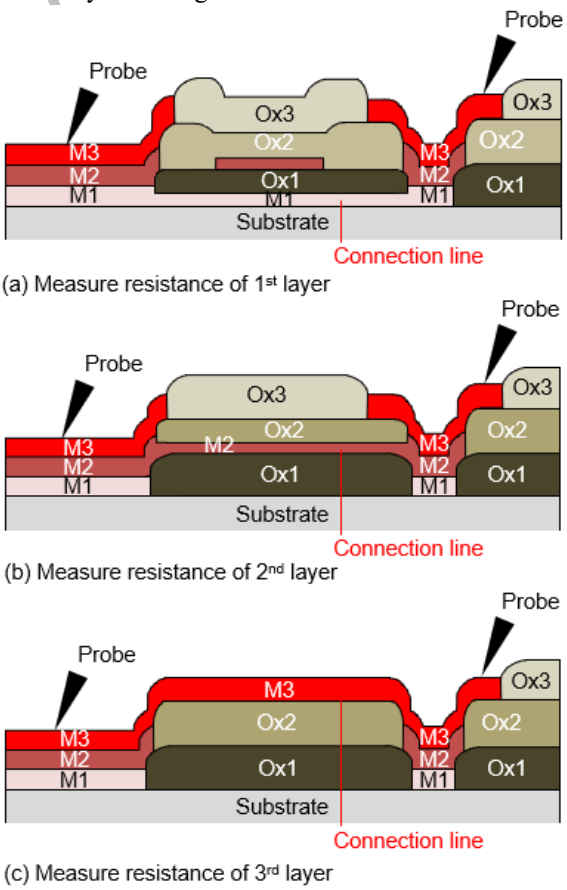

Figure 4. Resistance measurement for each conductive layer. The 3rd conductive layer, which was not anodized, was thicker than the 1st and 2nd conductive layers, which were partially anodized.

After the full anodization, which patterns electrodes within a tantalum layer, there should be no tantalum left below the tantalum pentoxide. To test the possibility of the residual tantalum shorting adjacent connection lines, we also measured the resistance between connection lines designed to be isolated from each other for each of the three tantalum layers. Resistance between adjacent connection lines was measured to be infinite, confirming successful electrical isolation by the full anodization.

4. Application to EWOD Microfluidics Devices

Utility of the proposed interconnections was demonstrated by using the developed process of Figure 1 to fabricate an EWOD device of Figure 5(a). On a typical EWOD device, a relatively high voltage (50-100 V) is applied on each of the electrodes to manipulate droplets on them. Defect-free isolation between adjacent electrodes and their connection lines are essential for successful high voltage operation. For the EWOD dielectric layer, we deposited a 1 μm-thick silicon nitride (SiN_x) by PECVD rather than partially anodizing the 3rd tantalum layer to avoid the polarity and frequencies dependencies reported by Huang et al. [21]. The fabrication of the substrate plate was completed by spin coating Teflon to form the hydrophobic topcoat. To reveal the different layers of the multilayer interconnection, we cleaved the glass substrate through an EWOD pad region and obtained SEM images (ZEISS Supra 40VP), as shown in Figure 5(b).

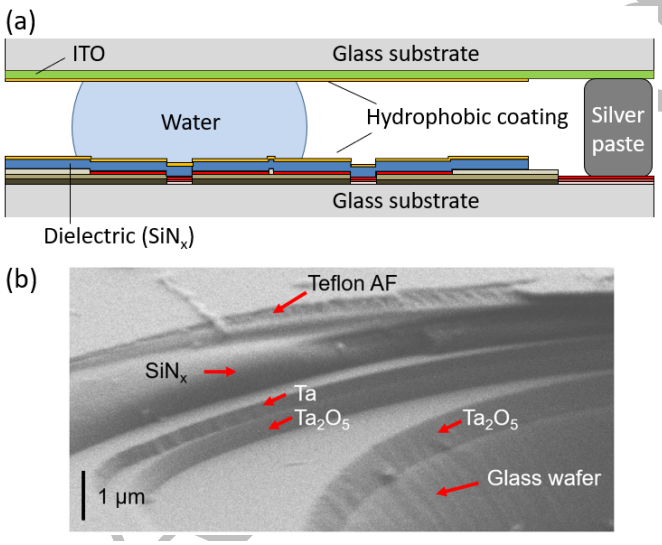

Figure 5. The multilayer interconnection fabrication applied to EWOD. (a) Cross-sectional schematic of a parallel-plate EWOD device assembled with two glass plates, showing three electrodes and a water droplet. The glass substrate with multilayer interconnections was coated with dielectric (1 μm SiN_x) and hydrophobic (100 nm Teflon AF) layer. Some of the electrodes were not coated (i.e., exposed) for electrically connecting the substrate to the cover plate (through silver paste) and also to the external control system. The cover plate with conductive ITO served as the ground for the EWOD device. (b) SEM image of a cleaved substrate reveals several layers of the multilayer interconnections as well as the two layers added for EWOD.

The EWOD device was made with two 1 mm-thick glass plates spaced by a ~0.2 mm-thick stack of 3 double-sided Scotch tapes (each ~75 μm-thick). The bottom substrate contained 100 independently controlled electrodes arranged as an array of 10x10 electrode pads, which required a multilayer electrical connection. On the device, the 10x10 EWOD electrode pads were made with the 3rd tantalum layer, and each EWOD pad (2 mm x 2mm) was exclusively connected to one of the 100 contact pads located near one edge of the device through the connection lines of all 3 tantalum layers, as illustrated in Figure 6.

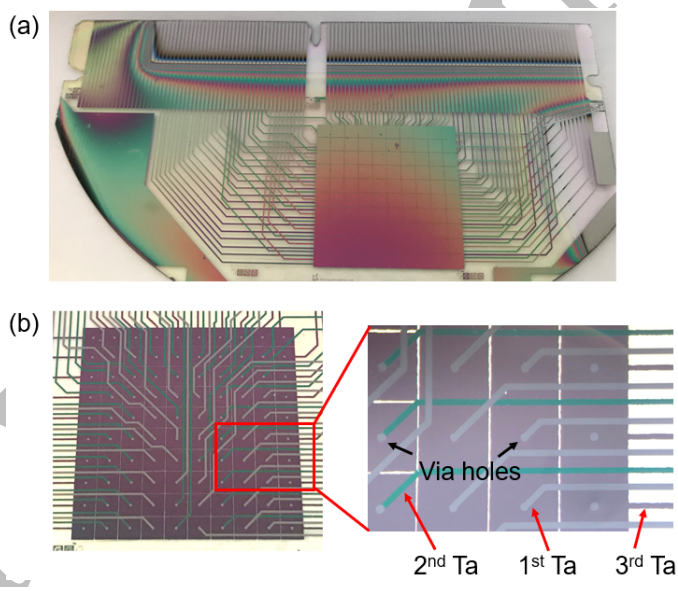

Figure 6. Pictures of the fabricated EWOD device featuring 100 independently controllable EWOD pads enabled by the multilayer interconnections. (a) The overall EWOD device shows a 10x10 array of EWOD pads; a linear array of 100 contact pads forming an edge connector; and numerous connection lines to route the EWOD pads to the edge connector. (b) The 10x10 array of EWOD pads shows each pad exclusively connected to one of the surrounding routing lines. The EWOD device is flipped for this picture to make the multilayer connections visible. The magnified inset (taken with an optical microscope) shows 9 electrode pads with vias connected to 9 connection lines of 3 different tantalum layers. The 1st and 2nd tantalum layers are visible through the overlaying tantalum pentoxide that is transparent.

Figure 7 shows the basic digital microfluidic operations (droplet translations in (a) and droplet splitting in (b)) confirmed on the fabricated EWOD device with 3-layer interconnections. The demonstration was performed using a handheld EWOD control system developed in our lab that can provide operation voltages up to 200 V and up to 1 Hz via 250+ independent channels. The transparent areas indicate that the initially opaque tantalum (~750 nm thick deposited on glass wafer) has been fully anodized to become transparent tantalum pentoxide (~1.5 μm thick) on the transparent glass. A sine wave of 70 V_{rms} at 1 kHz was used to perform the basic droplet manipulation functions for digital microfluidics (i.e., moving and splitting) with DI water in air environment (i.e., no filler oil). Although the 3rd metal is made of tantalum, which is non-transparent, in the current device, it can be made of ITO if fully

transparent devices are desired.

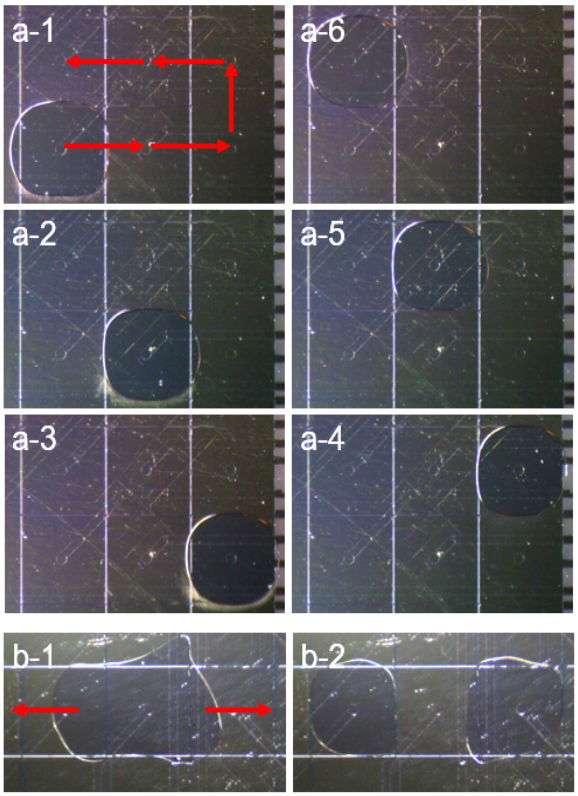

Figure 7. Digital microfluidic operations on an EWOD device with 3 layers of metal (tantalum) interconnections. The transparent top plate is made of a glass wafer coated with ITO and Teflon. (a) Sequential images of droplet translations. Arrows indicate the moving directions of the droplet. (b) A droplet split into two daughter droplets.

For successful operations, all EWOD pads should be connected to ground or high voltage and avoid floating. Since the insulation layer, i.e., the anodized metal, on the metal has a thickness comparable to the dielectric layer of a typical EWOD device, the connection lines placed underneath the electrode pad (the 1st and 2nd metal shown in Figure 3) may induce unintended electrowetting effect to the droplet if the electrode pad is floated. Another point to make is the limitation in the actuation voltage allowable for the EWOD devices made with the reported multilayer interconnection fabrication method. One cannot use voltages higher than the anodization voltage (~100 V) for EWOD actuation because it may cause electric breakdown between metal layers. In other words, the proposed EWOD devices are suitable for relatively low voltage (< 100 V) actuations.

5. Conclusions

We have developed a low cost and low topography fabrication method to obtain multilayer interconnections. The reported fabrication is of low cost compared with the usual method because all the insulation layers and isolating patterns are formed by anodization in a wet bath rather than by thin-film deposition, photolithography, and plasma etching. Also, the total number of masks needed is reduced by nearly a half. The maximum height difference for the topography on the device surface was ~0.75 μm and the gap between electrodes (i.e., feature size) was ~10 μm, which is significantly better than microdevices made of a PCB substrate (> 10 μm in maximum height difference and > 50 μm gap between electrodes). We used this method to fabricate an EWOD device with 3 layers of electric interconnection and demonstrated the basic droplet manipulations for digital microfluidics in air. The results support the potential of the proposed fabrication method as a low-topography and small feature-size alternative to the PCB EWOD devices and a low-cost alternative to the active matrix TFT EWOD devices.

Acknowledgments

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