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Modeling and Analysis of Shutdown Dynamics in Flying Capacitor Multilevel Converters

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Abstract: This work explores the dynamic behavior of the flying capacitor multilevel (FCML) converter during unplanned shutdown. A model for a general N-level FCML converter is developed, which captures capacitor non-linearities, component leakage paths, and body diode behavior. This work highlights how switch voltage ratings may be exceeded during unplanned shutdown, and proposes several mitigation strategies. Using a ten-level FCML converter hardware prototype, the time-domain behavior of the model is verified, and a successful hardware mitigation strategy is demonstrated which ensures safe and rapid converter shutdown.

I. Introduction

Flying capacitor multilevel (FCML) converters have been shown to have high efficiency and power density over a wide range of applications [1]; from high voltage electric aircraft drivetrains [2], to low voltage data center applications [3]. The FCML converter achieves high power density through the use of flying capacitors, which can be implemented using energy dense capacitors, such as Class II multilayer ceramic capacitors (MLCCs). Moreover, the flying capacitors provide dc voltage blocking, enabling the use of low voltage power transistors in the FCML topology, with corresponding fast switching speed and low conduction loss. While these flying capacitors enable compact and efficient designs they also present challenges, such as capacitor voltage balancing [4]. If the capacitor voltages are not balanced, the voltage stress on individual switches within the FCML converter may exceed their rating, causing failure. Ensuring balanced operation is particularly challenging at start-up and shutdown, where all flying capacitors must ramp up and ramp down with uniform voltages to avoid switch damage. Previous work has presented solutions to the challenge of start-up through additional auxiliary circuits [5] and sophisticated modulation techniques [6], [7]. While start-up has been the primary focus of previous work regarding the practical implementation of FCML converters, little work has been done exploring dynamics of converter shutdown, which is the focus of this work.

This work explores the voltage dynamics of the flying capacitors when an FCML circuit is suddenly de-energized, and investigates safe shutdown techniques in practical implementations. Moreover, a computationally efficient dynamic model of the FCML converter during shutdown operation is proposed, and used to demonstrate how device ratings and converter failure can result from sudden loss of control power. Based on the findings of the dynamic model, several safe shutdown techniques are verified and evaluated.

The remainder of this paper is organized as follows: Section II introduces the relevant FCML converter component models and the proposed model. Following this, Section III describes an experimental prototype used to validate the model. Section IV proposes three safe shutdown techniques and evaluates each method's performance. Finally, Section V concludes the paper.

II. Proposed Shutdown Model

A. FCML Converter Model Parameters

A generic N-level FCML boost converter is shown in Fig. 1. While the analysis presented here is for the boost converter, we note that due to the bi-directional nature of the FCML converter, the analysis also applies to a buck implementation. In the model of Fig. 1, input and output terminals are connected through relays (R_{input} and R_{output}) that may isolate the converter from the source and load during start-up and/or shutdown. This functionality is often required in practical implementations, where switches or solid-state circuit breakers may be employed.

During nominal FCML operation the flying capacitors are charged to $k \times \frac{V_{out}}{N-1}$, where k is the capacitor index, as defined in Fig. 1. When capacitor voltages are balanced the voltage across each switch when in the off-state (excluding any switching ripple) is $\frac{V_{out}}{N-1}$. However, if the capacitors are not balanced, i.e. they are not charged to their nominal voltages, then switch stress will vary and may result in overvoltage of switches.

As will be shown in this work, the shutdown behavior of the FCML converter is highly dependent on the

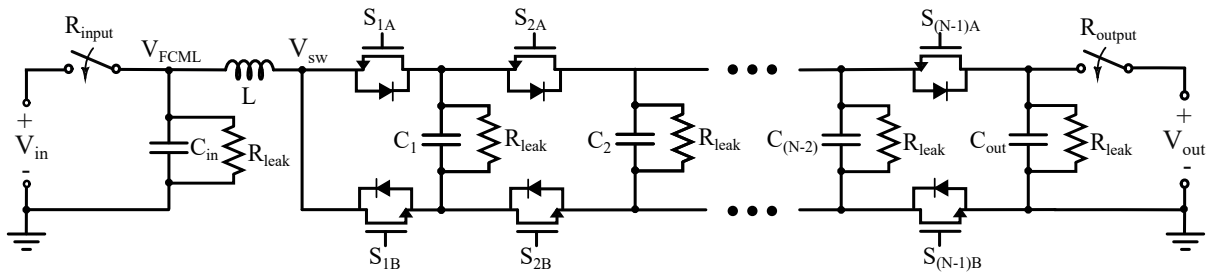

Fig. 1: Circuit model of a generic N-level FCML converter, with input and output breakers. Additionally, the proposed auxiliary shutdown circuit is shown.

component non-idealities, such as transistor body diodes and parasitic leakage paths. In the model presented in Fig. 1, the anti-parallel diodes correspond to body diodes in silicon MOSFET implementations. Although Gallium Nitride (GaN) transistors do not have a body diode, their reverse conduction associated with channel inversion is also captured by the diode model. For the capacitors, both leakage resistance and non-linear capacitance (particularly prominent in high density Class II MLCCs) are modeled [8].

B. Shutdown Dynamics

In general, converter shutdown can be either planned or unplanned. Here, we investigate the more difficult case - unplanned shutdown - stemming from a loss of control power which results in the opening of input and output relays (R_{input} and R_{output}), and the loss of gate-drive power to all switches.

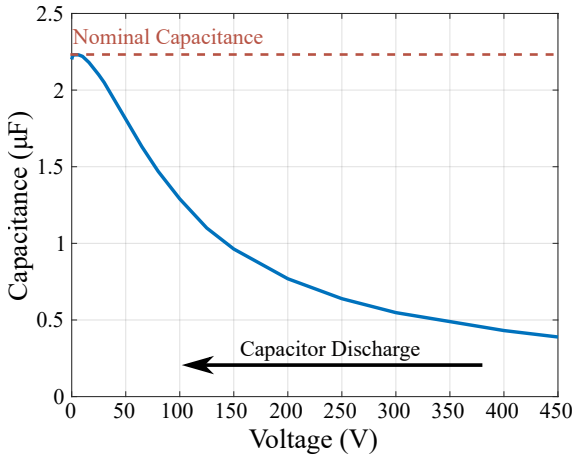

Fig. 3: Class II MLCC capacitance de-rating curve, as the capacitor discharges the capacitance will increase non-linearly [9].

1) Flying Capacitor Discharge: With gate drive power off, all the switches open, and the flying capacitors will begin to discharge through their internal leakage resistance and any leakage resistance of the switches. In the case where the flying capacitors are Class II MLCCs, the capacitance of the device will increase as the device discharges. An example capacitance de-rating with voltage curve, for a Class II MLCC can be seen in Fig. 3. This creates a non-linear function as the voltage of each flying capacitor decreases at a different rate dependent on the nominal voltage.

2) Leakage Resistance: Further complexity is added due to the leakage resistance which may vary between levels depending on the converter design. For the capacitor described in Fig. 3, the leakage resistance is listed as 227 MΩ on the datasheet [9]. However, this leakage resistance is not well documented and may change with operating conditions (such as MLCC parasitic series resistance). In many FCML converter designs the flying capacitors are implemented with stacked MLCCs in series to meet voltage rating requirements [10] [6]. To ensure even voltage balance across series stacked capacitors, parallel resistances are typically added as shown in Fig. 4. These balancing resistors decrease the effective parallel resistance to R_b (assuming R_b is significantly smaller than R_{leak}) and therefore increase the discharge rate of the flying capacitors during shutdown.

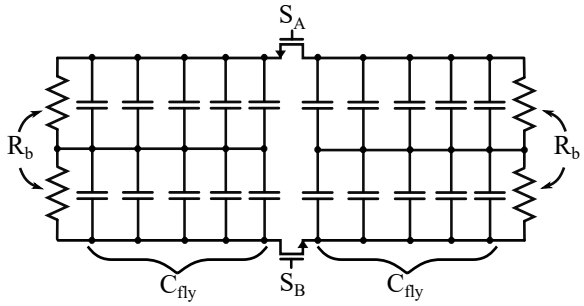

Fig. 4: Example flying capacitor implementation showing series stacked capacitors and balancing resistors.

3) Body Diode Conduction: As the flying capacitors discharge, reverse polarity may occur across several

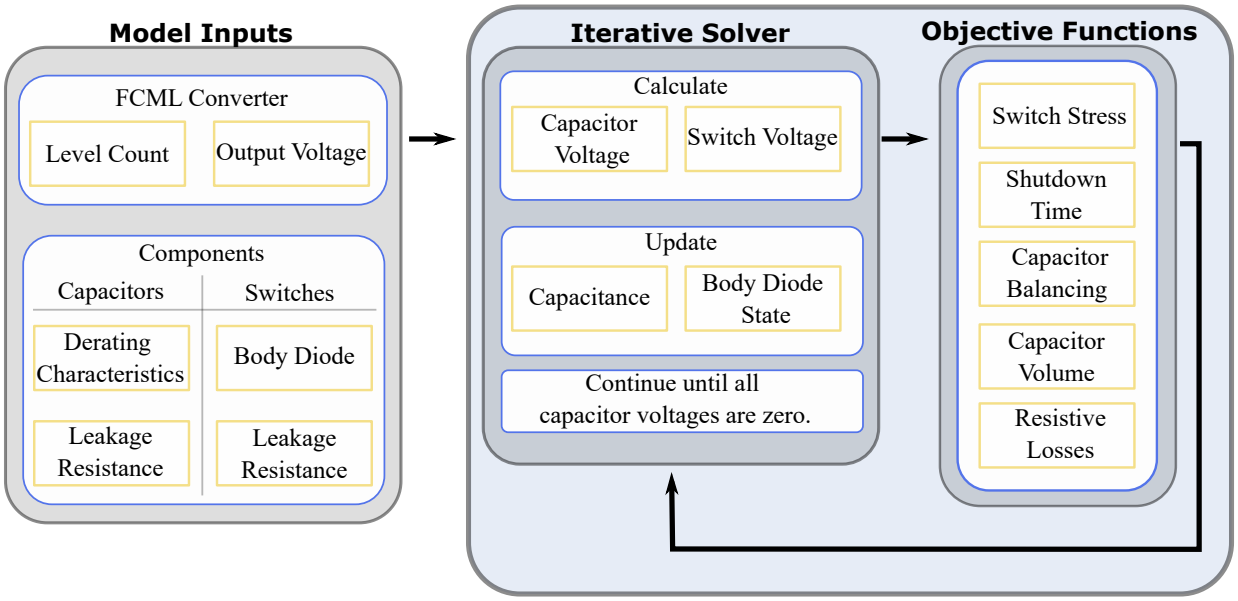

Fig. 2: Flowchart for proposed shutdown model.

switches causing reverse conduction. If reverse conduction occurs, the complexity is further increased as the flying capacitors no longer discharge along independent paths, and may combine in parallel, with modified leakage paths.

C. Model Description

As noted in the preceding section, the dynamic behavior of the FCML converter involves both non-linear passive elements, and switching circuit states due to diode turn-on. While circuit simulations (e.g., SPICE) can compute the behavior for a specific converter design under narrowly defined operating conditions, it becomes intractable to perform design optimization and investigation across full converter operating ranges using such an approach. To enable computationally efficient investigation and design optimization of the FCML converter at shutdown, an iterative MATLAB model for a wide range of FCML design choices was developed in this work. As described in Fig. 2, the model requires the FCML converter design parameters as inputs: the level count, the output voltage, and details of the switch and capacitor implementation. The model iteratively solves for capacitor discharge over time, updating the capacitance and diode states each cycle. As a result, the switch stress and capacitor voltage limits during shutdown can be included in overall FCML design optimization, with shutdown time, balancing effects, volume and losses accounted for.

III. Modeled Shutdown Procedures

A. Experimental Prototype

For this work, a ten-level FCML converter with a output voltage of 750 V is considered. An annotated photograph of the hardware prototype can be seen in Fig. 5, with the input and output relays. The nominal voltage and capacitance of each flying capacitor is shown in Table I. The de-rated capacitance is also shown, which is calculated based on the derating curve shown in Fig. 3. Furthermore, this converter is designed with 200 V GaNFETs (EPC2034C), therefore it is vital that the switch stress remains below 200 V during shutdown.

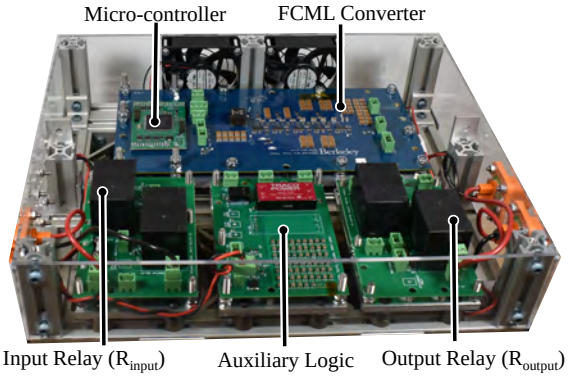

Fig. 5: Hardware prototype, showing FCML converter, input and output relays.

Flying Capacitor	Nominal DC Voltage	Nominal Capacitance	De-rated Capacitance	Series Capacitors	Parallel Resistance
C_{in}	550 V	33 μF	8.9 μF	Yes	2 MΩ
C_1	83 V	6.6 μF	3.96 μF	No	227 MΩ
C_2	167 V	6.6 μF	2.64 μF	No	227 MΩ
C_3	250 V	6.6 μF	1.98 μF	No	227 MΩ
C_4	333 V	6.6 μF	1.32 μF	No	227 MΩ
C_5	417 V	5.5 μF	1.65 μF	Yes	2 MΩ
C_6	500 V	5.5 μF	1.38 μF	Yes	2 MΩ
C_7	583 V	5.5 μF	1.20 μF	Yes	2 MΩ
C_8	667 V	5.5 μF	1.10 μF	Yes	2 MΩ
C_{out}	750 V	33 μF	6.9 μF	Yes	2 MΩ

TABLE I: Flying capacitor design specifications.

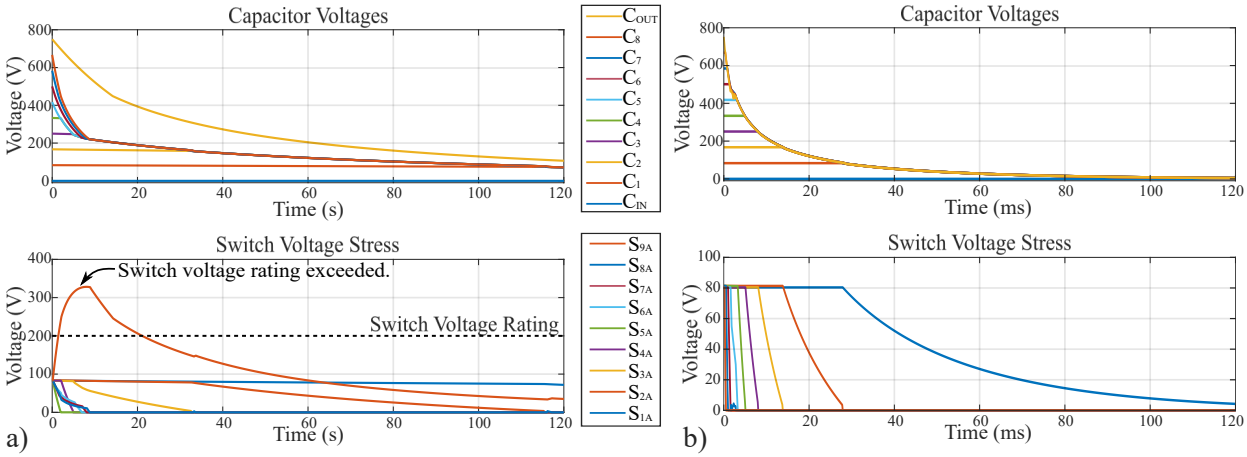

Fig. 6: a) Modeled shutdown, where no safe shutdown techniques are implemented. The complete shutdown process takes over two minutes and the voltage rating of the switches is exceeded. b) Modeled shutdown with resistive load. With this method complete shutdown occurs after 120 milliseconds, and all switches remain under their rated voltages.

B. Modeled Unsafe Shutdown

Shown in Fig. 6-a are plot of flying capacitor and switch voltages overtime for a shutdown procedure with the model parameters of Table I. Considering the prototype converter with no special consideration for shutdown, the MATLAB model determines the capacitor discharge and worst case switch stress. During this shutdown the highest high-side switch (S_{9A}) experiences switch stress over 300 V, well above the rated device voltage, which would result in a device failure. The key contributor to the large switch stress is the output capacitor, which decays much slower than the flying capacitors due to its significantly larger capacitance. In addition to the required terminal voltage filtering, a sufficiently large output capacitor (in comparison to the flying capacitors) is also needed to ensure good capacitor voltage balancing during steady-state operation [11]. Thus, simply reducing the output capacitor to avoid this condition is not a feasible solution in a practical implementation.

IV. Proposed Safe Shutdown Techniques

The proposed model was used to determine several safe shutdown techniques. These shutdown procedures are designed with the following goals of safe shutdown:

- Low switch stress: The switch stress should not exceed the voltage rating of the device during shutdown procedure.
- Short shutdown time: The shutdown time should remain short. If the system does not completely discharge before a subsequent start-up attempt, the capacitors may start-up non-uniformly, resulting in failure.
- Low losses: Any additional circuitry added to the system should not incur significant losses during nominal operation.
- Small footprint: The suggested shutdown circuitry should have a negligible impact on the overall converter volume/weight.

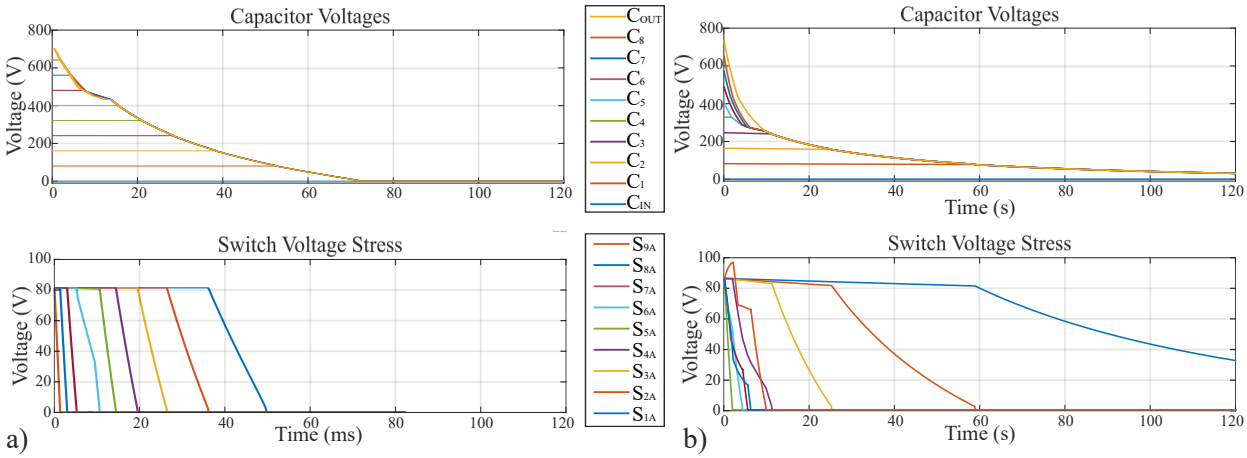

Fig. 7: a) Modeled shutdown with auxiliary shutdown circuit. b) Modeled shutdown with adjusted balancing resistor value to decrease voltage stress.

A. Normally Connected Resistive Load

The first proposed solution is to connect a resistive load during shutdown. This can be done with a normally-on configured switch in place of R_{output}, as shown in Fig. 1, so that even with loss of logic power the resistive load remains connected to the output capacitance. This method effectively increases the discharge rate of the output capacitance. Fig. 6-b shows modelled shutdown with the resistive load. With this method there is no over-voltage of the switches and the shutdown process occurs in approximately 120 milliseconds. This shutdown procedure was verified with the experimental prototype at high voltage (750 V) and the flying capacitor voltages were measured. As shown in Fig. 8, the experimental results signify safe shutdown through uniform capacitor discharge. Note, the delay shown in Fig. 8 between the switching and input relay opening is due to the internal delay in the relay.

While effective, it is not always feasible to keep the load connected during shutdown, which is the limitation of the suggested technique. For safety reasons it is often not desired to continue powering the load during a shutdown. Moreover, this method requires a primarily resistive load which also is dependent on system architecture.

B. Auxiliary Shutdown Circuit

Fig. 9 shows a proposed auxiliary circuit which implements a switchable current regulator (I_C) [12]. A normally high signal from the micro-controller, labeled Q_s keeps the current regulator off during nominal operation. Once shutdown occurs and Q_s transitions to 0 V, the current regulator turns on and provides a discharge path for the output capacitance. The resistor, R_C sets the constant current, designed in this case to 100 mA.

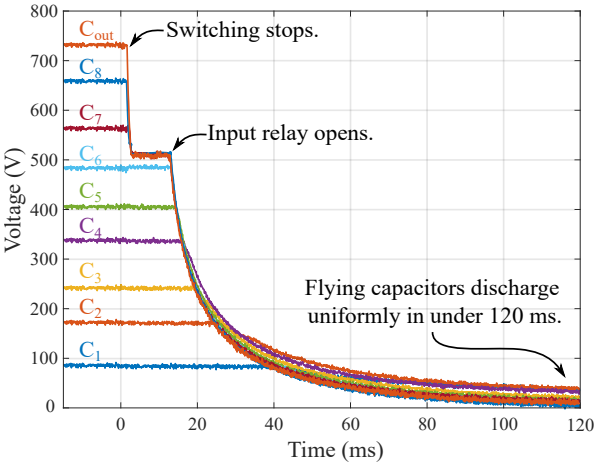

Fig. 8: Experimentally measured flying capacitor voltages during shutdown, with resistive load connected. Shutdown initiated from 750 V output steady-state operation.

The model was configured to account for this current regulating device, and the results are shown in Fig. 7-a. This method results in a shorter shutdown time than the previous method, and ensures no device overvoltage. However, this auxiliary circuit does require added volume. For this prototype the auxiliary circuit was implemented in less than 0.4% of the total converter volume. It should also be noted that this auxiliary circuit does not consume any power during nominal operation and therefore does not decrease the converter efficiency.

C. Adjustment of balancing resistors

As indicated by the proposed model, the selection of the balancing resistors has a significant impact on the discharge of the capacitors. To increase the discharge

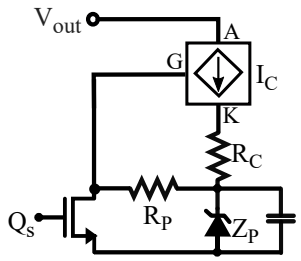

Fig. 9: Auxiliary shutdown circuit, utilizing a switchable current regulator (I_C).

rate of the output capacitance the balancing resistor at the output can be decreased. For this example, the effective parallel resistance of the output capacitance was decreased to 1 MΩ. As shown in Fig. 7-b, this method results in a small amount of additional voltage stress on the switches, but is still well below their rated voltage. This method results in a negligible volume increase as the balancing resistors were already included in the design. However, this resistance does add to the overall converter losses. At 750 V output, these balancing resistors will dissipate 1.2 W. These additional losses are considered negligible at high power (2.5 kW for this prototype), but may be deemed significant at light load or idle operation.

V. Conclusion

This work has demonstrated the need for safe shutdown techniques within the FCML converter. A framework for modeling the FCML converter during shutdown was introduced, which includes non-linear component effects. Subsequently, this model may be used to design for safe shutdown dynamics with constrained device stresses. Experimental results verify safe shutdown with a resistive load. Furthermore, several additional techniques that also result in safe shutdown are modeled and evaluated, providing a framework by which optimal shutdown strategies can be selected for a given design.

VI. Acknowledgements

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References

[1] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, Jun 1992, pp. 397–403 vol.1.

[2] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a GaN-based interleaved nine-level flying capacitor multilevel inverter for electric aircraft applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 153–12 165, 2020.

[3] J. S. Rentmeister and J. T. Stauth, "A 48V:2V flying capacitor multilevel converter using current-limit control for flying capacitor balance," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 367–372.

[4] Z. Xia, B. L. Dobbins, and J. T. Stauth, "Natural balancing of flying capacitor multilevel converters at nominal conversion ratios," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[5] A. Stillwell, C. N. Robert, and Pilawa-Podgurski, "A 5-level flying capacitor multi-level converter with integrated auxiliary power supply and start-up," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2932–2938.

[6] N. Pallo, S. Coday, J. Schaadt, P. Assem, and R. C. N. Pilawa-Podgurski, "A 10-level flying capacitor multi-level dual-interleaved power module for scalable and power-dense electric drives," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 893–898.

[7] P. Papamanolis, D. Neumayr, and J. W. Kolar, "Behavior of the flying capacitor converter under critical operating conditions," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, 2017, pp. 628–635.

[8] S. Coday and R. C. Pilawa-Podgurski, "High accuracy calorimetric measurements and modeling of ceramic capacitor losses under large ripple operation," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 188–194.

[9] TDK, "C series commercial grade mid voltage (100V to 630V)," Datasheet, Mar. 2015.

[10] S. Coday, N. Ellis, Z. Liao, and R. C. N. Pilawa-Podgurski, "A lightweight multilevel power converter for electric aircraft drivetrain," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021.

[11] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, "Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2017, pp. 1–7.

[12] IXYS Corporation, "Switchable current regulators," Datasheet, 2010.