UNIVERSITY OF CALIFORNIA
RIVERSIDE

Write-Once Read-Many-Times (WORM) Memory based on Zinc Oxide on Silicon

A Thesis submitted in partial satisfaction
of the requirements for the degree of

Master of Science

in

Electrical Engineering

by

Qing Zhang

August 2011

Thesis Committee:
Dr. Jianlin Liu Chairperson
Dr. Albert Wang
Dr. Elaine Haberer

The Thesis of Zhang Qing is approved:

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Committee Chairperson

University of California, Riverside

Acknowledgment

I want to thank my professor, Dr. Jianlin Liu for all his support, efforts and advice during the two years period, also providing me advanced equipment to complete the research I needed to finish my master's degree. Thanks to Dr. Sheldon Tan, and Dr. Ertem Tuncel for recommendation letters to the school, so I could have the opportunity to be in the master's degree program of UCR.

I sincerely appreciate the help from Jing Qi, a visiting scholar in our laboratory. She taught me like a mentor, providing samples I need for my experiment, and working closely with me to design test procedure and discuss test results. Without her dedication, I would not be able to do what I have done for the two years.

I would also like to show my thanks to other Ph. D students in my laboratory: Zheng Zhuo, Jian Huang, Mario Olmedo, Jinjian Ren and Huimei Zhou for their support on equipment setup, troubleshooting, and operation. Lot more time would have been lost during the use of equipment without their immediate help.

Finally, I want to thank my family for their mental and financial support, so I could concentrate on my study without having other burdens on my shoulder.

ABSTRACT OF THE THESIS

Write-Once Read-Many-Times (WORM) Memory based of Zinc Oxide on Silicon

by

Qing Zhang

Master of Science, Graduate Program in Electrical Engineering
University of California, Riverside, August 2011
Dr. Jianlin Liu, Chairperson

Write-once read-many-times (WORM) memory feature is found in ZnO films deposited on silicon substrates. The resistance ratio (R ratio) between the high resistance state (HRS or ON state) and low resistance state (LRS or OFF state) is mostly around 10^4 for all tested devices. The programming power required to switch the memory devices from HRS to LRS can be as low as 10^{-3} watts when current compliance is set at 50 μA. Lowering the current compliance will result in lower R ratio, because the maximum LRS current level will also be limited by the current compliance.

To test the devices for long term storage purpose, endurance to reading pulse with width of 2μs and amplitude of 1V were tested for several randomly selected devices with various top contact sizes. Results shown all devices sustained their R ratio with hardly noticeable resistance change throughout 10^8 reading cycles. Retention was also tested on several devices. The results showed that only R ratio of HRS showed some drop in resistance after 10^5 seconds (27.78 hours) testing period, while LRS current level was almost constant throughout. R ratio still retained around 10^3 after being extrapolated to 100 years. Temperature stability of the devices was also tested up to 120 ℃. There was current drop in both HRS and LRS under high temperature over time, but the overall R ratio did not change much, still above 10^3 for all tested devices. Endurance and retention test results under high temperature showed similar trend as room temperature.

Au metal contact devices showed almost undetectable HRS current by the equipment because the probe station used has current noise level which is almost the same as the current level of the HRS devices. Devices with Au and Ti metal have almost the same conductivity at LRS, and Au top contact has the potential to provide higher R ratio for WORM devices. Higher memory performance can be clearly observed in devices fabricated on p-Si substrates than that on n-Si substrates. Devices on p-Si substrate showed low rectifying ratio in HRS, and high rectifying ratio in LRS, thus the R ratio of the devices is higher. The high rectifying ratio in both HRS and LRS in devices with n-Si substrate resulted in lower R ratio of around 10^2.

The switching mechanism of all devices is explained by the filament model, in which conducting filaments consisting of oxygen vacancies are formed after applying external electric field to switch the device to ON state. The filament model explained why all devices' LRS conductivity is independent of contact size. As write-once memory, the LRS devices have to sustain their resistivity through any external electric field. Test results showed that all devices do not reset to HRS after repeatedly attempting to reset devices by looping the -5V ~ 5V sweep on them. Although all devices kept their LRS status, a slight reset can be observed in the negative bias region, positive bias region showed no sign of reset.

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Chapter 1: Introduction

ZnO semiconductor material has attracted a great deal of interest. With large exciton binding energy of about 60 meV and direct wide band gap of 3.37eV, ZnO is a promising candidate for applications in optoelectronics, spintronics and light-emitting-diodes (LED) near the UV region devices.[1-2] ZnO also possess other great properties, such as large piezoelectric constants for sensors, transducers and actuators application.[3] It can be used as a cheap smell sensor to detect the freshness of foods and drinks, due to its strong sensitivity of surface conductivity to adsorbed species.[4] High thermal conductivity that can achieve faster heat removal during device operation, and amenability to wet chemical etching, make ZnO thin films very flexible in the fabrication, design and integration of electronic memory devices.[2] There are reports about hetero-junction diode applications using ZnO material with other organic materials.[5] ZnO p-n junction has also been reported.[6] However, doping ZnO with metalloid element is required to achieve p-type[1], and the subject is still under debate because reliability and reproducibility of p-type ZnO is still an ongoing issue.[1-2]

On the other hand, write-once read many times memory (WORM), in which the data storage is permanent and cannot be modified, has extensive application for archival storage of video images and non-editable database.[5] Studies regarding the formation and electrical properties of WORM devices using organic materials[7], inorganic/organic nano-

composites[8], and inorganic/organic hetero-junction [9] have been carried out. However, no research on WORM devices based on ZnO film has been reported yet. ZnO is environmental friendly, abundantly available in nature, compatible with metal-oxide-semiconductor technology, and already has well developed growth technologies.[10] All those facts make ZnO a promising candidate for WORM application. In this thesis, ZnO thin films were utilized to fabricate WORM devices. The characteristics of the memory will be discussed in detail.

At first, the focus will be on test results from the device sample with Au/Ti/ZnO/p-Si/Al layered structure. The resistive switching from HRS to LRS is discussed in chapter 3. I-V characteristics and writing process of all tested devices are summarized. To reduce the power required for writing process, tests with various switching current compliance have been run. The smallest devices with contact size of 30 $\times$ 30 um^2 received extensive research. At the end of chapter 3, the effect from the MgO buffer layered is discussed.

Chapter 4 is mainly dedicated to show the nonvolatile properties of the sample, since long lasting storage is one of the most important properties that a WORM device must possess. Endurance, retention and thermal stability tests were run, and results are discussed in this chapter.

Test results on devices with Au top contact and n-Si substrate are discussed in chapter 5. Then, the results are compared among the devices in Chapter 3 and 4 to study the dependence of memory performance on top contact metal and substrates.

The switching mechanism and the chemical reaction during writing process in all devices are explained in chapter 6. The effect of oxygen vacancies that existed in ZnO material after the fabrication of the sample will also be shown. To make sure the memory devices are write-once memory (will not be switch back to OFF-state), experiments attempted to reset devices to HRS was run. In the last section of this chapter, the I-V curves of HRS and LRS from the Au/Ti/ZnO/p-Si/Al layered sample will be fitted into their current models.

Chapter 2: Fabrication

ZnO thin films of 60nm were deposited on both n type and p-type Si (111) substrates at 400 ℃. Doping was not included as one of the research subjects, all ZnO in this thesis is n-type, and n-type ZnO can be unintentionally achieved.[1-2,10] A few atomic layers of MgO were added as buffer to accommodate the crystallography difference between ZnO and Si. The MgO is designed to be very thin so that it has no impact on the overall memory performance. Radio-frequency (RF) plasma-assisted molecular beam epitaxy (MBE) system was used for this process. The Si substrates were cleaned using standard RCA method to remove contamination and the native SiO_2 layer. High-purity Mg (6N) and Zn (6N) sources were evaporated from conventional low-temperature effusion cells. Atomic oxygen was provided by RF plasma source. Ti (10nm)/Au (90nm) square-shaped metal patterns of different areas acting as top contacts were deposited on the surface of ZnO by electron beam evaporation. Ti is the material forming the metal-semiconductor junctions; Au is used to protect the Ti from corrosion. Photolithography followed by standard lift-off process was used to make the Ti metal contact in six different sizes. Al was evaporated by electron-beam evaporation to the bottom of the p-Si substrate as back contact. The whole device fabrication process was performed in the clean-room which is running and certified at class 100 in the Photolithography bay and class 1000 in other areas.

Other film samples with different substrates and top contacts were also fabricated. ZnO was deposited on n-Si substrate to compare test results with p-Si substrate devices,

Fig. 2.1: Mixed view of the structures of all fabricated samples

and Au metal was deposited as top contact to compare with the Ti top contact devices. The growth conditions for these samples were the same as mentioned in the first paragraph. The image in Figure 2.1 is the overall structure of all the samples mentioned above.

All film samples are prepared by a visiting researcher, Jing Qi. She deserves all credits for the fabrication of the films. This thesis is based on results after characterization of all the devices, and analysis of the WORM properties of these devices.

Chapter 3: WORM Effect

3.1: Testing Procedure

The sample consisted of n-type zinc oxide on p-type silicon substrate devices is placed on a Signatone H150 probe station under room temperature in open air environment. The sample is situated on the device stage exactly as it shown in figure 3.1. Micro-positioners are sitting on the U-shaped linear motion platen. There are micro-positioners sitting on top of the motion platen, and in my case, they are air based and an air pump is used to hold all of them in position. The needle at the tip of the micro-

Fig. 3.1: Signatone H150 probe station.

positioner is used to make contact with the top contact of the selected device to apply an external bias. The bottom contact is making direct contact with the highly conductive device stage, which is connected straight to ground. Device is selected looking through the 4" x 4" microscope stage. The device sizes on the sample are ranging from 30 x 30 um^2 to 600 x 600 um^2. Operation of the microscope is necessary to help place the needle right on the spot.

I-V characteristics of the samples are measured using Agilent 4155C semiconductor parameter analyzer. Two probes were used from the analyzer. One is set to output voltage and conduct current measurement and then connected to the micro-positioner, and the other is set to ground and connected with the device stage. 'Sweeping Mode' is selected for measuring I-V characteristics. A set range of voltage is applied on the selected device. The corresponding current value will be displaced as a two dimensional I-V curve graph and the detail of the graph is numerically listed as well. Length of the list depends on the step voltage setting. Current compliance can be specified up to 100mA.

3.2: Memory Effects in the Devices

Devices with Au/Ti/ZnO/p-Si/Al layered structure are discussed in this section. The initial I-V characteristics of selected devices are tested by applying external sweeping voltage from -1.5V to +1.5V. Current compliance is set to 100mA. At this point the resulting current is low and the device is at its high resistive state (HRS) or OFF state (figure 3.2). After the initial sweep, another external sweeping voltage from 0 to 20V is applied. This is also the "writing process" or "programming process" of the memory device. A sudden increase of current from the nano-ampere range to the set current compliance indicates that the selected device has switched from high resistive state to low resistive state as shown in figure 3.3. Another -1.5V to +1.5V sweep is performed again after the writing process. The result of this sweep is considered as the I-V characteristic of the device in low resistive state (LRS) or "ON-state".

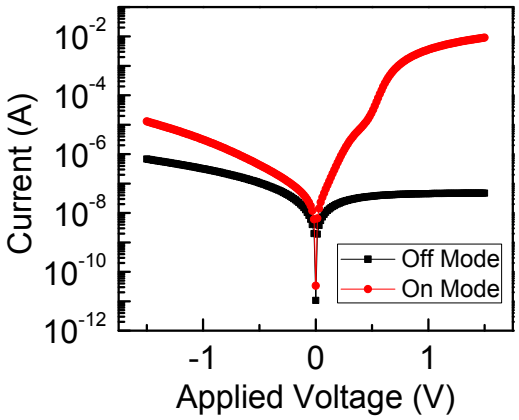

Fig. 3.2: On/Off mode I-V curves of a single 30x30 um^2 device swept from -1.5V – 1.5V.

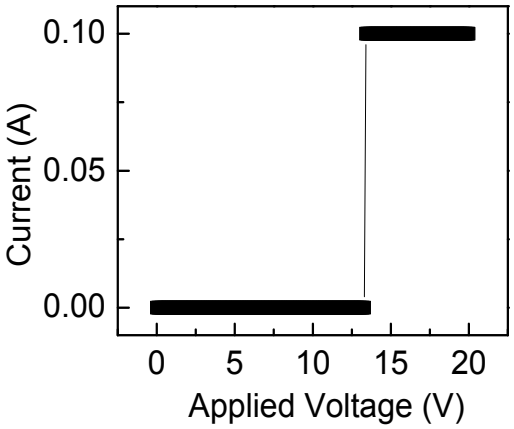

Fig. 3.3: 0 to 20V I-V swept of a 30x30 um^2 device with a sudden resistance breakdown.

Figure 3.2 provides a typical comparison of the ON- and OFF-state sweep. The R ratio in this example is about 10^5 at a reading bias of 1V. The writing process in figure 3.3 shows the writing voltage of around 14V for the device shown as an example. Current value burst from close to zero range to the maximum allowed current at a single voltage step. Both figures above have shown the typical results of reading and writing process for all of the devices. Testing has been done on more than 600 devices of different top contact sizes and the statistic results are shown and discussed next.

Figure 3.4 shows the resistance probabilities of all the 30×30 um^2 top contact devices in both ON and OFF states. The resistance for LRS and HRS distributes mainly

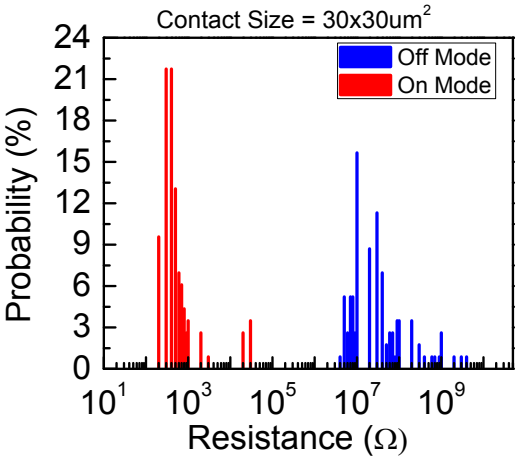

Fig. 3.4: High/Low resistance probability of 30x30 um^2 devices (all devices are switched from high to low resistance).

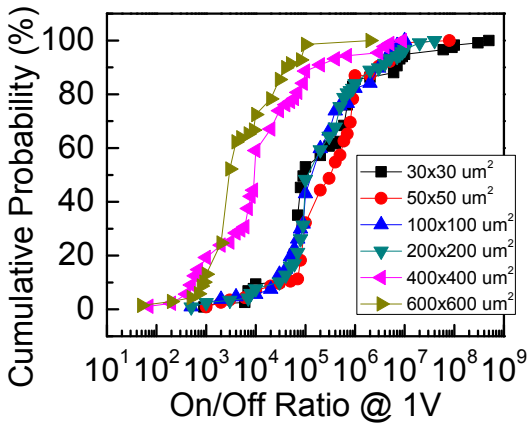

Fig. 3.5: R ratio of all devices in all contact sizes.

around 10^2 and 10^7 Ω respectively. Figure 3.5 is the R ratio cumulative probabilities plot for devices of all top contact sizes. The highest R ratio is in the order of 10^7, and the

lowest ratio is about 10^3. Majority of the R ratios are in the 10^4 ~10^6 range. In the plot, the R ratio is reduced by a whole order of magnitude starting from the device size 400x400 um^2. Increase in device top contact size results in lower R ratio.

The cumulative probabilities for the writing voltage of all tested devices in different top contact area sizes are illustrated in figure 3.6. The probabilities show that

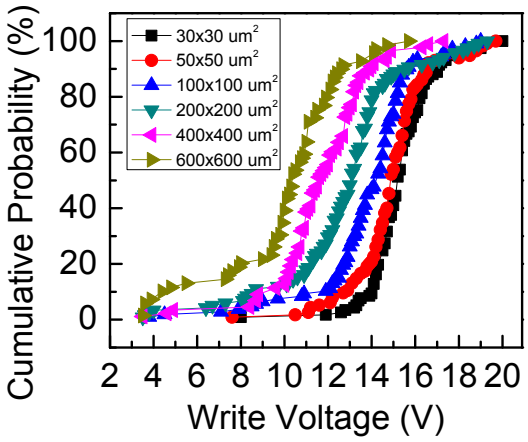

Fig. 3.6: Writing voltage of all devices in all contact sizes.

Write Voltage	R ratio
8	2.20E+04
11.9	5.90E+05
12.6	1.20E+04
13.2	3.90E+04
14.5	2.20E+05
15.3	5.00E+04
16.1	3.00E+05
17.1	2.10E+04
18.5	3.20E+04
19.1	1.90E+03
20	4.30E+04

Table 3.1: Writing voltage and the corresponding R ratio of the same device at 1V external bias.

larger devices require relatively lower writing voltage. Extreme cases do exist and they happen on both end, but the chance of them happening is low compared to the majority cases. At the lower end, the writing voltage can be as low as 3V; the high end is at or very close to 20V. However, among all the tested devices, the writing process never required more than 20V of external bias when current compliance was set to 100mA. The question for whether writing voltage is directly related to the R ratio of the same device is

considered. Table 3.1 is a list of devices with various breakdown voltages and their R ratios after the writing process. The numbers in the table suggest that the resulting R ratio of any device is independent of its breakdown voltage during the writing process, and the writing voltage is neither affected by the HRS value nor resulting in higher or lower ON-state current.

To summarize all the resistive changes and programming power, the error bar plot in figure 3.7 shows the average resistance and the average deviation for devices of different sizes. The lines across the graph are expected values of the corresponding mode.

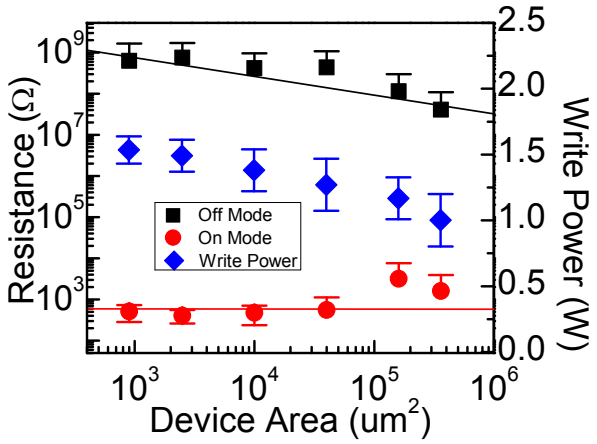

Fig. 3.7: Error bar presentation of on/off mode resistance for all the devices tested, average and the average deviation of each size is showed.

According to Schottky emission model, OFF state current should slightly increase as top contact size increases.[25] My test results show fairly similar behavior. The ON state resistance is expected to be the same for all sizes due to filament conducting mechanism which is discussed in chapter 6. The two largest devices seem to have little higher ON

state resistance than others. The average power required for all the devices is also shown, with slight drop of programming power as the top contact size increases.

3.3: Under Lower Current Compliance

The previous section mainly focuses on test results of memory devices in different sizes under the same current compliance of 100mA. However, with such high voltage and high current, the writing behavior resembles the well known and trivial electro-thermal breakdown.[11] Therefore, extra tests were done for the smallest 30×30 um^2 sized top contact devices under lower writing current compliances. The other purpose for this part of the experiment is to observe the WORM memory effect by reducing the power of the reading and writing processes.

In figure 3.8, the three figures are I-V sweeps in both OFF and ON states of the same device under 50μA, 1mA and 10mA respectively. The writing current compliance in plots (a) and (b) only limits the maximum current that can be read, not the actual

conductivity level of the LRS. In graph (c), the current never reaches the writing current compliance value because the LRS current does not normally go that high for this type of memory device. This concludes that the resistance switching mechanism for this particular WORM memory is not affected by the current density value. Therefore, reduction of the power for reading and writing process for this WORM device will most likely have minimal impact on its effectiveness.

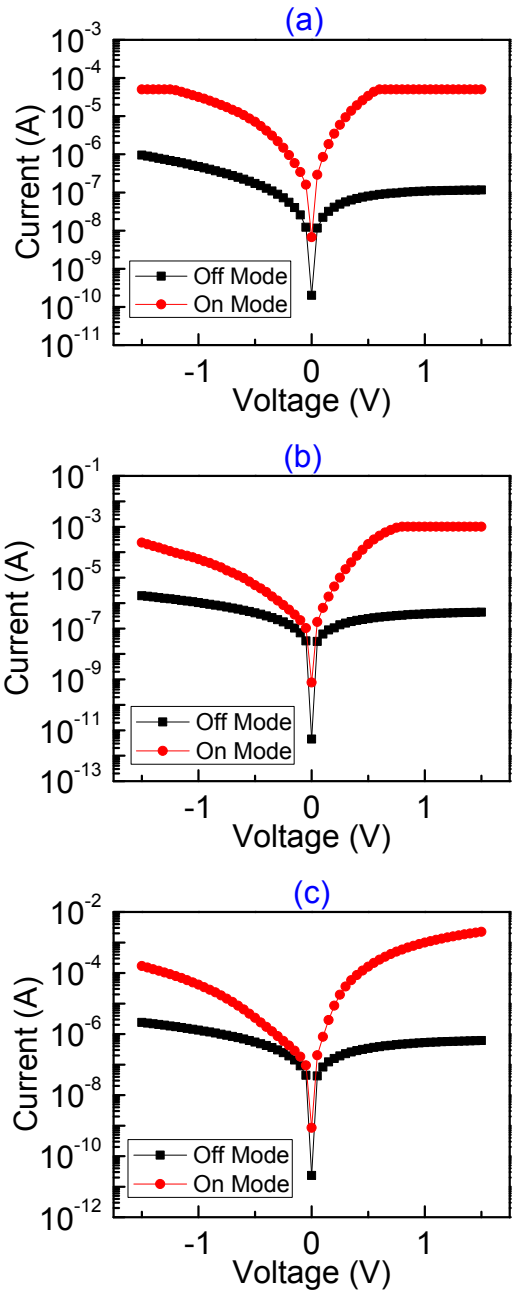

Fig. 3.8: (a) HRS & LRS with current compliance = 50μA. (b) Current compliance = 1mA. (c) Current compliance = 10mA.

The error bar graph shown in figure 3.9 verifies the conclusion made above. It shows the average and the deviation of both ON and OFF state resistance and writing power for all the devices that have been tested under various current compliances. The lowest writing power is around 1mW when current compliance is set to 50 μA. The R ratio for this one is lower than that written with higher power. However, the ratio is still around

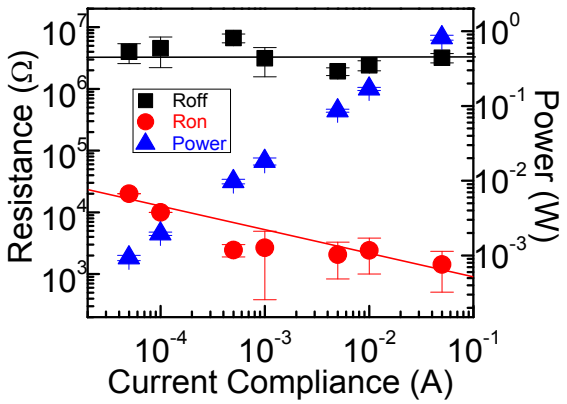

Fig 3.9: Error bar representation of LRS, HRS and power under various current compliance, 50μA, 100μA, 500μA, 1mA, 5mA, 10mA, and then 50mA.

10^3, which is large enough to distinguish the two different states. Both results from the 50 μA and 100 μA set current compliance show clearly lower R ratio than the others. According to the plot, at higher than 500 μA current compliance, R ratio for this type of WORM memory devices will not be limited by the current compliance level.

3.4: MgO Buffer Layer

In this section, the effect of the MgO atomic buffer layer that was deposited during the fabrication process is discussed. The purpose of the buffer layer in all film samples is to accommodate the lattice difference between ZnO and silicon in their

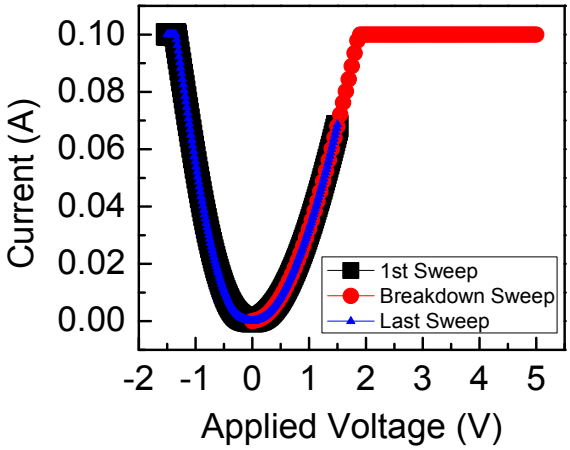

Fig 3.10: I-V curve of an Au/Ti/MgO/p-Si/Al layered device.

crystallographic structure. Any potential impact on the memory performance from this layer is undesired in my case. Ti square shaped metal contacts are deposited for a film consisted of only MgO/p-Si/Al for testing. Test procedure is duplicated exactly the same as described in the previous sections. I-V curves shown in figure 3.10 have no indication of any memory window between all the three different sweeps. Current reaches limit faster in the negative bias than positive bias. The breakdown attempt had current reached its set limit at around +2V with gradual linear increase, and it brought no different

between the 1st sweep (black color) and the last sweep (blue color). Therefore, the possibility that the MgO buffer layer may impact memory performance is eliminated here.

In conclusion, the results shown in this chapter indicate that the WORM devices have basic memory application capability, while OFF state and ON state can be clearly distinguished, writing voltages are also at a predictable range under 20V.

Chapter 4: Endurance, Retention and Thermal Stability

4.1: Endurance

The setup for this experiment is almost the same as mentioned in Chapter 3, with only the addition of Agilent 81104A pulse generator. Reading pulses with amplitude of 1V and period of 2μs with 50/50 duty cycle are constantly applied on the selected device from 1 reading cycle incrementally up to 10^8 cycles. "Sampling Mode" is selected in the Agilent 4155C semiconductor analyzer menu. After each increment of reading cycles, the current passing the device is measured at external bias of +1V. Both OFF state and ON state of the device are tested the same way.

Devices of all top contact sizes were put through endurance test. In figure 4.1, the six graphs are endurance test results from these devices. Current sample was taken selectively at certain reading cycle and shown as highlighted dots in the graphs. All six of them are showing steady current values for both ON and OFF states throughout the reading cycles of 1×10^8. Furthermore, R ratios were kept above 10^4 at the end of each test experiment. The similarities shown in each graph indicate that the endurance quality of the devices is independence of the top contact size. Overall, the results prove that

memory devices based on ZnO film can go through reasonable reading cycle without

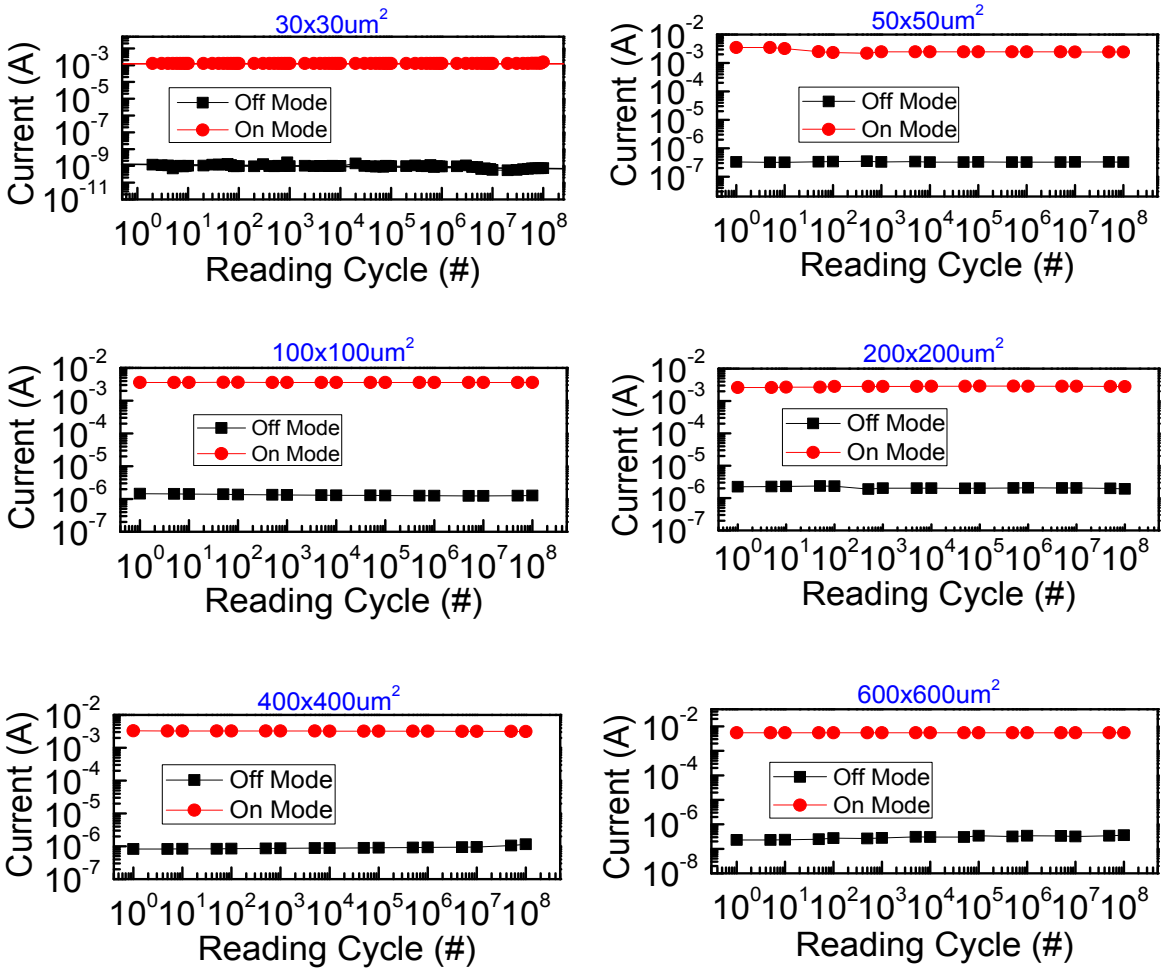

Fig. 4.1: Endurance of devices with various contact sizes, each point presents the current reading at 1V external bias after applying certain amount of reading pulses up to 10^8 pulses.

deterioration in their current conductivity.

4.2: Retention

The data stored in each device needs to be preserved for a significant amount of time as ideal WORM memory. Retention tests were done to find out the time period that the states stored in the ZnO WORM devices can preserve.

Semiconductor analyzer was set to "Sampling Mode" just like endurance test. A signal was sent into the analyzer from an external desktop computer. The signal is basically a command controlled by simple time counter software that tells the analyzer to

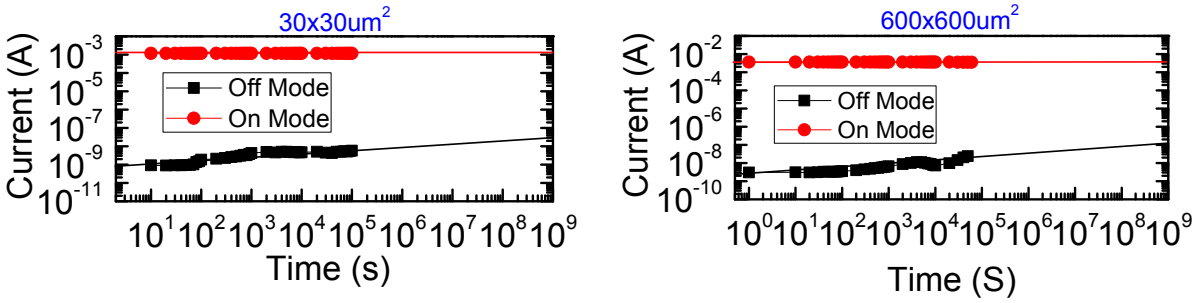

Fig. 4.2: Retention of a 30x30um^2 (left) device and a 600x600um^2 (right) device.

measure the current of the device at every 10 seconds, 100 seconds, 1000 seconds, and 10000 seconds until it's counted up all the way to 10^5 seconds. Currents were measured with voltage bias of +1V.

The deteriorating rate of resistance over time determines the retention quality of the devices on this sample. In both graphs of figure 4.2, ON state currents show no indication of dropping or rising within the 10^5 seconds testing period while slow current increase over time at OFF state can be observed. By using extrapolation method which is

also reported in other articles[12], following the current changing trend of both modes, R ratios after 100 years for those devices are still well above 10^4. The result showed here is a good proof that devices with such structure can be a descent candidate for long term information storage.

4.3: Thermal Stability

In the previous experiments performed under room temperature, WORM memory feature was found from the devices. However, at high temperature, electrons can gain thermal energy from the heat and thus the devices become unstable and leaky, which can cause the devices to have reduced electrical conduction.[13] To find out the memory performance dependence on temperature for ZnO WORM devices, Signatone Model S-1045 heat chunk was used to bake the device.

The setup for high temperature experiment was little different from room temperature experiment. Probe station and semiconductor analyzer were still connected

in the same way. Heat chunk was connected to the back of the device stage. High amplitude AC was applied on the stage by the heat chunk for heating purpose. Devices in HRS would be turned to LRS due to the high AC coming from the heat chunk. In order to block the AC, an electrical insulator with high thermal conductivity was placed between the sample and the stage. SiO_2 wafer was used for this purpose in this experiment. Another thin piece of copper sheet is place between the SiO_2 wafer and the device sample to ground the back contact. Device stage was also constantly discharged to prevent any current leakage to the surface of the SiO_2, because hot electrons and holes from high amplitude AC have the possibility to be injected into SiO_2.[14] An external thermometer was clipped together on top of the copper sheet with the stage for more accurate

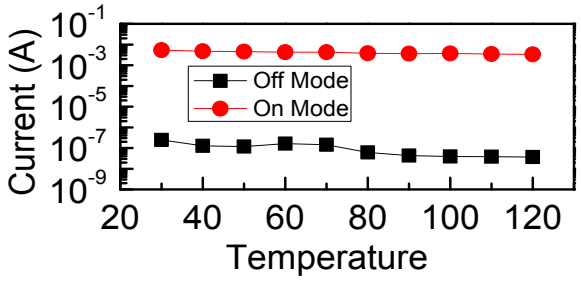

Fig. 4.3: Average current at 1V under temperatures from 30~120ºC and 120~30ºC.

temperature reading near the sample. The temperature feedback from the stage to the heat chunk is unreliable because thermal conduction does take some time.

Devices were swept exactly as in room temperature experiments for both OFF state and ON state using semiconductor analyzer. Voltage sweeping was taking every 10 ℃ with temperature both increasing from 30 ~ 120 ℃ and decreasing from 120 ~ 30 ℃.

The current averages at the reading voltage of +1V between the forward and reverse procedure were used to plot figure 4.3. The current drop is noticeable for OFF state, but can be hardly noticed for ON state. This means even at 120 ℃, the current leakage is still relatively small for both OFF and ON states. The R ratio actually increased slightly at higher temperature. No experiment with further increase of temperature was done because of the equipment limitation.

Endurance and retention experiments were also performed under high temperature with the exact high temperature setup as mentioned above. The device stage was heated

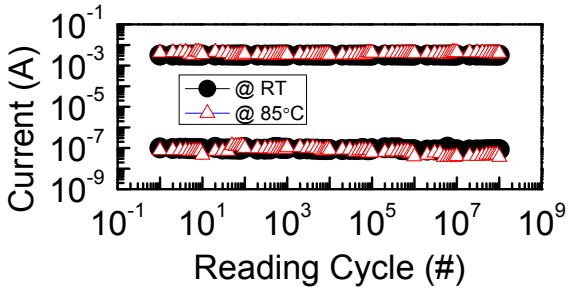

Fig. 4.4: Endurance of HRS and LRS under room temperature and high temperature at 85ºC.

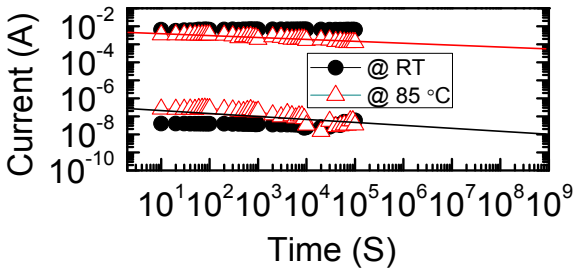

Fig. 4.5: Retention of HRS and LRS under room temperature and high temperature at 85ºC.

to a certain temperature until the thermometer near the sample reads 85 ℃. All procedures are exactly the same as in room temperature experiments with the sample staying at 85 ℃ the entire time.

Figure 4.4 and figure 4.5 are endurance and retention results respectively at 85 ℃ plotted together with the room temperature results of the exact same device. For the endurance, there is almost no difference between room temperature and high temperature

results. However, current drop can be clearly observed from the retention result at 85 ℃, which implies that at 85 ℃, devices will experience current drop over time, but the R ratio can still be clearly distinguished after extrapolated to 100 years.

Experimental results showed in this chapter conclude that the WORM devices do possess the read-many-times property without conductivity change, and resistance of those devices can be preserved for a long time. Under high temperature up to 120 ℃, no significant current drop can be seen, therefore, devices on this sample can be properly operated under 120 ℃.

Chapter 5: Top Contact and Substrate Effects

5.1: Metal-Semiconductor Junctions

The top contacts of all the devices are consisting of metal(s); metal-semiconductor junction is formed in between after depositing the metal(s) on top of ZnO semiconductor during the fabrication process. After photolithography, each top contact formed on the semiconductor can either be an ohmic contact or Schottky contact. Ohmic contact has linear I-V characteristic, and Schottky contact has rectifying I-V characteristic. The top contacts are Schottky contacts if the metals used to form the contacts have higher work function than ZnO as the left graph in figure 5.1 illustrates the work function of the metal $\emptyset_M$ and the semiconductor $\emptyset_S$ under the same vacuum level. If $\emptyset_M$ is smaller than $\emptyset_S$, then ohmic contact is formed. In order to achieve ohmic contact behavior, heavy doping on ZnO is required if the metal has higher work function, which is still under debate and it is not included in the experiment.[2]

At thermal equilibrium with no current flow, the Fermi level has to be constant throughout this metal-semiconductor system. Their Fermi level difference caused electrons in the semiconductor to lower their energy by traversing the junction. The charge caused by departure of electrons lowers the band edges of the semiconductor until

equilibrium is reached.[16] A potential-energy barrier is thus formed between the metal-semiconductor junctions. The barrier height $\emptyset_B$ is given by equation:

$$q\emptyset_B = q(\emptyset_M - \chi_S)$$

where χ_S is the electron affinity of the semiconductor, which is 4.35eV for ZnO,[26] and $\emptyset_M$ is the metal's work function, which is 4.33eV for Ti. The difference between the Fermi

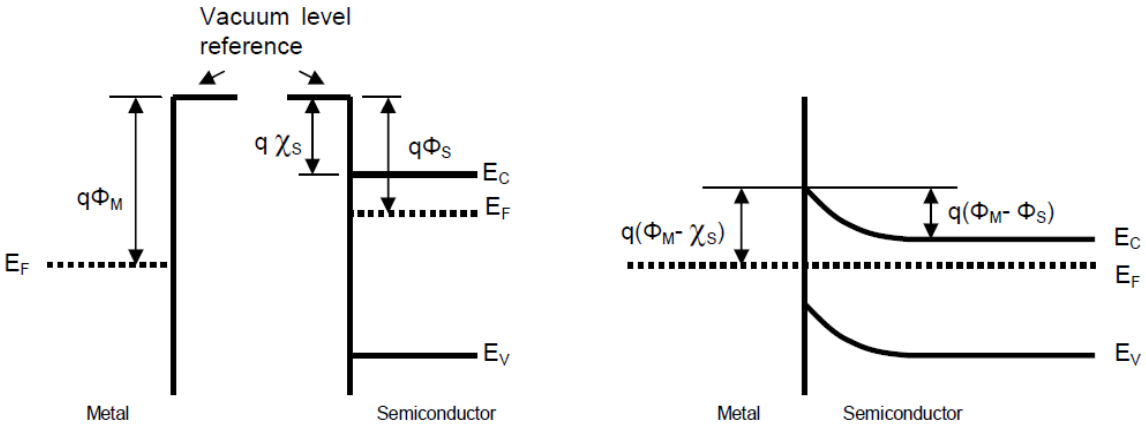

Fig. 5.1: Energy band diagram of metal-semiconductor junction with work function of $\emptyset_M > \emptyset_S$.[15]

energy of the metal and the semiconductor is defined as the built-in potential $\emptyset_i$ that can be represented by equation:

$$q\emptyset_i = q(\emptyset_M - \emptyset_S)$$

where $\emptyset_S = 4.35eV$ for ZnO. Built-in potential is also illustrated in the semiconductor side of the right image in figure 5.1. So with different metal material, the barrier height and build-in potential will also be different.

5.2: Ti and Au Top Contacts Comparison

In pervious chapters, Ti was used as top contact in the sandwich structure. Au has higher work function of 5.31eV, ZnO has work function of 4.35eV, and Ti has work function of 4.33eV. From the equations in the previous section, the potential-energy barrier and the build-in potential at equilibrium are higher in the Au/ZnO junctions than in the Ti/ZnO junctions. As mentioned in the fabrication chapter, Au was also deposited on top of the Ti materials as protection layer, and the metal-semiconductor junction is actually formed between Ti and ZnO. With higher barrier height, lower current reading at HRS should be observed in the devices with the Au top contacts. Devices were also

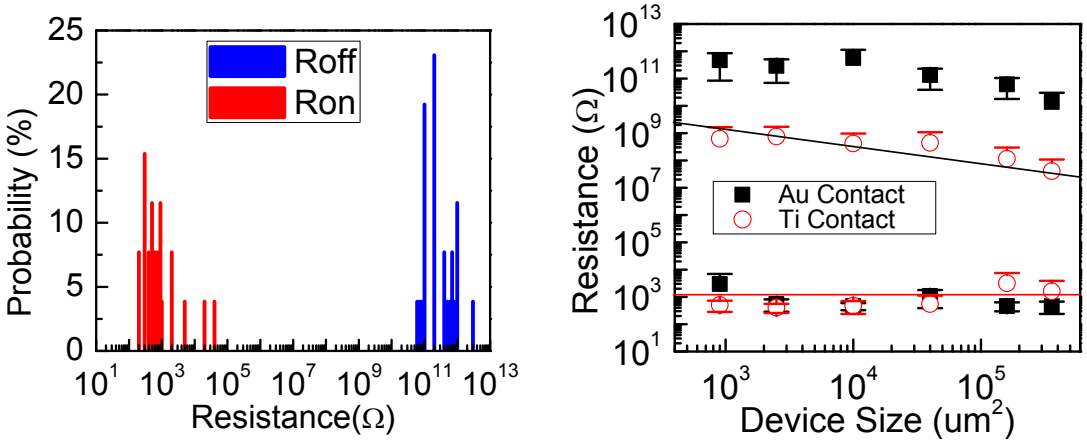

Fig 5.2: (left) HRS and LRS probability distribution for 30x30um² devices, (right) Error bar plot for HRS and LRS of all measured devices with Au top contact along with the comparison to the devices with Ti top contact.

fabricated using Au as top contact in Au/ZnO/p-Si/Al structure. All measurements were performed the same as Ti top contact devices, no experiment performed at high temperature.

Memory effect test has been done first. More than 100 devices in all six different sizes were measured. The results are show in figure 5.2. The left graph is probability of ON and OFF state resistances for the devices with area of 30x30um^2. Most devices had their HRS in the 10^{11} Ω range, and LRS in the 10^3 Ω ranges. The graph on the right is the error bar representation of all the devices. Devices of all sizes on the Au top contact sample all have their average HRS in the 10^{10}~10^{11} Ω range, and their average LRS in 10^3 Ω range. In comparison with the Ti top contact sample, this one has significantly larger R ratio. Both samples displayed the same trend of resistance drop in HRS as size increases, and their LRS fell into the same resistance range.

With such high R ratio on these Au top contact devices, this sample is definitely better than the Ti top contact sample on this part of the memory performance. As shown

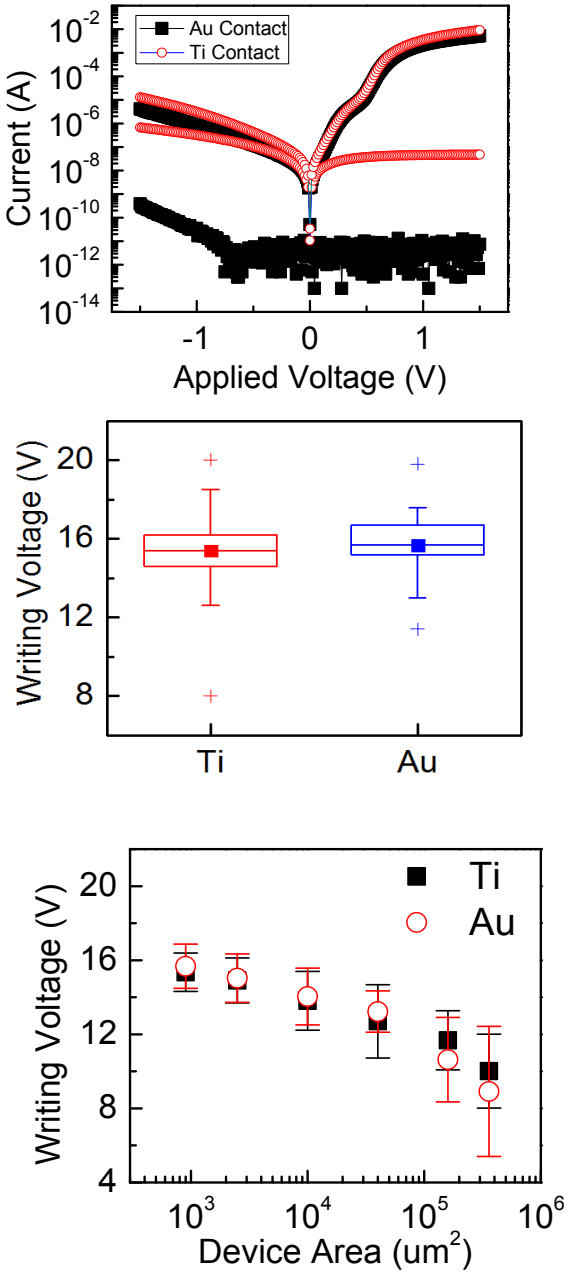

Fig 5.3: Comparison between Ti and Au top contacts (Top) I-V sweep from -1.5V ~ 1.5V of HRS and LRS 30x30um^2 devices (Middle) Box Chart representation of writing voltage for 30x30um^2 devices. (Bottom) Error Bar of writing voltage for all device top contact sizes.

in the top plot in figure 5.3, the HRS of the Au contact sample returned very low current after the -1.5V~1.5V sweeping comparison with the Ti contact sample. The LRS of those two samples are almost identical. Writing voltage of Au contact devices is similar to Ti contact devices, as the middle plot of figure 5.3 illustrates. The writing voltage box chart plot contains data from 30x30um^2 Ti and Au contact devices; the bars stick out from top and bottom of the box represent the 91st and 9th percentile of the overall date respectively, the top, middle and bottom lines of the box each represents the 75th, 50th, and 25th percentile, the center solid square is the mean, and the "+" signs are the maximum and minimum values. The range of the data fell closely for devices of both top contacts. Error bar plot at the bottom of figure 5.3 compares the average writing voltage and the average deviation for all top contact sizes between Ti and Au top contact devices. Majority part of the data from those devices overlap with each other, which indicate that the relationship between top contact area and writing voltage is similar between those two different devices. These results suggest that writing power maybe independent of the interface between metal and semiconductor

Room temperature endurance and retention tests were also carried out to find out

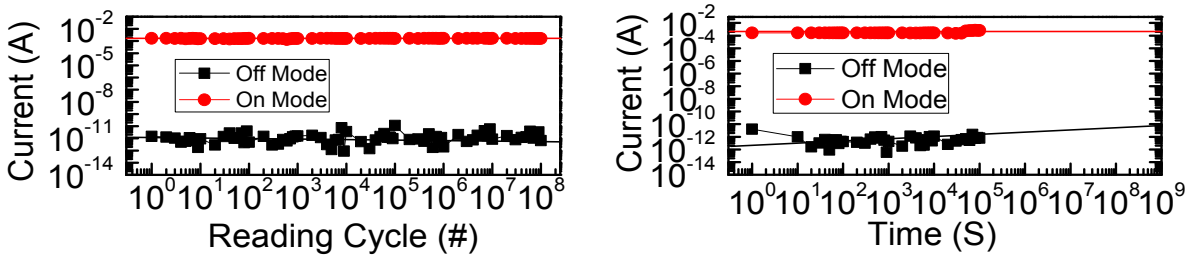

Fig. 5.4: (left) Reading pulse endurance test of the Au top contact sample, (right) retention test of the Au top contact sample up to 10^5 seconds (27.8 hours) and extrapolated to 10^9 seconds (100 years).

if these devices show any difference in the two areas. The endurance plot in figure 5.4 is done on a 30x30um^2 device. After 10^8 times of reading pulses, both currents of OFF state (HRS) and ON state (LRS) of the devices display very stable trend all the way through. Compare this device with the Ti contact device from one of the previous section, the difference still lies in their HRS. Same situation with the retention test of this Au contact sample was observed as it is shown in the right plot of figure 5.4, it displayed almost identical trend in the ON state as the Ti contact.

Au top contact devices theoretically and experimentally showed lower conducting current at HRS, the R ratio is definitely higher than that of devices with Ti as top contact, which can probably give the devices higher potential for lowering programming power; retention and endurance of the devices turned out to be stable throughout also.

5.3: ZnO/p-Si and ZnO/n-Si

So far only samples made using p-type silicon substrate were discussed. The different results from samples grown on p-Si and n-Si substrate are compared here in this section. ZnO was deposited on n-Si after few atomic buffer layer of MgO. Square shaped Au/Ti top contacts in six different sizes were also sitting on this sample as top contact after photolithography, and Al is evaporated to the bottom of the n-Si substrate as back contact. That makes this sample Au/Ti/ZnO/n-Si/Al structure.

The two plots in figure 5.5 are I-V curves for both OFF and ON states from two different devices on this sample. Comparing to the p-Si substrate device as shown in the

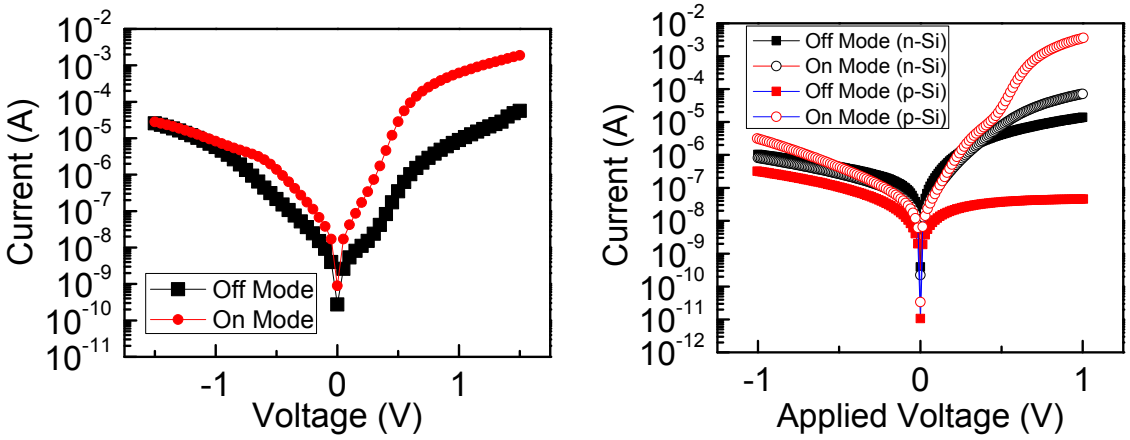

Fig 5.5: Both plots illustrate I-V curves of n-Si substrate sample swept under -1.5V~1.5V for both HRS and LRS, (right) plot also includes comparison with the p-Si substrate I-V curves.

right plot, the OFF state rectification ratio in devices on the n-Si substrate device is greater than the OFF state rectification ratio in the device on p-Si substrate. However for

ON state, it is the device on p-Si substrate that displays larger rectification ratio. This difference resulted in much smaller R ratio for the n-Si substrate device. In the above two graphs, the R ratio for n-Si substrate sample is only around 10^1~10^2 orders of magnitude, which is not ideally large enough for systems to tell the difference between these two modes.

In figure 5.6, the left plot is the writing voltage box chart plot of 30x30um^2 devices with both p-Si and n-Si substrates. The information contained in this graph has

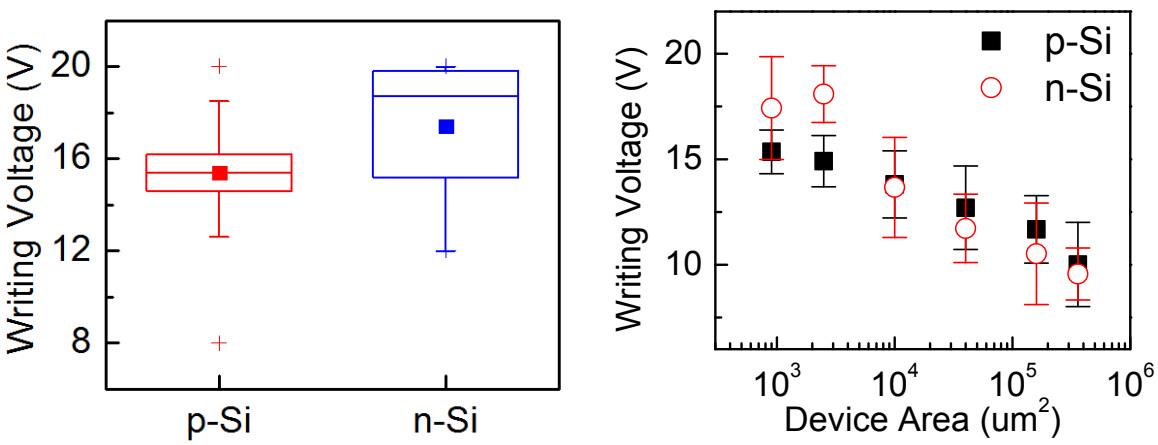

Fig. 5.6: Comparison of p-Si devices and n-Si substrate devices (Left) Writing voltage box chart for 30x30um^2 top contact devices (Right) Writing voltage error bar plot for devices of all top contact sizes.

the same format as described in the previous section 5.2. Although data percentiles are clearly different between these two different devices, data range was never above 20V. The error bar plot on the right side of figure 5.7 shows similar writing voltage range between these two different devices in all top contact sizes, both plots indicate that for

devices on either n-type or p-type Si substrate, the voltage required to turn devices from HRS to LRS is almost the same.

As illustrated in the error bar plot in figure 5.7, the average R ratios for devices of all top contact sizes on this n-Si substrate are all less than 10^3. The possibility of having devices with undistinguishable on and OFF state current is high. On the other hand, the p-Si substrate has much larger R ratio. The chance of having device with undistinguishable R ratio is none-existence from all the tests I have done so far. Therefore, the conclusion here is that ZnO material shows better memory properties deposited on p-Si substrate than on n-Si substrate.

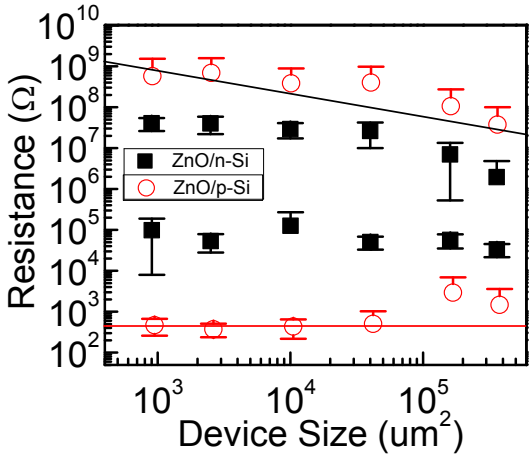

Fig. 5.7: Error bar plot of the n-Si substrate sample of devices with all top contact sizes alone with the comparison to the p-Si substrate sample.

Figure 5.8 shows band diagrams of ZnO on n-Si and p-Si substrates. With p-Si substrate, it forms a depletion region with the n-type ZnO, and when an electric field is

applied through the top contact, it acts like a diode connected in reverse bias, only very

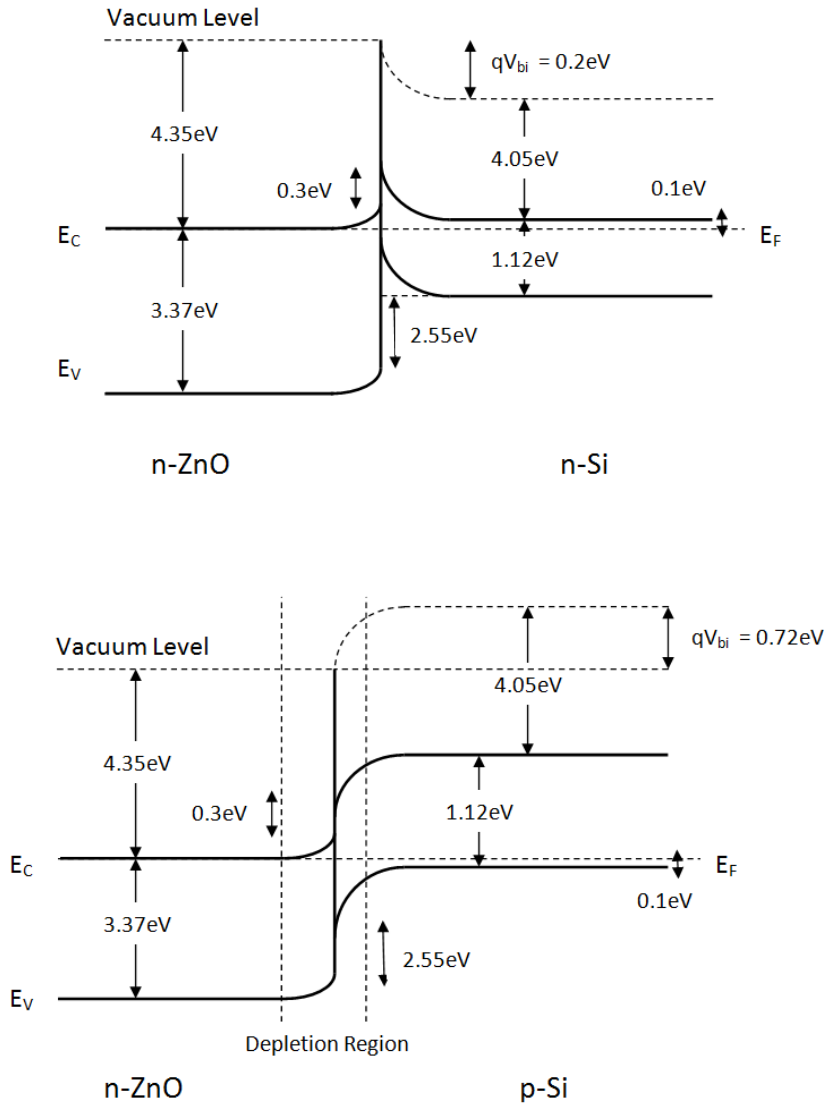

Fig. 5.8: Band diagrams of (top) ZnO on n-Si substrate, (bottom) ZnO on p-Si substrate. Assuming Fermi level of ZnO is at the conduction band.

small amount of current can pass through until breakdown voltage is reached. For n-type ZnO deposited on n-Si substrate, there is no depletion region in between the hetero-junctions. The built-in potential V_{bi} is also smaller in the n-ZnO/n-Si structure, and

electrons will be able to break through the barrier when the applied electric field gets stronger.

In conclusion, WORM devices showed good memory performance with both Ti and Au top contacts. Also, devices with p-type Si substrate are definitely much better WORM memory candidates than devices with n-type Si substrate mainly due to the R ratio between HRS and LRS.

Chapter 6: Resistive Switching Mechanism

6.1: Current Model Fitting

To further understand the device resistive switching from HRS to LRS in WORM type memory behavior, the I–V curves in both states were analyzed using theoretical models and fitted with those models to investigate the carrier transport mechanisms in the devices. The HRS I-V characteristic can be fitted in to the Ohmic model with the equation:

$$J = qn\mu V/d$$

Where q is the number of charges per carrier, n is the density of charge carriers, μ is the mobility of charge carriers, and d is the thickness of the film. I-V plot shown in the top plot of figure 6.1 illustrates that the HRS current is controlled by charge injection through the electrode. Two distinctive linear regions can be observed, the slope of the linear region changed dramatically once the polarity of the external bias is changed, this is due to depletion region formed between ZnO-Si junctions causing it go from forward bias to reverse bias.

At LRS, the I-V curve can be governed by the combination of ohmic and the space-charge-limited current (SCLC) model with the equation:

$$J \propto \frac{8\epsilon_i \mu V^2}{9d^3} + Vexp(-\frac{c}{kT})$$

where μ is the mobility of carriers , ϵ_i is the dynamic permittivity of the insulator and c is a positive constant independent of V and T.

The LRS ln(I) vs ln(V) is shown in the bottom plot of figure 6.1, three phases can be distinguished, and they are noted in the graph as ohmic, trap filling, and SCLC. During the Ohmic phase, when the electric field is still low, the number of injected electrons is smaller than that of the intrinsic free electrons and the current is depending on the applied field.[22] While the injected electrons are kept on increasing, the probability of these electrons getting captured by the traps in the bulk increases as well. This phase is at higher electric field than the ohmic region which can be recognized as the charge-injection-limited and trap-filling region.[23-24] As the applied electric field increases further and electrons still being inject from the

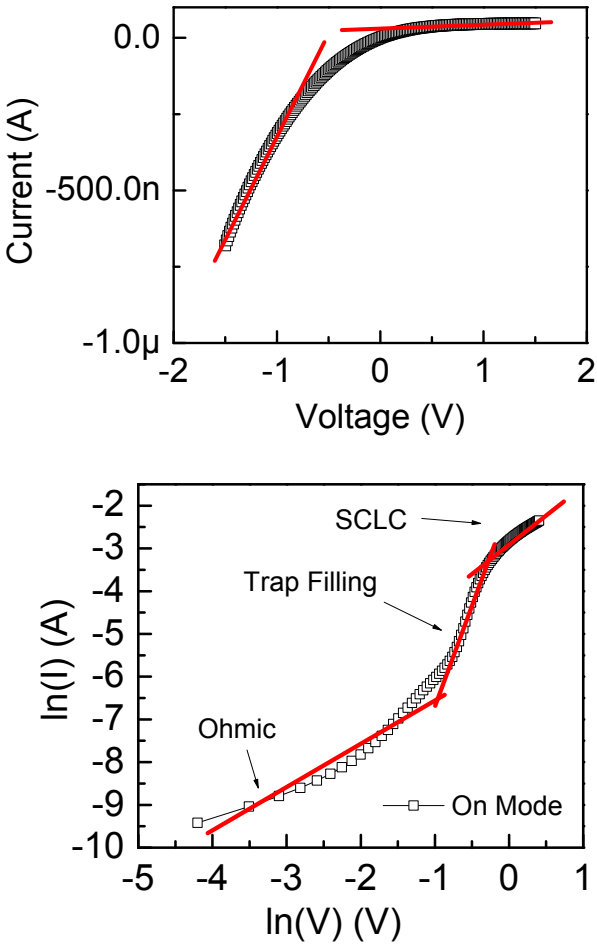

Fig. 6.1: (top) HRS I-V curve fitted with Schottky emission ON state, (bottom) LRS I-V curve fitted with space-charge-limited-current (SCLC) model.

electrode, more traps will be filled. This will cause the mobility of electrons to slow down, so extra injected electrons cannot travel to the bottom electrode at the rate as they have been injected. Therefore, space charge will start to build which will hinder further electrons injection. This is why the slope of the third linear phase which is the SCLC region is lower than the previous trap filling region.

6.2: Partial Reset Memory Feature

In this section, the test was done to make sure memory devices on the sample indeed have the write-once feature. After the devices have been set to ON state from OFF state, reset to OFF state is not desired for WORM type of memory.

Attempts to reset devices from LRS to HRS under different set current compliances have been done. Larger sweeping voltage from 5V ~ -5V then back from -5V ~ 5V was applied to devices at LRS. Each plot in figure 6.2 illustrates the results from the devices that went through this attempted reset process under each set current compliance. In the negative bias region of each device, a partial reset can be clearly

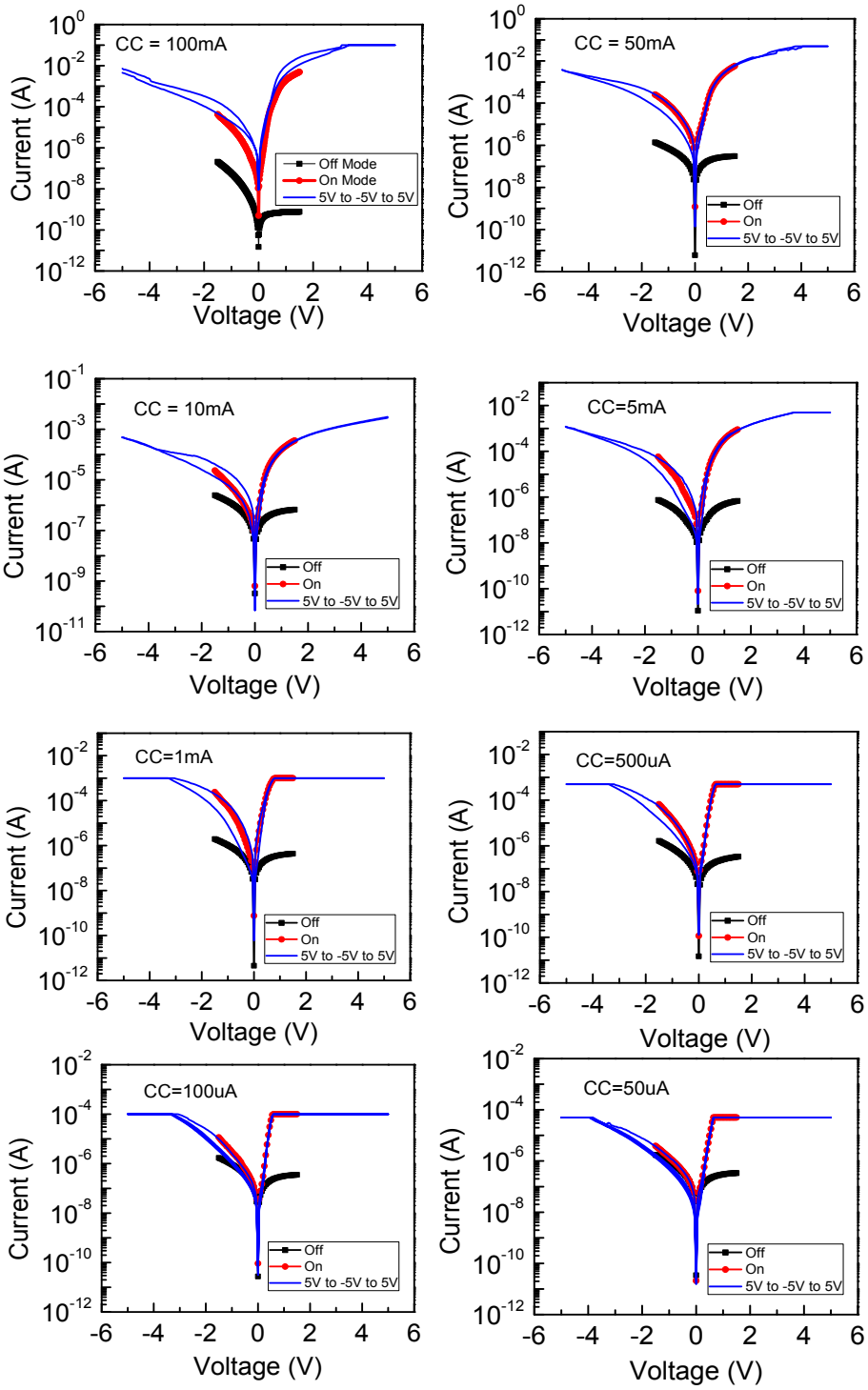

Fig. 6.2: on/off I-V characteristics and reset process (blue) under different current compliance

observed. Resistance was able to reset partially towards HRS except for the device with

CC = 50 μA where the negative bias on/off state resistance is almost identical. In the positive bias region of the figures, no device displayed any reset towards HRS at all. I-V curves for -5V ~ 5V sweeping loop never go below the current level of ON state I-V curves when the sweeping voltage reaches positive. The filament model describes resistive switching as the formation/rupture of metal filaments that exist within the device. In bipolar resistive switching, resistive switching is polarity dependent.[10] Apply positive voltage on the device will result in a set process from HRS to LRS, and whereas, apply negative voltage reset the device to HRS. The devices in my experiment showed voltage-induced bipolar behavior instead of current-induced unipolar behavior; the I-V curves for the attempted reset process are not linear when applied voltage is low, indicacting the formation of tunneling barrier at the MgO-Si interface during the writing process caused by the existance of a few MgO mono-layers. This barrier possibly prevents the device from being completely reset.[27] The conducting filaments were unable to be completely annihilated by the reset process. The plots in figure 6.2 also indicate that both WORM memory effect and resistive random access memory (RRAM) effect can coexist in one single device on the sample, although the on/off difference for the RRAM effect is less than one order of magnitude.

6.3: Conducting Filament

The mechanism of the HRS to LRS switching is discussed here. From several sections in the previous chapters, testing results revealed that for devices in HRS, current level went up linearly as the size of the device's metal contact increases, but LRS resistance stayed almost the same regardless the top contact size. While OFF state I-V characteristics can be understood as homogeneously distributed effect since resistance is proportional to the contact size, the ON state I-V characteristics for my case was most successfully explained as a confined, filamentary effect[10,17-18], which resistance is independent of contact size.

In this filament model, the switching between HRS and LRS is described as the formation/rupture of conducting filaments.[17-18] The sudden increase of conductivity due to formation of the conducting filament can be clearly seen in writing process plot like figure 3.3. At the threshold voltage, the conductivity of the device increased dramatically causing the operating current go up manifolds all the way to the set current compliance. Each device on the sample is similar to a heterojunction diode consisting of ZnO and Si substrate in OFF state, which leads to I-V characteristics resembling a diode. After the formation of conducting filaments in ZnO, the device became metal-semiconductor layered structure, while the top contact and conducting filaments acts as metal and the Si substrate act as the semiconductor part of the device.

For devices in LRS, resistance is attributed to the conducting filament density and diameter rather than to the geometrical size of the top contact, and all filaments of a device are confined within the geometrical size of the contact. However, my testing results do not suggest that the density and size of conducting filaments is dependent on the device contact size. The size of the conducting filaments formed during writing process directly affects the potential for future memory applications. Conductivity maps shown in figure 6.3 (a) and (b) indicates that a higher conductivity area is confined into a region about 5nm wide, which provides the information for the size of the conducting filaments and the potential for the scaling down the devices.

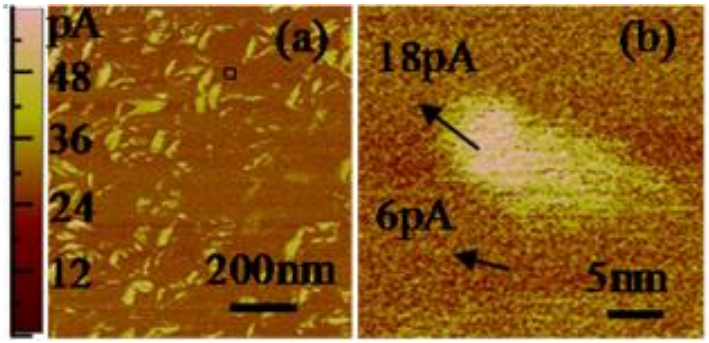

Fig. 6.3: (a) C-AFM image of the surface of ZnO thin film. (b) Line scan image across the selected black square area in (a).

6.4: Oxygen Vacancy and Bubble Phenomenon

Oxygen vacancies are most commonly reported defects in many ZnO related papers; oxygen vacancies may also contribute to ZnO n-type conductivity, but it's still under heavy debate.[2] During the fabrication process, there was no intention to control the oxygen vacancies population in the sample, because they are part of the conducting filament forming process, which is essential for conductivity switching in all devices. ZnO atom lacking the oxygen ion is pure Zn metal, which is highly conductive. The

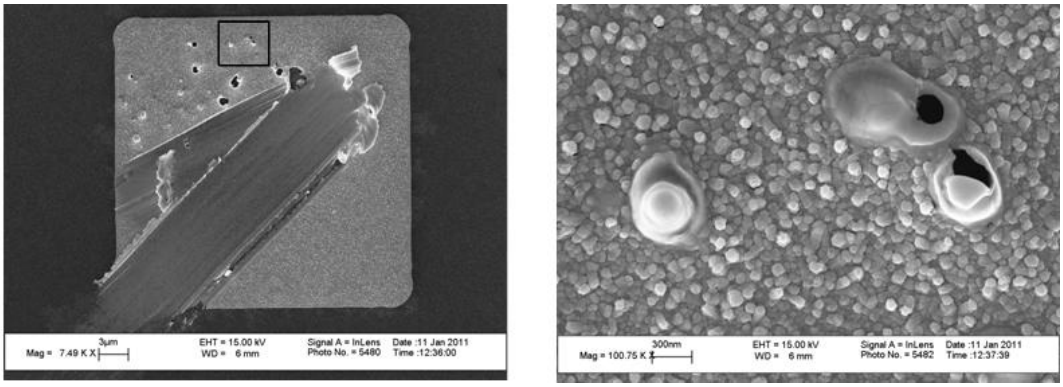

Fig. 6.4: (left) SEM image of an ON state device with gas bubbles on the surface of the top contact, (right) Magnified image after scanning the selected black square area in the (left) imagine.

extreme case can be that the oxygen vacancies align compactly along the Zn filament making the conducting filament completely metal.[19]

Oxygen gas bubble phenomenon is observed during my experiment with the devices, which indicates that the filaments are composed of oxygen vacancy. The top contact materials and majority carrier concentration of the Si substrate do not play any role in altering the result. All samples appear to have devices with oxygen gas bubbles at

the surface of the top contact after breakdown process; there is about half of the chance that devices do not turn out this way.

The gas bubbles appeared after device has switched to higher conductive state can be related to the formation of conducting filaments. Since conducting filaments are extended defects in insulating ionic crystals, on application of electric field, charge trapped in those existing aligned defects can overcome the defect potential and cause the filaments to conduct current. The defects are reported to be alignment of the pre-existing oxygen vacancies, Zn interstitials, and Zn dislocations during formation process.[10] The left SEM image in figure 6.4 is the top surface view after the breakdown process. The device in the image is at LRS. The right SEM image shows a closer look at the bubbles.

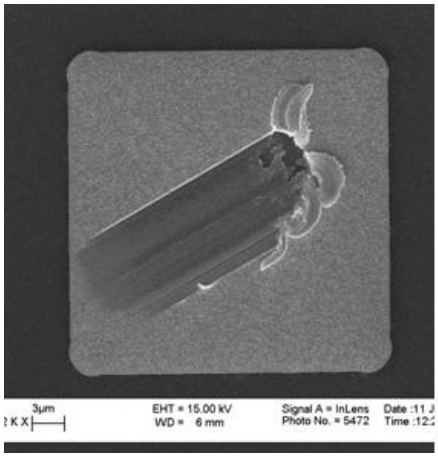

Fig. 6.5: SEM image of an ON state device without gas bubbles on the surface of its top contact.

The production of oxygen gas is due to the oxidation reaction happened during the writing process. This redox process can be considered as anion-migration cells, realized mostly with transition metal oxides like ZnO as the insulator, which electronically

conducting paths of sub-oxides are formed and removed by local redox processes.[17] Bubble phenomenon caused by redox reaction during conducting filament forming process is also reported from other people's experiments.[20]

The problem with oxygen gas bubble is that it will limit the scaling down potential of the devices. SEM image in figure 6.5 shows a device in LRS without any gas bubble on its top contact surface. About half of the time, devices will not have bubbles or holes, and the devices are still able to conduct current as LRS upon the application of electric field. A similar case to this bubble phenomenon is reported as pinhole phenomenon formed after application of high voltage and caused extra leakage of current.[21] However, the pinhole phenomenon reported was an extreme case of oxygen deficiency. Although both phenomena have the same behavior of current leakage, but in my case, the bubbles/holes are not always the sign for higher current conduction.

Chapter 7: Summary

WORM memory devices fabricated using n-type ZnO thin film on p-Si substrate utilizing molecular beam epitaxial growth technology have shown excellent memory performances and long term storage abilities. The programming voltage required to switch from OFF state to ON state takes between 12V~20V, the current required can be as low as 50μA. On/off state resistance ratio is mainly in the range of 10^5~10^6 and average above 10^4 for all tested devices. Nonvolatile properties including retention can be extrapolated to100 years while still retaining the same R ratio. Reading endurance tested up to 10^8 cycles reading cycles with pulses of 1V amplitude showed almost no change in resistance at all for both modes. Devices are write-once memories that cannot be reset by any applied external bias after set to ON state, which makes these devices permanently non-editable memories. Plus, all those good qualities shown through the test results can also be sustained at higher operating temperature up to 120 ℃.

Weaker memory performance is found in memory devices with n-type ZnO thin film on n-Si substrate, which the R ratio is clearly lower than devices with p-Si substrate. Ti material exhibited to be a good top contact for such structured WORM memory devices, and devices with Au material as top contact could potentially have higher R ratio.

Conductivity maps for the surface of ZnO thin film and morphology change of the

contact area for ON state devices illustrated that conducting filaments consisting of oxygen vacancies are responsible for the conduction mechanism. Therefore, conductivity of devices is independent of the top contact area; giving the devices higher potential for size scaling down.

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