UNIVERSITY OF CALIFORNIA,
IRVINE

The CMOS Integration of a Power Inverter

THESIS

submitted in partial satisfaction of the requirements
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by

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2016

Dedication

To

my parents and friends

for their love and support

my professors and teachers

for the light of knowledge they provide

We are whirling through endless space with an inconceivable speed. All around us everything is spinning, everything is moving, everywhere is energy. There must be some way of availing ourselves of this energy directly. Then, with the light obtained through the medium, with the power derived from it, with every form of energy obtained without effort, from stores forever inexhaustible, humanity will advance with giant strides. The mere contemplation of these magnificent possibilities expands our minds, strengthens our hopes, and fills our hearts with extreme delight.

Nikola Tesla

A new scientific truth does not triumph by convincing its opponents and making them see the light, but rather because its opponents eventually die.

Max Planck

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Acknowledgements

The work within this thesis, except where noted, represents work that is my own.

Abstract

CMOS Integration of a Power Inverter using a Novel Bused Switched-Capacitor topology

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Due to their falling costs, the use of renewable energy systems is expanding around the world. These systems require the conversion of DC power into grid-synchronous AC power. Currently, the inverters that carry out this task are built using discrete transistors. TowerJazz Semiconductor Corp. has created a commercial CMOS process that allows for blocking voltages of up to 700 V, effectively removing the barrier to integrating power inverters onto a single chip. This thesis explores this process using two topologies. The first is a cell-based switched-capacitor topology first presented by Ke Zou. The second is a novel topology that explores the advantage of using a bused input-output system, as in digital electronics. Simulations run on both topologies confirm the high-efficiency demonstrated in Zou's process as well as the advantage the bus-based system has in output voltage levels.

1 Introduction

Renewable energy technologies have long been a focus of research that is finally coming to fruition. In the coming years, renewable energy will replace fossil fuels as the dominant source of energy in many countries. In 2015, renewable energy systems represented two thirds of all new energy capacity installed in the United States [1]. While much of this installation is utility scale, the falling costs of solar panels, fuel cells and battery storage systems are allowing once traditional consumers of energy to install on-site generation capacity. This paradigm shift leads to many challenges for power systems built with the intention of one-way distribution of energy. Though these challenges are a subject of intense research, this thesis will only focus on one particular problem: DC/AC conversion.

1.1 Integration of Distributed Renewable Energy

The falling costs of residential and commercial scale renewable power generation is leading to a proliferation of small renewable generation systems (<10kW) [2]. Whether these systems are fuel cells, photovoltaic or wind based, they will, at some point, require conversion to a grid-synchronous AC waveform. This necessitates power electronics that can complete this task with high efficiency.

Power inverters for these applications tend to be large and expensive. One reason for this is the use of discrete transistors that are able to block voltages upwards of 120 volts and currents over 100 amps, for relatively small residential scale systems. These systems also tend to have fairly large inductors. With cost and size as barriers to wider implementation, it is

important that the power density of these devices be increased. Integration with modern CMOS manufacturing techniques is one possible answer that addresses these two concerns.

1.2 Current Converter Topologies

Medium-power applications (1 to 100 kW) for inverters almost universally use a topology with switches and inductors to convert from DC to AC in 1 or 3 phases. These systems are found in residential, commercial and utility scale applications and are based on mature technologies. Very low-power converters, such as those used in switching power supplies for cell phones and laptops, tend to use switched-capacitor (SC) topologies because of the ease of miniaturization of transistors and capacitors. For this reason, SC networks represent the best path towards CMOS integration of power inverters. Much of the research into SC topologies at higher power levels tend to use discrete components because of mature medium-voltage transistor technologies [3] [4].

1.2.1 Traditional Inverter Design

Typical power inverters use an inductor-based circuit topology such as the one shown in Figure 1.1 [5]. This common topology is also known as an H-bridge and is found in many

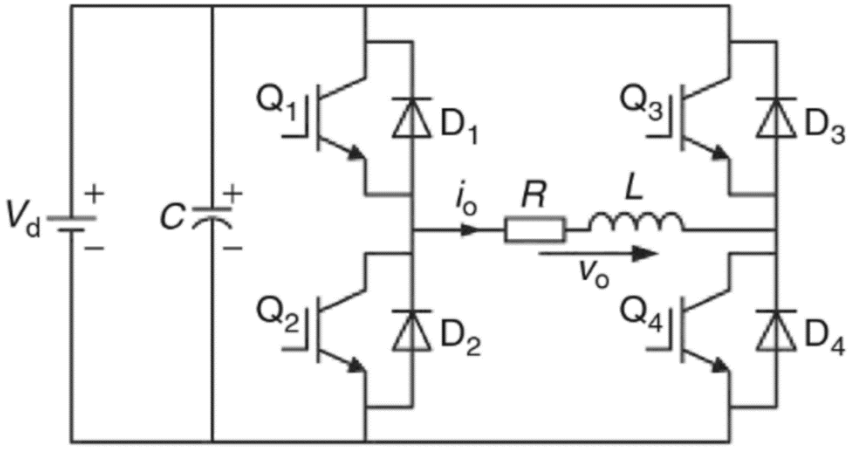


Figure 1.1 Typical AC/DC inverter topology with an inductor *[5]*

applications, including being paired with switched converters. The inverters feature discrete transistors (generally IGBT or MOSFET) in medium-power applications [5]. Though this may allow for on-chip integration, they rely on inductors and capacitors for current and voltage smoothing. Specifically, it is the large power inductors (~100 mH with a sufficient amperage rating) that make these topologies difficult to miniaturize.

Despite this, familiarity with the H-bridge topology, high efficiency and technological maturity make them pervasive in power electronics systems at all levels. Work towards miniaturization of these types of topologies tends to focus on high-frequency switching because of the ability to use smaller inductors at higher frequencies [6]. The work presented in [6] was able to reach 98% efficiency at a switching frequency of 50kHz. This is definitely above the norm, as most inverters using a variant of this topology tend to have efficiencies in the 92%-95% range [7] [8].

1.2.2 Inductor-less Inverter Design

Power converters require energy storage components to work properly. Because inductors tend to be large, one alternative to using them in inverter design is to use a switched-capacitor network. With CMOS integration in mind, it must be noted that, with current technologies, the capacitors for a larger power converter must be off-chip. This is because on-chip capacitors have low operating voltages (usually less than 5 V) and small energy storage capability (measured in picofarads). Despite this, even large capacitors are smaller elements than inductors at the same power level, lending themselves to miniaturization much more easily.

Switched-capacitor inverters use the principle of charge sharing to transfer voltage from an input to an output. By switching their configuration between parallel (charging) and series (discharging) the capacitor network is able to create voltage levels that are discrete multiples of an input voltage. Figure 1.2 shows the effects of charge sharing on a SC system (assuming both capacitors have the same capacitance and the system is lossless). On the left, the first capacitor is charged to voltage *V* and the second is left uncharged with 0 volts across it.

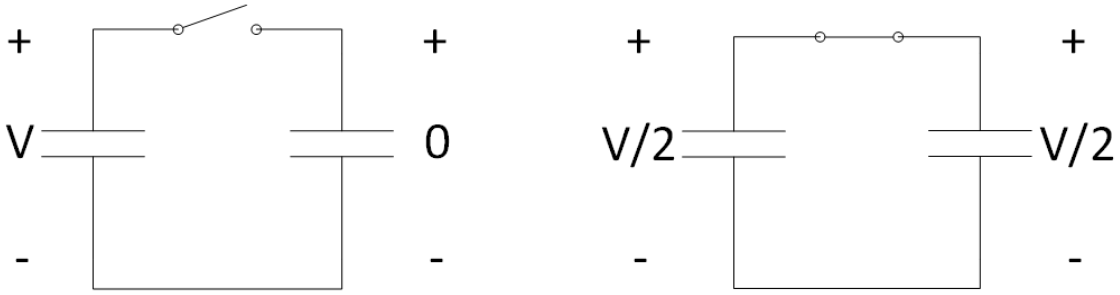


Figure 1.2 A demonstration of charge sharing between two capacitors

The total energy in this system is:

$$E = \frac{1}{2}CV^2 + 0 = \frac{1}{2}CV^2$$

After the switch is closed (neglecting transients), the conservation of charge dictates that the final voltage on each of the capacitors is $V/2$ (as shown on the right of Figure 1.2).

The total energy in the final state is:

$$E = \frac{1}{2}C\left(\frac{V}{2}\right)^2 + \frac{1}{2}C\left(\frac{V}{2}\right)^2 = \frac{1}{4}CV^2$$

This means that, without any other sources of loss, a SC system will lose energy through charge sharing that is proportional to the total change in the voltage squared. Because of this, it is very important to use zero voltage switching (ZVS) techniques in SC systems.

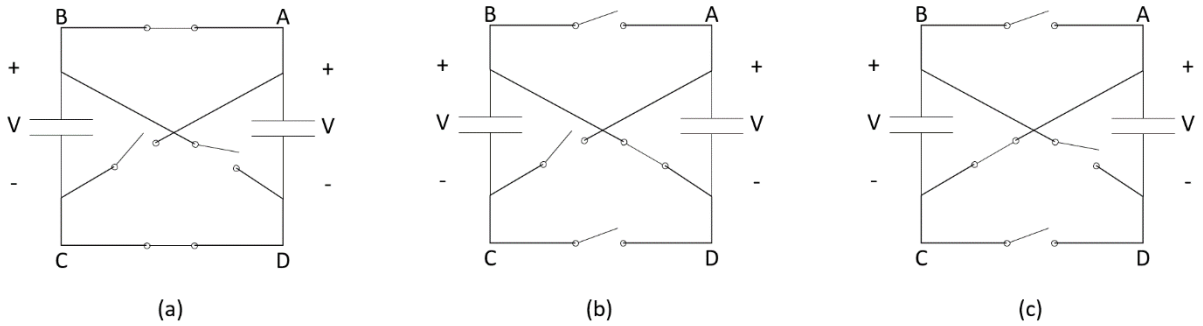


Figure 1.3 [a] Capacitors charging/Node AC = -DB = V [b] Node AC = 2V [c] Node DB = -2V

Figure 1.3 shows three configurations for a generic switched-capacitor network. Figure 1.3(a) shows the parallel configuration for charging. If additional switches are added for controlling the output, this configuration can also output voltage *V* (across nodes A and C) or -*V* (across nodes D and B). The configuration in Figure 1.3(b) shows the capacitors switched in series and outputing a voltage of 2*V* across nodes A and C. In Figure 1.3(c) the capacitors are again connected in series. However, this switch configuration will output a voltage of -2*V* across nodes D and B. In this way, a SC network can be used to output multiple voltage levels (both positive and negative). With proper sequencing, the switches allow the capacitor network to act as an inverter.

1.3 Multilevel Switched-Capacitor DC/AC Inverters

It is these multilevel converters that are an excellent starting place for integrating power electronics into the CMOS process. They have advantages over traditional two level converters; specifically enabling high-voltage outputs from medium-voltage transistor technology [9]. Furthermore, these systems allow for the control of voltage, phase angle and real and reactive power flow without the use of transformers [10]. These features also make them an excellent choice for integrating distributed energy systems with the grid.

Several topologies have been developed with CMOS integration in mind. In particular, a CMOS transmission gate-based SC converter was demonstrate based on a theoretical high-voltage CMOS process technology that did not yet exist at that time [11]. This topology was formalized and a variant was proposed in [12] as a cell-based SC converter. It is this converter that will serve as the starting point for CMOS integration in this thesis. Other switched-capacitor inverters of note are a cascaded H-Bridge converter and a SC inverter using series/parallel conversion [10] [4].

1.3.1 Cell-based Switched-Capacitor Inverter

Figure 1.4 (a) and (b) show half-cell and full-cell stages, respectively, for the DC/AC inverter proposed by Zou et al [12]. These stages contain a capacitor and the switches necessary to connect it either in parallel (for charging) or series (for discharging) with other stages in the converter. By connecting half-cells in series, an (*N*+2)-level inverter for *N*

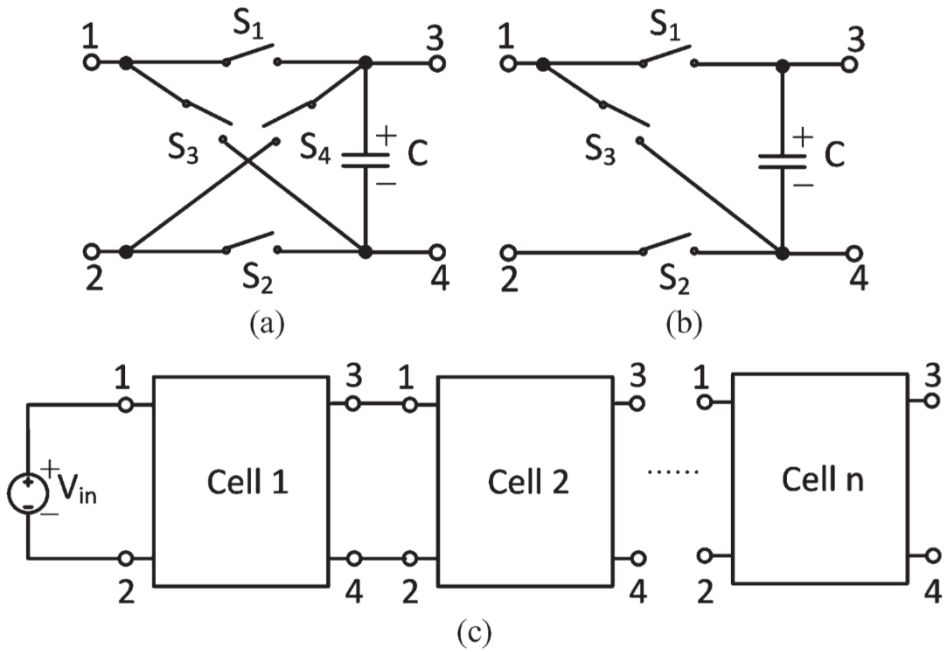
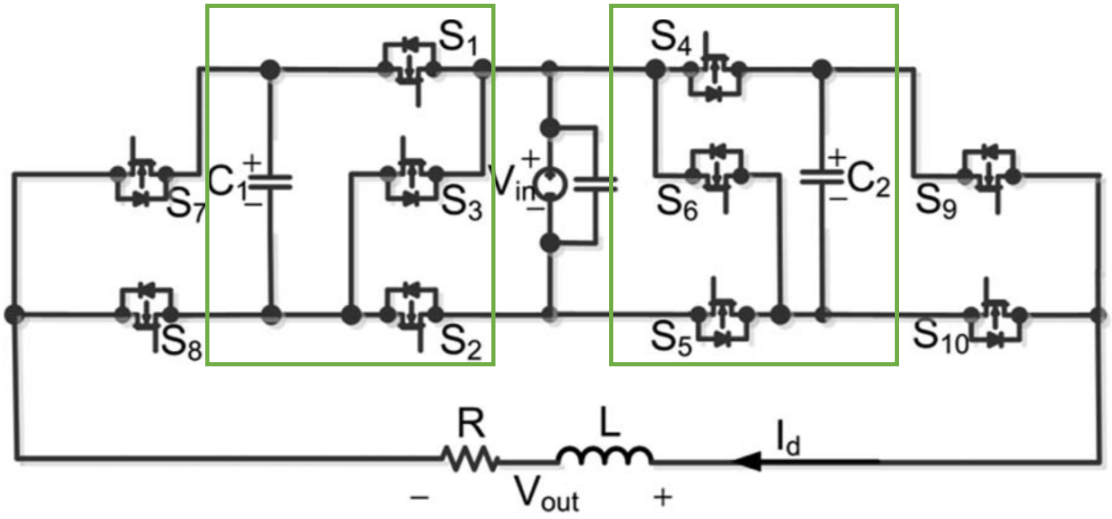


Figure 1.4 [a] full-cell [b] half-cell [c] series connection of cells *[12]*

capacitors (including the input capacitor) can be realized. A series of full-cell stages would realize a (2*N*+1)-level inverter.

A 5-level half-cell SC inverter was designed and tested in [12]. The converter schematic is shown in Figure 1.5 and consists of two half-cell stages placed on either side of the input with additional transistors at the end of each stage for output control. One possible weakness of this inverter topology is the lack of isolation between input and output; under the switch configurations for which $V_{out} = \pm V_{in}$, the output is connected directly to the input. This gives rise to the possibility of having transients from the input side of the converter pass to the output side without proper filtering. Another possible weakness is the large number of transistors in series, especially for a larger number of stages in series.

This circuit was simulated at 20kVA and experimentally verified at 1 kW. By adjusting the switching frequency to take advantage of stray loop inductance, zero-voltage switching was achieved. The efficiency of the system was found to vary between 92% and 96% over a range of 0.2 to 1 kW with a peak near 0.4 kW. At 272 W, the system had an output voltage of 58.74 V_{rms} and an output current of 5.38 A while driving a 9.4Ω and 17.4mH load (power factor of 0.83). Additionally, the system had a total harmonic distortion (measured to the 40th harmonic) of 4.98% [12].



Another multilevel SC converter designed with distributed generation applications in mind is the cascaded H-Bridge. Each of the capacitors is connected to an H-Bridge, which are then cascaded as shown in Figure 1.6. This inverter topology was introduced by F.Z. Peng as a method of connecting renewable energy systems to the distribution grid for transformer-less VAR compensation and voltage regulation [10] [13]. The cascaded H-Bridge inverter achieves 2*N*+1 voltage levels with *N* capacitors.

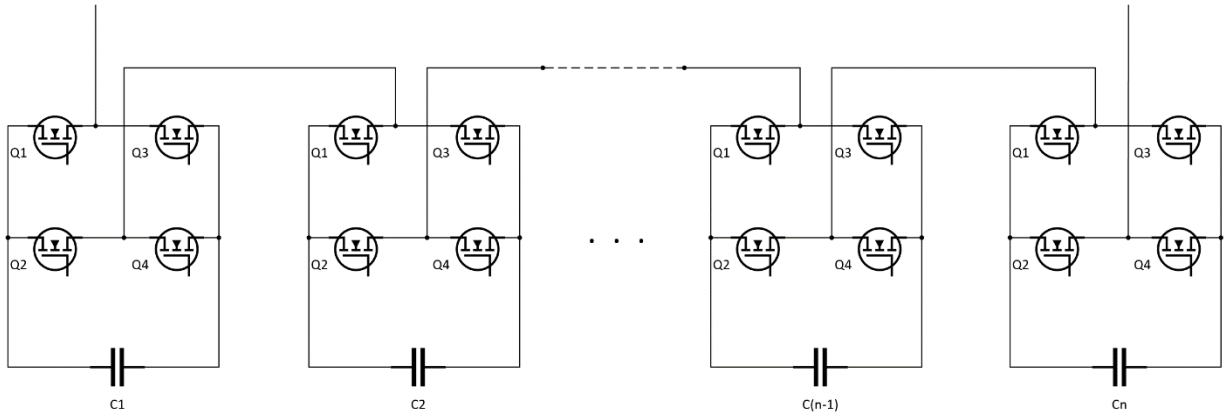


Figure 1.6 Multilevel cascaded H-Bridge inverter (charging network not shown)

Cascaded H-Bridge topologies have also been refined to minimize the number of components while maximizing the number of voltage levels. One such example was created by connecting a SC front end with an H-Bridge backend [14]. This converter is specifically designed as a high-frequency AC source for grid-connected photovoltaic networks and electric vehicle applications. The efficiency of this inverter is reported in [14] as 83% “over a wide range of output current.” Figure 1.7 shows a 9-level version of the inverter.

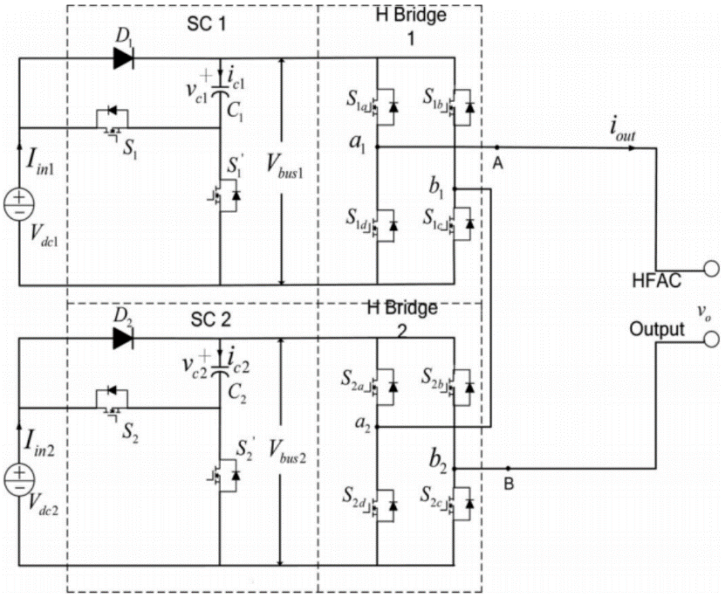


Figure 1.7 A 9 level hybrid switched capacitor H-Bridge inverter *[14]*

1.3.3 Series/Parallel Conversion

A third multilevel inverter topology uses series/parallel conversion of the capacitor network, already partially demonstrated in the front end of the hybrid SC H-Bridge. First proposed by Y. Hinago in 2010 and refined over several papers, this converter topology was created using a Marx inverter structure coupled with an H-Bridge to reduce the number of switching devices [4] [15].

This type of inverter, shown in Figure 1.8, is able to achieve 3*N*+1 voltage levels with *N* capacitors courtesy of the H-Bridge output. A 7-level inverter was tested in [4] and shown to have an efficiency of about 85%. One especially novel aspect of this topology is its relevant application towards both low-power and medium-power applications. The topology described in [4] was simulated at 5.7 W and 4.6 kW to prove its efficacy. A possible drawback of this inverter is the large number of series switches between the capacitors and the output.

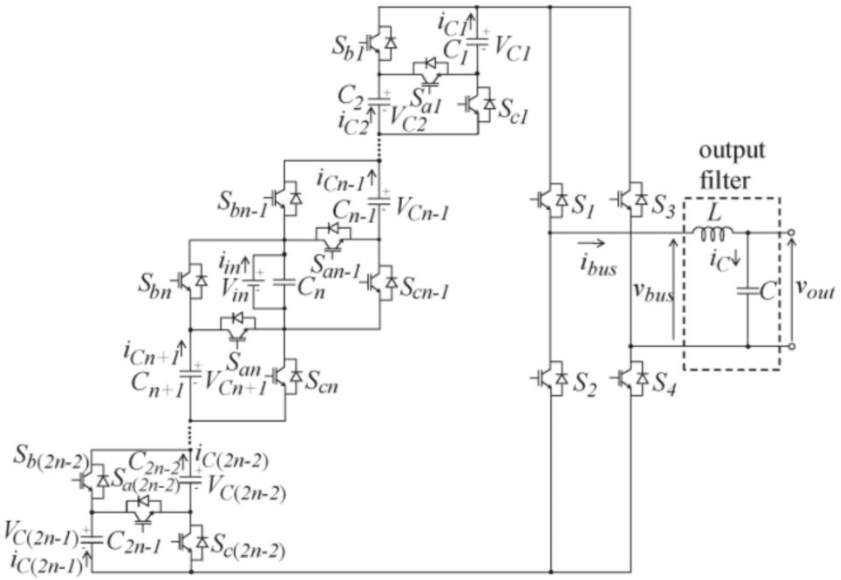


Figure 1.8 Switched Capacitor converter using series/parallel conversion *[15]*

1.4 Control methods

The large number of switching devices in multilevel converters lends an inherent level of complexity in controlling these converters. Because of this, the development of control methods for multilevel converters has become a popular topic of research. There are many different techniques for controlling these converters and many of them can be extended to SC inverters. Two primary sets of techniques are pulse width modulation (PWM) and space vector modulation (SVM).

PWM strategies for an *N*-level inverter involve *N*-1 triangular carrier waves overlaid on an input reference signal. The switches are turned on and off based on how the reference signal overlaps with the carrier signals (Figure 1.9). PWM techniques are fairly well established for SC inverters, though they may need to be adapted to a particular topology that is being used [16].

The explanation in [16] offers an excellent source of information on the various PWM methods which will not be covered more in-depth in this thesis.

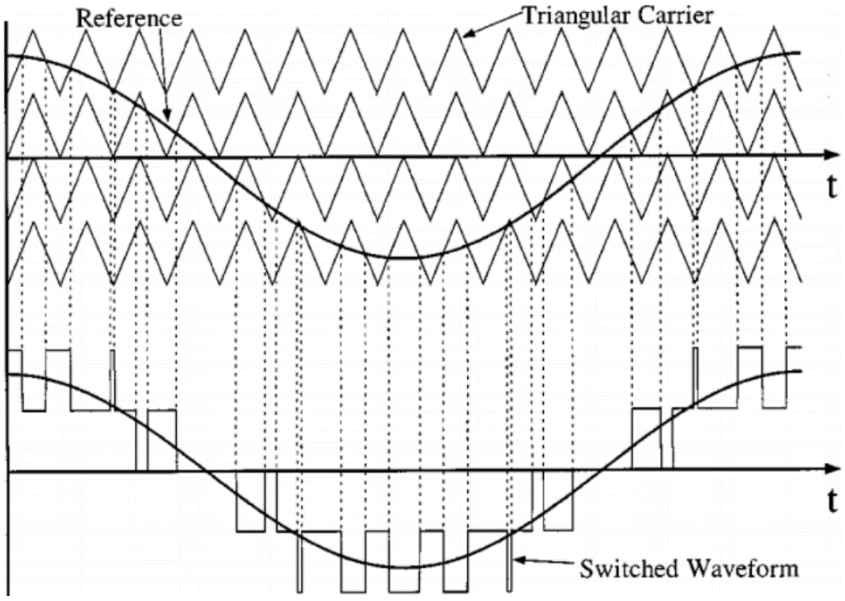


Figure 1.9 PWM control for a generic 5 level inverter *[16]*

SVM strategies take the reference voltage and represent it as a vector to be generated by the power converter. All of the switching states of the converter produce discrete output voltages that are then matched with the corresponding reference vectors. SVM techniques are superior to PWM methods in that they offer more control for capacitor load balancing and ripple voltage control in SC converters [17]. Until recently, they have also been more computationally complex. The previous study represents a good source of information on SVM techniques that will not be further developed in this paper.

Chapter 2 introduces the TowerJazz process and the integration of the half-cell inverter using this process. This chapter describes the simulation methodology and presents the findings. Chapter 3 presents a new inverter influenced by digital design. The results of the simulations of this inverter, using the methodology presented in Ch. 2, are also presented.

2 Integration with CMOS

As mentioned in Chapter 1, power inverters are large devices; even a relatively low-power (e.g. 1 kW) switched-capacitor inverter may need over half a square foot of circuit board to fit the components [12]. This footprint is primarily due to the size and spacing of the transistors to provide adequate heat dissipation of the IR^2 losses. The high-voltage also factors into the footprint of the board. This is one of the reasons that using the CMOS process has had difficulty with high-power integration. For typical residential applications, the output voltage needs to be 120 V_{rms} or 208 V_{rms} whereas CMOS typically operates nearer to 5 V_{rms}. This has so far necessitated the use of discrete transistors that could handle the blocking voltages and higher currents required for this application.

The idea of integrating high-voltage electronics onto CMOS has been a research topic for the last few decades [18]. In the late 1980's, researchers developed Laterally Diffused MOSFET (LDMOS) transistors with operating voltages near 500 V [19]. More recently, high-voltage CMOS processes have begun to move from theory to practical application. Cambridge Semiconductor created a 700-V lateral IGBT that was constructed using a 5-V 0.35 µm bulk CMOS technology [20]. Another process was developed by TowerJazz Semiconductor Corp. that integrated 700-V LDMOS and JFET transistors onto a 1.8-V and 5-V 0.18 µm CMOS technology [21]. It is the TowerJazz technology that will be used to explore CMOS integration within this thesis.

2.1 The TS18UHV Process

TowerJazz has developed several different processes with high-voltage capabilities. These processes, with operating voltages of 80 V, 200 V and 700 V, were developed using 0.18 µm CMOS technology. This thesis will focus on the TowerJazz Semiconductor 0.18µm Ultra-High Voltage (TS18UHV) process that supports operating voltages of up to 700 V [21]. This process was developed for DC-AC power conversion and switching-mode power supplies that can be powered directly from a wall socket. It uses a combination of shallow trench isolation and local oxidation to construct JFETs and LDMOS transistors that can handle 700 V alongside standard low-voltage CMOS (at 1.8 V or 5 V) [21]. Figure 2.1 shows the cross-section of an ultra high-voltage NMOS transistor in the TS18UHV process. A more detailed analysis of the production methods and materials used can be found in [21]. This transistor is designed with a maximum V_{GS} of 5 V.

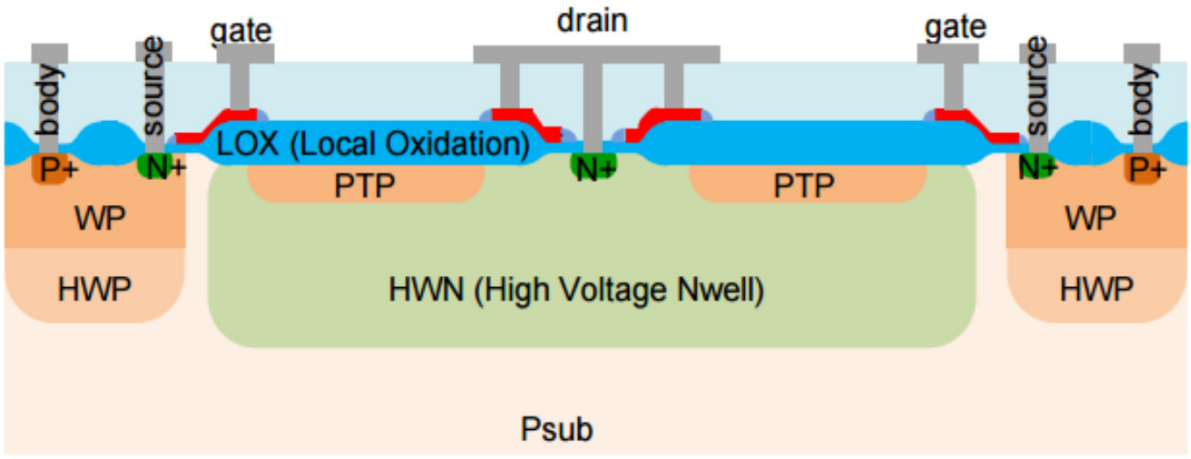


Figure 2.1 Cross-section of an ultra high-voltage transistor *[21]*

2.2 Implementing the Half-Cell Inverter on the TS18UHV Process

The half-cell 5-level inverter from [12] has been designed using pass transistor logic (PTL) on the TS18UHV process as a base case for how the process functions. The schematic is implemented using the Cadence Virtuoso version 6.1.6 Schematics L toolbox. Simulations were run on Cadence ADE GXL using the Spectre simulator. The TowerJazz TS18UHV process with the 3M1T3 flavor (3 metal layers) is the physical design kit (PDK) library used for constructing the circuits in this thesis. This flavor contains the tech libraries and the parasitic extraction run-set for a specific metal combination, though no layout has been created to extract the parasitics.

2.2.1 Simulation Setup

This thesis focuses on the physical viability of integrating a power inverter using a CMOS process. Because of this, the control methodology used for the converter does not include zero voltage switching, pulse-width modulation or space-vector modulation techniques. This may result in a lower efficiency than was realized in [12] but will serve to demonstrate the output viability of the inverter circuit. The stimulus files used to simulate the inverter is given in appendix A.

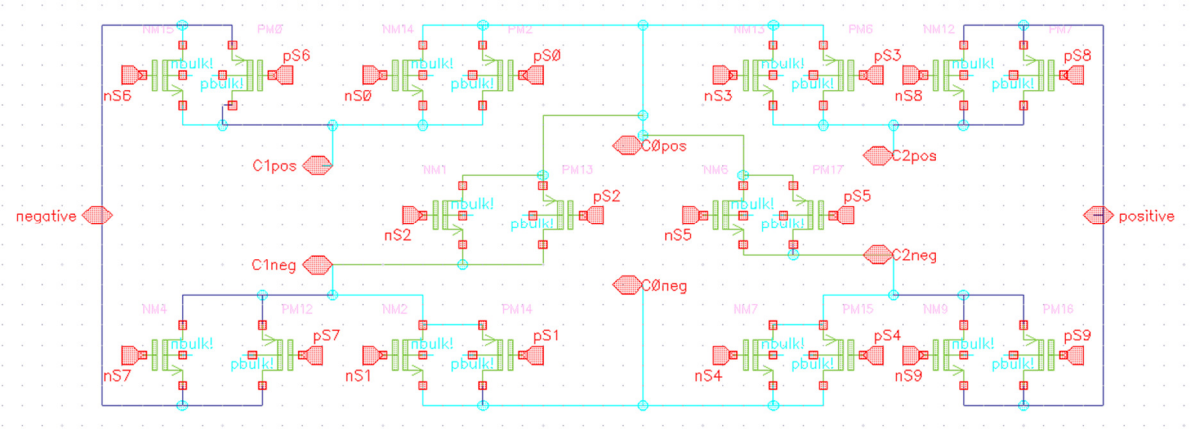


Figure 2.2 Half-cell inverter implemented in Cadence 6.1.6 using the Jazz TS18UHV PDK

Figure 2.2 shows the schematic of the 5-level half-cell inverter from [12] implemented using the Jazz TS18UHV process. This implementation uses a PTL configuration of transistors, similar to that described in [11]. This differs from the implementation in [12] which uses only NMOS transistors (see Figure 1.5). This change was made because, when simulating with only NMOS transistors, the output is severely reduced compared to using both NMOS and PMOS as shown in Figure 2.2. The corresponding outputs for the NMOS-only schematic (red) and the optimized PTL schematic (green) along with a PMOS-only schematic (orange) are shown in Figure 2.3.

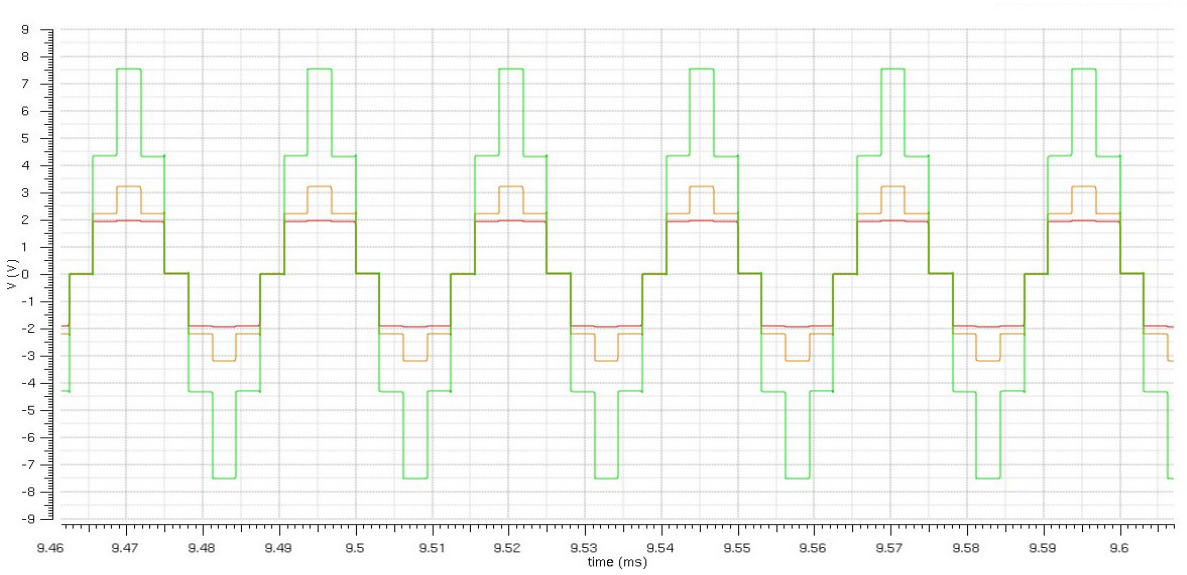


Figure 2.3 Output voltage of the half-cell inverter for V_{in} = 5 V and R_{load} = 1 kΩ.
[red] NMOS [orange] PMOS [green] NMOS and PMOS (PTL)

The transistors were sized with a finger width of 30 µm and gate length of 0.6 µm. The NMOS gate contained 5 fingers for a total width of 180 µm while the PMOS gate contained 15 fingers for a total width of 450 µm. Additionally, because the transistors are 4-terminal devices, the bulk cannot be left floating. In [12] the transistors used were discrete 3-terminal transistors, with the bodies connected to the sources. This is possible because each discrete transistor has

its own bulk. In CMOS, with the bulk shared among the transistors, this is not a practical way to eliminate the body effect. To prevent reverse-bias diode leakage, the corresponding bulks are connected to the highest (PMOS) or lowest (NMOS) voltages that we expect the transistors to encounter [22]. In the case of a 5-V input, the highest voltage is 10 V and the lowest is 0 V. This was verified through simulations, with the results shown in Figure 2.4 for an applied V_{gate} of 5 V. Because there is no high-voltage DC source to supply the biasing of this circuit, a charge pump, such as in [23], is recommended to accomplish this task. If the current flow through the body can be minimized, this charge pumping scheme should be minimally detrimental to the efficiency of the system.

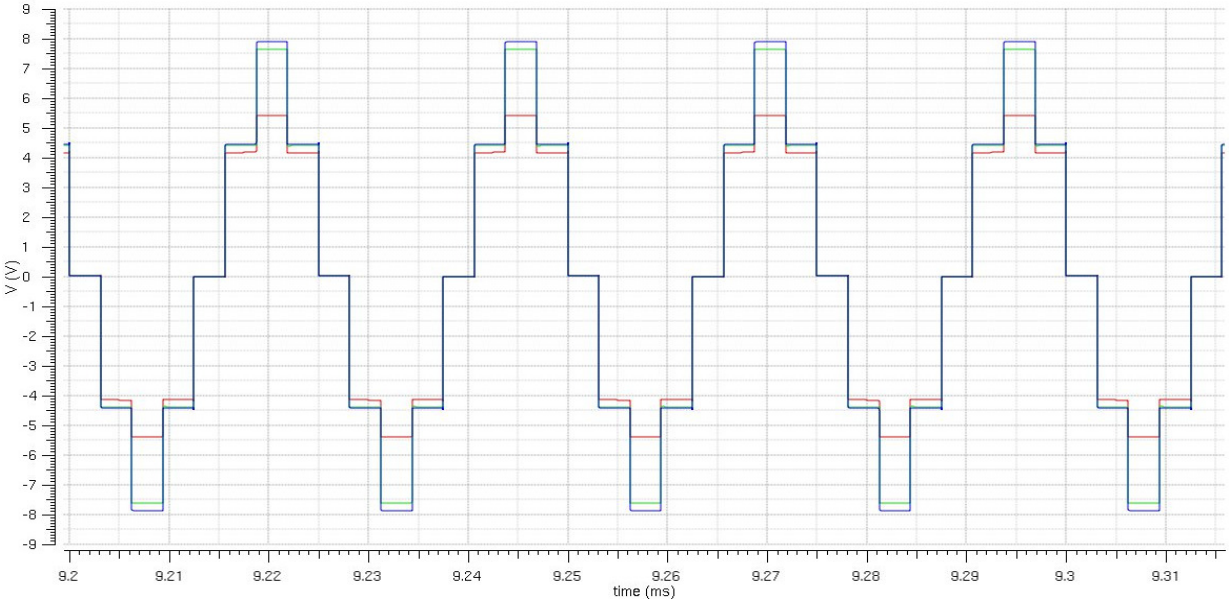


Figure 2.4. Output voltage for V_{in} = 5 V R_{out} = 1kΩ with the PMOS bulk at 5 V (red), 10 V (green) and 15 V (blue)

The capacitors were set to 20 µF as given in [12]. V_{in} was set to 5 V for initial simulations and 50 V to show higher-voltage operation. Three loads were simulated using the half-cell inverter given in [11]. Two resistive loads represented heavy loading (120 Ω) and light loading (1000 Ω). The third simulated load was an inductive load of 3 Ω in series with 300µH, a lower

inductive load than given in [12] due to the smaller scale of this simulation. The switching frequency used is 320 kHz, resulting in an output frequency of 40 kHz. The stimulus files used for the spectre simulation are given in Appendix A.

2.2.2 Simulation Results

The TS18UHV process is designed to have 5-V gate-drain and 5-V gate-source voltages, though the simulations show that using a 5 V gate voltage does not adequately control the on-off switching of the transistor at high-voltages. Because of this, the simulated gate voltage was set to 100 V to allow for strong on/off switching of both the NMOS and PMOS transistors. Figure 2.5 shows the effect of the gate voltage on the output voltage. This would be prohibitive in a physical device and a more adequate control system requires further research. In the simulations with 50-V input voltages and 100-V gate voltages, warnings were received for exceeding gate-drain and gate-source breakdown voltages. This did not occur during the low-voltage simulation.

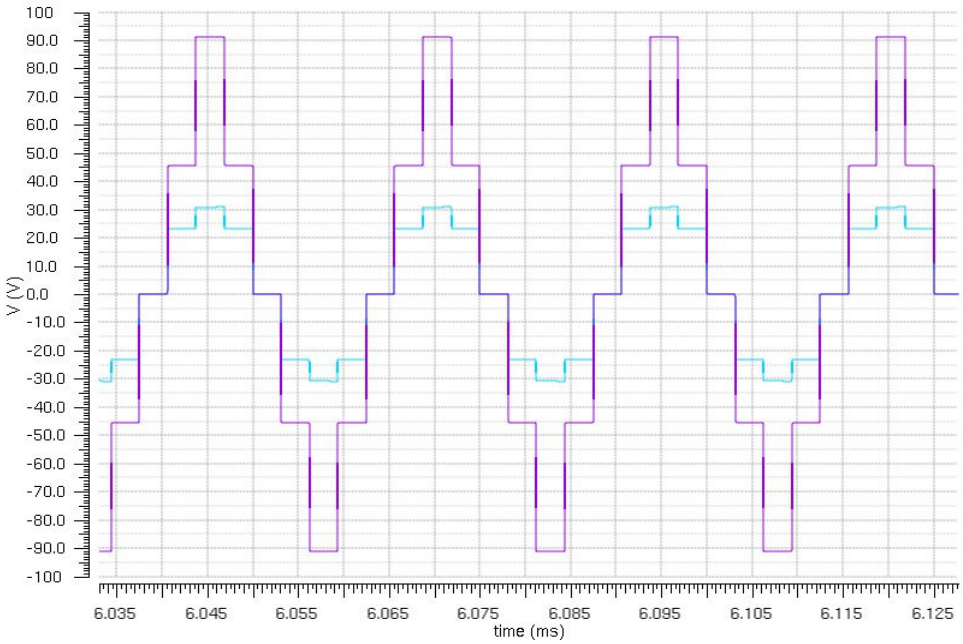


Figure 2.5 Output voltage for V_{in} = 50 V, V_{bulk} = 100 V, R_{load} = 1 kΩ (cyan) V_{gate} = 50 V (purple) V_{gate} = 100 V

Table 2.1 shows the results of the simulations. Figures of the simulations can be found in the left-hand column of Appendix B. The lack in efficiency at higher loads is mainly caused by the larger difference in voltages on the capacitor during switching due to the greater discharge of the capacitor. There is also a higher amount of shoot through current at the higher voltage level. This current is caused when the switching devices between the positive and negative input terminals are on at the same time, allowing a brief short across the device. This can be rectified with better switching techniques.

R_{load} (ohm)	L_{load} (uH)	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	Efficiency
120	0	5	0.04527	5.88	0.00584	73%
1000	0	5	0.04572	4.48	0.00584	95%
3	300	5	0.03279	5.28	0.06673	N/A
120	0	50	0.577	40.6	0.339	48%
1000	0	50	0.765	55.9	0.056	82%
3	300	50	0.997	44.8	0.564	N/A

Table 2.1 Simulation results showing load, input (RMS), and output (RMS) parameters

Simulations with the inductive load had a nearly 90-degree phase angle at the output. Though this calls into question the efficiency of the device, the simulations still allow the observation of the output voltage and current waveforms. The output voltage is especially distorted as the capacitor is very heavily loaded by the inductor. The capacitor was not resized for each of the loads to show the sensitivity of the inverter to different loading profiles.

Despite these problems, this set of simulations points towards the possibility of using CMOS manufacturing techniques to develop a power converter. The process used contains transistors for power applications, control logic, and communication systems all on one chip. With this path in mind, the scalability of this particular schematic comes into question. The half-

cell and, to a lesser extent, the full-cell inverters have many transistors in series used to transmit power, particularly when outputting $\pm 2V_{in}$. To reduce R_{on} and achieve the currents necessary for kW-scale inverters, many wide-gate transistors would need to operate in parallel. These two items, combined with the need for off chip capacitors, makes layout and power routing more difficult.

3 The Bused Switched-Capacitor Inverter

The CMOS process has been used extensively as a low-voltage digital process. The ability to incorporate low-voltage digital electronics and high-voltage power electronics, as in the TowerJazz process described in Chapter 2, will help usher more compact and intelligent power converters. In digital systems, buses are input and output signal routes that allow components to communicate with each other on- or off-chip. These communications pathways are critical to the compactness of design as well as to the organization of input/output capabilities on a chip. In power electronics, buses can be used as linkages to allow for a large network of transistors to charge and discharge capacitors. The usage of bus architecture has not yet been adequately explored in the realm of power electronics. In addition to exploring the feasibility of CMOS integration, this thesis explores practicality and usefulness of using bused architecture in a power inverter.

This thesis presents a novel inverter topology, shown in Figure 3.1, for a bused switched-capacitor inverter. The schematic shows the positive and negative input and output bussing for the inverter in addition to the relative connections of the capacitors. In general, for this topology if the circuit has N capacitors it will exhibit (N+2) voltage levels. Thus, since the circuit in Fig. 3.1 has 3 capacitors, it will output 5 voltage levels. Though this gives fewer voltage levels for the number of capacitors compared to [12], it adds the ability to charge and discharge the different capacitor banks simultaneously. This allows the capacitors to be fully charged when switched to output, which is especially important if switching between V_{out}=V_{in} and V_{out}=2V_{in} without needing to cycle back to V_{out}=0 to recharge a capacitor bank.

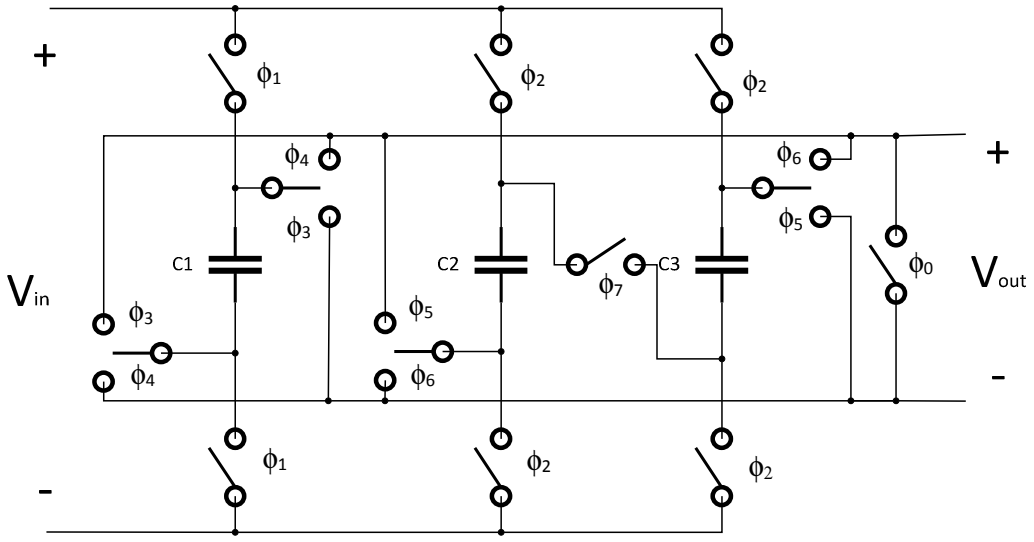


Figure 3.1 Schematic of a Switched Capacitor bused inverter showing power input and output buses

In high-power systems, it may be important to have isolation between input and output. In [4] , [11], and [12] the input and output are connected for the levels corresponding to $V_{out}=\pm V_{in}$. Because the bused SC inverter topology charges one bank of capacitors while outputting across the other bank, there is never a direct connection between the input and the output. This is an advantage because it reduces the potential to transmit harmonics and transient voltages between the input and output. This is especially important in high-voltage and high-current applications.

3.1 Operation

As discussed in [12], one method of creating multiple voltage levels in a switched capacitor circuit is by cascading switching cells together. The bused converter uses two different switching cells to accomplish the output voltage inversion. Figure 3.2 shows the two switch configurations for the converter. The full cell switching stage (Figure 3.2 (a)) creates 3 voltage levels. A half-cell stage (Figure 3.2 (b)) is used to add 2 more isolated voltage levels. This

two stage approach alternates charging and discharging between the stages. An additional *N*th stage can be connected through a switch to the $(N\text{-}2)^{th}$ stage capacitor's positive input. Another possibility is the use of multiple full cell switching stages so that they operate as necessary to perform the two-stage switching while providing the power necessary to the circuit. In this manner, it is possible to only use the amount of capacitance needed to adequately supply the load.

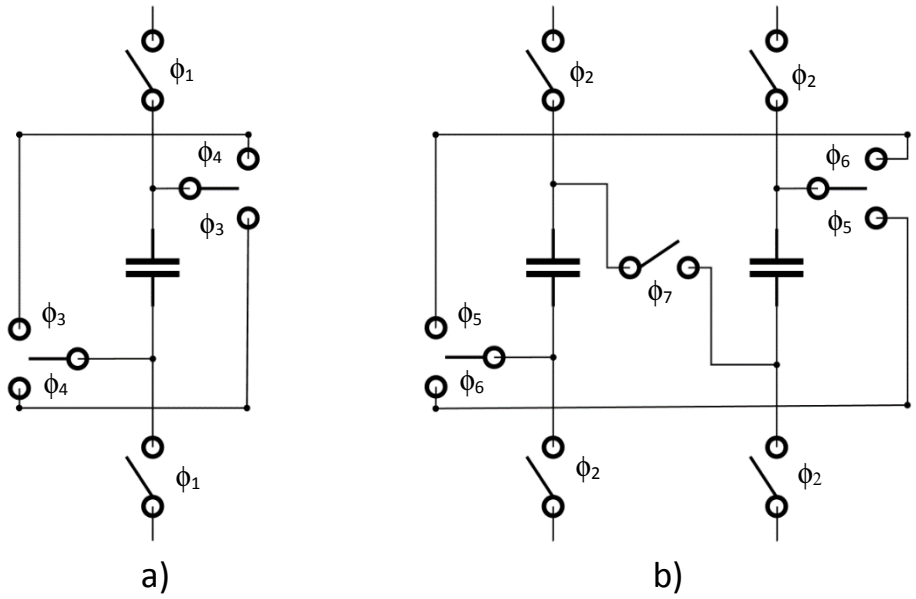


Figure 3.2 a) full-cell switching around a capacitor b) half-cell switching around two capacitors

For this thesis, the device will be limited to a five-level, two-stage inverter. Figure 3.3 shows the switching operation of such a converter in order to achieve the desired voltage levels at the output. Because of the ability to charge and discharge separate stages simultaneously, the diagram is split into two columns with the left showing the switch position for charging the relevant stage and the right for discharging the stage. This setup allows for isolation between the output and ground, as well as ensuring that the capacitors are completely charged between each cycle. This allows smaller capacitors to be used for a low output frequency since the output of the device does not need to cross 0 V to charge the system.

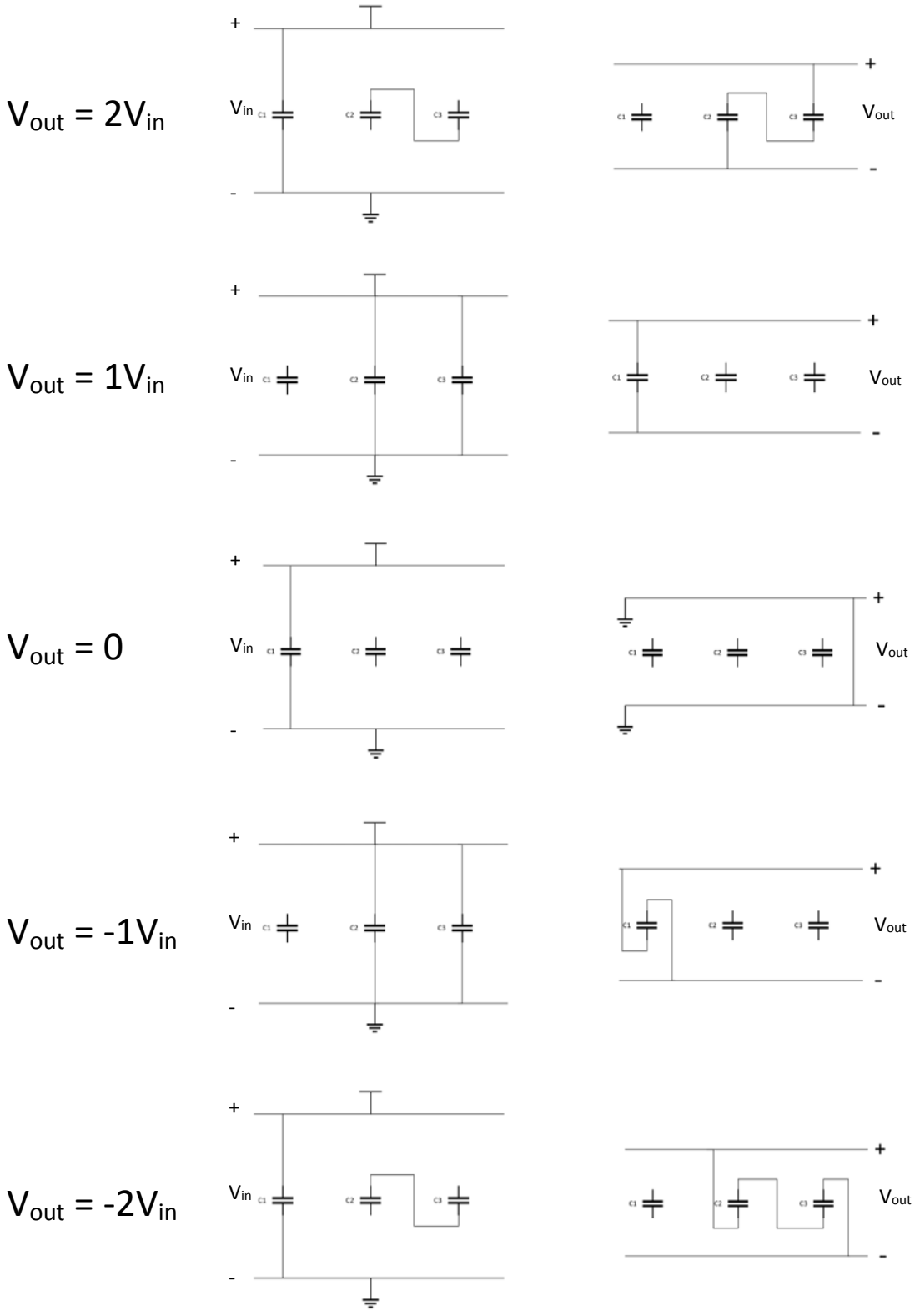


Figure 3.3 The left column shows the switch positions on the input side (for charging), the right shows the switching positions on the output side (for discharging). The capacitors are duplicated in the two columns.

3.2 Simulation Setup

For an equal comparison with the cell-based SC inverter, the simulation for the bused inverter does not make use of any advanced modulation techniques. This will mean that the system will not be working at peak efficiency, but will rather be used as a validation of the circuit topology's output capabilities. Transistor and capacitor sizing remain the same between the half-cell simulation and this one. The switching frequency used will remain at 320 kHz with an output frequency of 40 kHz. All of this is to result in a more direct comparison since the objective of this thesis is to look at CMOS integration of these power electronics.

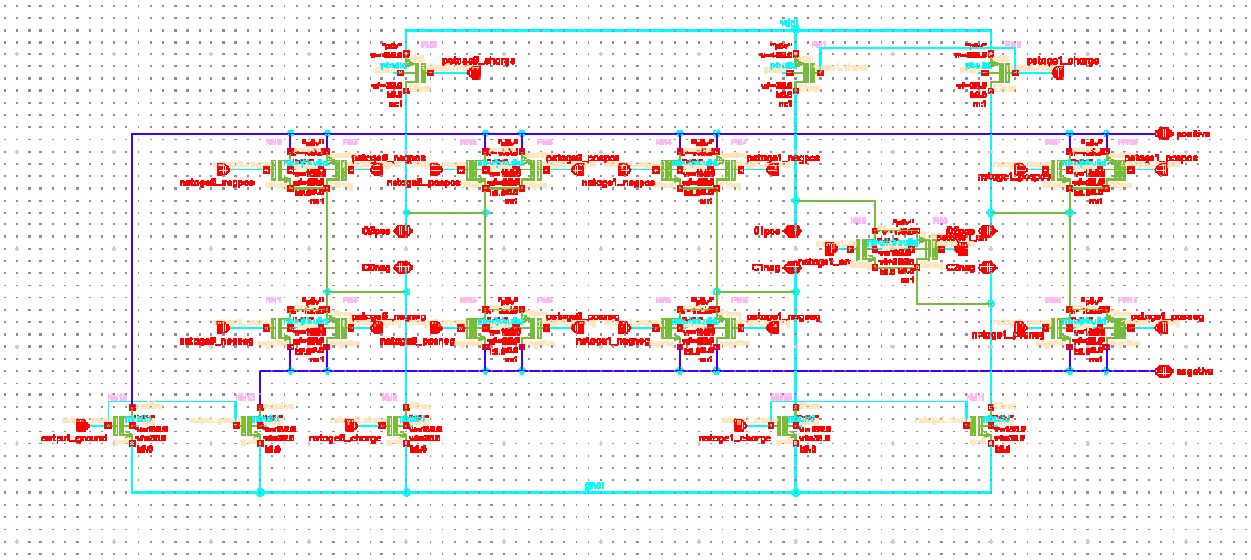


Figure 3.4 Cadence schematic of the bused switched-capacitor inverter

Figure 3.4 shows the arrangement of two stages (green) along the input (light blue) and output (dark blue) buses. The capacitors are not shown as they would be off chip. Bulk connections are independently set for the NMOS and PMOS transistors, similarly to the simulation for the cell-based inverter. It is of note to show the effect that different bulk voltage levels have on the output of this inverter. One of the design reasons was to give better output

voltage levels than the cell-based inverter. Figure 3.5 shows the output levels for the given bulk voltages under light and heavy resistive loads. Even with a p-bulk voltage set at 5 V, this inverter topology shows good differentiation between $V_{out} = \pm V_{in}$ and $\pm 2V_{in}$. There is a minor output improvement from setting $V_{bulk} = V_{gate} = 5$ V to 10 V. However, there is no additional

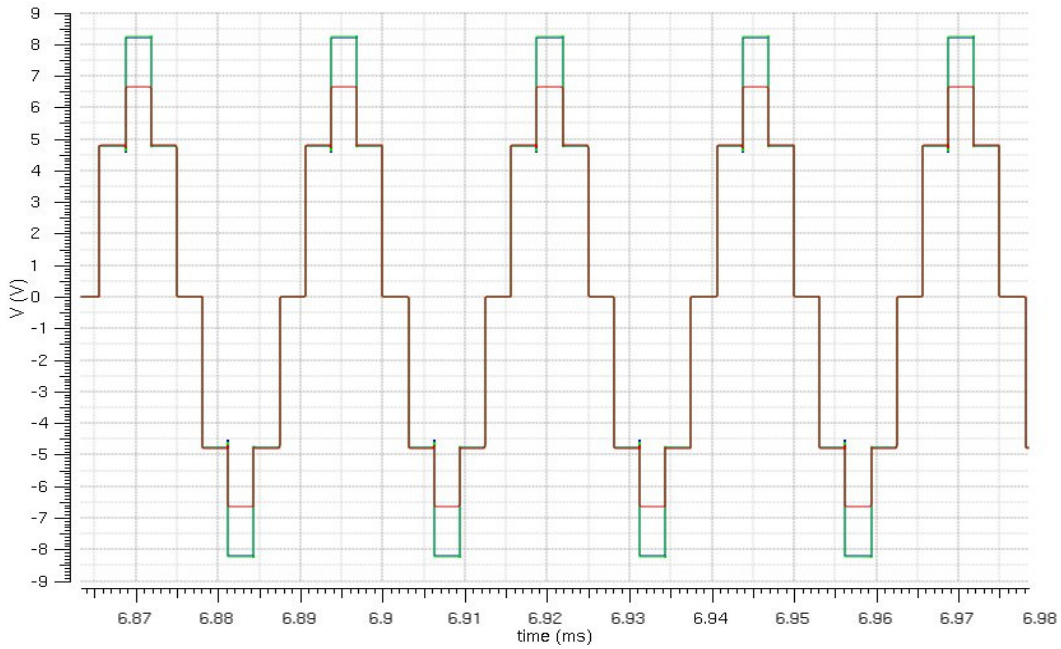


Figure 3.5 Output voltage for $V_{in} = 5$ V $R_{out} = 1\text{k}\Omega$ with the PMOS bulk at 5 V (red), 10 V (green) and 15 V (blue)

improvement when setting V_{bulk} and V_{gate} to 15 V. To maintain a more direct comparison to the cell-based inverter, V_{bulk} and V_{gate} will be set to 10 V for the low-voltage simulations and 100 V for the higher-voltage simulations. The stimulus file for the bused inverter is given at the end of Appendix A. As in the simulations for the cell-based inverter, and to ease switching control for the simulations, the applied gate voltage was equal to the PMOS bulk voltage.

3.3 Simulation Results

Figures of the results can be found in the right-hand column of Appendix B. The RMS voltages and currents as well as overall efficiencies are summarized in Table 3.1. Warnings for

exceeding the gate-drain and gate-source voltages were received while simulating the inverter at V_{in} = 50V and V_{gate} = 100V. Under this simple control scheme, the bused inverter does not perform very well. Efficiency tops out at 60% at the lower voltage and just under 40% at the higher input voltage. The inductive loads cause nearly a 90-degree phase shift between the voltage and current, making the RMS output power near zero. This could be rectified with a filter if an inductive load is being driven. Conversely, a switching technique such as space vector modulation can allow the inverter to perform power factor correction to properly drive an inductive load [24].

R_{load} (ohm)	L_{load} (uH)	V_{in} (V)	I_{in} (A)	V_{out}	I_{out} (A)	Efficiency
120	0	5	2.49E-02	5.33	0.0053	22.86%
1000	0	5	4.71E-02	4.125	0.0344	60.23%
3	300	5	3.38E-02	4.938	0.0632	N/A
120	0	50	0.6746	40.09	0.3341	39.71%
1000	0	50	0.6225	52.45	0.0525	8.84%
3	300	50	0.7897	40.4	0.5141	N/A

Table 3.1 Simulation results showing load, input (RMS), and output (RMS) parameters

Even with the lower observed efficiency, these simulations are effective in demonstrating the capabilities of this topology, notably the smaller effect of bulk biasing on the voltage output of the device. Because the device parameters were unchanged from the previous inverter, it may be possible to enhance the capabilities of the bused converter by changing the size of the capacitors and the operating frequency of this inverter. Additional efficiency gains may also be realized by incorporating better switching techniques.

4 Conclusion

Power electronics has seen a resurgence in recent years. Inverters are integrated into residential battery storage systems (such as Tesla's Powerwall) and string inverters are used to link sets of photovoltaic panels together. As this thesis has discussed, the next evolution of these systems is the integration of these power electronics onto a single chip. This would allow not only more compact and efficient power inverters, but also integration with control systems, communications, and even direct integration with PV panels.

Though this topic has been discussed for the last twenty years, it has only been in the last two that high-voltage CMOS processes have become commercially viable, with this thesis just discussing one such technology. It is only a matter of time until single-chip inverters become integrated with commercial technology. At first, these systems will use better known inverter topologies, such as the cell-based inverters, to build these systems. Already, the five-level inverters represent the forefront of technology in the commercial space, with many commercial inverters having only three output voltage levels due to the costs of circuitry for additional levels in high-power systems.

The main concern of grid-tied inverters, from a utility perspective, is the injection of harmonic distortion into the grid system. More voltage levels allow a reduction of distortion by having reduced switching voltage for the same output voltage. You can also decrease output harmonics though a robust control system that allows for soft switching. Lower harmonic distortion, along with localized VAR control, helps to alleviate many of the concerns of grid operators. Additionally, coupling these smart inverters with energy storage and demand

response allows consumers to participate in electricity markets, supplementing the utility or reducing the demand as necessary. This leads to a more robust and resilient grid [25].

4.1 Results

In these initial tests, both types of inverters performed well, especially for having only basic switching control. This is particularly true for the cell-based inverter, with simulations of a resistive loading finding the same high efficiencies (near 95%) as those reported in [12]. This efficiency dropped off with heavier loading mainly due to capacitive switching losses. The heavier loads caused a larger voltage drop across the capacitors in each cycle, contributing to the drop in efficiency. At higher voltages, the drawbacks of the simple switching scheme become more apparent with the efficiencies dropping even further. A multicarrier PWM scheme, as used in [12] would alleviate some of those losses.

Despite the benefits that were observed in these simulations, the simulations themselves showed some caveats. The biggest disadvantage of the cell-based inverter was the poor voltage reproduction without proper biasing. Though this is easily overcome at lower voltages, higher input voltages present the challenge of properly biasing the semiconductor bulks to prevent leakage currents. This may be preventable in other ways, but that is beyond this thesis.

The bused inverter described in Chapter 3 had lower overall efficiency than the cell-based inverter. Despite this, the design did have one advantage over the cell-based inverter: as was shown in Figure 3.5, the bus inverter exhibited less dependence on the bulk voltage biasing as compared with the cell-based inverter. With a 5-V bias on the P-bulk (and the N-bulk grounded), the inverter showed well differentiated output voltage levels. Biasing the P-Bulk

beyond 10 V had no effect on the output voltage levels. This shows that the bused inverter may have propensity towards less leakage current than the cell-based inverter when integrated using a CMOS process.

Regardless of the slight advantage with biasing voltage that the bused inverter has over the cell-based inverter, without large improvements in efficiency it does not represent a likely choice for integrating the inverter onto CMOS. This does not, however, rule out the possibility of further research using similar topologies, or of the chance to improve its efficiency through better switching methods. Using a bused network for the power transistors may prove easier to integrate at the larger scale necessary for kW-scale power inverters. Despite this, the cell-based inverter has a clear advantage in efficiency. It has already been proposed as an option for integrating into CMOS in [11] and represents the best choice for moving forward in that direction.

4.2 Future Research Directions

The biggest weakness of this thesis is the lack of an advanced switching control system for the inverters. Without using such a system, it is not possible in the simulations to scale up the output to the order of kW. Because of this, the most important next step is testing these inverters with an improved switching algorithm. Implementing a better switching technique would give a better understanding of the real-world capabilities of the inverters. It is especially important to use a zero-voltage switching technique, which would diminish switching losses by allowing the inverter to operate in a soft switching mode. The bused inverter was designed specifically with a pulse-width-modulation switching technique in mind, allowing the capacitors to be charged every cycle. The importance of this is to allow the device to operate at a high

switching frequency yet still output a grid matched sinusoid. Whichever topology is used to further CMOS integrated inverters, it is important that it outputs a 50/60Hz sinusoid. To the knowledge of this author, this has not yet been done.

Beyond schematic simulations, it is necessary to design and simulate a layout that can efficiently operate at higher output power. Process limitations may necessitate a review of the design of these inverters, as this thesis was attempting to take a first step towards addressing. Integrating large numbers of transistors in parallel, at high operating voltages, poses a challenge to both “traditional” switched-capacitor inverter design as well as current techniques for CMOS layouts.

The integration of these power inverters into CMOS is inevitable. It will likely take time before the designs are ready for commercial integration, but they hold a lot of promise for the increased efficiency and power density of energy systems. With the proliferation of distributed energy systems, it is important to achieve the highest possible efficiencies and resiliency for the next generation electrical network.

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Appendix A

Stimulus File for the Half-Cell 5-level Inverter with V_{in}= 5 V

simulator lang=spectre

Vn0 (nS0 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vn1 (nS1 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vn2 (nS2 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vn3 (nS3 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vn4 (nS4 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vn5 (nS5 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vn6 (nS6 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="00000111" rptstart=1 rpttimes=1500
Vn7 (nS7 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="11111000" rptstart=1 rpttimes=1500
Vn8 (nS8 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="01110000" rptstart=1 rpttimes=1500
Vn9 (nS9 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="10001111" rptstart=1 rpttimes=1500

Vp0 (pS0 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vp1 (pS1 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vp2 (pS2 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vp3 (pS3 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vp4 (pS4 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vp5 (pS5 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vp6 (pS6 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="00000111" rptstart=1 rpttimes=1500
Vp7 (pS7 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="11111000" rptstart=1 rpttimes=1500
Vp8 (pS8 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="01110000" rptstart=1 rpttimes=1500
Vp9 (pS9 0) vsource type=bit val0=10 val1=0 rise=5n fall=5n period=3.125u data="10001111" rptstart=1 rpttimes=1500

Stimulus File for the Half-Cell 5-level Inverter with V_{in}= 50 V

simulator lang=spectre

Vn0 (nS0 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vn1 (nS1 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vn2 (nS2 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vn3 (nS3 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vn4 (nS4 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vn5 (nS5 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vn6 (nS6 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="00000111" rptstart=1 rpttimes=1500
Vn7 (nS7 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="11111000" rptstart=1 rpttimes=1500
Vn8 (nS8 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="01110000" rptstart=1 rpttimes=1500
Vn9 (nS9 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="10001111" rptstart=1 rpttimes=1500

Vp0 (pS0 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vp1 (pS1 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="11111101" rptstart=1 rpttimes=1500
Vp2 (pS2 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vp3 (pS3 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vp4 (pS4 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="11011111" rptstart=1 rpttimes=1500
Vp5 (pS5 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vp6 (pS6 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="00000111" rptstart=1 rpttimes=1500
Vp7 (pS7 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="11111000" rptstart=1 rpttimes=1500
Vp8 (pS8 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="01110000" rptstart=1 rpttimes=1500
Vp9 (pS9 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="10001111" rptstart=1 rpttimes=1500

Stimulus File for the Bused 5-level Inverter V_{in}= 5 V

simulator lang=spectre

Vn0 (out_gnd 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="10001000" rptstart=1 rpttimes=1500
Vn1 (ns0_chg 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="10101010" rptstart=1 rpttimes=1500
Vn2 (ns1_chg 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="01010101" rptstart=1 rpttimes=1500
Vn3 (ns0_neg 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="00000101" rptstart=1 rpttimes=1500
Vn4 (ns0_pos 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="01010000" rptstart=1 rpttimes=1500
Vn5 (ns1_neg 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vn6 (ns1_pos 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vn7 (ns1_out 0) vsource type=bit val0=0 val1=10 rise=5n fall=5n period=3.125u data="00100010" rptstart=1 rpttimes=1500

Vp0 (pout_gnd 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="10001000" rptstart=1 rpttimes=1500
Vp1 (ps0_chg 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="10101010" rptstart=1 rpttimes=1500
Vp2 (ps1_chg 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="01010101" rptstart=1 rpttimes=1500
Vp3 (ps0_neg 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="00000101" rptstart=1 rpttimes=1500
Vp4 (ps0_pos 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="01010000" rptstart=1 rpttimes=1500
Vp5 (ps1_neg 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vp6 (ps1_pos 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vp7 (ps1_put 0) vsource type=bit val0=10 val1=10 rise=5n fall=5n period=3.125u data="00100010" rptstart=1 rpttimes=1500

Stimulus File for the Bused 5-level Inverter V_{in}= 50 V

simulator lang=spectre

Vn0 (out_gnd 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="10001000" rptstart=1 rpttimes=1500
Vn1 (ns0_chg 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="10101010" rptstart=1 rpttimes=1500
Vn2 (ns1_chg 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="01010101" rptstart=1 rpttimes=1500
Vn3 (ns0_neg 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="00000101" rptstart=1 rpttimes=1500
Vn4 (ns0_pos 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="01010000" rptstart=1 rpttimes=1500
Vn5 (ns1_neg 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vn6 (ns1_pos 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vn7 (ns1_out 0) vsource type=bit val0=0 val1=100 rise=10n fall=10n period=3.125u data="00100010" rptstart=1 rpttimes=1500

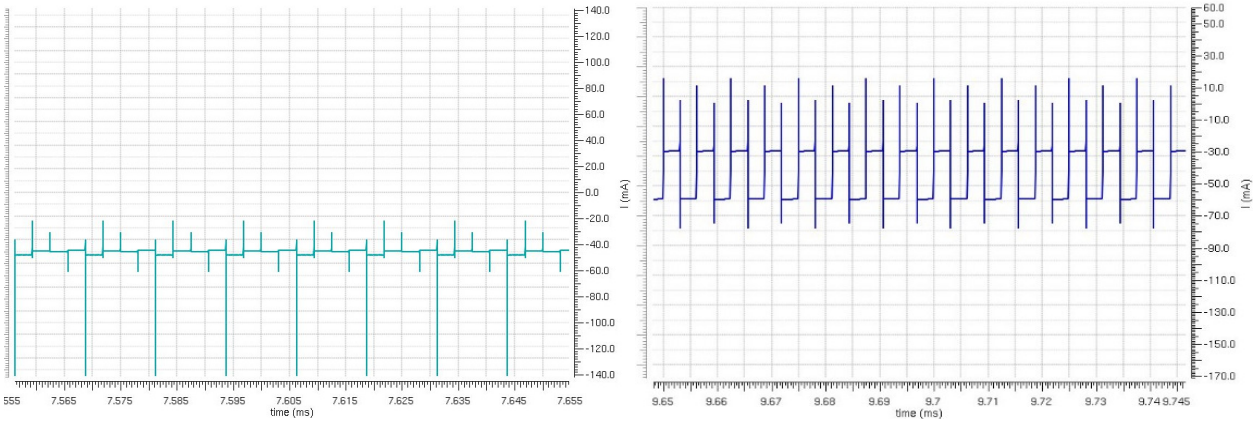
Vp0 (out_gnd 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="10001000" rptstart=1 rpttimes=1500
Vp1 (ps0_chg 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="10101010" rptstart=1 rpttimes=1500
Vp2 (ps1_chg 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="01010101" rptstart=1 rpttimes=1500
Vp3 (ps0_neg 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="00000101" rptstart=1 rpttimes=1500
Vp4 (ps0_pos 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="01010000" rptstart=1 rpttimes=1500
Vp5 (ps1_neg 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="00000010" rptstart=1 rpttimes=1500
Vp6 (ps1_pos 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="00100000" rptstart=1 rpttimes=1500
Vp7 (ps1_put 0) vsource type=bit val0=100 val1=0 rise=10n fall=10n period=3.125u data="00100010" rptstart=1 rpttimes=1500

Appendix B

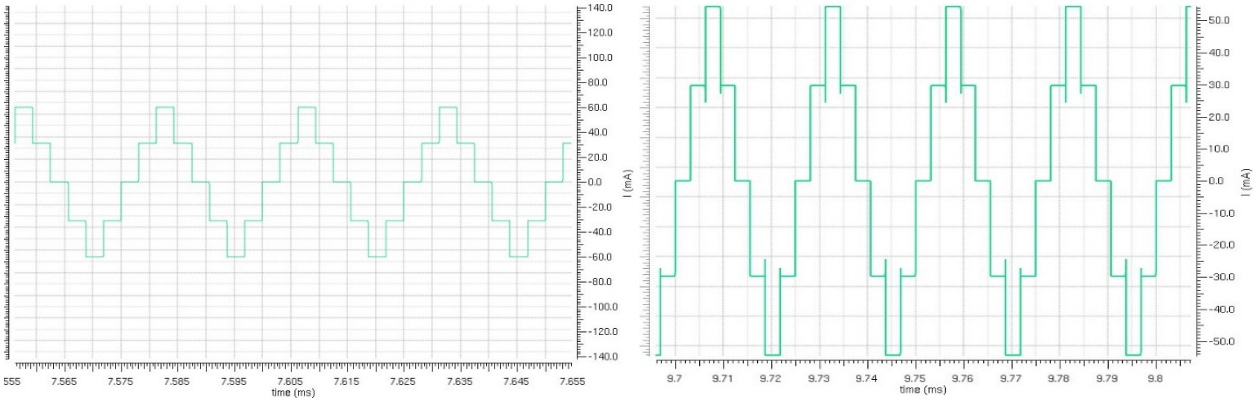
Left column is cell-based, right is bused inverter

V_{in} = 5V, V_g = 10V, R = 120Ω, L = 0µH

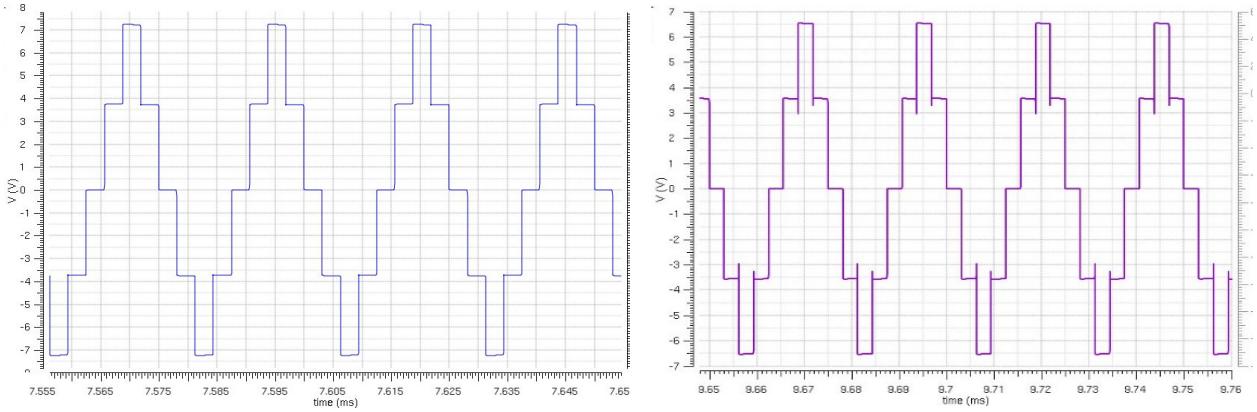
I_{in}



I_{out}

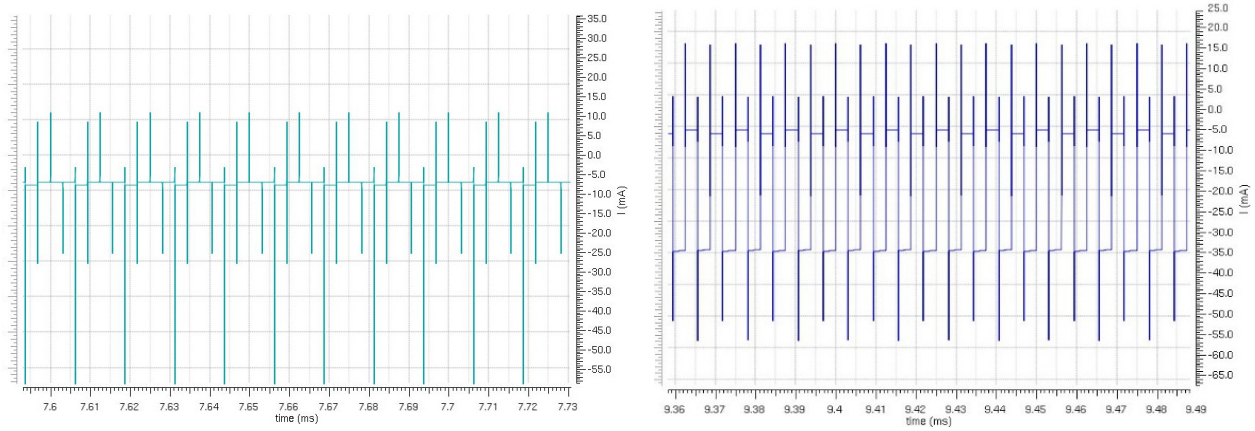


V_{out}

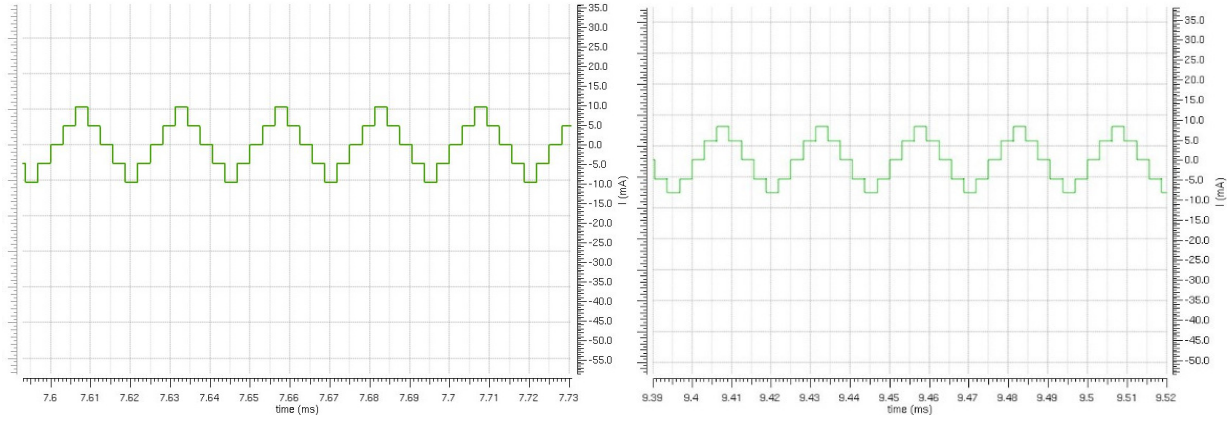


V_{in} = 5V, V_g = 10V, R = 1000Ω, L = 0μH

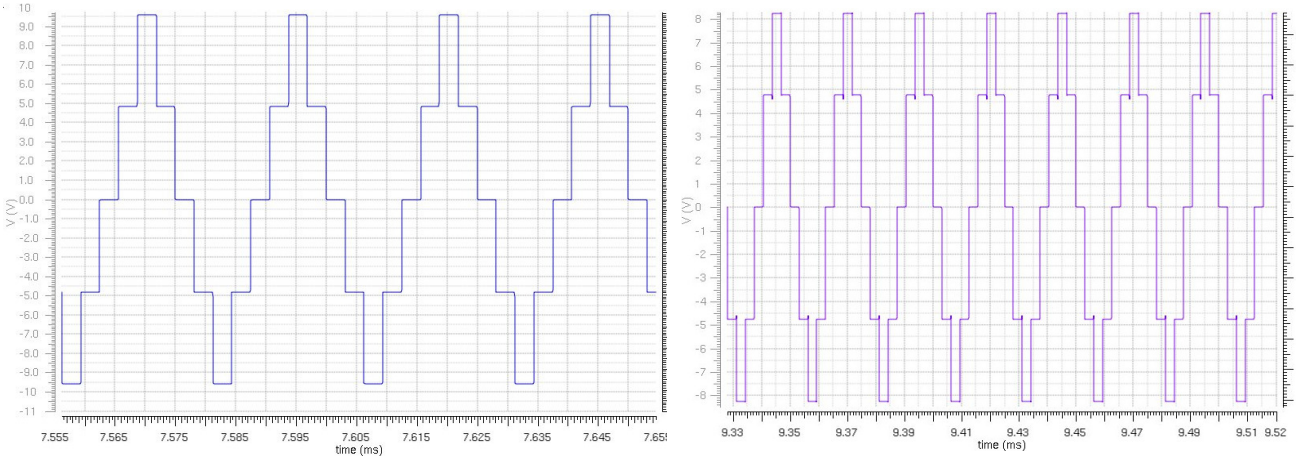
I_{in}



I_{out}

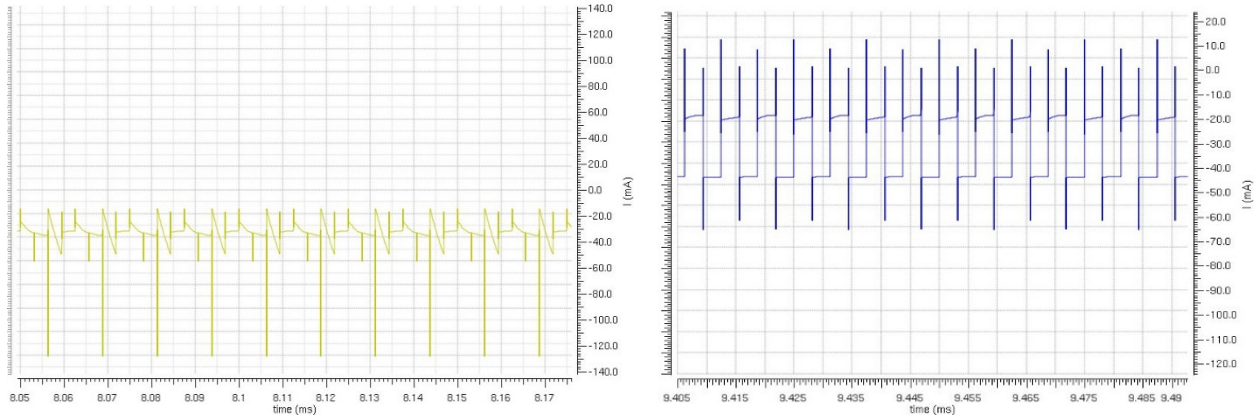


V_{out}

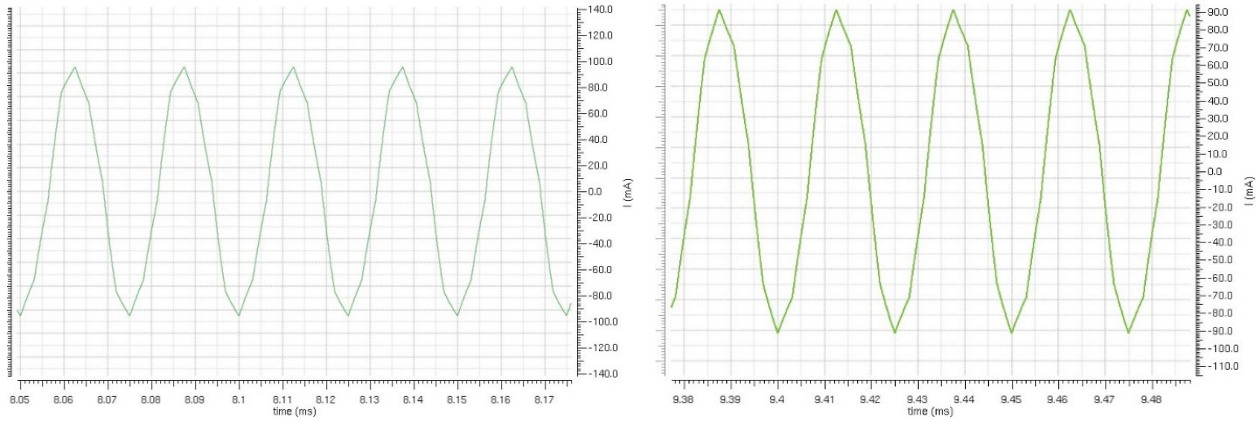


V_{in} = 5V, V_g = 10V, R = 3Ω, L = 300μH

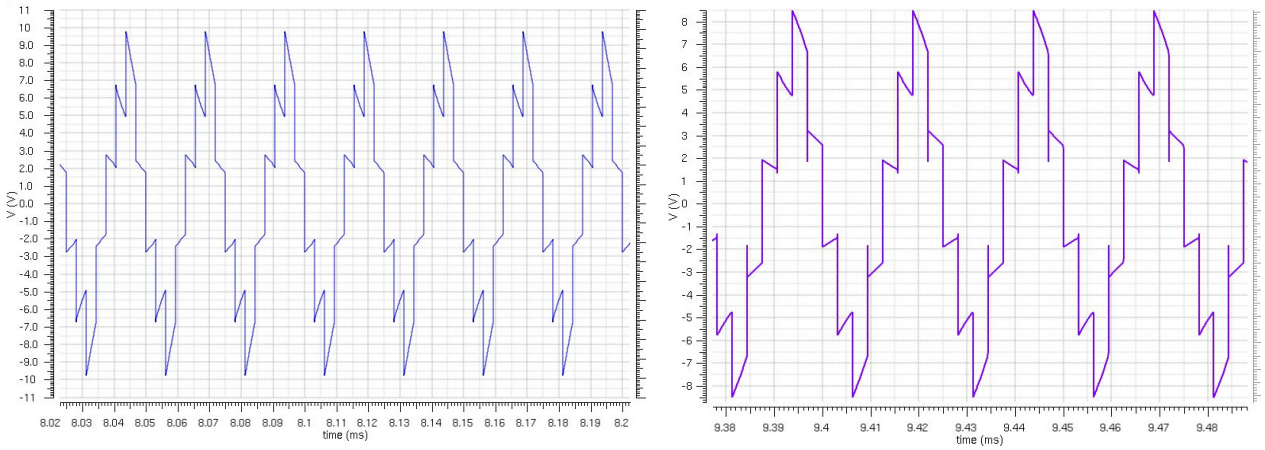
I_{in}



I_{out}

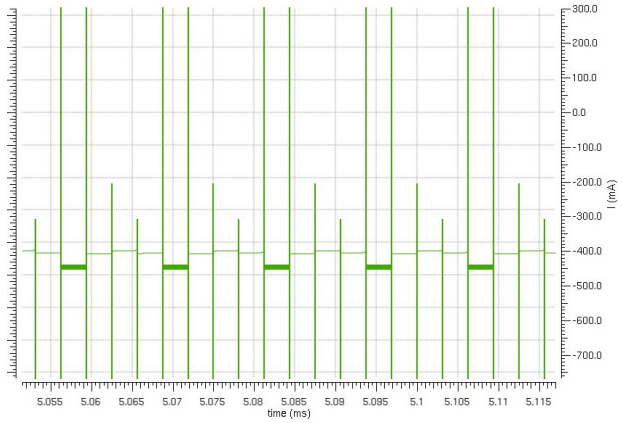


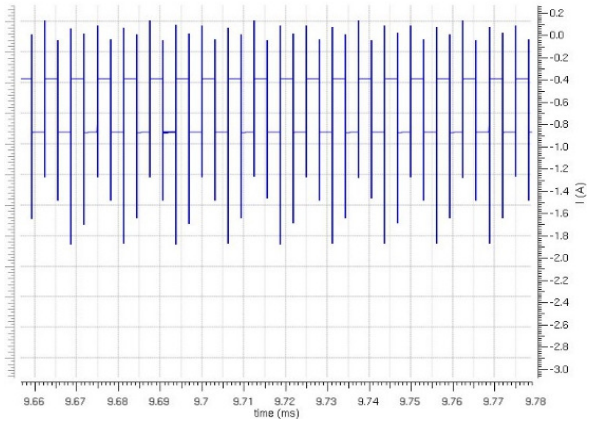
V_{out}



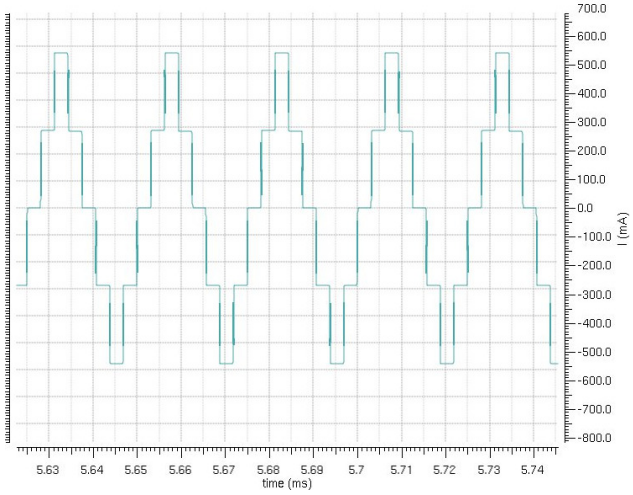
V_{in} = 50V, V_g = 100V, R = 120Ω, L = 0μH

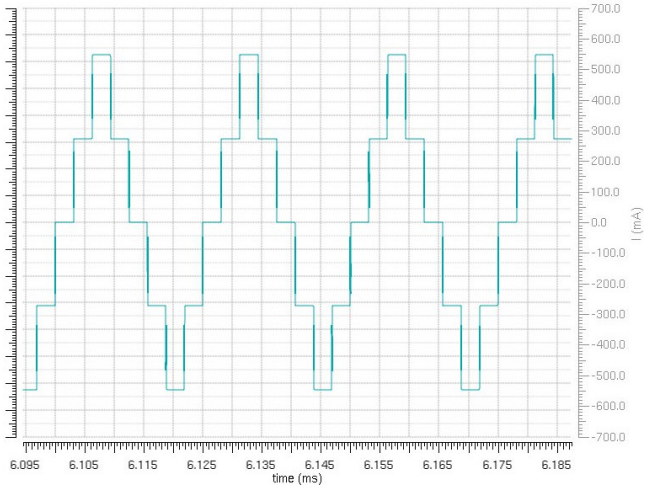
I_{in}



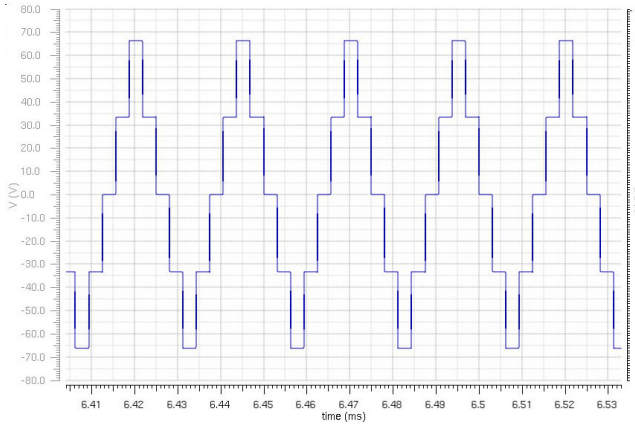


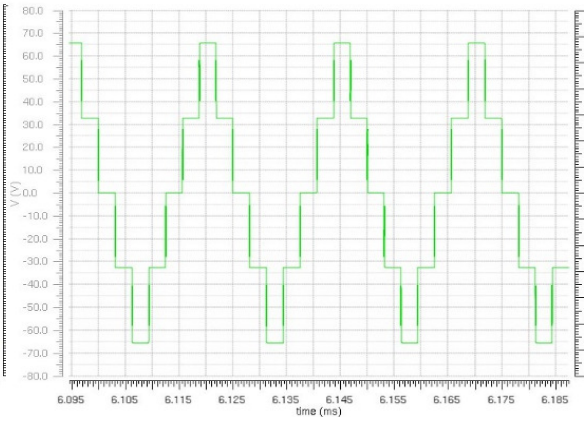
I_{out}





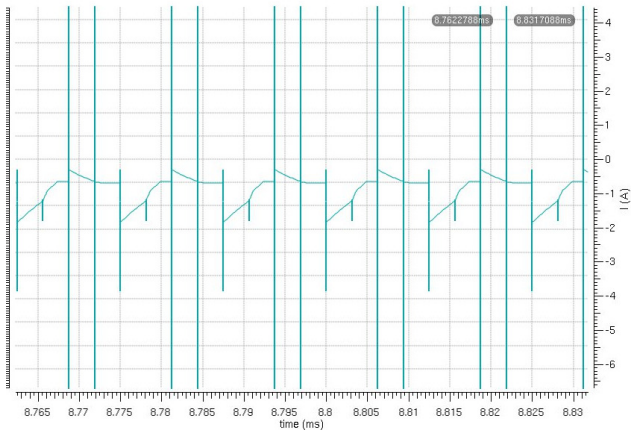
V_{out}

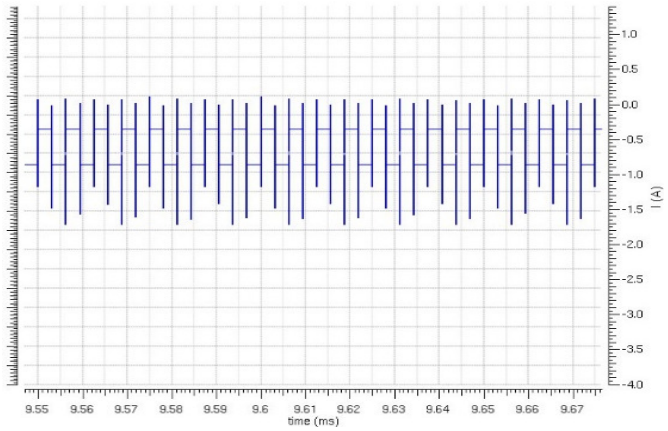




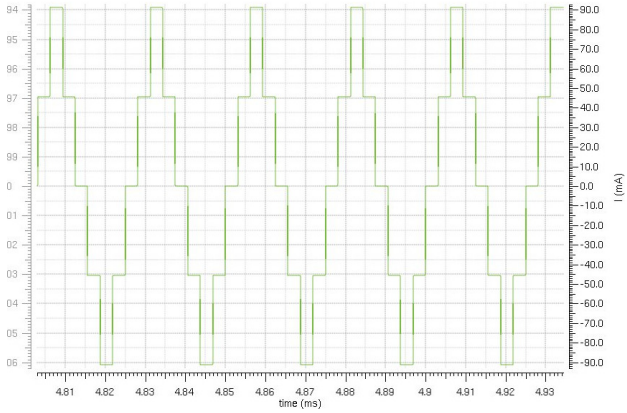
V_{in} = 50V, V_g = 100V, R = 1000Ω, L = 0μH

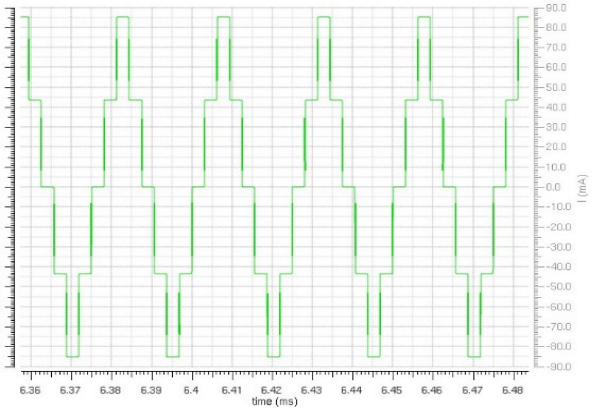
I_{in}



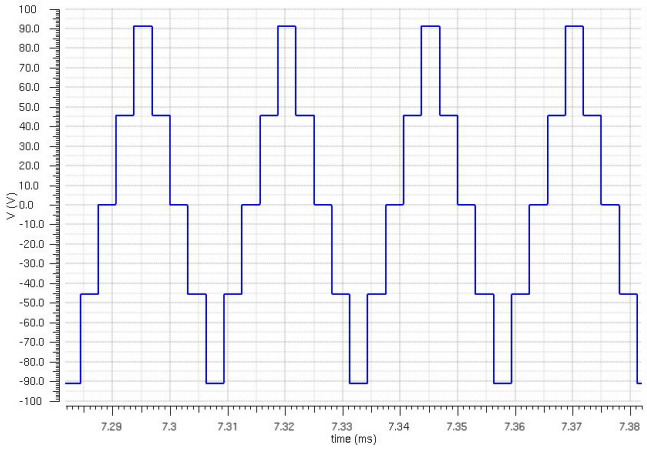


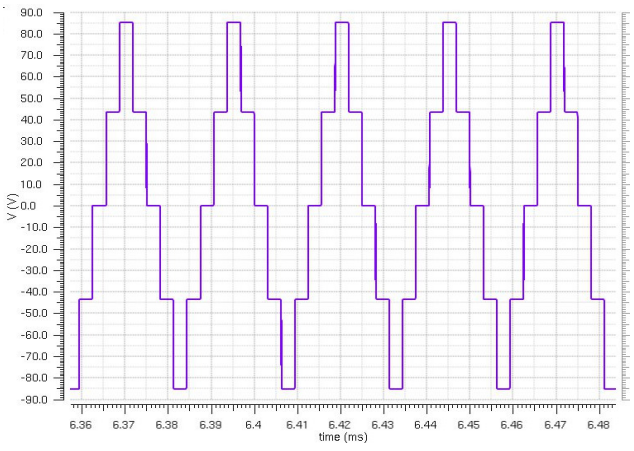
I_{out}





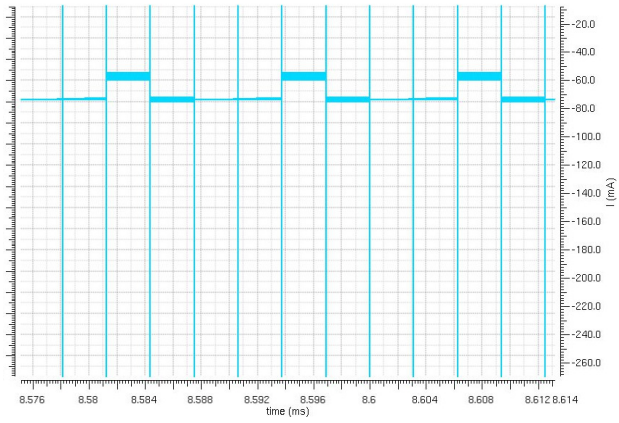
V_{out}

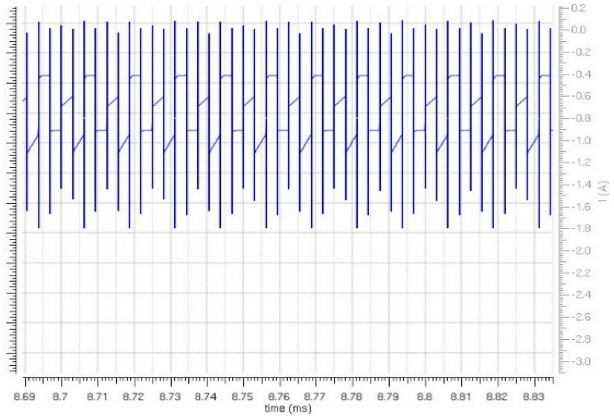




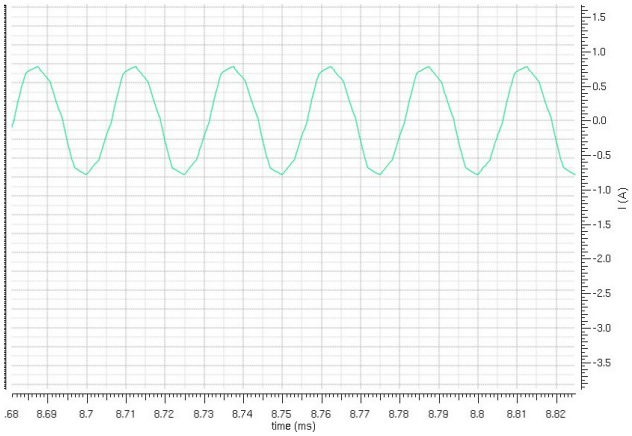
V_{in} = 50V, V_g = 100V, R = 3Ω, L = 300μH

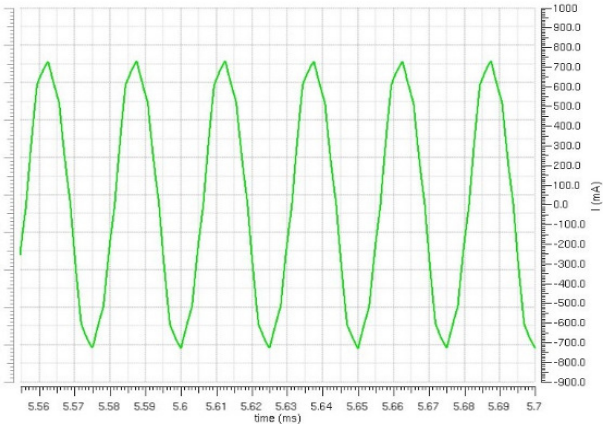
I_{in}





I_{out}





V_{out}