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PETAL: A Multi-Channel Differential ADC Driver for High-Speed CMOS Image Sensors

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***Abstract*— PETAL (Programmable Electronic Termination and Line Driver) is a 16-channel ADC driver chip that provides single-ended-to-differential conversion and column biasing for high-speed CMOS image sensors. By increasing the level of integration, the number of driver chips and associated number of passives and routing area is reduced, enabling smaller physical cameras. Power dissipation is reduced relative to many commercial approaches by the use of low-voltage CMOS technology and the increased level of integration. The driver chip also supplies programmable bias currents to the sensor, further reducing the number of required components on the camera board. The driver, fabricated in 180 nm CMOS technology, achieves settling to 0.1% in 11 ns with input noise of 89.9 μV-rms. The crosstalk between channels is below –56 dB. The power dissipation is 10.5 mW / channel. When applied to the readout of a high-speed X-ray sensor, the prototype reduced board area by 84% (from 100 mm^2 to 16 mm^2) and power dissipation by 25%.**

Index Terms—Mixed-Signal IC Design; Instrumentation Amplifier; Solid-State Imaging; CMOS Image Sensors

I. Introduction

CMOS image sensors are now making significant impacts in scientific imaging applications beyond visible light detection. They are used in charged particle detection for applications ranging from particle physics to electron microscopy, as well as X-ray and even neutron detectors. Increasing the readout rate is important for applications aimed at time-resolved or in-situ measurements, i.e. making movies. Architectures include both on-chip and off-chip digitization – with tradeoffs between area, power, and complexity dominating the choice. Off-chip digitization maximizes the imaging area. In addition, in a given technology, higher frame rates are possible when the pixel outputs are driven in the analog domain to external high-speed ADCs than when internal digitization with data transfer through serial digital interfaces is used [1].

Contemporary high-speed ADCs expect a fully differential input, yet image-sensor pixel outputs are inherently single-ended. In addition, driving ADCs at high speeds with controlled impedance lines requires buffering which results in a further cost in power and area.

In this work we report a highly integrated single-ended-to-differential ADC driver amplifier that meets system-level requirements with greatly reduced board space and number of components. In addition, required operation in vacuum mandates a low-power solution.

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The amplifier uses an open-loop approach, exploiting the relaxed linearity requirement of the application: here, we target the use of CMOS image sensors for particle detection. Because the sensitive volume (the moderate-resistivity region below the interface) is thin, energy fluctuations – described by a Landau distribution – are significant [2, 3]. This means that only moderate linearity is required, which is a key motivator of this design. In addition, in contrast to traditional differential amplifiers, the circuit presents high input impedance to the sensor, simplifying offset correction. Lastly, the circuit provides bias currents for the image sensor output source follower buffers, further reducing the number of board-level components required to implement a high-speed camera.

II. Multi-Channel ADC Driver

A. Chip Architecture

A block diagram of the ADC driver chip is shown in Fig. 1. It has 16 independent channels, each comprising a single-ended-to-differential converter with programmable output common-mode and 100-Ω differential termination (implemented with two physical 50-Ω series resistors). The zero level is also programmable by means of an offset input, allowing interfacing with different image sensors. The voltage amplified by the channel is the difference between the input and the offset value. In addition, 16 current sources are included to provide bias currents for the image sensor output source followers. Both the sensor bias currents and the bias currents used for the 16 ADC driver channels are programmable via simple external resistors to ground.

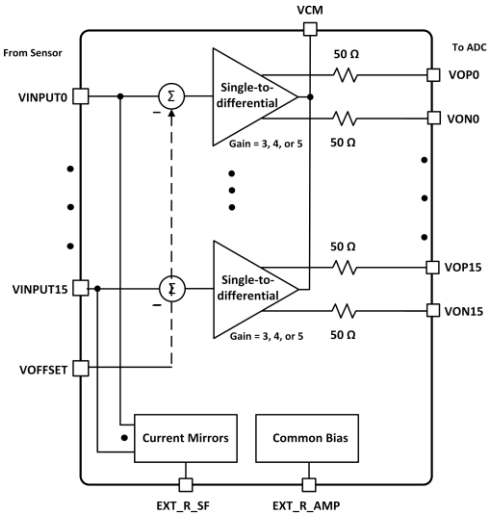

Fig. 1. ADC driver block diagram.

A key design consideration is the minimization of crosstalk. Most industry standard approaches to single-ended-to-differential converters use negative feedback amplifiers using resistors to set the gains [4]. This approach is effective but can be problematic in a multi-channel system because the offset correction voltage can become signal dependent, leading to undesired crosstalk between channels. Therefore, high-impedance inputs are preferred to reduce crosstalk.

B. ADC Driver Channel

A block diagram for a single ADC driver channel with high-impedance inputs is shown in Fig. 2. This conceptually simple approach uses two instrumentation amplifiers connected in a complementary way to implement the singled-ended-to-differential function. The key benefit here is that both the input and the offset input see high-impedance loads. Two possible issues are the complexity of implementing the instrumentation amplifiers (the design typically used needs three op amps per instrumentation amplifier) and the output common-mode voltage would still see a signal-dependent load which could be a crosstalk vector (depending on the CMRR of the ADC). These issues are both addressed in the specific implementation details of the instrumentation amplifier.

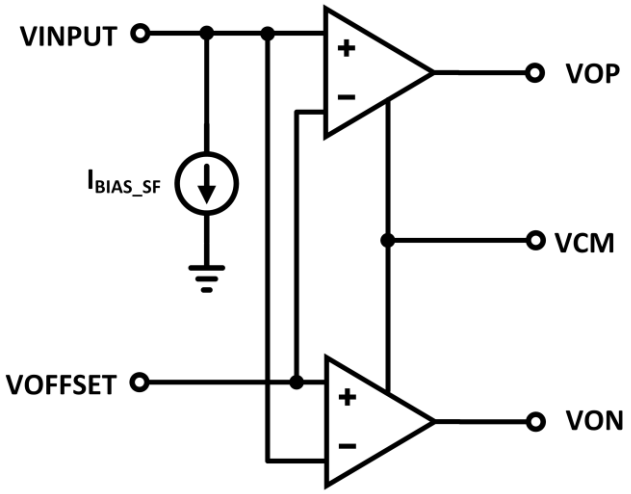

Fig. 2. ADC driver channel. Each amplifier is an open-loop instrumentation amplifier.

As can be seen in Fig. 2, the input node of the ADC driver is biased with a current sink. Since the instrumentation amplifier has a high-impedance input, this current is drawn through the input pin and therefore biases the source follower buffers in the image sensor. These buffers are often biased using external components so biasing them with the ADC driver not only simplifies bias programmability but also reduces the number of components on the board.

C. Open-Loop Instrumentation Amplifier

High-performance instrumentation amplifiers are traditionally implemented in a closed-loop configuration using two or three operational amplifiers to provide precision gain and high linearity [5]. The linearity of CMOS image sensors is typically poor compared to the linearity of closed-loop operational amplifier circuits and this relaxed linearity can be used to simplify the design of the instrumentation amplifier to reduce power. In addition, because the overall channel gain of the sensor is calibrated, the exact gain of the singled-ended-to-differential converter is not important as long as it is sufficient to scale the input so as to use a reasonable fraction of the ADC dynamic range. Lastly, reducing the number of amplifiers reduces the noise of the circuit.

A block diagram of the open-loop instrumentation amplifier implemented in the channel is shown in Fig. 3.

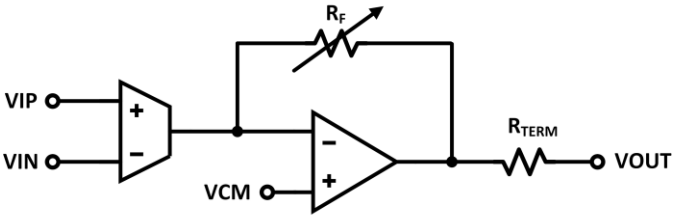

Fig. 3. Open-Loop Instrumentation Amplifier implementation comprising a transconductor and an operational amplifier.

The key idea is to use a transconductor (to provide the high input impedance) followed by a transresistance amplifier (to convert back to voltage). This can be done using another transconductor to generate the current feedback [6] but here we use a simple resistor to generate the current feedback. The amplifier is then back terminated in 50 Ω to reduce reflections when driving the trace or cable between the camera and the high-speed external ADC. The transconductor generates a current that is proportional to the difference of its input voltages. Because of the high loop gain of the op amp, this current is forced to flow through R_F, generating an output voltage. The gain of the circuit is G_mR_F, where G_m is the transconductance of the first stage and R_F is the operational amplifier feedback resistor. Ideally, the transfer characteristic is linear because G_m can be set using a linear device. However, the linearity of this circuit is lower than a traditional instrumentation amplifier for two reasons. First, the current feedback is generated by a resistor rather than a dedicated transconductor and therefore the feedback current is a function of the output voltage. Second, large input signals will cause the input transconductor to saturate. In the intended application (image sensor readout) the linearity requirements are relaxed because the linearity of the sensor is not expected to be better than a few percent.

The channel has three selectable nominal gains: 3, 4, 5. These gains are set by absolute values of g_m and R_F and as such are not expected to be accurate (the gain inaccuracy is less than the gain variation in the imaging pixels and is dealt with during system calibration).

D. Operational Transconductance Amplifier

The transconductance in Fig. 3 is implemented using the folded-cascode transconductor shown in Fig. 4.

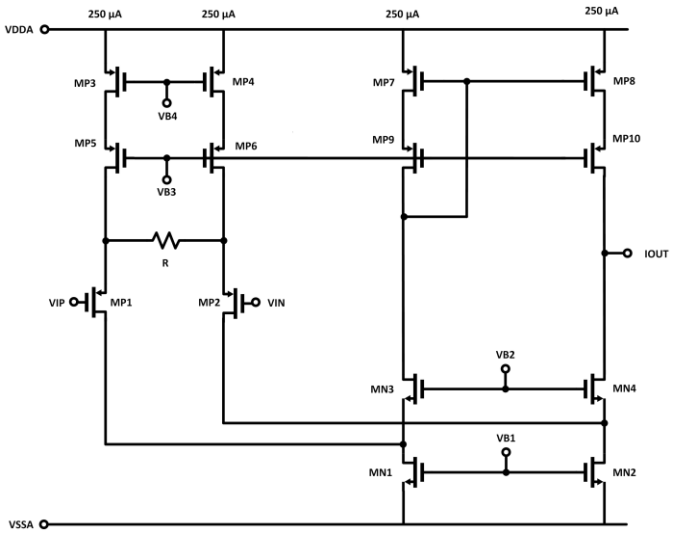

Fig. 4. Folded-cascode transconductor.

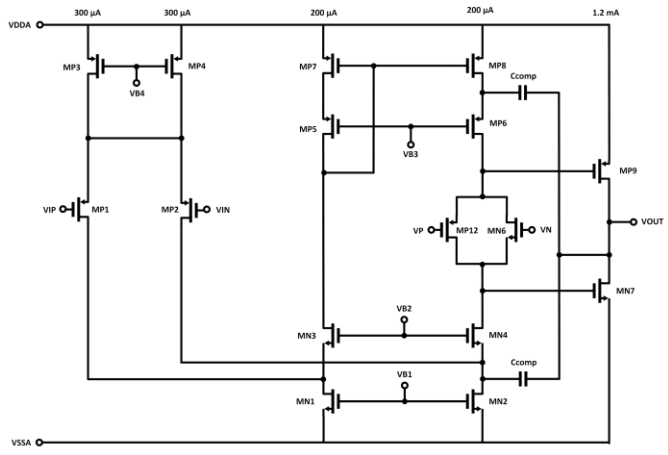

Fig. 5. Operational amplifier using class-AB output stage.

The amplifier works as follows. Assuming the input devices (MP1 and MP2) act as ideal source followers, a current proportional to the input voltage difference flows through resistor R. The transconductance of the stage is, ideally, 2/R, where R is the differential degeneration resistor seen in Fig. 4. In practice, however, the transconductance will be somewhat less than this because the product of R and the transconductance of the input transistors is less than one (i.e. the input devices do not act as ideal source followers). The output current IOUT flows through R_F in Fig. 3 to generate the output voltage of the driver.

E. Operational Amplifier with Class AB Output Stage

The operational amplifier in Fig. 3 that converts the output current of the transconductance amplifier to a voltage is required to deliver significant transient current to the load in order to settle quickly. Therefore, and since low power dissipation is desired, a well-known class AB output stage [7] for the op amp is used. The design was chosen to balance the desire for high speed with the desire for reasonable power dissipation and simplicity.

The operational amplifier schematic is shown in Fig. 5. The amplifier consists of a folded-cascode stage driving a class AB output stage. In addition, devices MP12 and MN6 are replicas of MPB and MNB in Fig. 6., respectively. Split compensation is applied here so the operational amplifier is compensated when both sinking and sourcing current. Since the left sides of the compensation capacitors are not connected to high impedance nodes, there are no right-hand planes zeros to deal with and power supply rejection is improved compared to the standard Miller compensation case [8].

A block diagram of the class AB bias circuit that uses replica biasing to ensure stable performance over process, voltage, and temperature is shown in Fig. 6 [9].

Diode-connected devices MP1, MP2, MN1, and MN2 bias the floating current source (MPB and MNB) at twice vdsat, which puts the common-source output devices (MPCS and MNCS) into a low-current quiescent state.

The signal current is injected into the output stage of the operational amplifier by the preceding differential pair. As an example of the operation of this stage, imagine the op amp differential-pair signal current increases due to the signal. Then, the signal current from the differential will flow into the output resistance of the current source and VX will increase, causing MNCS to sink more current from the load. If VX increases, the VGS of MNB decreases (VN is fixed) and more current will flow in MPB, increasing its VGS. This will cause VY to increase which will tend to turn off MPCS.

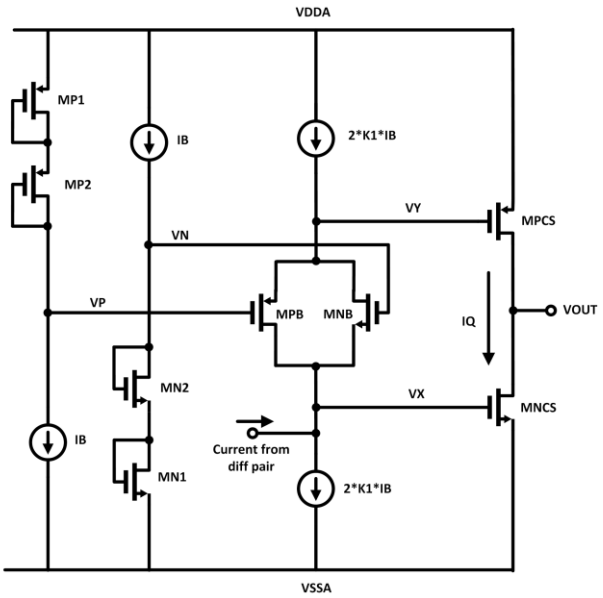

Fig. 6. Class-AB bias circuit.

On the other hand, when the signal current from the differential pair decreases (i.e. the transconductor pulls current out of VX) the opposite situation will occur in that MNCS will tend to turn off while MPCS will tend to turn on. This analysis only works when the signal current from the differential pair is less than half IB. Otherwise, one of the devices of the floating current source will turn off and the stage will be temporarily non-linear. It is not a problem in practice (as long as it is not pushed too far) since the gain provided by the differential stage preceding this output stage will still reject the distortion.

F. Sensor Bias

In addition to the single-ended-to-differential signal path, the ADC driver provides bias currents to the sensor output source follower buffers. The bias currents are programmable via an external resistor to between 1 mA and 3 mA. The currents are filtered to lower noise on-chip and to reject external noise and interference. A schematic of the sensor bias circuit is shown in Fig. 7. An external resistor sets the input current which is mirrored and then multiplied by a factor of 10 using a simple current mirror with long-length devices in order to give low noise and wide output compliance.

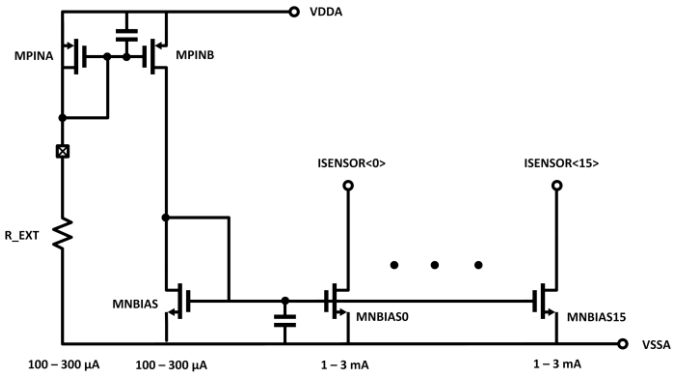

Fig. 7. Sensor bias circuit.

III. Prototype

The 16-channel ADC driver was implemented in a 180 nm CMOS Image Sensor (CIS) technology and fabricated at a commercial foundry. While CIS technology is sub-optimal for high-speed amplifiers, this process was chosen to facilitate potential future integration with an imaging array to further reduce overall system power and board space. A die photograph of the 16-channel fabricated prototype is shown in Fig. 8.

The prototype reduced the board space for this function (previously implemented using commercial standard parts) in the target system by 84% (from 100 mm^2 to 16 mm^2) and the power dissipation for this function by 25%.

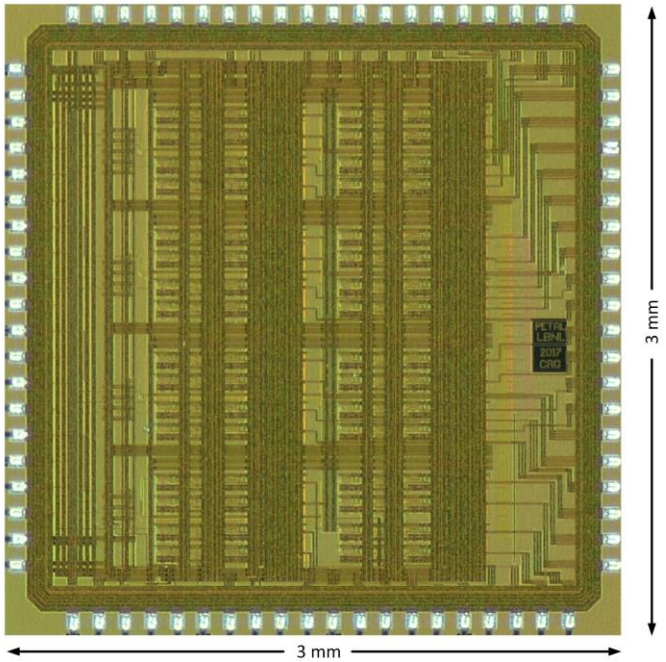

Fig. 8. Die photograph. The dimensions are approximately 3 mm by 3 mm. The single-ended inputs are all along the left side of the chip, and the differential outputs are distributed across the top, right, and bottom sides of the chip.

IV. Measured Results

The measured input-referred noise is shown in Fig. 9. The measurement was made using an idle-channel noise test [10]. In this test, a heavily filtered dc voltage is connected to the input and the differential driver output is measured using a 16-bit ADC. The input-referred channel noise is then simply the rms voltage calculated from the captured samples. The input-referred noise resulting from this measurement is 89.9 µV-rms.

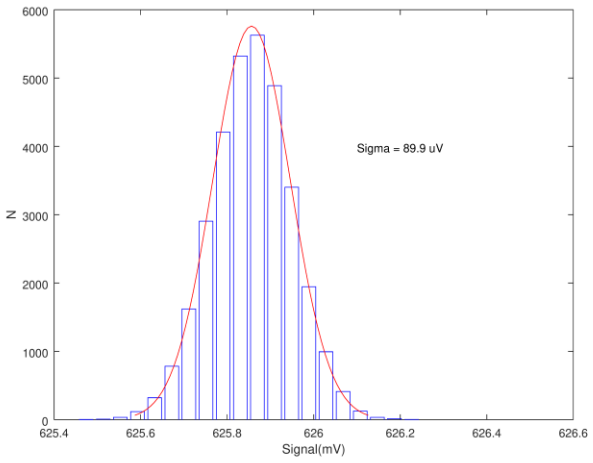

Fig. 9. ADC driver measured noise.

An oscilloscope photograph of typical ADC driver settling into a 6 pF load (after driving a terminated 100-Ω transmission line) is shown in Fig. 10. The ADC driver settles to better than 0.1% in less than 11 ns with a 100 mV input step.

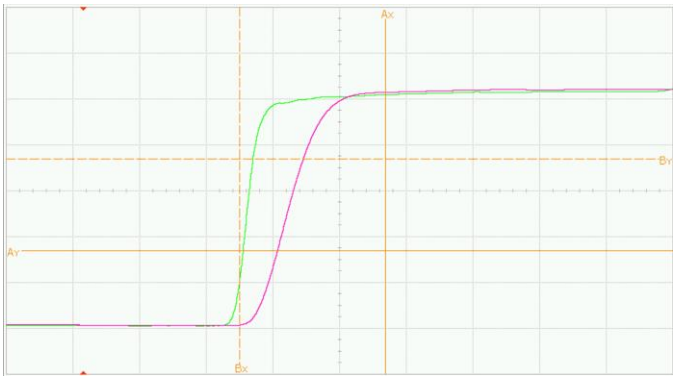

Fig. 10. Measured ADC driver settling. The green curve is the input trace and the pink curve is the output trace. The horizontal scale is 5 ns / division and the vertical scale is 20 mV / division for the input trace and 50 mV / division for the output trace. The measured channel gain is 2.5 here.

Crosstalk is a critical specification for multichannel image sensors. The crosstalk in the prototype was measured by driving a given channel and comparing the driven channel's output with the output of an undriven, adjacent channel. Fig. 11 shows the differential output of an undriven channel when the adjacent channel input is a 500 mVpp square wave. This is a worst case measurement as the channel is continuously swinging from peak to peak. The adjacent-channel crosstalk is approximately -56 dB. The close correlation between the input and output curves in Fig. 11 suggests that most of the crosstalk is happening on the board or between bondwires, rather than internal to the chip. An analysis of expected bondwire coupling agrees with this result. The measured crosstalk provides sufficient margin for the application specification of -50 dB crosstalk between adjacent channels.

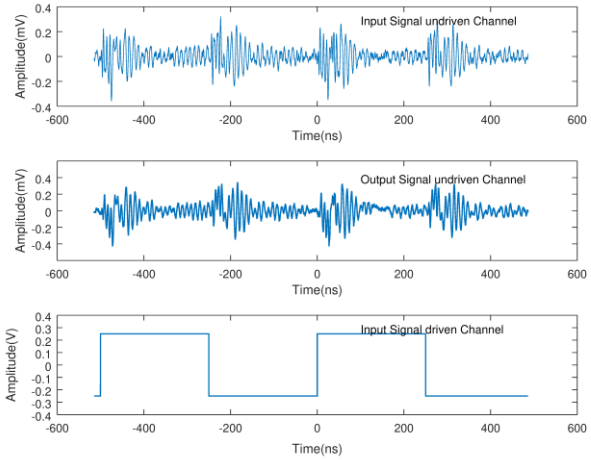

Fig. 11. Adjacent-Channel Crosstalk. The top curve is the input response, the middle curve is the output response and the bottom curve is the stimulus.

The driver linearity was measured by applying a linear ramp to the prototype, fitting its digitized output to a straight line and then defining the linearity as the maximum deviations over the expected swing of the driver. The linearity of the ADC driver measured this way is approximately +/- 0.5%

The measured power dissipation of ADC driver is approximately 10.5 mW/channel, which is significantly lower than commercial solutions that use lower levels of integration.

The measured results of the prototype are summarized in Table 1.

TABLE I. MEASURED RESULTS

ADC Driver Performance: 1.8 V and 25° C		
	Value	Units
CMOS Technology	180	nm
Bandwidth (-3dB)	156	MHz
Settling Time (0.1% with 100 mV input step voltage)	11	ns
Power Dissipation (total)	168	mW
Input-Referred Noise	89.9	µV-rms
Adjacent Channel Crosstalk	<-56	dB
Linearity (100 mVpp input)	0.5	%
Die Area	9.1	sq-mm

V. CONCLUSION

A 16-channel ADC driver array is presented that can reduce the board area, power dissipation, and number of components of a high-speed scientific camera system. The driver achieves 11 ns settling to 0.1% into 6 pF with a 100 mV input step and dissipates 10.5 mW / channel. The measured noise is 89.9 µV-rms.

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