Lawrence Berkeley National Laboratory

Lawrence Berkeley National Laboratory

Title

Determining the critical size of EUV mask substrate defects

Permalink

https://escholarship.org/uc/item/3985w4nj

Author

Han, Hakseung

Publication Date

2008-11-26

Determining the critical size of EUV mask substrate defects

H. –S. Han¹, W. Cho¹, K. A. Goldberg², E. Gullikson², C. Jeon¹, S. Wurm¹

¹Samsung Electronics assignee at SEMATECH, 255 Fuller Road, Suite 309, Albany, NY 12203 USA

²Center for X-ray Optics, Lawrence Berkeley National Laboratory, One Cyclotron Road, Berkeley, CA 94720 USA

February 2008

This work was supported by the Director, Office of Science, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

DETERMINING THE CRITCIAL SIZE OF EUV MASK SUBSTRATE DEFECTS

Hakseung Han^{*1}, Wonil Cho¹, Kenneth A. Goldberg², Eric M. Gullikson², Chan-Uk Jeon¹ and Stefan Wurm³

Samsung Electronics assignee at SEMATECH, 255 Fuller Road, Suite 309, Albany, NY 12203, USA

²Center for X-Ray Optics, Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA

³SEMATECH, 255 Fuller Road, Suite 309, Albany, NY 12203 USA

ABSTRACT

Determining the printability of substrate defects beneath the extreme ultraviolet (EUV) reflecting multilayer stack is an important issue in EUVL lithography. Several simulation studies have been performed in the past to determine the tolerable defect size on EUV mask blank substrates but the industry still has no exact specification based on real printability tests. Therefore, it is imperative to experimentally determine the printability of small defects on a mask blanks that are caused by substrate defects using direct printing of programmed substrate defect in an EUV exposure tool.

SEMATECH fabricated bump type program defect masks using standard electron beam lithography and performed printing tests with the masks using an EUV exposure tool. Defect images were also captured using SEMATECH's Berkeley Actinic Imaging Tool in order to compare aerial defect images with secondary electron microscope images from exposed wafers.

In this paper, a comprehensive understanding of substrate defect printability will be presented and printability specifications of EUV mask substrate defects will be discussed.

Keywords: EUV, Lithography, EUV Masks, EUV defect, printability, EUV inspection,

1. INTRODUCTION

For high volume manufacturing EUV lithography, mask blank defects have always been a major concern. The short EUV wavelength makes lithography sensitive to small variations of the multilayer (ML) and makes mask blank defect control essential. EUVL mask development must be ready to supply masks to wafer fabs before EUV scanners are ready to use. Considering that EUVL is a major candidate for wafer process development in the 2009 or 2010 time frame, defect-free masks and related technology should be available by the end of 2009, which means timing is urgent.

SEMATECH programs have widely covered various EUVL mask devolvement areas such as reducing mask blank defects and enabling the infrastructure for EUVL mask development. SEMATECH's Mask Blank Development Center (MBDC) has been working on reducing EUVL Mask blank defects and has shown great improvement in defect reduction¹. SEMATECH also has successfully developed the infrastructure to study the printability of phase defects in such tools as the EUV Microexposure Tool (MET) and the Actinic Inspection and Imaging Tool (AIT)². The SEMATECH/Berkeley MET is one of the most important tools for EUVL development. The tool has been well used to support resist development by providing lots of user times to industry and has shown one of the best performance EUVL resists³. Separately, the AIT has been used to study EUVL patterned masks without resist effects⁴. Current resists, despite good progress in resolution still show large line width roughness (LWR), making it difficult to study ML defect printability. The focus dependence of ML defects is well known and studying it requires accurate measurement of CD

^{*} Hak-seung.han@sematech.org or hakseung.han@samsung.com; phone +1 518 956 7154; fax +1 518 956 7101; www.sematech.org

variation. The AIT can be used to obtain ML defects-related CD variation dependence on focus since the focus can be changed easily and images can be recorded fast without moving the mask. To evaluate defect printability we fabricated a programmed substrate bump defect mask and studied defect printability in real tests using both the SEMATECH EUV MET and the AIT. This paper reports the results.

2. EXPERIMENT

2.1 Fabrication and structure of programmed defect mask

Hydrogen silsesquioxane (HSQ) bumps were created for a programmed defect mask using an e-beam pattern generation process. This was followed by the deposition of 40 Mo/Si bi-layers using a so-called 'smoothing' process. Finally, an 11-nm-thick Si capping layer was deposited on the ML. The surface roughness of the final ML and the programmed defect sizes were measured using an atomic force microscope (AFM).

A CrN buffer layer and a TaBN absorber layer were deposited on the test plate. Dense lines with 160-nm CD and (1:1 pitch) were patterned using normal e-beam lithography process and absorber etching, corresponding to 32 nm half pitch (HP) dense lines at wafer scale when printed with the SEMATECH/Berkeley 5× reduction MET. Considering a 4× reduction EUVL tool, 160 nm dense lines correspond to 40 nm HP dense lines. A detailed description about fabrication of the programmed defect mask can be found in Reference 5.

Figure 1 shows final programmed defect mask structure with substrate bump and absorber patterns.

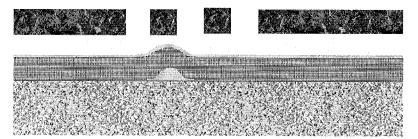


Figure 1. Programmed defect mask structure.

2.2 SEMATECH/Berkeley EUV MET and SEMATECH/Berkeley AIT

The wafer print test was performed using the SEMATECH/Berkeley MET at Lawrence Berkeley National Laboratory (LBNL). This tool is well used by the industry to evaluate resist performance such as resolution and LER and patterned mask quality. The programmed defect mask was exposed under annular illumination conditions. The defect printability was evaluated after resist development using a scanning electron microscope (SEM). The defect printability study requires fine analysis of small variation of CD caused by defects. Resist LWR makes it difficult to measure local CD change. Thus, the effect of ML embedded defects on the aerial test pattern image was assessed using the SEMATECH/Berkeley AIT at LBNL.

This AIT is a unique, dedicated EUVL reticle inspection system operating on a bending magnet beam line at the LBNL Advanced Light Source (ALS). The tool has two main functions, one is scanning inspection mode to catch defects and also local reflectivity changes on ML blank masks; and the other is an imaging mode which records the aerial images of patterned EUVL masks. The imaging mode uses a Fresnel zoneplate lens to emulate a 0.25 numerical aperture (NA) EUVL stepper as shown in Fig. 2. Aerial imaging inspection is more important in the EUVL than in the DUVL process using transmission masks since EUVL uses reflective masks and it is not possible to detect refractive index or phase changes on multilayers in a CD-SEM. However the industry still has no clear solution for the EUV aerial image monitor (AIMS) tools. The SEMATECH/Berkeley AIT will be used as a bridging tool for the time being. Ultimately, standalone EUV AIMS tools must be developed and commercialized to support the EUVL mask-making processes, to prepare EUVL masks before beta wafer lithography processes are employed in the industry.

Aerial images from the mask were obtained to study substrate bump effects from absorber patterns on wafer critical dimension (CD). Images were captured through focus with $0.8~\mu m$ steps corresponding to 50 nm on a 4× scanner. A through-focus image series can be obtained within a few minutes, which makes it possible to analyze focus dependence on phase defect printability. The background signal from the bright field area was used to accommodate illumination non-uniformity.

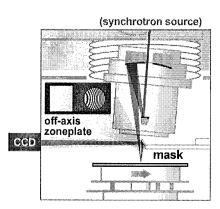


Figure 2. SEMATECH Berkeley Actinic Imaging tool

3. RESULT AND DISCUSSION

3.1 Wafer printing results

Figure 3 shows AFM images and SEM micrographs of MET-printed resist images of the programmed defect mask. 32-nm HP features were clearly resolved as shown in the SEM images; it is clear that the programmed bumps are printable down to 5.4 nm high and 49 nm FWHM. However below that size, it is difficult to determine whether or not the programmed bumps are printable because of the resist's large LWR. CD changes were also too difficult to measure. Thus, we used SEMATECH/Berkeley AIT images to study programmed bumps printability quantitatively.

SEMATECH and other consortia have been worked on improvement of resist resolution and LWR with several suppliers and secured better resists with low LWR and high resolution. We will keep studying substrate printability with these improved resists.

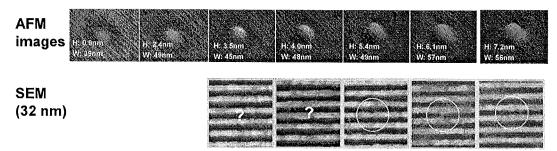


Figure 3. AFM images of programmed bump on ML and MET-printed resist images

3.2 AIT Sensitivity

SEMATECH/Berkeley AIT aerial images were used to determine the CD variation caused by programmed bumps. Figure 4 shows CCD images from the AIT around best focus down to the smallest bump. The programmed bump is in the center of the CCD images and bridges shown in the first three images are absorber fiducial marks to find out where the bumps are. It is clear that the AIT can detect the smallest bump of 0.9 nm high and 39 nm FHWM.

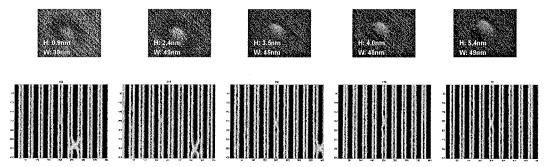


Figure 4. AIT CCD images: Defects are detectable down to the smallest bump of 0.9 nm high and 39 nm FHWM.

3.3 Coherence effect on CD variation according to focus change

Considering that phase defect printability depends on focus, we must study the effect of focus on substrate defect printability. In addition to that, the AIT has a $0.2~\sigma$, which is much lower than in real scanners. We performed a simulation study to determine what effect this high coherence would have on the CD variation as a function of focus. Figure 4 shows CD change as a function of focus at $0.2~\sigma$ and 40 nm HP. According to the model, the CD did not change significantly around best focus. The CD variation within 100 nm focus range (wafer-side) is less than 1 nm around threshold. We assumed at least focus margin which CD variation stays below specification should be more than 100 nm (not sure what oyu want to say here). Figure 5(b) shows CD variation with focus change at $0.5~\sigma$. CD variation also was less than 1 nm within 100 nm around center.

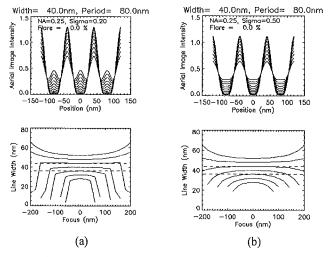


Figure 5. CD change vs focus as a function of threshold (a) sigma 0.2 (b) sigma 0.5

3.4 AIT image analysis and specification

The 'space CD' was used to assess printability of bumps. Figure 6 shows CCD image and corresponding CD variation of space using threshold. AIT has some illumination non-uniformity and because of that there is also CD variation. Thus, we determined a 'baseline' CD from adjacent areas and used that to measure CD independent of the illumination non-uniformity. Also, since both lines and spaces affect CD they must be considered together. Thus, we used a 15% CCD-change specification corresponding to 6 nm, instead of 10% of dark CD. In the previous section, there was a maximum 1 nm variation from focus dependence, which means that the change in CD caused by a defect should be below 5 nm instead of 6 nm. Ultimately, the 5 nm specification was used to determine whether the substrate defects were printable or not.

In Figure 6, both (a) and (b) were obtained from a bump of 5.4 nm high and 48 nm FWHM. In case (a) with the bump in the space area, the defect is more pronounced; it makes a CD change of about 8 nm. In case (b), the bump is in the absorber area, and it had no noticeable effect on CD.

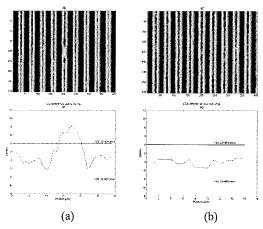


Figure 6 AIT CCD image and corresponding CD variation caused by programmed bump of 5.4 nm high and 48 nm FWHM in both (a) and (b)

CD changes with respect to focus variation were obtained and displayed in a graphs as shown in Figure 7. Figure 7 (a) and (b) show the focus dependence of CD changes corresponding to Figure 5, respectively. We observe that case (a) has no margin, which means the bump always cause CD changes of more than 5 nm through focus. However, case (b) has CD variations that are less than 5 nm through focus and a calculated margin of 609 nm: enough for an exposure process. As in the previous section, we assumed that bump defects with more than 100 nm focus margin are not printable.

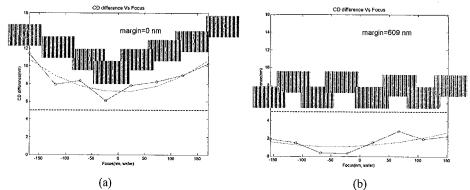


Figure 7 AIT Calculated focus margin of programmed bump of 5.4nm high and 48nm FWHM in both (a) and (b):

The bump is in space in (a), and is under absorber line in (b).

3.5 Focus margin according to distance to absorber

With the programmed defect mask used, there was no fixed-reference alignment between the substrate bumps and the absorber lines. Nonetheless, the bump to absorber line distance could be determined because the bumps and absorber patterns have their own regular periodicity, respectively. The bumps have a discrete pitch of 20 μ m, and that was used to guess the distance to the absorber.

Figure 8 (a) shows the focus margin according to spacing to absorber in the case of a bump 5.4 nm high and 48 nm FWHM. Negative values mean that the bumps were below the absorber lines. The maximum deviations were 80 nm for

both sides because the mask has 160 nm HP patterns. In total, five defects were analyzed: all bumps below spaces had no focus margin, and all bumps below absorbers had focus margins larger than 250 nm.

Figures 8 (b) and (c) show bumps of 4.0 nm high and 3.5 nm high, respectively. Most bumps below the absorber lines show a focus margin of more than 250 nm, but bumps below spaces show no focus margin—yet case (c) does have more than 100 nm margin. Figures 8 (d) and (f) are the 2.4 nm high and 0.9 nm high bumps, respectively. For these small size defects, it was difficult to analyze CD variations due to the low signal to noise ratio. In both cases, all bumps have more than 100 nm margin, which means these bumps are not printable. In summary, ML bumps above 3.5-nm high and 45-nm FWHM are printable, and ML bumps below 2.4 nm high and 48 nm FWHM are not.

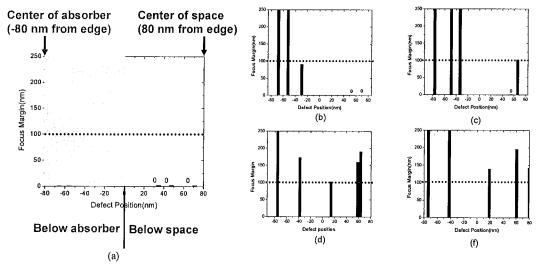
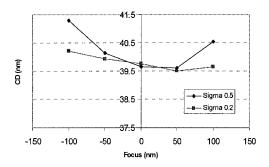


Figure 8. focus margin according to spacing to absorber. (a–f) corresponds to 5.4 nm high and 48 nm FWHM, 4.0 nm high and 48 nm FWHM, 3.5 nm high and 45 nm FWHM, 2.4 nm high and 48 nm FWHM and 0.9 nm high and 39 nm FWHM, respectively.

3.6 Coherence dependence study using simulation

Since the AIT illumination used in these studies has high coherence, we studied the effect of coherence (σ) on ML bump printability using the single surface approximation method simulation developed by Gullikson⁶. In Figure 9, graphs in (a) and (b) show the CD variation caused by bumps that were 0.9-nm high with 39-nm FWHM, and those that were 2.4-nm high with 48-nm FWHM. The difference between $\sigma = 0.2$ and 0.5 is negligible within 100 nm range from the center, but it becomes larger out of that range. Considering our most important is 100 nm (need to reword), it is reasonable to use σ of 0.2 instead of sigma 0.5 for these sizes of bumps.

The maximum CD change within 100 nm focus was obtained with various sizes of bumps. From Figure 10, ML bumps of 2.9 nm high and 45 nm FWHM show CD changes over 5 nm in the case of 0.5 σ . This result is well matched to the test result. Figure 10 also shows there is a ~0.5 nm gap between σ values of 0.2 and 0.5 for the critical bump size. In conclusion, considering a real EUV scanner with 0.5 σ , the critical bump size from this simulation study is about 2.3 nm high and about 45 nm FWHM based on this simulation and test study. However it should be noted that this study did not consider resist effects, which will be included in a future study.



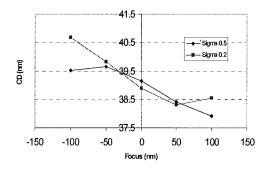


Figure 9. Simulated CD variation caused by (a) bumps of 0.9-nm high with 39-nm FWHM, and (b) 2.4-nm high and 48-nm FWHM with two different σ values.

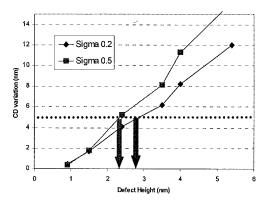


Figure 10. Maximum CD variation dependence on sigma difference

3.7 AIT Upgrade for bridging tool and necessity of standalone EUV AIMS Tool

As mentioned in the previous sections, the SEMATECH/Berkeley AIT has some illumination non-uniformity and high coherence. SEMATECH and LBNL are now upgrading the tool to improve the illumination uniformity and achieve lower coherence (higher σ). In addition, new zoneplates with higher NA up to 0.35 and magnification ratios have been installed to support even 2× HP mask imaging. In addition a new CCD with 240% higher pixel density will help to measure CD values more accurately.

SEMATECH's AIT has been and continues to provide an interim solution for aerial imaging until commercial standalone EUV AIMS tools become available. It is almost impossible to verify printability of ML defects using EUV scanner and also to repair ML defect without EUV AIMS tools.

For EUV lithography, AIMS tools are much more important than defect review tools at DUV wavelength because DUV pattern inspection can not detect ML defects. The industry must address the critical EUV AIMS tool gap as soon as possible to enable a pilot line introduction of EUVL in 2010.

4. SUMMARY

Multilayer defect printability has been studied with SEMATECH's EUV lithography infrastructure to understand substrate bump-size effect on wafer CD. A programmed defect mask with multilayer bumps and dense lines was fabricated and analyzed using SEMATECH EUV MET and AIT in Berkeley. Dense line width was 160nm, corresponding to 32nm on a wafer in a 5x demagnification tool and 40nm in 4x tool. EUV AIT CCD image analysis show that, considering at least 100nm focus margin should be secured for EUV scanner exposure, ML bumps down to 3.5nm high and 45nm FWHM are printable and ML bumps below 2.4nm high and 48nm FWHM are not. From the AIT

test result and the simulation study result and considering AIT's high coherence, the critical bump size is about 2.3nm high and about 45nm FWHM at 40nm HP dense line. The AIT is now being upgraded for high NA and better illumination uniformity and will be employed for further study in near future.

Though the AIT can well support current development needs, it is critical that a commercial standalone EUV AIMS tool becomes available soon to support EUVL mask fabrication because DUV pattern inspection is not sufficient for printability verification of mask defects in the EUVL era.

5. ACKNOWLEDGMENTS

The authors would like to thank to Hoon Kim, Won-Sun Kim, Sang-Hoon Han, Ni-Eun Kim, and Sungmin Huh of the Samsung Photomask team for helping us manufacture the test plate. The programmed embedded defect mask blank was fabricated by Farhad Salmassi of LBNL and Paul Mirkarimi of LLNL. The authors also would like to thank Patrick Naulleau, Senajith Rekawa, and C. Drew Kemp of LBNL; Tsutomu Shoki of HOYA; Anwei Jia of Lasertec USA; and Abbas Rastegar, James Kuss, Butch Halliday, and Nancy Lethbridge of the SEMATECH's MBDC for their helpful inputs and efforts.

REFERENCES

Chan-Uk Jeon, C.C. Lin, "Beta-level EUV Mask Blanks for the 32nm Half-Pitch," EUVL Symposium 2007, Sapporo, Japan, October 31, 2007.

K. A. Goldberg, P. P. Naulleau, A. Barty, S. B. Rekawa, C. D. Kemp, R. F. Gunion, F. Salmassi, E. M. Gullikson, E. H. Anderson, H.-S. Han, "Performance of actinic EUVL mask imaging using a zoneplate microscope," *Proc. SPIE* 6730, 67305E-1-12 (2007).

³ Andy Ma, Joo-on Park, *et al.* "SEMATECH EUV Resist Benchmarking Results," *EUVL Symposium 2007*, Sapporo, Japan, October 31, 2007.

G.-S. Yoon, H. Kim, H.-J. Oh, H.-S. Kim, H.-S. Sim, S.-H. Lee, G.-B. Kim, S.-M. Huh, K. A. Goldberg, A. Barty, S.-S. Kim, H.-K. Cho, "Evaluation of EUV Mask Repair Methods in Si-capping & Ru-capping Blanks," *EUVL Symposium 2007*, Sapporo, Japan October 31, 2007.

W. Cho, H.-S. Han, K. A. Goldberg, P. A. Kearney, C.-U. Jeon, "Detectability and printability of EUVL mask blank defects for the 32 nm HP node," *Proc. SPIE* 6730, 673013-1-9 (2007).
 E.M. Gullikson *et al.*, *Proc. SPIE* 5374, 791 (2004).