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Solid-state bonding of silicon chips to copper substrates with graded circular micro-trenches

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Abstract
Silicon (Si) chips of 5 mm × 5 mm were bonded directly to copper (Cu) substrates using solid-state process at 300 °C without using any die-attach materials. A static pressure of 6.9 MPa was applied. To deal with the large mismatch in coefficient of thermal expansion (CTE) between Si and Cu, graded circular micro-trenches were fabricated on the Cu substrates. The micro-trenches provide space for Cu material to move into during the bonding process where the Cu surface incurs plastic deformation to conform to Si bottom surface for intimate contact. The micro-trenches also help relax stresses on the bonding interface caused by the fact that Cu contracts significantly more than Si during cooling down. The results obtained are encouraging, implying that the concept of using micro-trenches work. Scanning electron microscopy (SEM) images on cross sections of bonded structures show that Si chips were well bonded to Cu substrates without voids or defects on the interface and without any cracks on Si chip. Shear test were performed on six samples. It turned out that, of all six samples, the Si chip fractured first and the entire Si bottom surface was stilled well bonded to the Cu substrate. The average breakage force of Si chips on six samples is 13.5 Kgf. The breakage force of the joint cannot be determined but is certainly higher than 13.5 Kgf, which is more than twice of the specification American Military Standard. The new chip bonding structure with solid-state process reported in this paper eliminates the use of die-attach materials and the thermal resistance associated with the die-attach. It also removes the operating temperature limit constrained by the melting temperature of die-attach materials. We except this new bonding structure design to be a valuable alternative to high power and high temperature devices.

1 Introduction

Nowadays, in view of the advance of high density integrated circuits (ICs) and high power devices, the density of power dissipation has been in rapid growth, which requires better thermal management solutions. In electronic packaging, the die-attachment is usually the place that inhibits efficient heat conduction. To reduce its thermal resistance, materials with high thermal conductivity and high temperature stability are highly preferred as the die-attachment material. The melting temperature of traditional high temperature solders such as gold–tin (Au–Sn) eutectic and high-lead (Pb) alloys is limited to 300 °C [1]. Higher temperature alloys require even higher process temperature to melt the alloy. A technique to produce high temperature joints at low process temperature is the solid–liquid inter-diffusion (SLID) process [2]. In this process, the low melting point element melts first and reacts with the high melting point element to form a new phase that has high melting temperature. The intermetallic compounds (IMCs) formed in the joint, if any, can be converted into solid solution phase by post annealing, as demonstrated using the silver–indium (Ag–In) system [3], where the resulting structures made between silicon (Si) chips and copper (Cu) substrates survive 5000 thermal cycles between −40 and +200 °C. Recently, nano-Ag paste sintering technique has attracted much research interest [4–6]. After a decade of improvement, the sintering temperature of pressure-less process has been reduced to 275 °C [7]. The challenge of this technique is that the pores in the Ag joint produced during the sintering process cannot be eliminated. Most of these pores are connected. Oxygen can easily penetrate through these pores to reach the substrate surface such as Cu and oxidize it at elevated temperature, thus largely weakening the joint strength [8, 9].

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A challenge of Si die-attachment process is the large mismatch of the coefficient of thermal expansion (CTE) between Si chips and Cu lead-frames or substrates, i.e., 3 versus 17 ppm/K. The stress induced by CTE mismatch may result in chip cracking or joint weakening. One method to mitigate this issue is the direct bonded copper (DBC) structure where relatively thick (200 μm) Cu foils are bonded onto ceramic substrate, as portrayed in Fig. 1. The equivalent CTE of the DBC structure is 7.2 ppm/K [10–12], which has been confirmed to perform better during high temperature storage (HTS) test and thermal cycling (TC) test [6, 9]. So far, DBC substrates have been widely used in high power modules installed in electric vehicles (EV), hybrid cars and aerospace power management units [13, 14]. However, bonding medium such as high temperature solder or nano-Ag paste is still needed to bond active chips to DBC, which inevitably increases the heat dissipation path. In addition, the ceramic within the DBC substrates (Al2O3 or AlN) has relatively lower thermal conductivity compared to Cu or other metals [14]. Therefore, there is still room for improvement in terms of bonding structure design.

In our previous research, pure Ag was selected as the bonding medium because of its superior physical properties, high ductility, and high melting temperature. Silicon (Si) chips were bonded to copper (Cu) substrates using 10 μm Ag layer [15]. Neither solder nor flux was used. The bonding was achieved by solid-state mechanism without molten phase involved. Successful solid-state bonding requires the Ag surface to deform and conform to the Cu surface within atomic distance [16]. To assist deformation and plastic flow of the Ag layer during bonding, 25 × 25 array of cavities of 200 μm in pitch and 100 μm in diameter was fabricated in the Ag layer. These cavities provide space for the extra Ag to flow into. Thus, the Ag flow distance is reduced from half of the chip size to half of the pitch of the array. In other words, the flow requirement is reduced from global to local movement that is determined by the pitch of the cavity array rather than by the chip size. The experimental results show that the Ag layer with cavities was able to manage the large CTE mismatch between Si chip and Cu substrate.

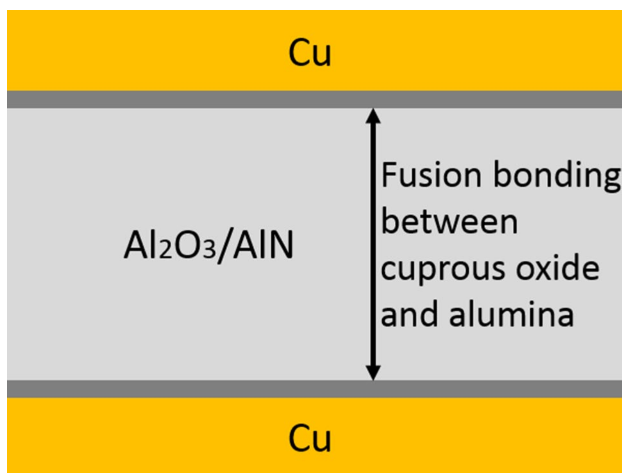

Fig. 1 Typical direct bonded copper (DBC) structure

In this research, the Ag layer on Cu substrates is reduced to 1 μm just to passivate the Cu surface. Thus, the Si chip is practically bonded directly to the Cu substrate without any die-attachment material. To deal with the CTE mismatch, circular micro-trenches are fabricated on Cu substrates before Ag passivation. The concept is that the trenches allow the Cu land regions between them to deform more easily in the shear direction. The trenches are graded in the radial direction, denser at larger radius where differential lateral displacement caused by CTE mismatch between Si and Cu is larger. The trenches also provide space for Cu land regions to move into during bonding, thus helping Cu land surface to deform and conform to the Si chips. In the following sections, experimental design and procedures are first presented. Experimental results are reported and discussed. A short summary is then given.

2 Experimental design and procedures

The major steps of fabricating the micro-trenches on the Cu substrate are illustrated in Fig. 2. Pure (99.8%) quarter-hard Cu sheets (0.8 mm in thickness) are firstly cut into 23 mm × 23 mm substrates. They are slightly polished to remove oxides and cleaned by acetone and de-ionized (DI) water. The photolithographic process is first performed. Briefly, drops of AZ4620 photoresist (AZ® Electronic Materials) are dispensed on the Cu substrate, which is spun on Laurell spinner at 2500 rpm for 30 s. The thickness of the photoresist is 9 μm, as measured by Dektak 3 surface profilometer. After soft bake at 90 °C, the sample is placed underneath a quartz photomask and exposed with UV light on Karl Suss MA6 Mask Aligner. After exposure, the sample is developed using diluted AZ4620 developer, rinsed by DI water and dried. Then, hard bake is performed at 120 °C for 3 min to increase the adhesion and strength of the resulting photoresist pattern. The photomask pattern is shown in Fig. 3 where clear regions correspond to micro-trenches. The area of the pattern is 5 mm × 5 mm which is also the Si chip size. Design data are listed in Table 1. The width of micro-trenches on the photomask is fixed at 25 μm, which will become wider on the Cu substrate due to lateral etching. The width of annulus lands is 500 μm for the inner three and 250 μm for outer ones.

To transfer the pattern on photoresist to the Cu substrate, etching process is performed. The etchant is ferric chloride ($FeCl_3$) solution from outsource (MG Chemicals 415 Ferric Chloride Liquid). Importantly, the etching rate by $FeCl_3$

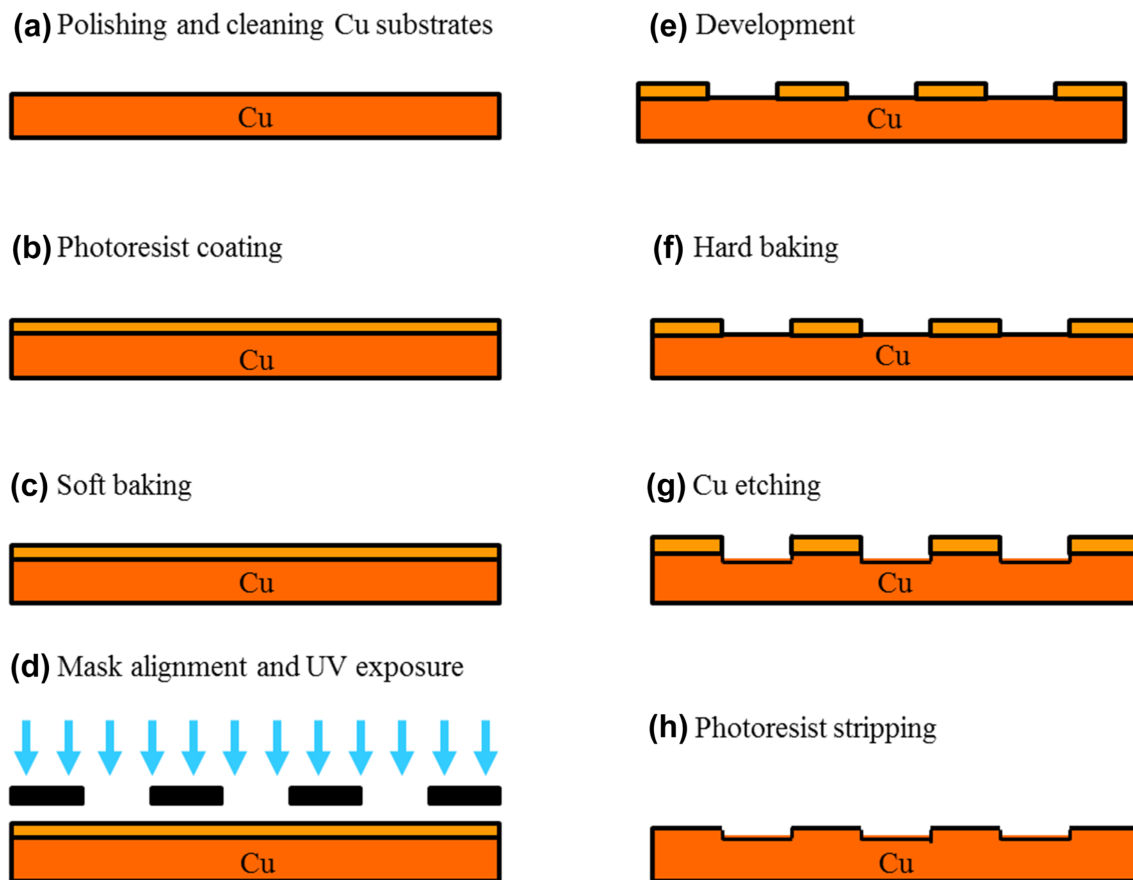

Fig. 2 The major steps of fabricating micro-trenches on Cu substrate **a** Polishing and cleaning, **b** Photoresist coating, **c** Soft baking, **d** Mask alignment and UV exposure, **e** Development, **f** Hard baking, **g** Cu etching, and **h** Photoresist stripping

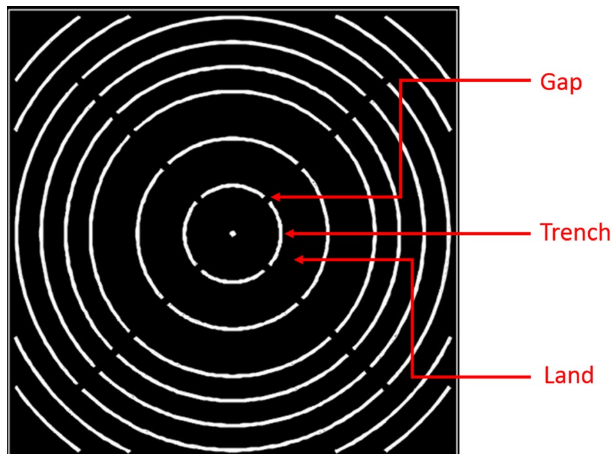

Fig. 3 The photomask where clear regions correspond to micro-trenches

highly depends on the processing temperature [17]. In this project, the Cu substrates with photoresist are soaked in the $FeCl_3$ solution for 5 min at 50 °C. The etching rate is measured to be 6 µm/min at 50 ± 2 °C. After etching, the photoresist is stripped by soaking in acetone. The final depth of trenches is measured to be 30 µm. To prevent oxidation, 1 µm Ag layer is electroplated over the Cu substrate at room temperature right after photoresist stripping.

To produce blank chips, 30 nm chromium (Cr) and 100 nm gold (Au) are deposited onto the polished side of 3-in. Si wafers by E-beam deposition in one vacuum cycle (5×10^{-6} torr). Cr provides strong adhesion to Si and Au prevents Cr from oxidation. After deposition,the wafers are diced into 5 mm × 5 mm chips which are ready for bonding. The metallized Si chip and Cu substrate with micro-trenches are held together by a fixture with a pressure of 1000 psi (6.9 MPa) onto a graphite heater stage in a vacuum chamber [18]. The chamber is then pumped down to 0.1 torr and the graphite stage is heated to 300 °C in 5 min, kept isothermally for 5 min, and cooled down naturally in vacuum. It is worth pointing out that the pressure used in our process is much lower than traditional thermal compression processes [19]. After bonding, the samples are mounted in epoxy resin, cut into halves, and polished for cross-sectional study. Optical microscopy (OM) and scanning electron microscopy (SEM) are used to check the etched pattern and the bonding quality.

Table 1 Numerical data of the micro-trenches

Designed pattern	Width (μm)	Cumulative radial position (μm)
Center reference cavity	25 (radius)	25
Land 1	500	525
Trench 1	25	550
Land 2	500	1050
Trench 2	25	1075
Land 3	500	1575
Trench 3	25	1600
Land 4	250	1850
Trench 4	25	1875
Land 5	250	2125
Trench 5	25	2150
Land 6	250	2400
Trench 6	25	2425
Land 7	250	2675
Trench 7	25	2700
Land 8	250	2950
Trench 8	25	2975
From the center to corners		3536

Then, shear test is conducted by using Nordson Dage 4000 to evaluate the bonding strength. The shearing speed is set at 500 μm/s. Finally, the fracture modes and surfaces are studied.

3 Experimental results and discussion

Figure 4 exhibits the optical image of the etched sample before stripping photoresist. It is clearly seen that the trenches were successfully built on the Cu substrate. After stripping the photoresist, the sample was uniformly electroplated with 1 μm thick Ag. Figure 5 shows the details of the sample surface afterwards. Due to lateral etching of Cu, the trench width increased from 25 to 75 μm and gap width was reduced to 50 μm. In the meantime, the width of the inner and outer annulus lands decreased from 250 to 200 μm, and 500 to 450 μm, respectively. Figure 6 display cross-section SEM images after the etching process. The depth of trenches is approximately 30 μm.

Figure 7 show cross-section SEM images of a bonded sample. It is observed that the chip/substrate bonding interface is clear and sharp without defects and voids. There are no cracks within the Si chip, which indicates that the whole structure is capable of managing the strains induced by the CTE mismatch between Si and Cu. The minor chipping of Si chip above the trench shown in Fig. 7b is caused by the polishing process. It is worth mentioning that the Si

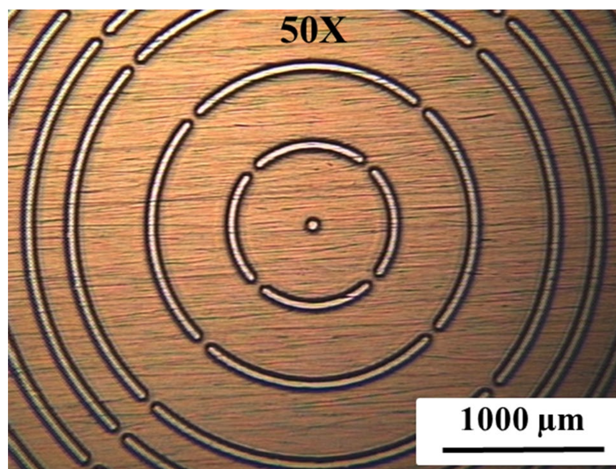

Fig. 4 The optical microscopic image of Cu substrate after the Cu etching process

chips were coated with thin Cr and Au layers and Cu surface was coated with thin Ag. Thus, solid-state bonding on the interface is between Au and Ag atoms. Given that the CTE mismatch between Cu and Si is really large, it is amazing that no cracks were induced when the sample cooled from 300 to 25 °C. The mechanism can be explained as follows with the help of Fig. 8b. At 300 °C, the atoms from Au and Ag sides are brought within atomic distance and begin to share outer electrons with each other. As a result, solid state bonding takes place as was reported in literature [16]. Since both chip and substrate can deform freely before bonding, the as-bonded structure is at zero stress state at 300 °C. During cooling, Cu contracts significantly more than Si. The difference in lateral contraction can produce large stresses along the interface, inducing possible Si cracks or

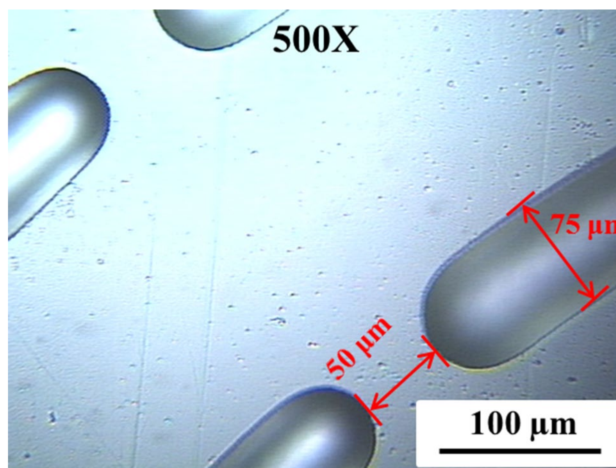

Fig. 5 The optical microscopic image of Cu substrate after the Ag electroplating process

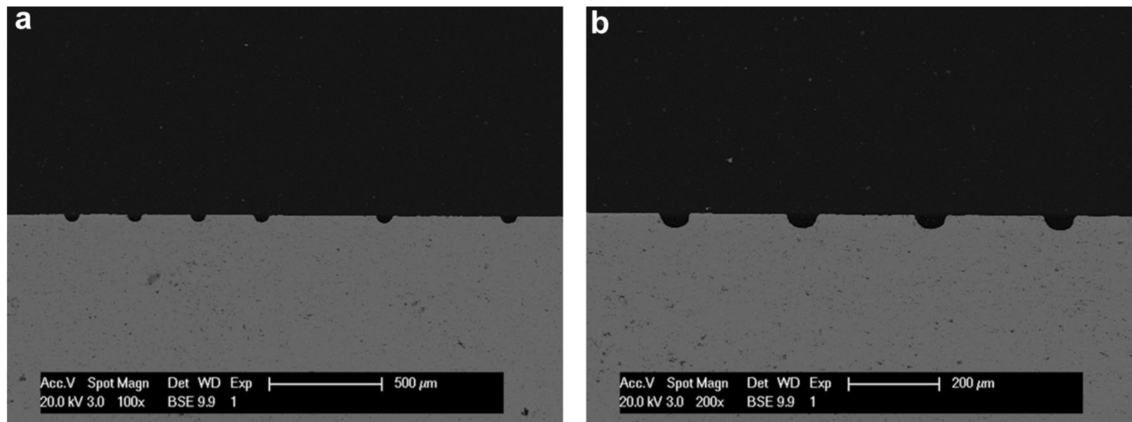

Fig. 6 The cross-section SEM images of Cu substrate with trenches before the solid-state bonding process

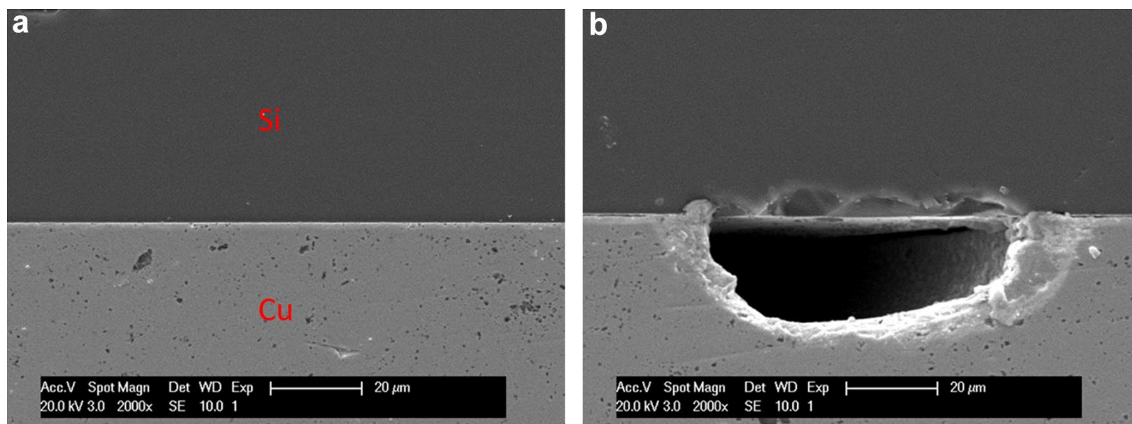

Fig. 7 Cross-section SEM images of a bonded sample. **a** A bonded region without trenches. **b** A bonded region with a trench

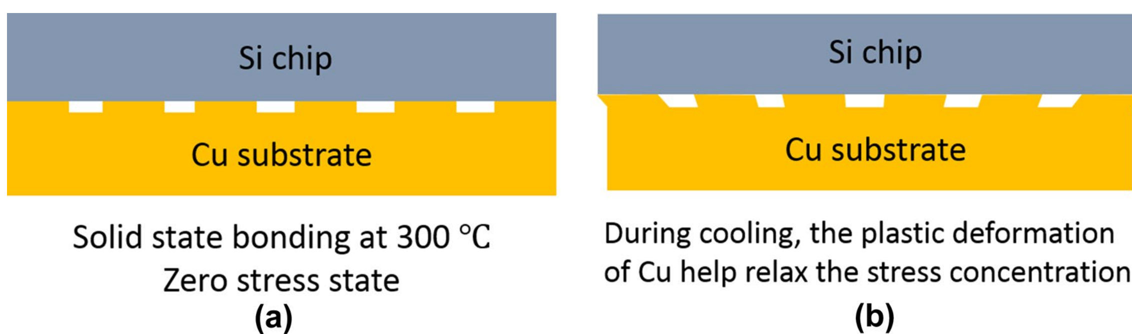

Fig. 8 Stress concentration relaxation mechanism

joint breakage. However, no cracks are observed in the final bonded structure at room temperature, which implies that the stress induced by CTE mismatch is relaxed during cooling. As illustrated in Fig. 8b, the trenches help the land regions to absorb the difference in lateral contraction and facilitate plastic deformation by providing space for plastic flow. The clue can be found in Fig. 7b where the trench region is plastically deformed and becomes asymmetric after cooling down to room temperature. The deformation form is similar to the trenches lying on the right side in Fig. 8b. Based on data in

Table 2 Typical physical properties of materials involved at room temperature [20–22]

Materials	Coefficient of thermal expansion (ppm/K)	Young's modulus (GPa)	Yield strength (MPa)
Si	2.6	160	1200–3000
Ag	18	80	56.6
Cu	17	128	100

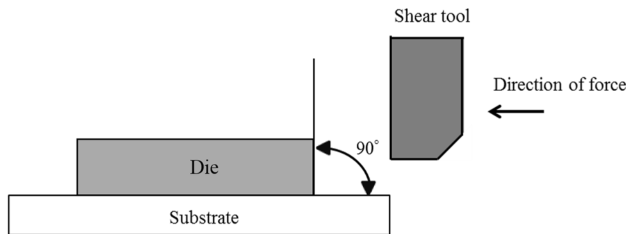

Fig. 9 Settings of die shear test

Table 3 Shear test results of six samples

Average breaking force (Kgf)	Average shear strength (MPa)	Standard deviation (MPa)
13.5	6.71	0.75

Since the chips broke first and the chip bonding was intact, the breaking force measured is the breaking force of Si chips rather than the bonding

Table 2, Ag and Cu have very low yield strength compared to Si. The yield strength decreases when the temperature is elevated. When the stress induced by CTE mismatch reaches the yield strength of Ag and Cu, the metals deformed plastically to relax stress concentration.

Regardless of how good the bonding interfaces look under optical microscope and SEM, the strength of samples is still unknown until it is measured. A commonly used method to determine the strength is the shear test, as illustrated in Fig. 9 [23]. Testing parameters are specified in American Military Standard (MIL-STD-883H method 2019.8) [24]. Six samples were tested and the average breaking force, corresponding shear strength and standard deviation are listed in Table 3. It is worth stating that the actual bonding area is the area of the chip subtracted by the area of trenches, that is, 19.7 mm^2. The ratio of bonding area and chip size of our design is 0.79. It is seen that the breaking force is 13.2 Kgf which is more than twice of the value specified in MIL-STD-883H (5 Kgf). Figure 10 shows the typical fracture mode and fracture surface. Of all six samples, the Si chip fractured rather than being sheared off. The fracture initiated at the edge of the chip followed by cleavage. Since the shear tool applied force on the chip edge and the shear speed

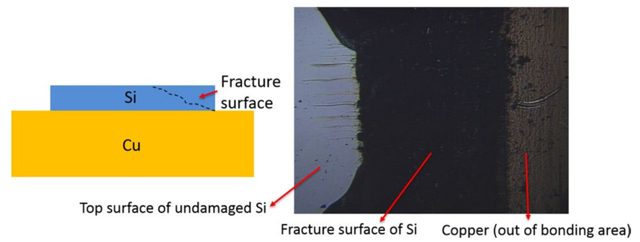

Fig. 10 The typical fracture mode and top view of shear tested sample. All six samples fractured the same way. The entire bottom surface of the Si chip is still bonded on the Cu substrate

is quite high, the stress concentration there broke the chip, which has been reported elsewhere [25, 26]. On Fig. 10, it is seen that the entire bottom of Si chip is still bonded to the Cu substrate. Thus, what the shear test actually measured is the fracture force of the Si chip rather than the shearing off force of the joint. Since the chip broke first before the bonding, the bonding strength cannot be determined. It is worth mentioning that the bonding is between Ag and Au in our design. Based on previous study [27], pure Ag can be easily bonded to pure Au since both of them are very soft and thus easy to deform during bonding and they are free of oxidation issues. No IMCs form between Ag and Au, which is an indication of high long-term reliability.

4 Summary

In this research, Cu substrates were fabricated with graded circular micro-trenches and electroplated with thin Ag layer for passivation purpose. Si chips were bonded directly onto the Cu substrates without any die-attach material at 300 °C with 1000 psi static pressure in 0.1 torr vacuum using solid-state bonding principle. Prior to bonding, the Si chips were coated with thin Cr and Au layers. Cross-section SEM examination and shear test were performed. Important results of this new chip bonding design are summarized as follows:

a. Despite large CTE mismatch between Si and Cu, the bonded Si chips did not break after the samples cooled down from 300 °C bonding temperature to room temperature, indicating that the whole structure could manage the induced shear stresses.
b. The micro-trenches on Cu substrates ease plastic deformation of Cu material during cooling down, thus relaxing induced thermal stresses.
c. The shear tester measured an average breaking force of 13.5 kgf, far exceeding the 5 kgf requirement specified in Military Standard, MIL-STD-883H method 2019.8.
d. During shear test, the Si chips broke first and the entire Si bottom surface was still well bonded on the Cu sub-

strate. Other than being higher than 13.5 kgf, the breaking force of the joints cannot be determined.

In this new chip bonding method, no die-attach material was needed, no flux was used, and no molten phase was involved. It is environmentally friendly because no hazardous chemicals are required to clean the flux residues as in the case of soldering processes. The operating temperature of the bonded structures is limited by the melting temperature of the thin passivation Ag layer, 952 °C. Accordingly, the new chip-bonding design should be valuable alternative for high temperature electronics. It is likely the structures themselves can survive a continuous operating temperature of 500 °C.

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