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Authors

Zhang, Yong

Huang, Chi-Hsin

Nomura, Kenji

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High mobility wide bandgap amorphous-Gallium Oxide thin-film transistors for NMOS inverters

Yong Zhang,[1] Chi-Hsin Huang,[1] and Kenji Nomura[1,2 a)]

[1]*Department of Electrical and Computer Engineering, University of California San Diego, 9500 Gilman Dr., La Jolla, California, 92093, USA*

[2]*Materials Science and Engineering Program, University of California San Diego, 9500 Gilman Dr., La Jolla, California, 92093, USA*

a) Corresponding author: Kenji Nomura

E-mail: kenomura@ucsd.edu

Tel: +1-858-246-2349

ABSTRACT

Wide bandgap Gallium Oxide thin-film transistor (TFT) is promising for next-generation sustainable energy-efficient power electronics. In particular, amorphous oxide channel exhibits inherent advantages on mass-productions based on a low-temperature processability compatible with cost-effective large-sized glass. Here, we developed hydrogen defect termination to produce amorphous GaO_x (a-GaO_x) channel for *n*-channel oxide-TFT and demonstrated high-mobility a-GaO_x-TFT exhibiting a high saturation mobility (μ_{sat}) of ~31 $cm^2V^{-1}s^{-1}$, threshold voltage (V_{th}) of ~3.3 V, a current on/off ratio of ~10^8, and subthreshold swing value (*s*-value) of ~1.17 $V{\cdot}dec^{-1}$. The study found that oxygen conditions during the channel fabrication process, i.e., oxygen partial pressure during the film deposition and post-thermal annealing atmospheres, were critical for the TFT performances of Gallium Oxide-TFTs, and subgap defects originated from low-valence Ga^+ state and excess oxygen rather than oxygen vacancy had a large responsibility for the device performances. The finding explains why the development of Gallium Oxide-TFTs is largely behind the other oxide-TFTs. We also fabricated depletion and enhancement-mode a-GaO_x-TFTs and developed a full-swing zero-V_{GS}-load inverter with high voltage gain ~200, and sufficient noise margins. The presented study demonstrates a high potential of Gallium Oxide channel for low-temperature processed *n*-channel oxide-TFT for next-generation electronic applications.

MANUSCRIPT

I. INTRODUCTION

Metal-oxide semiconductors consisted of post-transition metals such as In, Ga, Sn etc., are nowadays known as the mainstream of an *n*-channel material for thin-film transistor (TFT) application and are highly expected to develop next-generation sustainable energy-efficient device applications in the broad fields of electronics. Because of the excellent material properties such as high electron mobility over 10 $cm^2V^{-1}s^{-1}$ and the low-temperature processability less than 500 ºC, it also enables cost-effective "giant microelectronics" using a large-size glass substrate.[1–3] Therefore, *n*-channel oxide-TFT using amorphous In-Ga-Zn-O (a-IGZO) channel has been intensively investigated and already commercialized as a pixel TFT back-plane in several state-of-art displays such as high-resolution active-matrix flat panel display (AMFPD), large-sized liquid-crystal display (LCD) and high-resolution organic light-emitting display (OLED).[4–6] A wide variety of *n*-type metal-oxide semiconductor materials is so far proposed to improve the TFT device performances and explore new opportunity of device applications for next-generation electronics beyond display applications.[7, 8]

Wide-bandgap nature over 3.0 eV and high permittivity property originating from ionic chemical bonding mainly characterize oxide semiconductor channel materials. β-Gallium Oxide (β-Ga_2O_3) is a well-known *n*-type oxide with wide bandgap (E_g) of 4.5 − 4.9 eV, high dielectric constant (ε > 10), and high electron mobility (~300 $cm^2V^{-1}s^{-1}$ in single crystal), and is widely recognized as a promising material for oxide-semiconductor devices.[9, 10] The wide bandgap nature provides several benefits such as a high optical transparency through visible-ultraviolet region, a low intrinsic carrier concentration, and a high breakdown electric field of >6 $MV{\cdot}cm^{-1}$, which also enable to develop a variety of optoelectronics such as deep-ultraviolet sensor, power electronics devices, and novel applications.[9–15]

So far numerous efforts have been devoted for the development of Ga_2O_3-based transistors, which are mainly classified into two types of channel forms, i.e., bulk single-crystal and thin-film channel. The recent progress of single crystal (SC) β-Ga_2O_3-based field-effect transistor (FET) and TFTs are summarized in Table S1 and S2 (supplementary material). Several high-mobility SC-β-Ga_2O_3-FET (~191 $cm^2V^{-1}s^{-1}$ at the record value) have been demonstrated.[16–19] Because non-doped SC β-Ga_2O_3 channel shows semi-insulative behavior with high electrical resistivity of $>10^6$ Ω·cm, the electron doped β-Ga_2O_3 bulk channels using Si and Sn donors are used for the most

reported SC devices.[16] However, the precise control of electron doping level is not established yet and also the doping level is always high with >10^{18} cm^{-3} for β-Ga_2O_3 channels.[19, 20] Thus these devices operate in only depletion mode with a large negative threshold voltage (V_{th}), typically more than –30 V. Moreover, the SC-channels require high-temperature single crystal grown at 800 − 1400 °C and are fabricated by non-massive process such as mechanically exfoliation process.[17–19, 21, 22]

Although TFT device is in general highly preferable for massive production process, on the other hand, the development of Ga_2O_3-TFTs is largely behind from the SC devices, and the reports regarding β-Ga_2O_3-TFT are currently limited.[23, 24] (See Table S2 in supplementary material for the TFT device performances for previously reported Ga_2O_3-TFTs including epitaxial film, poly-crystalline film and amorphous film channels) Recently, Lv et al. achieved high mobility of ~90 $cm^2V^{-1}s^{-1}$ in the epitaxial β-Ga_2O_3-TFT fabricated by MOCVD at 750 °C.[25] Moreover, nanocrystalline β-Ga_2O_3 and amorphous GaO_x (a-GaO_x) channels are also developed by using several deposition methods such as spray pyrolysis[26], pulsed laser deposition (PLD)[27, 28], and sputtering[29]. However, it is still challenging to fabricate high-performance Ga_2O_3-TFTs at a low temperature less than 500 °C compatible with glass substrate.[30] To our best knowledge, typical TFT mobility of poly-crystalline Ga_2O_3-TFTs is still limited to 0.1−2 $cm^2V^{-1}s^{-1}$.[26–29, 31]

In this study, we developed high-performance amorphous-GaO_x-TFTs exhibiting good switching properties such as a large saturation mobility of ~31 $cm^2V^{-1}s^{-1}$, V_{th} of 3.28V, on/off current ratio of ~10^8 by using hydrogen subgap defect termination performing less than 500 °C. We investigated the electronic/defect structures of the GaO_x channel and explained why the development of Ga_2O_3-TFT was more challenging than another oxide-TFTs. In Gallium oxide, the subgap defects originating from low-valence Ga^+ state and excess oxygen rather than oxygen vacancy were significant for the TFT performances, and these defects caused the large degradation of the device performances. We also fabricated both depletion mode and enhancement mode a-GaO_x-TFTs for NMOS inverter application and demonstrated a-GaO_x-TFT-based-zero-V_{GS}-NMOS inverter exhibiting a full-swing inversion action and high voltage gain of ~200.

II. RESULTS AND DISCUSSION

Inverted-staggered structure, i.e., bottom gate and top-contact, TFT was fabricated using ~40 nm-thickness Gallium oxide channel (Fig. 1(a) for the schematic of the cross-sectional view for the TFT structure and the optical microscopic image of the channel region). Fig. 1(b) shows the variations of transfer characteristics, i.e., drain current (I_D) versus gate bias (V_{GS}) at drain-source voltage V_{DS} = 20V, for the as-deposited (i.e., unannealed)-TFTs prepared at different oxygen partial pressure (PO_2) during pulsed laser deposition (PLD) at room temperature (RT). The glancing-angle X-ray diffraction (GIXRD) measurement confirmed that no diffraction peak was observed for all the as-deposited films, revealing that these films were amorphous irrespective of the PO_2 conditions during the PLD depositions (Fig. S1 for the GIXRD patterns for the as-deposited films in supplementary material). All the amorphous-GaO_x (a-GaO_x) films exhibited semiconducting behavior, and *n*-channel field-effect transistor actions, i.e., the I_D current increased with applying positive V_{GS}, were confirmed. But the device performances are largely varied by the PO_2 deposition conditions, which suggests that the TFT characteristics are controlled by the channels that involve different defect structures originating from off-stoichiometry.

The variation of TFT characteristics by the PO_2 condition is not straightforward. The lowest PO_2 condition (i.e., PO_2 = 5mTorr) provides relatively good *n*-channel TFT device with the on/off-current ratio of $>10^5$ even in the RT device fabrication condition. When the PO_2 raises to ~10 mTorr, i.e., oxygen moderately-rich conditions, however, the film becomes highly conductive with the high electrical conductivity (σ) of ~7.1 $S \cdot cm^{-1}$ and thus the TFT device only shows very weak field-effect current modulation. On the other hand, the a-GaO_x channel turned out to be semiconducting state with the σ of ~1.2×10^{-5} $S \cdot cm^{-1}$ by furthermore increasing the PO_2 to 20 mTorr and decent *n*-channel TFT switching was confirmed again. However, the TFT characteristics for the 20 mTorr-device are not as good as the 5 mTorr-devices and quite poor with a small on/off-current ratio of ~10^3.

The important TFT device parameters, i.e., saturation mobility (μ_{sat}), V_{th}, on/off-current ratio, and subthreshold slope value (*s*-value) are summarized in Figs. 1(c)-(d). From the measured transfer curve, the V_{th} is determined from a straight line in a $(I_D)^{1/2}$ - V_{GS} plot to the V_{GS} axis. At V_{DS} = 20V, μ_{sat} is calculated by $I_D = 1/2 \cdot W \cdot \mu_{sat} \cdot C_{ox}/L \cdot (V_{GS} - V_{th})^2$, where *W* and *L* are channel width and length, respectively, C_{ox} is the gate insulator capacitance per unit area. The *s*-value is evaluated in the subthreshold region, with $s = (\partial \log I_D / \partial V_{GS})^{-1}$. The best TFT characteristics for the

as-deposited a-GaO_x channel were obtained when the channel was deposited at the PO_2 of 5 mTorr, and TFT performances were μ_{sat} of ~0.3 $cm^2V^{-1}s^{-1}$, V_{th} of −12.3 V, current on/off ratio of ~10^6, *s*-value of 1.0 $V{\cdot}dec^{-1}$, which were nearly comparable to the recently reported a-GaO_x-TFT performances.[28, 29]

The role of the deposition PO_2 condition of metal-oxide channels has been well investigated for several metal oxides such as a-IGZO, amorphous In-Zn-O (a-IZO), ZnO, In_2O_3 etc. It is well observed that most oxide channels simply transit from electrically conductive state to highly-resistive state by increasing the PO_2 condition and thus the corresponding V_{th} changes from negative to positive values.[32] The reason is mainly considered as the change of electron density (N_e) in the oxide channels by the formation/annihilation of oxygen vacancy (Vo) by the PO_2 conditions. However, the observed variations for the presented a-GaO_x-TFT are not simple and cannot be understood by the single effect of the N_e variation. Fig. 1(e) illustrates the variation of film conductivity as the PO_2 increasing, indicating non-linear relation between the film conductivity and the PO_2 condition during the RT-deposition. Thus we should consider the channel subgap defects, which also alter the Fermi level (E_F) position and vary the N_e and the conductivity in a-GaO_x channel, to explain the observed PO_2 dependency.

To obtain better insight for subgap density of state (DOS) for the a-GaO_x channels, Technology Computer-Aided Design (TCAD) device simulation was performed. Figs. 2(a) and 2(b) show the measured and simulated transfer curves for the as-deposited a-GaO_x-TFTs fabricated by PO_2 deposition at 5 and 20 mTorr, respectively. All the measured transfer curves were well reproduced by optimizing the subgap DOS profile, which was composed of acceptor-like exponential band-tail and Gaussian-distributed subgap defects. This indicates that TFT characteristics are mainly controlled by subgap defects. Especially, the defect density and the energy level of the Gaussian-distributed subgap defects have a large responsibility for the variations of the transfer characteristics for the a-GaO_x-TFTs.

The exponential tail-like DOS in the vicinity of the conduction band minimum (CBM) is expressed by $g_{CBa}(E) = g_{ta}\exp[(E - E_C)/W_{ta}]$, where E_C is conduction band edge energy, g_{ta} is acceptor-like states density at $E = E_C$, and W_{ta} is characteristic decay energy of conduction band-tail states. Meanwhile, the acceptor-like Gaussian states are assumed by $g_{Ga}(E) = g_{ga}\exp[-\left((E_{ga} - E)/W_{ga}\right)^2]$, where g_{ga} is the total acceptor-like Gaussian-

distributed DOS, E_{ga} is peak energy distribution measured from E_C, and W_{ga} is the characteristic decay energy. The subgap defect parameters for the device simulation are summarized in Table S3 (supplementary material).

Figures 2(c) and 2(d) show the corresponding subgap DOS profiles for the a-GaO_x channel extracted from the TFT device simulation analysis. When the channel is deposited at low PO_2 condition (i.e., 5 mTorr), TFT simulation analysis found that the film involves high N_e of > 10^{18} cm^{-3}. Moreover, the relatively deep acceptor-like defect was found at the energy level of E_V + 1.5 eV, where E_V is valence band edge energy, i.e., nearly near-valence band (VB) defect (Fig. 2(c)). To explain the observation, two carrier compensation mechanisms: 1) charge trapping mechanism, and 2) self-compensation mechanism, are considered. The observed deep acceptor-like states can capture free electrons, causing to lower the Fermi level due to carrier trap-induced charge compensation, shown as Fig. 2(e). Since the carrier density (N_e) relates to Fermi level (E_F) position, it follows the equation, $N_e = N_C \exp\left[-(E_C - E_F)/kT\right]$, where k is the Boltzmann constant, T is room temperature, N_C is the effective density of states at the conduction band edge E_C. Thus, the 5 mTorr a-GaO_x channel has the less N_e (~10^{18} cm^{-3}) by the presence of deep acceptor-like states and exhibits decent n-channel TFT action. On the other hand, the self-compensation mechanism is often used for metal oxide semiconductor to explain the variation of the electron density because most oxides have the electronic structure consisted of a shallow donor and a compensating deep acceptor levels, which is similar to the presented a-GaO_x channel.[33] In this model, the deep state is treated as acceptor with the density of N_A, while the near-CBM state is donor with density of N_D, shown as Fig. 2(f). When the Fermi level is above the acceptor level, the acceptor is negatively charged with N_A^-. On the other hand, the donor states are also nearly completely ionized and charged with N_D^+. Charge neutrality requires $N_D^+ = N_e + N_A^-$ for such n-type oxide semiconductor. From the charge neutrality condition, $N_D^+ = N_e + N_A^-$ for n-type semiconductor, the existence of the deep acceptor states compensates part of the charge and results in the lower electron density.

Soft X-ray photoelectron spectroscopy (XPS) measurements were performed for the as-deposited a-GaO_x films deposited at different PO_2 conditions, as shown in Figs. S2 and S3 in supplementary material. We observed the

extra subgap defect states above the VBM. The defect strongly depends on the deposition PO_2 condition, and the density increases when the a-GaO_x films are deposited at the low PO_2 conditions. The near-VB defect is often observed in metal-oxide semiconductors, but the exact origin is not clarified yet.[4, 28, 34, 35] Currently, Vo and low-valence metal cation state (i.e., Ga^+ in Gallium oxide) are considered as possible sources. The bulk-sensitive hard X-ray photoemission spectroscopy (HX-PES) study showed that the amount of Ga contents in a-IGZO channel significantly affected the near VB-defect structure and the VB-defect DOS increased by increasing the Ga content.[36] From the reported HX-PES observation and our experimental fact that near VB-defect is obvious for the low-PO_2 condition, we speculate that low-valence Ga^+ is strong candidate for the formation of the near-VB-defects.

Significant reduction of the N_e down to ~5×10^{17} cm^{-3} and the appearance of shallow acceptor-like states near E_C – 0.2 eV (i.e., near CB-defect) were observed in the highest PO_2-deposited channel (Fig. 2(d)). This observation allows us to speculate that oxygen-rich deposition condition eliminates oxygen deficient-related defects such as Vo and low-valence metal but is likely to form extra subgap defect, such as weakly-bonded (excess) oxygen defect, which is also often observed in amorphous metal oxide and works as acceptor-like traps.[28, 37] Therefore, the 20 mTorr-deposited a-GaO_x channel satisfies the TFT operation conditions but exhibits poor performances with a very large *s*-value and a large hysteresis with the hysteresis window of >25 V.

We next examined the effect of post-thermal hydrogen annealing for the a-GaO_x channel to improve the TFT device characteristics. Fig. 3(a) shows the variation of transfer curves for the devices where the channels were annealed at 450 ºC in hydrogen atmosphere.[31] The GIXRD measurement confirmed that the 450 ºC-annealed films maintained amorphous phase (Fig. S4 for the GIXRD analysis in supplementary material). We confirmed that β-Ga_2O_3 was formed after 550 ºC-post-annealing. The observation is consistent with previous reports that high temperature annealing above 500 °C is required for the crystallization of Ga_2O_3.[28, 30, 31]

The variations of fundamental device parameters by hydrogen annealing are summarized in Figs. 3(b)-(e), compared with the corresponding as-deposited devices. The 5mTorr-TFT showed the improvement of TFT mobility, but no apparent improvement of *s*-value and the on/off current ratio were observed. Large positive shift of V_{th} was observed in the 20mTorr-devices. Significant improvement was observed only in the channel deposited

at PO_2 = 10 mTorr, suggesting that the as-deposited 10mTorr-film has better stoichiometry, i.e., less subgap defect originating from oxygen-related off-stoichiometry. Therefore, the a-GaO_x film deposition condition is still important to obtain high performance TFT fabricated with post-thermal annealing process. The H concentration was measured by Secondary Ion Mass Spectrometry (SIMS) and was found to be ~ 2×10^{19} cm^{-3} for the 450 ºC-H_2 annealed-a-GaO_x film (See Fig. S5 for the Hydrogen SIMS depth profile in supplementary material).

Figure 4(a) also shows the variation of transfer characteristics of the a-GaO_x-TFTs annealed in different annealing atmospheres such as hydrogen, vacuum, oxygen, and ambient air. All the channel was deposited at 10 mTorr and then annealed at 450 ºC for 1 hour. The TFTs performances are also summarized in Table I. The trap state density (D_{it}) can be estimated from the s-value with the following relation: $s = \ln10 \cdot k_BT/q \cdot [1+eD_{it}/C_{ox}]$, where k_B is Boltzmann constant, T is the temperature, and e is the elementary charge. We observed that the TFT characteristics were largely affected by the annealing atmospheres. The vacuum annealing and hydrogen annealing produce TFT devices with good switching property such as large on/off-current ratio (I_{on}/I_{off}) over 10^8. The μ_{sat} values are ~27 $cm^2V^{-1}s^{-1}$, and ~31 $cm^2V^{-1}s^{-1}$ for the vacuum-annealed and hydrogen-annealed TFTs, respectively. It is well known that the mobility is sometimes overestimated due to fringe effect of channel region and the channel length contributed by the peripheral channels. Therefore, it is important to show the accuracy of the mobility and the accuracy is estimated as ~89% for the presented TFTs. The s-values are ~2.5 V·dec^{-1} and ~1.0 V·dec^{-1}, which correspond to the D_{it} values of ~5.9×10^{12} $cm^{-2}eV^{-1}$, and ~2.3×10^{12} $cm^{-2}eV^{-1}$, respectively. The V_{th} are −30 V and +3.3 V for the vacuum and hydrogen-annealed TFTs, indicating that these devices are operated in depletion (D) mode (normally-on) and enhancement (E) mode (normally-off) modes, respectively. This is understood by the difference of the N_e in the a-GaO_x channels, which are estimated be ~2×10^{18} cm^{-3} and ~1×10^{17} cm^{-3} for the vacuum- and hydrogen-annealed channels, respectively. Studies regarding native point-defect analysis for crystalline β-Ga_2O_3 have been done by using density functional theory (DFT) material simulations. These studies predict that the Vo defect[38, 39], impurity hydrogen[40, 41], Gallium interstitials (Ga_i)[42] are considered as the possible sources of electron for Ga_2O_3. Several experimental studies also supported the DFT predictions for the carrier generation, but it is still controversial.[43–45] Our experimental observations showed that vacuum-annealing produces one order higher N_e than hydrogen-annealing, and Vo and Ga_i defects are more obvious than hydrogen impurity for electron

carrier generation. Currently, the exact kind of defect that is terminated by hydrogen annealing is still unclear. Because the defect should be electron trap state, oxygen vacancy is still considered as a strong candidate for the defect. It was reported that hydrogen could be easily incorporated and possibly substitute with oxygen vacancy site for amorphous metal oxide.[46] Another plausible defect relates to a free space in amorphous structure, which causes the formation of shallow unoccupied state below the CBM for oxide-TFT.[47] Since the film density of the presented a-GaO_x film is only ~ 5.2 g/cm^3, the amorphous structure is speculated to have a large volume of free space with high density vacancy defects and bond angle distortions, which work as electron trap. Therefore, such free space facilitates fast migration/diffusion of Hydrogen, and Hydrogen helps to terminate electron trap defect sites.

Both the D and E-mode TFT devices showed clockwise-hysteresis, indicating the presence of electron trap. The hysteresis windows for the hydrogen-annealed are ~1.8 V and ~1.5 V at V_{DS} = 1 V and 20 V, respectively, which are well suppressed as compared with that in the vacuum-annealed TFTs (~8 V) (See Fig. S6 for the hysteresis characteristics in supplementary material).

On the other hand, oxygen-containing annealing atmospheres such as dry-O_2 and ambient air showed apparent degradation of the device characteristics from the as-deposited device. These annealed devices showed very low mobility of < 5×10^{-3} cm^{2}V^{-1}s^{-1} and a small on/off-current ratio of <10^4, which are the similar device performances as the previously reported Ga_2O_3-TFT devices[27, 31], and similar as the as-deposited device fabricated at high PO_2 conditions in this study. In general, oxygen-containing annealing is believed to improve the device characteristics for several *n*-channel metal oxide-TFTs such as IGZO, ZnO and In_2O_3. This is based on the assumption that Vo defect forms electron-trap states and oxygen-containing annealing compensate Vo-defects.[1, 48, 49] However, we clearly observed opposite effects of oxygen-containing annealing for the presented a-GaO_x-TFTs. Since the device performances for the air and oxygen-annealed-TFTs are very similar with the high PO_2-deposited TFT device, we speculate that excess oxygen defects that work as acceptor-like defect are introduced by oxygen-containing annealing.

We also analyzed the subgap DOS by microwave-photoconductivity decay (μ-PCD) measurement and found that the subgap DOS profile was significantly altered by the deposition PO_2 and post-thermal annealing conditions. For the unannealed films, it was observed that the 10 mTorr and 20 mTorr a-GaO_x films involved relatively high

subgap DOS of > 10^{18} $cm^{-3}eV^{-1}$, while the subgap DOS for the 5 mTorr film was well suppressed to ~10^{17} $cm^{-3}eV^{-1}$. This observation is consistent with the TCAD simulation analysis, which explains the reason why the 5mTorr-channel TFT shows decent reasonable TFT performances. Moreover, we observed hydrogen annealing significantly reduced the subgap DOS down to ~10^{16} $cm^{-3}eV^{-1}$. It is also confirmed that vacuum annealed film has a relative low amount of shallow subgap DOS of ~10^{17} $cm^{-3}eV^{-1}$. The air-annealed film involved high-density shallow states with DOS of > 10^{18} $cm^{-3}eV^{-1}$. (See Figs. S7-S10, Table S4 and S5 for μ-PCD analysis and extracted subgap DOS profiles in supplementary material) These observations support our claim that oxygen-containing annealing generates extra subgap DOS and does not improve TFT performances for the a-GaO_x-TFTs. On the contrary, hydrogen annealing produces good n-channel oxide-TFT originating from the reduction of subgap defect.

We measured the bandgap (E_g) for the presented a-GaO_x films and confirmed a-GaO_x films maintained wide bandgap nature (Fig. S11 for the bandgap and urbach energy for the presented a-GaO_x films in supplementary material). The E_g values of the as-deposited a-GaO_x films are varied by the PO_2 conditions and are from ~3.5 to 4.1 eV by increasing the PO_2 condition. Post-annealing also increases the E_g values, which were ~3.8 eV and ~4.0 eV for vacuum-annealed film, and the hydrogen-annealed film, respectively. The observed E_g is smaller than crystalline β-Ga_2O_3 but in good agreement with the previously reported amorphous Gallium oxide.[28, 31] The variation of E_g can be mainly understood by the change of the film density (Fig. S12 for the film density analysis in supplementary material). The film density of the a-GaO_x films has the tendency to be increased by high PO_2 condition and post-thermal annealing. The film density was determined as ~5.2 – 5.4 $g \cdot cm^{-3}$ that is ~12 % lower than that of β-Ga_2O_3 (density ~5.95 $g \cdot cm^{-3}$).

Figures 4(b) and 4(c) show high-voltage output characteristics for the depletion (D-) mode vacuum-annealed and enhancement (E-) mode hydrogen-annealed-TFTs, respectively. The linear output characteristics confirmed the ohmic behavior, indicating that ITO contact made good ohmic contact for both operation modes. We confirm that both devices maintain stable operation under high V_{DS} DC voltage sweeping up to 100 V, the maximum current density is ~1.4 $mA \cdot mm^{-1}$ for the presented D-mode TFT, and ~2.3 $mA \cdot mm^{-1}$ for the presented E-mode TFT, which are comparable to the previously reported E-mode epitaxial β-Ga_2O_3 MOSFET.[24, 50]

The D-mode-TFT exhibits larger linear region than the E-mode device and insufficient pinch-off characteristics. This is due to the effective channel length modulation by high-density accumulated carrier formation near drain region at high V_{DS}. The band diagrams for the D-mode TFT operations are depicted as Figs. 4(d)-(e). For the low drain-source electric field at low V_{DS} condition (< 25 V), band bending structure is not altered (Fig 4(d)). In contrast, at high V_{DS} condition (> 40 V), the band bending is largely impacted by large positive drain-source electric field and larger downward bending is formed near drain electrode region. In this case, the E_F level is close to the CBM and the accumulated electrons are significantly increased near drain region, and the channel length modulation effect becomes remarkable (Fig 4(e)). The drain-current is modified by the channel modulation factor (λ), and is expressed by $I_D = ½ \cdot W \cdot \mu_{sat} \cdot C_{ox}/L \cdot (V_{GS} - V_{th})^2 \cdot [1 + \lambda(V_{DS} - V_{Dsat})]$, where V_{Dsat} is the value of $V_{GS} - V_{th}$. In the presented D-mode TFT, λ value is ~0.01 V^{-1}. The effective channel length (L') becomes shorter compared with the total channel length (L) of 150 µm, following the relation $(L - L')/L = \lambda(V_{DS} - V_{Dsat})$, and L' is estimated as ~50 µm at V_{DS} = 100 V. Therefore, the insufficient pinch-off is observed from the D-mode output characteristics.

On the other hand, the E-mode device exhibits ideal output characteristics with a good pinch-off and current saturation characteristics, which originates from the low N_e condition in the E-mode channel with ~10^{17} cm^{-3}. Generally, a low N_e material system exhibits several advantages such as a less self-heating effect due to low thermal conductivity properties.[51] As compared with the previously reported SC-based β-Ga_2O_3-FETs, the presented TFT exhibits comparable device mobility of ~31 $cm^2V^{-1}s^{-1}$ and a lower operation voltage (V_{th} ~ 0V).

To furthermore understand the TFT operation mode of the D and E-modes a-GaO_x-TFTs, the electrical characteristics were analyzed by TCAD-TFT device simulation. Figs. 5(a)-(b) show the measured and simulated transfer curves for the above D- and E- mode a-GaO_x-TFTs, respectively. For the comparison, the device with a large positive V_{th}, which was fabricated by 450 ºC-hydrogen-annealed a-GaO_x channel deposited at high PO_2 condition (PO_2 = 20 mTorr), is also included as Fig. 5(c). All the measured transfer curves were well simulated by optimizing the subgap DOS profile in a-GaO_x channel. The simulation parameters are also summarized in Table S6 (supplementary material).

Figures 5(d)-(f) show the extracted subgap DOS profile for the corresponding a-GaO_x-TFTs. For the D-mode TFT, high-density midgap-defects with ~1.2×10^{18} $cm^{-3}eV^{-1}$ located at E_C – 1.2 eV was observed (Fig. 5(d)). When

the CB energy is upward bending by large negative V_{GS}, carrier is depleted and TFT is turned off in the D-mode-TFTs. The surface potential (ψ_S) is defined as the potential difference between front channel and the bulk, and the sign of ψ_S is defined as negative for upward band bending. At $\psi_S = -1.7$ V when $V_{GS} = -40$ V, the channel depletion width (W_d), defined by $W_d = \sqrt{2\varepsilon |\psi_S| / qN_e}$, is ~40 nm, which is comparable to the channel thickness and suggests that the device meets the fully-depleted condition. Fig. 5(g) (bottom) shows the corresponding band diagram with bulk VB energy ($E_{V(bulk)}$) as reference, and the electron density map for the D-mode-TFT at $V_{GS} = -40$ V, confirming that carriers are fully-depleted and total upward band bending is 1.7 eV. Fig. 5(g) (top) is the band diagram and electron density map for the D-mode-TFT at $V_{GS} = 20$ V, showing a weak carrier accumulation with the ψ_S of ~0.04 V. The E_F is located around ~0.05 eV below the CBM for the on-state, while for the off-state the E_F is at $E_C - 0.25$ eV in bulk and is at $E_C - 1.95$ eV near front channel. This indicates that the device requires a large Fermi level sweeping and shift (~1.9 eV) by the gate bias between turn-off and turn-on. Due to the relatively high-density midgap defect screened by Fermi level during energy band from upward to downward bending, the D-mode-TFT showed a large subthreshold slope property.

In contrast, the extracted E-mode device DOS confirms negligible midgap defect and the device operation is mainly controlled by shallow acceptor-like defect located at $E_C - 0.3$ eV (Fig. 5(e)). The observation also indicates that hydrogen annealing significantly suppresses the formation of midgap defect.[47] For the accumulation operation mechanism, the E_F is at $E_C - 0.35$ eV with $\psi_S = -0.12$ V at negative bias of $V_{GS} = -3$ V and no carrier is accumulated (Fig. 5(h) (bottom)). While for the turn-on condition at positive V_{GS}, the E_F is shifted up to $E_C - 0.17$ eV, indicating that carriers are accumulated near the front channel region (Fig. 5(h) (top)).

On the other hand, the TFT simulation analysis for the large positive-V_{th}-TFT revealed that the channel involved high-density shallow trap of ~8.5×10^{17} $cm^{-3}eV^{-1}$ near $E_C - 0.6$ eV (Fig. 5(f)). The high-density acceptor-like defect generates negatively-charged defects by electron trapping and causes the large positive shift of V_{th} due to the gate bias screening effect. Moreover, the on-current is largely degraded. Indeed, the most previously reported Ga_2O_3-TFTs show very similar performances as such device, i.e., large V_{th} and low on-current, [26, 52] which can be

understood by high-density acceptor-like defect in the Ga_2O_3-channels produced by oxygen-rich conditions. It concludes that the development of high performance Ga_2O_3-TFT requires the optimal PO_2 condition during film deposition and post-thermal annealing atmosphere.

Figure 6 summarizes the electronic/defect structures for the presented a-GaO_x channels deduced by the presented material characterizations and TFT simulations. Fig. 6(a) depicts the DOS profile for the as-deposited channels. All the as-deposited amorphous channel involves high N_e of ~10^{18} - 10^{19} cm^{-3}, which is consistent with the previous discussion about total donor density (N_0) of ~8×10^{19} cm^{-3} for the RT-PLD-deposited a-GaO_x channel.[28] Since the donor level (E_D) forms near the CBM, the N_e is expressed by $N_e = N_0 \exp(-(E_C - E_D)/k_BT)$. However, the observed N_e strongly depends on the subgap defect profiles that are varied by the PO_2 deposition conditions. The observations indicate that the E_D is ~0.1 eV below the CBM for the low PO_2-film. Instead, highly conductive film can be obtained at optimal PO_2 when the deep-level states near-VB are no longer formed, and the corresponding donor level is ~0.05 eV below the CBM. Furthermore, the conductivity drops sharply by further increasing PO_2 due to high-density near-CB electron traps and thus the E_D is shifted to ~0.15 eV below CBM for the high PO_2-film. On the other hand, post-thermal annealing also alters the N_e into range of 10^{17} to 10^{18} cm^{-3}, and the annealing atmospheres largely modify the subgap defect profiles, as shown in Fig. 6(b). Our observations showed that hydrogen annealing significantly reduced the subgap defects, which is also consistent with the previous report.[47] We also observed that vacuum annealing created midgap states and higher N_e of the a-GaO_x channel to fabricate the D-mode TFT. On the other hand, oxygen-containing annealing generated extra high density shallow subgap defect. Similar high density shallow subgap defect was observed in a-GaO_x channels prepared oxygen rich process conditions such as high PO_2 deposition conditions and oxygen-containing annealing and has a large responsibility for the poor TFT performances such as low mobility and very large-positive V_{th} (Fig. 6(c)). The discussion also clarifies a reason for the poor performance of the previously reported polycrystalline Ga_2O_3-TFTs [26, 28]. We also performed positive and negative bias stress (PBS and NBS) tests, negative and positive bias illumination stress (NBIS and PBIS) tests for the high mobility a-GaO_x TFTs (Figs. S13-16 in the supplementary material). Both NBS and PBS showed bias stress-induced V_{th} instability and the enhanced V_{th} instability was observed by the light-illuminated bias stress. These observations indicate the presence of high-density subgap defects and developing

effective defect termination is strongly required to improve the bias-stability for the a-GaO_x-TFTs. Since the long-term TFT bias stability is important for practical applications, we preliminary examined a back-channel passivation for a-GaO_x-TFT and confirmed that the V_{th} stability in both the PBS/NBS was improved (Figs. S17-18 in the supplementary material). The long-term positive/negative bias illumination stress (PBIS/NBIS) for the passivated devices were also assessed (See Figs. S19-20 in the supplementary material). To further improve the bias stability, the a-GaO_x TFTs with 30nm-Al_2O_3 gate dielectric were developed, exhibiting μ_{sat} of 23.3 cm^2/Vs, V_{th} of 0.67 V, and *s*-value of 0.14 V/dec, and confirmed the improvement of both long-term PBS/NBS and PBIS/NBIS stability (Figs. S21-24 in the supplementary material).

Finally, we fabricated a zero-V_{GS}-NMOS inverter composed of the D- and E-mode a-GaO_x-TFT as load- and drive-TFTs, respectively. Fig. 7(a) shows the corresponding transfer characteristics of the load/drive a-GaO_x-TFTs. In order to achieve a full-swing inverter property in the voltage transfer characteristics (VTC), i.e., output voltage (V_{out}) vs. input voltage (V_{in}), the I_{on} of the drive-TFT should be higher than that of the load device. Thus, we adjusted the I_{on} level on the load-TFTs. The load-device was fabricated by 450 ºC-vacuum-annealing and exhibited V_{th} of −27 V at V_{DS} = 20 V, *s*-value of 1.3 V·dec^{-1}. For the drive-TFTs, the E-mode TFT with the V_{th} of 6.6 V at V_{DS} = 20 V, *s*-value of 0.83 V·dec^{-1} was used. Fig. 7(b) represents the VTC and the corresponding voltage gain, defined as $-dV_{out}/dV_{in}$, for the zero-V_{GS}-load inverter and V_{DD} is varied from 20 to 60 V. The inset shows the equivalent circuit diagram. The gate and source terminals in the load-TFT are connected, so the load-TFT is always on the "ON" state. At low input voltage (V_{in}), drive-TFT is on the "OFF" state and the output voltage (V_{out}) is equal to the supplied voltage (V_{DD}). At high V_{in}, drive-TFT is on the "ON" state, so the output voltage potential is pulled down to the ground and V_{out} becomes 0 V. A full-swing operation with rail-to-rail output was observed in all V_{DD} conditions, indicating that the inverter operated in proper NMOS schemes. The voltage gain was ~200, which is nearly comparable as the previously reported oxide-TFT-based zero-V_{GS}-NMOS inverters.[53, 54] The observed switching threshold voltage V_{inv} was 22.2V, which was nearly ½V_{DD} at V_{DD} = 40 V (Fig. 7(c)). The noise margin is estimated as ~17 V and good noise immunity over 85% is achieved in the present zero-V_{GS}-NMOS inverters. The obtained noise immunity is sufficient for the operation of radio-frequency identification tags and oxide-based logic gates. Note that at this point the D-mode and E-mode TFTs are fabricated in different process of vacuum and hydrogen

annealing, respectively, demanding further effort to integrate in the same chip or circuit. The presented device still requires high voltage operations due to a large subthreshold swing characteristics. The use of high-k gate dielectric will improve low power operation. Fig. 7(d) shows the static current (I_{DD}), and the static power dissipation (P_{stat}) which is defined as $I_{DD} \cdot V_{DD}$. At V_{DD} = 40 V, the I_{DD} was ~3 pA and the corresponding P_{stat} was as low as 120 pW before the inversion. During inversion, the I_{DD} was ~350 nA. Right after inversion, the NMOS inverter reached full swing, where I_{DD} was ~570 nA and P_{stat} was ~23 μW. Thus, such NMOS inverters exhibit negligible power consumption before inversion, decent gain, sufficient noise margin, and low static current to achieve full swing under high voltage operation. These good inverter characteristics were attributed to the proper switching property of both the D- and E-mode a-GaO_x-TFTs.

III. CONCLUSION

We developed a wide bandgap amorphous GaO_x-TFT where the channel was fabricated by post-hydrogen thermal annealing at 450 °C, exhibiting good TFT switching characteristics such as high saturation mobility of ~31 $cm^2V^{-1}s^{-1}$, V_{th} of 3.28V, current on/off ratio of ~10^8, *s*-value of 1.17 $V \cdot dec^{-1}$, and hysteresis widths of ~1.5 V. The oxygen condition during the channel fabrication process (i.e., PO_2 deposition condition and post-annealing atmosphere) was significant for the TFT device performances of the a-GaO_x-TFTs, because off-stoichiometric defects such as low-valence Ga^+ and excess oxygen formed high-density deep near-VB and shallow near-CB subgap defects, respectively. We concluded that these defects hindered the development of high-performance Gallium oxide thin-film electronic devices. We developed hydrogen annealing to effectively reduce the channel subgap defects. Both D-mode and E-mode TFTs were fabricated for oxide-TFT-based NMOS inverter, and the TFT characteristics and the operation mechanisms were analyzed by using TFT device simulation. Finally, the a-GaO_x-TFT-based zero-V_{GS}-load inverter, composed of D-mode load TFT and E-mode drive TFT, was demonstrated with full-swing VTC, gain of ~200, and noise immunity over 85%. The presented work demonstrated the high potential of Gallium oxide-TFT and NMOS circuit applications, offered the prospects to combine with high-k dielectric technologies for further development, and promised new opportunities in next-generation sustainable cost-effective oxide-TFT technology.

IV. EXPERIMENTAL SECTIONS

A. Film growth and material characterization of amorphous GaO_x film

The a-GaO_x films were deposited by pulsed laser deposition (PLD, KrF excimer laser, wavelength of 248 nm, pulsed duration 20 nsec) at RT. The base vacuum pressure of the PLD chamber was $<1.8\times10^{-8}$ Torr. The commercial sintered body of Ga_2O_3 (purity: 99.99%) was used as a target. The laser power density was set to ~6 $J\cdot cm^{-2}$ at the target surface that yielded a film growth rate of ~10 $nm\cdot min^{-1}$. Oxygen partial pressure (PO_2) during the deposition was varied from 5 to 20 mTorr. The films were subjected to thermal-annealing at 450 ºC for 1 hour in H_2 forming gas (5%-H_2 in N_2), vacuum (~10^{-5} Torr), and dry O_2 atmosphere using rapid thermal annealing (RTA) system, and in air using hot plate. For the material characterization, the films were deposited on quartz substrates. The film structure was characterized by grazing incidence X-ray diffraction (GIXRD) with an incident angle of 0.5°. UV-visible spectrophotometer was used to measure the optical transmittance, reflectance spectra and analyze the optical bandgap of the film. The photoconductivity decay curve was measured by microwave-photoconductivity decay (μ-PCD) with yttrium lithium fluoride (YLF) pulsed laser (λ = 349 nm) at RT. X-ray reflectivity measurement was performed to determine the film density. X-ray photoemission spectroscopy (XPS) measurements were carried out with Al Kα (hν = 1486.6 eV). No surface treatment was performed for the XPS measurement, and the C 1s core level from the adsorbed carbon was used for binding energy correction. The depth profile of Hydrogen in the annealed films was measured by Secondary-Ion Mass Spectroscopy (SIMS).

B. Device fabrication and characterization

Top-contact and bottom-gate a-GaO_x-TFT was fabricated on thermally-oxidized SiO_2 (the thickness of 150 nm)/n^+-Si substrates where the n^+ Si substrate acted as the common gate electrode. The RT-PLD deposited 40-nm-thick a-GaO_x films were used for a channel layer. The channel and electrode were patterned by shadow mask and the channel width (W) and length (L) were 300 and 150 μm, respectively. The channels are subject to post-thermal annealing in hydrogen, vacuum, dry O_2, and air atmospheres at 450 ºC for one hour. After the post-thermal annealing, RT-deposited PLD-ITO film (the thickness of 50 nm) was used for source/drain contacts. All electrical DC measurements were performed in the dark ambient environment at RT.

C. TCAD TFT device simulation

TCAD device simulator was used in this study to extract subgap defect DOS profiles of the a-GaO_x channel. The simulation was conducted by using Silvaco's 2D ATLAS simulator package. Inverted-staggered TFT configuration was employed in the simulator. For the IV characteristics simulation, the following material parameters were used: the relative permittivity values of the silicon oxide as the gate insulator and Ga_2O_3 as the channel semiconductor were 3.9 and 10, respectively. The electron affinity of Ga_2O_3 was 4.0 eV and the bandgap (E_g) was determined by measured value. The measured saturation mobility was used for the electron mobility values for the channel. The effective densities of states in the conduction and valence bands were 3.7×10^{18} cm^{-3}.

SUPPLEMENTARY MATERIAL

See the supplementary material for the summary of reported single-crystal Ga_2O_3 FETs, reported epitaxial, polycrystalline, and amorphous Ga_2O_3-TFTs, GIXRD measurements for the a-GaO_x films under different conditions, XPS measurements for the a-GaO_x films deposited by different PO_2, a-GaO_x TFT simulation parameters, Hydrogen SIMS depth profile, a-GaO_x TFT hysteresis characteristics, a-GaO_x thin-film microwave photoconductivity decay measurement, analysis, and extracted subgap DOS, a-GaO_x thin-film bandgap and urbach energy analysis, a-GaO_x film density under different conditions, the positive/negative bias stress and negative/positive bias illumination stress tests for the high mobility a-GaO_x TFTs, PBS/NBS and PBIS/NBIS for a-GaO_x TFTs with back-channel passivation, PBS/NBS and PBIS/NBIS for a-GaO_x TFTs with 30nm-Al_2O_3 gate dielectric, and optical microscope image of the a-GaO_x TFT.

DATA AVAILABLITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

ACKNOWLEDGEMENTS

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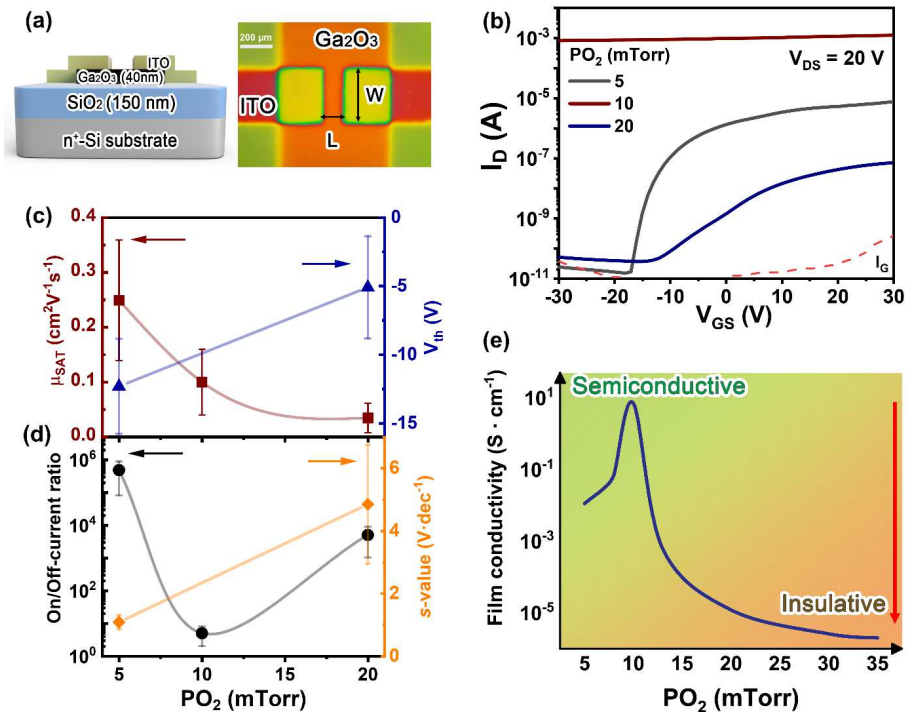

FIG. 1. (a) Schematic of the device structure of a-GaO_x-TFT and the optical microscope image of the channel region (scale bar: 200 μm). (b) Variation of transfer characteristics at V_{DS} = 20 V for the a-GaO_x-TFTs using the unannealed film deposited by different deposition PO_2 at 5, 10, and 20 mTorr at RT. The extracted fundamental TFT parameters (c) μ_{sat} and V_{th}, (d) on/off-current ratio and *s*-value were plotted as a function of the deposition PO_2. (e) The variation of as-deposited film conductivity as the function of PO_2 during a-GaO_x channel deposition.

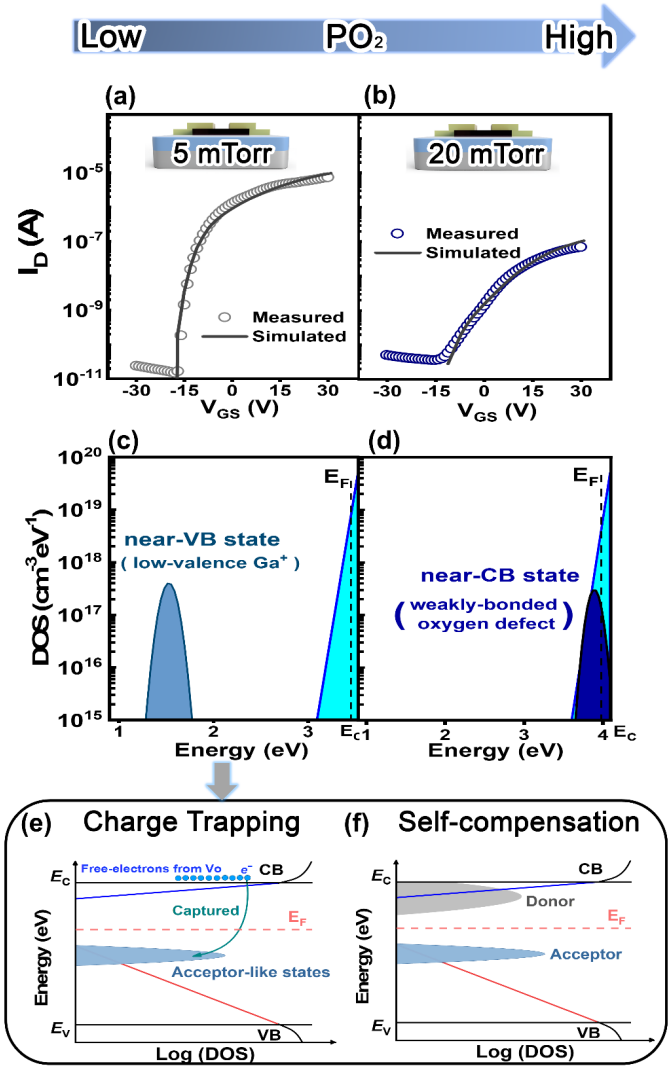

FIG. 2. The measured (symbols) and simulated (solid) transfer curves at V_{DS} = 20 V for the as-deposited a-GaO_x-TFT fabricated by PO_2 deposition at (a) 5 and (b) 20 mTorr. (c-d) The corresponding subgap defect DOS profiles. The proposed (e) charge trapping and (f) self-compensation mechanisms of carrier compensation for the 5 mTorr-a-GaO_x channel device.

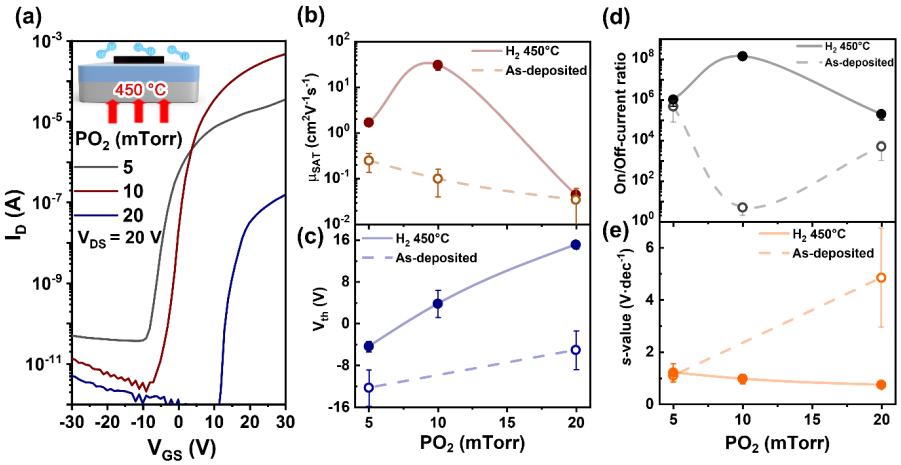

FIG. 3. (a) Variation of transfer characteristics at V_{DS} = 20 V for the 450 ºC-hydrogen-annealed device with the a-GaO_x-channel deposited at different PO_2 conditions. The variation of fundamental TFT parameters (b) μ_{sat}, (c) V_{th}, (d) on/off-current ratio, and (e) *s*-value by hydrogen annealing, compared with as-deposited films.

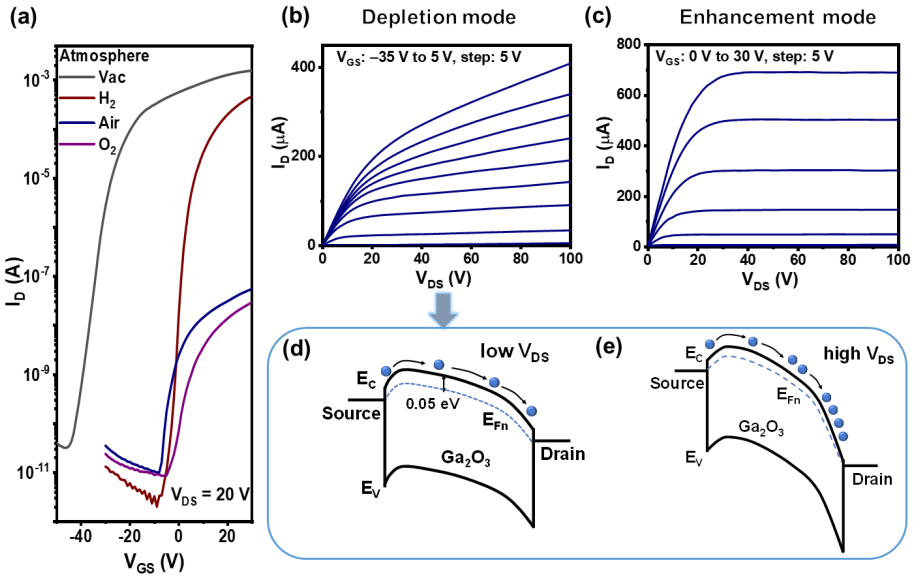

FIG. 4. (a) Variation of the transfer characteristics for the a-GaO_x TFTs at V_{DS} = 20 V by post-annealing with different atmospheres (vacuum, H_2, dry O_2, and ambient air) at 450 ºC. The output characteristics for (b) D-mode device and (c) E-mode device, fabricated by vacuum and hydrogen annealing, respectively. The schematics of band diagram corresponding to D-mode at (d) low and (e) high positive V_{DS}.

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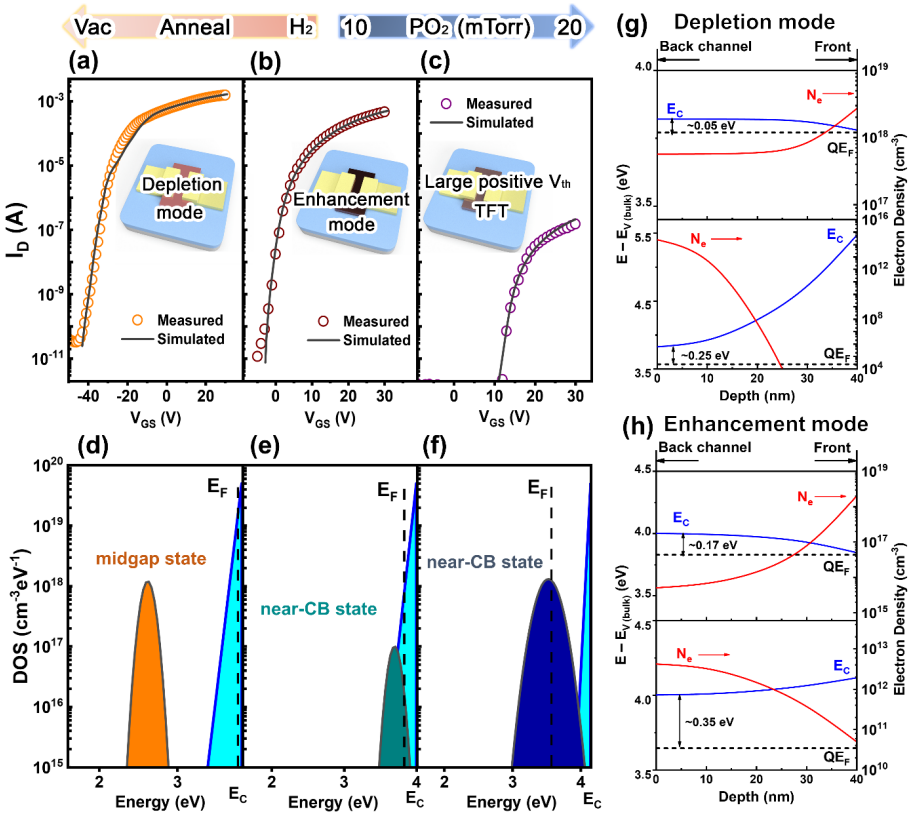

FIG. 5. Measured (symbols) and simulated (lines) transfer curves at V_{DS} = 20 V for (a) depletion-mode (b) enhancement-mode, and (c) large positive V_{th} TFTs. (d-f) The corresponding extracted DOS distributions near CBM. Conduction band energy diagrams with the corresponding the quasi-Fermi level (QE_F) and the quasi-electron density (N_e) for (g) D-mode at V_{GS} = –40 V (bottom) and +20 V (top), and for (h) E-mode at V_{GS} = –3 V (bottom) and +20 V (top). The blue and red lines are the conduction band energy (E_C) and N_e, respectively. The black dashed line denotes the QE_F.

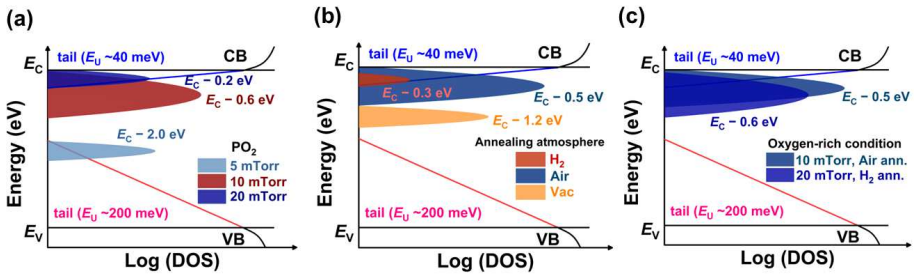

FIG. 6. Electronic and subgap defect DOS structures of a-GaO_x channels for (a) unannealed films under different deposition PO_2 at 5, 10, and 20 mTorr at RT, (b) the 10mTorr-PO_2 films annealed in different atmospheres of hydrogen, vacuum and air, and (c) the films deposited (PO_2 of 20mTorr) or annealed (air annealing) in oxygen-rich conditions.

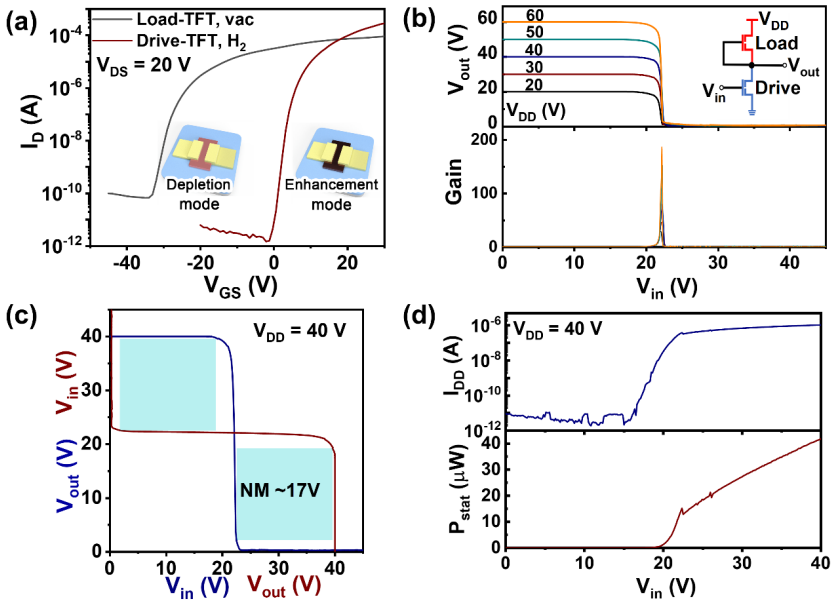

FIG. 7. (a) The transfer characteristics for load-TFT and drive-TFT of the zero-V_{GS}-load inverter. (b) The voltage transfer characteristics (top) with the corresponding voltage gains (bottom) at different V_{DD} values for the a-GaO_x-TFT-based inverter. Inset shows the schematic circuit diagram of the zero-V_{GS}-load NMOS inverter composed of load/drive TFTs. (c) Noise margin at V_{DD} = 40 V of the corresponding inverter. (d) The corresponding static current in log scale (I_{DD}, top) and static power dissipation (P_{stat}, bottom).

TABLES

TABLE I. The summary of TFT performances for the a-GaO_x-TFTs annealed in different annealing atmospheres at 450 ºC for one hour.

Annealing atmosphere	V_{th} (V)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	I_{on}/I_{off}	s-value ($V{\cdot}dec^{-1}$)	D_{it} ($\times10^{12}$ $cm^{-2}eV^{-1}$)
Vacuum	−38±11	27±17	~10^8	2.5±0.9	5.88±2
H_2	3.3±3	31±7	~10^8	1±0.18	2.27±0.3
Air	−6.2±5	2.7×10^{-3}	~5×10^3	1.94±0.2	4.53±0.3
O_2	−0.07±2.5	1.5×10^{-3}	~3.4×10^3	3.35±0.15	7.93±0.2

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