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Design and Implementation of Digital Baseband Receiver for 60 GHz Wireless Communication

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Yen-Cheng Kuan

2014

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ABSTRACT OF THE DISSERTATION

Design and Implementation of Digital Baseband Receiver for 60 GHz Wireless Communication

by

Yen-Cheng Kuan

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2014

Professor Mau-Chung Frank Chang, Chair

To support the increasing demand of various high data-rate wireless communications, the 7 GHz band at 57–64 GHz has been allocated by the FCC for unlicensed system applications. This decision results in the formations of several standards aiming to develop multi-gigabit wireless communication systems, e.g., IEEE 802.15.3c, IEEE 802.11ad, WiGig, among many others. One of their common and ultimate goals is to expedite the realization of widespread integrated circuits supporting large data transfers over the air.

Designing a digital baseband receiver for the 60 GHz communication system (802.15.3c) requires the following features: (1) a proper architecture to mitigate design challenges of the high-speed analog-to-digital converters (ADCs) that are required by the

synchronizer of the receiver; and (2) an effective technique to decouple the interferences that result from adjacent channel estimation sequences (CESs) as well as degrade the equalizer performance of the receiver.

To fulfill these requirements, this work realizes the following: (1) a fractional-sampling-rate (FSR) digital baseband receiver to relax the ADC sampling rate requirement through multi-rate signal processing techniques; and (2) a high-accuracy channel estimator to reconstruct interference-less CES responses for improving the BER performance of the equalizer. Compared with the prior arts, the 65 nm CMOS implementations of (1) and (2) demonstrate the feasibilities of reducing the required ADC sampling rate by 25%, and assisting the equalizer in achieving 170x BER reduction, respectively.

The dissertation of Yen-Cheng Kuan is approved.

Kung Yao

Wentai Liu

Mau-Chung Frank Chang, Committee Chair

University of California, Los Angeles

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Last but not the least, I would like to thank my parents, my sister, my brother in law, and Shu-Shiuan. It is their love, support, and patience that brought me to this stage.

Biographical Sketch

Yen-Cheng Kuan received his B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, and his M.S. degree in electrical engineering from the University of California, Los Angeles. From 2004 to 2007, he was a system engineer at Realtek Semiconductor Corp., Irvine, CA, where he contributed to the design of Ultra-wideband (UWB) System-on-a-Chip. Since 2009, he has been with Hughes Research Laboratories (HRL), Malibu, CA, working on software-defined radios, compressed-sensing receivers, and multi-rate signal processing for high-speed ADCs. His research interests include transceiver algorithm and implementation for communication systems, mixed-signal circuits, and communication standardizations.

Chapter 1

Introduction

The era of big data inevitably demands a large amount of data transfers in all communication mediums, among which wireless data link has become the most popular one due to its user-friendly and hassle free operation with mobility support. To support increasing demands of high-speed wireless data link applications, the 7 GHz unlicensed millimeter wave (mm-Wave) band spanning from 57 to 64 GHz has been allocated by the Federal Communication Commission (FCC) [1]. This wide unlicensed bandwidth stimulates several standard developments, such as IEEE 802.15.3c wireless personal area networks (WPAN) [2] and IEEE 802.11ad wireless local area networks (WLAN) [3], dedicated to multi-gigabit wireless communication and networking systems. Those standards/protocols greatly improve the effectiveness of data transfers for multiple users, and expand the linkage and coverage of various applications. Moreover, they aim to expedite the realization of widespread integrated circuits supporting big data transfers over the air.

Within the digital baseband receiver of an integrated circuit for wireless communications, the synchronizer is an essential component since all other digital signal processing (DSP) tasks, such as equalization, demodulation, and channel decoding, execute under the assumption that the receiver is “Synchronized”. The existing digital synchronizer designs for narrowband communication systems [4][5] require the receiver analog-to-digital converters (ADCs) to over-sample the receiving signal by an integer factor of 2 to 4 (relative to the symbol rate or signal bandwidth). For example, 44 MS/s

and 20MS/s receiver ADCs are utilized by the digital synchronizers for IEEE 802.11 a/b/g WLAN [4] and W-CDMA cellular network [5], respectively.

However, applying this integer over-sampling approach in the digital synchronizer design for a wideband communication system results in ADC design challenges, For example, in 802.15.3c and/or 802.11ad the defined 1.76 GS/s symbol rate and the required 10^{-7} bit-error-rate (BER) for $\pi/2$ 16-QAM to achieve 7 Gb/s throughput demand the ADC with 3.52 to 7.04 GS/s sampling rate and 6 to 8-bit resolution [6]. Furthermore, this high speed ADC requirement implicitly introduces the area overhead of the digital synchronizer. This overhead comes from the fact the synchronizer has to be implemented in a parallel architecture due to the speed constraint of the digital standard cells used for implementation. In addition, the number of parallelism is normally a power of two for ease of implementation. Therefore, given the maximum clock rate that a standard-cell based digital circuitry can operate at, the increasing in ADC sampling rate potentially causes the parallelism number to double, which increases the implementation area.

In addition to the synchronizer, an equalizer is another essential component of the digital baseband receiver due to its capability to combat notorious channel fading in wireless communications. Data-aided (DA) equalization is commonly used in most burst-mode wireless networking standards, including 802.15.3c and 802.11ad. A DA equalizer estimates the channel impulse response (CIR), and then equalizes the received symbols. Therefore, the performance of the equalizer highly depends on the accuracy of the channel estimation.

For DA equalization, the channel estimation can be obtained by assessing the received and distorted channel estimation sequence (CES). The preamble of a transmitted packet normally encapsulates multiple CESs. In order to get the frame of a received CES, the

existing DA equalizers [8]-[10] perform the frame synchronization by correlating the received signal with a known pattern that also resides in the preamble, and derive the frame boundaries from the correlation peak.

However, this approach does not guarantee that each frame represents the true channel response to a CES because those CESs are transmitted successively. The channel responses to adjacent CESs interfere with each other at the frame boundaries. The conducted simulation shows that in 802.15.3c the channel estimation generated by these contaminated channel response frames degrades the equalizer performance; the error-vector-magnitude (EVM) values increases from –19.1dB to –15.7dB under the non-line-of-sight (NLOS) 60 GHz channel model (CH2.3) provided in [11], and given 22dB receiver SNR.

In this dissertation, we present the algorithm and circuit design for a fractional-sampling-rate (1.5x) digital synchronizer to relax the required ADC specifications, and reduce the number of hardware parallelism. In addition, we present the algorithm and circuit for a high-accuracy digital channel estimator that can decouple the interferences from adjacent CESs to reduce the BER of an 802.11ac and/or 802.11ad compliant equalizer.

The dissertation is organized in the following order: Chapter 2 reviews the frequency plan, channel characteristics as well as emerging standards of the 60 GHz unlicensed band. Chapter 3 describes the digital baseband model, and illustrates the design challenge and/or issue for the digital synchronizer and channel estimator/equalizer in details. Chapter 4 describes the algorithms and hardware architecture of the fractional-sampling-rate (FSR) digital synchronizer. In particular, the parallel hardware architecture and multi-rate signal processing techniques are addressed. Chapter 5 describes the algorithm

and hardware architecture of the high-accuracy channel estimator. Moreover, the hardware architecture of a frequency-domain equalizer (FDE) that utilizes this channel estimator is illustrated. Chapter 6 describes the chip design and implementation methodologies, build-in-self-test (BIST) setups, and the measurement results. Chapter 7 draws the conclusion and future works.

Chapter 2

60 GHz Communication System

2.1 Frequency Plan

Since 1995 the US Federal Communications Commission (FCC) has started planning the regulations [1] for the unlicensed band at 59-64 GHz to react the envisioned and unstoppable demand of large data transfers over the air. Meanwhile the regulator organizations of other countries initiated investigations on the similar unlicensed frequency allocations to embrace this new era of high-speed wireless communication networks.

Currently, the North America (US and Canada), Japan, Australia, Korea, Europe Union, and China have established their respective spectrum allocations in the 60 GHz region. Figure 2.1 illustrates these frequency allocations.

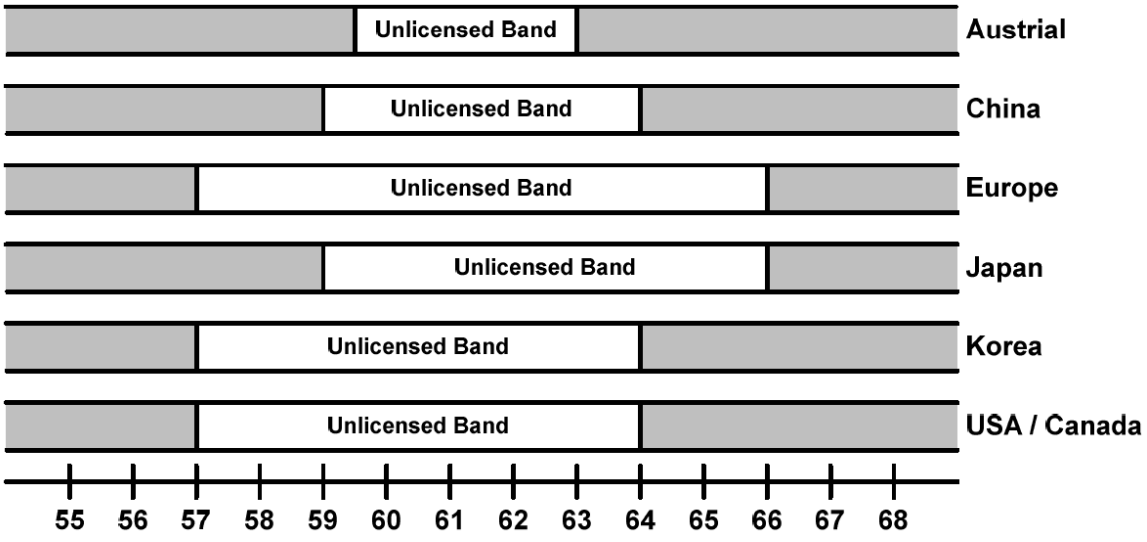


Figure 2.1 Worldwide 60 GHz frequency allocations.

It can be seen from Figure 2.1 that an overlapped and almost 4 GHz continuous bandwidth exists among the worldwide 60 GHz frequency band. By employing a low-order modulation scheme such as BPSK or QPSK on this wide unlicensed bandwidth, it is highly feasible to realize a wireless communication system ubiquitously supporting large data transfers at a rate of multi-Gb/s.

2.2 Main Link Losses

However, two major link losses affect the communication range of a 60 GHz wireless link. They are path loss and oxygen absorption. The commonly used free-space path loss model, which is described in Equations (2-1) and (2-2), indicates that the pass loss is about 68 dB for 1 meter transmission range.

$$PL(d,\lambda) = 20\log\left(\frac{4\pi d}{\lambda}\right) \quad \textbf{(2-1)}$$

$$PL(d,f)_{dB} = 32.45 + 20\log(f)_{GHz} + 20\log(d)_{m} = 68\Big|_{f=60,d=1} \quad \textbf{(2-2)}$$

The oxygen absorption is caused by a resonance of atmospheric oxygen molecules. As shown in Figure 2.2, at the sea level an attenuation peak of 15 dB/Km happens at 60 GHz. This value suggests the 60 GHz applications to operate within a range of 200 meters.

Considering those major losses whiling aiming to provide reliable wireless links, the FCC allows the maximum transmit power–equivalent isotropic radiated power (EIRP)–of the 60 GHz applications to be 40 dBm. This high EIRP limit provides more freedom to the transmitter design for the 60 GHz band than that for the ultra wideband (UWB) at 3.1-10.6 GHz; a UWB transmitter needs to confine a FCC-regulated power spectrum

mask of -41.3 dBm/MHz. The 60 GHz EIRP regulations of other countries range from 27 to 57 dBm.

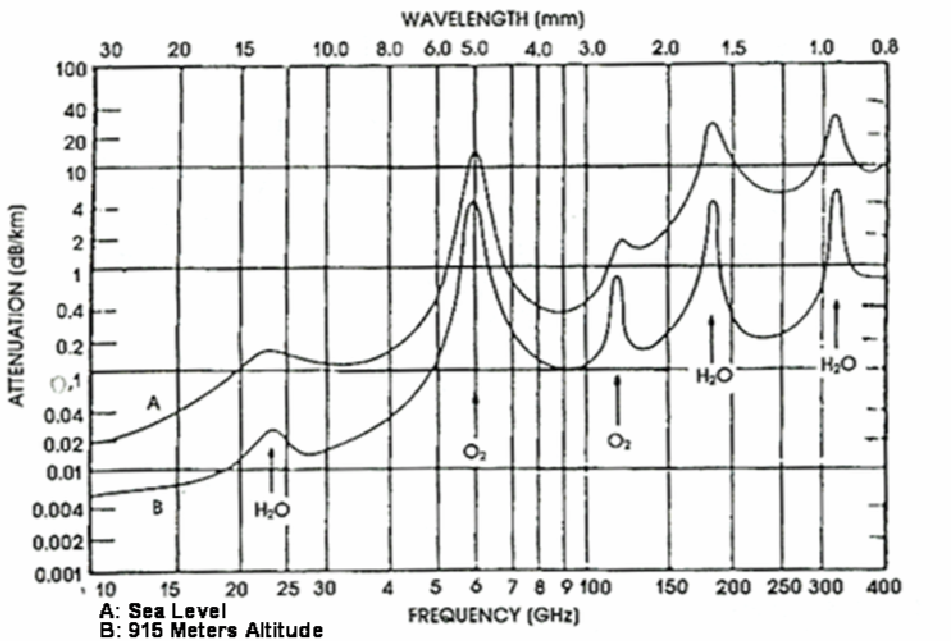


Figure 2.2 Average atmospheric absorption of millimeter waves (10-400 GHz).

2.3 Potential Applications

These nature-born losses and the regulated EIRP implicitly profile the types of potential applications in the 60 GHz band. Table 2-1 categorizes those applications, and shows that they are aligned with emerging standards and technologies in various areas such as multimedia, home entertainment, mobile computing, internet-of-things (IoT), etc. Among those applications, wireless high-definition TV (HDTV) streaming can be regarded as one of the very beginning driving forces to bring the 60 GHz band into the commercial usage. The popular 1920×1080 HDTV resolution with a progressive scan, 60 Hz frame rate as well as 24-bit pixel resolution demands a data rate of 3 Gb/s. Moreover, the pursuit for higher pixel resolution (30 or 26-bir) and/or faster frame rates (90 or 120

Hz) inevitably pushes the data rate requirement over 5 Gb/s. Realizing such high data rate wireless link in the popular unlicensed narrow bands (20-40 MHz) at 2.4 and/or 5 GHz requires high-order modulation schemes and high-complexity signal processing techniques, which cannot be implemented in an economical manner. As shown in Table 2-1, these potential applications are not limited to use only in indoor environments. Though the oxygen absorption constrains the transmission range of a 60 GHz wireless link within few hundred meters, a 60 GHz-based outdoor backhaul equipment that operates within such range finds its right spot to serve as a small-cell base station for the emerging long-term-evolution (LTE) cellular network. The deployments of small-cell base stations are envisioned as one of the enablers to boost the LTE network capacity by a factor of 1000x or more [13].

Category	Applications
Wireless display / HDTV	• TV projections in auditorium or conference room
	• Streaming from camcorder to TV / display
	• In-room video gaming
	• Video broadcasting in multiple rooms
	• Tablet / laptop display and storage
	• Multiple picture viewing
	• Wireless networking for office
Wireless file transfer	• Kiosk movie downloading
	• File synchronization between smartphone and laptop
	• Picture sharing among gadgets
	• Data center cable replacement
Backhaul	• Point-to-point backhaul
	• Intra large vehicle communication
	• Optical network replacement
	• Multimedia mesh network
Biomengineering	• High resolution medical image transferring
	• Wireless data telemetry for large-scale neural recording

Table 2-1 Categories of various 60 GHz applications.

2.4 Standardization

As described in Chapter 1, the unlicensed wide band in the 60 GHz region triggers a number of standard developments. Currently five related standards are finalized. They are WirelessHD [14], IEEE 802.15.3c [2], IEEE 802.11ad [3], WiGig [15], and ECMA-387 [16]. The first four standards are regarded as the representative ones because they are highly advocated by the industrial institutions and/or commercial companies.

2.4.1 WirelessHD

In 2007, the WirelessHD Consortium was established to develop a 60 GHz standard for consumer electronics products. As the name implies, it specially targets at the wireless high-definition (HD) video streaming; it aims to replace the High-Definition-Multimedia-Interface (HDMI) cable connecting an HDTV and a set-box. This standard applies the unequal-protection (UEP) technique to encode the video data for ensuring acceptable video perception while reducing the complexities of the channel encoder and decoder designs. In addition, this standard utilizes a hybrid network architecture that consists of wireless links in the 60 GHz and 2.4/5 GHz bands. The former serves as the main backbone for large data transfering, namely High-Rate Physical layer (HRP), and the latter constructs a control network with low or medium data traffic, namely Low-Rate Physical layer (LRP). Orthogonal-frequency-division-multiplexing (OFDM) modulation is adopted in both HRP and LRP. Though the system analysis shows that OFDM modulation has better BER performance for video streaming than the single-carrier modulation, the well-known drawback of high peak-to-average ratio (PARR) for OFDM modulation weakens the feasibility of using WirelessHD in portable devices. Given the 2.538GHz OFDM bandwidth, the latest WirelessHD specification (v1.1) [14] can support the coded data rate up to 7.138 Gb/s under 64-QAM modulation (in each sub-carrier).

2.4.2 IEEE 802.15.3c

The IEEE 802.15.3c standard is an amendment to IEEE 802.15.3-2003. The tasking group of IEEE 802.15.3c, namely TG3c, was formed before 2003 to develop the specifications for high-rate wireless personal area networks (WPAN) in an ultra wideband (UWB) ranging from 3.1 to 10.6 GHz. Two physical layer technologies: impulse radio and OFDM, were regarded as equivalently important at that time. The contention between these two camps ended up an un-finalized physical layer specification. The finalized medium-access control (MAC) specification became IEEE 802.15.3-2003. The promoters for the OFDM technology established the WiMedia alliance [17] after their breakup with IEEE 802.15.3. The specifications of WiMedia OFDM PHY and MAC layers were adopted by Wireless Universal-Seral-Bus (WUSB) Consortium [18]. In addition, the Bluetooth technology [19] once considered using the WiMedia OFDM PHY specification as the physical layer of Bluetooth 3.0.

After the un-resolvable contention of the impulse radio and OFDM camps, in 2005 a tasking group seeking for an alternative physical layer for IEEE 802.15.3 WPAN was formed. They shifted the frequency plan to the 60 GHz band. The number of participants in this tasking group (TG3c) gradually increased after a draft specification of WirelessHD was announced. It ended with a significant overlap of the participants working on these two standards. In 2009, the IEEE 802.15.3c standard was finalized with three physical layer modes. They are single carrier (SC), high-speed interface (HSI), and audio/visual (AV) modes. The HSI and AV modes use OFDM modulations. Furthermore, the AV mode is essentially the same as the PHY specification of WirelessHD 1.0. Given the 1.76 GS/s symbol rate in SC mode, 2.64 GHz OFDM bandwidth in HSI mode, and 2.538 GHz OFDM bandwidth in AV mode, the highest coded data rates provided by these three PHY

are 5.28, 5.05, and 3.807 Gb/s under π/2 16-QAM, 16-QAM, and 16-QAM modulations, respectively. Compared to the two OFDM-based modes (HSI and AV), the SC mode has the potential of consuming lower power; therefore being used in portable devices.

Figure 2.3 shows the channel frequency plan of IEEE 802.15.3c, and Figure 2.4 depicts its transmit spectral mask. This frequency plan and spectral mask are the same as those of the WirelessHD standard since IEEE 802.15.3c incorporates WirelessHD as its AV mode.

Channel Index	Start Freq. (GHz)	Center Freq. (GHz)	Stop Freq. (GHz)
1	57.24	58.32	59.40
2	59.40	60.48	61.56
3	62.56	62.64	63.72
4	63.72	64.80	65.88

Figure 2.3 Channel frequency for IEEE 802.15.3c (WirelessHD / IEEE 802.11ad / WiGig).

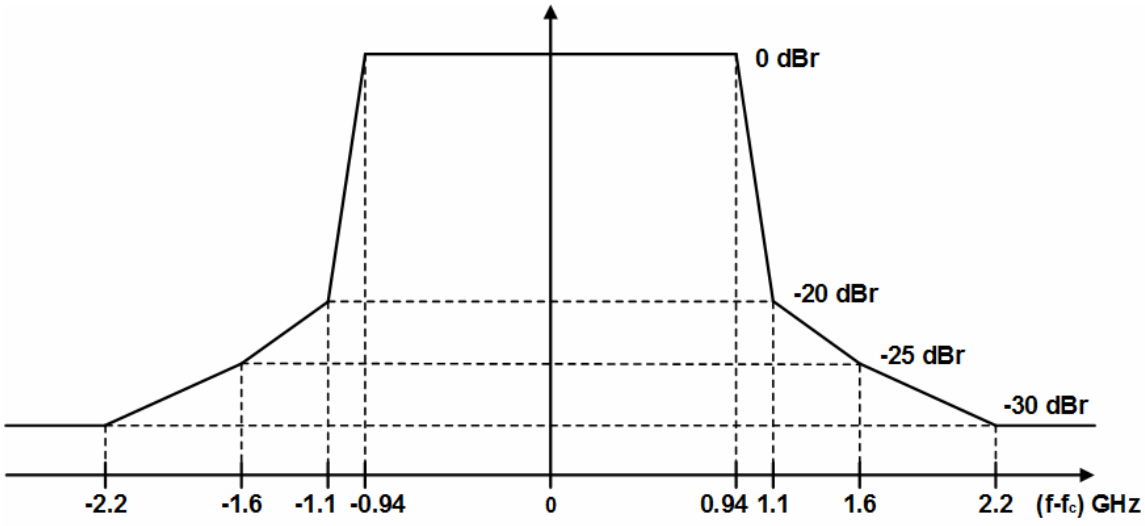


Figure 2.4 Transmit spectral mask of IEEE 802.15.3c (and WirelessHD).

2.4.3 IEEE 802.11ad

In late 2008, two tasking groups within IEEE 802.11 were formed for the project authorization request (PAR) of enabling very-high-throughput (VHT) in IEEE 802.11, where VHT stands for the capability of delivering over 1 Gb/s throughput. One tasking group, namely TGac, investigated new signal processing techniques in the existing 2.4 and/or 5 GHz bands, and the other one, namely TGad, started a new frequency plan in the 60 GHz band. The works of TGad became the IEEE 802.11ad standard. Like IEEE 802.15.3c, the physical layers of both SC and OFDM modes are defined in IEEE 802.11ad as well. Moreover, the SC modes of IEEE 802.11.ad and IEEE 802.15.3c are very similar, but the OFDM mode of IEEE 802.11ad is quite different to the OFDM-based HSI mode of IEEE 802.15.3c. The SC symbol rate and OFDM bandwidth of IEEE 802.11ad are the same as those of IEEE 802.15.3c (SC and HIS modes). They are 1.76 GS/s and 2.64 GHz, respectively. Furthermore, the SC and OFDM modes of IEEE 802.11ad can support the coded data rates up to 4.62 and 6.76 Gb/s under $\pi/2$ 16-QAM and 64-QAM modulations, respectively.

The channel frequency plan of IEEE 802.11ad is the same as that of IEEE 802.15.3c (and WirelessHD), which is shown in Figure 2.3. Figure 2.5 shows the transmit spectral mask of IEEE 802.11ad, which is slightly different to that of IEEE 802.15.3c (and WirelessHD).

2.4.4 WiGig

The Wireless Gigabit Alliance (WGA), which defined the WiGig standard, was established closely after the formation of IEEE 802.11 TGad. Essentially the WiGig 1.0 MAC and PHY specifications served as the initial draft (D.01) of IEEE 802.11ad. The similarities between the WiGig and IEEE 802.11ad standards eventually lead to a

consolidation; the WiGig 1.2 standard is identical to IEEE 802.11ad-2012. Moreover, in late 2012, the WGA was merged into the Wi-Fi Alliance [20], which promotes and certifies the 2.4/5 GHz IEEE 802.11-based products This incorporation reinforces the integration of IEEE 802.11-related standards for various frequency bands.

The channel frequency plan and transmit spectral mask of WiGig are shown in Figure 2.3 and Figure 2.5 since currently WiGig is identical to IEEE 802.11ad.

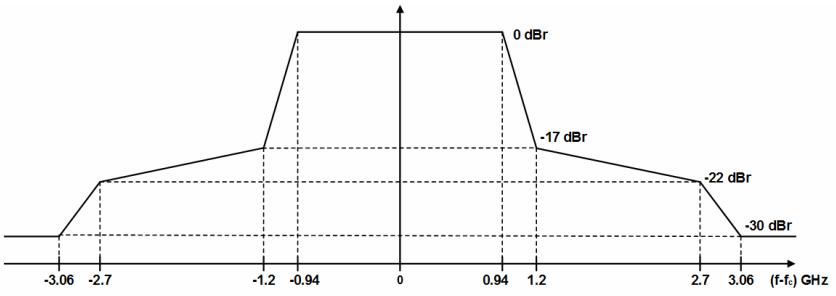


Figure 2.5 Transmit spectral mask of IEEE 802.11ad (and WiGig).

2.4 Channel Model

In the physical layer design for a wireless communication system, a proper and commonly-agreed channel model is necessary for system designers to evaluate the performances of the system with various parameter configurations. Among the aforementioned four representative 60 GHz standards, IEEE 802.15.3c is regarded as the one that provides most data of the 60 GHz channel model in public. Moreover, IEEE 802.11ad, which was established after the IEEE 802.15.3c, inherited a number of concepts and frameworks of the channel model developed in IEEE 802.15.3c. Therefore, the 60 GHz channel mode of IEEE 802.15.3c is adopted in this dissertation.

The TG3c conducted a series of 60 GHz channel measurements, and built a channel model [21] based on the Saleh-Valenzuela (SV) model [22] with the angular extension

proposed by Spencer at al [23]. The related model parameters are extracted from the measurement results. Furthermore, a distinct and strong line-of-sight (LOS) component found in most measurements is incorporated into the model. The equation (2-3) [21] describes the channel model.

$$h(t,\phi)=\beta\delta(t,\phi)+\sum_{l=0}^{L}\sum_{k=0}^{K_l}\alpha_{k,l}\delta(t-T_l-\tau_{k,l})\delta(\phi-\Omega_l-w_{k,l}) \qquad (2\text{-}3)$$

where $\beta\delta(t,\phi)$ is the LOS component, and $\sum_{l=0}^{L}\sum_{k=0}^{K_l}\alpha_{k,l}\delta(t-T_l-\tau_{k,l})\delta(\phi-\Omega_l-w_{k,l})$ is the SV model with the angular extension. Figure 2.6 [21] illustrates the channel model described by Equation (2-3).

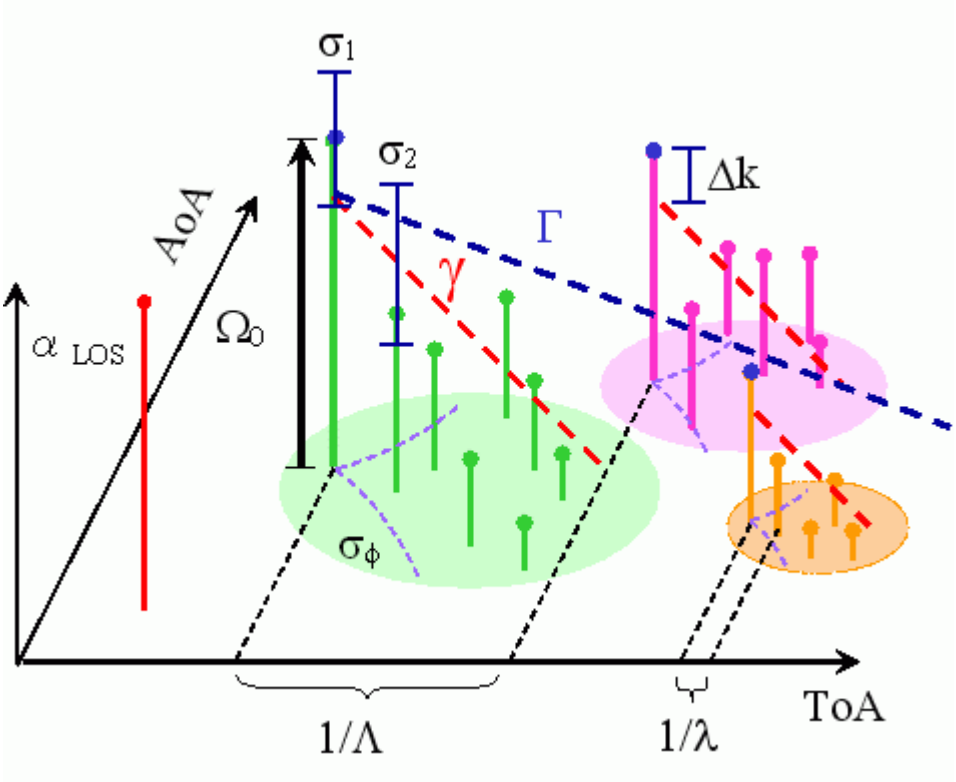


Figure 2.6 IEEE 802.15.3c clustered channel model consisting.

The LOS component can be obtained through a determinist approach like ray tracing or low-complexity geometrical models and/or in a statistical way. For example, the LOS component in a desktop environment can be modeled as following [21]:

$$\beta_{dB} = 20\log_{10}\left[\frac{\mu_d}{d}\left|\sqrt{G_{t1}G_{r1}} + \sqrt{G_{t2}G_{r2}}\Gamma_0 \exp\left[j\frac{4\pi h_1 h_2}{\lambda d}\right]\right|\right] - PL_d(\mu_d) \quad (2\text{-}4)$$

where

$$PL_d(\mu_d) = 20\log_{10}\left(\frac{4\pi d_0}{\lambda}\right) + A_{NLOS} + 10n_d \log_{10}\left(\frac{d}{d_0}\right) \quad (2\text{-}5)$$

where μ_d, Γ_0, λ, and A_{NLOS} are the mean distance, reflection coefficient, wavelength, and non-line-of-sight (NLOS) attenuation, respectively; h_1 and h_2 are the heights of the transmitter (TX) and receiver (RX), respectively; G_{t1} and G_{t2} are the TX gains for the first and second paths, respectively; G_{r1} and G_{r2} are the RX gains for the first and second paths, respectively.

The SV model can be regarded as the superposition of the channel impulse responses (CIRs) of each cluster. In equation (2-3), L is the number of clusters, and K_l is the number of rays in the l_{th} cluster. Furthermore, T_l and Ω_l are the mean time-of-arrival (ToA) and the mean angle-of-arrival (AoA) of the l_{th} cluster, respectively. Similarly, $\tau_{k,l}$, $\Omega_{k,l}$, and $\alpha_{k,l}$ represent the ToA, AoA, and amplitude of the k_{th} in the l_{th} cluster, respectively.

In addition, the cluster and ray ToAs: T_l and $\tau_{k,l}$, can be modeled as exponential random variables (RVs) conditioned on the previous arrival times. The equations (2-6) and (2-7) [21] show their probability density functions (PDFs).

$$p(T_l \mid T_{l-1}) = \Lambda[-\Lambda \exp(T_l - T_{l-1})], \qquad l > 0 \qquad \textbf{(2-6)}$$

$$p(\tau_{k,l} \mid \tau_{(k-1),l}) = \lambda[-\lambda \exp(\tau_{k,l} - \tau_{(k-1),l})], \qquad k > 0 \qquad \textbf{(2-7)}$$

where Λ and λ are the cluster and the ray arrival rates, respectively. Moreover, a conditional uniform distribution RV, as shown in Equation (2-8) [21], is used to model the cluster AoA

$$p(\Omega_l \mid \Omega_{l-1}) = \frac{1}{2\pi} \qquad \textbf{(2-8)}$$

As for the ray AoA in a cluster, it can be modeled by either zero-mean Laplacian or zero-mean Gaussian distributions, which are shown in Equations (2-9) and (2-10) [21], respectively.

$$p(w_{k,l}) = \frac{1}{\sqrt{2}\sigma_\phi} \exp\left(-\left| \frac{\sqrt{2} w_{k,l}}{\sigma_\phi} \right| \right) \qquad \textbf{(2-9)}$$

$$p(w_{k,l}) = \frac{1}{\sqrt{2\pi}\sigma_\phi} \exp\left(\frac{-w_{k,l}^2}{2\sigma_\phi^2} \right) \qquad \textbf{(2-10)}$$

Finally, the cluster and ray amplitudes can be modeled by the log-normal distributions as shown in Equation (2-11) and (2-12) [21], respectively.

$$p(R) = \frac{1}{\sqrt{2\pi}\sigma_R R} \exp\left(\frac{-(\ln R - \mu_R)^2}{2\sigma_R^2} \right) \quad \textbf{(2-11)}$$

$$p_l(r) = \frac{1}{\sqrt{2\pi}\sigma_r r} \exp\left(\frac{-(\ln r - \mu_r)^2}{2\sigma_r^2} \right) \quad \textbf{(2-12)}$$

where μ_R and μ_r are the means of $\ln(R)$ and $\ln(r)$, respectively, and σ_R and σ_r are the variances of $\ln(R)$ and $\ln(r)$, respectively.

Figure 2.7 shows the values of aforementioned channel model parameters, which are extracted from the measurement data of experiments conducted in various environments.

Parameters	CM1.1	CM1.3	CM1.4	CM3.1	CM4.1
Γ (ns)	4.5	21.5	12.6	49.8	109.2
γ (ns)	6.25	4.35	4.98	45.20	67.90
Λ (1/ns)	0.191	0.144	0.045	0.041	0.032
λ (1/ns)	1.22	1.17	0.93	0.97	3.45
Δk (dB)	18.8	11.9	4.6	21.9	19.0
σ_R	6.28	3.71	7.34	6.60	3.24
σ_r	13.01	7.31	6.11	11.30	5.54
σ_ϕ	50	46	107	102	60
n_d	2.00	2.00	2.00	2.00	3.35

CM1: Residential LOS, CM3: Office LOS, CM4: Office NLOS

Figure 2.7 IEEE 802.15.3c channel model parameter values.

Combing these measured parameter values and the aforementioned equations describing the channel model, TG3c built a Matlab®-based program [11], which can take inputs of the user such as the environment scenario, carrier frequency, beam-width of the transmitter and receiver, baseband sampling rate, etc to generate the channel model in a format of discrete-time channel impulse response (CIR). Figure 2.8 shows four exemplary CIR realizations generated by the program for the case of NLOS residential environment (CM2.3), 60 GHz carrier frequency, 30-degree receiver reception beam-width, and 1.76 GS/s baseband sampling rate. Figure 2.9 depicts the corresponding frequency responses of these four CIR realizations.

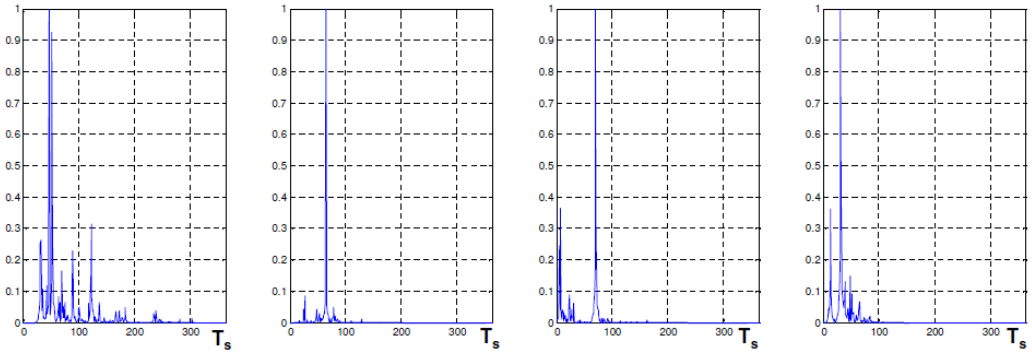


Figure 2.8 Four exemplary time-domain CIR realizations of IEEE 802.15.3c channel model.

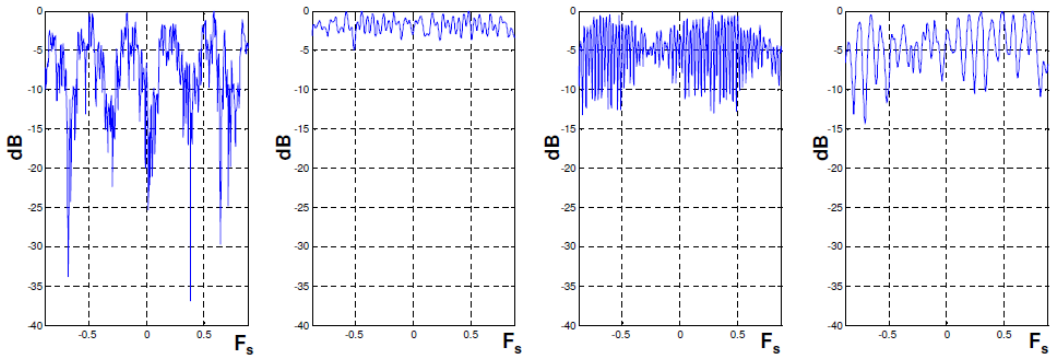


Figure 2.9 Frequency responses of the four exemplary CIR realizations.

Chapter 3

System Model

3.1 Digital Baseband Model

Among the aforementioned four representative 60 GHz standards, the single-carrier physical layer (SC-PHY) exists in each of them except WirelessHD, which adopts the OFDM modulation only. Furthermore, the SC modulation is used in the preambles for both SC and OFDM modes of these three standards–IEEE 802.15.3c, IEEE 802.11ad, and WiGig. Though the respective highest data rates of these three standards are provided by their corresponding OFDM modes, the SC-PHY finds its unique and important role to fulfill the increasing demand of energy-efficient wireless devices. In particular, compared to the OFDM PHY, the SC-PHY provides lower PAPR, and fits more nicely in the category of battery-powered (mobile) devices that has the stringent requirement on power consumption. In addition, the frequency contention caused by devices of various standards becomes more and more significant. Using frequently-exchanged control/signaling packets is regarded one of the effective approaches to resolve this contention. Adopting the OFDM modulation for those control/signaling packets may overkill since these packets carry only a small amount of control and/or identification information in stead of large data for applications. Indeed, the control/signaling physical layers of these three standards all choose the SC modulation. Moreover, their packet structures are similar to those of the SC-PHY used for data transferring (not for controlling/signaling). Therefore, the SC-PHY hardware has the potential of being reused by the control/signaling PHY through a few reconfigurations.

In this dissertation, the SC-PHY of IEEE 802.15.3c is adopted for the design and implementation of a digital baseband receiver for the 60 GHz wireless communication. This receiver can be migrated to support the SC-PHY of IEEE 802.11ad (and/or WiGig) due to the similarity of the packet structures of IEEE 802.15.3c and 802.11ad. Furthermore, this dissertation addresses the inner receiver–synchronizer and equalizer–design, so the channel encoder and decoder are not included; the un-coded metrics serve as the performance benchmarks. In addition, the IEEE 802.15.3c channel model [11] described in Chapter 2 is used in the development for this digital baseband receiver.

Figure 3.1 depicts the system model used in this dissertation. In the digital baseband transmitter (DBB-TX), two bit-streams: preamble and data, are mapped to the I/Q (complex) symbols through their corresponding modulators. $\pi/2$ BPSK is employed on the preamble bit-stream. On the other hand, the data bit-stream has multiple modulation options including $\pi/2$ BPSK, $\pi/2$ QPSK, $\pi/2$ 8-PSK, and $\pi/2$ 16-QAM. The symbols generated by the two modulators are multiplexed into the subsequent pulse-shaping filter (PS-FIR). For a complete packet transmission, the preamble symbols are sent first, and followed by the data symbols. The output spectrum of the PS-FIR should follow the transmission spectral mask specified in IEEE 802.15.3c. Figure 3.2 redraws this mask, and shows that a square-root-raised-cosine (SRRC) filter with 0.25 roll-off factor meets this specification.

As shown in Figure 3.1, the output of the PS-FIR goes into the 60 GHz channel model provided by the IEEE 802.15.3c task group (TG3c) [11]. The channel-distorted symbols generated by the channel model are further added by the additive-white-Gaussian noise (AWGN) that models the aggregation of all the thermal noise seen at the input of the digital baseband receiver (DBB-RX).

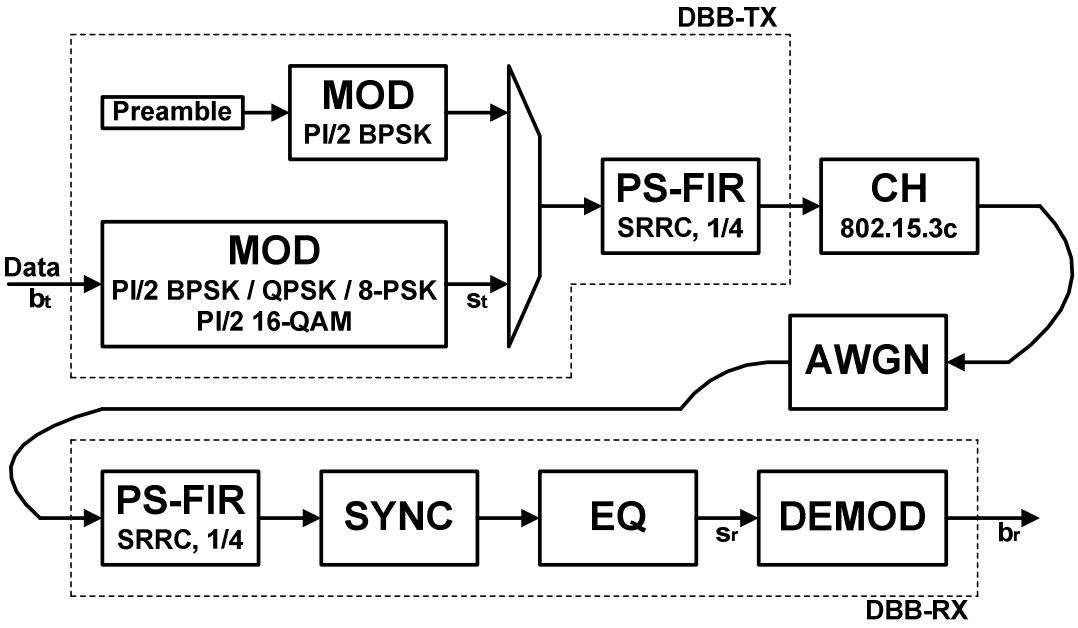


Figure 3.1 System model for development of digital baseband receiver (DBB-RX)

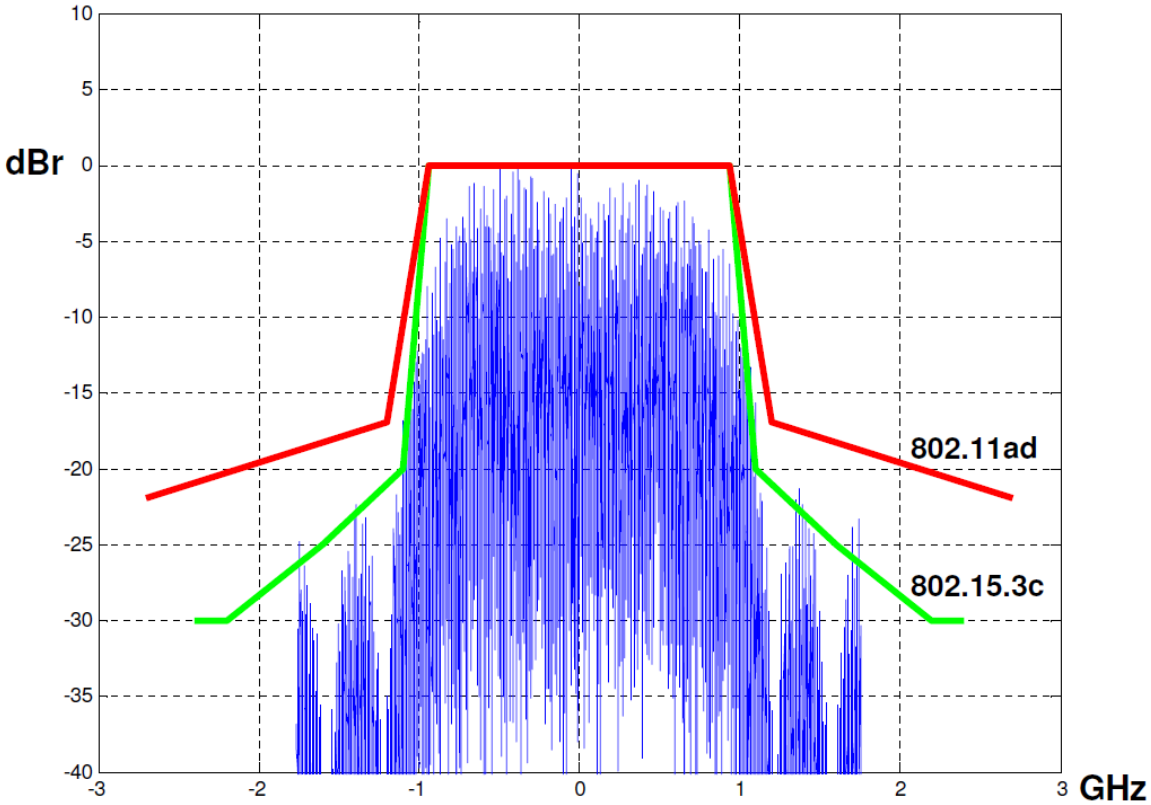


Figure 3.2 Power spectrum of symbols shaped by square-root-raised-cosine filter with 0.25 roll-off factor.

The DBB-RX takes the output of the AWGN model, and sequentially performs the tasks of pulse-shape filtering (PS-FIR), synchronization (SYNC), equalization (EQ) and demodulation (DEMOD). To be paired with the pulse-shaping filter used in the DBB-TX, another SRRC filter with the same roll-off factor (0.25) is adopted in the pulse-shaping filter of the DBB-RX. Moreover, in this dissertation, the synchronizer (SYNC) addresses the digital signal processing (DSP) units of packet detection, carrier recovery, symbol timing recovery, and frame synchronization. The output of the synchronizer goes into the equalizer (EQ) that compensates the distortion effects caused by the channel model. The following demodulator (DEMOD) makes the decisions for each equalized symbol and generates the corresponding data bits. All the signals in the system model are complex numbers except the preamble and data bit-streams at DBB-TX, and the bit-stream generated by the DEMOD at DBB-RX. Those bit-streams are binary numbers.

In this dissertation, two metrics are used to evaluate and demonstrate the performances of the DBB-RX design. They are error-vector magnitude (EVM) and bit-error-rate (BER), which are defined in Equations (3-1) and (3-2), respectively.

$$\boldsymbol{EVM}_{\boldsymbol{dB}} = 10\log_{10}\left(\frac{\frac{1}{N}\sum_{k=1}^{N}\left|s_{r,k}-s_{t,k}\right|^2}{\frac{1}{N}\sum_{k=1}^{N}\left|s_{t,k}\right|^2}\right) = 10\log_{10}\left(\frac{\sum_{k=1}^{N}\left|s_{r,k}-s_{t,k}\right|^2}{\sum_{k=1}^{N}\left|s_{t,k}\right|^2}\right) \qquad \textbf{(3-1)}$$

$$\boldsymbol{BER}_{\%} = \left(\frac{\sum_{k=1}^{N}\sum_{j=1}^{M}\left|b_{r,k}(j)-b_{t,k}(j)\right|}{NM}\right)\times 100\% \qquad \textbf{(3-2)}$$

where $s_{t,k}$ and $s_{r,k}$ represent the k_{th} symbol generated by the data modulator at DBB-TX and the k_{th} symbol generated by the equalizer at DBB-RX, respectively; $b_{t,k}$ and $b_{r,k}$ denote the bit set corresponding to the k_{th} symbol generated by the data modulator at DBB-TX and the bit set corresponding to the k_{th} symbol generated by the equalizer at DBB-RX, respectively; N and M are the number of transmitted (received) symbols and the number of bits that each symbol conveys, respectively.

3.2 Synchronizer Design Challenge

In a digital baseband receiver for wireless communications, the synchronizer has the highest priority than other digital signal processing (DSP) units, such as equalizer, demodulator, channel decoder, etc, since those units execute under the assumption that the receiver is "synchronized". The synchronizer can be regarded as the first unit that processes the receiving signal samples provided by the receiver ADCs. The maximum sampling rate of the receiver ADC affects the hardware architecture of the synchronizer, and vice-versa; the hardware architecture of the synchronizer determines the required sampling rate of the receiver ADC.

Moreover, an all digital synchronizer requires the receiver ADCs to over-sample the receiving signal by an over-sampling ratio (relative to the symbol rate or signal bandwidth). This can be validated by the sampling rate requirement for the symbol timing recovery in a single-carrier receiver. The symbol-rate only symbol timing recovery can only be achieved in an analog or hybrid (partial analog and partial digital) manner [24]; the all digital symbol timing recovery requires higher-than-symbol-rate sampling.

Only few published papers describe the hardware architecture and silicon (CMOS) implementation of a single-carrier digital baseband receiver including the synchronizer.

Figure 3.3 shows a published commercial IEEE 802.11b system including the baseband processor (BBP) [4]. Figure 3.4 shows the hardware architecture a fabricated baseband (modem) chip for WCDMA [5]. In Figure 3.3, the (I/Q) ADCs of the BBP operate at the sampling rate of 44 MS/s, which is four times of the symbol rate defined in IEEE 802.11b. In addition, it can be seen from Figure 3.4 that the ADCs adopt a 4x over-sampling ratio (OSR), which corresponds to a sampling rate of 5MS/s given the 1.25MHz signal bandwidth used in WCDMA. (The 4x OSR ADC used for intermediate-frequency (IF) architecture can be regarded as equivalent to two 2x OSR ADCs for direct-conversion (zero-IF) architecture) Designing these low sampling rate (5 to 44 MS/s) and medium to high resolution (8 to 12-bit) ADCs in state-of-art CMOS technologies is manageable and can be well achieved.

However, applying this integer OSR (2x to 4x) scheme on the digital synchronizer (baseband) design for the 60 GHz wireless communication (IEEE 802.15.3c) results in ADC design challenges. Given the 1.76 GS/s symbol rate defined in the standard, a sampling rate of 3.52 to 7.04 GS/s is required. In addition, achieving an acceptable BER, normally 10^{-7}, at 7Gb/s throughput under $\pi/2$ 16-QAM modulation implicitly determines the ADC resolution, which is from 6 to 8-bit. From the well-know Walden and Murmann chart [25] tracking the measured ADC performances historically, the ADC with such high sampling rate (> 3.5 GS/s) and medium resolution (6 to 8-bit) is still a territory that hasn't been completely conquered yet. ADC designers need to spend significant efforts fighting the trade-off between speed and linearity for such specification, especially when the low-power consumption required by mobile and/or gadget devices is taken into account.

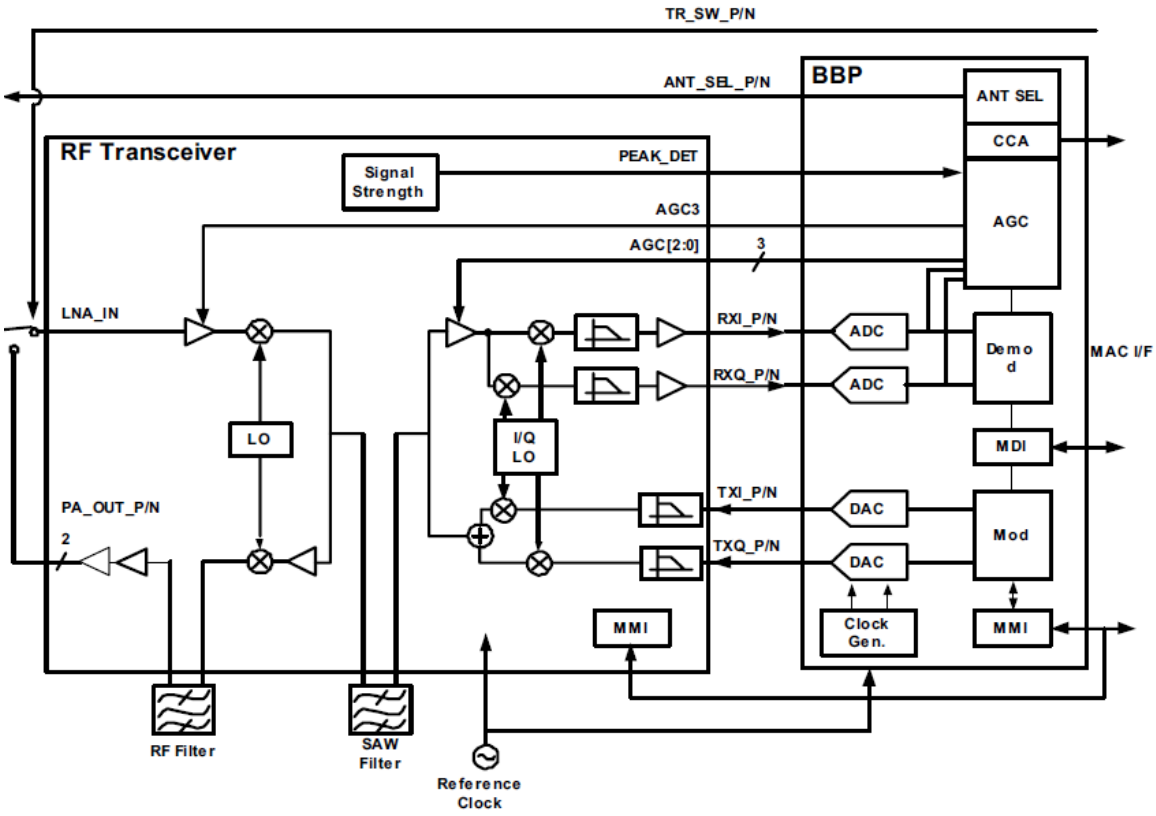


Figure 3.3 Commercial IEEE 802.11b system including digital baseband processor.

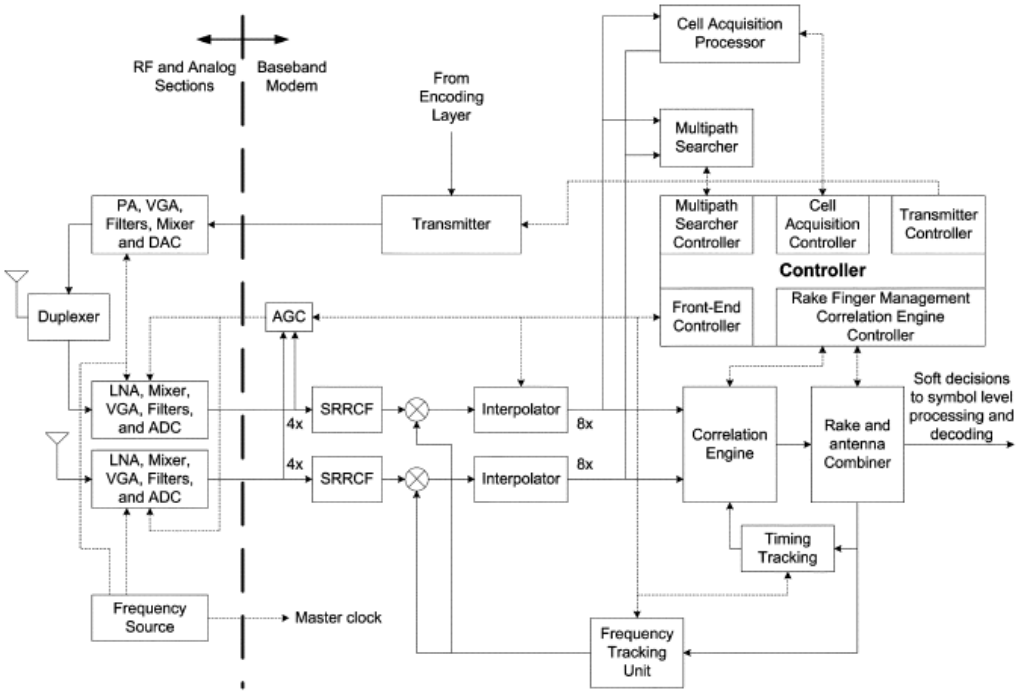


Figure 3.4 WCDMA digital baseband modem.

Furthermore, this requirement of high speed ADCs implicitly imposes the area overhead on the digital synchronizer. This overhead comes from the fact that the synchronizer has to be implemented in a parallel architecture because none of the state-of-art DSP circuits that are implemented through the digital standard cells can achieve the clock speed that equals to this high ADC sampling rate (> 3.5 GS/s). In addition, the number of the hardware parallelism is normally a power of two for ease of clock implementations. Considering the 65-nm CMOS digital implementation, in which the digital circuits usually operate below 700MHz, an 8 to 16 parallel architecture is required for the synchronizer that process the samples generated the receiver ADCs which are operating at 3.52-7.04GS/s.

3.3 Equalizer (Channel Estimator) Design Issue

On the other hand, to combat notorious channel fading in wireless communications, an equalizer is another essential unit of the receiver. Data-aided (DA) equalization is commonly used in most burst-mode wireless networking standards including IEEE 802.15.3c. A DA equalizer estimates the channel impulse response (CIR), and then equalizes the received symbols. Therefore, the equalizer performance highly depends on the accuracy of the channel estimation.

For DA equalization, the channel estimation can be obtained by assessing the received and distorted channel estimation sequence (CES). The preamble of a transmitted packet normally encapsulates several CESs. Figure 3.5 shows the preamble structure used in IEEE 802.15.3c. It consists of 18 repetitions of G_{128a}, a Golay code, with various polarities for synchronization, and five CESs. These CESs are G_{256a}, G_{256b}, G_{256a}, G_{256b}, and G_{128b}, among which G_{256a} and G_{256b} are a pair of Golay complementary codes (GCC), and so are G_{128b} and G_{128a} that is used for synchronization. As described previously in the

DBB-TX model, this preamble bit-stream is employed by π/2-BPSK modulation. The IEEE 802.11ad (WiGig) standard has a similar preamble definition [3].

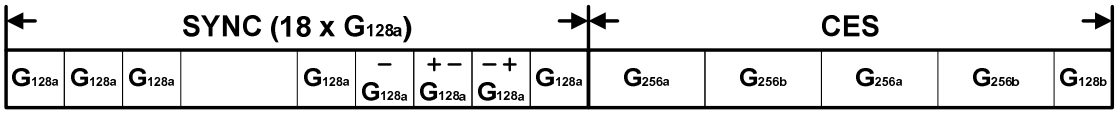


Figure 3.5 Preamble structure of IEEE 802.15.3c.

The "Part a" and "Part b" of GCC, G_{256a} and G_{256b} for example, have a special property that the summation of the correlation result of the "received Part a" and "Part a", and that of the "received Part b" and "Part b" is the channel impulse response (CIR) [26]. Therefore, the straightforward and existing approaches [8][9] for an IEEE 802.15.3c-compliant equalizer to estimate the CIR consist of two steps: (1) find the frames of the two successively received CESs (G_{256a} and G_{256b}) by correlating the received signal with a known pattern (for example, G_{128a} in the SYNC field); and (2) pass these two frames to their corresponding Golay correlators, add the correlator outputs, and obtain the CIR. The two occurrences of the GCC (G_{256a} and G_{256b}) in the preamble allow averaging two CIRs to remove certain amount of noise.

However, this straightforward approach does not guarantee each frame representing the true channel response to a CES (G_{256a} or G_{256b}) because those CESs are transmitted successively. As shown in Figure 3-4, the channel responses to adjacent CESs (G_{256a} and G_{256b}) interfere with each other at the frame boundary. Furthermore, Figure 3-5 depicts the equalized 16-QAM constellations obtained through the channel estimations with and without those channel response interferences. It can be observed from Figure 3-5 that the channel estimation generated by the contaminated channel response frames will degrade

the equalizer performance; the EVM increases from –19.1dB to –15.7dB under the non-line-of-sight (NLOS) 60 GHz channel model (CH2.3) of IEEE 802.15.3c, and given 22dB receiver SNR.

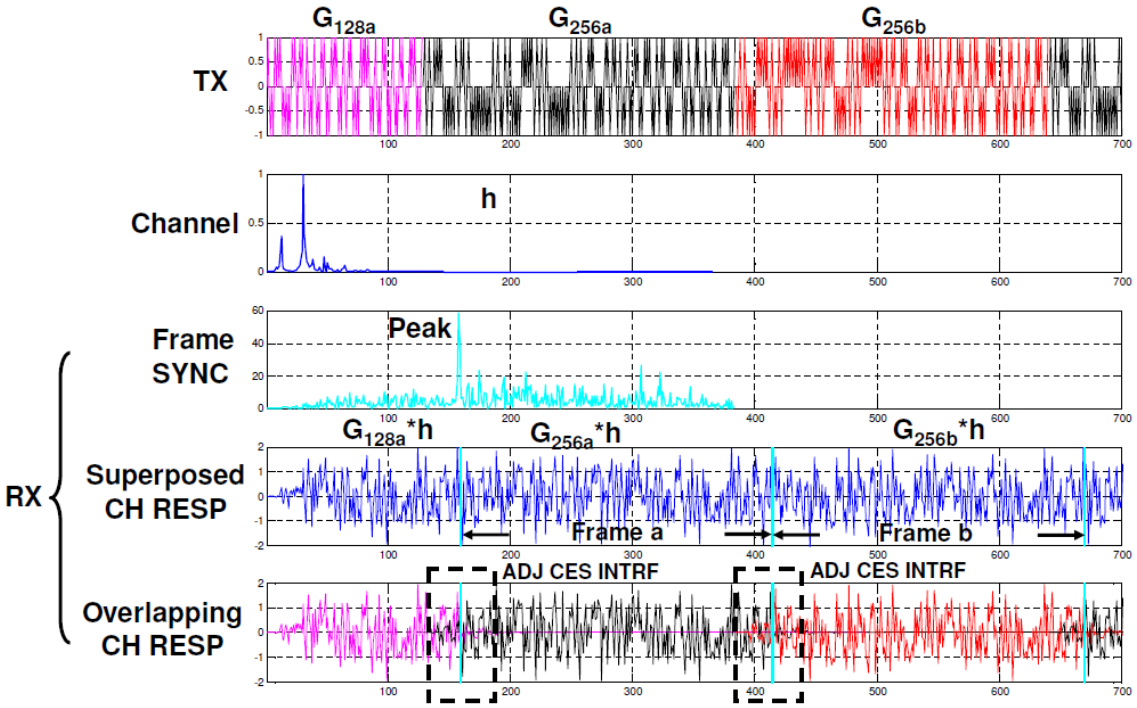


Figure 3.6 Interference at boundary of channel responses to adjacent CESs.

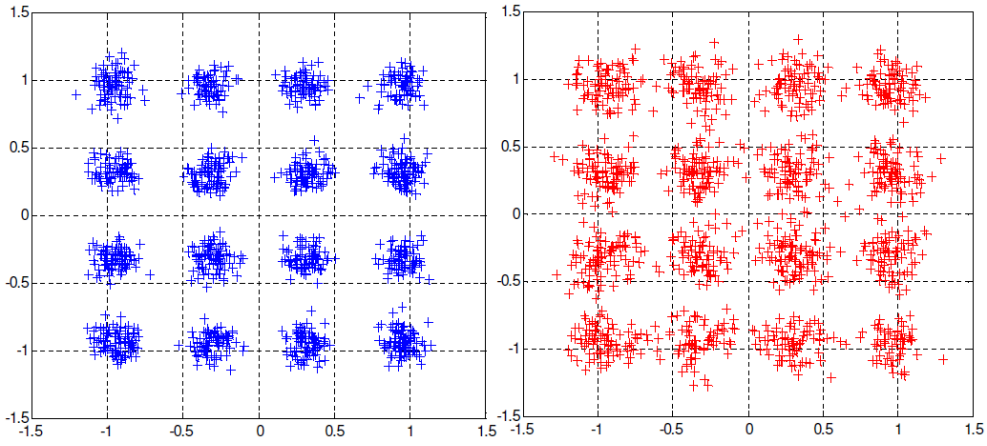


Figure 3.7 EVM comparisons for cases with (right) and w/o (left) adjacent CES interferences.

Chapter 4

Fractional-Sampling-Rate Digital Baseband Receiver / Synchronizer

As described in Chapter 3, applying the integer OSR scheme on the digital receiver baseband (synchronizer) design for IEEE 802.15.3c results in ADC design challenges and the potential area overhead. In this chapter, we present a digital synchronizer that requires only 2.64GS/s (one and half of the symbol rate) ADCs for an 802.15.3c baseband receiver in SC mode. This sampling rate reduction relaxes the ADC specification, and reduces the hardware parallelism. The proposed synchronizer performs packet detection, carrier recovery, and timing recovery for various 60GHz channel conditions of IEEE 802.15.3c [11]. Multi-rate signal processing techniques are used extensively to make those synchronization tasks operate at proper (just enough) clock rates. Especially in timing recovery, a polyphase match filter is utilized to eliminate the timing interpolator, and therefore reduce power consumption. The proper choice of the sub-filter number for the polyphase filter makes the synchronizer achieve timing synchronization within the SYNC period of the 802.15.3c preamble in a data-aided manner. The (almost) feed-forward architecture is adopted for this synchronizer due to the must-have hardware parallelism resulted from the speed limitation of the standard-cell based digital implementation. Parallel architectures for single-stream (non-parallel) digital signal processing (DSP) units are developed and will be described in the following sections.

4.1 Digital Synchronizer Architecture

The digital synchronizer uses the SYNC field of the 802.15.3c preamble in SC mode to perform packet detection, carrier recovery and timing recovery sequentially and at various throughputs. Figure 4.1 shows the preamble structure with the fields of SYNC, SFD and CES. The synchronization process has to settle within the SYNC period, which consists of 14 repetitions of Golay code (G_{128a}) modulated by PI/2 BPSC.

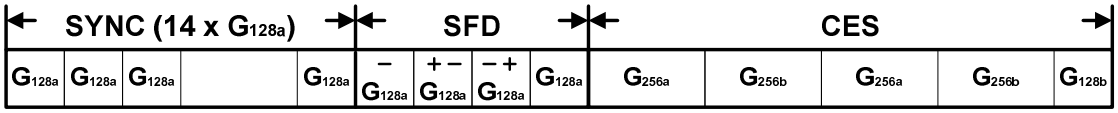


Figure 4.1 Preamble structure of IEEE 802.15.3c. (Redrawing of Figure 3.5)

Figure 4.2 shows the architecture of the digital synchronizer architecture. The incoming radio-frequency (RF) signal is down-converted to the analog baseband through the RF I/Q mixers. The down-converted I/Q signals are filtered by the analog baseband filter. The I/Q ADCs sample the filtered analog baseband signals at a sample rate of 2.64GS/s and de-multiplex the digital samples into 4-parallel data streams, each of which operate at 660MS/s to satisfy the speed constraint of the digital circuit implementation in 65-nm CMOS. Given the 1.76GS/s symbol rate ($\boldsymbol{F}_{sym}$) and the square-root raised-cosine (SRRC) filter with approximately 0.25 roll-off factor fulfilling the transmission spectral mask requirement of IEEE 802.15.3c [2], the two-sided bandwidth of the received signals equals to 2.2GHz ($1.25\boldsymbol{F}_{sym}$). Therefore, the sample rate of 2.64GS/s ($1.5\,\boldsymbol{F}_{sym}$) does not introduce aliasing because it covers the two-side signal bandwidth. Though the sampling rate increases from 2.2GS/s to 2.64GS/s, this increasing is still manageable for the related

mixed-signal circuit designs. Moreover, this sampling rate increasing helps relax design specifications of the I/Q low-pass filters (LPF) at the analog baseband.

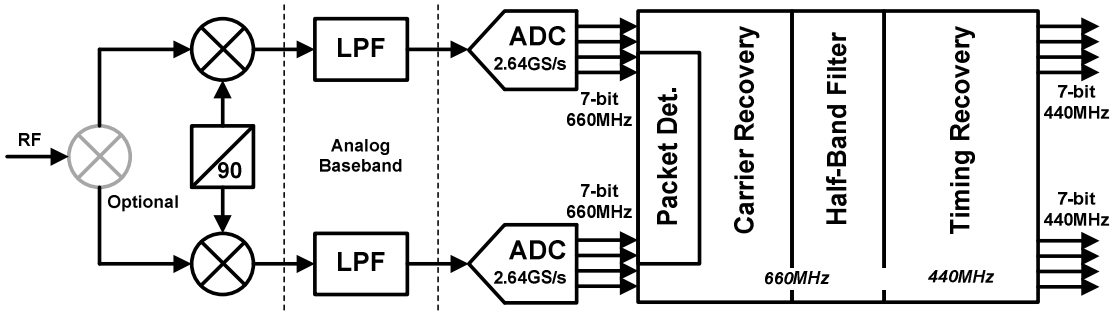


Figure 4.2 Architecture of digital synchronizer

4.2 Packet Detector

As shown in Figure 4.2, the packet detector and carrier synchronizer directly fetch the 4-parallel digital outputs of the I/Q ADCs. The packet detection adopts the delay-and-correlate algorithm [31], which is described in Equations (4-1) to (4-4). Given the received signal $\boldsymbol{r_n}$, the algorithm calculates the cross-correlation value of $\boldsymbol{r_n}$ and $\boldsymbol{r_{n+D}^*}$, the square magnitude of $\boldsymbol{r_n}$, and the square magnitude of $\boldsymbol{r_{n+D}}$, where $\boldsymbol{D}$ equals to the length of the repetitive pattern for synchronization. In the ideal scenario without noise, comparing the ratio of $\dfrac{\boldsymbol{w_c}\left|\boldsymbol{r_n r_{n+D}^*}\right|^2}{\boldsymbol{w_a}\left(\left|\boldsymbol{r_n}\right|^2\right)^2+\boldsymbol{w_p}\left(\left|\boldsymbol{r_{n+D}}\right|^2\right)^2}$ with a threshold $\boldsymbol{\gamma}$ can determine the existence of a valid packet. However, the noise existing in the real scenario degrades the accuracy of this packet detection. Therefore, three moving averages (MAs), each denoted as $\sum_{k=0}^{L=1}$, are employed on $\left|\boldsymbol{r_n r_{n+D}}\right|$, $\left|\boldsymbol{r_n}\right|^2$, and $\left|\boldsymbol{r_{n+D}}\right|^2$, respectively to remove certain amount of noise for increasing the rate of the accurate detection.

$$c_n = \sum_{k=0}^{L-1} r_{n+k} r_{n+k+D}^{*} \quad (4\text{-}1)$$

$$a_n = \sum_{k=0}^{L-1} r_{n+k} r_{n+k}^{*} = \sum_{k=0}^{L-1} \left| r_{n+k} \right|^2 \quad (4\text{-}2)$$

$$p_n = \sum_{k=0}^{L-1} r_{n+k+D} r_{n+k+D}^{*} = \sum_{k=0}^{L-1} \left| r_{n+k+D} \right|^2 \quad (4\text{-}3)$$

$$m_n = \frac{w_c \left| c_n \right|^2}{w_a (a_n)^2 + w_p (p_n)^2} \quad (4\text{-}4)$$

$$m_n \geq \gamma \Rightarrow valid - packet \quad (4\text{-}5)$$

Figure 4.3 shows a single-stream hardware architecture of this packet detection for the preamble of IEEE 802.15.3c. In this architecture, D is set to 192 because the length of the repetitive pattern–G_{128a} is 128, and 1.5x over-sampling is applied. Shows a cascaded-integrated-combo (CIC) filter-based moving average, which has the advantage of using only two adders, and (N+1) delays (if no pipeline register exists in between these two adders).

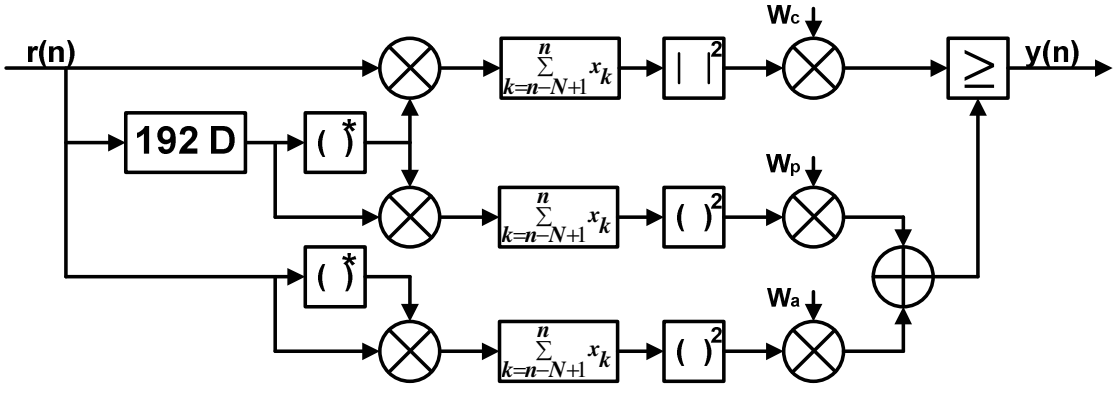


Figure 4.3 Single-stream architecture realizing delay-and-correlate packet detection algorithm for IEEE 802.15.3c.

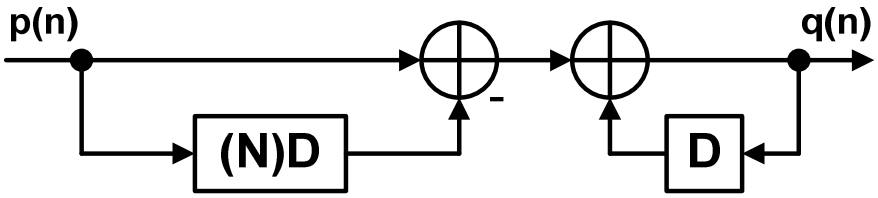


Figure 4.4 Single-stream architecture of moving average.

Assuming the parallel architecture of the single-stream MA is available, the single-stream packet detector architecture shown in Figure 4.4 can be parallelized. Figure 4.5 shows this parallel architecture whose number of parallelism is four.

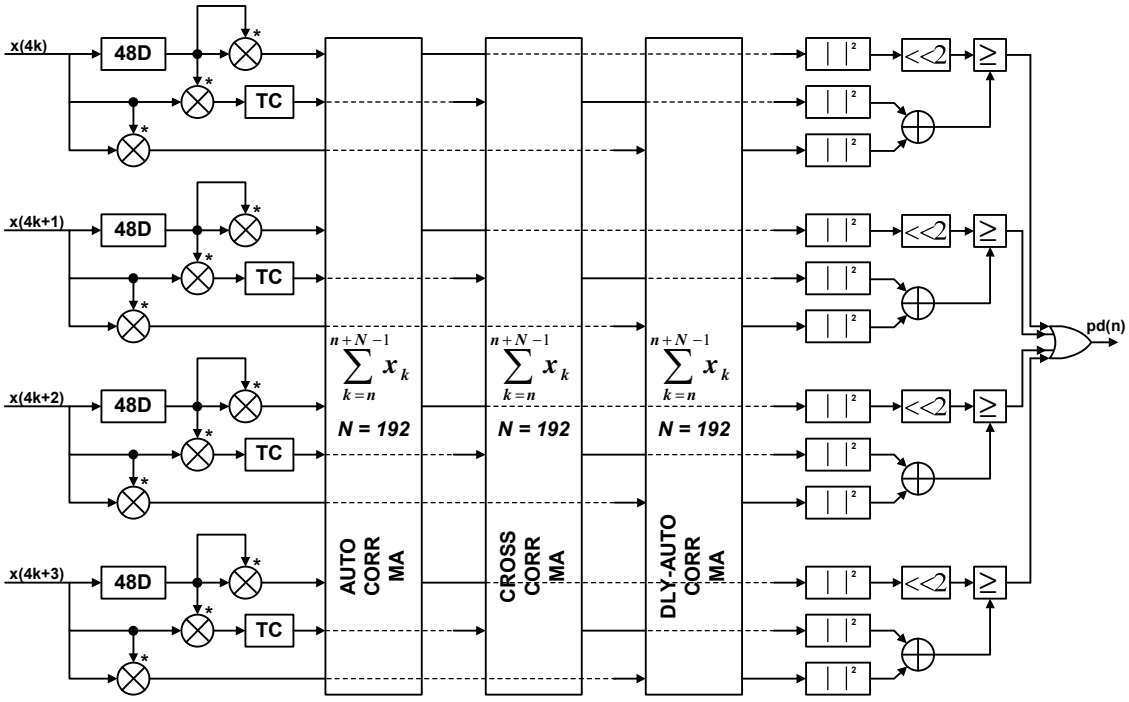


Figure 4.5 Architecture of 4-parallel packet detector.

As shown in Figure 4.4, the single-stream MA can be regarded as a cascade of a feed-forward delay and add unit (left) and a 1st-order infinite-impulse-response (IIR) filter

(right), which has a feedback path. By employing the loop-unrolling on the IIR, Fig. shows a 4-parallel MA architecture, which cascades a 4-parallel delay and add unit and a 4-parallel IIR. However, this loop-unrolling increases the critical path length.

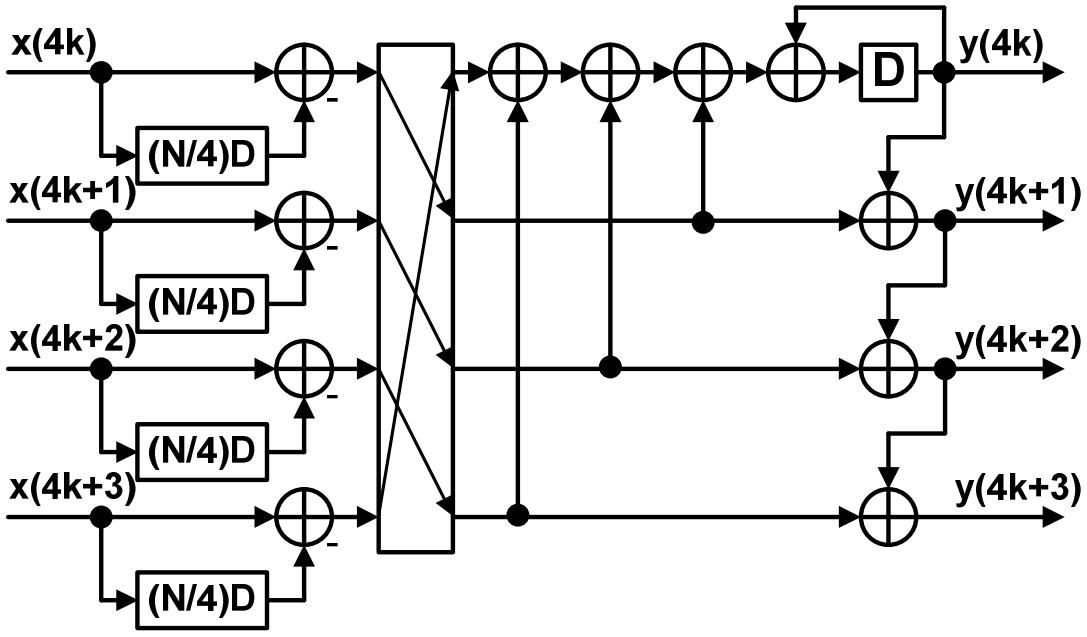


Figure 4.6 4-parallel MA architecture through straightforward parallelism on the single-stream.

Instead of directly parallelizing the CIC-based MA, we observe the parallel data flow directly, and present a 4-paralle MA architecture that keeps the minimum critical path (one adder if pipeline applied) while still utilizing the CIC filters to minimize the adder usage. Figure 4.7 depicts the proposed architecture, which consists of four CIC-based MAs operating in parallel, and a 4-parallel feed-forward data preprocessor that provides data to the those four MAs.

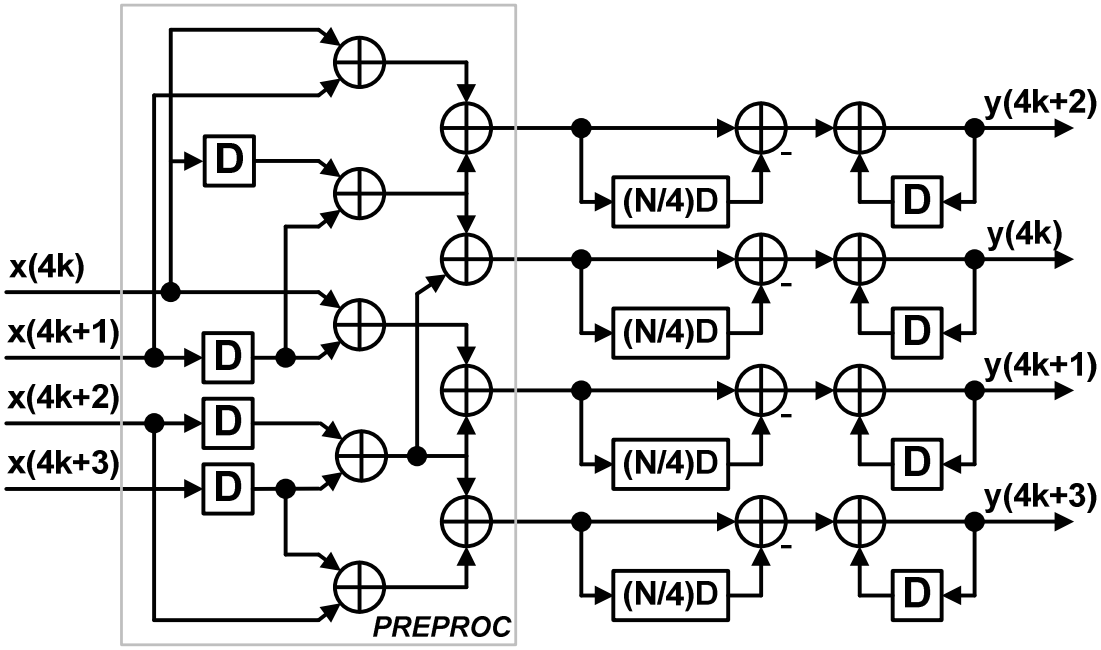


Figure 4.7 4-parallel MV with shortest (one adder) critical path (if pipeline is applied)

The architecture can be explained by the following example. Assuming the average number N equals to 8, the branch $y(4k+1)$ of the 4-parallel MA should generate the following summations/averages when k equals to 0, 1, and 2, respectively:

$$y(4k+1)|_{k=0} = x(-7)+x(-6)+x(-5)+x(-4)+x(-3)+x(-2)+x(-1)+x(0) \quad \text{(4-6)}$$

$$y(4k+1)|_{k=1} = x(-3)+x(-2)+x(-1)+x(0)+x(1)+x(2)+x(3)+x(4) \quad \text{(4-7)}$$

$$y(4k+1)|_{k=2} = x(1)+x(2)+x(3)+x(4)+x(5)+x(6)+x(7)+x(8) \quad \text{(4-8)}$$

It is observed from Equation (4-7) that $\{x(-3), x(-2), x(-1), x(0)\}$ is a block-delay version of $\{x(1), x(2), x(3), x(4)\}$ with four delays on each element, and from Equations (4-6)-(4-8) that the block $\{x(-3), x(-2), x(-1), x(0)\}$ is excluded after two ($2 = 8/4 = N/4$) clock cycles. Therefore, a CIC-based MA with two delays on the feed-

forward path can be utilized. Moreover, since $x(-3)$, $x(-2)$ and $x(-1)$ are the delay versions of $x(1)$, $x(2)$, and $x(3)$, respectively, the branch $y(4k+1)$ can be expressed as:

$$\begin{aligned} y(4k+1) &= D(x(4k+1)) + D(x(4k+2)) + D(x(4k+3)) \\ &+ x(4k) + x(4k+1) + x(4k+2) + x(4k+3) \end{aligned} \quad \text{(4-9)}$$

,where D stands for the delay. Similar derivations apply on the other three branches.

4.3 Carrier Synchronizer

The cross-correlation unit used for detecting the packet can be reused for estimating the carrier frequency offset. Equations (4-10)-

(4-14) describe this estimation algorithm.

$$y_n = s_n \exp(j2\pi f_{tx} n T_s) \quad \text{(4-10)}$$

$$\begin{aligned} r_n &= y_n \exp(-j2\pi f_{rx} n T_s) \\ &= s_n \exp[j2\pi(f_{tx} - f_{rx}) n T_s] = s_n \exp(j2\pi \Delta f n T_s) \end{aligned} \quad \text{(4-11)}$$

$$z = \sum_{n=0}^{L-1} r_n r_{n+D}^* \quad \text{(4-12)}$$

$$\begin{aligned} &= \sum_{n=0}^{L-1} s_n \exp(j2\pi f_\Delta n T_s)(s_{n+D} \exp(j2\pi \Delta f_\Delta (n+D) T_s))^* \\ &= \sum_{n=0}^{L-1} s_n s_{n+D}^* \exp(j2\pi f_\Delta n T_s)(s_{n+D} \exp(j2\pi \Delta f_\Delta (n+D) T_s))^* \\ &= \exp(j2\pi f_\Delta D T_s) \sum_{n=0}^{L=1} |S_n|^2 \end{aligned} \quad \text{(4-13)}$$

$$f_\Delta = \frac{-1}{2\pi D T_s} \angle z \quad \text{(4-14)}$$

Figure 4.8 shows the single-stream architecture for realizing this algorithm. This architecture reuses the cross-correlation unit of the (single-stream) packet detector shown in Figure 4.3. In addition, the single-stream architectures of the CORDIC-based arctangent calculator (ATAN) and the conventional direct-digital-frequency-synthesizer (DDFS) with phase adjustment are shown in Figure 4.9 and Figure 4.10, respectively.

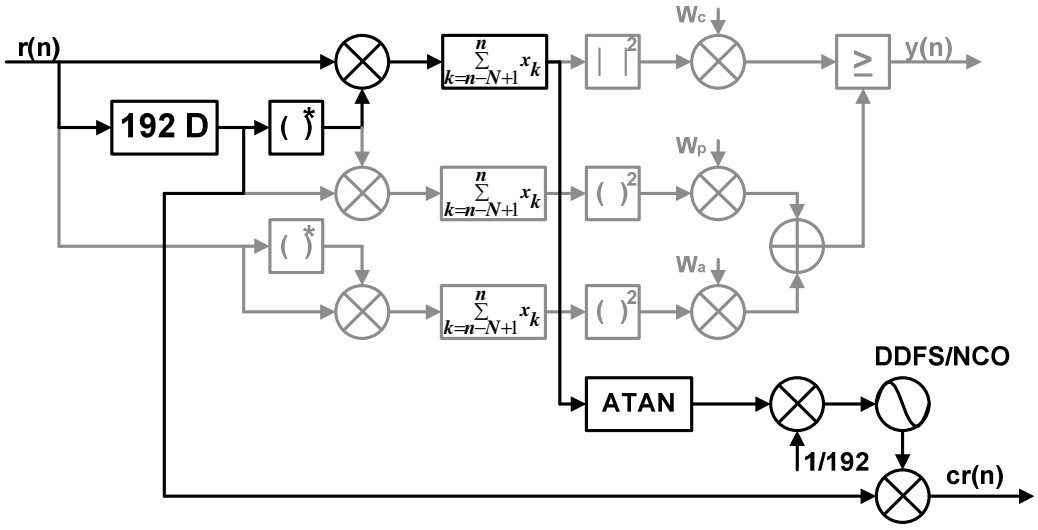


Figure 4.8 Single-stream architecture reusing packet detector to realize carrier frequency offset estimation.

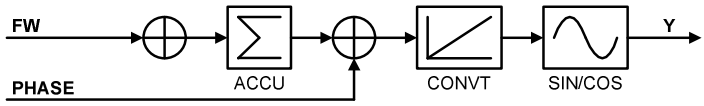


Figure 4.9 Single-stream architecture of direct-digital frequency synthesizer.

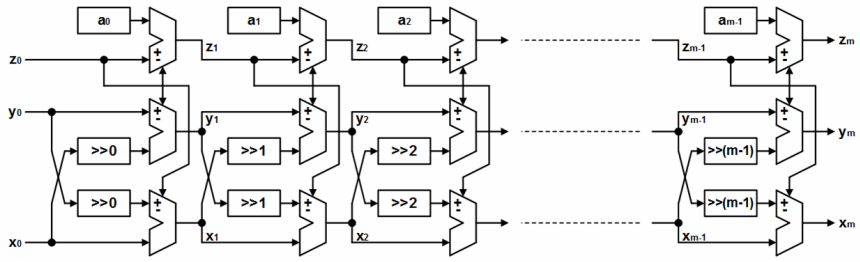


Figure 4.10 Single-stream architecture of CORDIC-based arctangent calculator

It can be seen from Figure 4.10 that parallelizing the ATAN is straightforward since it is a feed-forward architecture. Moreover, utilizing four single-stream DDFS shown in Figure 4.9, and assigning proper frequency word (FW) and phase (PHASE) values to each of them can achieve a 4-parallel DDFS, which is shown in Figure 4.11. In this architecture, the frequency word– $\boldsymbol{FW}_4$ is four times of the frequency word ($\boldsymbol{FW}$) used in the single-stream architecture. In addition, the phase adjustment for $\boldsymbol{y}(4\boldsymbol{k})$ is zero, and the phase adjustments for $\boldsymbol{y}(4\boldsymbol{k}+1)$, $\boldsymbol{y}(4\boldsymbol{k}+2)$, and $\boldsymbol{y}(4\boldsymbol{k}+3)$ are $0.25\boldsymbol{FW}$, $0.5\boldsymbol{FW}$, and $0.75\boldsymbol{FW}$, respectively. These three phase adjustments are frequency (word) modulated.

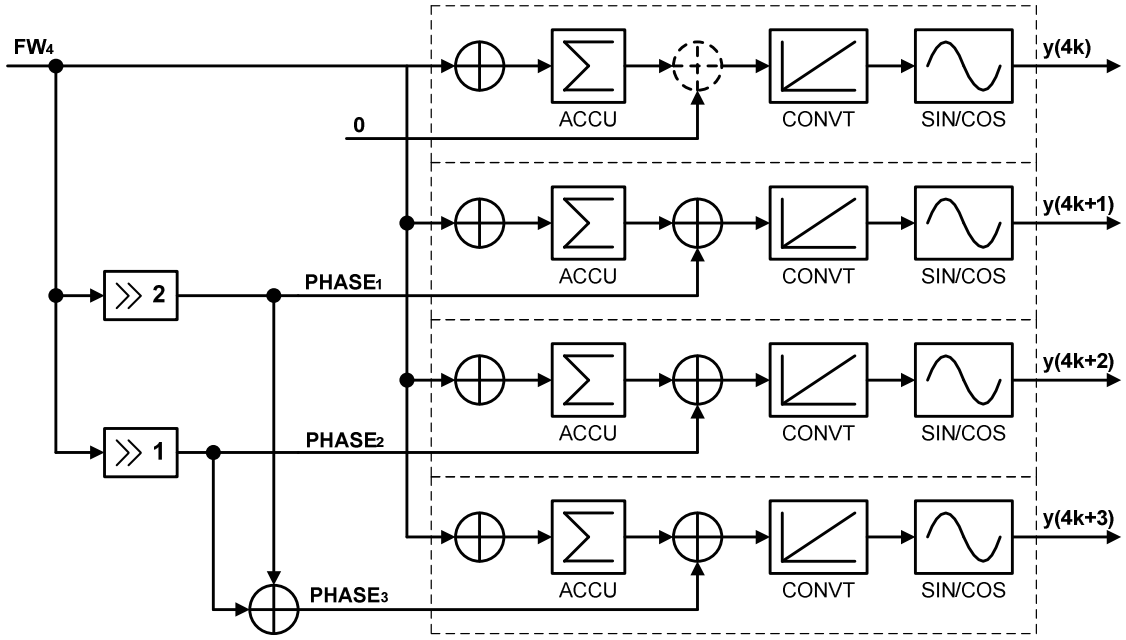


Figure 4.11 4-parallel direct-digital-frequency-synthesizer.

Since the 4-parallel architectures of the MA, ATAN, and DDFS are all available, the 4-parallel architecture of the carrier frequency synchronizer can be achieved. Figure 4.12 illustrates this architecture.

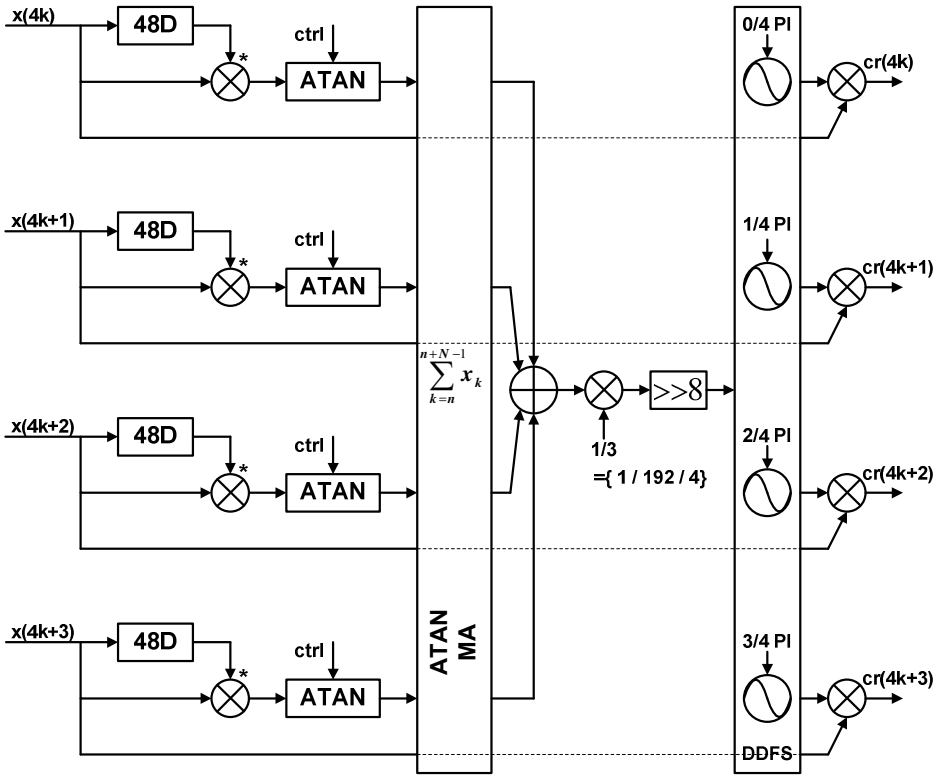


Figure 4.12 4-parallel architecture of carrier frequency synchronizer.

4.4 Half-Band Filter

As shown in Figure 4.2, the output of the carrier synchronizer is up-sampled by a factor of two through a half-band filter (HBF). Figure 4.13 shows the single-stream architecture of a half-band filter [34]. This architecture consists of a finite-impulse-response filter (FIR) and a delay line. The length of the delay line is half of the FIR length. This architecture can be parallelized straightforwardly because of its feed-forward nature. Figure 4.14 shows the parallel architecture of the half-band filter, which has four parallel inputs and eight parallel outputs. At the operation clock rate of 660 MHz, these 8-parallel outputs constitute a 5.28 GS/s throughput, which is equivalent to 3 sample/symbol. Therefore, the outputs of this parallel HBF outputs can be regarded as the carrier-synchronized received signal samples with 3x over-sampling ratio (OSR).

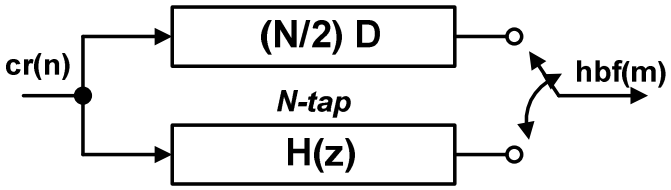


Figure 4.13 Single-stream architecture of half-band filter.

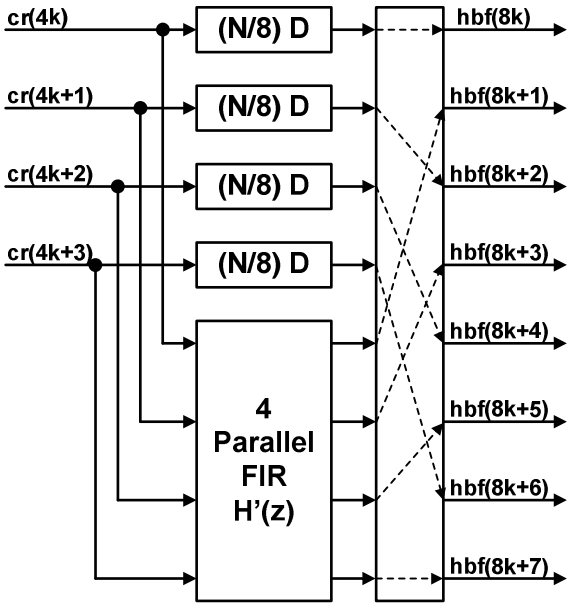


Figure 4.14 4-parallel architecture of half-band filter.

The 4-parallel FIR architecture based on the Iterated Short Convolution (ISA) algorithm [35] is adopted in this parallel HBF. In this architecture, nine single-stream FIRs are constructed from various combinations of four elementary single-stream FIRs: $\boldsymbol{H}_0$, $\boldsymbol{H}_1$, $\boldsymbol{H}_2$, and $\boldsymbol{H}_3$, which are the four-way polyphase partition of the original / prototype FIR ($\boldsymbol{H}(z)$) of the (single-stream) HBF shown in Figure 4.13. In addition, two adder trees/networks are respectively inserted in the front and back of these nine single-stream FIRs.

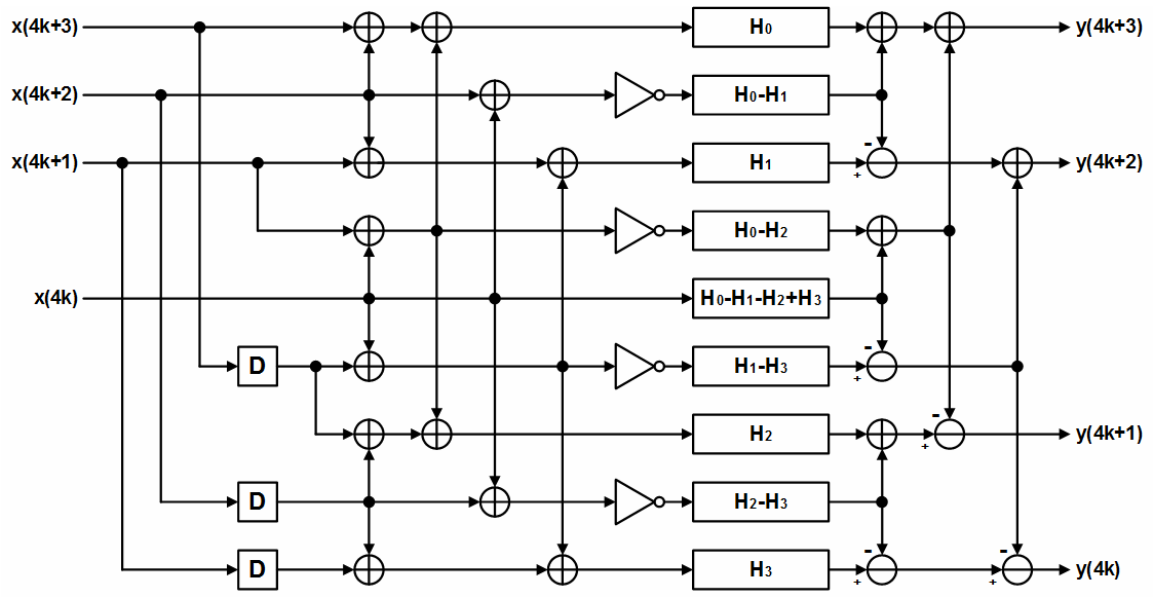


Figure 4.15 4-parallel FIR based on iterated short convolution algorithm.

4.5 Timing Synchronizer

Figure 4.16 shows the architecture of the parallel (data-aided) timing synchronizer. This timing synchronizer consists of a 1-to-4 8-parallel polyphase match filter, a 1-to-3 8-parallel de-multiplexer, a 4-parallel Golay correlator, and a path selector. The path selector chooses one of the four 8-parallel sub-filters (e.g. the sub-filter with coefficients $\boldsymbol{h}_0$, $\boldsymbol{h}_4$, $\boldsymbol{h}_8$, … $\boldsymbol{h}_{4k}$) of the polyphase match filter. Those chosen sub-filter performs the match filtering on the output of the parallel HBP at 660 MHz clock rate. Therefore, the output of the chosen sub-filter can be regarded as the received signal samples that are empowered by match filtering but with a timing delay relative to the prototype (non-polyphase) match filter operating at 5.28 GS/s ($3\boldsymbol{F}_{sym}$) symbol sampling rate. This delay equals $\boldsymbol{M}\times 47.35$ ps ($\boldsymbol{M}/4/(3\boldsymbol{F}_{sym})$) where $\boldsymbol{M}$ ranges from 0 to 3.

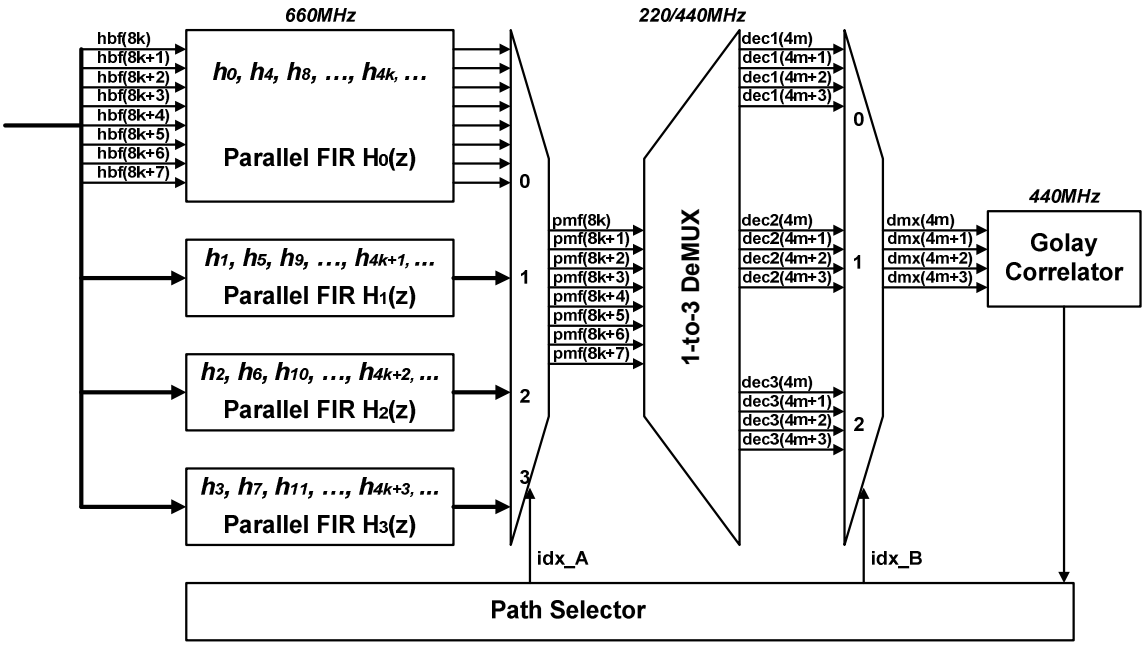


Figure 4.16 Architecture of parallel data-aided timing synchronizer using polyphase match filter.

The de-multiplexer splits the output of the chosen sub-filter into three data streams, each of which has a 4-parallel output, and operates at 440 MHz clock rate. Therefore, the output of each data stream can be regarded as the received signal samples that are empowered by the matching filtering, and sampled at the symbol rate (1760 GS/s = 4×440 MS/s) with a timing delay relative to the prototype (non-polyphase) match filter operating at 1.76GS/s. This timing delay equals to $N \times 47.35$ ps ($N/12/F_{sym}$) where N ranges from 0 to 11.

The path selector chooses one de-multiplexer output streams. The 4-parallel Golay correlator correlates the output of the chosen de-multiplexer stream with the G_{128a} code for a period of 6.82 ns ($128/F_{sym}$), and generates the maximum correlation value after this period. This maximum value and the path index are stored by the path selector. There are totally 12 (4×3) path combinations formed by the 1-to-4 polyphase match filter and

the 1-to-3 de-multiplexer. The path selector selects one path combination in a round-robin scheduling manner every 6.82 ns until it collects 12 maximum correlation values and 12 path indexes.

The path selector has enough time to select all (12) paths within the SYNC field, which has 14 repetitions of G_{128a} because the tasks of packet detection and the carrier recovery are expected to finish within the duration of the first two repetitions of G_{128a} in the SYNC field. In the set of 12 maximum correlation values, the path selector further finds the largest one, identifies the corresponding path index as well as selects the corresponding sub-filter and the corresponding output stream of the de-multiplexer. The output of the identified path can be regarded as the received signal samples with timing synchronization since these samples most resemble the G_{128a} code when they are compared with those provided by other paths. The conducted simulation shows that this timing delay granularity, which equals to 47.35 ps ($1/12/\boldsymbol{F}_{sym}$), of the outputs provided by these 12 paths is enough for the synchronizer to supply the synchronized samples/symbols that the SC-FDE can use to equalize and demodulate under 16-QAM modulation for various channel conditions of IEEE 802.15.3c [11].

4.5 De-Multiplexer

Figure 4.17 shows the 1-to-3 parallel de-multiplexer of the timing synchronizer. The de-multiplexer uses three 8-parallel decimators to de-multiplex the 8-parallel output that is provided by one of the 8-parallel sub-filters at 660 MHz clock rate into three sets of 8-parallel output streams, each set running at 220MHz. The 8-parallel decimator output streams are further multiplexed by a factor of two, providing 4 parallel output streams at 440MHz. Each decimator has its own signal routing table to forward the decimated samples to the proper output positions.

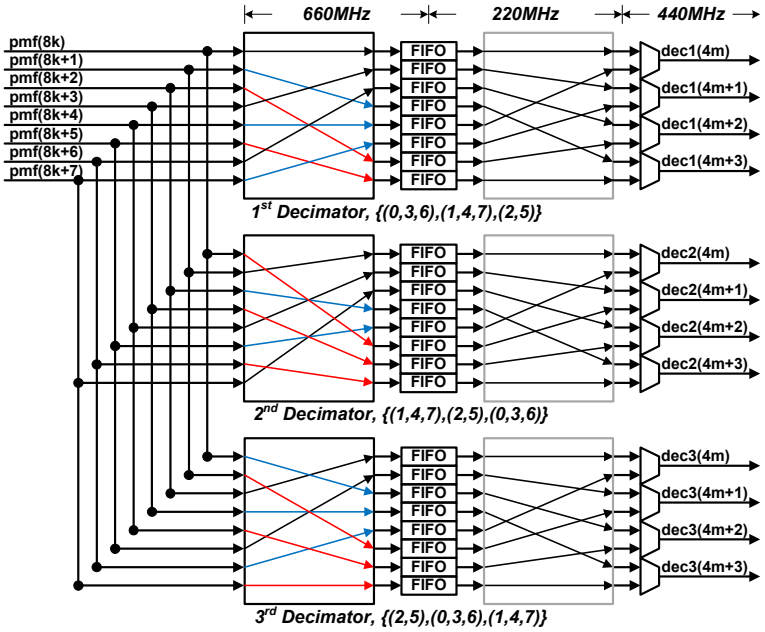


Figure 4.17 Architecture of 1-to-3 8-parallel de-multiplexer

The timing diagram shown in Figure 4.18 illustrates the signal routing in the 1st (top) routing table. Given 24 (8×3) input samples every three cycles of a 660 MHz clock, the decimator generates 8 samples by eliminating two samples whenever it receives three samples. At the 1st clock cycle of the 220 MHz clock,

The generated 8 samples are as follows:

{pmf(8k),pmf(8k+3),pmf(8k+6)}, at the 1st cycle

{pmf(8k+1),pmf(8k+4),pmf(8k+7)}, at the 2nd cycle

{pmf(8k+2),pmf(8k+5)}, at the 3rd cycle

The next 8 samples in the following three cycles of a 660MHz clock will repeat the same pattern. Therefore, we can build the following time-dependent signal routing table:

$$\{(0,3,6),(1,4,7),(2,5)\} \Rightarrow \{0,1,2,3,4,5,6,7\} \quad \textbf{(4-15)}$$

for the 1st decimator. Similar routing table derivations apply on the other two decimators, which have one and two initial sample offsets relative to the 1st decimator, respectively.

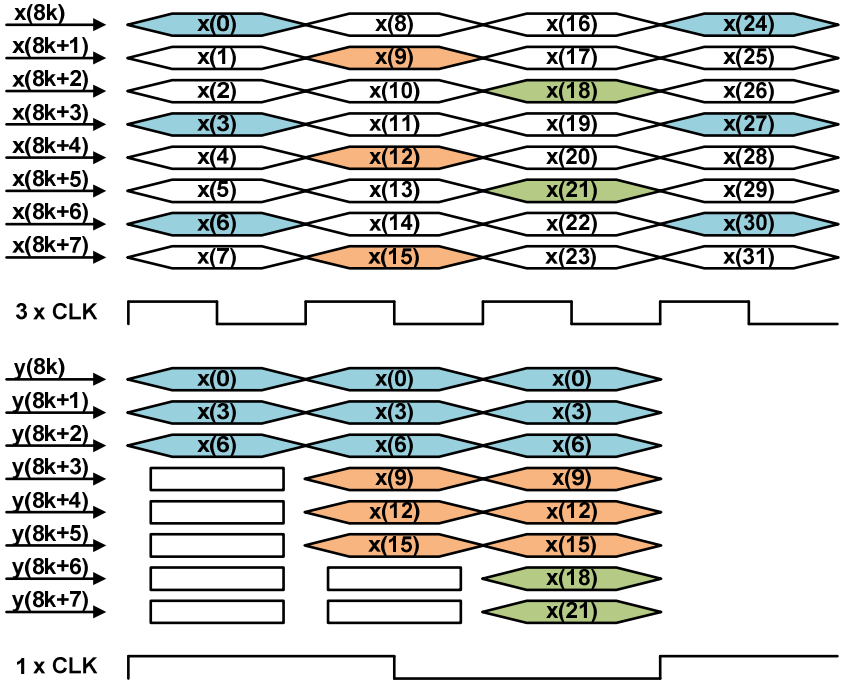


Figure 4.18 Timing diagram for the 1st (top) routing table of 1-to-3 8 parallel de-multiplexer

4.6 Golay Correlator

The 4-parallel Golay correlator will be described in 5.2.2 in Chapter 5. The high-accuracy channel estimator presented in Chapter 5 needs this Golay correlator as well.

Chapter 5

High-Accuracy Channel Estimator

As described in Chapter 3, the interferences at the boundaries of the channel responses to adjacent channel estimation sequences (CESs) result in the performance degradation of an IEEE 802.11ac-compliacnt equalizer. In this chapter, we present a high-accuracy (a.k.a. bi-sectional) channel estimator that can de-couple the interferences between successively received CESs, and reconstruct the interference-free CES responses. This channel estimator can generate more accurate channel estimation to reduce the equalizer's bit error rate (BER) (so as to decrease its error-vector-magnitude (EVM) values) regardless of its type. It can also be easily migrated to support 802.11ad owing to the similarity of the packet structures defined in these two standards.

5.1 Bi-Sectional Channel Estimation Algorithm

Figure 5.1 redraws the preamble structure of IEEE 802.15.3c, which is shown in Figure 3.5. The preamble consists of five CESs–G_{256a}, G_{256b}, G_{256a}, G_{256b}, and G_{128b}.

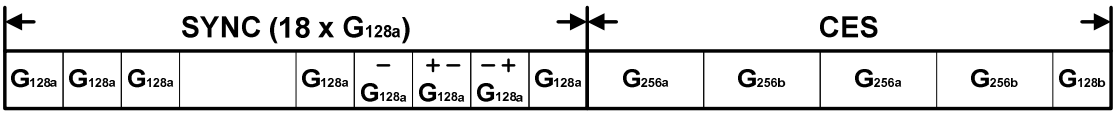


Figure 5.1 Preamble structure of IEEE 802.15.3c. (Redrawing of Figure 3.5)

The 802.15.3c standard [2] and Golay-code theory [26][27] indicate that G_{256a} and G_{256b} are constructed from G_{128a} and G_{128b}, which are a pair of Golay complementary codes (GCC). Furthermore, G_{256a} and G_{256b} are equivalent to [G_{128b}, G_{128a}] and [–G_{128b},

G_{128a}], respectively. As aforementioned in Chapter 3, G_{128a} and G_{128b} are a pair of GCC as well.

Figure 5.2 illustrates the channel responses as the SYNC pattern (G_{128a}) and the first CES ($G_{256a} = [G_{128b}, G_{128a}]$) are transmitted via a communication channel, whose impulse response (IR) has pre and post-cursors. The total channel response to G_{128a} is a superposition of the pre and post-cursor channel responses to G_{128a}: Y_{a_pre} and Y_{a_post}, respectively. Assuming that the lengths of the pre and post-cursors are N_{pre} and N_{post}, respectively, Y_{a_pre} will start at time zero (reference), and stop at time $N_{pre} + 126$; meanwhile Y_{a_post} will start at the time N_{pre}, and stop at the time $N_{pre} + N_{post} + 126$. Furthermore, the superposition of Y_{a_pre} and Y_{a_post} can be partitioned into three consecutive sections: x_a (head), y_a (body), and z_a (tail), of which the lengths are N_{pre}, 128, and $N_{post} - 1$, respectively. We can segment sections x_b, y_b, and z_b similarly for the total channel response to G_{128b} of the first CES.

Moreover, y_b starts at the same time as the aforementioned z_a. Assuming there is no noise in the packet transmission and reception, G_{128a} of the first CES will have the same total channel response as the aforementioned SYNC pattern (G_{128a}), and the response starts at the time 256. Furthermore, its head section (x_a) ends at the same time as the body section (y_b) for the preceding G_{128b}.

Consequently, the frame that has 128 symbols starting from the time $N_{pre} + 128$, is superimposed by z_a, y_b, and x_a, which come from channel responses to the SYNC pattern (G_{128a}) and the complementary codes (G_{128b}, G_{128a}) of the first CES. This frame is obtained through the existing frame synchronization approach [8][9]. This approach will generate a peak at the time $N_{pre} + 127$ for the channel whose pre-cursor length is N_{pre} if it

uses the SYNC pattern (G_{128a}) to correlate the incoming signal for finding the frame boundary.

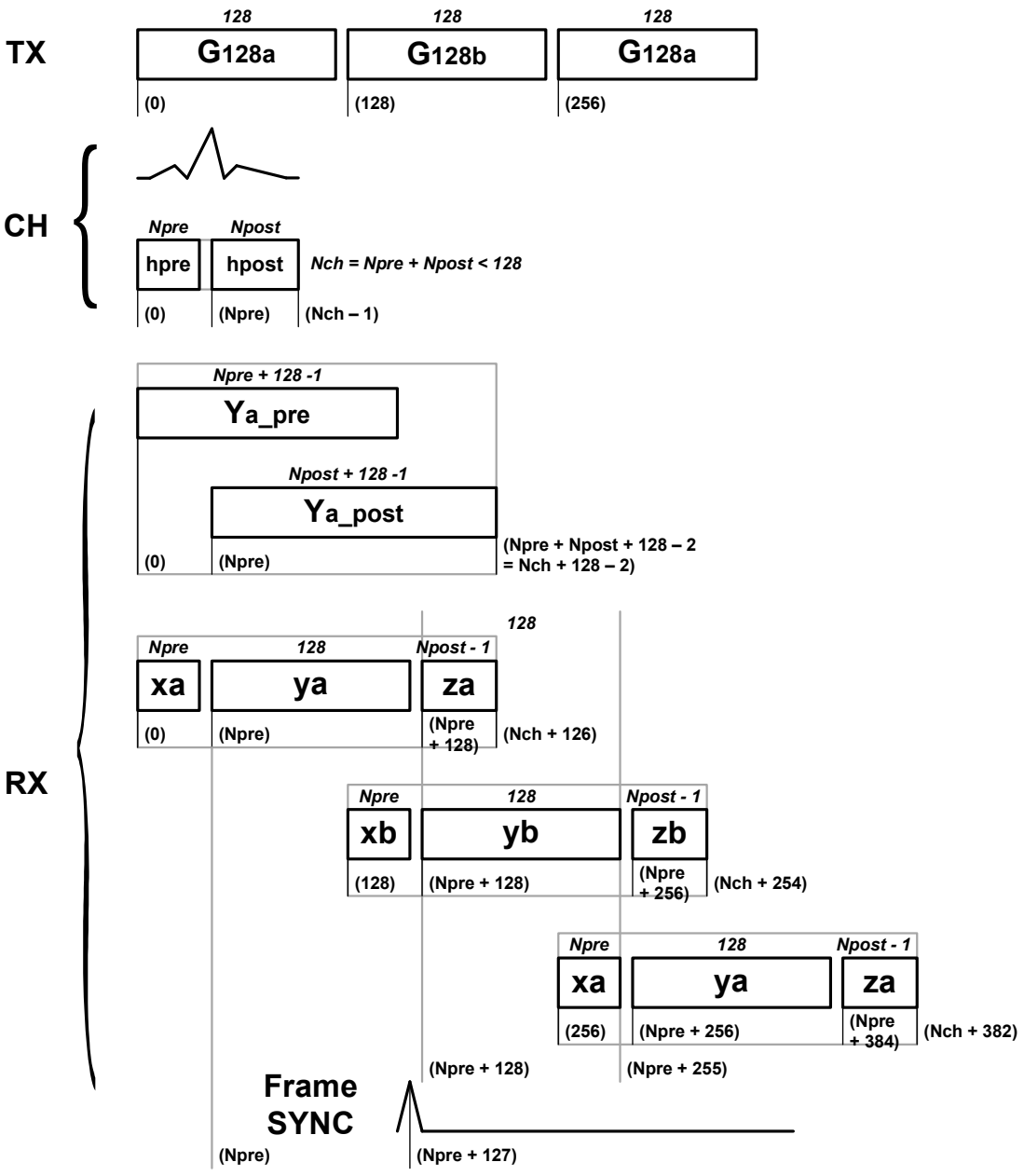


Figure 5.2 Channel response details within a frame after frame synchronization.

As shown in Figure 5.3, multiple 128-symbol frames: y_1, y_2, …, y_8, can be obtained after the frame synchronization to estimate the channel responses to the CESs G_{256a}, G_{256b},

G_{256a}, and G_{256b} of a transmitted preamble. Each frame is a superposition of head, body and tail sections coming from channel responses to three consecutive 128-symbol Golay codes. The body section can be viewed as a 128-element vector, and the superposition of head and tail sections can be viewed as another 128-element vector, in which the tail and head sections would occupy the front and back portions and then with a few zeros residing in between them.

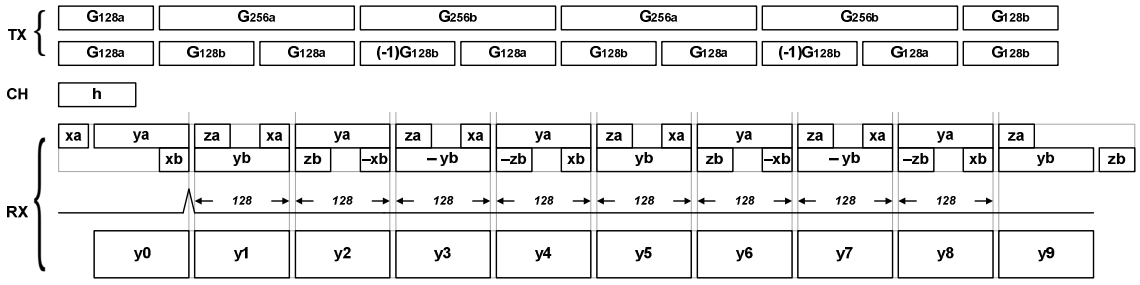


Figure 5.3 Multiple received frames corresponding to successively transmitted CESs.

Therefore, as shown in Figure 5.4, four vector equations are formulated for the frames y1 to y4. Four unknown vectors: ya, yb, [za, 0, xa], and [zb, 0, –xb] can be solved through element-wise addition, negation, and division-by-2, which equals to right-shift-1. As a result, the contents of "two" vectors ya and [za, 0, xa] (or yb and [zb, 0, –xb]) can fully determine the total channel response to CES G128a (or G128b), which also leads to the naming of our proposed algorithm–"Bi-Sectional".

Additionally, Figure 5.4 depicts that inserting ya in between two [za, 0, xa], and inserting yb in between [–zb, 0, xb] and [zb, 0, –xb] result in two 384-element vectors, in which the true channel responses–[xa, ya, za] and [xb, yb, zb]–to G128a and G128b can be extracted as well. Further summing the correlation result of [xa, ya, za] and G128a and that of [xb, yb, zb] and G128b results in the CIR.

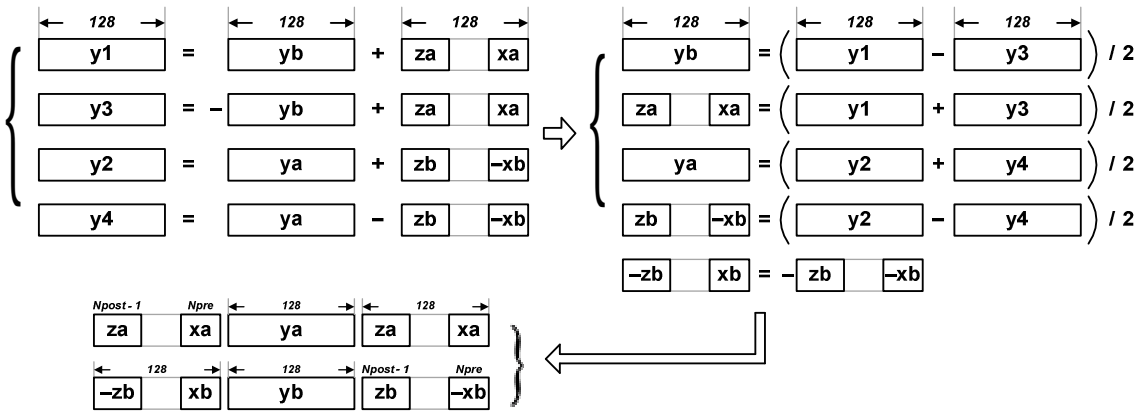


Figure 5.4 Vector equations for calculating the two vectors (sections) required for obtaining a complete channel response

5.2 Bi-Sectional Channel Estimation Hardware Architecture

Figure 5.5 shows the block diagram of the proposed bi-sectional channel estimator to realize the aforementioned algorithm. The 4-parallel hardware architecture allows the channel estimator to achieve a symbol rate of 1.76GS/s defined in 802.15.3c while operating at the clock rate 440MHz. The estimator uses the 4-parallel FIFOs (FIFO1 and FIFO2) with built-in access controls initiated by the frame synchronization as well as the 4-parallel butterfly units (BF1 and BF2) to solve the four vector equations, and utilizes the 4-parallel extractors (EXTA and EXTB), which comprise of controllers, multiplexers and additional FIFOs, to perform vector concatenation and extraction. The vector generated by EXTB is delayed and multiplexed with the one generated by EXTA. Therefore, only one 4-parallel Golay-128 correlator is required to process these two vectors (true channel responses). Finally, 128 registers (32 registers in each parallel unit) are used to align the two outputs of the correlator, and the aligned outputs are combined by the following adders to generate the channel estimation.

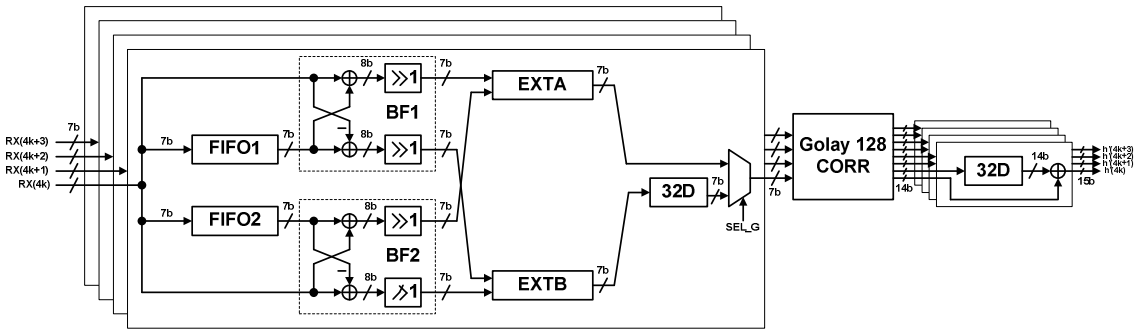


Figure 5.5 Hardware architecture of bi-sectional channel estimator

5.2.1 Butterfly Unit

Figure 5.6 illustrates the procedure of computing each element of the vectors y_a, [z_a, 0, x_a], y_b, and [$-z_b$, 0, x_b] (in a single-stream manner). Starting at time zero (reference) right after the frame synchronization, the channel estimator sequentially pushes 128 incoming samples that constitute the frame y_1 into FIFO1. The same operation is performed for the frame y_2 in FIFO2. When the first sample of the frame y_3 arrives, the channel estimator starts fetching out the samples stored in FIFO1. The BF1 computes the sum and difference of each fetched sample and each incoming sample, and divides each result by 2 through the 1-bit right-shifters. These operations leads to the vectors [z_a, 0, x_a] and y_b, For example, at the time 256, $z_a(0)$ and $y_b(0)$ equal $[y_1(0) + y_3(0)] / 2$ and $[y_1(0) – y_3(0)] / 2$, respectively. The BF2 operates similarly to compute the vectors y_a and [$-z_b$, 0, x_b] when the frame y_4 starts arriving. Apparently, z_a, x_a, and y_a are generated sequentially; meanwhile y_b, $-z_b$, and x_b are generated sequentially.

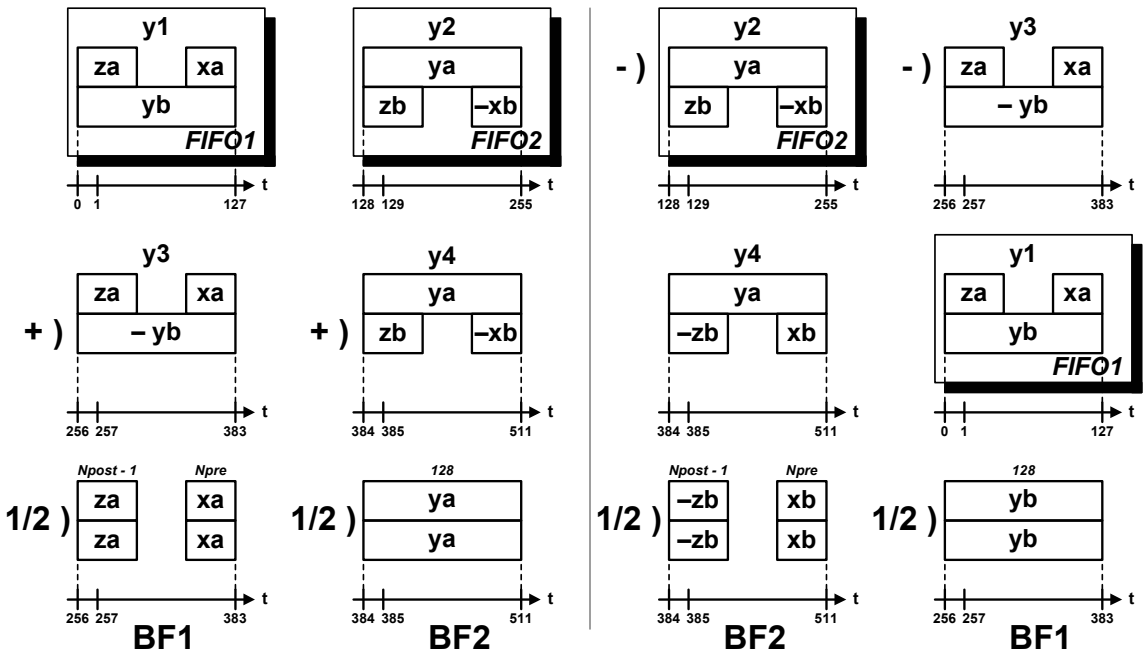


Figure 5.6 Vector generation of {ya, [za, 0, xa]} (left) and {yb, [-zb, 0, xb]} (right)

5.2.2 Extractor

The computed vector elements are re–arranged by the extractors EXTA and EXTB to generate the true channel responses–[x_a, y_a, z_a] and [x_b, y_b, z_b]–to G_{128a} and G_{128b}. Figure 5.7-(a) and Figure 5.7-(b) show the single-stream architectures of EXTA and EXTB in each parallel unit. The extractors use FIFOs and multiplexers to schedule the delivery for the vector elements. Using [x_a, y_a, z_a] as an example, Figure 5.6 shows that the upper butterfly generates z_a, x_a and y_a in sequence instead of x_a, y_a and y_a. Therefore, the upper extractor shown in Figure 5.7–(a) uses a FIFO to store z_a, and fetches that after the delivery of x_a and z_a.

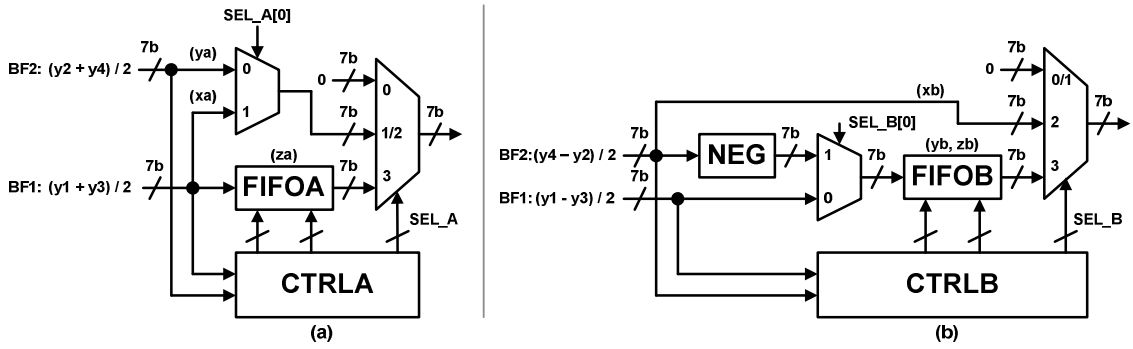


Figure 5.7 Hardware architecture of EXTA (a) and EXTB (b)

The upper extractor lets the truncated outputs of the upper butterfly ($(y_1+y_3)/2$) pass through its last–stage multiplexer when it detects the start of x_a. The post-cursor and pre-cursor length estimator shown respectively in Figure 5.8–(a) and Figure 5.8-(b) realize this detection. Each estimator has two counters. When the pre-cursor estimator starts, its 1st counter (CNT_0) starts incrementing. In addition, the magnitude of the truncated outputs of the upper butterfly ($(y_1+y_3)/2$) is computed and compared with a threshold value (TH_MAG), which is set to very close to zero. Once the magnitude is below to this threshold value, the 2nd counter (CNT_1) of the post-cursor estimator starts incrementing. This output value of this counter is compared with another threshold value (TH_CNT_POST). Once it exceeds this threshold value, both counters CNT_0 and CNT_1 stops incrementing. This exceeding indicates the diminishing of z_a; therefore the output value of CNT_0 is used to estimate Npost, the post–cursor length of the channel impulse response. This exceeding also enables the 1st counter (CNT_2) of the pre–cursor length estimator to start counting. This estimator has a similar hardware architecture to that of the post–cursor length estimator. The pre-cursor length estimator tries to detect the increasing of x_a by checking whether the magnitude exceeds the near–zero threshold (TH_MAG) for a while. Figure 5.9 illustrates this detection process.

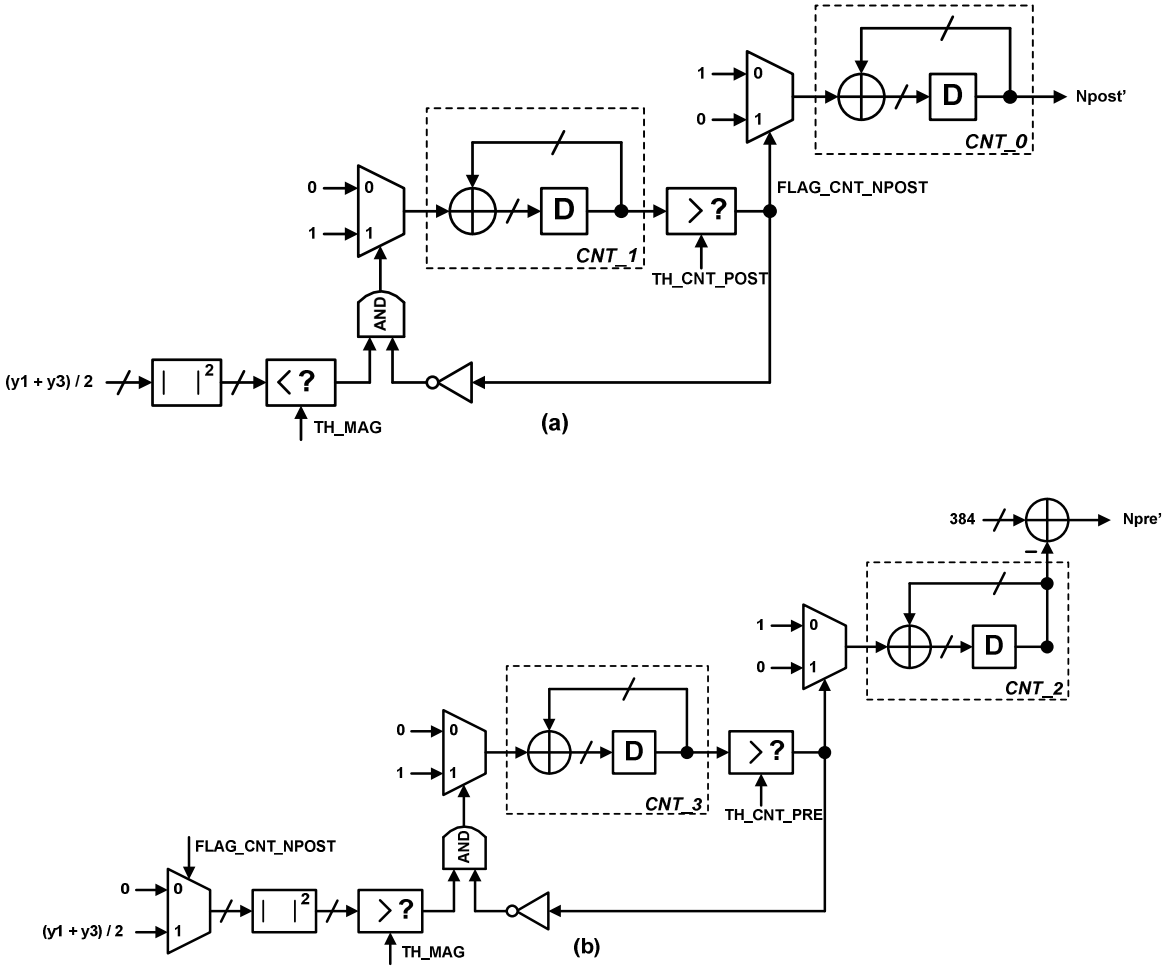


Figure 5.8 (a) Post–cursor length estimator; (b) Pre–cursor length estimator

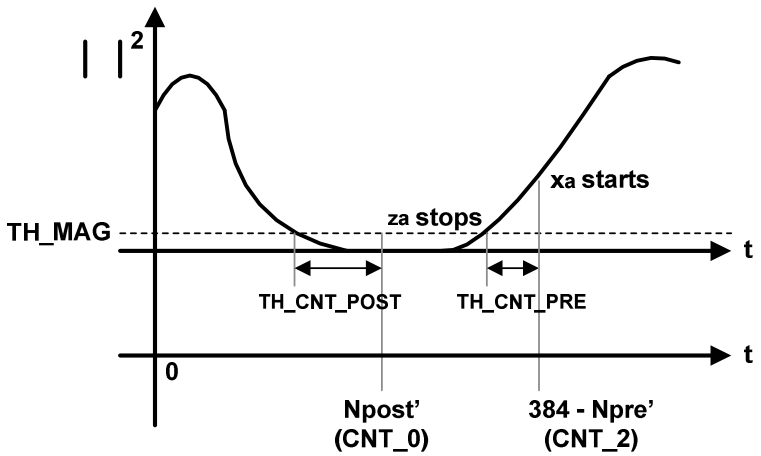


Figure 5.9 Detection of x_a through post and pre–cursor estimators

5.2.2 Golay Correlator

Figure 5.10 shows the generic hardware architecture of a fast Golay correlator proposed in [27]. It has k stages, and each stage has a butterfly unit, a weighting unit (W_i), and a delay unit (D_i), where W_i is either +1 or -1, and D_i has a power of two delays. This correlator can generate the correlation value of the incoming signal $r(n)$ and the "Part a" of a GCC, and the correlation value of the incoming signal $r(n)$ and the "Part b" of a GCC. $r_a(n)$ and $r_b(n)$ denote these two correlation values, respectively. Furthermore, the length of the "Part a" ("Part b") of the GCC is 2^k. Equations (5-1) and (5-2) show the values of W_i and D_i enabling the correlator to correlate the incoming signal with the G128a and G128b defined in IEEE 802.15.3c.

$$\{W_1, W_2, W_3, W_4, W_5, W_6, W_7\} = \{-1, 1, 1, 1, 1, 1, 1\} \quad (5\text{-}1)$$

$$\{D_1, D_2, D_3, D_4, D_5, D_6, D_7\} = \{64, 32, 8, 2, 16, 1, 4\} \quad (5\text{-}2)$$

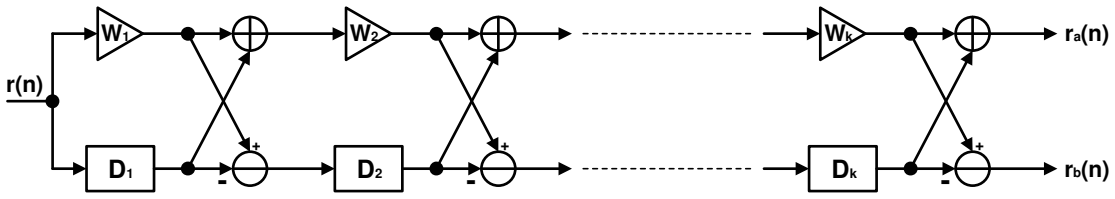


Figure 5.10 Generic single-stream architecture of fast Golay correlator.

The architecture shown in Figure 5.10 can be parallelized without increasing the critical path length because of the feed-forward nature of this architecture. Figure 5.11 generalize the 4-parallel architectures of Stages 1, 2, 3, 5, and 7. In this generic

architecture, the amount of the delay in each parallel unit equals to the amount of the original stage delay (D_i) divided by 4. However, for Stages 4 and 6, their respective D_i divided by 4 are fractional numbers (1/2 and 1/4) fractional number. Therefore, special wirings are requires for their respective 4-parallel architectures, which are shown in

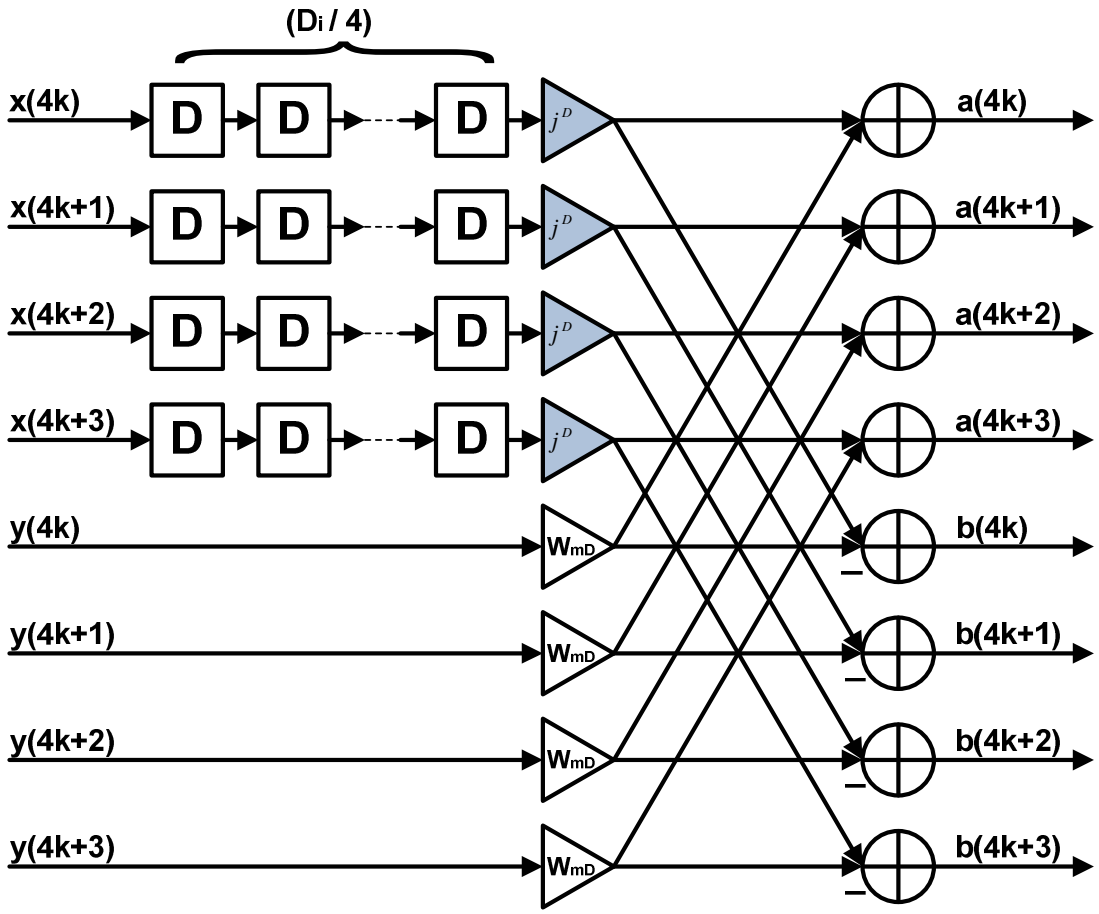


Figure 5.11 4-parallel architecture of single-stream Golay correlator stages with 64, 32, 16, 8, or 4 delays.

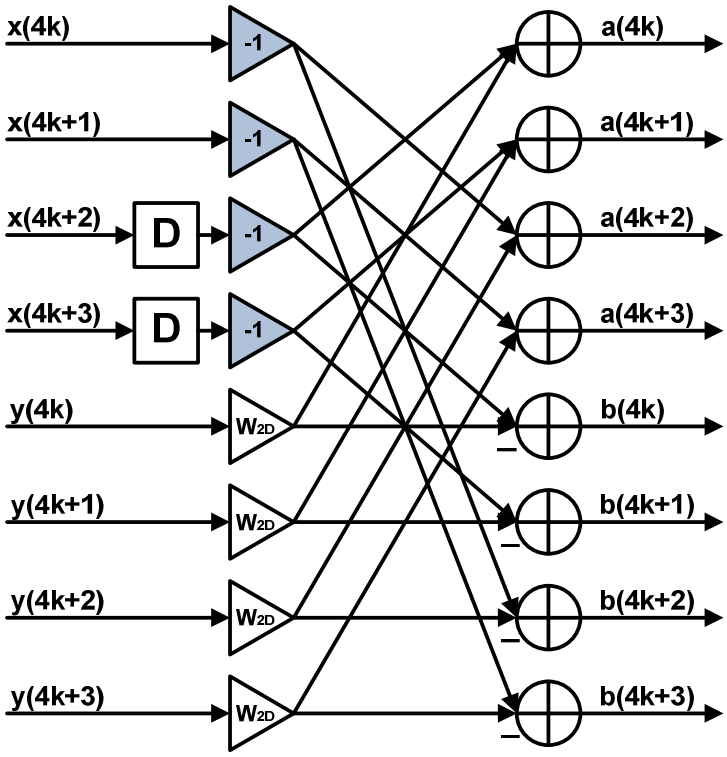


Figure 5.12 4-parallel architecture of single-stream Golay correlator stage with 2 delays.

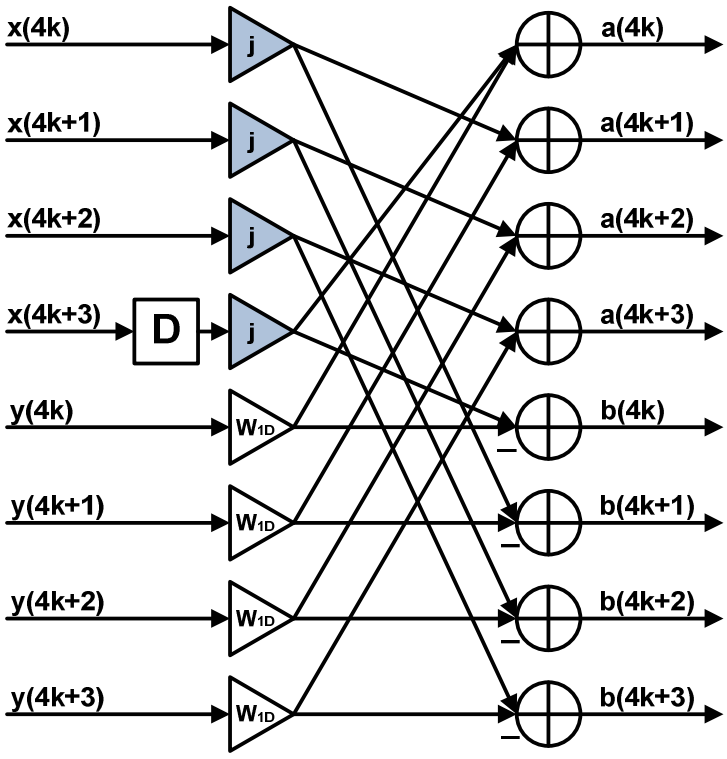


Figure 5.13 4-parallel architecture of single-stream Golay correlator stage with 1 delay.

5.2.3 MMSE Frequency-Domain Equalizer

A single-carrier minimum-mean-square-error frequency domain equalizer (SC-MMSE-FDE) [28] is designed together with the bi-sectional channel estimator to validate the performance improvement contributed by this channel estimator. Figure 5.14 depicts the architecture of this FDE. It adopts the 4-parallel hardware architecture to accommodate the speed constraints of the 65nm CMOS implementation. Given a clock rate at 440 MHz, this FDE can achieve 1.76 GS/s throughput required by IEEE 802.15.3c. This FDE consists of a 4-parallel 512-pt FFT, a 4-paralle 512-pt IFFT, a 4-paralle MMSE equalizer (EQ), a 4-paralle channel estimator (CH-EST), and a controller (CTRL).

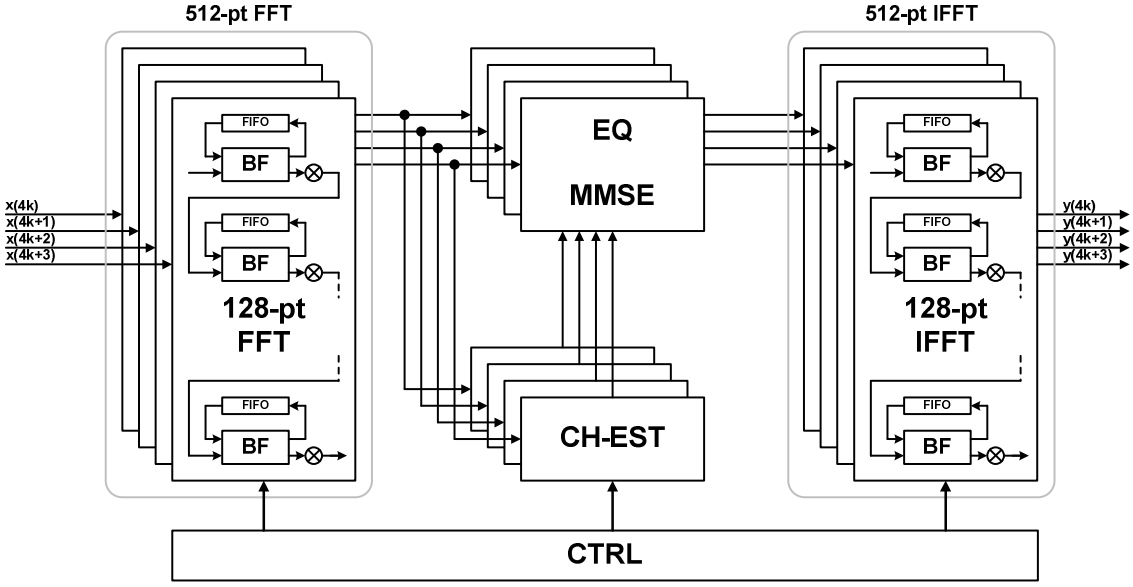


Figure 5.14 Architecture of 802.15.3c-complicant minimum-mean-square-error frequency domain equalizer.

Figure 5.15 shows the architecture of the 4-parallel 512-pt FFT. It consists of four identical single-stream (non-parallel) 128-pt FFTs, three twiddle-factor units, and a 4-pt FFT. Each of the three twiddle-factor units follows a 128-pt FFT, and the 4-pt FFT

combines the outputs of these three twiddle-factor units, and the output of the 128-pt FFT that is not followed by any twiddle-factor unit. Furthermore, each 128-pt FFT adopts the Radix-2 single delay feedback architecture [29].

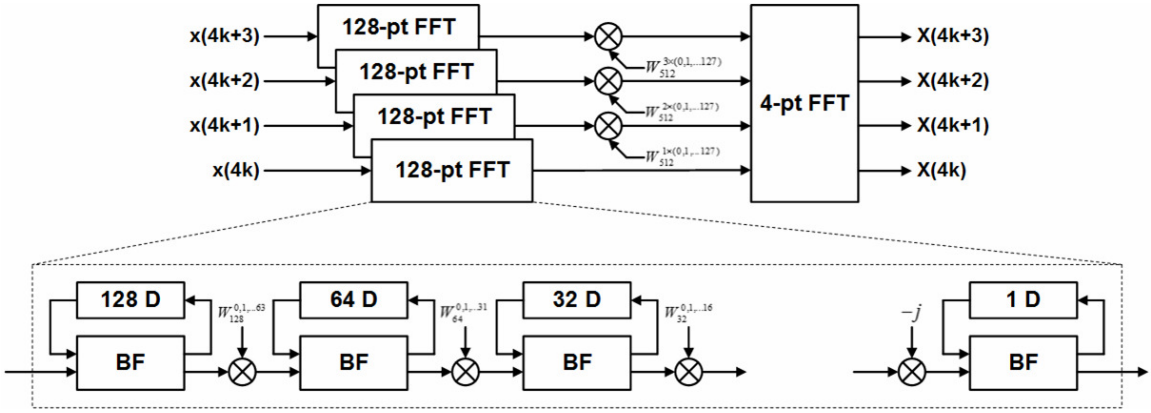


Figure 5.15 Architecture of 4-parallel 512-pt FFT.

The SC-MMSE-FDE is modeled mathematically in the following. Given a series of K received symbols and their corresponding K -pt FFT as described in Equations (5-3)-(5-5), a series of K MMSE equalized symbols is shown in Equation (5-6) and (5-7)., where $\hat{C}_{mmse}$ is the coefficients of the frequency domain gain and phase adjustments for MMSE equalization, $\hat{H}$ is the channel estimation, and $\hat{\eta}$ is the estimated signal to noise ratio (SNR).

$$y \equiv (y[0]\, y[1] \ldots\ldots y[K-1]\, y[K]) \qquad (5\text{-}3)$$

$$Y \equiv (Y[0]\, Y[1] \ldots\ldots Y[K-1]\, Y[K]) \qquad (5\text{-}4)$$

where

$$Y[k] \equiv \sum_{l=0}^{K-1} y[l] W_K^{kl}, W_K = e^{-j\left(\frac{2\pi}{K}\right)} \qquad (5\text{-}5)$$

$$\tilde{y}[k] \equiv \sum_{l=0}^{K-1} \hat{C}_{mmse} Y[l] W_K^{-kl}, W_K = e^{-j\left(\frac{2\pi}{K}\right)} \quad \textbf{(5-6)}$$

where

$$\hat{C}_{mmse}[k] = \frac{\hat{H}[k]^*}{\left|\hat{H}[k]\right|^2 + \hat{\eta}} \quad \textbf{(5-7)}$$

$$\hat{\eta} = \frac{P_s}{P_n} \quad \textbf{(5-8)}$$

As described previously, the preamble of IEEE 802.15.3c has two sets of [G_{256a}, G_{256b}]; therefore, two channel estimations: H_1 and H_2 (Equations (5-9) and (5-10)), can be obtained. The summation and difference of H_1 and H_2 can be defined as in Equations (5-11) and (5-12). They can lead to the average channel estimation and the estimated SNR.

$$H_2 \equiv (H[2,0] H[2,1] ..... H[2, K-1] H[2, K]) \quad \textbf{(5-9)}$$

$$H_2 \equiv (H[2,0] H[2,1] ..... H[2, K-1] H[2, K]) \quad \textbf{(5-10)}$$

$$H_{1+2} \equiv (\{H[1,0] + H[2,0]\}\{H[1,1] + H[2,1]\}....\{H[1, K] + H[2, K]\}) \quad \textbf{(5-11)}$$

$$H_{1-2} \equiv (\{H[1,0] - H[2,0]\}\{H[1,1] - H[2,1]\}....\{H[1, K] - H[2, K]\}) \quad \textbf{(5-12)}$$

Equation (5-13) defines the average channel estimation $\hat{H}$, which will be used to calculate the MMSE coefficient $\hat{C}_{mmse}$ shown in Equation (5-7). Moreover, Equations (5-14) and (5-15) define $\hat{W}_1$ and $\hat{W}_2$ and $\hat{H}$ –the difference between the average channel estimation and the 1st channel estimation, and the difference between the average

channel estimation and the 2nd channel estimation, respectively. $\hat{\boldsymbol{W}}_1$ and $\hat{\boldsymbol{W}}_2$ can be used as the estimated noise.

$$\hat{\boldsymbol{H}}[\boldsymbol{k}] = \frac{1}{2}\{\boldsymbol{H}[1,\boldsymbol{k}] + \boldsymbol{H}[2,\boldsymbol{k}]\} \quad \textbf{(5-13)}$$

$$\hat{\boldsymbol{W}}[1,\boldsymbol{k}] = \hat{\boldsymbol{H}}[\boldsymbol{k}] - \boldsymbol{H}[1,\boldsymbol{k}] = \frac{1}{2}\{\boldsymbol{H}[2,\boldsymbol{k}] - \boldsymbol{H}[1,\boldsymbol{k}]\} \quad \textbf{(5-14)}$$

$$\hat{\boldsymbol{W}}[2,\boldsymbol{k}] = \hat{\boldsymbol{H}}[\boldsymbol{k}] - \boldsymbol{H}[2,\boldsymbol{k}] = \frac{1}{2}\{\boldsymbol{H}[1,\boldsymbol{k}] - \boldsymbol{H}[2,\boldsymbol{k}]\} \quad \textbf{(5-15)}$$

Therefore, the signal power $\boldsymbol{P}_s$ and the noise power $\boldsymbol{P}_n$ can approximated as Equations (5-16) and (5-17).

$$\boldsymbol{P}_s = \frac{1}{\boldsymbol{K}}\sum_{\boldsymbol{k}=1}^{\boldsymbol{K}}\left|\hat{\boldsymbol{H}}[\boldsymbol{k}]\right|^2 = \frac{1}{\boldsymbol{K}}\times\sum_{\boldsymbol{k}=1}^{\boldsymbol{K}}\frac{1}{4}\times\left|\boldsymbol{H}[1,\boldsymbol{k}] + \boldsymbol{H}[2,\boldsymbol{k}]\right|^2 \quad \textbf{(5-16)}$$

$$\boldsymbol{P}_n = \frac{1}{\boldsymbol{K}}\sum_{\boldsymbol{k}=1}^{\boldsymbol{K}}\frac{1}{2}\times\left\{\left|\hat{\boldsymbol{W}}[1,\boldsymbol{k}]\right|^2 + \left|\hat{\boldsymbol{W}}[1,\boldsymbol{k}]\right|^2\right\}$$

$$= \frac{1}{\boldsymbol{K}}\sum_{\boldsymbol{k}=1}^{\boldsymbol{K}}\frac{1}{2}\times\left\{\frac{1}{4}\times\left|\boldsymbol{H}[2,\boldsymbol{k}] - \boldsymbol{H}[1,\boldsymbol{k}]\right|^2 + \frac{1}{4}\times\left|\boldsymbol{H}[1,\boldsymbol{k}] - \boldsymbol{H}[2,\boldsymbol{k}]\right|^2\right\}$$

$$= \frac{1}{\boldsymbol{K}}\times\sum_{\boldsymbol{k}=1}^{\boldsymbol{K}}\frac{1}{4}\times\left|\boldsymbol{H}[1,\boldsymbol{k}] - \boldsymbol{H}[2,\boldsymbol{k}]\right|^2 \quad \textbf{(5-17)}$$

Equation (5-18) recaps the definition of the MMSE equalization coefficient $\hat{\boldsymbol{C}}_{mmse}$. By incorporating $\boldsymbol{P}_s$ and $\boldsymbol{P}_n$ shown in Equations (5-16) and (5-17), $\hat{\boldsymbol{C}}_{mmse}$ can be expressed in Equation (5-19), and further derived to Equation (5-20).

$$\hat{C}_{mmse}[k] = \frac{\hat{H}[k]^*}{\left|\hat{H}[k]\right|^2 + \hat{\eta}}, \ \hat{\eta} = \frac{P_s}{P_n} \qquad (5\text{-}18)$$

$$= \frac{P_n \times \hat{H}[k]^*}{P_n \times \left|\hat{H}[k]\right|^2 + P_s} = \frac{P_n \times \frac{1}{2}\{H[1,k] + H[2,k]\}^*}{P_n \times \frac{1}{2}\left|H[1,k] + H[2,k]\right|^2 + P_s} \qquad (5\text{-}19)$$

$$= \frac{\frac{1}{2}\{H[1,k] + H[2,k]\}^* \times \frac{1}{K} \times \sum_{k=1}^{K} \frac{1}{4} \times \left|H[1,k] - H[2,k]\right|^2}{\frac{1}{2}\left|H[1,k] + H[2,k]\right|^2 \times \frac{1}{K} \times \sum_{k=1}^{K} \frac{1}{4} \times \left|H[1,k] - H[2,k]\right|^2 + \frac{1}{K} \times \sum_{k=1}^{K} \frac{1}{4} \times \left|H[1,k] + H[2,k]\right|^2}$$

$$= \frac{\{H[1,k] + H[2,k]\}^* \times \sum_{k=1}^{K} \left|H[1,k] - H[2,k]\right|^2}{\left|H[1,k] + H[2,k]\right|^2 \times \sum_{k=1}^{K} \left|H[1,k] - H[2,k]\right|^2 + 2 \times \sum_{k=1}^{K} \left|H[1,k] + H[2,k]\right|^2}$$

$$= \frac{H_{1+2}[k]^* \times \sum_{k=1}^{K} \left|H_{1-2}[k]\right|^2}{\left|H_{1+2}[k]\right|^2 \times \sum_{k=1}^{K} \left|H_{1-2}[k]\right|^2 + 2 \times \sum_{k=1}^{K} \left|H_{1+2}[k]\right|^2} \qquad (5\text{-}20)$$

Equation (5-20) give the direction to the hardware architecture for computing the MMSE coefficient $\hat{C}_{mmse}$. Figure 5.16 shows this architecture. It consists of two accumulators– $\sum_{k=1}^{K} \left|H_{1-2}[k]\right|^2$ and $\sum_{k=1}^{K} \left|H_{1+2}[k]\right|^2$, which accumulate $\left|H_{1-2}[k]\right|^2$ and $\left|H_{1+2}[k]\right|^2$, respectively, two squarers, one conjugator to negate the imaginary part of $H_{1+2}[k]$, one right-shifter for multiplying $\sum_{k=1}^{K} \left|H_{1+2}[k]\right|^2$ by 2, two multipliers, and one divider. The divider utilizes the look-up-table (LUT) based pipeline architecture proposed in [30]. Figure 5.17 illustrates this divider architecture.

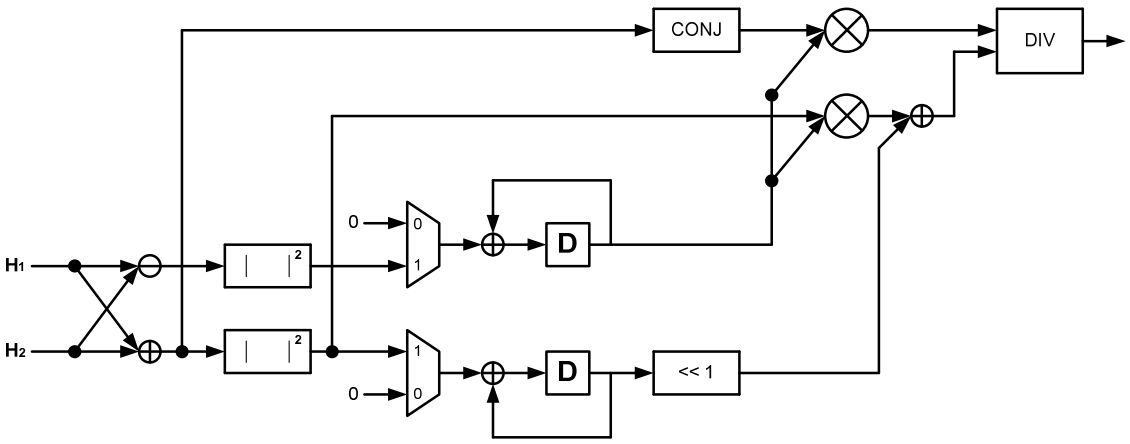


Figure 5.16 Architectue of MMSE coefficient computation.

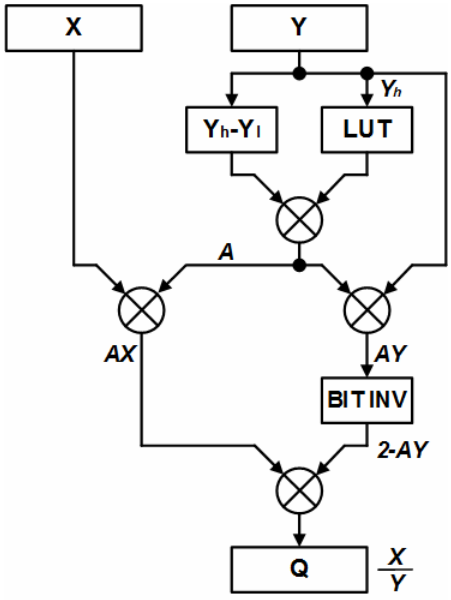


Figure 5.17 Pipeline divider with look-up table.

Chapter 6

Chip Design and Testing

6.1 DSP circuit design flow

The designs and implementations of the fractional-sampling-rate (FSR) synchronizer and the frequency-domain equalizer with high-accuracy channel estimator adopt the model-based design flow [36] as shown in Figure 6.1. The flow starts with the algorithm modeling and design by using DSP-oriented design languages or environment such as Matlab®, Simulink® and C/C++. The designed and modeled algorithms are then mapped to the hardware architecture in the format of register-transfer language (RTL) such as Verilog or VHDL through two concurrent approaches: (1) automatic mapping by commercial tools (e.g. Synplify®, System Designer®, Forte®, etc); and (2) manual mapping by the designer(s). The mapped RTL design is transformed into the standard-cell based circuits by the commercial logic synthesis and place and route (P&R) tools. (e.g. Cadence® RTL compiler and Encounter).

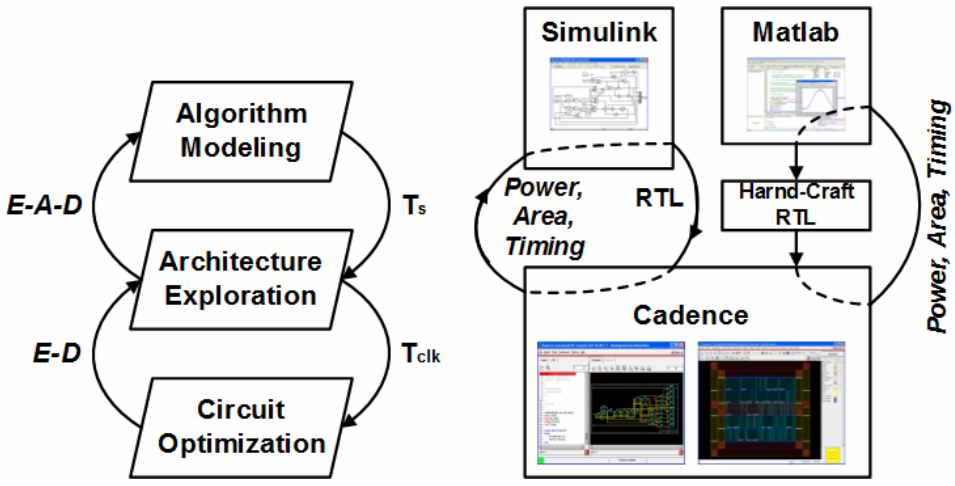


Figure 6.1 Design flow for digital signal processing circuits.

Theses synthesis and P&R tools also perform further circuit optimization in terms of power, area, and speed. It can be imagined that several iterations are needed for each stage of this flow in order to produce an optimized digital circuitry meeting functional and physical requirements.

6.2 Chip Testing Platform

Figure 6.2 illustrates the developed system for testing the fabricated chips of the synchronizer and the equalizer. Since these two chips operate at high clock rates (>440 MHz), and the number of inputs accepting the I/Q testing vectors and the number of the outputs providing the debug information are large, each of these two chips incorporate the on-chip memory module to store the testing vectors and results. The 4-wire serial SPI interfaces are incorporated into each chip to control the on-chip memory modules, and serve as the interfaces for the access of the external host computer. This combination of memory modules and SPI interfaces greatly save the number of I/O pads required for testing the chips. SPI adapters are used

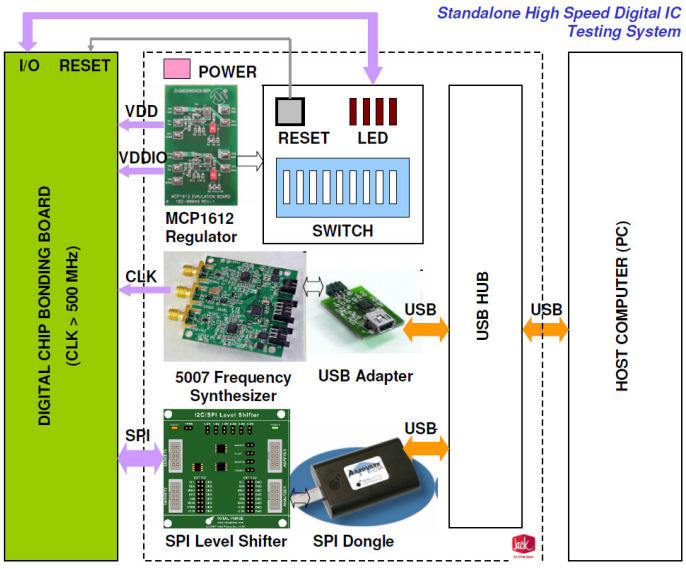
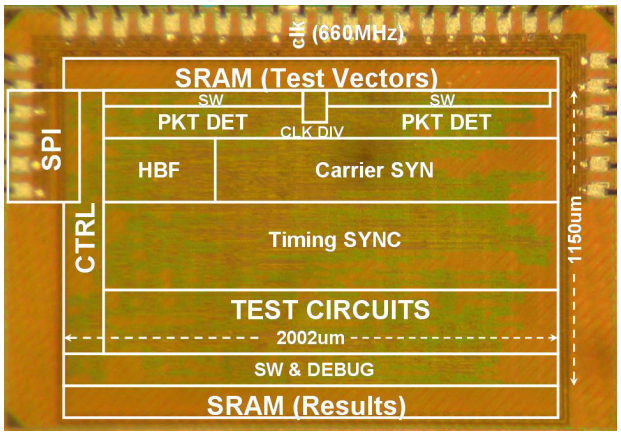


Figure 6.2 Standalone digital chip testing system

6.3 Chip Testing Results

6.3.1 FSR Synchronizer

The FSR synchronizer presented in Chapter 4 is fabricated in 65 nm general purpose CMOS process. Figure 6.3 shows the die photo of the fabricated chip and the summary of the chip performance. The testing results–the synchronized received signal samples–obtained from the on-chip memory storage are fed into the simulator of the frequency-domain equalizer with high-accuracy channel estimator presented in Chapter 5 for BER evaluation. Figure 6.4 shows that the synchronized signal samples provided by the path with maximum (Golay) correlation value can achieve about 100x BER reduction when compared with those provided by the path with minimum correlation value. This BER performance improvement validate the feasibility and concept of the FSR digital baseband receiver (synchronizer).



Technology	65nm
Core Area	1.32mm^2
Gate Count	350K
Voltage	1.2V/1.5V (core/IO)
Clock Freq	660/440/220MHz
Power	275mW
Modulation	PI/2 BPSK (Preamble) PI/2 16-QAM (Data)
Throughput	2.64GS/s (Preamble) 7.04GS/s (Data)

Figure 6.3 Micrograph of FSR synchronizer prototype and performance summary.

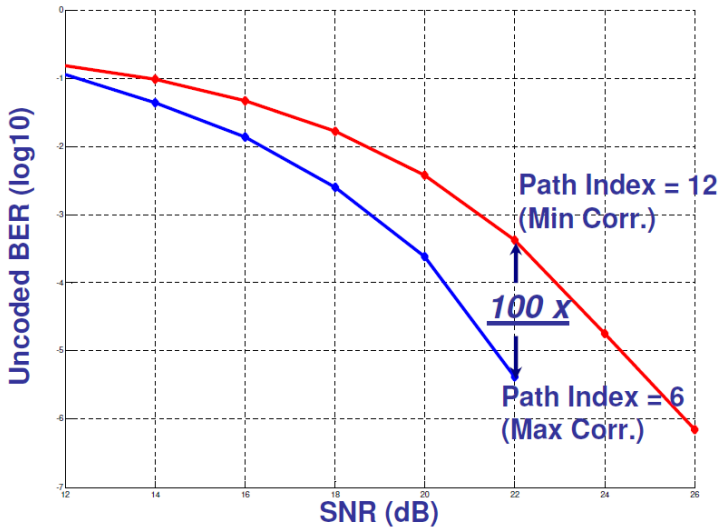
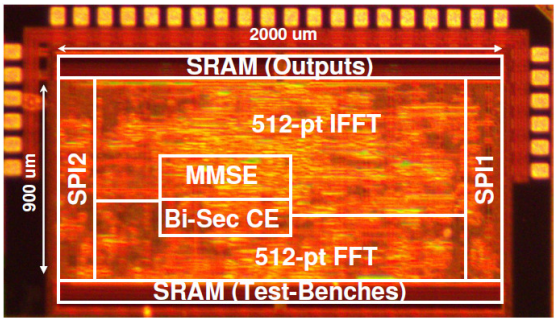


Figure 6.4 BER performance of FSR synchronizer.

6.3.1 MMSE FDE with Hi-Accuracy channel estimator

The hi-accuracy (bi-sectional) channel estimator presented in Chapter 5 is fabricated together with a MMSE frequency-domain equalizer in 65 nm general purpose CMOS process. Figure 6.5 shows the die photo of the fabricated chip and the its performance comparisons with the existing channel estimator in the prior art [8]. The testing results– the equalized received signal symbols–obtained from the on-chip memory storage are fed into the demodulator software program running on the host computer for BER calculation.



	This Work	[8]
Process	65nm	65nm
Architecture	Bi-SEC Golay CE	Golay CE
ADJ CES Interference De-Coupling	YES	NO
BER Reduction Factor (16QAM)	1/170	1
Chip Area	0.35 mm^2	0.13 mm^2
Clock Frequency	440MHz	440MHz
Power	4.8mW (ρ=0.1)	N/A

Figure 6.5 Micrograph of MMSE FDE with bi-sectional channel estimator and its performance comparison with the prior art.

The experiments with the presented bi-sectional channel estimation and with the existing approaches are conducted for validating the equalizer performance improvement. The implemented channel estimator can act similarly as the existing design [8] by disabling its building blocks of FIFO1/2, BF1/2, and EXTA/B. Figure 6.6 shows the experiment results. It is noted that the MMSE-FDE achieves substantially lower uncoded BER when adopting the proposed channel estimator than those of existing designs. Furthermore, the performance gap enlarges as the receiver SNR increases. When the SNR is larger than 22dB, the BER improvement factor is more than 170X.

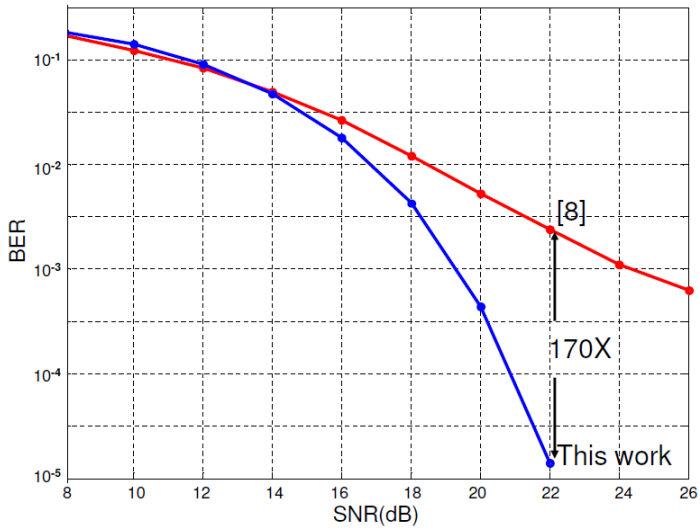


Figure 6.6 BER improvement under 16QAM modulation in comparison with the existing approach.

Chapter 7

Conclusions

The VLSI architectures and implementations of a digital fractional-sampling-rate synchronizer and a digital high-accuracy channel estimator for IEEE 802.15.3c 60 GHz communication system are accomplished and presented in this dissertation. The measurement results of the two 65-nm CMOS fabricated chips for these two essential processing units in a digital baseband design demonstrate the feasibilities of relaxing the ADC sampling rate specification by 25%, and assisting the MMSE frequency-domain equalizer in achieving 170x BER reduction.

Though the presented designs utilize the packet structure of IEEE 802.15.3c, they can be migrated to support other emerging 60 GHz standards such as IEEE 802.11ad and WiGig due to the similarity of the packet structure in these standards. Moreover, the architecture of the digital synchronizer is generic, and can be applied in various burst-mode communication systems. In addition, the explored advantage of utilizing the recursive structure of Golay complementary codes to reconstruct true channel responses gives a direction of specifying or searching an effective sequence for channel estimation in future and/or on-going high speed wireless communication systems, such as 5G cellular networks.

The presented architectures in this dissertation have the potential of being further formulated as a design framework which can provide performance and cost analysis before the chip fabrication. This framework can assist system designers in evaluating and/or defining wireless communication systems in a more practical manner.

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