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UNIVERSITY OF CALIFORNIA
SANTA CRUZ

**DESIGN OF A READOUT AMPLIFIER FOR A-SE/CMOS
HETEROGENEOUS X-RAY IMAGING IN 130 NM CMOS**

A thesis submitted in partial satisfaction of the
requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL AND COMPUTER ENGINEERING

by

Mariana Huerta

December 2023

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2023

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Abstract

Design of a Readout Amplifier for a-Se/CMOS Heterogeneous X-Ray Imaging in

130 nm CMOS

by

Mariana Huerta

As the need for precise, high performing imaging in applications such as medical imaging and high energy physics increases, so does the need for sensitive image detectors to capture crucial information and convert it to high-resolution images. Heterogeneous imaging addresses this by combining the advantages of non-CMOS photoconductive sensors with the flexibility and robustness of CMOS readout electronics. Heterogeneous imaging can open the doors to new and improved capabilities in X-ray and visible light imaging. This thesis describes the design of a readout amplifier for a heterogeneous X-ray camera based on amorphous selenium (a-Se) as a photoconductive material fabricated upon CMOS.

To my family,
friends, and mentors.

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Chapter 1

Introduction

The resolution of an imaging system determines the smallest object it can detect. In applications such as medical imaging, resolution is a critical feature that can impact diagnoses. For example, high resolution chest X-rays can detect cancerous tumors at early stages, making a difference in patient outcomes [5]. Small pixel sizes can be used to achieve high resolution X-ray imaging systems. However, pixel pitch alone is not sufficient in determining the resolution. High quantum efficiency in the photoconductive layer is crucial for high resolution.

For these reasons, a hybrid system combining a high quantum efficiency photoconductive layer with the small pixel sizes of CMOS technology is an attractive solution. Amorphous selenium, a direct conversion detector, can be hybridized to CMOS pixels to achieve gains in image resolution [6, 7, 8]. Direct conversion detectors typically achieve higher spatial resolution than indirect conversion detectors which use scintillators. In addition, sub-micron pixels can be implemented in CMOS technology, enabling the cap-

ture of more photons for higher spatial resolution. In previous work, the combination of direct conversion X-ray detectors with high resolution CMOS readouts has been proven to enable high spatial resolution readout. [9, 10]

Amorphous selenium is fabricated, characterized, and deposited onto thin-film transistors, CMOS integrated circuits, PCBs, and flexible substrates at UC Santa Cruz. However, these devices have not been customized for optimal use with amorphous Selenium. There is a need for custom CMOS integrated circuit design in order to create an imager system that is optimized for the unique characteristics of amorphous Selenium. One major objective is to improve resolution by designing an imager with smaller pixels. The goal is a pixel pitch of 7 μm with an imaging system operating up to 60 frames per second (fps) for video applications.

Noise performance is crucial in some applications. In CMOS imagers, correlated double sampling (CDS) is often used to reduce one of the important noise source contributors. Although CDS is typically used with 4T pixel architectures with a pinned photodiode to collect charge, we will use a 4T pixel with a MIM capacitor to collect charge. The long-term objective is to build a monolithic X-ray imager that combines an a-Se sensor and CMOS pixel array with high spatial resolution.

1.1 Imaging Technologies

1.1.1 Analog vs. Digital Imaging

The earliest form of X-ray imaging was analog, namely film or screen X-ray imaging [11]. An analog image detector for X-ray imaging is composed of X-ray film, an intensifying screen, and a cassette. The emulsion layer on X-ray film is of particular interest because it consists a blend of gelatin and photoconductive silver halide crystals [11]. In the film X-ray image capture process, photosensitive silver halide crystals absorb the photon energy of X-rays and release electrons to form electron-hole pairs. These released electrons then go on to react with silver ions containing crystalline defects to produce neutral silver atoms. This leads to an accumulation of silver atoms which form photosensitive spots. The photosensitive spots create a latent image which must be processed to become visible. Once the X-ray film is photochemically processed, the image becomes visible [11].

Although conventional film X-ray imaging can produce excellent images and has had an enormous impact on the medical field, it faces several challenges [12]. Some challenges faced by analog imaging include complex chemical processing, expensive film materials, time and labor for processing, and inconvenient image storage and communications [12]. The drawbacks of analog X-ray imaging provided a need for digital imaging as a replacement.

Digital imaging detectors use a sensor to convert X-ray photons into charges by generating electron-hole pairs [11, 12]. The resulting voltage or current from these

charges is detected by a pixel readout circuit and can be stored digitally. Digital imagers can provide wide dynamic range and the ability to communicate, store, and digitally manipulate images [1, 12]. However, digital imaging technology faced two major challenges in its early development:

1. Electronic noise in digital imagers corrupted the signal
2. Image resolution suffered from the large size of digital pixels

Through technological improvements, these problems were addressed and enabled digital imagers to become the foremost technology for both X-ray and visible light imaging [12, 11].

1.1.2 Direct vs. Indirect Conversion

X-rays are converted to electron-hole pairs via two different mechanisms: direct conversion and indirect conversion. [13] Direct conversion transforms X-ray photons into charges directly in the detector material. Amorphous selenium (a-Se) is the most well-known direct conversion material [14, 15, 16, 17]. Amorphous selenium can be manufactured at relatively low cost, can be fabricated over a large area, and has a low dark current at room temperature due to its 2.2 eV bandgap[18, 19, 20].

Conversely, indirect conversion has an intermediate step called a scintillator. In indirect conversion, X-ray photons are first converted to visible light in the scintillator which scatters the light. Then the visible light photons are converted to charge by a sensor [21]. The disadvantage of indirect conversion is that the scintillator scatters light

in every direction, leading to spatial resolution loss. [22] Direct X-ray conversion typically results in a higher modulation transfer function than indirect conversion, leading to better spatial resolution. [23]

A-Se fabrication consists of physical vapor deposition over a large area, so it can be directly evaporated onto the readout substrate. This fabrication process makes a-Se a desirable direct conversion material for flat-panel X-rays because it is simple and inexpensive to deposit it over a large flat area. [17]

1.1.3 Readout Technologies

After an X-ray sensor converts X-ray photons to electronic charges, pixels convert these charges to voltage signals. There are three main pixel technologies: thin film transistors (TFT), charge coupled devices (CCD) and CMOS pixels [1, 11]. Although TFTs can be developed for a large area at low cost, they can be more prone to process irregularities than CMOS. TFTs are also larger than CMOS transistors and have lower device mobilities, so they require a larger pixel area than CMOS [1, 11].

CCDs are known to provide high quality images with low noise [24]. Improvements in lithography, however, enabled CMOS imager performance to catch up to CCDs. CCDs operate much like a shift register by transferring the charge stored in each pixel to the adjacent one [1, 24]. A disadvantage of CCDs is that they are fabricated with custom processes, making the integration of additional analog/mixed-signal circuits a challenge. CMOS allows for flexible design and small pixel size, making it a good choice for digital imaging.

1.2 CMOS Pixel Architectures

CMOS imaging technology is composed of a variety of pixel architectures suitable for various conditions and specifications. A basic CMOS image sensor contains a 2-dimensional array of pixels and peripheral circuits [1]. The figure below illustrates the general structure of a CMOS image sensor.

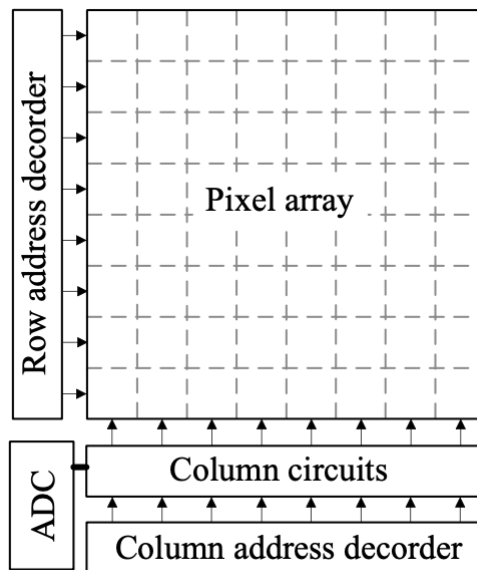


Figure 1.1: A general CMOS image sensor architecture, from [1]

There are three main pixel types [1]:

- Passive pixel sensor (PPS)
- Active pixel sensor (APS)
- Digital pixel sensor (DPS)

The resulting image quality depends on the type of pixel used in the imaging array, so it is important to choose the right type of pixel for the system. In this section, the passive pixel sensor and two types of active pixel sensor will be discussed.

1.2.1 Passive Pixel Sensor (PPS)

A passive pixel sensor (PPS) contains a photodiode and one MOS transistor (1T) per pixel [1]. As seen in Figure 1.2, the transistor connects the photodiode output to the pixel readout.

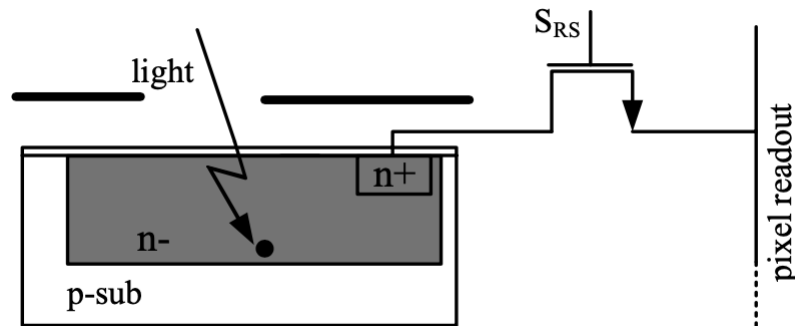


Figure 1.2: Passive pixel, image from [1]

The sensor operates as follows: light reaches the photodiode and is converted to charge by the capacitance inherent to the photodiode. The accumulated charges are then passed to a column bus when the MOS transistor is turned on [1]. In this way, the MOS transistor acts like a simple switch between the photodiode collected charges and the readout. The charges in the column bus are subsequently converted into voltages using a charge amplifier at the end of the column [2], as seen in Figure 1.3.

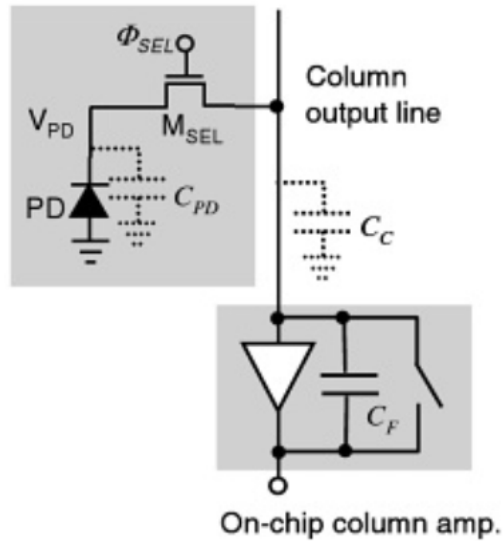


Figure 1.3: Passive pixel and column amplifier, from [2]

If using an n+/p-well photodiode, the n+ region of the MOS transistor can be extended to act as a photodiode [1]. This is an advantage of the passive pixel sensor because it can reduce overall pixel size. Other advantages of passive pixels are their high fill factor, large voltage swing and their simple architecture. Fill factor is the ratio of pixel area actively sensing photons to the total pixel area. [1]

$$\text{Fill factor} = \frac{\text{Area of the photodiode}}{\text{Area of the total pixel}} \quad (1.1)$$

Passive pixels have a large fill factor because they contain only one transistor. This means more area is taken up by the photodiode which actively collects photons, hence a high fill factor. The main disadvantage of the passive pixel is that the photodiode junction capacitance and parasitic column bus capacitance combine, resulting in longer

response time and excess noise charge [1]. Column bus capacitance can be seen in Figure 1.3, represented by C_C . Noise charge in electrons is defined [1]

$$q_{noise} = \frac{\sqrt{kTC}}{q} \quad (1.2)$$

where k is the Boltzmann's constant (1.38×10^{-23} J/K), T is the absolute temperature, C is the column capacitance and q is the elementary charge (1.6×10^{-19}) C.

The main advantage of this pixel architecture is its small area and high fill factor [1]. However, PPS image quality tends to be low due to noise. From Equation (1.2), we can see that noise charge increases as column capacitance increases. Therefore, for a passive pixel sensor, larger column capacitance results in a lower signal-to-noise ratio.

1.2.2 3T Active Pixel Sensor (APS)

A 3-Transistor active pixel contains a photodiode, reset transistor, in-pixel source follower amplifier and a row select transistor [1]. The photodiode component can consist of either a n+/p-well or n-well/p-well junction.

APS pixel operation begins when the reset transistor S_{RST} , acting like a switch, turns on [1]. This resets the photodiode sensor node to V_{DD} . After reset, integration occurs, where light is captured and converted to charge by the photodiode. The photo-generated charges discharge the photodiode capacitance, leading to a decrease in photodiode node potential. This is how the charges from the photodetector get converted to

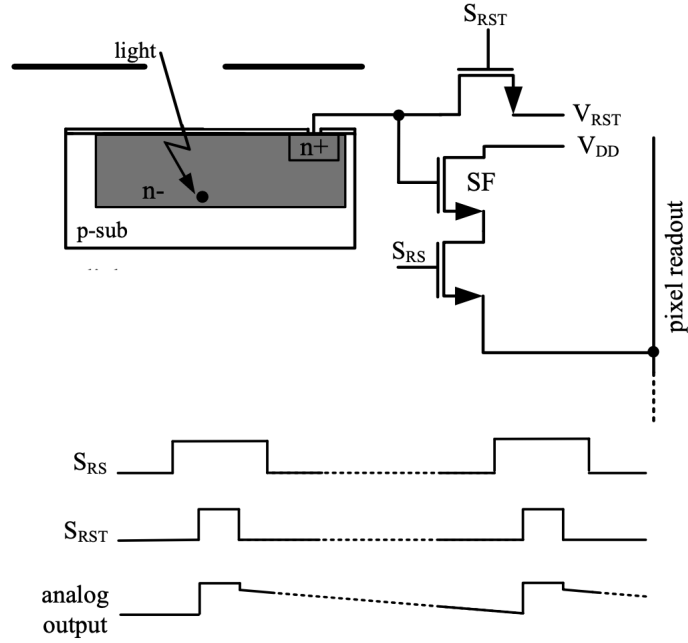


Figure 1.4: 3T Active Pixel, from [1]

voltage within pixel. the photo-generated charges are converted to voltage in the pixel itself. The conversion gain, which is defined as the output voltage per signal electron detected and expressed as $\mu\text{V}/e^-$, is determined by the photodiode capacitance [1].

A 3T APS typically contains a source follower amplifier within the pixel. The gain of a source follower is given by [1]

$$A_{vsf} = \frac{1}{1 + \frac{g_{mb}}{g_m}} \quad (1.3)$$

where A_{vsf} is the gain of the source follower, g_m is the transconductance and g_{mb} is the bulk transconductance of the source follower. As seen in equation 1.3, the

gain of the source follower is typically close to 1, so although it is an in-pixel amplifier, there is not much voltage gain in the pixel itself. Thus, an additional column amplifier is required to further amplify the voltage signal from the pixel sensor. This amplifier will be discussed later. After the signal has been amplified by the source follower, it is read out through the row select (S_{RS}) switch [1]. Since three transistors are used in APS, the fill factor is lower compared to PPS. However, because the photodiode can be reversely biased using a strong positive potential, a larger depletion region is formed which improves the quantum efficiency and the well capacity of the photodiode.

One disadvantage of a 3T APS is its fill factor. Because an APS uses three transistors, it has a lower fill factor than a PPS. Another disadvantage of the APS is limited output voltage swing [1]. The highest output voltage is reduced by two threshold voltages due to the NMOS reset transistor and the source follower. The minimum output voltage is limited by the operating region of the row select transistor. The minimum and maximum output voltage of the APS is given by equations (1.4) and (1.5) from [1]

$$V_{out,min} = V_{DS,sat} = V_{GS} - V_{TH} \quad (1.4)$$

$$V_{out,max} = V_{DD} - V_{TH} - V_{GS,sf} \quad (1.5)$$

Another drawback is that process mismatch in the source follower amplifier of an APS can result in fixed pattern noise (FPN) [1]. Fixed pattern noise is the spatial variation in the signal from pixel to pixel due to process variations.

1.2.3 4T Active Pixel Sensor (APS)

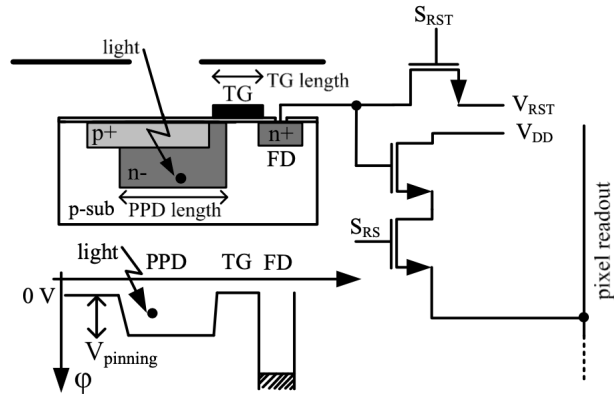


Figure 1.5: 4T Active Pixel, from [1]

A 4-Transistor pixel has four transistors inside the pixel and is schematically shown in figure 1.5 [1]. In a standard 4T pixel, a pinned photodiode (PPD) collects the charges generated by the photons and a transfer gate (TG) transistor transfers collected charges from the photodiode to the floating diffusion (FD) node. The pixel also includes a transistor (S_{RST}) to reset FD to a known voltage level (V_{RST}) prior to charge transfer. The other two transistors are the source follower and row select transistor (S_{RS}). The row select transistor transfers the signal to the column bus for pixel readout.

The pinned photodiode forms a fully depleted n-region. It is “pinned” to a voltage $V_{pinning}$, which is the potential when the depletion region of the two junctions p+/n- and n-/p-sub merge, depleting the n- region. The fully depleted structure reduces reset noise and image lag [1]. Reset noise is a type of thermal noise occurring when the photodiode is reset to a different level at each reset interval. Image lag occurs when not

all collected electrons are transferred to the FD node and some remain at the sensor node. The full depletion of the n- region allows the dissipation of collected electrons from the previous frame, resulting in reduced image lag [1].

1.3 Detector Performance Metrics

The performance of an imager system can be measured by several standard metrics. Nominal resolution and effective resolution are two such terms, commonly used to describe different aspects of image quality [25]. Nominal resolution refers to the maximum resolution that can be captured or displayed by an imaging system. It is typically expressed in terms of the number of pixels or dots per inch. However, nominal resolution alone does not provide a complete picture of image quality because it does not take into account other factors and their impact on the image resolution.

Effective resolution takes into consideration various factors that can affect the actual resolution of an image. It considers the overall quality of the image, taking into account factors such as sensor size, lens quality, image processing algorithms, and noise reduction techniques [25]. It can provide a more accurate representation of the level of detail that can be observed in the final image.

Nominal resolution represents the maximum capability of a device or system, while effective resolution provides a more realistic assessment of the actual level of detail and quality that can be achieved in an image. [25] The effective resolution will always be equal to or worse than nominal resolution due to this.

1.3.1 Signal-to-Noise Ratio and Contrast-to-Noise Ratio

The signal-to-noise ratio (SNR) is an important measure used in imaging to quantify the level of signal strength compared to the level of background noise present in an image [1]. In imaging, the signal represents the useful data and information captured from an image, such as small distinct details in a chest X-ray. The noise represents unwanted variations or random fluctuations captured by the system. Noise contributors include electronic noise, sensor noise, or environmental interference, all of which can degrade an image's quality and make it more difficult to distinguish fine, critical details in an image.

SNR is typically expressed as a ratio in decibels (dB) [1]. A higher SNR indicates a stronger signal relative to the noise, resulting in a clearer and more distinguishable image. In contrast, a lower SNR indicates a weaker signal compared to the noise, which can lead to a loss of detail and reduced image quality. Achieving a high SNR is important in imaging applications because it helps us see important details and enhances overall image quality. Various techniques can be used to improve SNR, such as increasing the signal strength, optimizing sensor performance, reducing noise sources, and using advanced image processing algorithms [1].

CNR, like SNR, is another useful metric in assessing detector performance [26]. Contrast-to-noise ratio (CNR) is a measure used in imaging to assess the level of contrast between different regions or structures in an image relative to the level of background noise. Contrast represents the difference in intensity or appearance between

different regions or structures within an image. It is used to highlight boundaries, edges, or variations in the image. Noise represents unwanted variations or random fluctuations. We can find CNR by taking the difference in contrast between two regions of interest and dividing it by the standard deviation of the noise in the image. A higher CNR indicates a greater contrast between the regions of interest relative to the noise level, resulting in better differentiation and clearer visualization of the distinct features.

We want a high CNR in imaging applications because it helps enhance the visibility and differentiation of important structures or details in an image [26]. We can improve CNR through techniques such as optimizing imaging parameters, reducing noise sources, and using advanced image processing algorithms to improve image quality and diagnostic accuracy.

1.3.2 Limit of Detection

The limit of detection (LOD) is the minimum signal or lowest X-ray dose that can be detected by an imager [27]. It represents the lowest amount or smallest size of an object or signal that can be reliably distinguished from the background noise or other interfering factors. LOD can be impacted by the amount of noise present in the system. The limit of detection is affected by many factors, including the sensitivity of the imaging system, the noise level, the image resolution, and image processing techniques. A lower LOD corresponds to a higher sensitivity and the ability to detect smaller or weaker signals or features.

The LOD is often determined by statistical analysis and is typically defined as

the signal or feature level that can be detected with a certain level of confidence [27]. LOD is an important parameter for assessing the ability of imaging systems to detect and resolve small or weak signals or features in an image.

1.3.3 Dynamic Range

Dynamic Range (DR) for an imager is defined as the difference between a bottom limit (limit of detection) and an upper limit (imager's supply voltage) [1]. For a linear image sensor, the dynamic range is the ratio of the largest possible signal divided by the smallest possible signal it can detect. The lowest signal is the noise floor, which is the noise level when the sensor is not exposed to any light [1].

Dynamic range is the range of brightness that a camera or imaging system can capture or display. It represents the ability of the system to accurately reproduce both the darkest and brightest parts of an image [1]. In other words, dynamic range measures the difference between the darkest and brightest areas that can be captured or displayed in an image without losing detail or introducing significant noise.

A high dynamic range means that the imaging system can capture a wide range of brightness levels, resulting in images with rich detail and tonal gradations. This is particularly important in scenes with high contrast, where there are both very bright and very dark areas. Dynamic range is influenced by various factors, including the sensor's sensitivity and noise levels [1].

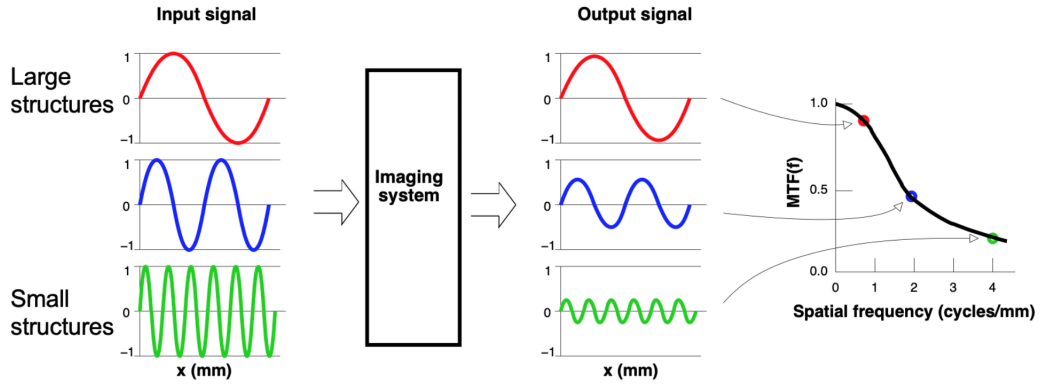


Figure 1.6: Modulation Transfer Function

1.3.4 Modulation Transfer Function

The modulation transfer function (MTF) describes the spatial frequency response of the system. Due to resolution loss in the imager, not all frequencies of a signal may be transferred to the system output equally. MTF tells us how well an imager system can reproduce all frequencies of an input signal at the output [28].

1.3.5 Detective Quantum Efficiency

Detective quantum efficiency (DQE) is a standard measurement of image quality in X-ray imaging. DQE measures the efficiency of an X-ray imaging detector in detecting X-ray photons [29]. DQE also takes the signal-to-noise ratio (SNR) and the system noise into account. DQE can show the performance of the X-ray imaging detector in terms of X-ray imaging quality and the X-ray radiation dose. Digital X-ray imaging typically has a higher DQE than conventional film X-rays, meaning that digi-

tal X-ray imaging can convert a higher proportion of photons into charges compared to analog film X-ray imaging [11].

1.4 Sensor Material

1.4.1 Amorphous Selenium

Amorphous Selenium (a-Se), when used as a photodetector material, provides many benefits useful for X-ray imaging, such as high sensitivity, direct conversion, wide dynamic range, fast response time, high spatial resolution, and stability [4, 17, 30, 31]. Amorphous selenium's high sensitivity to X-rays allows for good image quality even for small details. This is crucial for radiological medicine, where being able to see small discrepancies in an X-ray can significantly impact a diagnosis. Amorphous selenium also offers the advantage of directly converting X-ray photons into charges, which reduces signal loss and improves efficiency of X-ray detection [16, 32]. The wide dynamic range of a-Se detectors means they can accurately capture a range of X-ray signal intensities, from low-intensity to high-intensity. [33] Amorphous selenium's high spatial resolution is also advantageous for producing detailed, sharp X-ray images for precise medical analysis. [34] In medicine, precise X-ray images are essential for proper diagnosis. Finally, a-Se detectors maintain stable performance over time with little degradation due to mitigation through alloying. [35] Amorphous Selenium is a mature technology which has evolved to address stability issues over time.

In commercial mammography devices, it has been deposited in 200 μm thick

layers all the way up to 1 μm , making it suitable for absorbing high energy X-rays [36, 37, 38]. Furthermore, its high vapor pressure allows for uniform coverage over a large detection area.[39] Amorphous selenium can undergo an avalanche process when a large voltage is applied, making it an advantageous detector due to avalanche gain in the sensor. [40] It is also a direct conversion detector, allowing medical professionals to see small calcifications in breast tissue through mammography. [41, 42] Therefore, there is growing interest in researching novel detector structures and integrating a-Se with new materials to make use of its unique properties.

For X-ray readout, the capabilities of a-Se make it well suited for the photodetection layer [43]. Integrated with solid state CMOS readout circuits, we can enable higher quality medical imaging for effective and early diagnoses. Due to all these advantages, amorphous selenium (a-Se) is presently used for low-cost and large area flat panel X-ray imagers [17].

Chapter 2

Proposed Architecture and Specifications

The proposed architecture for image readout of an amorphous Selenium photodetector can be found in Figure 2.1. In the proposed system, each 4T pixel in the array is read out one by one, where an entire column is read out at a time and one row in each column is selected at a time. The pixel array contains a readout amplifier, which I have designed in 130 nm CMOS for this purpose. The output of the amplifier can subsequently be sent to an off-chip analog-to-digital converter (ADC) for digitization.

The diagram in Figure 2.1 shows a single unit of the proposed architecture. Each 4x4 array of 4T pixels is read out by a single voltage amplifier as seen in the block diagram. A 4x4 pixel array is used for demonstration of the system architecture, but the pixel array plus readout amplifier core unit can consist of any size pixel array and be scaled up to achieve a desired pixel array size. The number of pixels can be determined

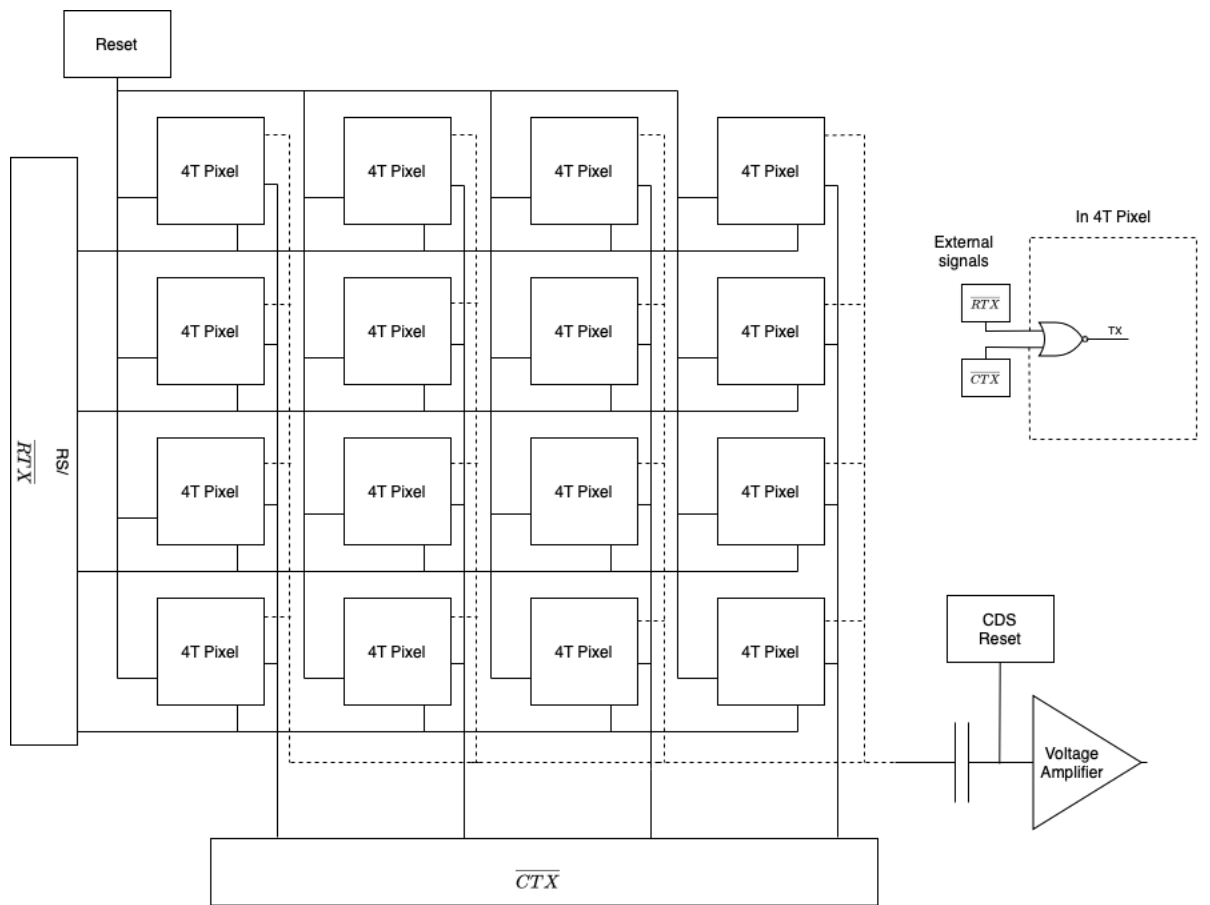


Figure 2.1: System Diagram of Proposed Imaging System

by the following relationship:

$$\text{Number of pixels} = \frac{\text{clock speed}}{\text{frame rate}} \quad (2.1)$$

Where clock speed is in units of Hertz and frame rate is in frames per second (fps). For purposes of our imaging system, the attainable clock speed is 4 MHz and the desired frame rate is 10 fps. Therefore, the imaging system needed to meet these

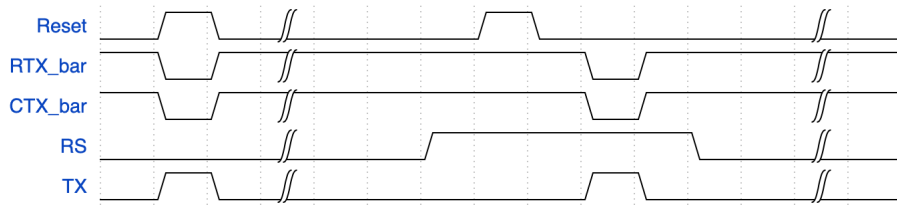


Figure 2.2: Timing Diagram of Proposed Imaging System

specifications will require 400,000 pixels. The more pixels are needed for the imager, the more amplifiers will be needed to maintain readout at a desired frame rate.

2.0.1 Correlated Double Sampling

A technique for measuring electrical values like voltages or currents that enables the removal of an unwanted offset is called correlated double sampling (CDS). It is frequently applied while gauging sensor outputs. Two measurements are made of the sensor's output: one under known conditions and one under unknown conditions. To obtain a value with a known relation to the physical quantity being measured, the value measured from the known condition is subtracted from the unknown condition [44].

At the end of each integration period, the dark-level voltage of the pixel (the pixel's voltage after it is reset) is subtracted from the signal voltage of the pixel (the pixel's voltage at the end of integration) in order to cancel kTC noise (the thermal noise associated with the sensor's capacitance).

In the proposed system architecture, an AC coupling capacitor can be seen between the pixel array column lines and the input to the voltage amplifier. This

capacitor collects charge from the pixel array. Following the principles of CDS, the signal from the sensor is measured once after all pixels have been reset and once after integration of a pixel. Then, the signal after reset, also known as the fixed pattern noise, is subtracted from the signal after integration. This is outlined in the following equation:

$$(Signal + reset + noise_2) - (reset + noise_1) = signal + (noise_2 - noise_1) \quad (2.2)$$

By subtracting out the noise from the pixel reset, we are left with only the signal and the difference between noise samples 1 and 2, which is reduced. In this way, CDS, can help mitigate noise in the readout signal chain.

2.1 System Specifications

When deciding parameters for sensor, pixel, and readout amplifier design, we must consider the desired system specifications for our X-ray application. Below is a table listing desired specifications for both the pixel array and output amplifier. These specifications have been derived with guidance from Michael Farrier based on similar a-Se/CMOS hybrid imagers that have previously been implemented for similar performance targets. We have chosen a 7um x 7um square pixel, with a targeted frame rate of 10 fps. Our pixel model is also a 4T hole integrator with global shutter operation.

Regarding output voltage swing, we want the output of the readout signal to

Feature	Specification
Array size (number of pixels)	400K
Pixel size (μm)	7 x 7
Max frame rate (fps)	10
Pixel type	4T hole integrating, global shutter
Pixel cap (fF)	25 to 55
RMS noise (e-)	≤ 100
CMOS Technology	130nm 5-metal process, 3.3V mixed signal, MIMCAP

Table 2.1: Pixel Array Specifications

Feature	Specification
Open-loop gain (dB)	> 85
Unity-gain bandwidth (Hz)	$> 10\text{M}$
Output voltage swing (V)	0.25 to 2.9
Phase margin (degrees)	> 60
Input noise (e-)	< 20
Column scan rate (Hz)	$> 7\text{M}$

Table 2.2: Readout Amplifier Specifications

swing as close to rail to rail as possible. This allows the system to detect wider ranges in image value more sensitively.

We have a MIM capacitor at the input of each 4T pixel integrating charge from the photodetector stage. A higher capacitance is desired for maximum charge integration, but there comes a tradeoff with signal to noise ratio (SNR). Due to the inverse relationship between SNR and capacitance discussed in the previous chapter, a large capacitor diminishes our SNR. Therefore, an input capacitor must be chosen such that it can store enough charge to produce an adequate signal without degrading SNR.

After determining the desired design and parameters of our detector, pixel,

and readout amplifier, the system design becomes an iterative process of simulation and adjustment of parameters. In Chapter 3, I discuss the design of an instrumentation amplifier designed for the specifications of a hybrid a-Se/CMOS imager.

Chapter 3

Design

3.1 Amorphous Selenium Photoconductor

Amorphous Selenium is sought after as a detector because it can be deposited over a large area with sufficient thickness to absorb the required energy of X-ray photons [45]. A-Se can be evaporated onto the surface of a CMOS chip during post-processing to achieve a large area pixel imager.

3.1.1 Resolution

As a direct conversion sensor, a-Se demonstrates higher spatial resolution than indirect conversion sensors. In indirect conversion, X-ray photons are converted to visible light and scattered in a scintillator, then absorbed and converted to charges in the detector. This can result in photons spreading to neighboring pixels during image capture and a lower resulting quantum efficiency [46]. Using a-Se as a direct conversion

detector enables us to achieve high spatial resolution and high quantum efficiency [46].

3.1.2 Sensor Capacitance

	Device Diameter		
	3 mm	4 mm	5mm
$C_{Se}(pF)$	24.84 ± 0.13	44.26 ± 0.20	69.41 ± 0.17
$C_{PI/Se}(pF)$	21.91 ± 0.58	39.71 ± 0.02	62.14 ± 0.31
$C_{PI}(pF)$	185.51 ± 41.99	386.90 ± 15.54	593.28 ± 30.53

Table 3.1: Capacitance measurements at 100 KHz for devices with and without polyimide hole-blocking layer and the resulting calculated capacitance of polyimide, from [4]

For our desired system, we require a pixel of size $7 \mu\text{m}$ by $7 \mu\text{m}$. Table 3.1 shows measured sensor capacitances for $15 \mu\text{m}$ thick a-Se sensors with different diameters.

From the Table above, the capacitance of a $7 \mu\text{m}$ by $7 \mu\text{m}$ would be:

1. Without PI: 0.17 fF
2. With PI: 0.15 fF

Although the goal thickness for this system is $200 \mu\text{m}$, the data from this table shows that from a fabricated sensor, capacitance can be extrapolated for a sensor of any thickness or diameter.

3.2 CMOS Pixel

For this hybridized imager, we aim to use an amorphous Selenium detection layer bonded to a 4T readout pixel with a global shutter. Global shutter image capture

mode is when all pixels of an imager array are exposed simultaneously. This is different from a "rolling" shutter mode, where different lines of the array are exposed at different times.

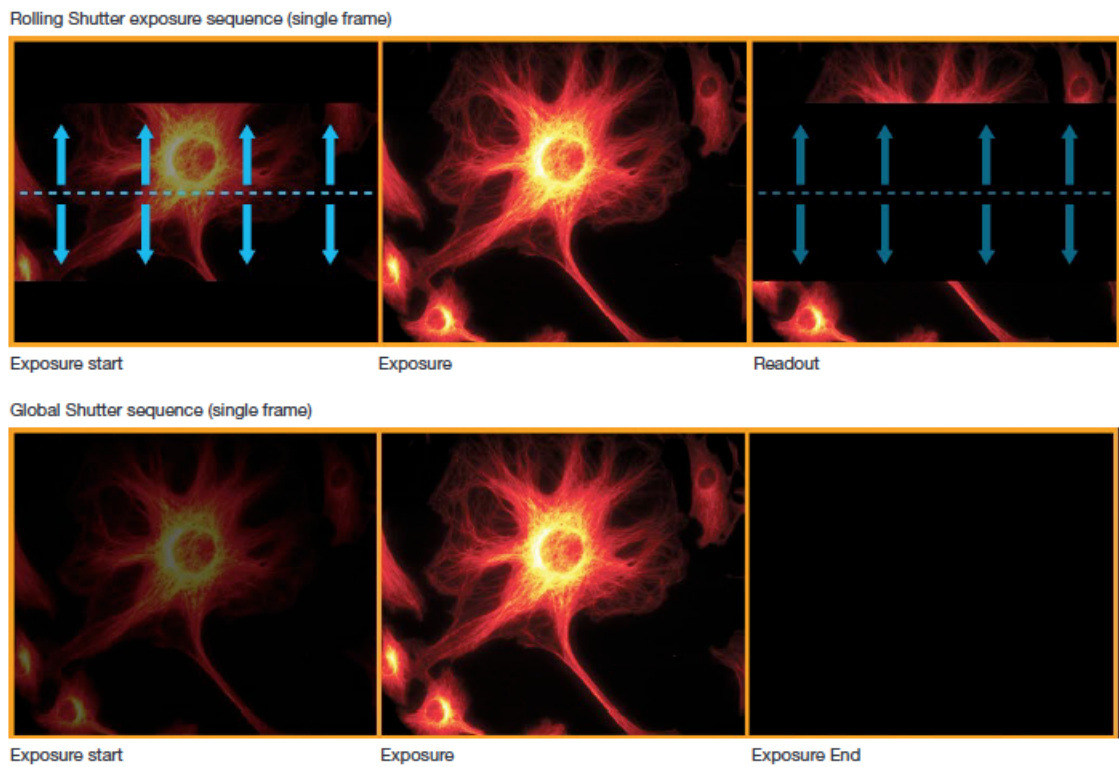


Figure 3.1: Illustration of event sequence in rolling and global shutter modes for a single image capture, from [3]

Although the rolling shutter capture method provides low noise and fast non-synchronized frame rates, it creates some problems for image quality. The rolling shutter method can result in spatial distortion. Spatial distortion is more likely in cases where larger objects are moving at a rate that the image readout cannot match [3]. However, distortion is less likely when the imager's frame rate oversamples the rate at which

relatively small objects are moving.

Another disadvantage of rolling shutter mode is that different regions of the exposed image will not be precisely correlated in time to other regions. Depending on the application, this can be detrimental. In addition, synchronizing to rolling shutter readouts can be complex can lead to slower cycle times and frame rates compared to what's possible with a global shutter capture [3].

In contrast to rolling shutter mode, global shutter mode is when all pixels of the array are exposed simultaneously. This enables the capture of fast moving or fast changing events. Before exposure, all pixels in the array will be held in a reset state. When exposure starts, each pixel simultaneously begins to collect charge for the duration of exposure time. At the end of exposure, the pixels all transfer charge to readout at once [3].

Global shutter mode is easier to synchronize and can achieve faster synchronized frame rates than a rolling shutter with comparable exposure time. Global shutter also enables precise time correlation between different regions of the sensor area. However, a drawback of global shutter is that it requires an extra reference readout in order to eliminate noise accumulated during reset, leading to slower unsynchronized frame rates [3].

We choose global shutter mode for its spatial resolution, precise time correlation, and high synchronized frame rates.

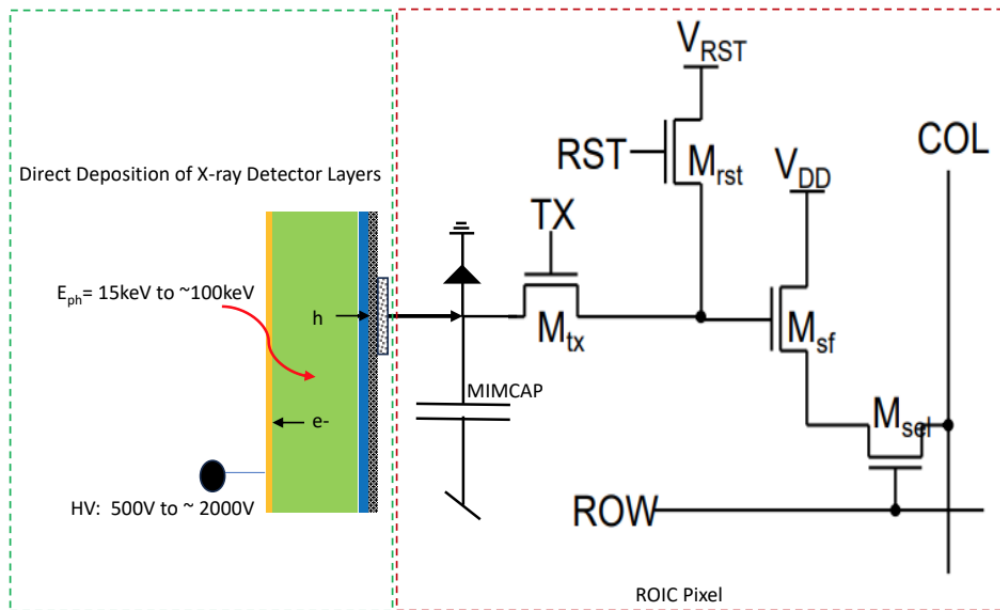


Figure 3.2: a-Se/ROIC Pixel: 4T Global Shutter.

Feature	Specification
MIMCAP (fF)	25 to 55
V_{rst} (V)	3.3 to 5
V_{dd} (V)	3.3 to 5
W/L	0.5 to 10
Pixel gain ($\mu\text{V}/e^-$)	5 to 15
Column rate (MHz)	3 to 9

Table 3.2: 4T CMOS Pixel Specifications

3.2.1 4T Pixel Model

The green box in Figure 3.3 contains the amorphous Selenium detection layer. It will receive high voltage bias of 500 V to 2000 V and can handle photon energies of 15 keV to 100 keV.

The red box on the right side of Figure 3.3 contains the 4T active pixel which

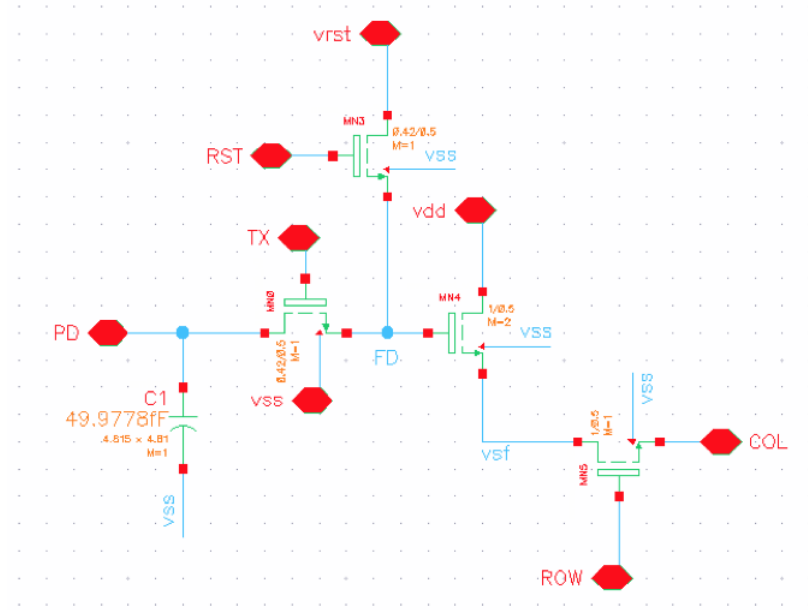


Figure 3.3: 4T Pixel Model in Skywater 130 nm

contains a photodiode and MIM (metal-insulator-metal) capacitor at the input. This is followed by a TX (transmit) transistor, M_{tx} , which separates the charge accumulated by the MIM capacitor from the input to the source follower transistor, M_{sf} . The pixel also contains a reset transistor M_{sf} , which performs the global reset for all pixels. Finally, the selection transistor M_{sel} is connected to the row and column buses and can be activated for each pixel during integration and readout.

3.3 Analog Readout

3.3.1 Instrumentation Amplifier

The instrumentation amplifier for a-Se builds on my earlier work on design of an instrumentation amplifier for the readout of signals from functionalized carbon nanotube sensors in the NanoCMOS chip at LBNL. The voltage amplifier required a high input impedance to sense input changes from the carbon nanotubes and a low output impedance to drive a low impedance load. While the output impedance of the carbon nanotubes is currently unknown, the load resistance is about 50 Ohms, a standard value for electronic test bench equipment (i.e. oscilloscope). The instrumentation amplifier configuration allows for the flexibility to meet a wide range of input impedances from the CNT sensors while maintaining high speed. The first iteration of the readout IC for NanoCMOS was designed and implemented by Lawrence Berkeley National Laboratory IC Design Engineer Katerina Papadopoulou in TSMC 180 nm technology. As a research intern working with the NanoCMOS team, I was tasked with porting Katerina's design to the open-source Skywater 130 nm technology. As part of the porting process, I characterized the technology, created schematics with the existing bias points and transistor sizes, and made testbenches to simulate the performance of the existing design in Skywater 130 nm CMOS. Upon finding performance disparities between the existing 180 nm design and the ported 130 nm design, my objective was to resize the op-amp, as well as redesign a biasing circuit from scratch. The following sections explain the biasing and sizing process from technology characterization to op-amp schematic, as

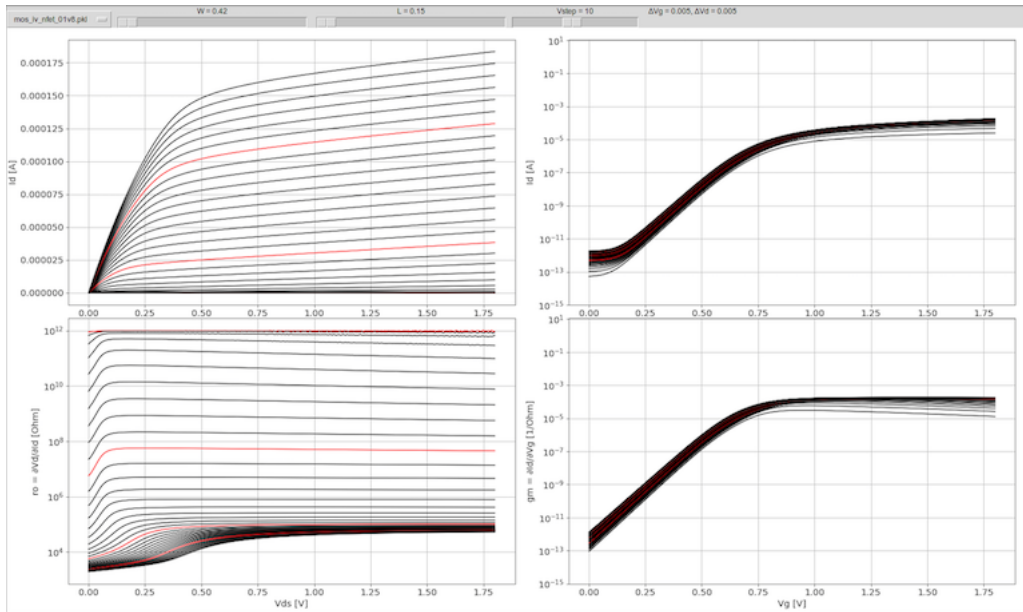


Figure 3.4: Skywater 130 nm NMOS and PMOS I/V curve plotting window

well as the resulting performance specifications of the redesigned circuits for Skywater 130 nm CMOS.

3.3.1.1 Technology Characterization

As seen in Figure 3.4, a first step in understanding Skywater 130 nm technology was to plot the I/V response of the different flavors of NMOS and PMOS transistors in the process kit. In Figure 3.4, I/V curves for different transistor types, W/L ratios, and Vgs or Vds steps were plotted. This characterization step helped me understand the large signal operating behavior of the transistors I would be working with for the amplifier.

Another step in my process was to determine bias points for my voltage ampli-

fier. The amplifier's topology is a PMOS-input folded cascode with a Class-AB output stage and Monticelli bias [47]. From the I_D vs. V_{dsat} curves in Figure 3.1, I found overdrive voltages and W/L ratios for each transistor through the following process.

3.3.1.2 Device Sizing

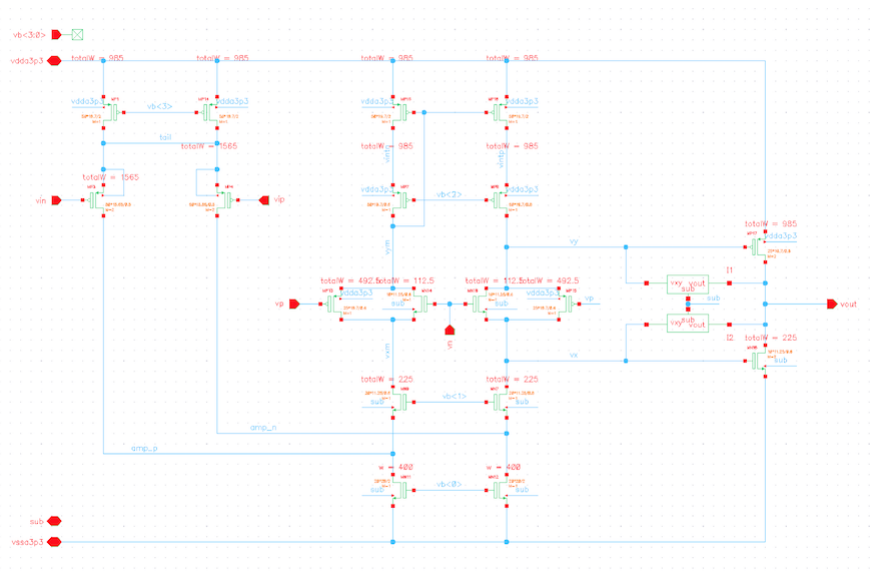


Figure 3.5: Op-Amp Schematic with Sizing for 130 nm CMOS

The device size calculations for the first stage of the voltage amplifier are presented in Table 3.3. The main design specifications for the voltage amplifier were a high input impedance, high gain, wide input common mode, and a wide output swing. The design methodology was as follows:

- Calculate required g_m from circuit bandwidth $\frac{g_m}{C_L}$
- Starting with minimum L, choose current density I_D/W for optimal performance

- Confirm the transition frequency f_T of the devices is sufficient
- Iterate on the design/topology until performance specs are achieved

For a desired unity-gain bandwidth of $\Omega = 100$ MHz and load capacitance of $C = 10$ pF, I found the required transconductance g_m through the input devices of the folded cascode stage. From this transconductance value and a chosen input device overdrive voltage of 100 mV, I calculated that 630 μ A of current through each branch were needed to bias the op-amp. Assuming minimum device lengths, I needed to find device widths as a function of desired current over current density per micron. I used the I_d vs. V_{dsat} curves from Figure 3.1 to find the current density for a 1 μ m wide transistor for a desired overdrive voltage, given that V_{dsat} is equal to overdrive voltage in saturation. From this analysis, I determined the transistor sizes found in Table 3.3 for the voltage amplifier. The op-amp schematic can be found in Figure 3.2.

Transistor	W/L (μ m)
M_{in}	1565/0.5
M_{tail}	985/2
M_{Isrc1}	985/2
$M_{cascode1}$	985/0.6
$M_{cascode2}$	225/0.6
M_{Isrc2}	400/2
M13, M15	492.5/0.6
M14, M16	112.5/0.6
M17	985/0.6
M18	225/0.6

Table 3.3: Operational Amplifier Sizing

3.3.1.3 Biasing Circuit

For initial simulation, the op-amp was biased using ideal voltage and current sources. However, these voltages and currents eventually need to be generated with physical devices. In order to maximize signal to noise ratio, it is preferable that the bias circuitry have the ability to produce high voltage swing. This section describes the design choices for the biasing circuit.

Bias voltages can be generated by applying a current through a diode connected transistor to create a current mirror. The gate to source voltage of this transistor, V_{GS} , is expressed as:

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{\mu n C_{ox} \frac{W}{L}}} \quad (3.1)$$

A constant bias voltage, V_{GS} , results from a constant bias current, I_D .

A bias circuit based on the high-swing folded cascode current mirror was used to provide bias voltages and currents to the op-amp. The high swing folded cascode current mirror is a specific type of current mirror circuit that is designed to achieve a high output voltage swing while maintaining good linearity and stability. In a folded cascode current mirror, the basic current mirror configuration is combined with a cascode amplifier. This configuration helps to improve the output impedance and increase the voltage swing capability of the circuit by saving one threshold voltage.

High swing folded cascode biasing is used to provide a high voltage swing and improve the linearity of amplifiers. The biasing circuit is designed to allow a larger

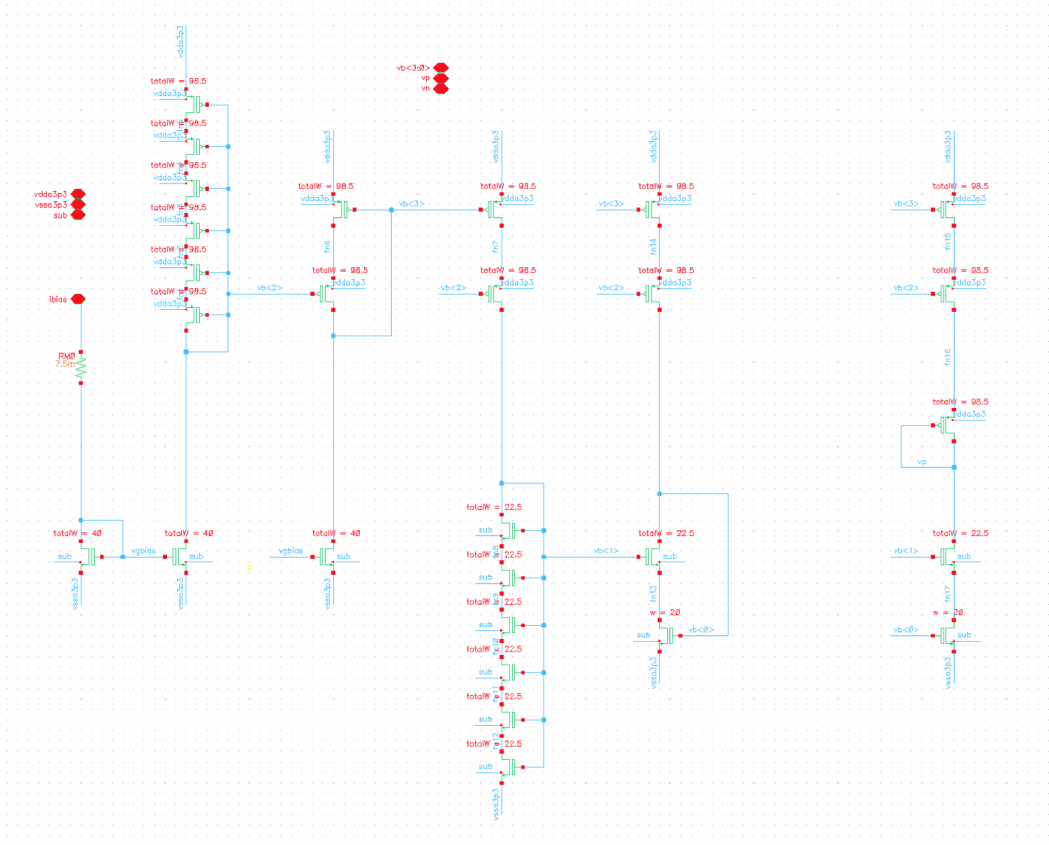


Figure 3.6: High Swing Folded Cascode Bias Circuit for Voltage Amplifier in 130 nm CMOS

voltage swing at the output, which is beneficial for applications requiring a wide dynamic range such as medical X-ray imaging.

The sizing for the bias circuit is as follows:

Transistor	W/L (μm)
All M_P	98.5/2
$M_{N1} - M_{N3}$	40/2
$M_{N4} - M_{N12}$	22.5/2
$M_{N13} - M_{N15}$	20/2

Table 3.4: Biasing Circuit Transistor Sizing

3.3.2 Open-Loop Analysis

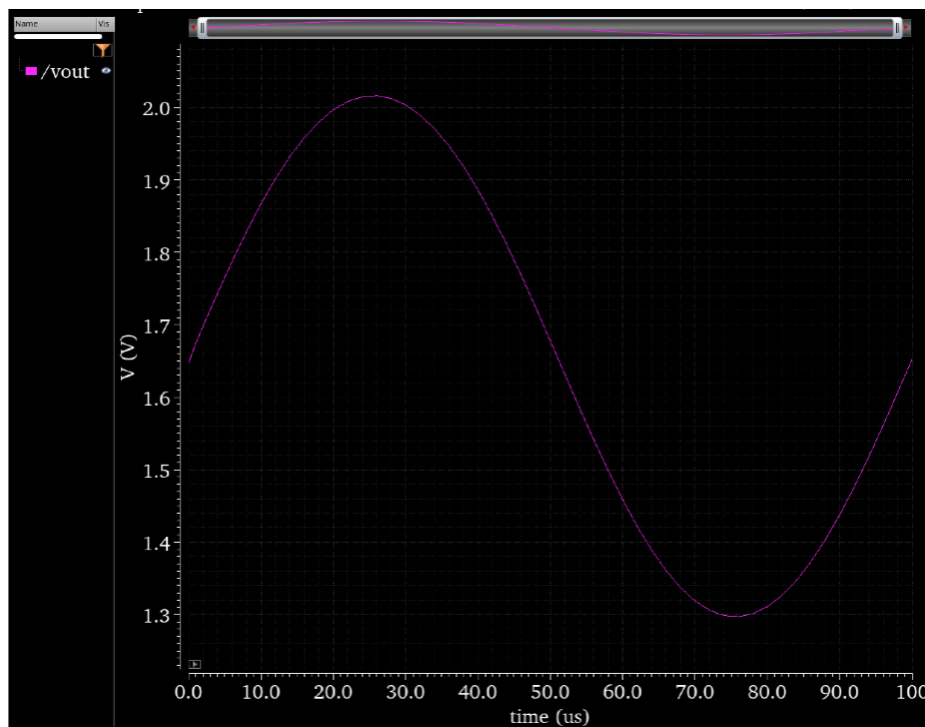


Figure 3.7: Open-loop transient analysis of opamp

For the given op-amp, we are particularly interested in the behavior of the amplifier when loaded by 50 ohms. This corresponds to load the amplifier sees when connected to electronic test equipment, i.e. oscilloscope. It was necessary to achieve a low output impedance for the op-amp to drive a small resistive load. The following plots show the AC behavior of the amplifier with a load of 50 ohms. Note that the design objective was to create an amplifier with unity gain frequency of greater than 10 MHz (with a goal of up to 100 MHz) and open loop gain of at least 85 dB. The results from Figure 3.9 and Table 3.4 show that the phase margin and unity gain frequency

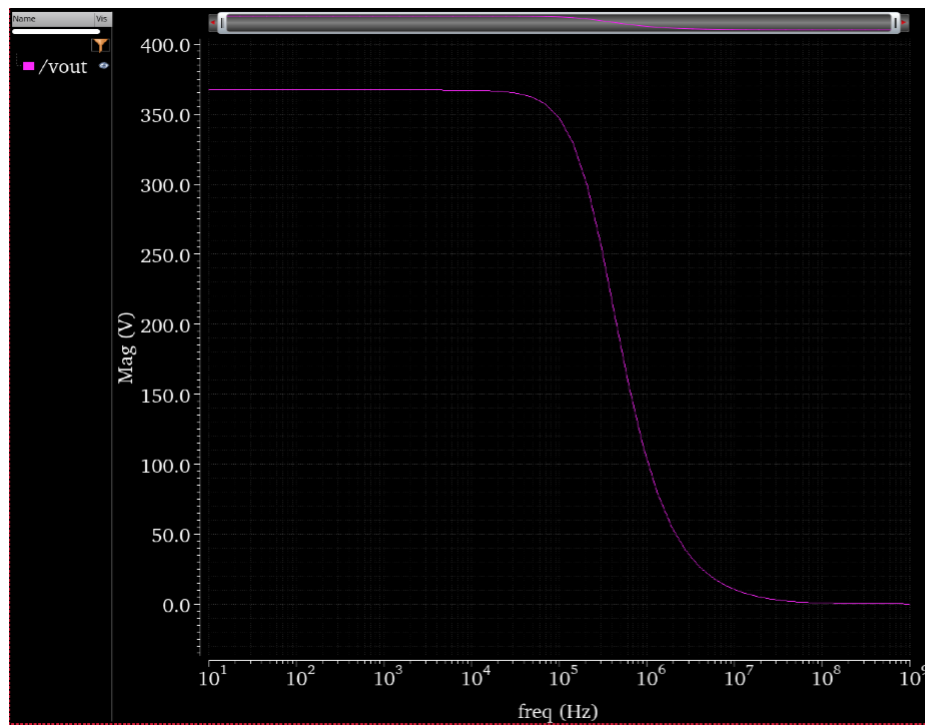


Figure 3.8: Open-loop AC analysis of opamp

targets were met. However, the open-loop gain target was not met and requires further optimization or tradeoff with other specifications. The output voltage swing can be seen in Figure 3.8 as ranging from approximately 1.3 V to 2.0 V. With the goal for output voltage swing being 0.25 V to 2.9 V, there is further optimization to be done to meet the output voltage swing specification. Overall, the simulated performance of the opamp that we see is sufficient for the proof-of-concept application in mind.

AC Characteristics	
Gain (dB)	51.3
Phase Margin (degrees)	84.5
Unity-gain bandwidth (Hz)	85.2M
Bandwidth (Hz)	291K

Table 3.5: AC Characteristics of Op-Amp from Frequency Response

Chapter 4

Conclusion

Through this research work, I have investigated the properties of amorphous Selenium as a direct conversion photoconductive layer and designed a custom instrumentation amplifier for readout in Skywater 130 nm CMOS. The CMOS amplifier is designed to meet the demands of high energy X-ray imaging applications and match the characteristics of previously fabricated and characterized amorphous Selenium. The Radiological Instrumentation Lab (RIL) at UC Santa Cruz possesses expertise in the fabrication and characterization of amorphous Selenium, as well as post processing techniques to hybridize an a-Se detection layer onto CMOS readout integrated circuits. In the past, the RIL group has faced high CMOS IC development costs and relied on readout circuits from external vendors, which has limited the ability to customize the system for the desired application specifications. My work in designing an instrumentation amplifier for detector readout in open source Skywater 130 nm CMOS opens the door to greater customization and optimization of readout integrated circuits at a low

cost.

As expected, the instrumentation amplifier meets the desired system specification in some areas and needs further optimization in others. The amplifier has a high unity-gain bandwidth, which can help achieve high frame rates in the overall integrated imager system. As a next step, the noise characteristics of the amplifier can be further investigated and optimized to ensure it meets target input noise specs. Future work to be done is a noise analysis and optimization for the op-amp, as well as simulating the performance of the CMOS pixel and readout amplifier together. Finally, fabrication of a CMOS pixel detector and post-processing to deposit the a-Se sensor layer can be done to fully integrate and test the system.

Overall, hybrid a-Se/CMOS imager systems combine the best of both worlds: high quantum efficiency of amorphous Selenium and small pixel architecture of CMOS. As a result, we can work towards combining the advantages of amorphous Selenium with custom CMOS readout circuits to achieve high resolution direct-conversion imaging systems for biomedical applications.

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